NOVATEK
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Data Sheet

NT51008

1536 ch Source Driver with LVDS TCON

For 1024RGBx768/600 TFT LCD

V0.6

Preliminary Spec

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Revision History

NT51008 Specification Revision History			
Version	**Content**	**PAGE**	**Date**
0.6	Add no_clock detection Add DIMI for brightness control	4 9,12,42	2009/09/17
0.5	Reivse Pad Sequence Revise Pad Coordinate	9 42,43	2009/09/15
0.4	Add Appendix A : BIST pattern	52	2009/09/10
0.3	Modify Application Power Circuit Modify Chip Outline Dimension Modify Pad Coordinate	8 40,41 42,43,47,51	2009/09/03
0.2	Revise all	All	2009/08/06
0.1	Revise all	All	2009/03/04
0.0	New spec.	-	2009/02/18

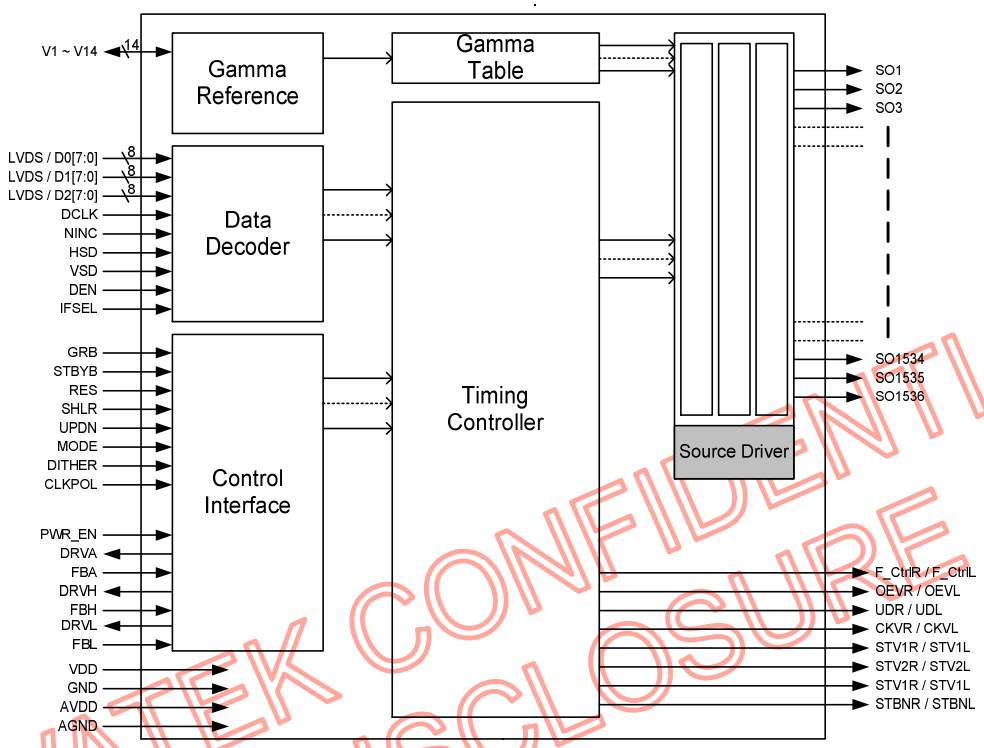
Features

- Special design for 1024RGBx600 TFT LCD Panel with LVDS/TTL interface
- Integrate 1536 channel source driver with single or dual gate function
- Support cascade function with bidirectional shift control (CMOS signal)
- Support panel resolution (HxV) : 1024(RGB) x 768 , 1024(RGB) x 600 , 800(RGB) x 600 , 800(RGB) x 480
- 8-bit resolution 256 gray-scale with Dithering (6 bits DAC + 2 bit FRC or HFRC)
- Support Pin Control function for Up/Down, Left/Right … control
- Power for digital circuit(VDD): 2.3V ~ 3.6V
- Power for analog circuit(AVDD): 6.5V ~ 13.5V
- Operating frequency : 71 MHz (Max.)
- Embedded Gamma Table for special custom request
- V1~V14 for adjusting Gamma correction
- 1 + 2 dot inversion architecture
- Built-In PWM controller for AVDD , Charge pump for VGH / VGL , and VCOM buffer
- Built-In CABC function
- Built-In AUTO pattern
- Built-In SDRRS function
- Support no_clock detection
- COG package
- Chip size = 25000um x 700um
- Output bump pitch = 15um

General Description

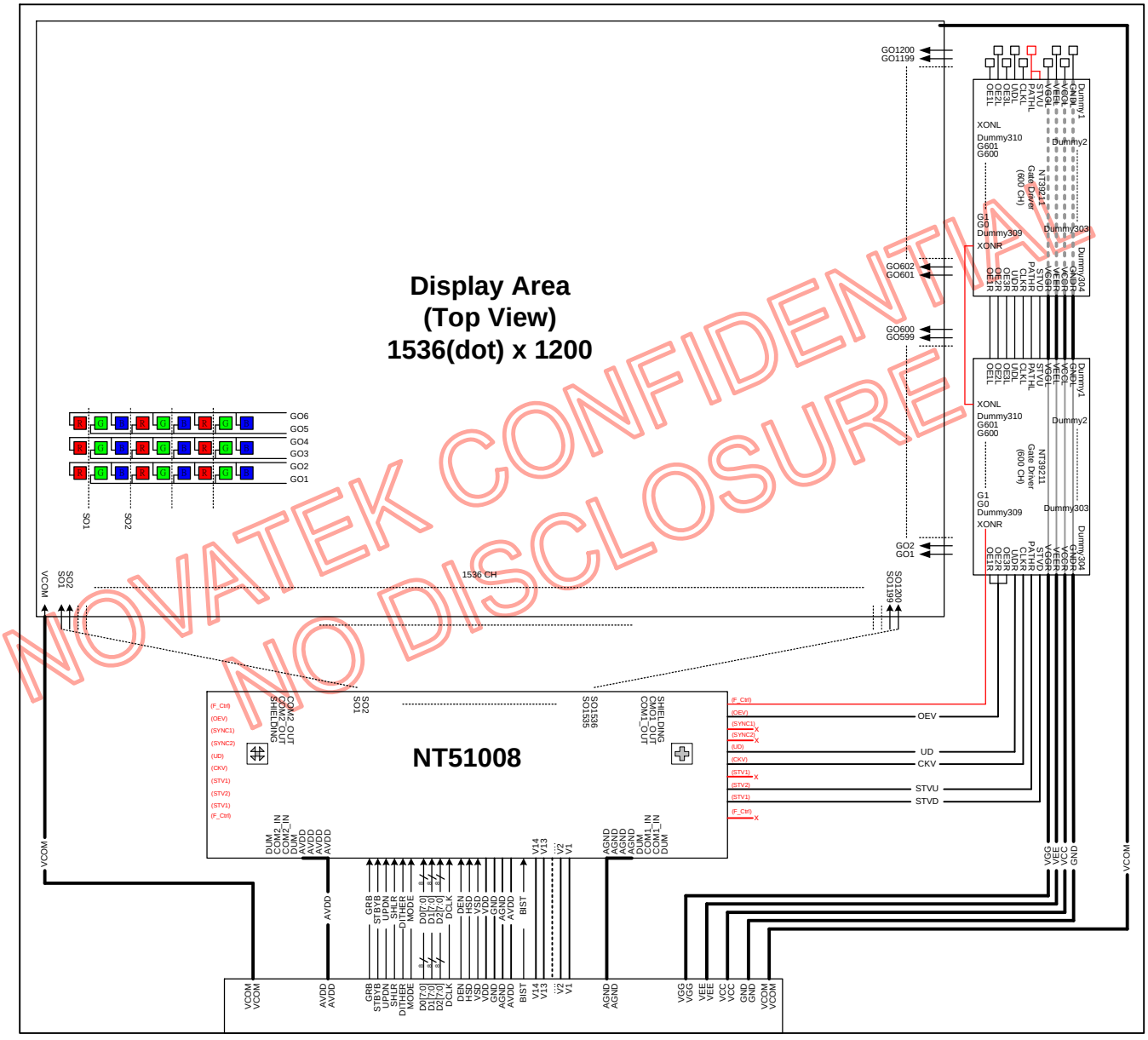
The NT51008 is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch dual gate mode source driver with LVDS and parallel RGB input interface . This chip is special designed for low cost UMPC application.

Function Block Diagram

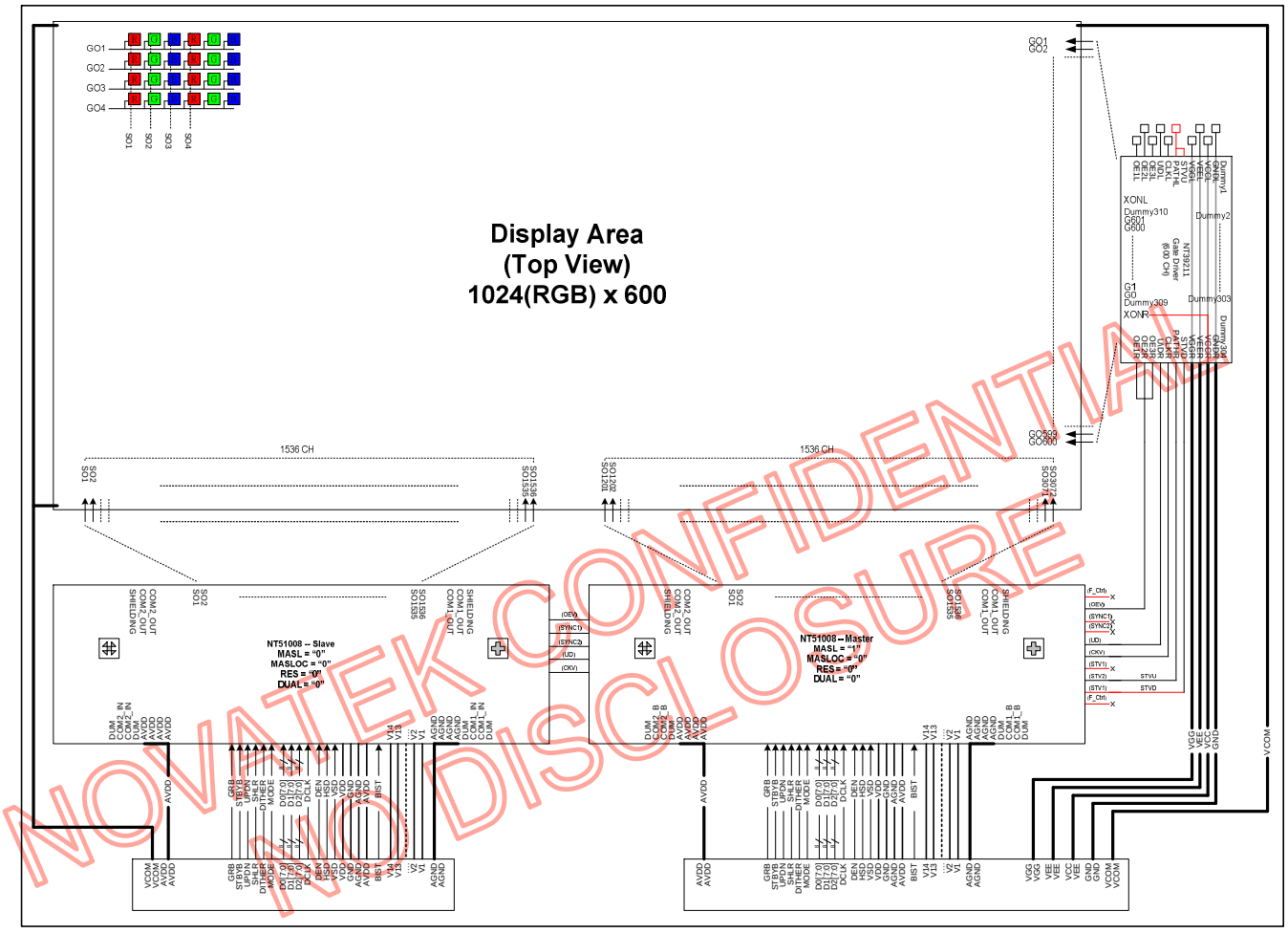


Application Block Diagram

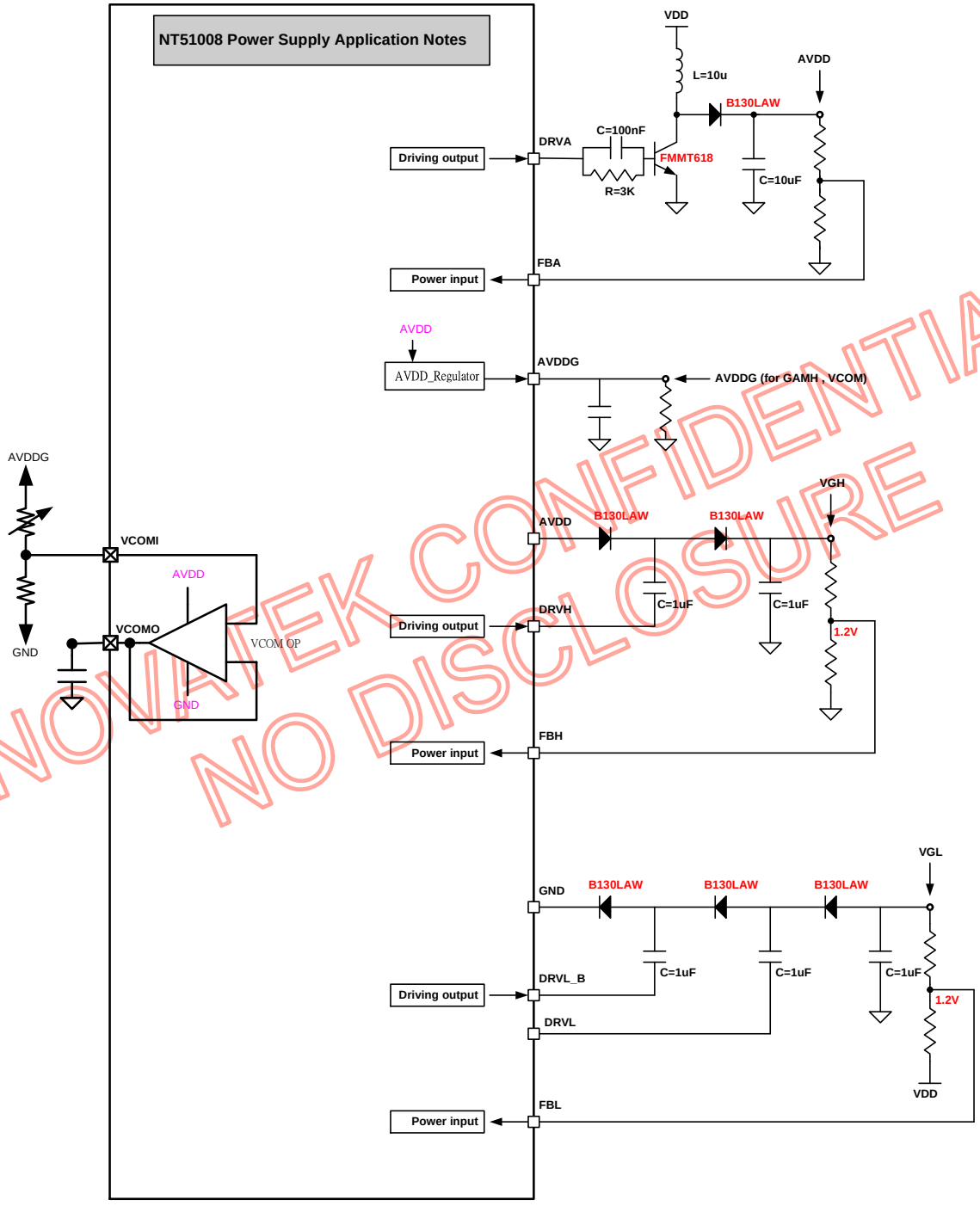
1. Dual Gate



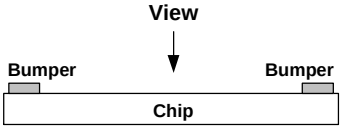
2. Cascade with Two-FPC



Application Power Circuit



Pad Sequence (bump side)



Pin Descriptions

<table>
<tr><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>D07~D00
D17~D10
D27~D20</td><td>I</td><td>LVDS or Parallel RGB data Input. Select by “IFSEL” pin.
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL = L</th><th>LVDS input mode
IFSEL = H</th></tr>
<tr><td>D2[0], D2[1]</td><td>B[0], B[1]</td><td>NIND0, PIND0</td></tr>
<tr><td>D2[2], D2[3]</td><td>B[2], B[3]</td><td>NIND1, PIND1</td></tr>
<tr><td>D2[4], D2[5]</td><td>B[4], B[5]</td><td>NIND2, PIND2</td></tr>
<tr><td>D2[6], D2[7]</td><td>B[6], B[7]</td><td>NIND3, PIND3</td></tr>
</table>
LVDS 6 bit data input : PIND[2:0], NIND[2:0].
D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; D[27:20] = B[7:0] data.
For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
Note : D07~D00 → SO1 , SO4 … SO1531 , SO1534
D17~D10 → SO2 , SO5 … SO1532 , SO1535
D27~D20 → SO3 , SO6 … SO1533 , SO1536
Please note the relation between RGB data and Color Filter sequence</td></tr>
<tr><td>DCLK</td><td>I</td><td>Clock Input pin for LVDS or TTL mode. Select by “IFSEL” pin.
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL = L</th><th>LVDS input mode
IFSEL = H</th></tr>
<tr><td>DCLK</td><td>DCLK</td><td>PINC</td></tr>
</table></td></tr>
<tr><td>NINC</td><td>I</td><td>Negative LVDS differential clock input.</td></tr>
<tr><td>HSD</td><td>I</td><td>Horizontal Sync input for TTL mode. Negative polarity.</td></tr>
<tr><td>VSD</td><td>I</td><td>Vertical Sync input for TTL mode. Negative polarity.</td></tr>
<tr><td>DEN</td><td>I</td><td>Data Input Enable. Active High to enable the data input bus under “DE Mode”.
Normally pull low.</td></tr>
<tr><td>MODE</td><td>I</td><td>DE / SYNC mode select under TTL mode. Normally pull high
H : DE mode. L : HSD/VSD mode.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>TTL and LVDS Interface selection. Normally pull low
IFSEL = L : TTL interface
IFSEL = H : LVDS interface</td></tr>
<tr><td>RES[1:0]</td><td>I</td><td>Display resolution selection. Normally pull low
RES[1:0] = “01”, for 1024(RGB)*768 display resolution(dual or cascade)
RES[1:0] = “00”, for 1024(RGB)*600 display resolution(dual or cascade) (Default)
RES[1:0] = “10”, for 800(RGB)*600 display resolution(dual or cascade)
(601~936 channel disable)
RES[1:0] = “11”, for 800(RGB)*480 display resolution(dual or cascade)
(601~936 channel disable)</td></tr>
<tr><td>DITHER</td><td>I</td><td>Dithering function enable control. Normally pull low
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function</td></tr>
<tr><td>HFRC</td><td>I</td><td>H-FRC selection. Normally pull low
HFRC = H : H-FRC enable
HFRC = L : FRC enable
If DITHER = “0” , disable dithering function(H-FRC and FRC disable)</td></tr>
<tr><td>DCLKPOL</td><td>I</td><td>Input clock edge selection. Normally pull low
CLKPOL = “1”, Latch data at DCLK rising edge.</td></tr>
</table>

		CLKPOL = “0”, Latch data at DCLK falling edge. (Default)
DUAL	I	Dual Gate function enables control. Normally pull high DUAL = “1”, Enable Dual Gate Function. (Default) DUAL = “0”, Disable Dual Gate Function Note: Cascade function will be disabled under “dual gate” mode!!
V1 ~ V14	I	When INTERNAL Gamma Table is used. GAMH tied to AVDDG , GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floaging , and V1~V14 are the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD .
GAMH	I	When using INTERNAL Gamma Table , tied to AVDDG . Otherwise floating.
GAML	I	When using INTERNAL Gamma Table , tied to GND . Otherwise floating.
GRB	I	Global reset pin. Active Low to enter Reset State. Normally pull high. Suggest to connecting with an RC reset circuit for stability.
STBYB	I	Standby mode, Normally pulled high. STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z
MASL	I	Master and Slave Mode selection. Normally pull high. MASL = ”H”, for Master mode. (Default Mode) MASL = ”L”, for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	I	Master location definition pin. Normally pull low. MASLOC = ”L”, Master locate on right side (Panel top view). (Default Mode) MASLOC = ”H”, Master locate on left side (Panel top view).
SHLR	I	Source Right or Left sequence control. Normally pull high. SHLR = “L”, shift left: last data = S1←S2←S3.....←S1200 = first data. SHLR = “H”, shift right: first data = S1→S2→S3.....→S1200 = last data.
UPDN	I	Gate Up or Down scan control. Normally pull low. UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver. UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.
BIST	I	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
NBW	I	Normally black or normally white setting. Normally pulled low. NBW = H : Normally black NBW = L : Normally white
REV	I	Controls whether the data of D00~D27 are inverted or not, normally pulled low. When “REV”=1 these data will be inverted. EX. “00” → “ 3F”, “07”→ “ 38”, “15”→ “2A”, and so on.
FRAME	I	Frame inverse or not select. FRAME = “1”, Uniform FRAME = “0”, Frame inverse (Default)

<table>
<tr><td>SEL[1:0]</td><td>I</td><td>Gate on sequence select. Normally pull low
<table>
<tr><th>SEL[0]</th><th>SEL[1]</th><th>Pin control function</th></tr>
<tr><td>1</td><td>1</td><td>Z+ Z</td></tr>
<tr><td>1</td><td>0</td><td>Z</td></tr>
<tr><td>0</td><td>1</td><td>Z</td></tr>
<tr><td>0</td><td>0</td><td>Z</td></tr>
</table></td></tr>
<tr><td>OEVR/OEVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>SYNC1R/SYNC1L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>SYNC2R/SYNC2L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>UDR/UDL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>CKVR/CKVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>STV1R/STV1L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STV2R/STV2L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STBNR/STBNL</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>F_CtrlR/F_CtrlL</td><td>O</td><td>Gate driver control signal (For special Gate on sequence).</td></tr>
<tr><td>CABC_EN[1:0]</td><td>I</td><td>CABC H/W enable pin. Normally pull low.
When CABC_EN=”00”, CABC OFF. (Default mode)
When CABC_EN=”01”, User interface Image.
When CABC_EN=”10”, Still Picture.
When CABC_EN=”11”, Moving Image.</td></tr>
<tr><td>DIMI</td><td>I</td><td>Brightness control signal. Normally pull high</td></tr>
<tr><td>DIMO</td><td>O</td><td>Backlight dimmer signal for external controller.
DIMO = “0”, Turn off external backlight controller
DIMO = “1”, Logical control signal to turn on external backlight controller
NOTE : If CABC OFF , DIMO = DIMI . Else DIMO is controlled by CABC</td></tr>
<tr><td>PINCTL</td><td>I</td><td>Enable pin control function. Normally pull high
PINCTL=”0”, Disable pin control function.
PINCTL=”1”, Enable pin control function.
NOTE: The related 3-wire control register bit control will be disabled under PINCTL=”1”.</td></tr>
<tr><td>CSB</td><td>I</td><td>Serial communication chip select. Normally pull low</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input. Normally pull low</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input. Normally pull low</td></tr>
<tr><td>AVDD</td><td>PI</td><td>Power supply for analog circuits</td></tr>
<tr><td>AGND</td><td>PI</td><td>Ground pins for analog circuits</td></tr>
<tr><td>VDD</td><td>PI</td><td>Power supply for digital circuits</td></tr>
<tr><td>GND</td><td>PI</td><td>Ground pins for digital circuits</td></tr>
<tr><td>VDD_LVDS</td><td>PI</td><td>LVDS power</td></tr>
<tr><td>GND_LVDS</td><td>PI</td><td>LVDS ground</td></tr>
<tr><td>PWR_EN</td><td>I</td><td>POWER enable. Normally pull low
PWR_EN = H , enable PWM , Charge pump and VCOM buffer
PWR_EN = L , disable PWM , Charge pump and VCOM buffer</td></tr>
<tr><td>FBA</td><td>VI</td><td>PWM controller feedback input. (for AVDD)</td></tr>
<tr><td>DRVA</td><td>O</td><td>PWM output driver signal for the boost converter (for AVDD)</td></tr>
<tr><td>FBH</td><td>VI</td><td>Charge Pump controller feedback input. (for VGH)</td></tr>
<tr><td>DRVH</td><td>O</td><td>Charge Pump driver signal for the boost converter (for VGH)</td></tr>
<tr><td>FBL</td><td>VI</td><td>Charge Pump controller feedback input. (for VGL)</td></tr>
</table>

DRVL	O	Charge Pump driver signal for the boost converter (for VGL)
DRVL_B	O	Inverse of DRVL(for VGL)
VCOMI	I	VCOM buffer in
VCOMO	O	VCOM buffer out
SO1~SO1536	O	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
COM1_IN COM1_OUT	S	Internal link together between input side and output side.
COM2_IN COM2_OUT	S	Internal link together between input side and output side.
TP	T	Test pin for Novatek only. Float these pins for normal operation.
SHIELDING	SH	IC Shielding pads. Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel.
DASHD	SH	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUM	D	Dummy pads. Those pins are floating pads.

Note:
I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, C: Capacitor pin.

NT51008 Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_IN	COM1_OUT
2	COM2_IN	COM2_OUT

Value of Wiring Resistance

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value(Ω)
AVDD	<5	RES0	<100
AGND	<5	RES1	<100
VDD	<5	SHLR	<100
GND	<5	UPDN	<100
V1~V14	<5	BIST	<100
DRVx	<5	MODE	<100
FBx	<5	DCLKPOL	<100
VCOMI	<5	DIMO	<100
VCOMO	<5	IFSEL	<100
D00~D07	<5	F_Ctrlx	<500
D10~D17	<5	OEVx	<500
D20~D27	<5	UDx	<500
DCLK	<5	CKVx	<500
NINC	<5	STV1x	<500
VSD	<20	STV2x	<500
HSD	<20	STBNx	<500
DEN	<20		
GRB	<100		
STBYB	<100		
DITHER	<100		

3-Wire Serial Port Interface

1. 3-Wire Command Format

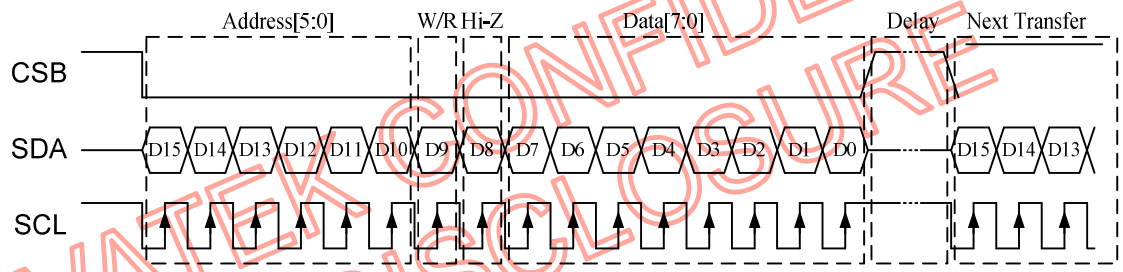
NT51008 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. NT51008 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing Diagram” for the detail timing.



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	DATA (Issue by 3-Wire engine)							

2. 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for NT51008. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

R0: System Control Register

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S960=First data. SHLR="1", Shift right: First data=S1->S2->S3 … ->S960=Last data. (Default)
	R0[6]	Reserved
PWR_EN	R0[7]	POWER enable. PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer (Default)

R1: System Control Register

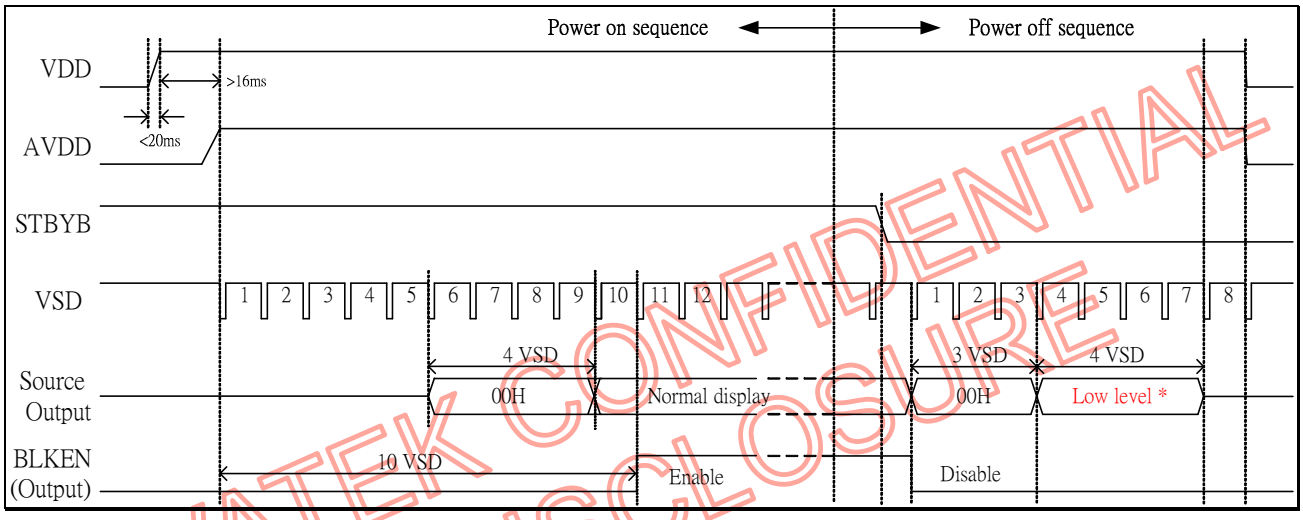
Designation	Address	Description
		Reserved
RES[1:0]	R1[2:1]	Display resolution selection. RES[1:0] = “01”, for 1024(RGB)*768 display resolution(dual or cascade) RES[1:0] = “00”, for 1024(RGB)*600 display resolution(dual or cascade) (Default) RES[1:0] = “10”, for 800(RGB)*600 display resolution(dual or cascade) (601~936 channel disable) RES[1:0] = “11”, for 800(RGB)*480 display resolution(dual or cascade) (601~936 channel disable)
BIST	R1[3]	Normal Operation/BIST pattern select. BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation (Default)
DITHER	R1[4]	Dithering function enable control. DITHER = “1”, Enable internal dithering function DITHER = “0”, Disable internal dithering function (Default)
HFRC	R1[5]	H-FRC selection. HFRC = H : H-FRC enable HFRC = L : FRC enable (Default) If DITHER = “0” , disable dithering function(H-FRC and FRC disable)
CABC_EN[1:0]	R1[7:6]	CABC H/W enable pin. Normally pull low. When CABC_EN=”00”, CABC OFF. (Default mode) When CABC_EN=”01”, User interface Image. When CABC_EN=”10”, Still Picture. When CABC_EN=”11”, Moving Image.

Function Description

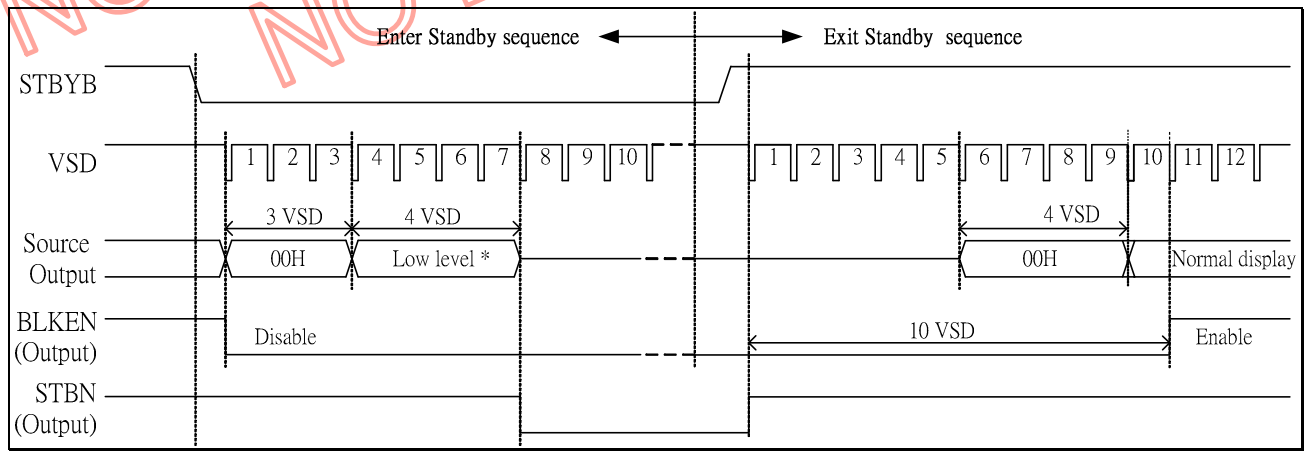
1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

Power-On/Off Timing Sequence:



Enter and Exit Standby Mode Sequence:



***Note :** Low level = 3FH , when NBW = L (Normally white)
Low level = 00H , when NBW = H (Normally black)

2. Input Data VS Output Channels

1. DUAL="0"

(1) SHLR="1" , right shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	First data			→	Last data		
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

(2) SHLR="0", left shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	Last data			←	First data		
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

2. DUAL="1"

(1) SHLR="1" , right shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	First data			→	Last data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20

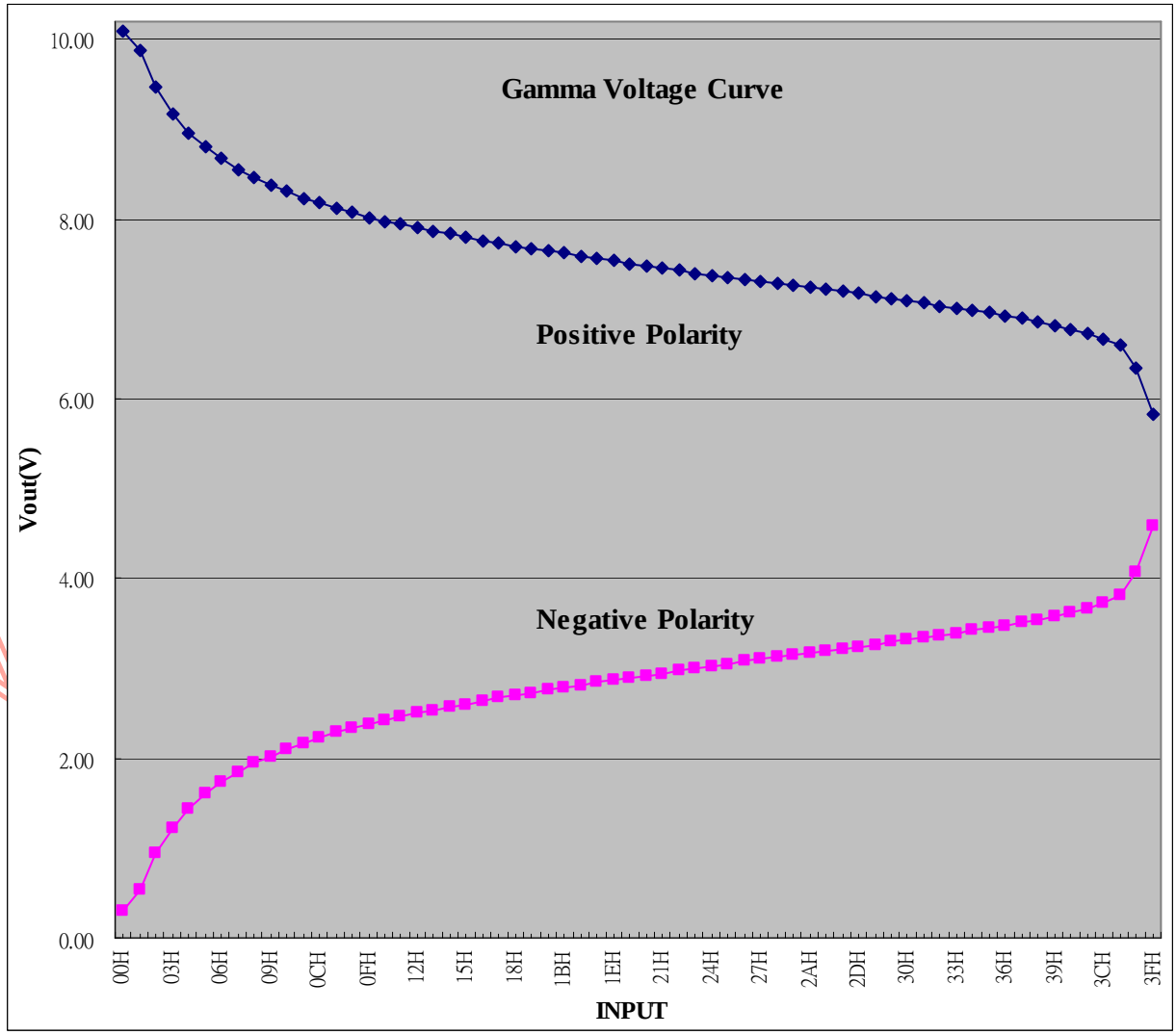
(2) SHLR="0", left shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	Last data			←	First data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20

3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

Gamma Tables very for each customer. Contact Novatek for more detail information.



Remark:

AVDD-1 ≥ V1 ≥ V2≥ V3 ≥ V4 ≥ V5 ≥ V6 ≥ V7; V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ V14 ≥ AGND+0.1V

4. Input Data and Output Voltage Reference Table

Note: Gamma Tables vary for each custom. Contact Novatek for more detailed information.

@AVDD=10.4V

Chip Version	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	[unit]
NT51008	10.003	9.783	7.945	7.487	7.161	6.597	6.073	4.869	4.327	3.38	2.895	2.362	0.432	0.207	V

Negative Polarity

Data	Negative Polarity
3FH	AVDD X 0.468
3EH	AVDD X 0.416
3DH	AVDD X 0.389
3CH	AVDD X 0.379
3BH	AVDD X 0.372
3AH	AVDD X 0.366
39H	AVDD X 0.36
38H	AVDD X 0.355
37H	AVDD X 0.35
36H	AVDD X 0.346
35H	AVDD X 0.342
34H	AVDD X 0.339
33H	AVDD X 0.335
32H	AVDD X 0.332
31H	AVDD X 0.328
30H	AVDD X 0.325
2FH	AVDD X 0.322
2EH	AVDD X 0.319
2DH	AVDD X 0.316
2CH	AVDD X 0.313
2BH	AVDD X 0.31

Data	Negative Polarity
2AH	AVDD X 0.308
29H	AVDD X 0.305
28H	AVDD X 0.302
27H	AVDD X 0.299
26H	AVDD X 0.297
25H	AVDD X 0.294
24H	AVDD X 0.291
23H	AVDD X 0.288
22H	AVDD X 0.284
21H	AVDD X 0.281
20H	AVDD X 0.278
1FH	AVDD X 0.276
1EH	AVDD X 0.273
1DH	AVDD X 0.271
1CH	AVDD X 0.268
1BH	AVDD X 0.265
1AH	AVDD X 0.262
19H	AVDD X 0.259
18H	AVDD X 0.256
17H	AVDD X 0.253
16H	AVDD X 0.25

Data	Negative Polarity
15H	AVDD X 0.246
14H	AVDD X 0.243
13H	AVDD X 0.239
12H	AVDD X 0.235
11H	AVDD X 0.231
10H	AVDD X 0.227
0FH	AVDD X 0.222
0EH	AVDD X 0.218
0DH	AVDD X 0.213
0CH	AVDD X 0.207
0BH	AVDD X 0.201
0AH	AVDD X 0.194
09H	AVDD X 0.187
08H	AVDD X 0.179
07H	AVDD X 0.17
06H	AVDD X 0.159
05H	AVDD X 0.146
04H	AVDD X 0.13
03H	AVDD X 0.109
02H	AVDD X 0.081
01H	AVDD X 0.042
00H	AVDD X 0.02

Positive Polarity

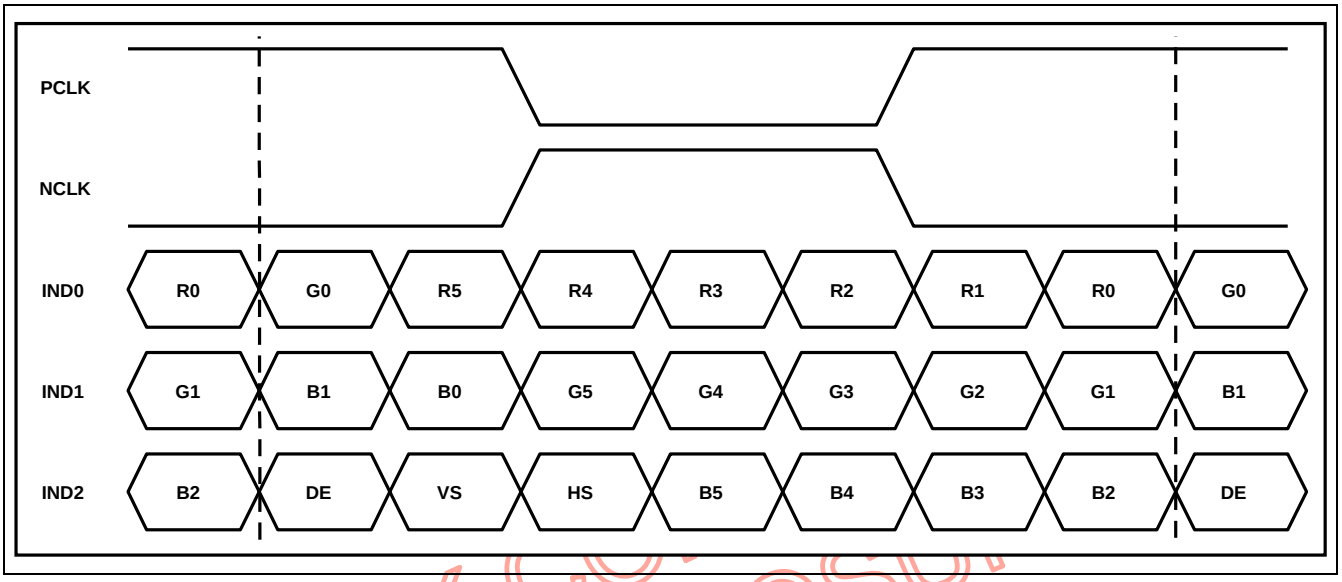
Data	Positive Polarity
00H	AVDD X 0.962
01H	AVDD X 0.941
02H	AVDD X 0.903
03H	AVDD X 0.875
04H	AVDD X 0.856
05H	AVDD X 0.84
06H	AVDD X 0.828
07H	AVDD X 0.817
08H	AVDD X 0.808
09H	AVDD X 0.801
0AH	AVDD X 0.794
0BH	AVDD X 0.788
0CH	AVDD X 0.782
0DH	AVDD X 0.777
0EH	AVDD X 0.772
0FH	AVDD X 0.768
10H	AVDD X 0.764
11H	AVDD X 0.76
12H	AVDD X 0.757
13H	AVDD X 0.753
14H	AVDD X 0.75

Data	Positive Polarity
15H	AVDD X 0.747
16H	AVDD X 0.744
17H	AVDD X 0.741
18H	AVDD X 0.739
19H	AVDD X 0.736
1AH	AVDD X 0.733
1BH	AVDD X 0.731
1CH	AVDD X 0.728
1DH	AVDD X 0.726
1EH	AVDD X 0.724
1FH	AVDD X 0.722
20H	AVDD X 0.72
21H	AVDD X 0.718
22H	AVDD X 0.716
23H	AVDD X 0.713
24H	AVDD X 0.711
25H	AVDD X 0.708
26H	AVDD X 0.706
27H	AVDD X 0.705
28H	AVDD X 0.703
29H	AVDD X 0.701

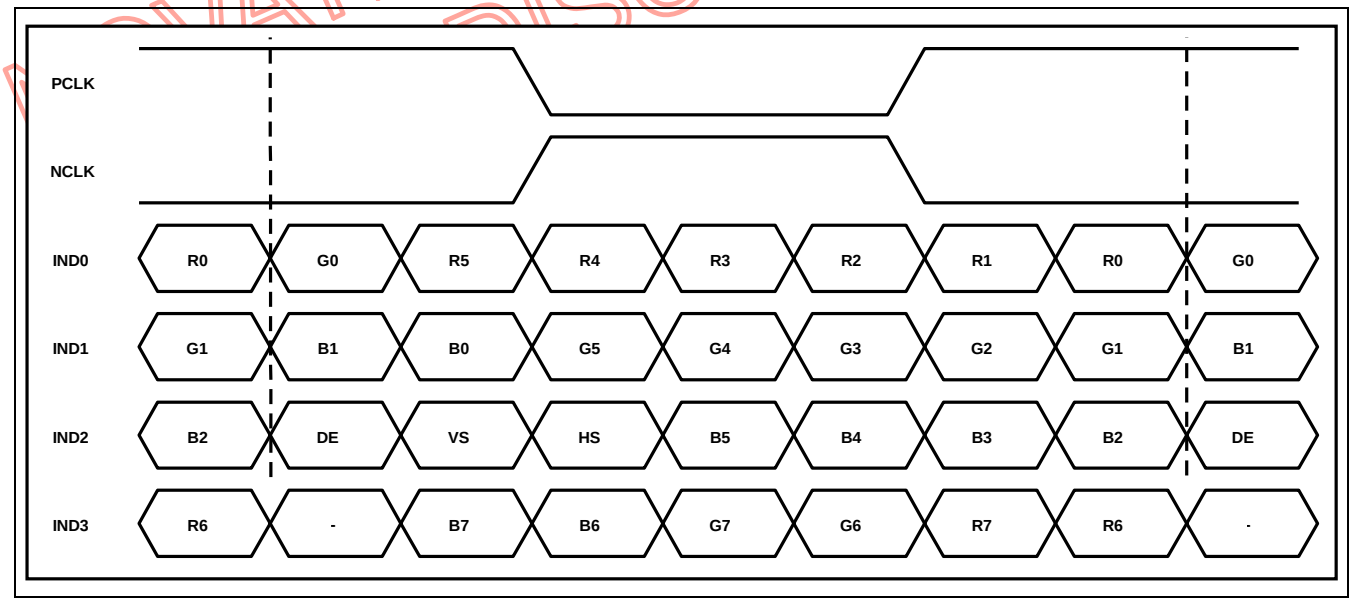
Data	Positive Polarity
2AH	AVDD X 0.699
2BH	AVDD X 0.697
2CH	AVDD X 0.695
2DH	AVDD X 0.694
2EH	AVDD X 0.692
2FH	AVDD X 0.69
30H	AVDD X 0.689
31H	AVDD X 0.687
32H	AVDD X 0.685
33H	AVDD X 0.683
34H	AVDD X 0.682
35H	AVDD X 0.68
36H	AVDD X 0.678
37H	AVDD X 0.676
38H	AVDD X 0.674
39H	AVDD X 0.672
3AH	AVDD X 0.669
3BH	AVDD X 0.666
3CH	AVDD X 0.662
3DH	AVDD X 0.656
3EH	AVDD X 0.634
3FH	AVDD X 0.584

Data Input Format for LVDS

6bit LVDS input (DITHER='L')

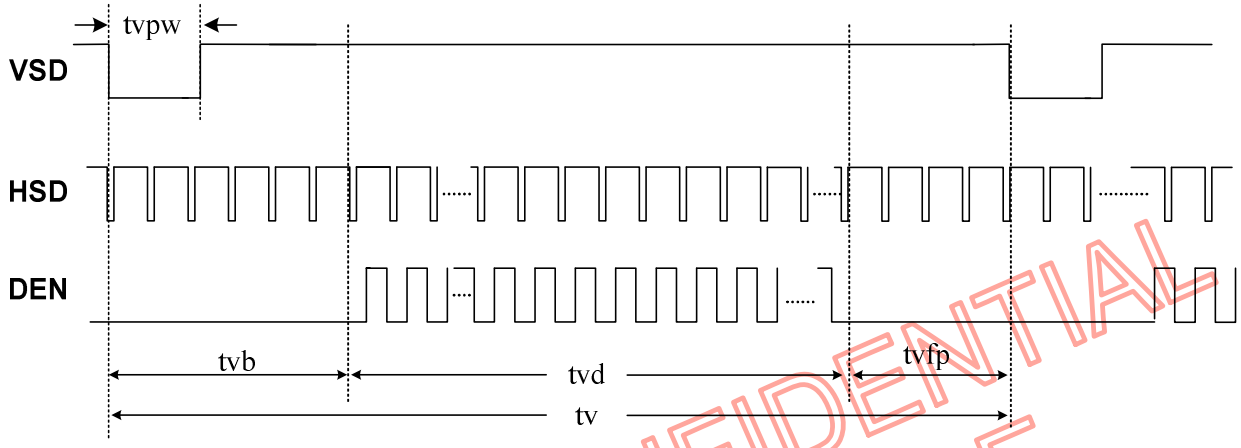


8-bit LVDS input

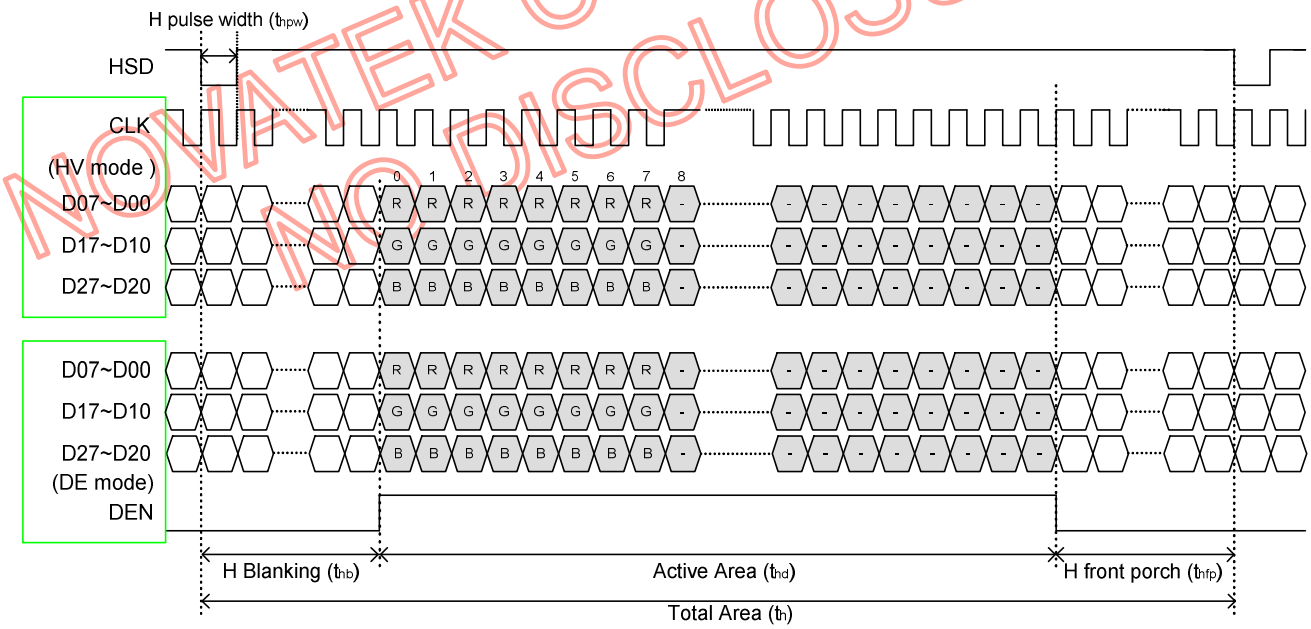


Data Input Format for TTL

Vertical input timing



Horizontal input timing



Parallel RGB input timing table

For 1024x768 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	52	65	71	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		768		H
VSYNC period time	tv	778	806	845	H
VSYNC blanking	tvb+tvfp	10	38	77	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			57	65	70.5	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		768		H
VSYNC period time	tv	792	806	840	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	1	15	49	H

For 1024x600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	1	12	127	H

For 800x600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	32.6	39.6	62.4	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	1000	1300	DCLK
HSYNC blanking	thb+thfp	90	200	500	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	660	800	H
VSYNC blanking	tvb+tvfp	10	60	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			34.5	39.6	50.4	MHz
1 Horizontal Line		th	900	1000	1200	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	112	312	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	640	660	700	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	39	39	39	H
VSYNC Front porch (tvfp)	tvfp	1	21	61	H

For 800x480 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	26.2	29.2	54.6	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	928	1300	DCLK
HSYNC blanking	thb+thfp	90	128	500	DCLK
Vertical display area	tvd		480		H
VSYNC period time	tv	490	525	700	H
VSYNC blanking	tvb+tvfp	10	45	220	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			27.7	29.2	39.6	MHz
1 Horizontal Line		th	900	928	1100	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	40	212	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		480		H
VSYNC period time	tv	513	525	600	H
VSYNC pulse width	tvpw	1	-	3	H
VSYNC Blanking (tvb)	tvb	32	32	32	H
VSYNC Front porch (tvfp)	tvfp	1	13	88	H

Absolute Maximum Ratings

	MIN.	MAX.	UNIT
Logic supply voltage, VDD **Digital input voltage**	-0.5	5	V
Analog supply voltage, AVDD **Gamma voltage , V1~V14** **OUT1 ~ OUT1536**	-0.5	15	V

TEMPREATURE

	MIN.	MAX.	UNIT
Operating temperature	-20	85	°C
Storage temperature	-55	125	°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

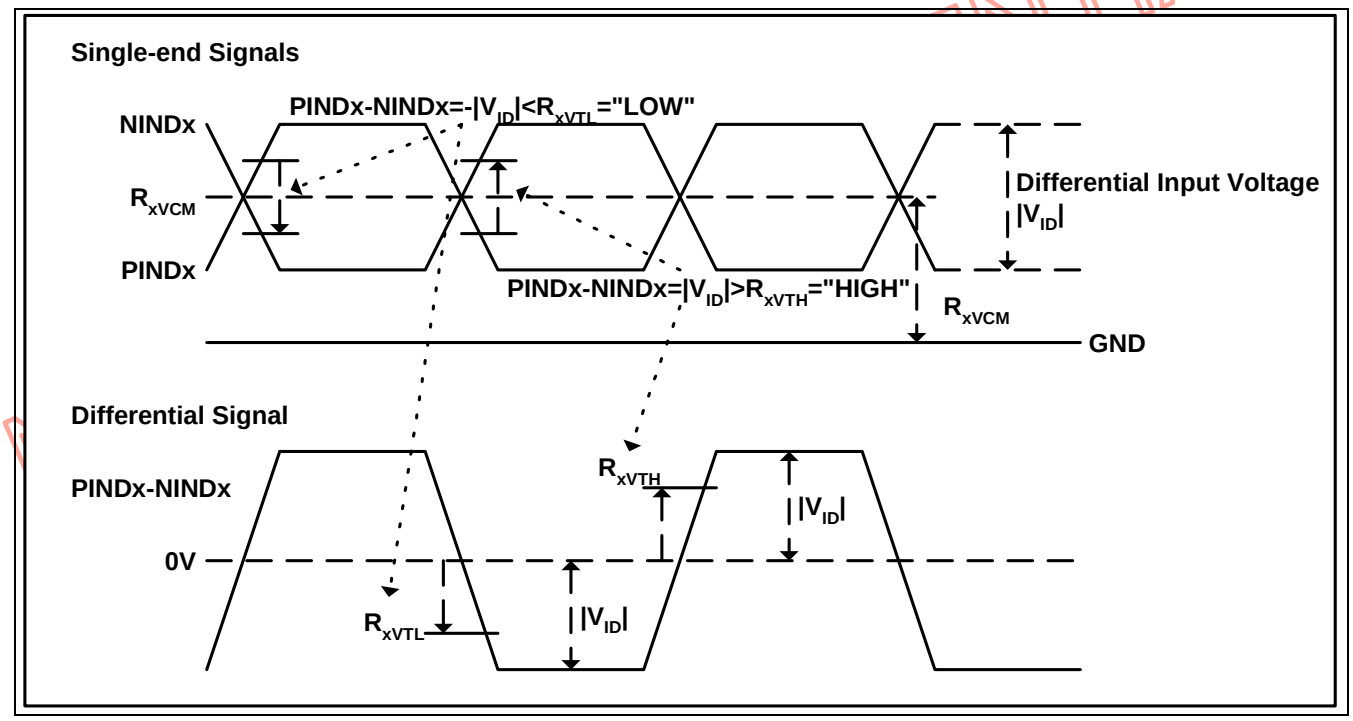
DC Electrical Characteristics

(VDD= 2.3 to 3.6V, AVDD= 6.5 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)
TTL mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Low level input voltage	Vil	0	-	0.3xVDD	V	For the digital circuit
High level input voltage	Vih	0.7xVDD	-	VDD	V	For the digital circuit
Input leakage current	Ii	-	-	±1	μA	For the digital circuit
High level output voltage	Voh	VDD-0.4	-	-	V	Ioh= -400μA
Low level output voltage	Vol	-	-	GND+0.4	V	Iol= +400μA
Pull low/high resistor	Ri	200K	250K	300K	ohm	For the digital input pin @ VDD=3.3V
Digital Operation current	Idd	-	8 (TBD)	10 (TBD)	mA	Fclk=65 MHz, FLD=50KHz, VDD=3.3V
Digital Stand-by current	Ist1	-	10 (TBD)	50 (TBD)	μA	Clock & all functions are stopped
Analog Operating Current	Idda	-	10 (TBD)	12 (TBD)	mA	No load, Fclk=65MHz, FLD=50KHz @ AVDD=10V,V1=8V, V14=0.4V
Analog Stand-by current	Ist2	-	10 (TBD)	50 (TBD)	μA	No load, Clock & all functions are stopped
Input level of V1 ~ V7	Vref1	0.4* AVDD	-	AVDD-0.1	V	Gamma correction voltage input
Input level of V8 ~ V14	Vref2	0.1	-	0.6* AVDD	V	Gamma correction voltage input
Output Voltage deviation	Vod1	-	±20	±35	mV	Vo = AGND+0.1V ~ AGND+0.5V & Vo = AVDD-0.5V ~ AVDD-0.1V
Output Voltage deviation	Vod2	-	±15	±20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Output Voltage Offset between Chips	Voc	-	-	±20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	SO1 ~ SO1536
Sinking Current of Outputs	IOLy	80	-	-	uA	SO1 ~ SO1536; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	SO1 ~ SO1536; Vo=13.4V v.s 12.5V , AVDD=13.5V
Resistance of Gamma Table	Rg	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn: Internal gamma resistor

LVDS mode (Receiver Differential Input: PIND0~PIND3, NIND0~NIND3, PINC, NINC)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{xVTH}			+0.1	V	R_{xVCM} =1.2V
Differential input low threshold voltage	R_{xVTL}	-0.1			V	
Input voltage range (singled-end)	R_{XVIN}	0		2.4	V	
Differential input common mode voltage	R_{xVCM}	$\|V_{ID}\|/2$		$2.4-\|V_{ID}\|/2$	V	
Differential input voltage	$\|V_{ID}\|$	0.2		0.6	V	
Differential input leakage current	RV_{xliz}	-10		+10	uA	



Power(TBD)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Base drive current for PWM	IDRV	-	-	60	mA	DRVA = 0.7V
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feed back voltage for PWM	VFB	0.55	0.6	0.65	V	
Duty cycle maximum	Dmax	-	-	85	%	
VCOM buffer input voltage	VCOMI	1	-	AVDD	V	
VCOM buffer output voltage	VCOMO	VCOMI – 0.2	VCOMI	VCOMI+ 0.2	V	
VCOM buffer output current	IVCOM	-	-	10	mA	VCOMO = 5V vs 4.9V

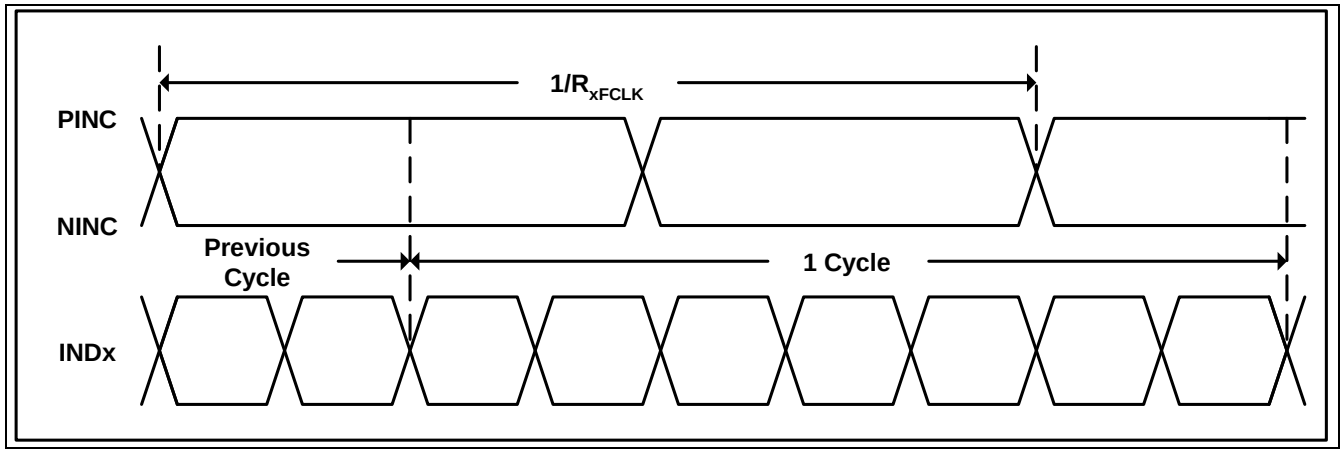
AC Electrical Characteristics

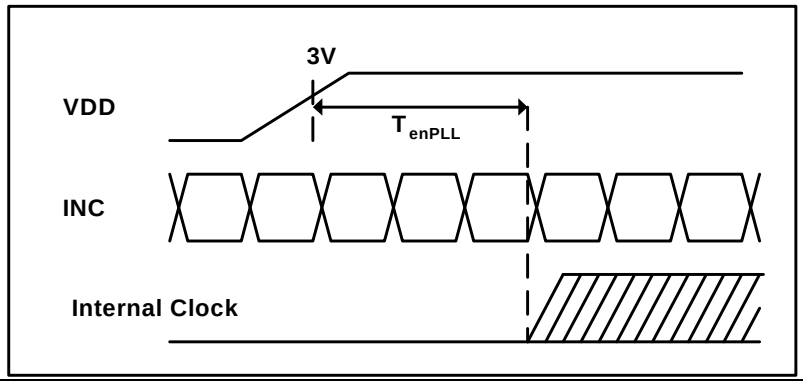
(VDD= 2.3 to 3.6V, AVDD= 6.5 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)
TTL mode

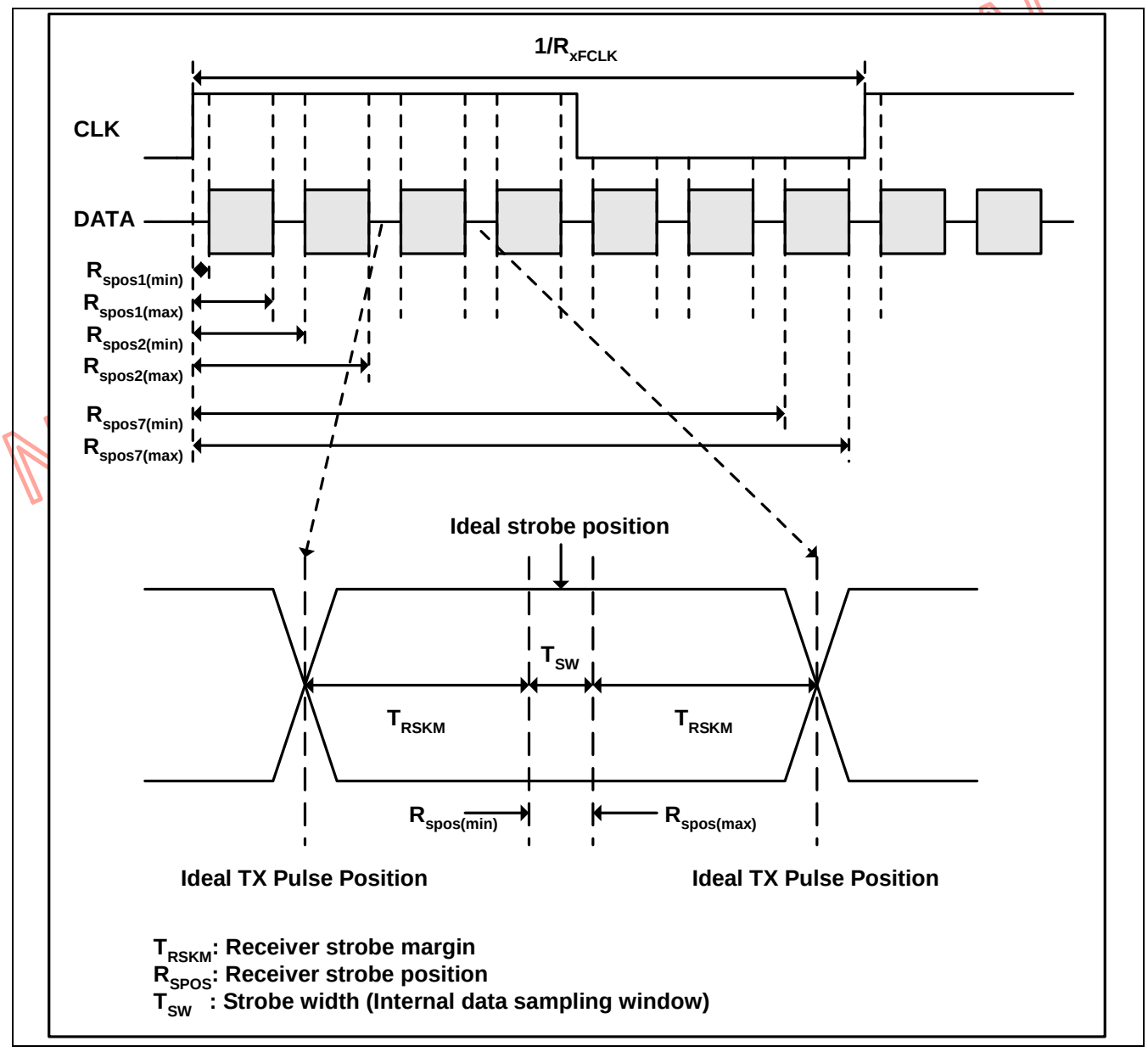
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power On Slew rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	T_{Rst}	50	-	-	us	DCLK = 65MHz
DCLK cycle time	Tcph	14			ns	
DCLK pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	5	-	-	ns	
VSD hold time	Tvhd	5	-	-	ns	
HSD setup time	Thst	5	-	-	ns	
HSD hold time	Thhd	5	-	-	ns	
Data set-up time	Tdsu	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	Tdhd	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	Tesu	5	-	-	ns	
DE hold time	Tehd	5	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target voltage. CL=90pF, R=10K ohm (Cascade)
				3		Dual gate

LVDS mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	R_{xFCLK}	20		71	MHz	
Input data skew margin	T_{RSKM}	500			pS	$\|V_{ID}\|$ = 400mV R_{xVCM} = 1.2V R_{xFCLK} = 71 MHz
Output clock duty	T_{CODUTY}		50		%	
PLL wake-up time	T_{enPLL}			150	uS	







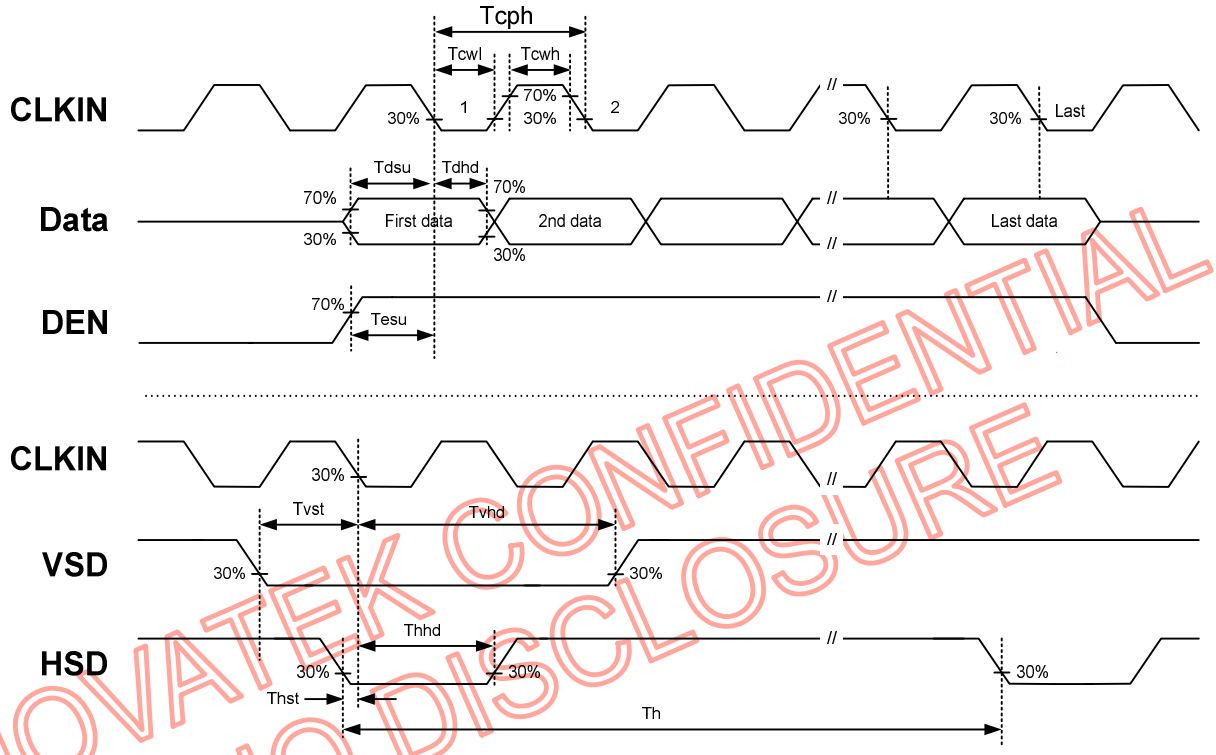
T_{RSKM}: Receiver strobe margin
R_{SPOS}: Receiver strobe position
T_{SW} : Strobe width (Internal data sampling window)

Output Timing Table

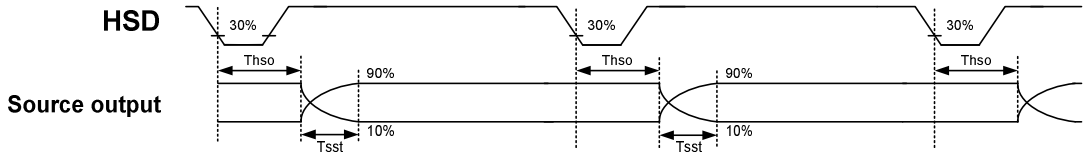
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK Frequency	Fclk	-	65	71	MHz	VDD = 2.3V ~3.6V
DCLK Cycle Time	Tclk	14.1	15.4	-	ns	
DCLK Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	DCLK	
Time from HSD to LD	Thld	-	64	-	DCLK	
Time from HSD to STV	Thstv	-	2	-	DCLK	
Time from HSD to CKV	Thckv	-	20	-	DCLK	
Time from HSD to OEV	Thoev	-	4	-	DCLK	
LD Pulse Width	Twld	-	10	-	DCLK	
CKV Pulse Width	Twckv	-	66	-	DCLK	
OEV Pulse Width	Twoev	-	74	-	DCLK	

Timing Diagram

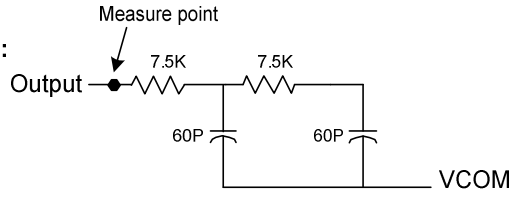
1. Input Clock and Data Timing Diagram



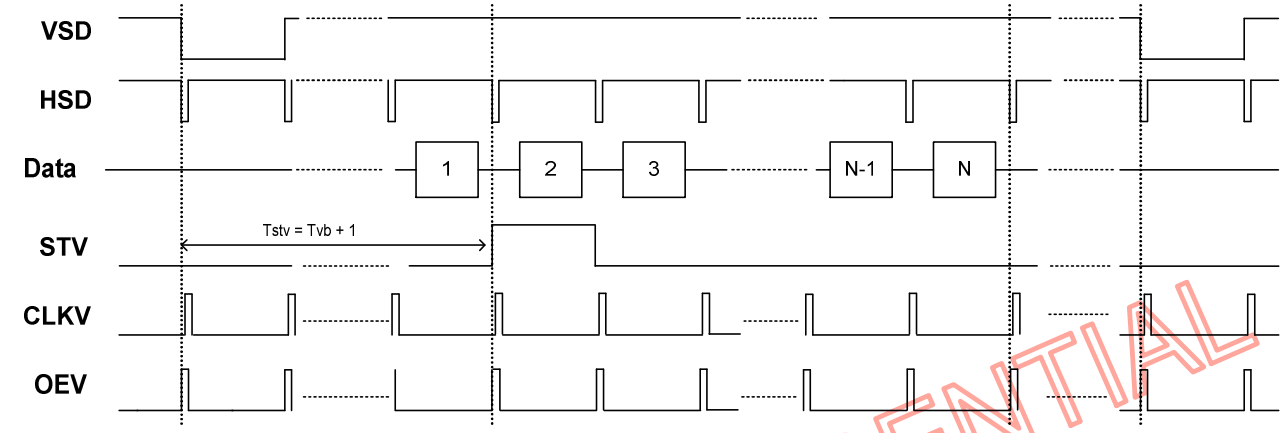
2. Source Output Timing Diagram (Cascade)



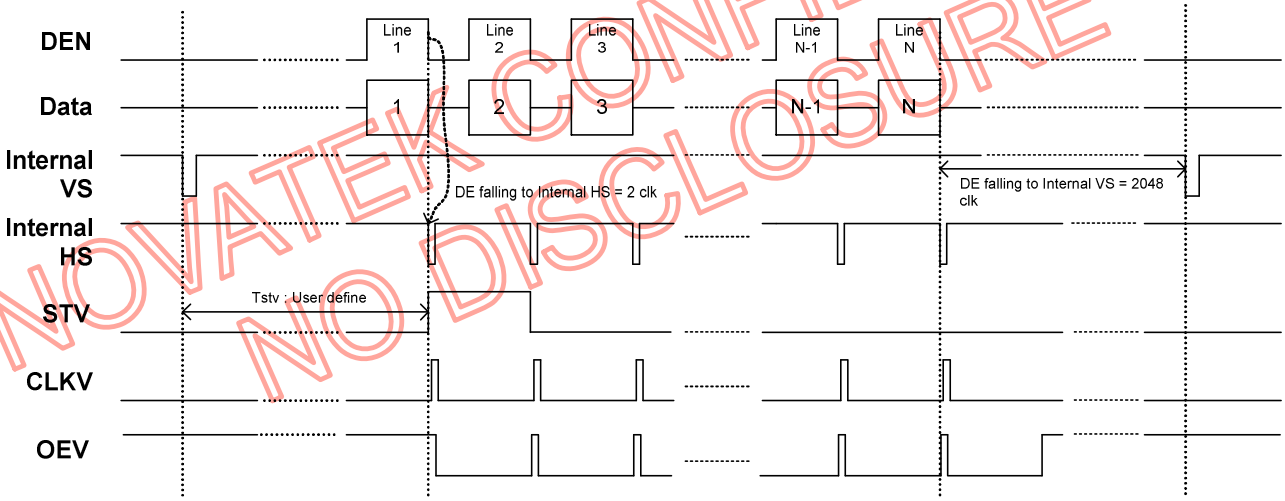
Output load condition :



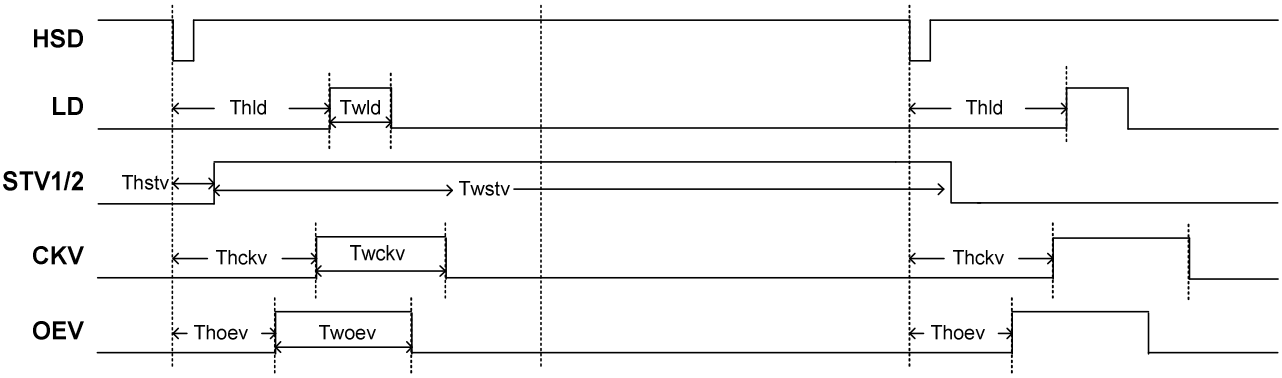
3. Vertical Timing Diagram HV (Cascade)



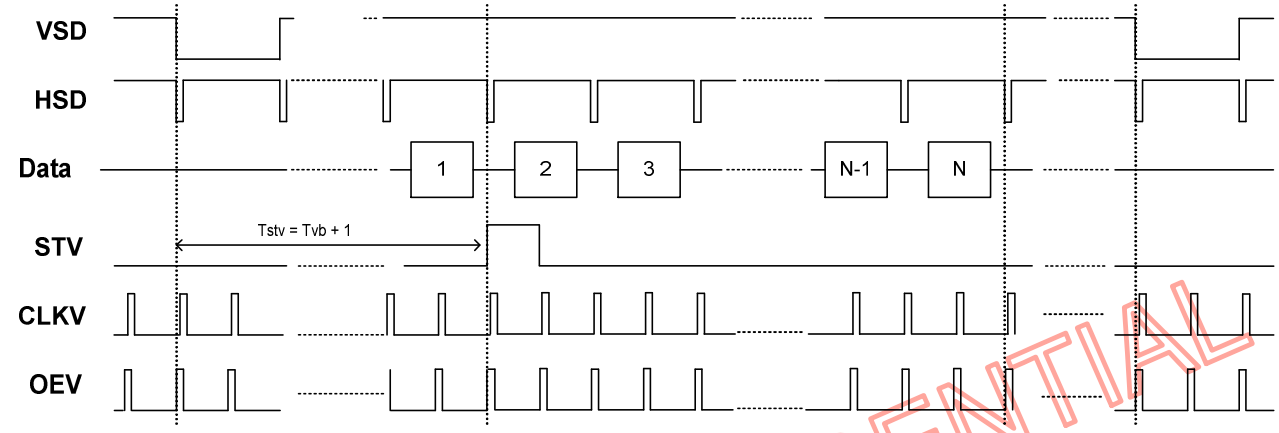
4. Vertical Timing Diagram DE (Cascade)



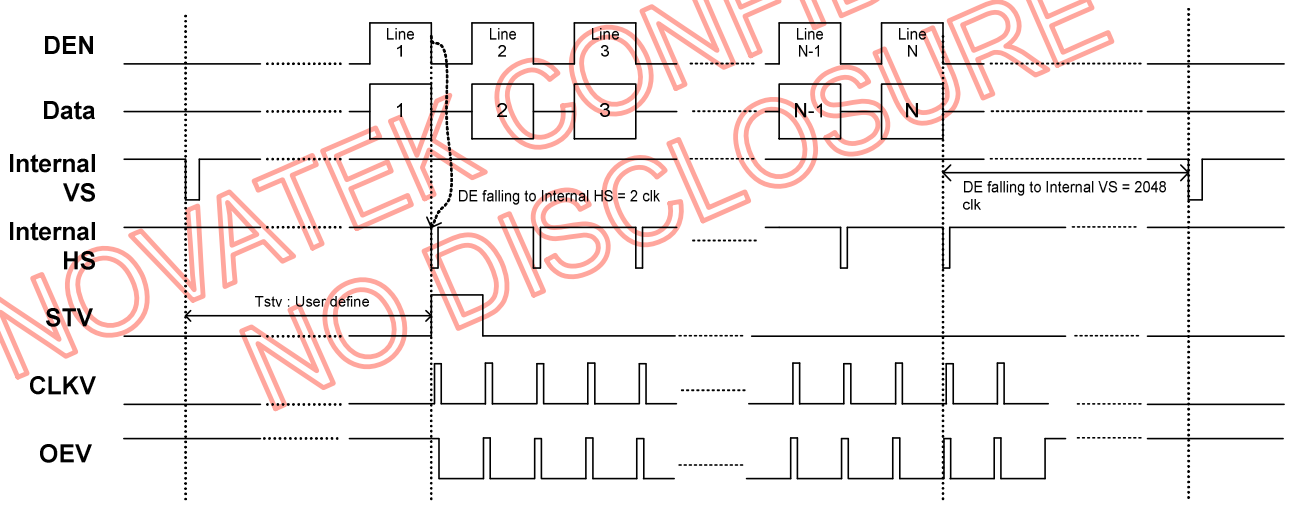
5. Gate output timing diagram (Cascade)



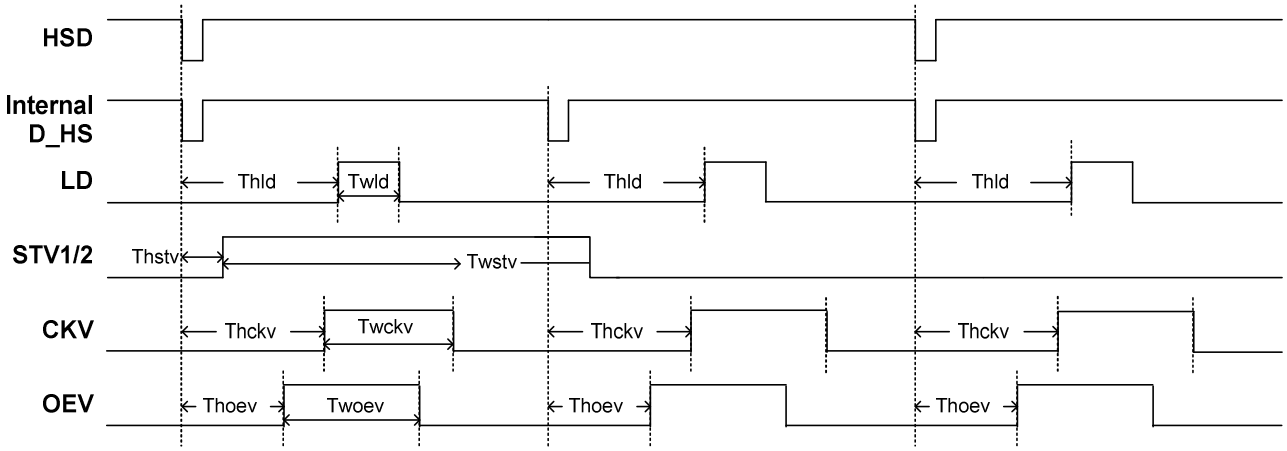
6. Vertical Timing Diagram HV (Dual Gate)



7. Vertical Timing Diagram DE (Dual Gate)



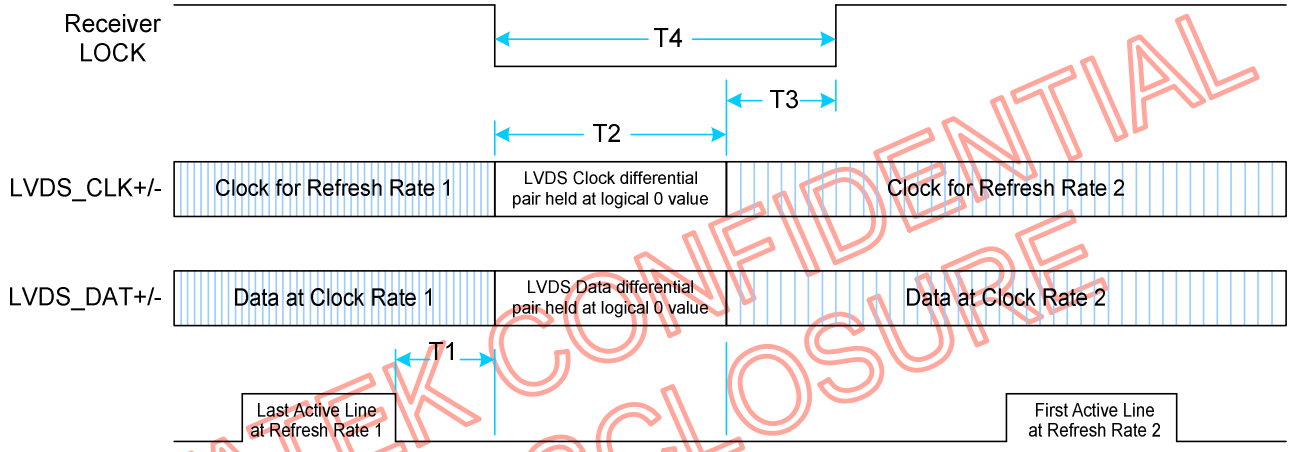
8. Gate output timing diagram (Dual Gate)



9. SDRRS timing diagram

SDRRS (seamless display refresh rate switching)

When Showing the still picture, it is accept to reduce the refresh rate from 60Hz to low refresh rate (for example 40Hz). The purpose is mainly for power saving. INTEL defined a timing chart switch between different refresh rate. Following this timing chart, the switch between different refresh rates is seamless for end user.



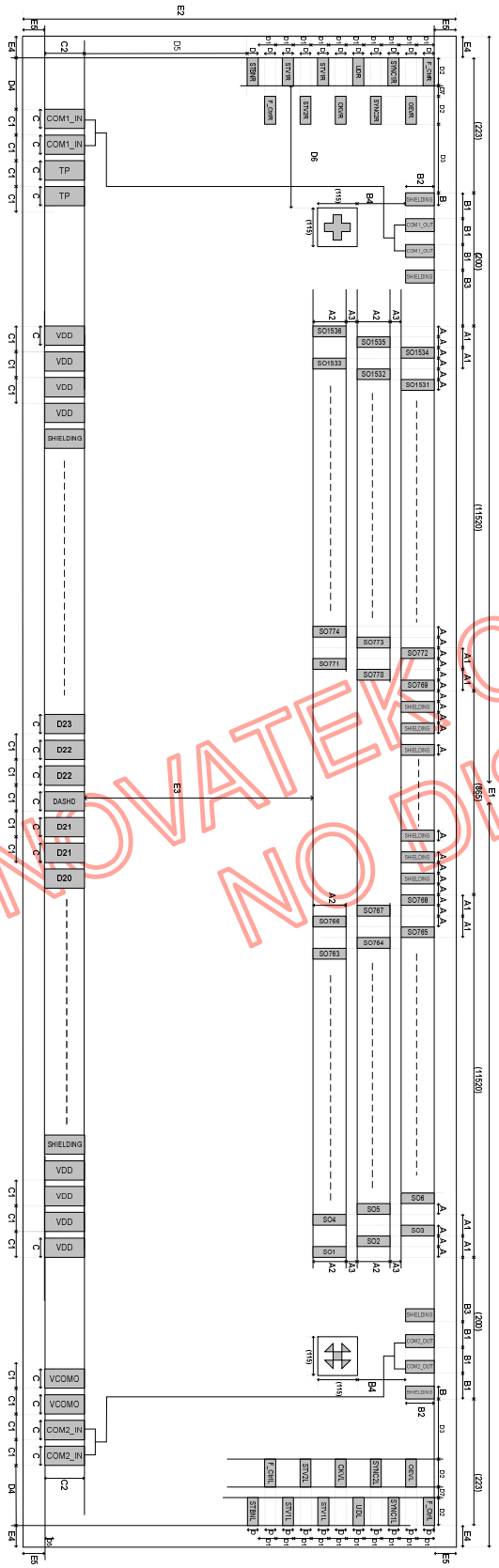
T1 - Min delay from start of vert blank to start of timing change: 2 lines (HSYNC periods)

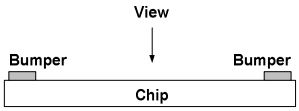
T2 - Max delay for clock to transition to new frequency: 100us

T3 - Max receiver lock delay from stable clock: Display specific (TBD)

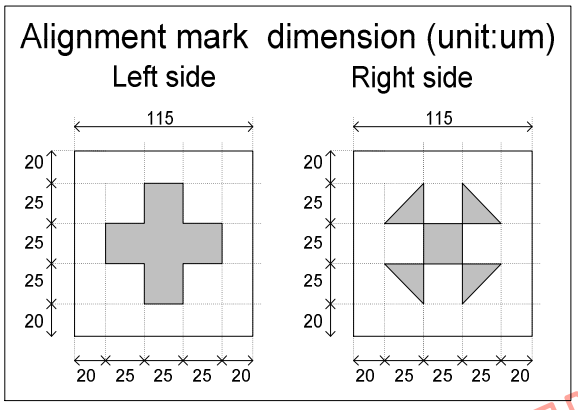
T4 - Max period during which panel maintains display (T2+T3): Display specific (TBD)

Chip Outline Dimensions





Alignment Mark



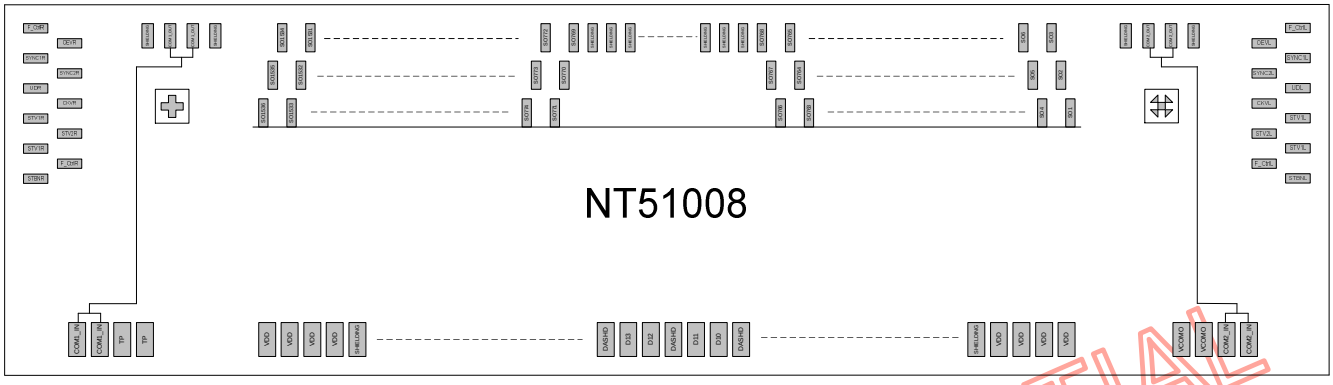
Pad Information

Symbol	Dimension (um)
A	15
A1	30
A2	120
A3	20
B	30
B1	50
B2	70
B3	50
B4	50
C	65
C1	85
C2	120

Symbol	Dimension (um)
D	30
D1	40
D2	80
D3	43
D4	33
D5	36
D6	154
D7	20
E1	25000
E2	700 (TBD)*
E3	216(TBD)*
E4	57(max)
E5	57(max)

***Note: Chip dimension includes scribe line.**

Pad Coordinate



Pad	TextName	CX	CY
1	COM1_IN	-12377.5	-233
2	COM1_IN	-12292.5	-233
3	TP	-12207.5	-233
4	TP	-12122.5	-233
5	TP	-12037.5	-233
6	TP	-11952.5	-233
7	SHIELDING	-11867.5	-233
8	AGND	-11782.5	-233
9	AGND	-11697.5	-233
10	AGND	-11612.5	-233
11	AGND	-11527.5	-233
12	SHIELDING	-11442.5	-233
13	AVDD	-11357.5	-233
14	AVDD	-11272.5	-233
15	AVDD	-11187.5	-233
16	AVDD	-11102.5	-233
17	SHIELDING	-11017.5	-233
18	GND	-10932.5	-233
19	GND	-10847.5	-233
20	GND	-10762.5	-233
21	GND	-10677.5	-233
22	SHIELDING	-10592.5	-233
23	VDD	-10507.5	-233
24	VDD	-10422.5	-233
25	VDD	-10337.5	-233
26	VDD	-10252.5	-233
27	SHIELDING	-10167.5	-233
28	TP	-10082.5	-233
29	TP	-9997.5	-233
30	TP	-9912.5	-233
31	TP	-9827.5	-233
32	TP	-9742.5	-233
33	TP	-9657.5	-233
34	TP	-9572.5	-233
35	TP	-9487.5	-233
36	TP	-9402.5	-233
37	TP	-9317.5	-233
38	TP	-9232.5	-233
39	DIMI	-9147.5	-233
40	DIMI	-9062.5	-233
41	NBW	-8977.5	-233
42	NBW	-8892.5	-233
43	PINCTL	-8807.5	-233
44	PINCTL	-8722.5	-233
45	SHIELDING	-8637.5	-233
46	DIMO	-8552.5	-233
47	DIMO	-8467.5	-233
48	SHIELDING	-8382.5	-233
49	DITHER	-8297.5	-233
50	DITHER	-8212.5	-233
51	HFRC	-8127.5	-233
52	HFRC	-8042.5	-233
53	TP	-7957.5	-233
54	TP	-7872.5	-233
55	FRAME	-7787.5	-233
56	FRAME	-7702.5	-233
57	SEL[0]	-7617.5	-233
58	SEL[0]	-7532.5	-233
59	SEL[1]	-7447.5	-233
60	SEL[1]	-7362.5	-233
61	CSB	-7277.5	-233
62	CSB	-7192.5	-233
63	SHIELDING	-7107.5	-233
64	SDA	-7022.5	-233
65	SDA	-6937.5	-233
66	SHIELDING	-6852.5	-233
67	SCL	-6767.5	-233
68	SCL	-6682.5	-233
69	SHIELDING	-6597.5	-233
70	VDD	-6512.5	-233
71	VDD	-6427.5	-233
72	VDD	-6342.5	-233
73	VDD	-6257.5	-233
74	SHIELDING	-6172.5	-233
75	GND	-6087.5	-233
76	GND	-6002.5	-233
77	GND	-5917.5	-233
78	GND	-5832.5	-233
79	SHIELDING	-5747.5	-233
80	AVDD	-5662.5	-233
81	AVDD	-5577.5	-233
82	AVDD	-5492.5	-233
83	AVDD	-5407.5	-233
84	SHIELDING	-5322.5	-233
85	AGND	-5237.5	-233
86	AGND	-5152.5	-233
87	AGND	-5067.5	-233
88	AGND	-4982.5	-233
89	SHIELDING	-4897.5	-233
90	V1	-4812.5	-233
91	V1	-4727.5	-233
92	V2	-4642.5	-233
93	V2	-4557.5	-233
94	V3	-4472.5	-233
95	V3	-4387.5	-233
96	V4	-4302.5	-233
97	V4	-4217.5	-233
98	V5	-4132.5	-233
99	V5	-4047.5	-233
100	V6	-3962.5	-233
101	V6	-3877.5	-233
102	V7	-3792.5	-233
103	V7	-3707.5	-233
104	GAMH	-3622.5	-233
105	GAMH	-3537.5	-233
106	SHIELDING	-3452.5	-233
107	DASHD	-3367.5	-233
108	VSD	-3282.5	-233
109	DASHD	-3197.5	-233
110	HSD	-3112.5	-233
111	DASHD	-3027.5	-233
112	DEN	-2942.5	-233
113	GND_LVDS	-2857.5	-233
114	GND_LVDS	-2772.5	-233
115	GND_LVDS	-2687.5	-233
116	GND_LVDS	-2602.5	-233
117	D27	-2517.5	-233
118	D26	-2432.5	-233
119	DASHD	-2347.5	-233
120	D25	-2262.5	-233
121	D24	-2177.5	-233
122	DASHD	-2092.5	-233
123	D23	-2007.5	-233
124	D22	-1922.5	-233
125	DASHD	-1837.5	-233
126	D21	-1752.5	-233
127	D20	-1667.5	-233
128	DASHD	-1582.5	-233

129	DCLK	-1497.5	-233
130	NINC	-1412.5	-233
131	DASHD	-1327.5	-233
132	VDD_LVDS	-1242.5	-233
133	VDD_LVDS	-1157.5	-233
134	VDD_LVDS	-1072.5	-233
135	VDD_LVDS	-987.5	-233
136	REV	-902.5	-233
137	DASHD	-817.5	-233
138	D17	-732.5	-233
139	D16	-647.5	-233
140	DASHD	-562.5	-233
141	D15	-477.5	-233
142	D14	-392.5	-233
143	DASHD	-307.5	-233
144	D13	-222.5	-233
145	D12	-137.5	-233
146	DASHD	-52.5	-233
147	D11	32.5	-233
148	D10	117.5	-233
149	DASHD	202.5	-233
150	D07	287.5	-233
151	D06	372.5	-233
152	DASHD	457.5	-233
153	D05	542.5	-233
154	D04	627.5	-233
155	DASHD	712.5	-233
156	D03	797.5	-233
157	D02	882.5	-233
158	DASHD	967.5	-233
159	D01	1052.5	-233
160	D00	1137.5	-233
161	DASHD	1222.5	-233
162	SHIELDING	1307.5	-233
163	GAML	1392.5	-233
164	GAML	1477.5	-233
165	V8	1562.5	-233
166	V8	1647.5	-233
167	V9	1732.5	-233
168	V9	1817.5	-233
169	V10	1902.5	-233
170	V10	1987.5	-233
171	V11	2072.5	-233
172	V11	2157.5	-233
173	V12	2242.5	-233
174	V12	2327.5	-233
175	V13	2412.5	-233
176	V13	2497.5	-233
177	V14	2582.5	-233
178	V14	2667.5	-233
179	SHIELDING	2752.5	-233
180	AGND	2837.5	-233
181	AGND	2922.5	-233
182	AGND	3007.5	-233
183	AGND	3092.5	-233
184	SHIELDING	3177.5	-233
185	AVDD	3262.5	-233
186	AVDD	3347.5	-233
187	AVDD	3432.5	-233
188	AVDD	3517.5	-233
189	SHIELDING	3602.5	-233
190	GND	3687.5	-233
191	GND	3772.5	-233
192	GND	3857.5	-233
193	GND	3942.5	-233
194	SHIELDING	4027.5	-233
195	VDD	4112.5	-233
196	VDD	4197.5	-233
197	VDD	4282.5	-233
198	VDD	4367.5	-233
199	SHIELDING	4452.5	-233
200	DUAL	4537.5	-233
201	DUAL	4622.5	-233
202	MASL	4707.5	-233
203	MASL	4792.5	-233
204	MASLOC	4877.5	-233
205	MASLOC	4962.5	-233
206	CABC_EN[0]	5047.5	-233
207	CABC_EN[0]	5132.5	-233
208	CABC_EN[1]	5217.5	-233
209	CABC_EN[1]	5302.5	-233
210	TP	5387.5	-233
211	TP	5472.5	-233
212	MODE	5557.5	-233
213	MODE	5642.5	-233
214	IFSEL	5727.5	-233
215	IFSEL	5812.5	-233
216	BIST	5897.5	-233
217	BIST	5982.5	-233
218	RES[0]	6067.5	-233
219	RES[0]	6152.5	-233
220	RES[1]	6237.5	-233
221	RES[1]	6322.5	-233
222	DCLKPOL	6407.5	-233
223	DCLKPOL	6492.5	-233
224	STBYB	6577.5	-233
225	STBYB	6662.5	-233
226	GRB	6747.5	-233
227	GRB	6832.5	-233
228	SHLR	6917.5	-233
229	SHLR	7002.5	-233
230	UPDN	7087.5	-233
231	UPDN	7172.5	-233
232	TP	7257.5	-233
233	TP	7342.5	-233
234	TP	7427.5	-233
235	TP	7512.5	-233
236	TP	7597.5	-233
237	TP	7682.5	-233
238	TP	7767.5	-233
239	TP	7852.5	-233
240	TP	7937.5	-233
241	TP	8022.5	-233
242	TP	8107.5	-233
243	TP	8192.5	-233
244	TP	8277.5	-233
245	TP	8362.5	-233
246	TP	8447.5	-233
247	SHIELDING	8532.5	-233
248	VDD	8617.5	-233
249	VDD	8702.5	-233
250	VDD	8787.5	-233
251	VDD	8872.5	-233
252	SHIELDING	8957.5	-233
253	GND	9042.5	-233
254	GND	9127.5	-233
255	GND	9212.5	-233
256	GND	9297.5	-233
257	SHIELDING	9382.5	-233
258	AVDD	9467.5	-233
259	AVDD	9552.5	-233
260	AVDD	9637.5	-233
261	AVDD	9722.5	-233
262	SHIELDING	9807.5	-233
263	AGND	9892.5	-233
264	AGND	9977.5	-233
265	AGND	10062.5	-233
266	AGND	10147.5	-233
267	SHIELDING	10232.5	-233
268	PRE_CHARGE	10317.5	-233
269	VCOMI	10402.5	-233
270	VCOMI	10487.5	-233
271	PWR_EN	10572.5	-233
272	PWR_EN	10657.5	-233
273	FBL	10742.5	-233
274	FBL	10827.5	-233
275	FBH	10912.5	-233
276	FBH	10997.5	-233
277	FBA	11082.5	-233
278	FBA	11167.5	-233
279	AVDDG	11252.5	-233
280	AVDDG	11337.5	-233
281	DRVA	11422.5	-233
282	DRVA	11507.5	-233
283	DRVH	11592.5	-233
284	DRVH	11677.5	-233
285	DRVL	11762.5	-233
286	DRVL	11847.5	-233
287	DRVL_B	11932.5	-233
288	DRVL_B	12017.5	-233
289	VCOMO	12102.5	-233
290	VCOMO	12187.5	-233
291	COM2_IN	12272.5	-233
292	COM2_IN	12357.5	-233
293	STBNL	12403	-122
294	F_CtrlL	12303	-82
295	STV1L	12403	-42
296	STV2L	12303	-2
297	STV1L	12403	38
298	CKVL	12303	78
299	UDL	12403	118
300	SYNC2L	12303	158
301	SYNC1L	12403	198
302	OEVL	12303	238
303	F_CtrlL	12403	278
304	SHIELDING	12205	258
305	COM2_OUT	12155	258
306	COM2_OUT	12105	258
307	SHIELDING	12055	258
308	SO1	12012.5	78
309	SO2	11997.5	168
310	SO3	11982.5	258
311	SO4	11967.5	78
312	SO5	11952.5	168
313	SO6	11937.5	258
314	SO7	11922.5	78
315	SO8	11907.5	168
316	SO9	11892.5	258
317	SO10	11877.5	78
318	SO11	11862.5	168
319	SO12	11847.5	258
320	SO13	11832.5	78
321	SO14	11817.5	168
322	SO15	11802.5	258
323	SO16	11787.5	78
324	SO17	11772.5	168
325	SO18	11757.5	258
326	SO19	11742.5	78

327	SO20	11727.5	168
328	SO21	11712.5	258
329	SO22	11697.5	78
330	SO23	11682.5	168
331	SO24	11667.5	258
332	SO25	11652.5	78
333	SO26	11637.5	168
334	SO27	11622.5	258
335	SO28	11607.5	78
336	SO29	11592.5	168
337	SO30	11577.5	258
338	SO31	11562.5	78
339	SO32	11547.5	168
340	SO33	11532.5	258
341	SO34	11517.5	78
342	SO35	11502.5	168
343	SO36	11487.5	258
344	SO37	11472.5	78
345	SO38	11457.5	168
346	SO39	11442.5	258
347	SO40	11427.5	78
348	SO41	11412.5	168
349	SO42	11397.5	258
350	SO43	11382.5	78
351	SO44	11367.5	168
352	SO45	11352.5	258
353	SO46	11337.5	78
354	SO47	11322.5	168
355	SO48	11307.5	258
356	SO49	11292.5	78
357	SO50	11277.5	168
358	SO51	11262.5	258
359	SO52	11247.5	78
360	SO53	11232.5	168
361	SO54	11217.5	258
362	SO55	11202.5	78
363	SO56	11187.5	168
364	SO57	11172.5	258
365	SO58	11157.5	78
366	SO59	11142.5	168
367	SO60	11127.5	258
368	SO61	11112.5	78
369	SO62	11097.5	168
370	SO63	11082.5	258
371	SO64	11067.5	78
372	SO65	11052.5	168
373	SO66	11037.5	258
374	SO67	11022.5	78
375	SO68	11007.5	168
376	SO69	10992.5	258
377	SO70	10977.5	78
378	SO71	10962.5	168
379	SO72	10947.5	258
380	SO73	10932.5	78
381	SO74	10917.5	168
382	SO75	10902.5	258
383	SO76	10887.5	78
384	SO77	10872.5	168
385	SO78	10857.5	258
386	SO79	10842.5	78
387	SO80	10827.5	168
388	SO81	10812.5	258
389	SO82	10797.5	78
390	SO83	10782.5	168
391	SO84	10767.5	258
392	SO85	10752.5	78
393	SO86	10737.5	168
394	SO87	10722.5	258
395	SO88	10707.5	78
396	SO89	10692.5	168
397	SO90	10677.5	258
398	SO91	10662.5	78
399	SO92	10647.5	168
400	SO93	10632.5	258
401	SO94	10617.5	78
402	SO95	10602.5	168
403	SO96	10587.5	258
404	SO97	10572.5	78
405	SO98	10557.5	168
406	SO99	10542.5	258
407	SO100	10527.5	78
408	SO101	10512.5	168
409	SO102	10497.5	258
410	SO103	10482.5	78
411	SO104	10467.5	168
412	SO105	10452.5	258
413	SO106	10437.5	78
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416	SO109	10392.5	78
417	SO110	10377.5	168
418	SO111	10362.5	258
419	SO112	10347.5	78
420	SO113	10332.5	168
421	SO114	10317.5	258
422	SO115	10302.5	78
423	SO116	10287.5	168
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425	SO118	10257.5	78
426	SO119	10242.5	168
427	SO120	10227.5	258
428	SO121	10212.5	78
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441	SO134	10017.5	168
442	SO135	10002.5	258
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444	SO137	9972.5	168
445	SO138	9957.5	258
446	SO139	9942.5	78
447	SO140	9927.5	168
448	SO141	9912.5	258
449	SO142	9897.5	78
450	SO143	9882.5	168
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452	SO145	9852.5	78
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477	SO170	9477.5	168
478	SO171	9462.5	258
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488	SO181	9312.5	78
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497	SO190	9177.5	78
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523	SO216	8787.5	258
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627	SO320	7227.5	168
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833	SO526	4137.5	78
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842	SO535	4002.5	78
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861	SO554	3717.5	168
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887	SO580	3327.5	78
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972	SO665	2052.5	168
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974	SO667	2022.5	78
975	SO668	2007.5	168
976	SO669	1992.5	258
977	SO670	1977.5	78
978	SO671	1962.5	168
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980	SO673	1932.5	78
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1007	SO700	1527.5	78
1008	SO701	1512.5	168
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1038	SO731	1062.5	168
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1052	SO745	852.5	78
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1064	SO757	672.5	78
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1071	SO764	567.5	168
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1074	SO767	522.5	168
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1557	SO1241	-7587.5	168
1558	SO1242	-7602.5	78
1559	SO1243	-7617.5	258
1560	SO1244	-7632.5	168
1561	SO1245	-7647.5	78
1562	SO1246	-7662.5	258
1563	SO1247	-7677.5	168
1564	SO1248	-7692.5	78
1565	SO1249	-7707.5	258
1566	SO1250	-7722.5	168
1567	SO1251	-7737.5	78
1568	SO1252	-7752.5	258
1569	SO1253	-7767.5	168
1570	SO1254	-7782.5	78
1571	SO1255	-7797.5	258
1572	SO1256	-7812.5	168
1573	SO1257	-7827.5	78
1574	SO1258	-7842.5	258
1575	SO1259	-7857.5	168
1576	SO1260	-7872.5	78
1577	SO1261	-7887.5	258
1578	SO1262	-7902.5	168
1579	SO1263	-7917.5	78
1580	SO1264	-7932.5	258
1581	SO1265	-7947.5	168
1582	SO1266	-7962.5	78
1583	SO1267	-7977.5	258
1584	SO1268	-7992.5	168
1585	SO1269	-8007.5	78
1586	SO1270	-8022.5	258
1587	SO1271	-8037.5	168
1588	SO1272	-8052.5	78
1589	SO1273	-8067.5	258
1590	SO1274	-8082.5	168
1591	SO1275	-8097.5	78
1592	SO1276	-8112.5	258
1593	SO1277	-8127.5	168
1594	SO1278	-8142.5	78
1595	SO1279	-8157.5	258
1596	SO1280	-8172.5	168
1597	SO1281	-8187.5	78
1598	SO1282	-8202.5	258
1599	SO1283	-8217.5	168
1600	SO1284	-8232.5	78
1601	SO1285	-8247.5	258
1602	SO1286	-8262.5	168
1603	SO1287	-8277.5	78
1604	SO1288	-8292.5	258
1605	SO1289	-8307.5	168
1606	SO1290	-8322.5	78
1607	SO1291	-8337.5	258
1608	SO1292	-8352.5	168
1609	SO1293	-8367.5	78
1610	SO1294	-8382.5	258
1611	SO1295	-8397.5	168
1612	SO1296	-8412.5	78
1613	SO1297	-8427.5	258
1614	SO1298	-8442.5	168
1615	SO1299	-8457.5	78
1616	SO1300	-8472.5	258
1617	SO1301	-8487.5	168
1618	SO1302	-8502.5	78
1619	SO1303	-8517.5	258
1620	SO1304	-8532.5	168
1621	SO1305	-8547.5	78
1622	SO1306	-8562.5	258
1623	SO1307	-8577.5	168
1624	SO1308	-8592.5	78
1625	SO1309	-8607.5	258
1626	SO1310	-8622.5	168
1627	SO1311	-8637.5	78
1628	SO1312	-8652.5	258
1629	SO1313	-8667.5	168
1630	SO1314	-8682.5	78
1631	SO1315	-8697.5	258
1632	SO1316	-8712.5	168
1633	SO1317	-8727.5	78
1634	SO1318	-8742.5	258
1635	SO1319	-8757.5	168
1636	SO1320	-8772.5	78
1637	SO1321	-8787.5	258
1638	SO1322	-8802.5	168
1639	SO1323	-8817.5	78
1640	SO1324	-8832.5	258
1641	SO1325	-8847.5	168
1642	SO1326	-8862.5	78
1643	SO1327	-8877.5	258
1644	SO1328	-8892.5	168
1645	SO1329	-8907.5	78
1646	SO1330	-8922.5	258
1647	SO1331	-8937.5	168
1648	SO1332	-8952.5	78
1649	SO1333	-8967.5	258
1650	SO1334	-8982.5	168
1651	SO1335	-8997.5	78
1652	SO1336	-9012.5	258
1653	SO1337	-9027.5	168
1654	SO1338	-9042.5	78
1655	SO1339	-9057.5	258
1656	SO1340	-9072.5	168
1657	SO1341	-9087.5	78
1658	SO1342	-9102.5	258
1659	SO1343	-9117.5	168
1660	SO1344	-9132.5	78
1661	SO1345	-9147.5	258
1662	SO1346	-9162.5	168
1663	SO1347	-9177.5	78
1664	SO1348	-9192.5	258
1665	SO1349	-9207.5	168
1666	SO1350	-9222.5	78
1667	SO1351	-9237.5	258
1668	SO1352	-9252.5	168
1669	SO1353	-9267.5	78
1670	SO1354	-9282.5	258
1671	SO1355	-9297.5	168
1672	SO1356	-9312.5	78
1673	SO1357	-9327.5	258
1674	SO1358	-9342.5	168
1675	SO1359	-9357.5	78
1676	SO1360	-9372.5	258
1677	SO1361	-9387.5	168
1678	SO1362	-9402.5	78
1679	SO1363	-9417.5	258
1680	SO1364	-9432.5	168
1681	SO1365	-9447.5	78
1682	SO1366	-9462.5	258
1683	SO1367	-9477.5	168
1684	SO1368	-9492.5	78
1685	SO1369	-9507.5	258
1686	SO1370	-9522.5	168
1687	SO1371	-9537.5	78
1688	SO1372	-9552.5	258
1689	SO1373	-9567.5	168
1690	SO1374	-9582.5	78
1691	SO1375	-9597.5	258
1692	SO1376	-9612.5	168
1693	SO1377	-9627.5	78
1694	SO1378	-9642.5	258
1695	SO1379	-9657.5	168
1696	SO1380	-9672.5	78
1697	SO1381	-9687.5	258
1698	SO1382	-9702.5	168
1699	SO1383	-9717.5	78
1700	SO1384	-9732.5	258
1701	SO1385	-9747.5	168
1702	SO1386	-9762.5	78
1703	SO1387	-9777.5	258
1704	SO1388	-9792.5	168
1705	SO1389	-9807.5	78
1706	SO1390	-9822.5	258
1707	SO1391	-9837.5	168
1708	SO1392	-9852.5	78
1709	SO1393	-9867.5	258
1710	SO1394	-9882.5	168
1711	SO1395	-9897.5	78
1712	SO1396	-9912.5	258

1713	SO1397	-9927.5	168
1714	SO1398	-9942.5	78
1715	SO1399	-9957.5	258
1716	SO1400	-9972.5	168
1717	SO1401	-9987.5	78
1718	SO1402	-10002.5	258
1719	SO1403	-10017.5	168
1720	SO1404	-10032.5	78
1721	SO1405	-10047.5	258
1722	SO1406	-10062.5	168
1723	SO1407	-10077.5	78
1724	SO1408	-10092.5	258
1725	SO1409	-10107.5	168
1726	SO1410	-10122.5	78
1727	SO1411	-10137.5	258
1728	SO1412	-10152.5	168
1729	SO1413	-10167.5	78
1730	SO1414	-10182.5	258
1731	SO1415	-10197.5	168
1732	SO1416	-10212.5	78
1733	SO1417	-10227.5	258
1734	SO1418	-10242.5	168
1735	SO1419	-10257.5	78
1736	SO1420	-10272.5	258
1737	SO1421	-10287.5	168
1738	SO1422	-10302.5	78
1739	SO1423	-10317.5	258
1740	SO1424	-10332.5	168
1741	SO1425	-10347.5	78
1742	SO1426	-10362.5	258
1743	SO1427	-10377.5	168
1744	SO1428	-10392.5	78
1745	SO1429	-10407.5	258
1746	SO1430	-10422.5	168
1747	SO1431	-10437.5	78
1748	SO1432	-10452.5	258
1749	SO1433	-10467.5	168
1750	SO1434	-10482.5	78
1751	SO1435	-10497.5	258
1752	SO1436	-10512.5	168
1753	SO1437	-10527.5	78
1754	SO1438	-10542.5	258
1755	SO1439	-10557.5	168
1756	SO1440	-10572.5	78
1757	SO1441	-10587.5	258
1758	SO1442	-10602.5	168
1759	SO1443	-10617.5	78
1760	SO1444	-10632.5	258
1761	SO1445	-10647.5	168
1762	SO1446	-10662.5	78
1763	SO1447	-10677.5	258
1764	SO1448	-10692.5	168
1765	SO1449	-10707.5	78
1766	SO1450	-10722.5	258
1767	SO1451	-10737.5	168
1768	SO1452	-10752.5	78
1769	SO1453	-10767.5	258
1770	SO1454	-10782.5	168
1771	SO1455	-10797.5	78
1772	SO1456	-10812.5	258
1773	SO1457	-10827.5	168
1774	SO1458	-10842.5	78
1775	SO1459	-10857.5	258
1776	SO1460	-10872.5	168
1777	SO1461	-10887.5	78
1778	SO1462	-10902.5	258
1779	SO1463	-10917.5	168
1780	SO1464	-10932.5	78
1781	SO1465	-10947.5	258
1782	SO1466	-10962.5	168
1783	SO1467	-10977.5	78
1784	SO1468	-10992.5	258
1785	SO1469	-11007.5	168
1786	SO1470	-11022.5	78
1787	SO1471	-11037.5	258
1788	SO1472	-11052.5	168
1789	SO1473	-11067.5	78
1790	SO1474	-11082.5	258
1791	SO1475	-11097.5	168
1792	SO1476	-11112.5	78
1793	SO1477	-11127.5	258
1794	SO1478	-11142.5	168
1795	SO1479	-11157.5	78
1796	SO1480	-11172.5	258
1797	SO1481	-11187.5	168
1798	SO1482	-11202.5	78
1799	SO1483	-11217.5	258
1800	SO1484	-11232.5	168
1801	SO1485	-11247.5	78
1802	SO1486	-11262.5	258
1803	SO1487	-11277.5	168
1804	SO1488	-11292.5	78
1805	SO1489	-11307.5	258
1806	SO1490	-11322.5	168
1807	SO1491	-11337.5	78
1808	SO1492	-11352.5	258
1809	SO1493	-11367.5	168
1810	SO1494	-11382.5	78
1811	SO1495	-11397.5	258
1812	SO1496	-11412.5	168
1813	SO1497	-11427.5	78
1814	SO1498	-11442.5	258
1815	SO1499	-11457.5	168
1816	SO1500	-11472.5	78
1817	SO1501	-11487.5	258
1818	SO1502	-11502.5	168
1819	SO1503	-11517.5	78
1820	SO1504	-11532.5	258
1821	SO1505	-11547.5	168
1822	SO1506	-11562.5	78
1823	SO1507	-11577.5	258
1824	SO1508	-11592.5	168
1825	SO1509	-11607.5	78
1826	SO1510	-11622.5	258
1827	SO1511	-11637.5	168
1828	SO1512	-11652.5	78
1829	SO1513	-11667.5	258
1830	SO1514	-11682.5	168
1831	SO1515	-11697.5	78
1832	SO1516	-11712.5	258
1833	SO1517	-11727.5	168
1834	SO1518	-11742.5	78
1835	SO1519	-11757.5	258
1836	SO1520	-11772.5	168
1837	SO1521	-11787.5	78
1838	SO1522	-11802.5	258
1839	SO1523	-11817.5	168
1840	SO1524	-11832.5	78
1841	SO1525	-11847.5	258
1842	SO1526	-11862.5	168
1843	SO1527	-11877.5	78
1844	SO1528	-11892.5	258
1845	SO1529	-11907.5	168
1846	SO1530	-11922.5	78
1847	SO1531	-11937.5	258
1848	SO1532	-11952.5	168
1849	SO1533	-11967.5	78
1850	SO1534	-11982.5	258
1851	SO1535	-11997.5	168
1852	SO1536	-12012.5	78
1853	SHIELDING	-12055	258
1854	COM1_OUT	-12105	258
1855	COM1_OUT	-12155	258
1856	SHIELDING	-12205	258
1857	F_CtrlR	-12403	278
1858	OEV1R	-12303	238
1859	SYNC1R	-12403	198
1860	SYNC2R	-12303	158
1861	UDR	-12403	118
1862	CKVR	-12303	78
1863	STV1R	-12403	38
1864	STV2R	-12303	-2
1865	STV1R	-12403	-42
1866	F_CtrlR	-12303	-82
1867	STBNR	-12403	-122
	ALIGNMENT MARK_L	-12131.5	115.5
	ALIGNMENT MARK_R	12131.5	115.5

Appendix A : BIST pattern

R→ G → B → Black → White → Color Bar → Horizontal 256 gray scale → Vertical 256 gray scale → Crosstalk pattern → Chess board (L255/L0) → Flicker pattern → Black background with white out frame