CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A080SN01 V5**
CUSTOMER APPROVED	**Title :** **Name :**

☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)

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Product Specification

8" COLOR TFT-LCD MODULE

Model Name： **A080SN01 V5**

Planned Lifetime:	From 2009/Feb To 2011/Feb
Phase-out Control:	From 2010/Sep To 2011/Feb
EOL Schedule:	2011/Feb

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2009/01/21	All	First Draft.
0.1	2009/02/11	4,5	Update Drawing
		24	Update Chromaticity
0.2	2009/02/18	10	Update Electrical DC Characteristics
0.3	2009/05/08	9	Update Vcc min. to 3.0V from 2.7V
0.4	2009/05/15	11	Update Gamma voltage

Contents

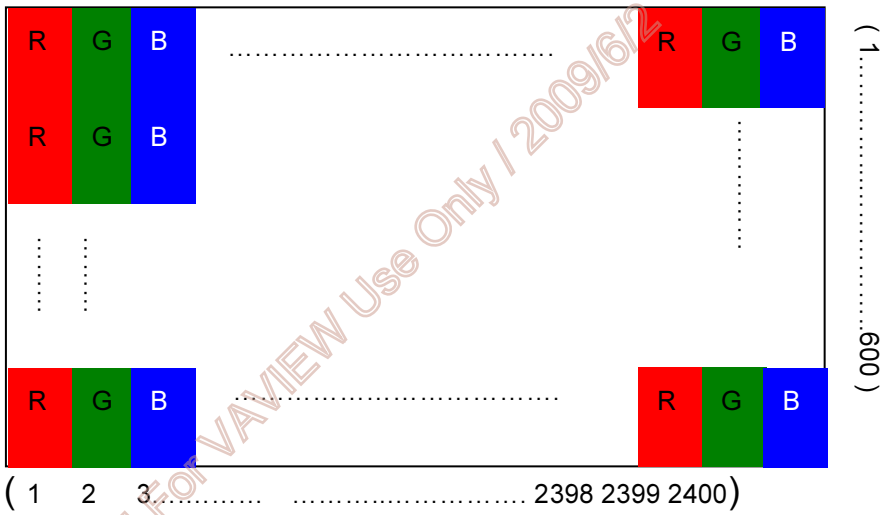
A. General Information

This product is for portable DVD and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	8(Diagonal)	
2	Display Resolution	dot	800RGB(W)x600(H)	
3	Overall Dimension	mm	183(W)x141(H)x6.3(D)	Note 1
4	Active Area	mm	162(W)x121.5(H)	
5	Pixel Pitch	mm	0.2025(W)x0.2025(H)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	188 ±10	
12	Panel Power Consumption	mW	260	Note 4
13	Backlight Power Consumption	W	1.87	
	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.

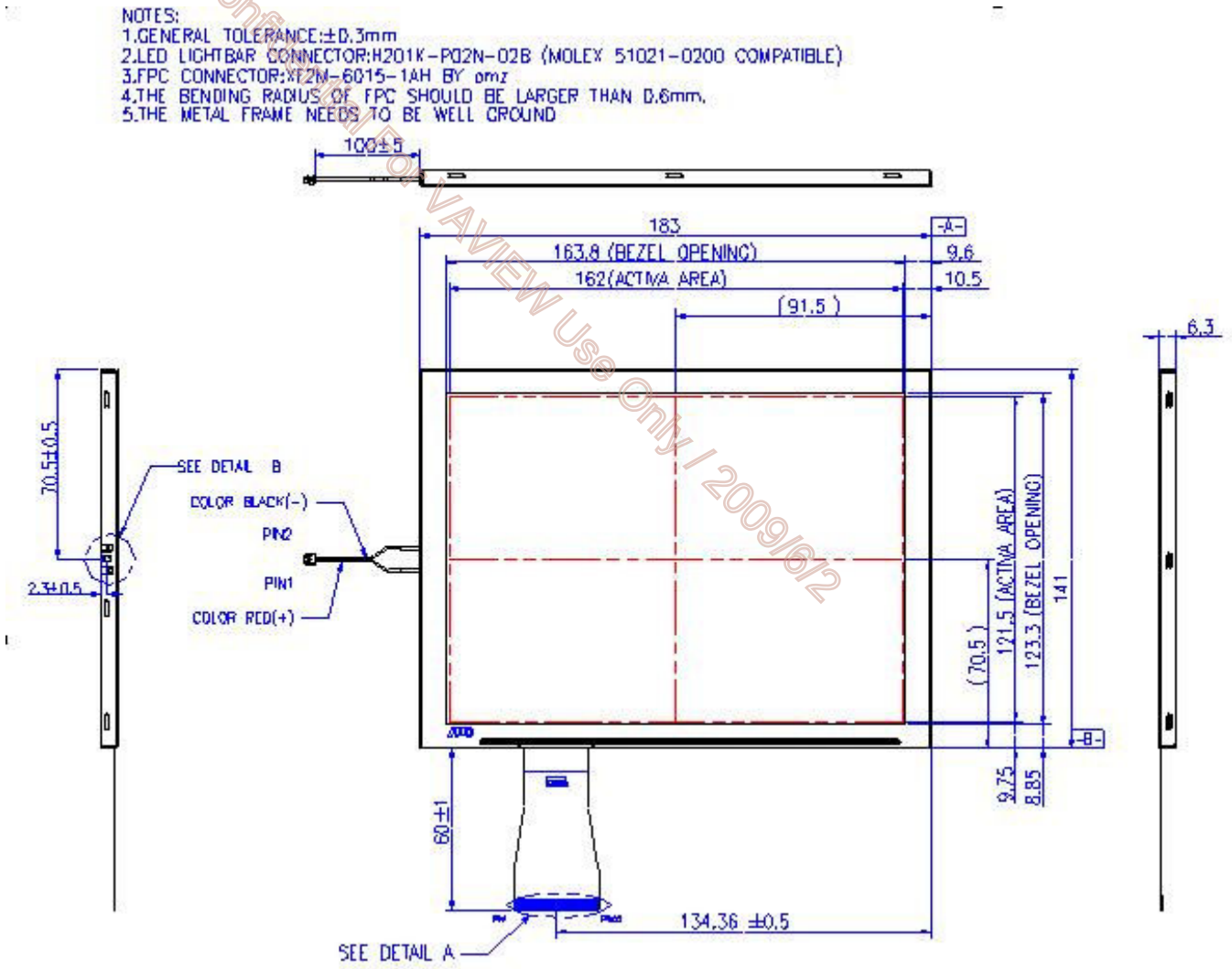


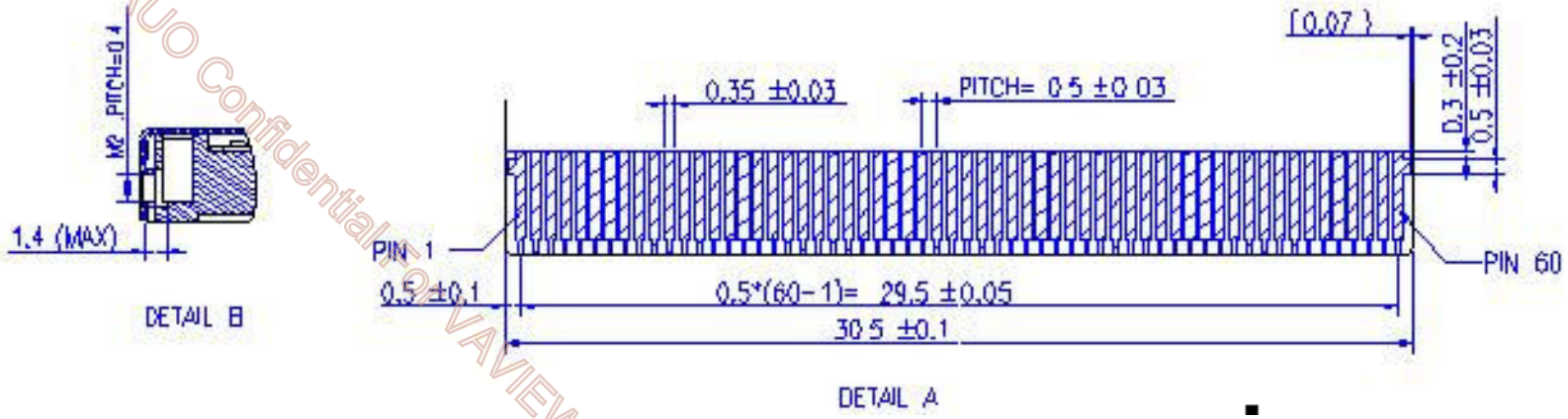
Note 3: The full color display depends on 24-bit data signal (pin 4~27).

Note 4: Please refer to Electrical Characteristics chapter.

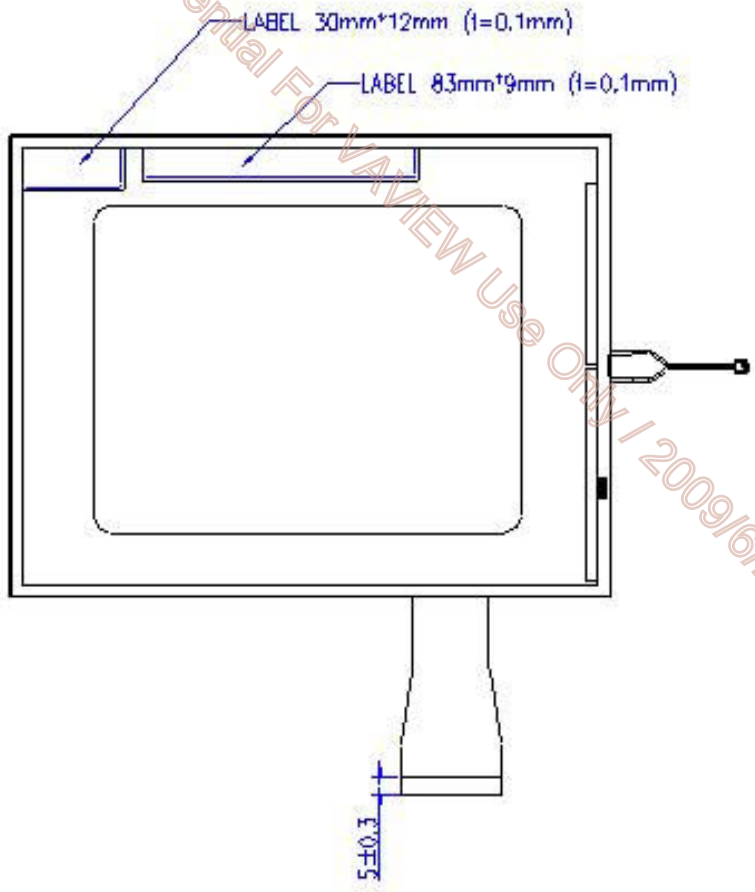
B. Outline Dimension

1. TFT-LCD Module – Front View





2. TFT-LCD Module – Rear View



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector : XF2M-6015-1AH

Pin no	Symbol	I/O	Description	Remark
1	AGND	P	Analog Ground	
2	AVDD	P	Analog Power	
3	VCC	P	Digital Power	
4	R0	I	Data input (LSB)	
5	R1	I	Data input	
6	R2	I	Data input	
7	R3	I	Data input	
8	R4	I	Data input	
9	R5	I	Data input	
10	R6	I	Data input	
11	R7	I	Data input (MSB)	
12	G0	I	Data input (LSB)	
13	G1	I	Data input	
14	G2	I	Data input	
15	G3	I	Data input	
16	G4	I	Data input	
17	G5	I	Data input	
18	G6	I	Data input	
19	G7	I	Data input (MSB)	
20	B0	I	Data input (LSB)	
21	B1	I	Data input	
22	B2	I	Data input	
23	B3	I	Data input	
24	B4	I	Data input	
25	B5	I	Data input	
26	B6	I	Data input	
27	B7	I	Data input (MSB)	
28	DCLK	I	Clock input	
29	DE	I	Data enable signal	
30	HSYNC	I	Horizontal sync input. Negative polarity	
31	VSYNC	I	Vertical sync input. Negative polarity	
32	SCL	I	Serial communication clock input	
33	SDA	I	Serial communication data input	

34	CSB	I	Serial communication chip select	
35	NC	-	For test, do not connect (Please leave it open)	
36	VCC	P	Digital Power	
37	NC	-	For test, do not connect (Please leave it open)	
38	GND	P	Digital ground	
39	AGND	P	Analog ground	
40	AVDD	P	Analog Power	
41	VCOMin	I	For external VCOM DC input (Optional)	
42	DITH/SDA	I/O	Dithering setting DITH = "L" 6bit resolution(LSB last 2 bits of input data turncated) DITH = "H" 8bit resolution(Default setting) When register R14 and D7 is set to "H". CABC enable.This Pin would used as I^2C Data pin.	
43	SCL/GND	I/O	When register R14 and D7 is set to "H". CABC enable.This Pin would used as I2C Clock pin. (refer to section G2 – CABC function block) When register R14 and D7 is set to "L", CABC is disable. This pin must connect to GND.	
44	VCOM	O	connect a capacitor	
45	V10	P	Gamma correction voltage reference	
46	V9	P	Gamma correction voltage reference	
47	V8	P	Gamma correction voltage reference	
48	V7	P	Gamma correction voltage reference	
49	V6	P	Gamma correction voltage reference	
50	V5	P	Gamma correction voltage reference	
51	V4	P	Gamma correction voltage reference	
52	V3	P	Gamma correction voltage reference	
53	V2	P	Gamma correction voltage reference	
54	V1	P	Gamma correction voltage reference	
55	NC/ LED_CABC OUT	O	NC Pin When register R14 and D7 is set to "H". CABC enable.This Pin would used as LED PWM duty output.	
56	VGH	P	Positive power for TFT	
57	VCC	P	Digital Power	
58	VGL	P	Negative power for TFT	
59	GND	P	Digital Ground	
60	NC	-	NC PIN	

I: Input; P: Power; G: Ground; C: Capacitor

2. Backlight Pin Assignment

Recommended connector : H201K-P02N-02B (MOLEX 51021-0200 COMPATIBLE)

Pin no	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	
2	GND	-	Ground for backlight unit	

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5	V	
	AV_{DD}	AGND=0	-0.5	15	V	
	V_{GH}	GND=0	-0.3	42	V	
	V_{GL}		-20	0.3	V	
	$V_{GH}-V_{GL}$		-	40	V	
Input signal voltage	V_I		-0.3	V_{CC}+0.3	V	Note 1
	VCOM		0	6.5	V	
Operating temperature	Topa		-10	60	℃	
Storage temperature	Tstg		-20	70	℃	

Note 1: HS , VS , DE, Digital Data.

Note 2: Functional operation should be restricted under ambient temperature (25℃).

Note 3: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

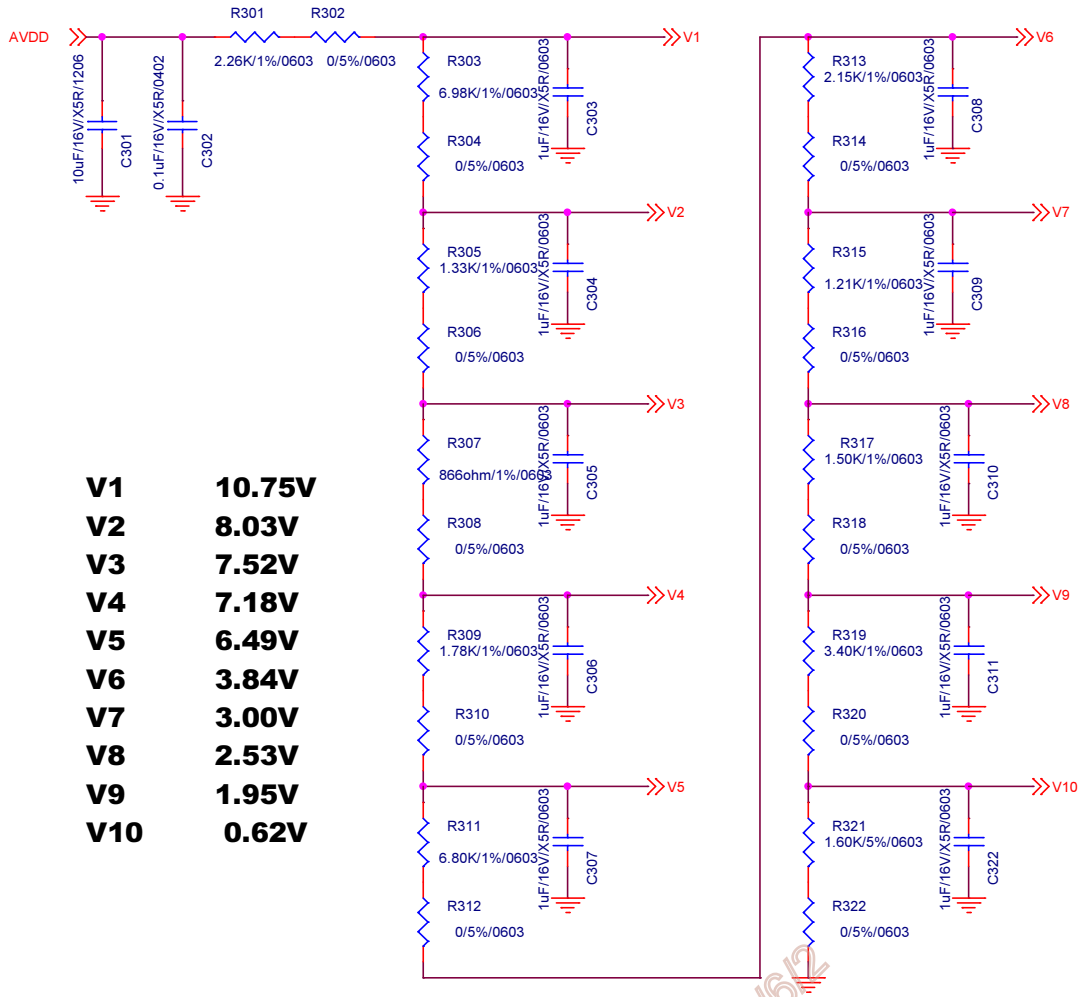
4. Electrical DC Characteristics

a. (VCC = +3.3V, AVDD=11.68V, AGND=GND=0V, TOPR = -10°C to +60°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	3.0	3.3	3.6	V	
		AV_{DD}	11	11.68	12	V	
		V_{GH}	14	15	16	V	
		V_{GL}	-7.5	-6.75	-5	V	
Power		P	-	230	260	mW	Black Pattern
VCOM		V_{CDC}	3.4	3.6	3.8	V	DC component
Input signal	H Level	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	Note 1
	L Level	V_{IL}	0	-	0.3 V_{CC}	V	
Input level of V1~V5		Vx	0.4*AVDD	-	AVDD-0.5		Positive gamma correction voltage Note 2
Input level of V6~V10		Vx	0.5	-	0.6*AVDD		Negative gamma correction voltage Note 2

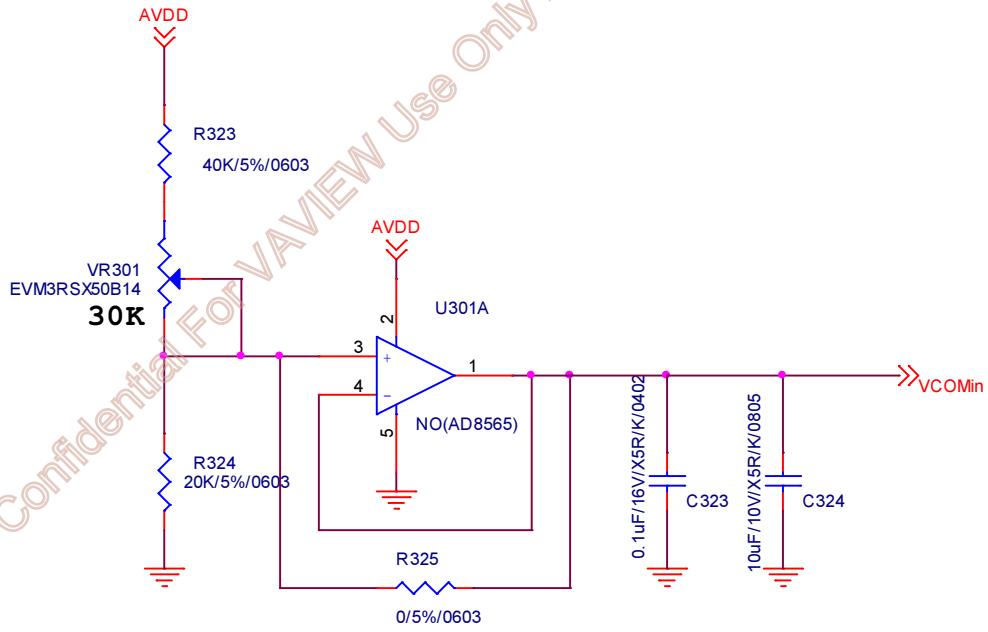
Note 1: HS , VS , DE, Digital Data
Note 2 : AGND <V10<V9V<8V7<V6<V5<V4<V3<V2<V1<AVDD

b. Gamma voltage suggested circuit is as follows



V1	**10.75V**
V2	**8.03V**
V3	**7.52V**
V4	**7.18V**
V5	**6.49V**
V6	**3.84V**
V7	**3.00V**
V8	**2.53V**
V9	**1.95V**
V10	**0.62V**

c.Vcom buffer suggested circuit is as follows



d. Current Consumption (AGND=GND=0V)

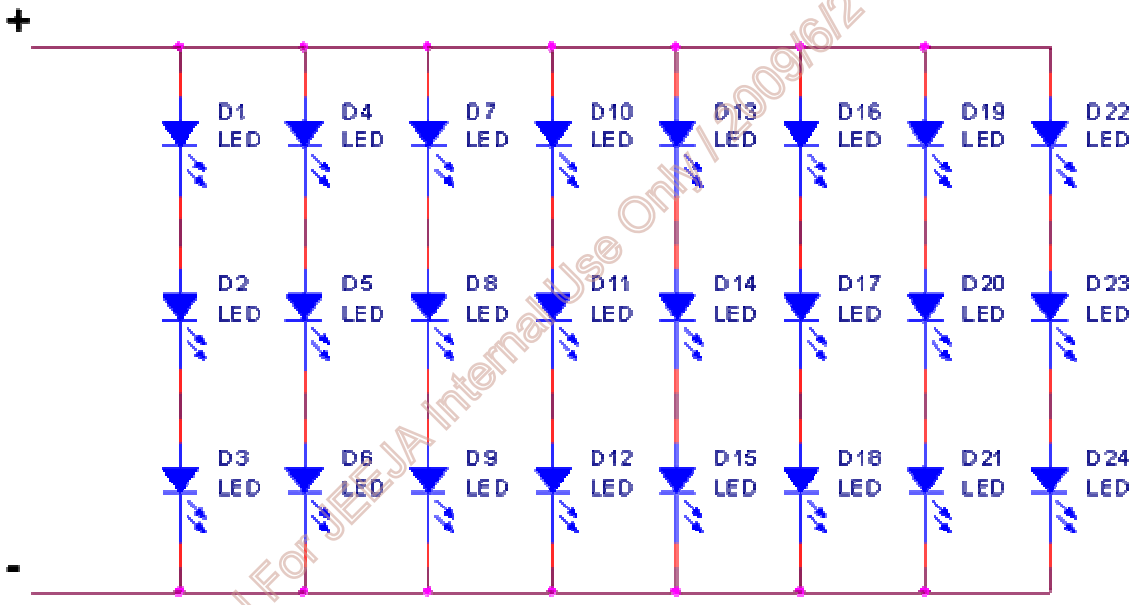
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VCC	I_{VCC}	V_{CC}=3.3V	-	11	14	mA	Black Pattern
Inpur current for AVDD	I_{AVDD}	AVDD=11.7V	-	16	20	mA	Black Pattern
Input current for VGH	I_{VGH}	VGH=15V	-	0.16	0.2	mA	Black Pattern
Inpur current for VGL	I_{VGL}	VGL=-6.75V	-	0.16	0.2	mA	Black Pattern

e. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Lightbar current	I_L	-	200	-	mA	Note 1, 2
Power consumption	P	-	2.08	-	W	
LED Lightbar life time		10,000	-	-	Hr	Note 1, 2, 3, 4

Note 1: LED backlight is LED lightbar type(24 pcs of LED).

Note 2: Definition of “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current= 200mA



Note 3: The value is only for reference.

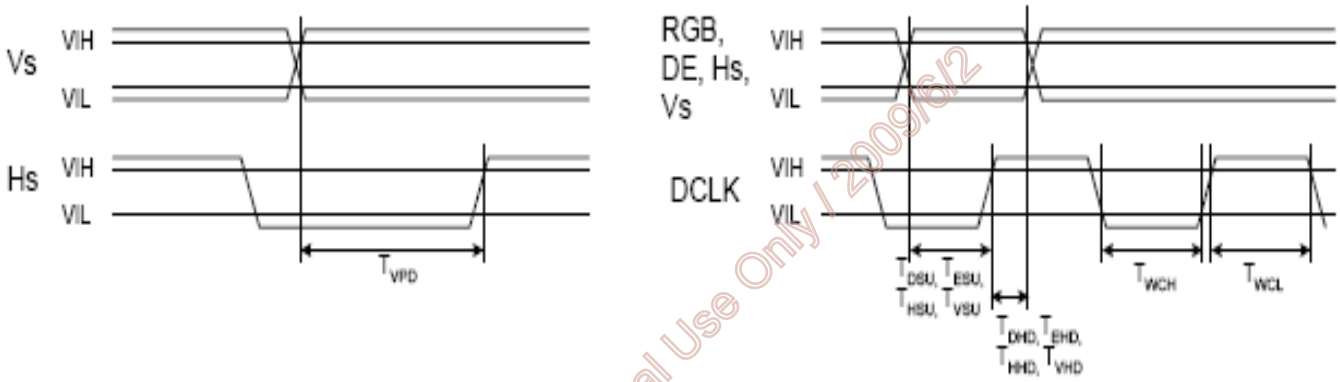
Note 4: If it operates with LED lightbar current more than 200mA, it maybe decreases LED lifetime.

5. Electrical AC Characteristics

a. Signal AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock High time	T_{WCL}	8	-	-	ns	
Clock Low time	T_{WCH}	8	-	-	ns	
Hsync setup time	T_{HSU}	5	-	-	ns	
Hsync hold time	T_{HHD}	10	-	-	ns	
Vsync setup time	T_{VSU}	0	-	-	ns	
Vsync hold time	T_{VHD}	2	-	-	ns	
Data setup time	T_{DSU}	5	-	-	ns	
Data hold time	T_{DHD}	10	-	-	ns	
Data enable set-up time	T_{ESU}	4	-	-	ns	
Data enable hold time	T_{EHD}	2	-	-	ns	

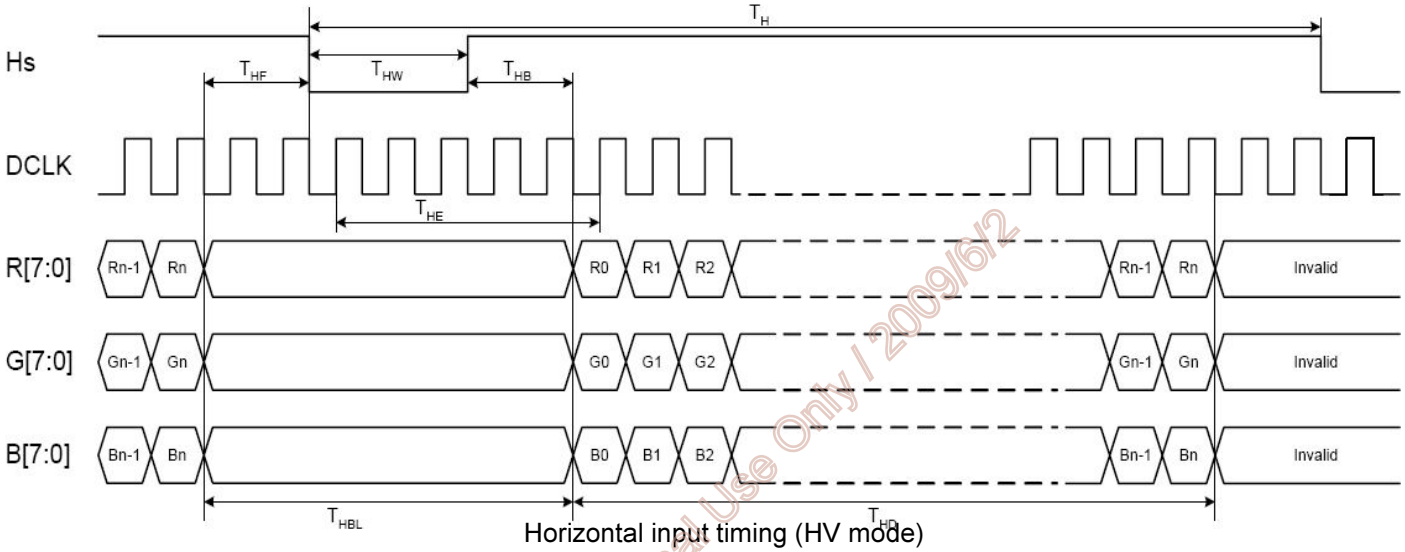
b. Input Timing



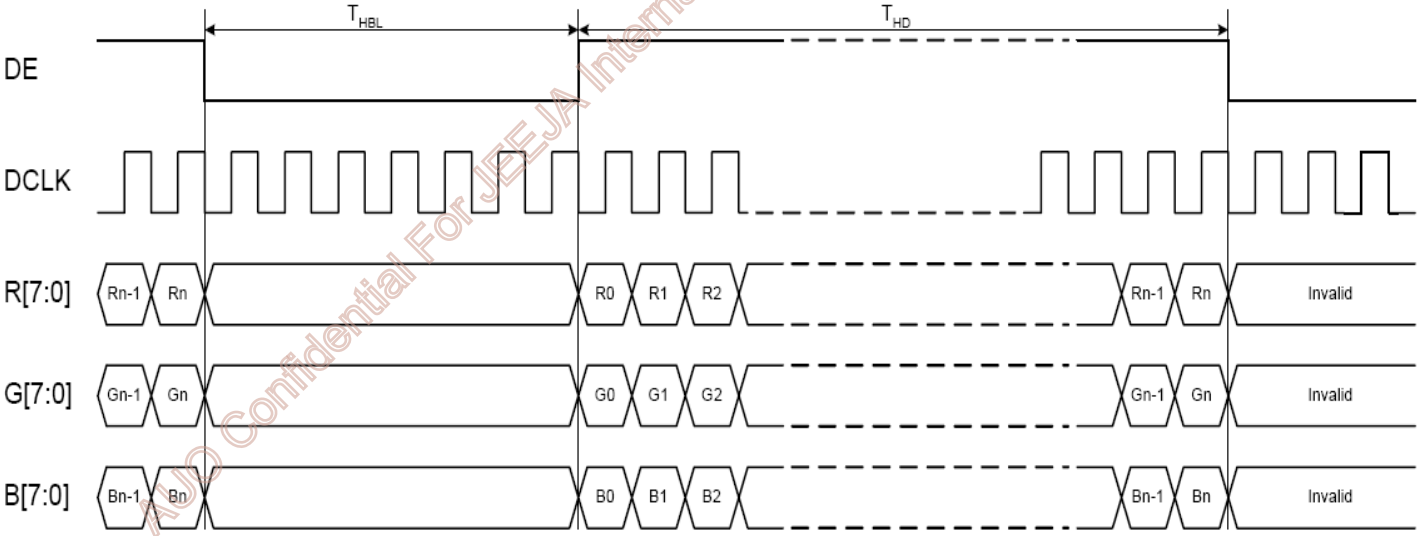
c. Input Timing Setting

Horizontal timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	F_{DCLK}	25	40	45	MHz	
DCLK period	T_{DCLK}	22	25	40	ns	
Hsync period (= T_{HD} + T_{HBL})	T_H	986	1056	1183	DCLK	
Active Area	T_{HD}	-	800	-	DCLK	
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}	186	256	383	DCLK	
Hsync front porch	T_{HF}	-	40	-	DCLK	
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	88	216	343	DCLK	Function of HDL[7..0] settings
Hsync pulse width	T_{HW}	1	128	136	DCLK	
Hsync back porch	T_{HB}	10	88	342	DCLK	



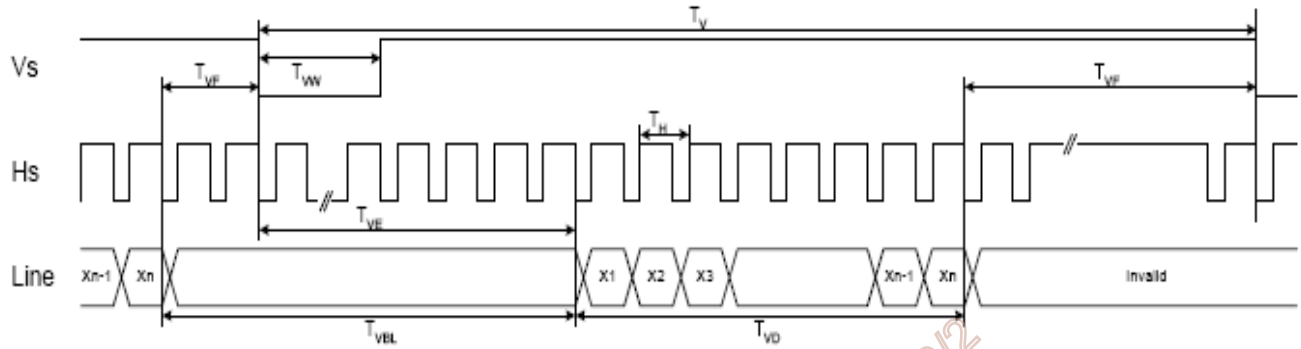
Horizontal input timing (HV mode)



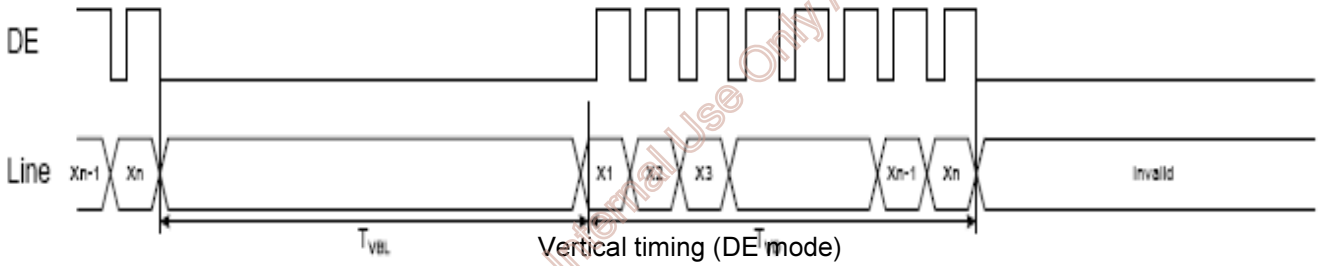
Horizontal input timing (DE mode)

Vertical timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Vsync period (= T_{VD} + T_{VBL})	T_V	620	628	635	Th	
Active lines	T_{VD}	-	600	-		
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}	20	28	35	Th	
Vsync front porch	T_{VF}	-	1	-	Th	
GD start pulse delay	T_{VE}	19	27	34	HS	Function of VDL[3..0] settings
Vsync pulse width	T_{VW}	1	3	16	Th	
Hsync/Vsync phase shift	T_{VPD}	2	320	-	DCLK	



Vertical timing (HV mode)

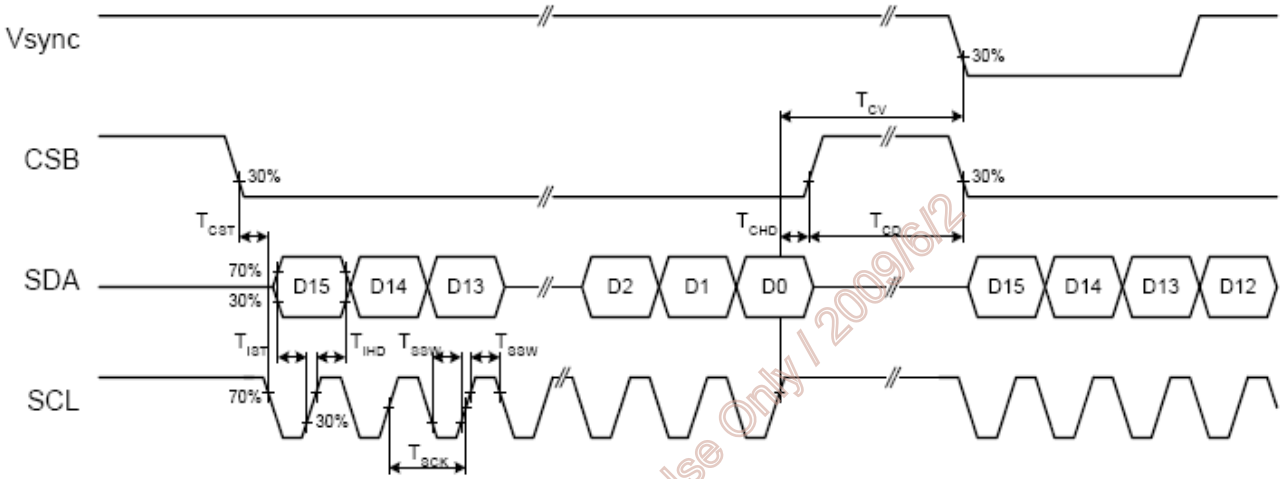


Vertical timing (DE mode)

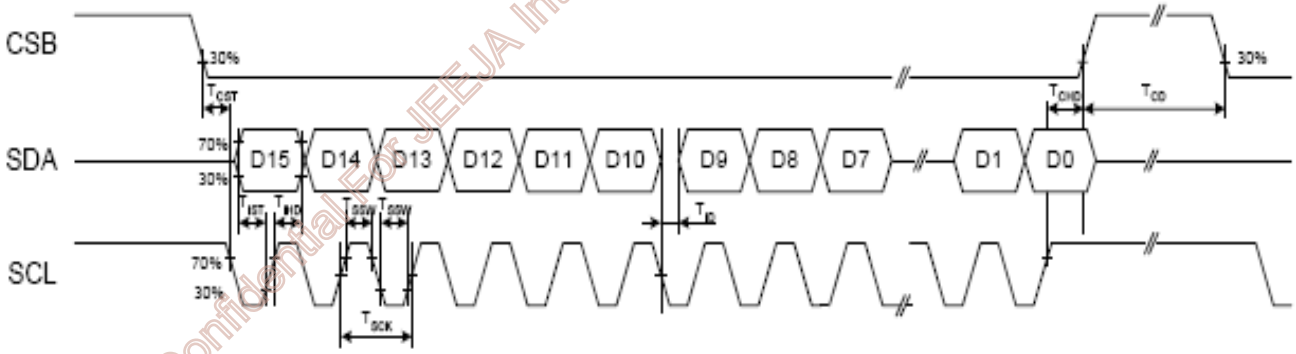
6. Serial Interface Characteristics

a. Serial Control Interface AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial data setup time	T_{IST}	120	-	-	ns	
Serial data hold time	T_{IHD}	120	-	-	ns	
CSB setup time	T_{CST}	120	-	-	ns	
CSB hold time	T_{CHD}	120	-	-	ns	
Serial clock high/low	T_{SSW}	120	-	-	ns	
Serial clock	T_{SCK}	320	-	-	ns	
Delay from CSB to VSYNC	T_{CV}	120	-	-	us	
Chip select distinguish	T_{CD}	120	-	-	us	
Serial data output delay	T_{ID}	-	-	60	ns	CL=20pF



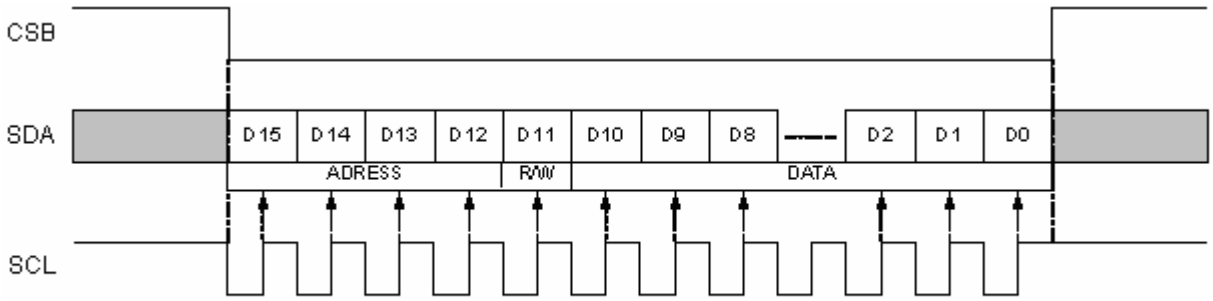
AC serial interface write mode timings



AC serial interface read mode timings

b. Register Bank

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table. The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.



Serial interface write/read sequence

1. At power-on, the default values specified for each parameter are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
   b. The read operation is interrupt.
3. If more than 16-bit data are read during the CS low time period, the last 16 bits are kept.
   a. Address & R/W are always defined form CSB falling edge.
   b. The write operation load last 11 bit data before CSB rising edge.
   c. The read operation is “D0” is output to SDA until CSB rising edge.
4. All items are set at the falling edge of the vertical sync, except R0[1:0].
5. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
6. Register R/W setting: D11 = “L” → write mode; D11 = “H” → read mode.
7. The register setting values are valid when VCC already goes to high and after VSYNC starts.
8. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
9. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
10. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

c. Serial Interface Setting Table.

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		DITH (1)	(0)	(1)	SHDB1 (1)	(0)	GRB (1)	STB (1)
R1	0	0	0	1	0	×	(0)	(1)	(6Fh)							
R2	0	0	1	0	0	×	×	×	HDL (80h)							
R3	0	0	1	1	0	×	×	(0)	(0)	(0)	(0)	(0)	VDL (1000)			
R4	0	1	0	0	0	×	×	(1)	(0)	(0)	(0)	(1)	(1111)			
R6	0	1	1	0	0	×	(0)	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)
R8	1	0	0	0	0	×	(0)	(0)	(0)	(0)	(1)	(1)	(1)	(0)	(1)	CABC_EN (0)
R13	1	1	0	1	0	(1)	(0)	(0)	(1)	(1)	(0)	(0)	(1)	(0)	(0)	(0)
R14	1	1	1	0	0	×	×	×	I2C_EN (0)	(1)	(0)	(1)	(0)	(0)	(0)	(0)

X: Reserved. Please set to “0”.

d. Register Description

R0 setting

Address	**Bit**	**Description**		**Default**
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	1
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	1
		Bit3 (SHDB1)	AVDD DC-DC converter shutdown setting.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit3	SHDB1 function
0	AVDD DC-DC converter is off.
1	AVDD DC-DC converter is on. **(default)**

Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DCs converters are off. All outputs are set to GND.
1	Normal operation. **(default)**

R2 setting

Address	**Bit**	**Description**		**Default**
0010	[7..0]	Bit7-0(HDL)	Horizontal start pulse adjustment function	80H

Bit7-0	HDL function
00h	$T_{HE} = T_{HEtyp}$ - 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

R3 setting

Address	**Bit**	**Description**		**Default**
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0(VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function
0000	$T_{VE} = T_{VEtyp} – 8$ Hs period.
0001	$T_{VE} = T_{VEtyp} – 7$ Hs period.
0010	$T_{VE} = T_{VEtyp} – 6$ Hs period.
0011	$T_{VE} = T_{VEtyp} – 5$ Hs period.
0100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
0101	$T_{VE} = T_{VEtyp} – 3$ Hs period.
0110	$T_{VE} = T_{VEtyp} – 2$ Hs period.
0111	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1000	$T_{VE} = T_{VEtyp.}$ (default)
1001	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1010	$T_{VE} = T_{VEtyp} – 2$ Hs period.
1011	$T_{VE} = T_{VEtyp} – 3$ Hs period.
1100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
1101	$T_{VE} = T_{VEtyp} – 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} – 6$ Hs period.
1111	$T_{VE} = T_{VEtyp} – 7$ Hs period.

R6 setting

Address	**Bit**	**Description**		**Default**
0110	[9..0]	Bits9	AUO Internal Use	0
		Bits8(EnGB12)	Gamma buffer Enable for V9	1
		Bits7(EnGB11)	Gamma buffer Enable for V8	1
		Bits6(EnGB10)	Gamma buffer Enable for V7	1
		Bits5	AUO Internal Use	0
		Bits4	AUO Internal Use	0
		Bits3(EnGB5)	Gamma buffer Enable for V4	1
		Bits2(EnGB4)	Gamma buffer Enable for V3	1
		Bits1(EnGB3)	Gamma buffer Enable for V2	1
		Bits0	AUO Internal Use	0

Bitx	EnGBx function
0	Gamma buffer for VX is disabled (High Z).
1	Gamma buffer is enabled. VX must be connected externally.

R8 setting

Address	Bit	Description		Default
1000	[1]	Bit0	CABC function enable 0: CABC function is disabled. (default) 1: CABC function is enabled.	0

R14 setting

Address	Bit	Description		Default
1000	[1]	Bit7	CABC 2-wire serial interface is enabled. 0: 2-wire serial interface is disabled. (default) 1: 2-wire serial interface is enabled.	0

7. Power On/Off Characteristics

a.1 Recommended Power On Register Setting (Without CABC)

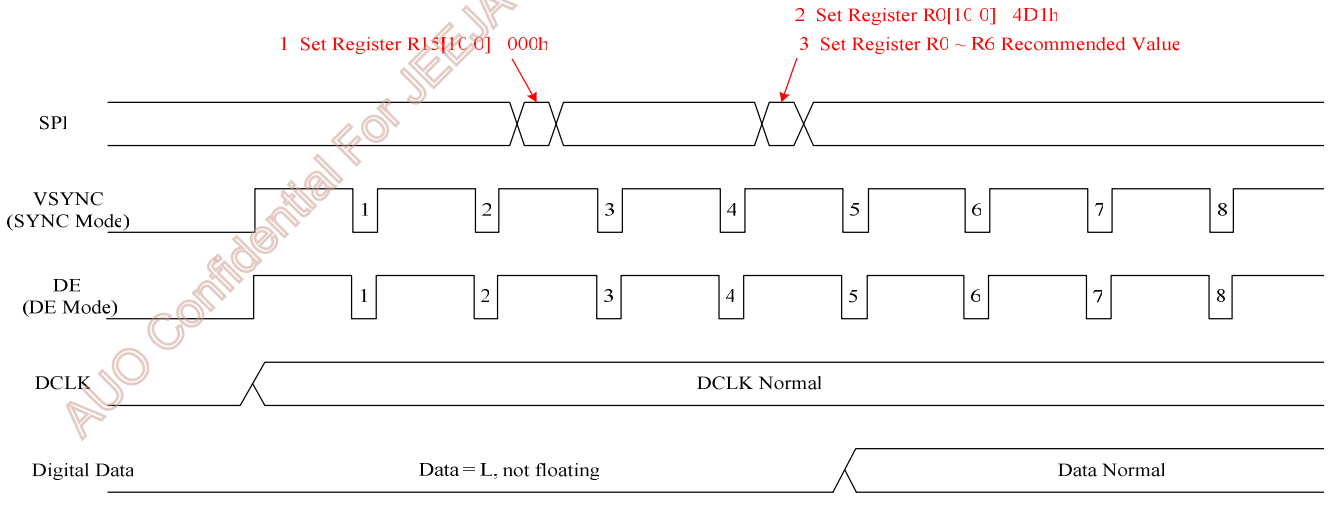
Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

a.2 Recommended Power On Register Setting (With CABC)

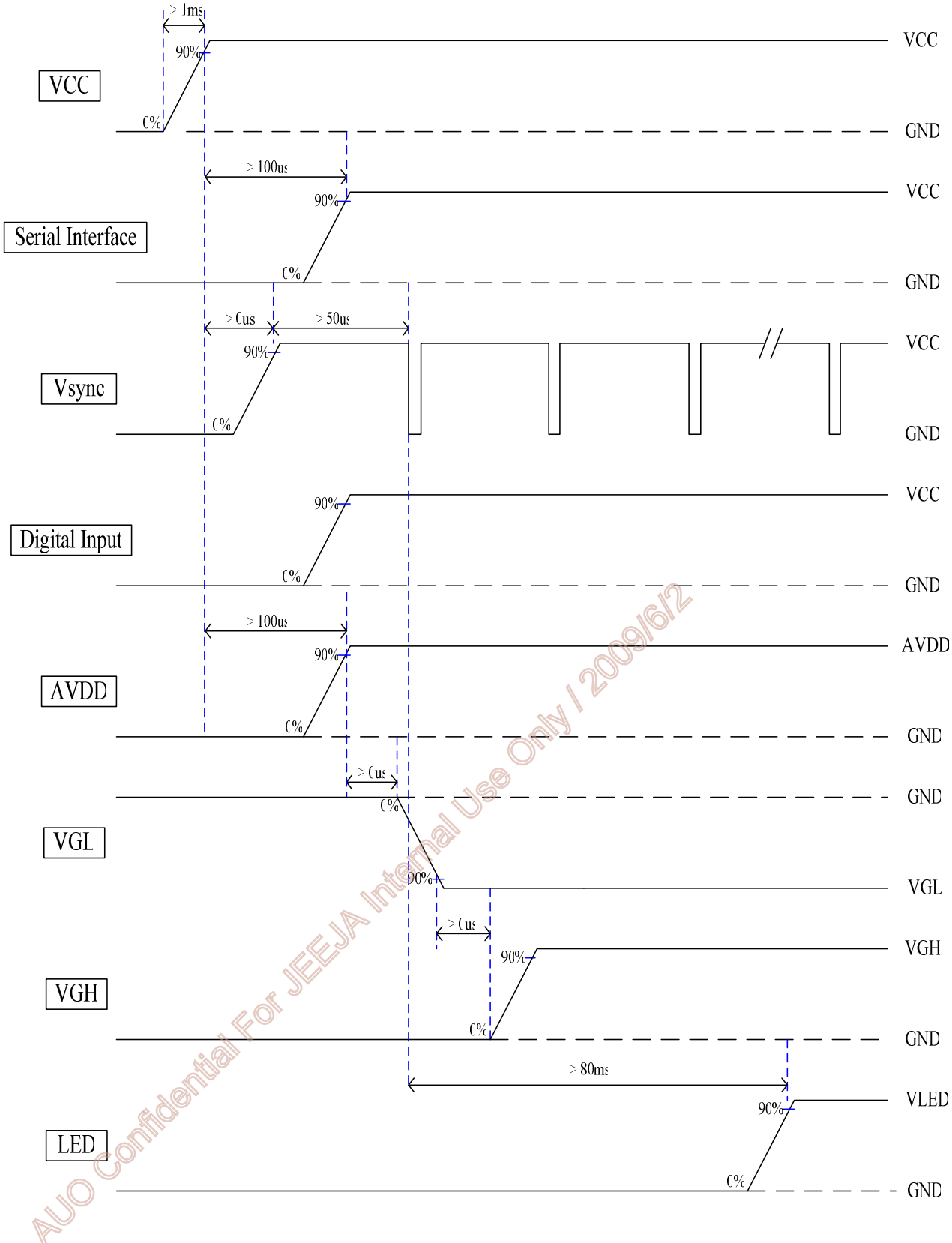
Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0
R13	1	1	0	1	0	1	0	0	1	1	1	1	0	1	0	0
R14	1	1	1	0	0	×	×	×	1	1	0	1	0	0	0	0
R8	1	0	0	0	0	×	0	0	0	0	1	1	1	0	1	1

Note : Start to provide SPI commend at least after 2 frame.

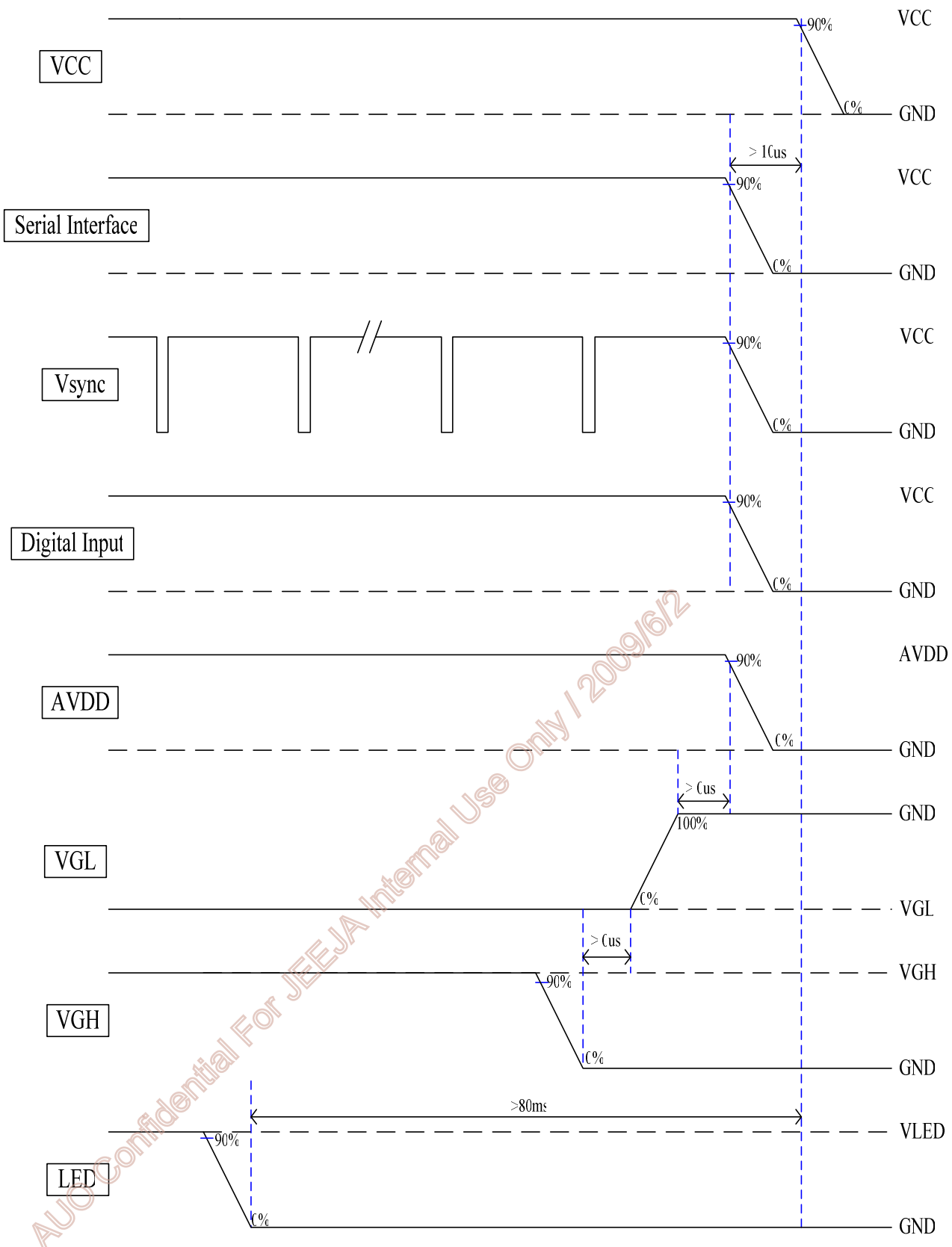
1. Send R15 : 000h(Normal register bank) at first.
2. Wait at least after more than one frame, send R0 : 4D1h(Global Reset)
3. After send Global Reset, start to send R0 to R14 recommend register value.



b. Recommended Power On Sequence



c. Power Off Sequence



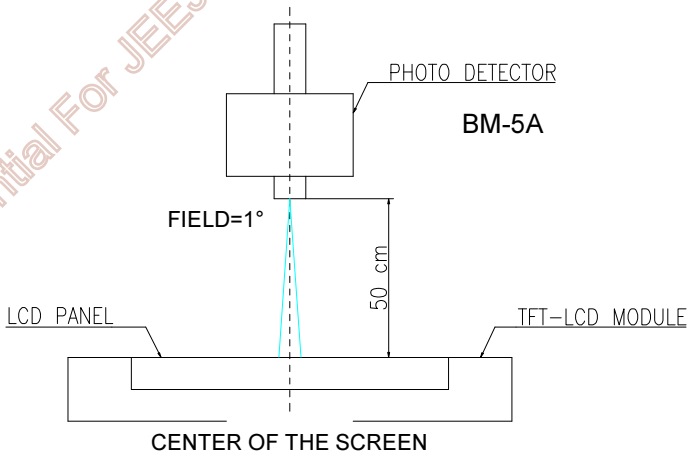
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	 θ=0°	 -- --	 4 16	 8 32	 ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle	400	500	--		Note 4
Viewing Angle	Top Bottom Left Right		CR≧10	50 50 60 60	60 65 70 70		deg.	Note 5
Brightness		Y_L	θ=0°	220	250	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.26	0.31	0.36		
		Y	θ=0°	0.28	0.33	0.38		
	Red	X	θ=0°	0.52	0.57	0.62		
		Y	θ=0°	0.32	0.37	0.42		
	Green	X	θ=0°	0.30	0.35	0.40		
		Y	θ=0°	0.53	0.58	0.63		
	Blue	X	θ=0°	0.10	0.15	0.20		
		Y	θ=0°	0.06	0.11	0.16		
Uniformity		ΔY_L	%	70	75	--	%	Note 7

Note 1: Ambient temperature =25℃, and LED lightbar currently I_L = 200mA. To be measured in the dark room.

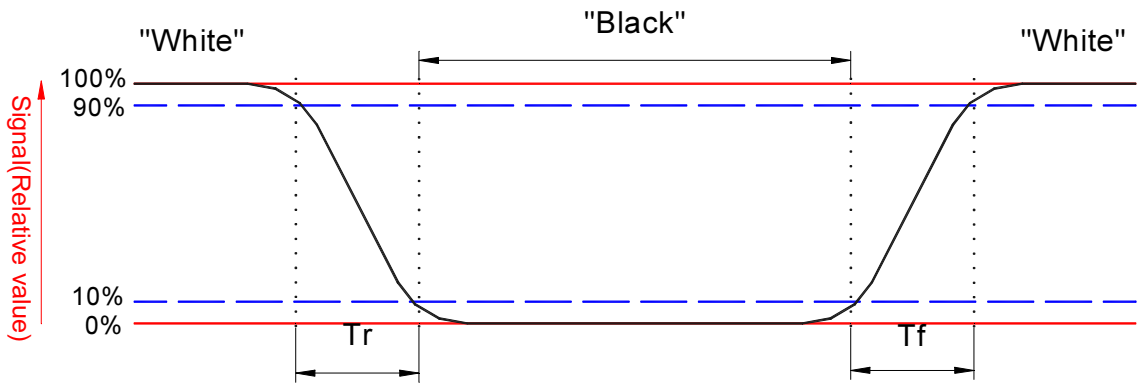
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

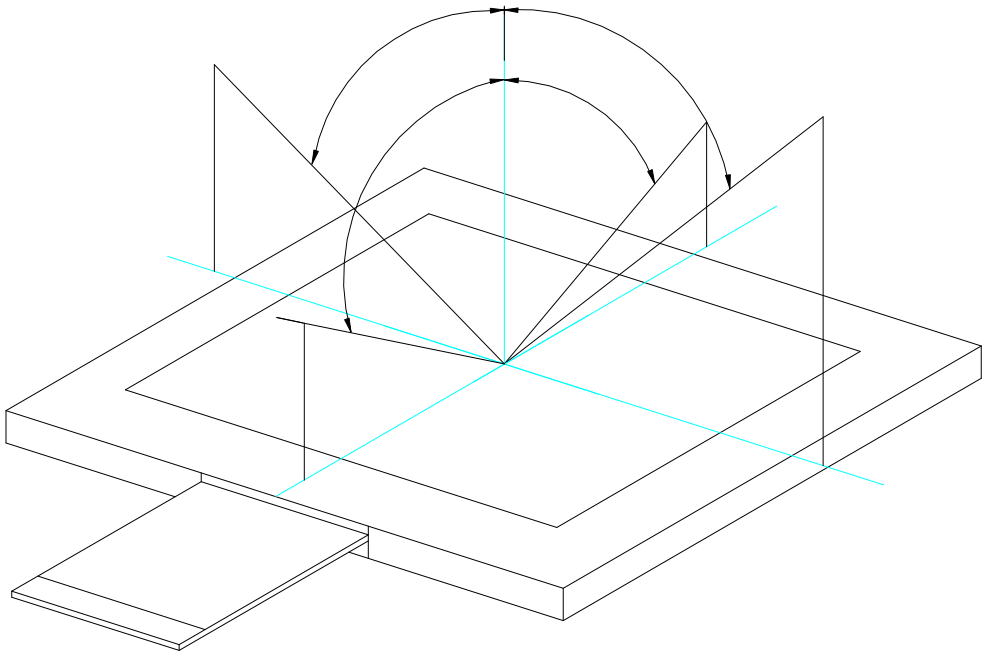


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

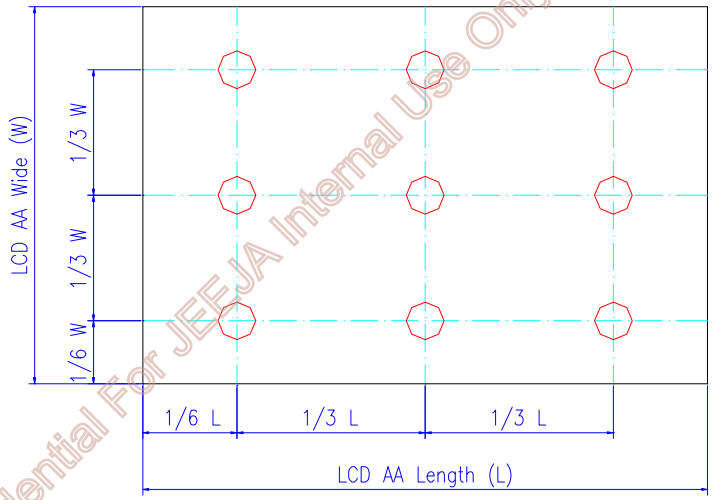
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

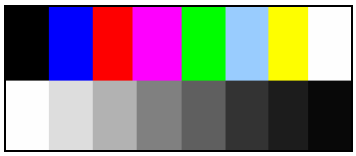
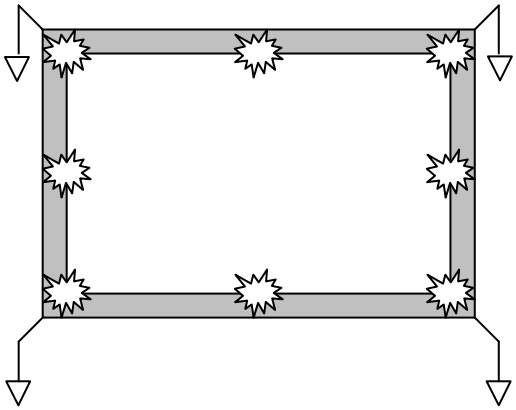
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -20□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= -10□ 240Hrs	
5	High Temperature & High Humidity	Tp= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-10□~60□, 100 cycle, 1Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 4
8	Image Sticking	25□, 4hrs	Note 5
9	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 6

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

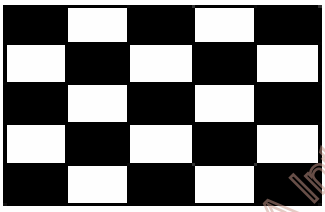
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

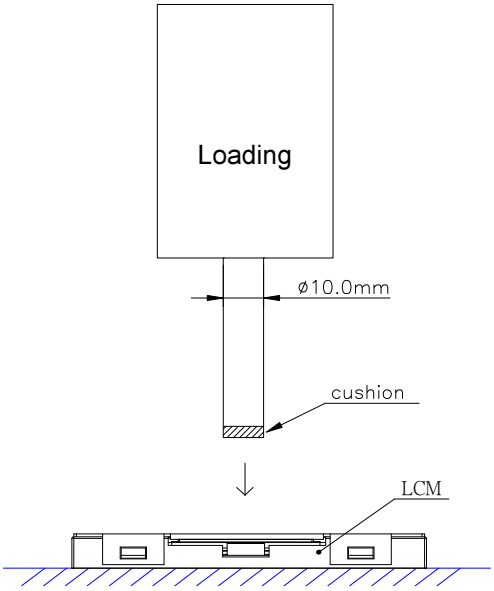
Note4 : All test techniques follow IEC6100-4-2 standard.

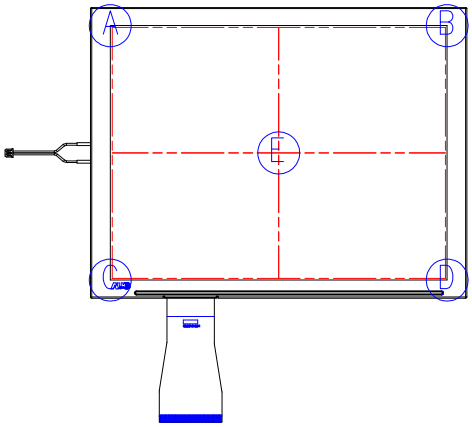
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

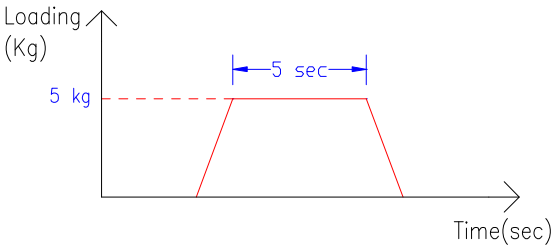
Note 5: Operate with 5x5 chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level after waiting 20 min, the mura is less than JND 2.5.



Note 6: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)



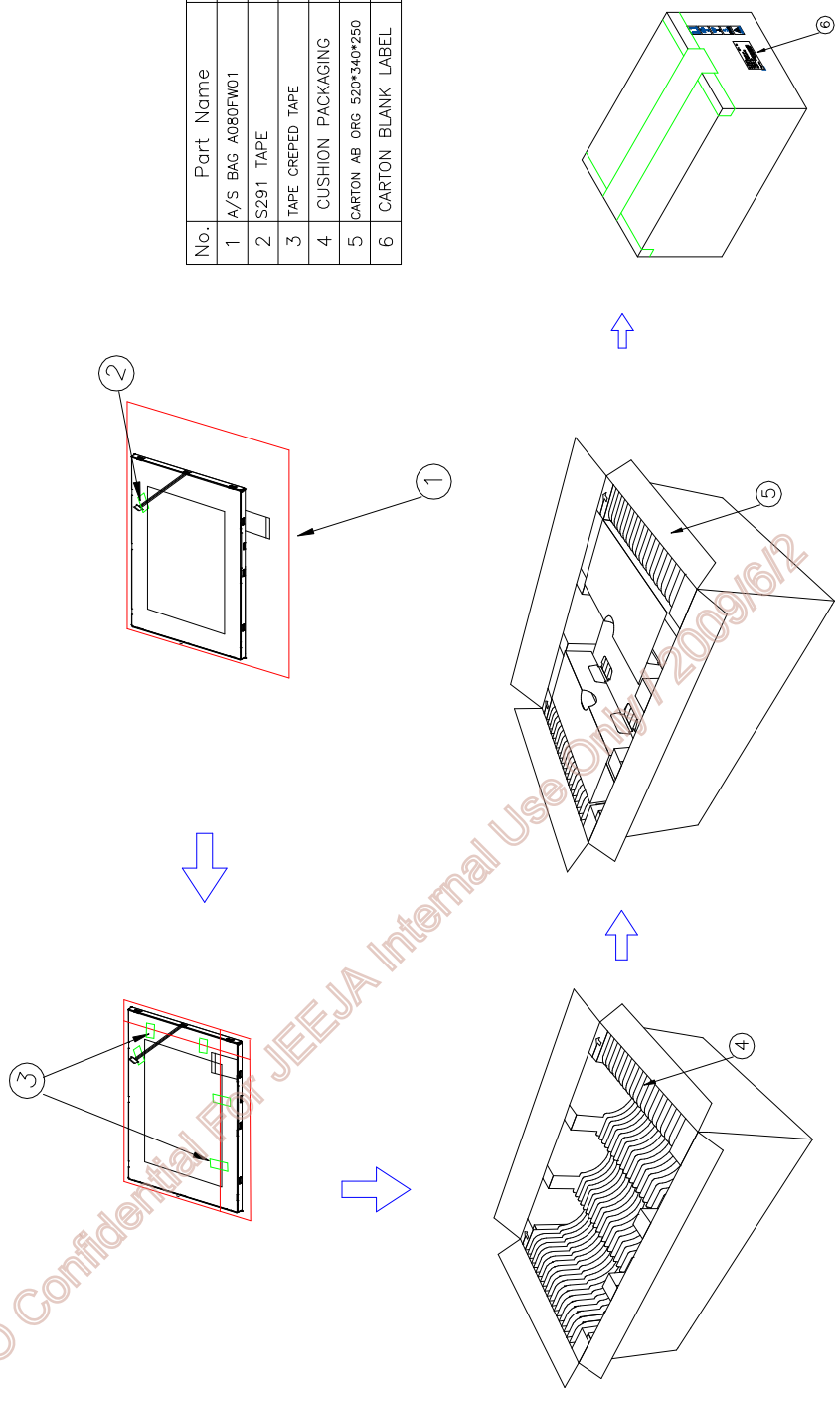




F. Packing and Marking

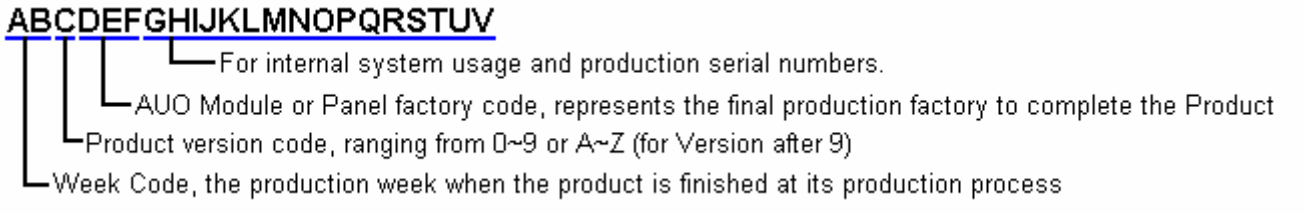
1. Packing Form

No.	Part Name	Part No.
1	A/S BAG A080FW01	79.08A02.001
2	S291 TAPE	84.01A04.001
3	TAPE CREPED TAPE	80.07C01.004
4	CUSHION PACKAGING	83.08A07.001
5	CARTON AB ORG 520*340*250	81.01A09.003
6	CARTON BLANK LABEL	82.17B02.001



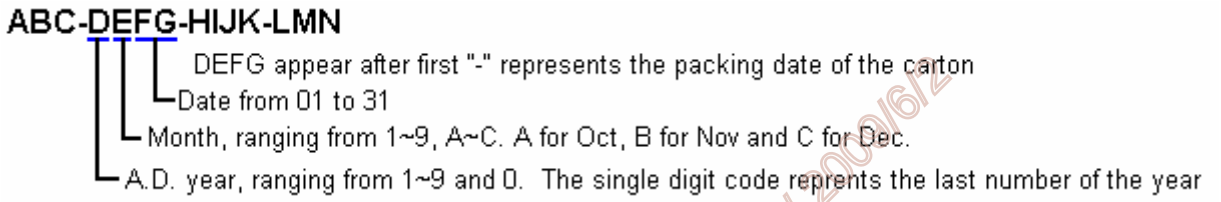
2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

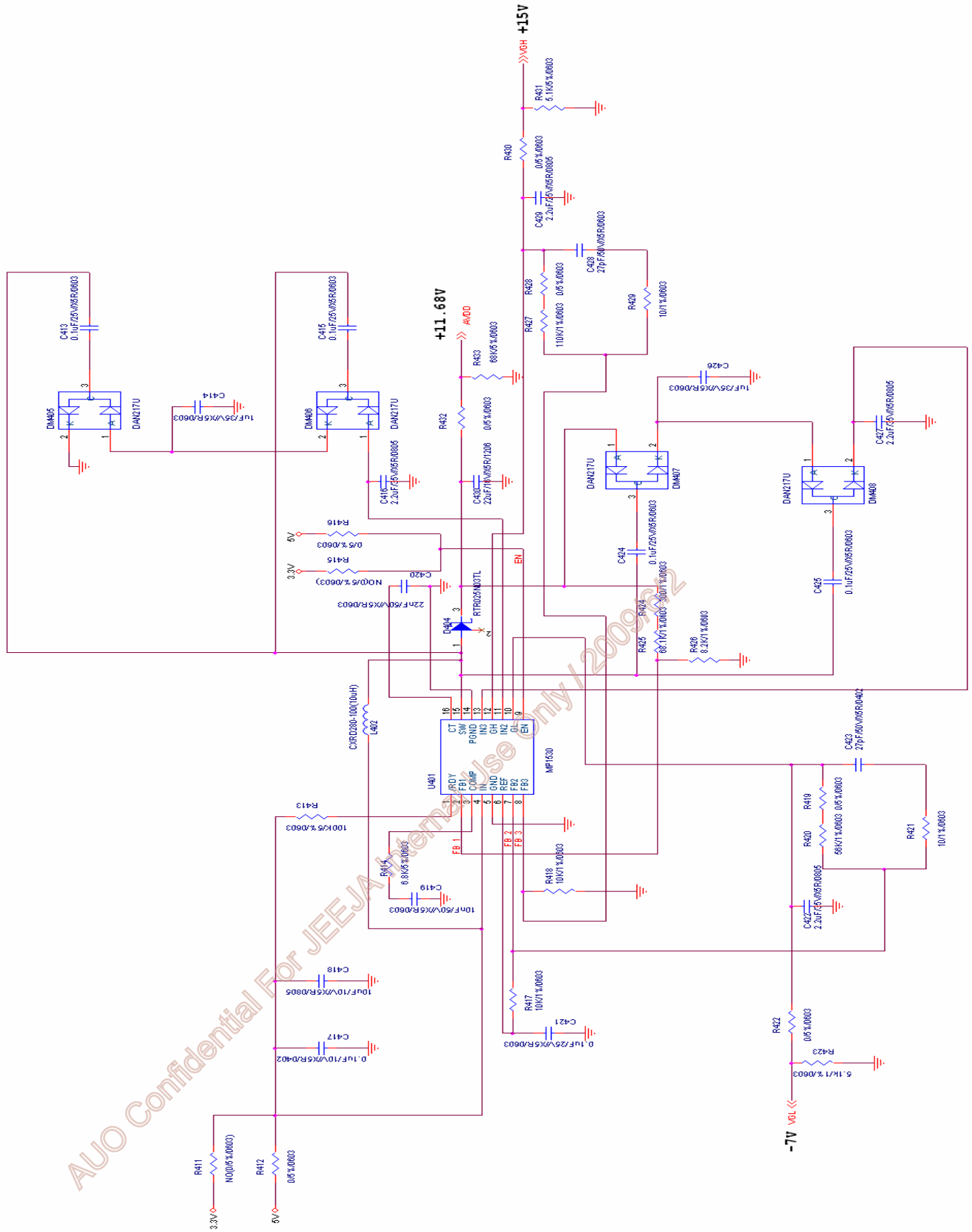
The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



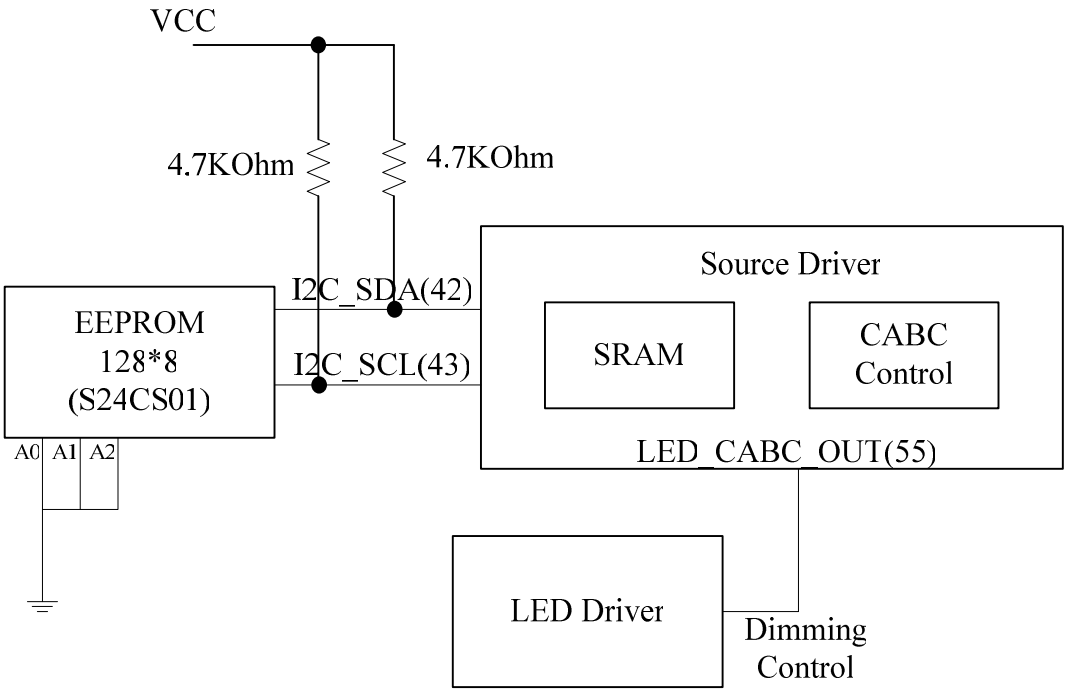
Refer to the drawing of packing format for the location and size of the carton label.

G. Application Note

1. Application Circuit



2. CABC function block



H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.