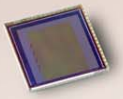
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/5" color CMOS QSXGA (3 megapixel) image sensor
with OmniBSI™ technology

OV3660

color CMOS QSXGA (3 megapixel) image sensor with OmniBSI™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.2
january 2011

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV03660-A51A** (color, lead-free)
  51-pin CSP3

features

- 1.4 µm x 1.4 µm pixel with OmniBSI technology for high performance (high sensitivity, low crosstalk, low noise, improved quantum efficiency)
- optical size of 1/5"
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic flicker detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, CCIR656, YCbCr422, and compression
- support for LED and flash strobe mode
- support for horizontal and vertical sub-sampling, binning
- support 2x2 binning with binning filter to minimize binning artifacts
- support for data compression output
- standard serial SCCB interface (see **section 2.10** for details)
- digital video port (DVP) parallel output interface
- embedded 1.5V regulator for core power
- programmable I/O drive capability, I/O tri-state configurability
- support for black sun cancellation
- support for images sizes: 3 megapixel and any arbitrary size scaling down from 3 megapixel
- suitable for module size of 6.5 x 6.5 x <6mm

key specifications (typical)

- **active array size:** 2048 x 1536
- **power supply:**
  core: 1.5V ± 5% (with embedded 1.5V regulator)
  analog: 2.6 ~ 3.0V (2.8V typical)
  I/O: 1.8V / 2.8V (1.8V recommended)
- **power requirements:**
  active: 98 mA
  standby: 20 µA
- **temperature range:**
  operating: -20°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats:** 8-/10-bit RAW, RGB and YCbCr output, compression
- **lens size:** 1/5"
- **lens chief ray angle:** 27.6° (see **figure 10-2**)
- **input clock frequency:** 6~27 MHz
- **max S/N ratio:** 34 dB
- **dynamic range:** 70 dB @ 8x gain
- **maximum image transfer rate:**
  2048x1536: 15 fps
  1080p: 20 fps
  720p: 45 fps
  XGA (1024x768): 45 fps
  VGA (640x480): 60 fps
  QVGA (320x240): 120 fps
- **sensitivity:** 670 mV/Lux-sec
- **shutter:** rolling shutter
- **maximum exposure interval:** 1560 x t_{ROW}
- **pixel size:** 1.4 µm x 1.4 µm
- **dark current:** TBD
- **image area:** 2912 µm x 2167.2 µm
- **package dimensions:** 5010 µm x 4960 µm

note pixel performance shown are target values. These values are subject to change based on real measurements.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV3660 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
A1	DVDD	power	power for digital circuit
A2	DOGND	ground	ground for digital circuit
A3	NC	–	no connect
A4	NC	–	no connect
A5	NC	–	no connect
A6	NC	–	no connect
A7	VNH	reference	internal analog reference
A8	VH	reference	internal analog reference
B1	**HREF**	I/O	video output horizontal sync signal
B2	**XVCLK**	input	system input clock/scan clock input
B3	DOVDD	power	power for I/O circuit
B6	VNL	reference	internal analog reference
B7	AGND	ground	ground for analog circuit
B8	AGND	ground	ground for analog circuit
C1	**D8**	I/O	image data output 8
C2	**D9**	I/O	image data output 9
C3	NC	–	no connect
C6	**RESETB**	input	reset (active low with internal pull-up resistor)
C7	AVDD	power	power for analog circuit
C8	AVDD	power	power for analog circuit
D1	**D6**	I/O	image data output 6
D2	**D7**	I/O	image data output 7
D3	DOGND	ground	ground for digital circuit
D6	DOGND	ground	ground for digital circuit
D7	DOGND	ground	ground for digital circuit
D8	DOGND	ground	ground for digital circuit

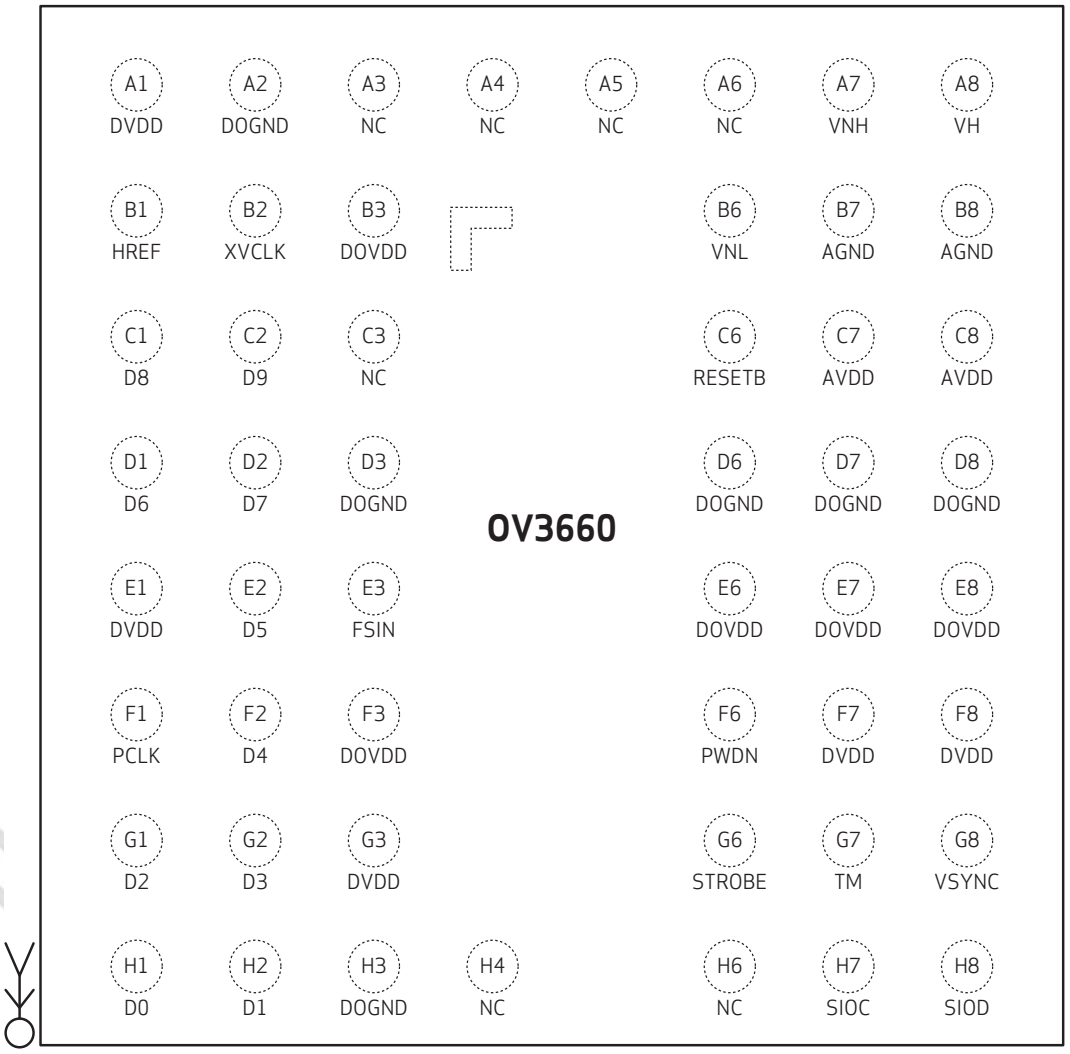
table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
E1	DVDD	power	power for digital circuit
E2	**D5**	I/O	image data output 5
E3	**FSIN**	I/O	frame sync
E6	DOVDD	power	power for I/O circuit
E7	DOVDD	power	power for I/O circuit
E8	DOVDD	power	power for I/O circuit
F1	**PCLK**	I/O	image output clock
F2	**D4**	I/O	image data output 4
F3	DOVDD	power	power for I/O circuit
F6	**PWDN**	input	power down (active high with pull down resistor)
F7	DVDD	power	power for digital circuit
F8	DVDD	power	power for digital circuit
G1	**D2**	I/O	image data output 2
G2	**D3**	I/O	image data output 3
G3	DVDD	power	power for digital circuit
G6	**STROBE**	I/O	LED/flash control
G7	**TM**	input	test mode (active high with pull down resistor)
G8	**VSYNC**	I/O	video output vertical sync signal
H1	**D0**	I/O	image data output 0
H2	**D1**	I/O	image data output 1
H3	DOGND	ground	ground for digital circuit
H4	NC	–	no connect
H6	NC	–	no connect
H7	**SIOC**	input	SCCB input clock
H8	**SIOD**	I/O	SCCB data

table 1-2 configuration under various conditions

pin	signal name	RESET	after RESET release	software standby	hardware standby (PWDNB = 0)
B1	HREF	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
B2	XVCLK	input	input	input	high-z
C1	D8	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
C2	D9	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
C6	RESETB	input	input	input	input
D1	D6	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
D2	D7	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
E2	D5	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
E3	FSIN	input	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
F1	PCLK	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
F2	D4	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
F6	PWDN	input	input	input	input
G1	D2	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
G2	D3	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
G6	STROBE	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
G7	TM	input	input	input	input
G8	VSYNC	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
H1	D0	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
H2	D1	high-z	high-z by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
H7	SIOC	input	input	input	high-z
H8	SIOD	input	input	input	high-z

figure 1-1 pin diagram



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top view

table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

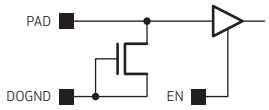
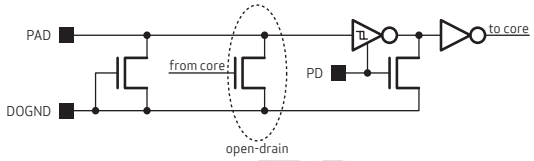
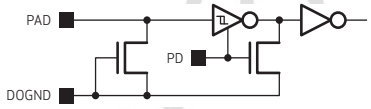
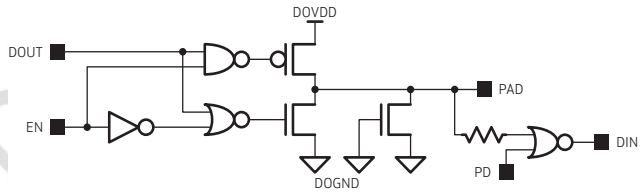
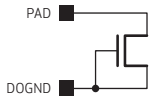
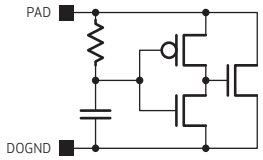
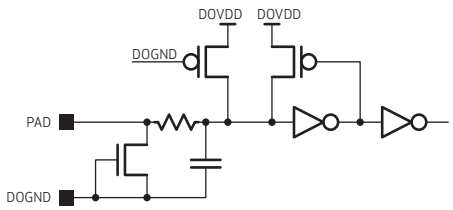
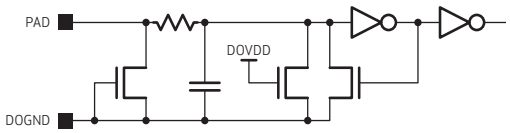
symbol	equivalent circuit
XVCLK	
SIOD	
SIOC	
D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, VSYNC, STROBE, FSIN	
AGND, DOGND, DGND	
AVDD, DVDD, DOVDD	
RESETB	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
TM, PWDN	

2 system level description

2.1 overview

The OV3660 (color) image sensor is a low voltage, high-performance, 1/5-inch 3 megapixel CMOS image sensor that provides the full functionality of a single chip 3 megapixel (2048x1536) camera using OmniBSI™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV3660 has an image array capable of operating at up to 15 frames per second (fps) in 3 megapixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. The OV3660 also includes a compression engine for increased processing power. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For identification and storage purposes, the OV3660 includes a one-time programmable (OTP) memory.

The OV3660 supports a digital video parallel port.

2.2 architecture

The OV3660 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV3660 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of the array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV3660 block diagram

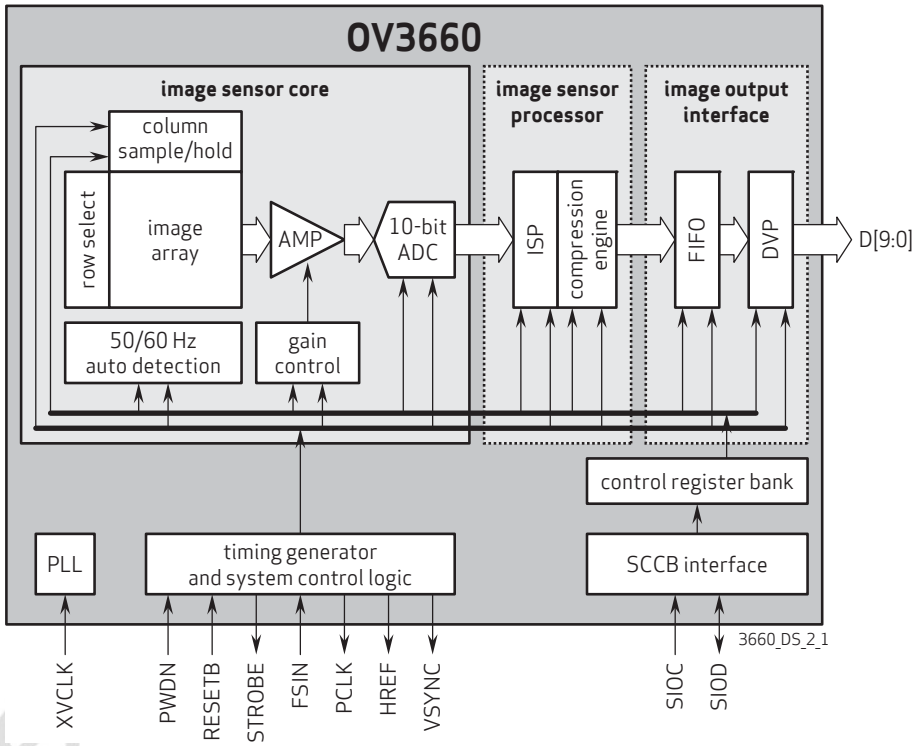
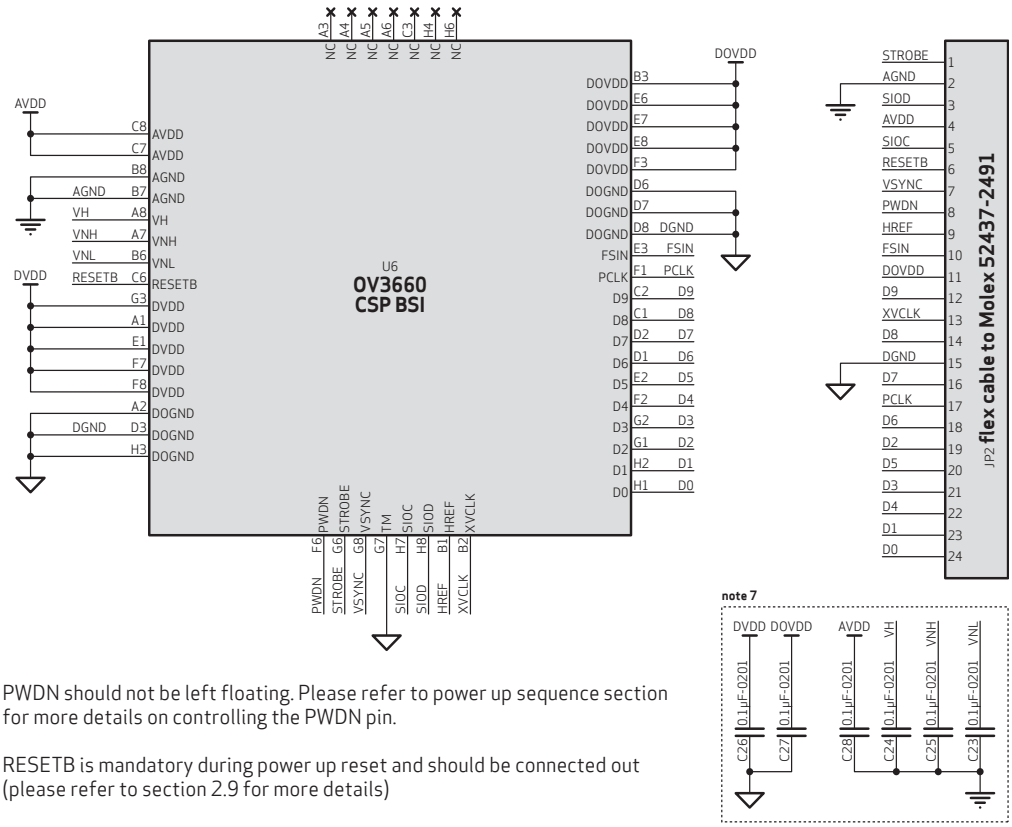


figure 2-2 reference design schematic



note 1 PWDN should not be left floating. Please refer to power up sequence section for more details on controlling the PWDN pin.

note 2 RESETB is mandatory during power up reset and should be connected out (please refer to section 2.9 for more details)

note 3 AVDD is 2.8 V of sensor analog power (clean). During OTP programming, an AVDD voltage range of 2.5 V ±5% is required. OTP read may use normal AVDD voltage range.

note 4 DOVDD is 1.7 - 3 V of sensor digital IO power (clean). 1.8 V is recommended.

note 5 DVDD is 1.5 V sensor core power (clean). DVDD can be provided by internal regulator (recommended).

note 6 sensor AGND and DGND should be separated and connected to a single point outside module (do not connect inside module).

note 7 capacitors should be close to the related sensor pins.

note 8 if more space is available, use a capacitor of 1 µF-0402 between DVDD and DGND

note 9 D[9:0] (D9:MSB, D0:LSB) is sensor RGB raw 10-bit output
D[9:2] (D9:MSB, D2:LSB) is 8-bit output.

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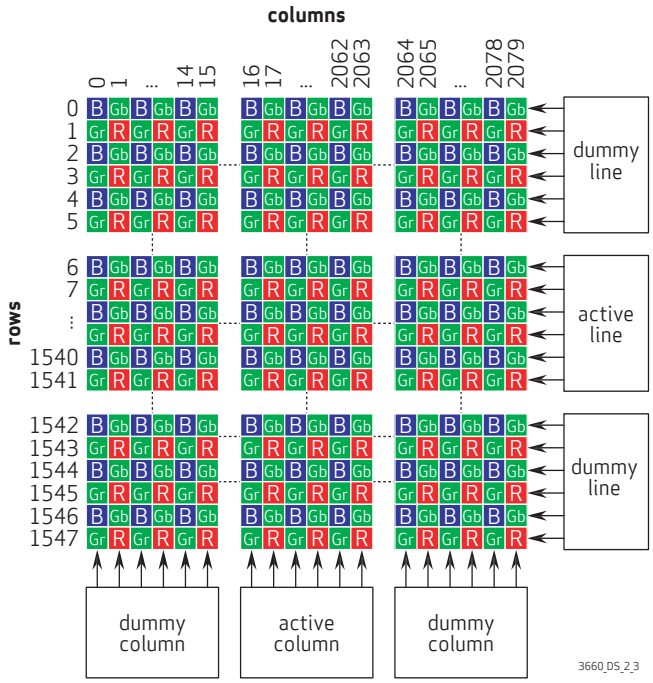
2.3 pixel array structure

The OV3660 sensor has an image array of 2080 columns by 1548 rows (3,219,840 pixels). **figure 2-3** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,219,840 pixels, 3,145,728 (2048x1536) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 2-3 sensor array region color filter layout



2.3.1 binning

Binning mode is usually used for low resolution. When the binning function is ON, voltage levels of adjacent pixels are averaged before sent to the ADC. If the binning function is OFF, the pixels, which are not output, are merely skipped. The OV3660 supports 2x2 binning, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged before entering the ADC.

figure 2-4 illustrates 2x2 binning, where the voltage levels of four (2x2) adjacent same-color pixels are averaged before entering the ADC.

figure 2-4 example of 2x2 binning

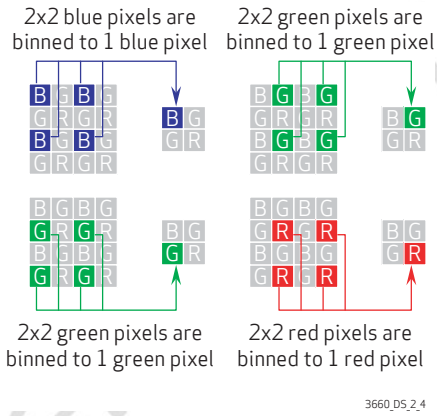


table 2-1 binning-related registers

address	register name	default value	R/W	description	
0x3820	TIMING TC REG20	0x64	RW	Bit[0]:	Vertical binning enable
0x3821	TIMING TC REG21	0x0C	RW	Bit[0]:	Horizontal binning enable

2.4 power up sequence

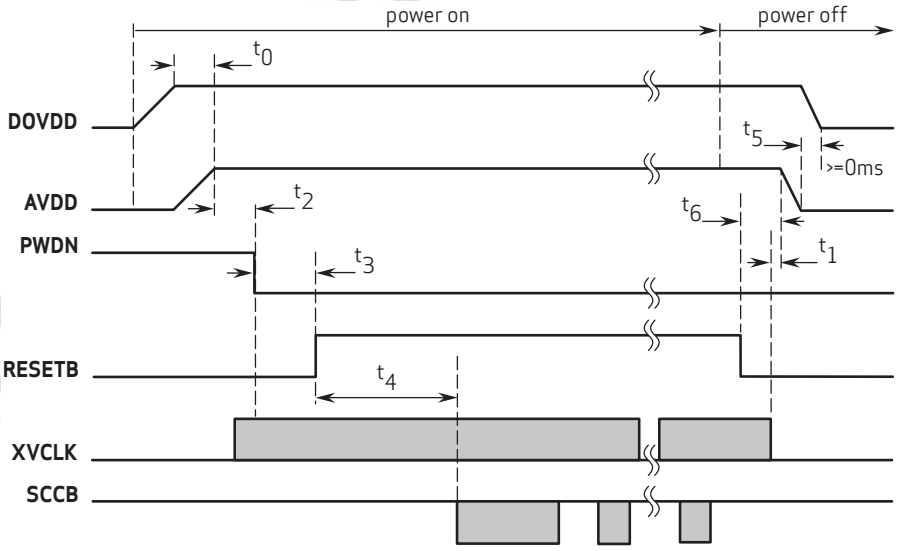
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.4.1 power up with internal DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high during the power on period
4. for PWDN to go low, power must first become stable (AVDD to PWDNB ≥ 5 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power on period once DOVDD is up
7. master clock XVCLK should provide at least 2 ms before host accesses the sensor's registers
8. host can access I2C bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESETB goes high if reset is inserted after PWDN goes low, host can access the sensor's registers to initialize sensor

figure 2-5 power up timing with internal DVDD



note $t_0 \geq 0$ms, delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
$t_1 \geq 0$ms, delay from XVCLK off to AVDD off
$t_2 \geq 5$ms, delay from AVDD stable to sensor power up stable, PWDN can be pulled low after this point, XVCLK can be turned on after power on
$t_3 \geq 1$ms, delay from sensor power up stable to RESETB pull up
$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization
$t_5 \geq 0$ms, delay from AVDD off to DOVDD off
$t_6 \geq 0$ms, delay from RESETB pull low to AVDD off

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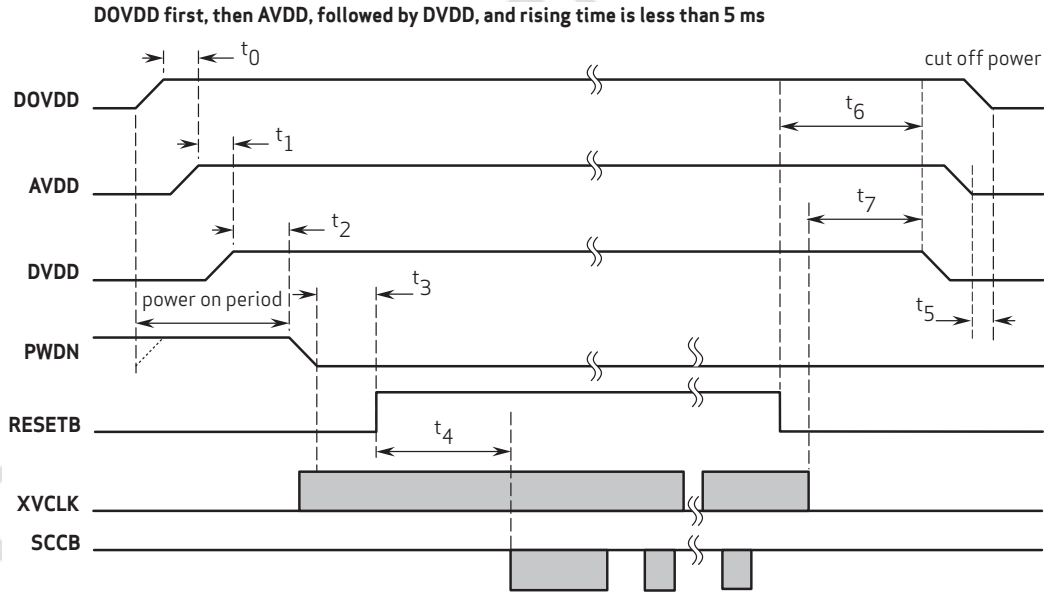
2.4.2 power up with external DVDD source

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power must first become stable (DVDD to PWDNB ≥ 5 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power on period once DOVDD is up
8. master clock XVCLK should provide at least 2 ms before host accesses the sensor's registers
9. host can access I2C bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESETB goes high if reset is inserted after PWDN goes high, host can access the sensor's registers to initialize sensor

figure 2-6 power up timing with external DVDD source



note $t_0 \geq 0$ ms: delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
$t_1 \geq 0$ ms: delay from AVDD stable to DVDD stable
$t_2 \geq 5$ ms: delay from DVDD stable to sensor power up stable
$t_3 \geq 1$ms, delay from sensor power up stable to RESETB pull up
$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization
$t_5 \geq 0$ms, delay from AVDD off to DOVDD off
$t_6 \geq 0$ms, delay from RESETB pull low to DVDD off
$t_7 \geq 0$ms, delay from XVCLK off to DVDD off

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2.5 reset

The OV3660 sensor includes a RESETB pin (pin C6) that forces a complete hardware reset when it is pulled low (GND). The OV3660 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register **0x3008**[7] to high. Reset requires ~2ms settling time.

2.5.1 power ON reset generation

The power on reset can be controlled from the RESETB pin. However, inside this chip, a power on reset is generated after power is stable.

2.6 hardware and software standby

Two suspend modes are available for the OV3660:

- **hardware standby**
- **software standby**

2.6.1 hardware standby

To initiate a hardware standby, the PWDN pin (pin F6) must be tied to high. When this occurs, the OV3660 internal device clock is halted and all internal counters are reset and registers are maintained. Majority of the digital circuitry will remain in the power-cut state.

2.6.2 software standby

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.7 format and frame rate

table 2-2 format and frame rate

format	resolution	frame rate	scaling method	system clock
3 megapixel	2048x1536	15 fps	full resolution	54 MHz
1080p	1920x1080	20 fps	cropping from full resolution	54 MHz
720p	1280x720	45 fps	cropping from full resolution	54 MHz
XGA	1024x768	45 fps	subsampling in vertical and horizontal	54 MHz
VGA	640x480	60 fps	subsampling from 1280x960	27 MHz
QVGA	320x240	120 fps	subsampling from 1280x960	27 MHz

2.7.1 output format control

table 2-3 output format control registers

address	register name	default value	R/W	description
0x501F	FORMAT CTRL	0x03	RW	Format Control[a] Bit[2:0]: Format select 000: YUV422 001: RGB 010: Dither 011: RAW after DPC 101: RAW after CIP

a. for details, contact your local OmniVision FAE for the software application note

2.7.1.1 format description

Format control converts the internal data format into the desired output format including YUV, RGB, or RAW. Format setting should also combine with 0x501F.

table 2-4 format control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4300	FORMAT CTRL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format selection 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: Not used 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4~0x5: Not used 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]}

table 2-4 format control registers (sheet 2 of 4)

address	register name	default value	R/W	description
				0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xF: Not allowed 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]} 0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]} 0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]} 0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x7: {r[4:0],1'b0,g[4:2]}, {g[2:0],b[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed 0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]}

table 2-4 format control registers (sheet 3 of 4)

address	register name	default value	R/W	description
				0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xF: Not allowed 0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0,g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0,g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0,r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0,b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0,b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0,r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed

table 2-4 format control registers (sheet 4 of 4)

address	register name	default value	R/W	description
				0xF: Bypass formatter module Bit[3:0]: Output format 0x8: Raw 0x9: YUV422
0x4301	FORMAT CTRL 01	0x00	RW	Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 10: Not valid 11: U/V generated from second pixel
0x4302	YMAX VALUE	0x03	RW	Bit[1:0]: Set y max clip value[9:8]
0x4303	YMAX VALUE	0xFF	RW	Bit[7:0]: Set y max clip value[7:0]
0x4304	YMIN VALUE	0x00	RW	Bit[1:0]: Set y min clip value[9:8]
0x4305	YMIN VALUE	0x00	RW	Bit[7:0]: Set y min clip value[7:0]
0x4306	UMAX VALUE	0x03	RW	Bit[1:0]: Set u max clip value[9:8]
0x4307	UMAX VALUE	0xFF	RW	Bit[7:0]: Set u max clip value[7:0]
0x4308	UMIN VALUE	0x00	RW	Bit[1:0]: Set u min clip value[9:8]
0x4309	UMIN VALUE	0x00	RW	Bit[7:0]: Set u min clip value[7:0]
0x430A	VMAX VALUE	0x03	RW	Bit[1:0]: Set v max clip value[9:8]
0x430B	VMAX VALUE	0xFF	RW	Bit[7:0]: Set v max clip value[7:0]
0x430C	VMIN VALUE	0x00	RW	Bit[1:0]: Set v min clip value[9:8]
0x430D	VMIN VALUE	0x00	RW	Bit[7:0]: Set v min clip value[7:0]

2.8 I/O control

The I/O control allows the user to configure the I/O pad direction to either be an input or output. In addition, the I/O control also allows the user to set the driving capability for the output. Please take note that the driving capability is not independently controlled for each output. Setting the driving capability will apply to all configured outputs. **table 2-5** lists the driving capability and direction control registers of the I/O pads.

note
To achieve optimal signal quality, for high speed and high capacitance loading designs, OmniVision recommends using a higher drive capability. Conversely, for low speed and low capacitance loading, use a lower driving capability setting.

table 2-5 driving capability and direction control for I/O pads (sheet 1 of 2)

function	register	default value	R/W	description
output drive capability control	0x302C	0x02	RW	Bit[7:6]: output drive capability for all I/O type pads (see **table 1-2**) 00: 1x 01: 2x 10: 3x 11: 4x
D[9:0] I/O control	0x3017[3:0], 0x3018[7:2]	0x00	RW	input/output control for the D[9:0] pins 0: input 1: output
D[9:0] output select	0x301D[3:0], 0x301E[7:2]	0x00	RW	output selection for the D[9:0] pins 0: normal data path 1: register-controlled value
D[9:0] output value	0x301A[3:0], 0x301B[7:2]	0x00	RW	D[9:0] output value
D[9:0] input value	0x3051[3:0], 0x3052[7:2]	–	R	D[9:0] input value
VSYNC I/O control	0x3017	0x00	RW	Bit[6]: input/output control for the VSYNC pin 0: input 1: output
VSYNC output select	0x301D	0x00	RW	Bit[6]: output selection for the VSYNC pin 0: normal data path 1: register-controlled value
VSYNC output value	0x301A	0x00	RW	Bit[6]: VSYNC output value
VSYNC input value	0x3051	–	R	Bit[6]: VSYNC input value
HREF I/O control	0x3017	0x00	RW	Bit[5]: input/output control for the HREF pin 0: input 1: output

table 2-5 driving capability and direction control for I/O pads (sheet 2 of 2)

function	register	default value	R/W	description
HREF output select	0x301D	0x00	RW	Bit[5]: output selection for the HREF pin 0: normal data path 1: register-controlled value
HREF output value	0x301A	0x00	RW	Bit[5]: HREF output value
HREF input value	0x3051	–	R	Bit[5]: HREF input value
PCLK I/O control	0x3017	0x00	RW	Bit[4]: input/output control for the PCLK pin 0: input 1: output
PCLK output select	0x301D	0x00	RW	Bit[4]: output selection for the PCLK pin 0: normal data path 1: register-controlled value
PCLK output value	0x301A	0x00	RW	Bit[4]: PCLK output value
PCLK input value	0x3051	–	R	Bit[4]: PCLK input value

2.9 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers.

table 2-6 system control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3000~ 0x3003	SYSTEM RESET00~ SYSTEM RESET03	–	RW	Reset for Individual Blocks
0x3004~ 0x3007	CLOCK ENABLE00~ CLOCK ENABLE03	–	RW	Clock Enable Control for Individual Blocks
0x3008	SYSTEM CTROL0	0x02	RW	System Control Bit[7]: Software reset Bit[6]: Software power down Bit[5]: Reserved Bit[4]: SRB clock SYNC enable Bit[3]: Isolation suspend select Bit[2:0]: Not used
0x300A	SENSOR CHIP ID HIGH BYTE	0x36	R	Chip ID High Byte
0x300B	SENSOR CHIP ID LOW BYTE	0x60	R	Chip ID Low Byte
0x3016	PAD OUTPUT ENABLE 00	0x22	RW	Input/Output Control (0: input; 1: output) Bit[2]: FSIN output enable Bit[1]: STROBE output enable Bit[0]: Not used
0x3017	PAD OUTPUT ENABLE 01	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: Not used Bit[6]: VSYNC output enable Bit[5]: HREF output enable Bit[4]: PCLK output enable Bit[3:0]: D[9:6] output enable
0x3018	PAD OUTPUT ENABLE 02	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7:2]: D[5:0] output enable Bit[1:0]: Not used
0x3019	PAD OUTPUT VALUE 00	0xF0	RW	PAD Output Value Bit[7:3]: Not used Bit[2]: FSIN Bit[1]: STROBE Bit[0]: Not used

table 2-6 system control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x301A	PAD OUTPUT VALUE 01	0x00	RW	GPIO Output Value Bit[7]: Reserved Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x301B	PAD OUTPUT VALUE 02	0x00	RW	GPIO Output Value Bit[7:2]: D[5:0] Bit[1:0]: Not used
0x301C	PAD SEL0	0x00	RW	Pad select control Bit[2]: IO FSIN select Bit[1]: IO STROBE select Bit[0]: Not used
0x301D	PAD SEL1	0x00	RW	Pad select control Bit[7]: Not used Bit[6]: IO VSYNC select Bit[5]: IO HREF select Bit[4]: IO PCLK select Bit[3:0]: IO D[9:6] select
0x301E	PAD SEL2	0x00	RW	Pad select control Bit[7:2]: IO D[5:0] select Bit[1:0]: Not used
0x302A	CHIP REVISION	–	R	Bit[7:4]: Process 0xB: BSI Bit[3:0]: Chip revision
0x302C	PAD CONTROL	0x03	RW	Pad control Bit[7:6]: Pad driving strength 00: 1x 01: 2x 10: 3x 11: 4x Bit[5]: pd_dato_en Bit[4:2]: Reserved Bit[1]: FSIN input enable Bit[0]: STROBE input enable
0x303A	SC PLLS CTRL0	0x00	RW	Bit[7]: PLLS bypass Bit[6:0]: Reserved
0x303B	SC PLLS CTRL1	0x1B	RW	Bit[4:0]: PLLS multiplier
0x303C	SC PLLS CTRL2	0x11	RW	Bit[6:4]: PLLS charge pump control Bit[3:0]: PLLS system divider

table 2-6 system control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x303D	SC PLLS CTRL3	0x30	RW	Bit[5:4]: PLLS predivider 00: /1 01: /1.5 10: /2 11: /3 Bit[3]: Not used Bit[2]: PLLS root divider 0: /1 1: /2 Bit[1:0]: PLLS seld5 00: /1 01: /1 10: /2 11: /2.5
0x3050	IO PAD VALUE	–	R	Read pad value Bit[7:4]: Not used Bit[3]: PWDN Bit[2]: Not used Bit[1]: SIOC
0x3051	IO PAD VALUE	–	R	Read pad value Bit[7]: OTP memory out Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x3052	IO PAD VALUE	–	R	Read pad value Bit[7:2]: D[5:0] Bit[1:0]: Not used

2.9.1 system clock control

The OV3660 PLL allows input clock frequency from 6~27 MHz and has VCO frequency of 150MHz~500MHz. SYS_CLK is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x303A[7] to 1.

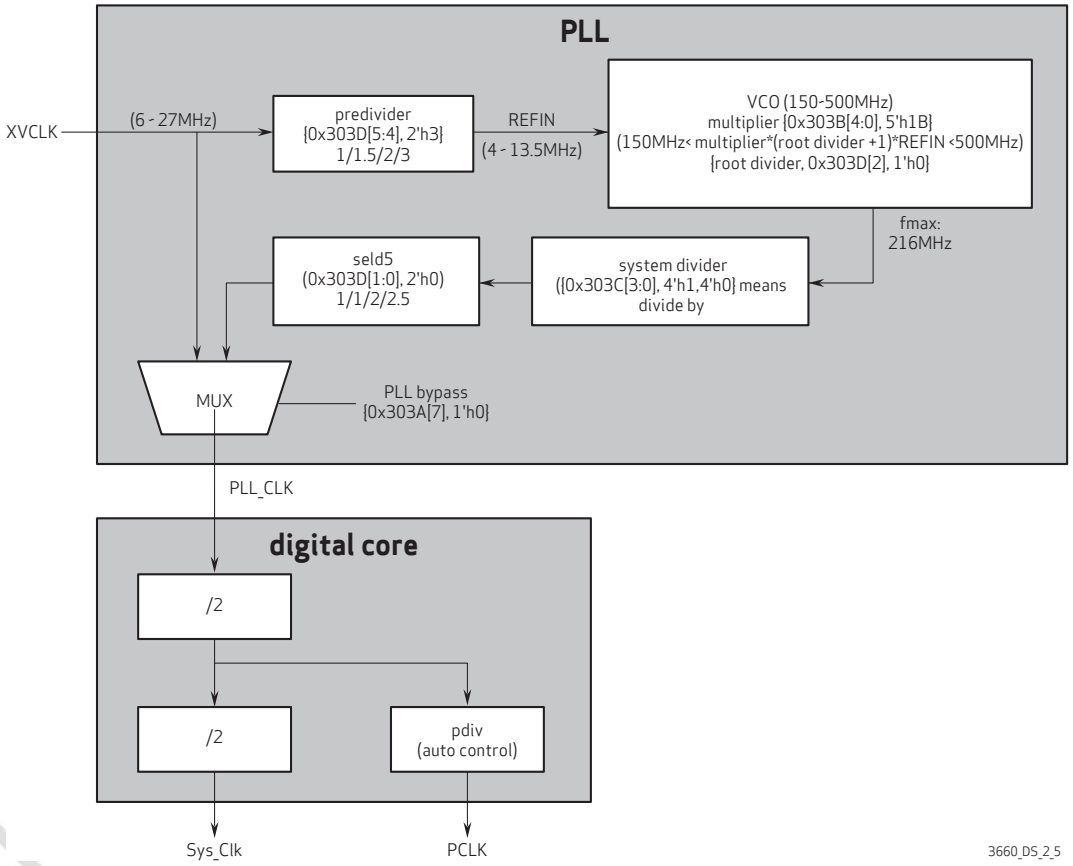
By default, the PCLK frequency is decided by the horizontal scaling ratio. Refer to **table 2-7** for the auto PCLK divider ratio. When 0x460C[1] is set to 1, the PCLK divider ratio is manually set by 0x3824[4:0].

CF = horizontal input size / horizontal output size

table 2-7 PCLK divider ratio

horizontal scaling factor (CF)	PCLK divider ratio
CF<2	1
2<=CF<4	2
4<=CF<8	4
8<=CF<16	8
CF>16	16

figure 2-7 PLL block diagram



note
Contact your local OVT FAE for additional assistance on PLL configuration.

table 2-8 PLL configurations

configuration	register 0x303A	register 0x303B	register 0x303C	register 0x303D	register 0x3824	register 0x460C
default[a]	0x00	0x1B	0x11	0x30	0x01	0x20
(sample 1)[b]	0x00	0x1B	0x12	0x30	0x01	0x20

a. default settings are for 54MHz pixel clock, sensor output of 3 Mpixel at 15 fps, and DVP output

b. sample settings are for 54MHz pixel clock, sensor output of 3 Mpixel at 7.5 fps and DVP output

table 2-9 PLL control registers

address	register name	default value	R/W	description
0x303A	SC PLLS CTRL0	0x00	RW	Bit[7]: PLLS bypass Bit[6:0]: Reserved
0x303B	SC PLLS CTRL1	0x1B	RW	Bit[4:0]: PLLS multiplier
0x303C	SC PLLS CTRL2	0x11	RW	Bit[6:4]: PLLS charge pump control Bit[3:0]: PLLS system divider
0x303D	SC PLLS CTRL3	0x30	RW	Bit[5:4]: PLLS predivider 00: /1 01: /1.5 10: /2 11: /3 Bit[2]: PLLS root divider 0: /1 1: /2 Bit[1:0]: PLLS seld5 00: /1 01: /1 10: /2 11: /2.5
0x3824	TIMING TC REG24	0x01	RW	Bit[7:5]: Not used Bit[4:0]: PCLK ratio manual
0x460C	VFIFO CTRL0C	0x20	RW	Bit[1]: PCLK manual enable 0: DVP PCLK divider control by auto mode 1: DVP PCLK divider control by 0x3824[4:0]

2.10 group write

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV3660 supports up to four groups. These groups share 512 MB RAM and the size of each group is programmable by adjusting the start address.

table 2-10 group write registers

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

3 image sensor core digital functions

3.1 mirror and flip

The OV3660 Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 3-1**).

figure 3-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

3660_DS_4_1

table 3-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING TC REG20	0x40	RW	Timing Control Register Bit[2:1]: Vertical flip enable[a] 00: Normal 11: Vertical flip
0x3821	TIMING TC REG21	0x00	RW	Timing Control Register Bit[2:1]: Horizontal mirror enable[b] 00: Normal 11: Horizontal mirror[c]

a. for full size flip, it is necessary to set register 0x4514 to 0x88

b. for full size mirror + flip, also set register 0x4514 to 0xBB

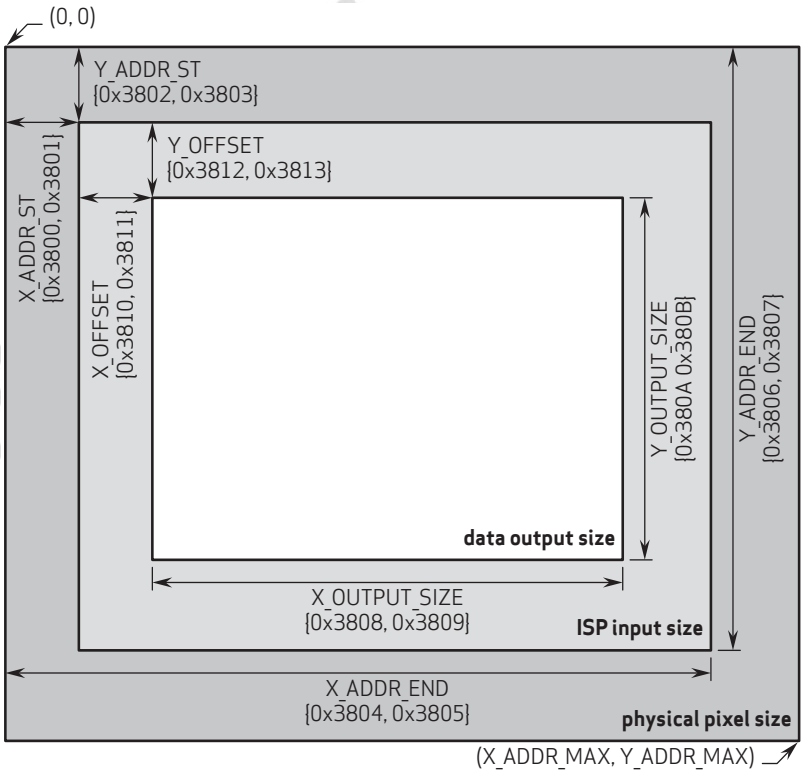
c. for bin + mirror, set register 0x4514 to 0xBB

3.2 image windowing and scaling

3.2.1 image windowing

The OV3660 uses registers 0x3800 ~ 0x3814 for image windowing. **figure 3-2** illustrates how the registers define the windowing size. Physical pixel size is the total pixel array size we have in the sensor. The ISP input size is the total pixel data read from pixel array. Typically, the larger ISP input size is, the less maximum frame rate can be reached. The data output size is the image output size of OV3660. This size is windowed from ISP input size and is defined by x_offset and y_offset as **figure 3-2** shows.

figure 3-2 image windowing



3660_DS_4_2

figure 3-3 shows the windowing configuration when scaling function is enabled. The pre-scaling image size is the ISP input size subtracted by two times of offsets for both horizontal and vertical.

figure 3-3 image windowing configuration

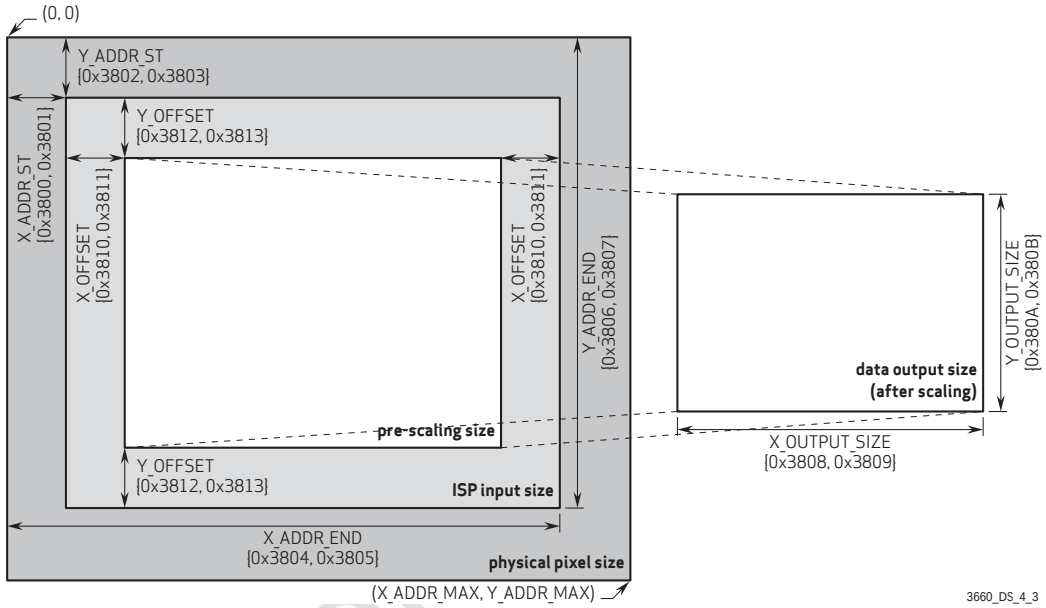


table 3-2 image windowing registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[3:0]: X address start[11:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: X address start[7:0]
0x3802	TIMING VS	0x00	RW	Bit[2:0]: Y address start[10:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: Y address start[7:0]
0x3804	TIMING HW	0x08	RW	Bit[3:0]: X address end[11:8]
0x3805	TIMING HW	0x1F	RW	Bit[7:0]: X address end[7:0]
0x3806	TIMING VH	0x06	RW	Bit[2:0]: Y address end[10:8]
0x3807	TIMING VH	0x0B	RW	Bit[7:0]: Y address end[7:0]
0x3808	TIMING DVPHO	0x08	RW	Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x00	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x06	RW	Bit[2:0]: DVP output vertical height[10:8]

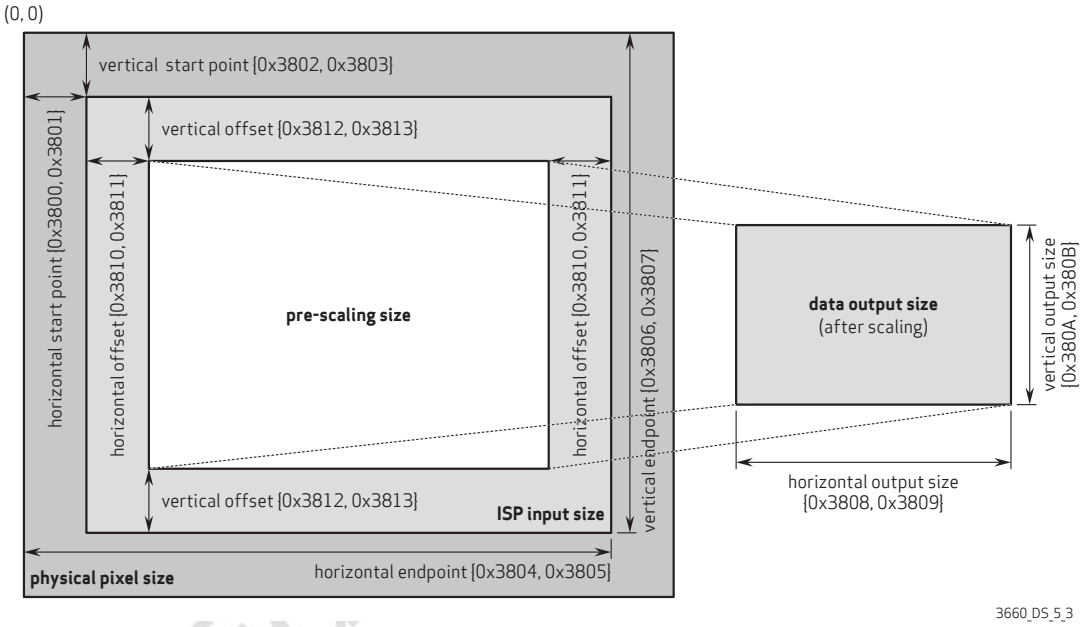
table 3-2 image windowing registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x380B	TIMING DVPVO	0x00	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING HTS	0x08	RW	Bit[3:0]: Total horizontal size[11:8]
0x380D	TIMING HTS	0xFC	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING VTS	0x06	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0x1C	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFSET	0x00	RW	Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING HOFFSET	0x10	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[2:0]: ISP vertical offset[10:8]
0x3813	TIMING VOFFSET	0x06	RW	Bit[7:0]: ISP vertical offset[7:0]

3.2.2 scaling

The OV3660 includes a scalar function that allows the user to arbitrarily set an output image size (width and height) up to 1/32 of the designated array size. The scalar module outputs the specified image size and maintains the field-of-view as the input image to the scalar. Note that the frame rate will not change in scaling mode.

figure 3-4 scaling function



The following steps allow the user to set their required output size:

1. The scaling function is enabled and disabled by register bit 0x5001[5]. The user then needs to set the image input size, output size and offset. The output size < (input size - 2 offset).

   Horizontal output size: {0x3808, 0x3809}

   Vertical output size: {0x380A, 0x380B}

   Horizontal offset: {0x3810, 0x3811}

   Vertical offset: {0x3812, 0x3813}

   Horizontal input size: Horizontal endpoint {0x3804, 0x3805} - Horizontal start point {0x3800, 0x3801} + 1 - 2 x {0x3810, 0x3811}

   Vertical input size: Vertical endpoint {0x3806, 0x3807} - Vertical start point {0x3802, 0x3803} + 1 - 2 x {0x3812, 0x3813}

2. The scaling factor is calculated automatically.

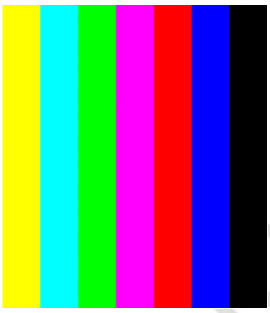
table 3-3 scaling control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Scale enable 0: Disable 1: Enable
0x5601	SCALE CTRL 1	0x00	RW	Bit[6:4]: HDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 100: DCW 8 times 101: DCW 16 times Others: DCW 16 times Bit[2:0]: VDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 100: DCW 8 times 101: DCW 16 times Others: DCW 16 times
0x5602	SCALE CTRL 2	0x02	RW	XSC High Bits
0x5603	SCALE CTRL 3	0x00	RW	XSC Low Bits
0x5604	SCALE CTRL 4	0x02	RW	YSC High Bits
0x5605	SCALE CTRL 5	0x00	RW	YSC Low Bits
0x5606	SCALE CTRL 6	0x00	RW	Bit[3:0]: Voffset
0x3804	TIMING HW	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF horizontal endpoint[11:8]
0x3805	TIMING HW	0xDF	RW	Bit[7:0]: HREF horizontal endpoint[7:0]
0x3806	TIMING VH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF vertical endpoint[11:8]
0x3807	TIMING VH	0x9B	RW	Bit[7:0]: HREF vertical endpoint[7:0]
0x3808	TIMING ISPHO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP output horizontal width[11:8]
0x3809	TIMING ISPHO	0xC0	RW	Bit[7:0]: ISP output horizontal width[7:0]
0x380A	TIMING ISPVO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP output vertical width[11:8]
0x380B	TIMING ISPVO	0x90	RW	Bit[7:0]: ISP output vertical width[7:0]
0x3810	TIMING HOFFS HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal offset[11:8]
0x3811	TIMING HOFFS LOW	0x10	RW	Bit[7:0]: Horizontal offset[7:0]
0x3812	TIMING VOFFS HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Vertical offset[11:8]
0x3813	TIMING VOFFS LOW	0x10	RW	Bit[7:0]: Vertical offset[7:0]

3.3 test pattern

For testing purposes, the OV3660 offers one type of test pattern, color bar.

figure 3-5 test pattern



color bar

table 3-4 test pattern selection control

address	register name	default value	R/W	description
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: Color bar enable 0: Color bar disable 1: Color bar enable Bit[3:2]: Color bar style 00: Standard eight color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2

3.4 exposure / gain control

3.4.1 overview

The exposure/gain control mode allows for a companion backend processor to control the exposure and gain of the OV3660 externally. The pixel array is reset and sampled in series on a row-by-row basis (also known as "rolling shutter"). The time between reset and sampling is called exposure time. As each pixel is exposed, the charge in the pixel decreases proportionally with the time exposed to incident light and the light intensity.

In the OV3660, the exposure time is set by registers {0x3500[3:0], 0x3501[7:0], ox3502[7:0]} in units of 1/16 row period.

$$exposure = \{0x3500[3:0], 0x3501[7:0], 0x3502[7:0]\} / 16 \times t_{ROW}$$

The pixel output can be further amplified by the analog amplifier and/or digital multiplier. The OV3660 supports up to 16x analog gain and 4x digital gain. The gain can be calculated from the register value using the following formula:

$$gain = \{0x350A[1:0], 0x350B[7:0]\} / 16$$

The first 15.9375x gain ({0x350A[1:0] = 2b'00, 0x350B[7:0] = 0x00~0xFF}) is analog gain and the remaining 4x gain is digital gain. Please note that analog gain is always preferred to reduce image noise; thus, for gain adjustments, it is always advisable to maximize analog gain before moving on to use digital gain.

Under AC lighting conditions (e.g., 50Hz or 60Hz fluorescent light), the light intensity is not constant. Though the exposure time of each row is equal to each other, the amount of photons each row receives may vary with the start point of the exposure. In order for each row to receive the same amount of photons, the exposure time must be a multiple of the flicker period of the light intensity.

$$exposure = \begin{cases} n/100\ second, & for\ 50Hz \\ n/120\ second, & for\ 60Hz \end{cases}$$

If the exposure time does not fall in these steps, the pixel array will not be evenly illuminated and horizontal bands will show up in the image.

3.4.2 automatic exposure/gain control

The Automatic Exposure Control (AEC) function allows the OV3660 image sensor to adjust the exposure and gain values without any external command or control to the sensor. The OV3660 has a built-in AEC/AGC (auto exposure control / auto gain control) algorithm to automatically control the exposure and gain to bring the image level to a pre-defined range, namely stable range. The AEC and AGC can be enabled by setting register 0x3503[0] and 0x3503[1] to 1'b0, respectively. Although the AEC and AGC can be enabled/disabled independently, it is highly recommended that both

AEC and AGC are enabled/disabled together; otherwise, the auto control may induce flicker artifacts in the image due to the precision limitation of the exposure time.

The image level is a weighted average over a user-defined area as shown in **figure 3-6**. The area is specified by the top-left point ({0x5680[3:0], 0x5681[7:0]}, {0x5682[2:0], 0x5683[7:0]}) and the bottom-right point ({0x5684[3:0], 0x5685[7:0]}, {0x5686[2:0], 0x5687[7:0]}). The area is equally divided into 4x4 zones and the weight of each zone can be programmed by registers 0x5688~0x568F as shown in **table 3-5**. The average value is calculated in the linear domain when register 0x5025[1:0] is 2'b00 or after gamma correction when register 0x5025[1:0] is set to 2b'10.

figure 3-6 average-based window definition

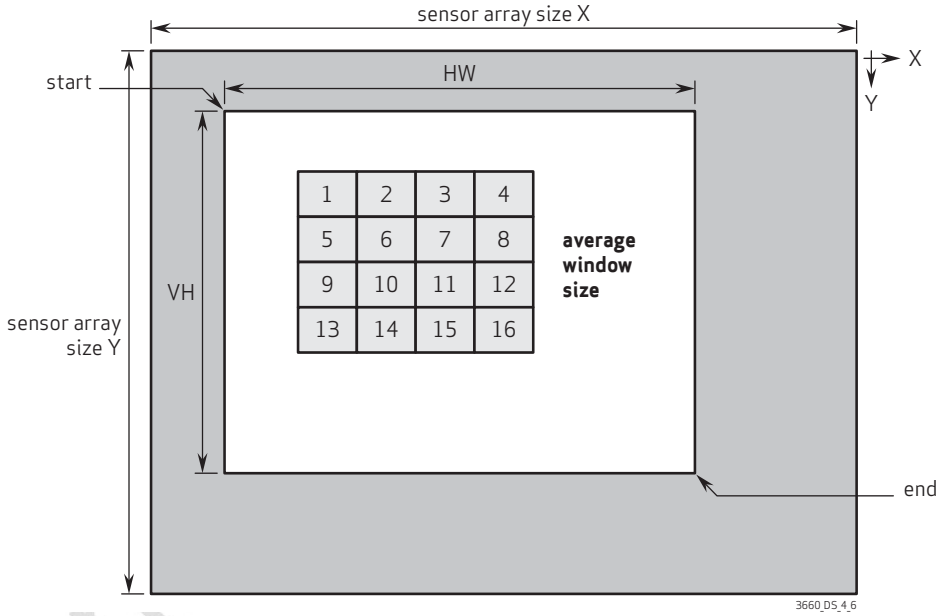


table 3-5 timing control functions (sheet 1 of 3)

address	register name	default value	R/W	description
0x3810	TIMING HOFFSET	0x00	RW	Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING HOFFSET	0x10	RW	Bit[7:0]: ISP Horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[3:0]: ISP vertical offset[11:8]
0x3813	TIMING VOFFSET	0x06	RW	Bit[7:0]: ISP vertical offset[7:0]
0x3808	TIMING DVPHO	0x08	RW	Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x00	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x06	RW	Bit[3:0]: DVP output vertical height[11:8]

table 3-5 timing control functions (sheet 2 of 3)

address	register name	default value	R/W	description
0x380B	TIMING DVPVO	0x00	RW	Bit[7:0]: DVP output vertical height[7:0]
0x501D	ISP MISC	0x00	RW	Bit[4]: Average size manual enable
0x5680	X START	0x00	RW	Bit[3:0]: X start[11:8] Horizontal start position for average window high byte, valid when 0x501D[4]=1
0x5681	X START	0x00	RW	Bit[7:0]: X start[7:0] Horizontal start position for average window low byte, valid when 0x501D[4]=1
0x5682	Y START	0x00	RW	Bit[2:0]: Y start[10:8] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5683	Y START	0x00	RW	Bit[7:0]: Y start[7:0] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5684	X WINDOW	0x10	RW	Bit[3:0]: Window X[11:8] Horizontal end position for average window high byte, valid when 0x501D[4]=1
0x5685	X WINDOW	0xA0	RW	Bit[7:0]: Window X[7:0] Horizontal end position for average window low byte, valid when 0x501D[4]=1.
0x5686	Y WINDOW	0x0C	RW	Bit[2:0]: Window Y[10:8] Vertical end position for average window high byte, valid when 0x501D[4]=1
0x5687	Y WINDOW	0x78	RW	Bit[7:0]: Window Y[7:0] Vertical end position for average window low byte, valid when 0x501D[4]=1
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: Window 01 weight Bit[3:0]: Window 00 weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: Window 03 weight Bit[3:0]: Window 02 weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: Window 11 weight Bit[3:0]: Window 10 weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: Window 13 weight Bit[3:0]: Window 12 weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: Window 21 weight Bit[3:0]: Window 20 weight
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: Window 23 weight Bit[3:0]: Window 22 weight

table 3-5 timing control functions (sheet 3 of 3)

address	register name	default value	R/W	description
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: Window 31 weight Bit[3:0]: Window 30 weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: Window 33 weight Bit[3:0]: Window 32 weight

The upper limit of the stable range is specified by register 0x3A1B and the lower limit is set by register 0x3A1E.

When register 0x3A05[5] is set to 1, the sensor automatically calculates the exposure/gain step according to the distance between the current image level and the center of the stable range. The ratio of the adjustment step to the distance can be set using register 0x3A05[4:0]:

$$step = \frac{0x3A05[4:0]}{32} \times |current\_image\_level - target\_image\_level|$$

where *target_image_level* equals (0x3A1B+0x3A1E/2)

When register 0x3A05[5] is set to 0, the exposure/gain adjustment is manually set by registers 0x3A06 and 0x3A07, depending on where the current image level is. Another wider range, specified by (0x3A10, 0x3A0F), is used to control the step of the exposure/gain adjustment. When the image level is greater than the value of register 0x3A0F, the sensor will decrease the exposure/gain by a big step1:

$$step1 = \frac{0x3A07[3:0]}{16} \times current\_exposure\_gain$$

When the image level is less than the value of register 0x3A10, the sensor will increase the exposure/gain by a big step 2:

$$step2 = \frac{0x3A06[4:0]}{32} \times current\_exposure\_gain$$

When the image level is within the wider range of (0x3A10, 0x3A0F) but outside of the stable range (0x3A1E, 0x3A1B), the sensor will adjust the exposure/gain by a small step 3:

$$step3 = \frac{0x3A07[7:4]}{16} \times current\_exposure\_gain$$

3.4.3 50Hz/60Hz detection

The OV3660 has a built-in capability to identify 50Hz and 60Hz flickering frequency. When this function is enabled by setting register 0x3004[2] to 1, the sensor will continuously detect the light frequency. The sensor will keep the previous result whenever it is not able to determine the current AC flickering frequency.

The 50Hz/60Hz detection block needs an input clock at a frequency of approximately 3 MHz. Register 0x300C[3:0] is the divider that generates this input clock frequency from the input clock pin (XVCLK).

Register 0x3C01[7] must be set to 0 for the AEC/AGC algorithm to apply the exposure constraint based on the result of the 50Hz/60Hz detection.

Register 0x3C0C[0] shows the result of the 50Hz/60Hz detection. When the detection result is 60Hz, register 0x3C0C[0] = 0, the AEC/AGC algorithm will set the exposure time to an integer multiple of {0x3A0A[1:0], 0x3A0B[7:0]}. Conversely, when the detection is 50Hz, register 0x3C0C[0] = 1, the AEC/AGC algorithm will set the exposure time to an integer multiple of {0x3A08[1:0], 0x3A09[7:0]}.

3.4.4 anti-flicker

Under AC lighting conditions, the user can specify whether to restrict the exposure time to n/100 or n/120 second using register 0x3A00[5]. When the exposure time is restricted to n/100 in 50Hz light or n/120 in 60Hz light, the pixel array will be evenly exposed despite the flickering nature of the AC light source.

In order for the sensor to restrict the exposure time to n/100 or n/120 second, registers {0x3A08, 0x3A09} should be set to 1/100 second in units of row period and registers {0x3A0A, 0x3A0B} should be set to 1/120 second in units of row period. Furthermore, registers 0x3A0E and 0x3A0D should be set to the maximum number of flickering periods in one frame period for 50Hz and 60Hz, respectively.

Given the frame rate (frame period) and the number of row period per frame period, registers {0x3A08, 0x3A09}, {0x3A0A, 0x3A0B}, 0x3A0E, and 0x3A0D can be calculated by the following formula with the result rounded to the closest integer:

$$\{0x3A08, 0x3A09\} = \frac{frame\_per\_second \times row\_per\_frame}{100}$$

$$\{0x3A0A, 0x3A0B\} = \frac{frame\_per\_second \times row\_per\_frame}{100}$$

$$0x3A0E = \frac{100}{frame\_per\_second}$$

$$0x3A0D = \frac{120}{frame\_per\_second}$$

For example, for a YUV output at 15 fps and full resolution of 2048x1536:

$$row\_per\_frame = register\ \{0x380E, 0x380F\} = 0x61C = 1564\ (decimal)$$

$$\{0x3A08, 0x3A09\} = (1564 \times 15)/100 = 234.6\ (decimal) = 0xEA$$

$$\{0x3A08, 0x3A09\} = (1564 \times 15)/120 = 195.5\ (decimal) = 0xC3$$

$$0x3A0E = 100/15 = 6.67\ (decimal) = 0x06$$

$$0x3A0D = 120/15 = 8\ (decimal) = 0x08$$

The light flickering frequency is either automatically set by the 50Hz/60Hz detection circuit (explained in detail in **section 3.4.3**) or manually selected through register 0x3C00[2].

Under very bright AC light conditions, the desired exposure time may be less than 1/100 or 1/120 second. In this case, the sensor can either adjust the exposure time to the desired value or limit the minimum exposure time to 1/100 or 1/120 second. By adjusting the exposure time under such bright AC lighting conditions, the user should expect that there will be horizontal flickering artifacts in the image as the pixels are no longer integrating in a multiple of the flicker periods. Conversely, by limiting the minimum exposure time to 1/100 or 1/120 second, the user can expect an over exposed image.

The trade-off described above can be controlled through register 0x3A00[4]. When this register is set to 1, the exposure time is allowed to go below 1/100 or 1/120 second to avoid over exposure. When this register is set to 0, the minimum exposure is limited to 1/100 or 1/120 second to avoid the flicker.

3.4.5 extending the exposure time under dark conditions

From a noise point of view, it is always preferable to extend the exposure time rather than increasing gain. However, the exposure time is limited to the frame period at a given frame rate. Under extremely dark conditions, the image may still be too dark when the exposure reaches its maximum and the gain then increases to a certain level. One common way to achieve a better image is to slow down the frame rate which, in turn, extends the exposure time. The AEC/AGC algorithm of the OV3660 supports this feature and terms this as night mode. Night mode can be enabled by setting register 0x3A00[2] to 1.

The sensor enters night mode when the exposure time reaches the maximum and the gain reaches the threshold defined by register 0x3A17[1:0] (see **table 3-6**). The sensor starts to extend the frame period by the original frame period, or the flickering period, depending on the value set in register 0x3A05[6]. When this register is set to 1, the sensor will extend the exposure time up to the value set in register 0x3A21[6:4] until the image level falls into the stable range. If the image is still too dark after the exposure has been extended to its maximum exposure time, the sensor will further increase the gain. When register 0x3A05[6] is set to 0, the sensor will extend the exposure time by flickering period {0x3A0A[1:0], 0x3A0B[7:0]} or {0x3A08[1:0], 0x3A09[7:0]}, depending on the light frequency. Note that even when the anti-flickering function is disabled, the sensor will extend the exposure time by the flickering period when register 0x3A05[6] is set to 0.

table 3-6 night mode control registers

function	registers
night mode ceiling setting	{0x3A02[7:0], 0x3A03[7:0], 0x3A14[7:0], 0x3A15[7:0]}
night mode disable	0x3A00[2] 0: disable night mode
increase/decrease step in night mode based on band or frames	0x3A05[6] 0: in night mode, insert frame disable 1: in night mode, insert frame enable

3.4.6 sub-row exposure time under extremely bright conditions

Under extremely bright conditions, even the exposure time of one row period will result in an over exposed image. In this case, the AEC/AGC algorithm can set the exposure time to sub-row period. This function can be enabled by setting register 0x3A00[6].

Due to the readout timing limitation, the minimum and maximum sub-row exposure times have certain constraints. The maximum and minimum sub-row exposure times are:

$$max\_sub\_row\_exposure = \frac{0x3A0C[7:4]}{16} \times row\_period$$

$$min\_sub\_row\_exposure = \frac{0x3A0C[3:0]}{16} \times row\_period$$

OmniVision recommends setting registers 0x3A0C to 0xC4.

3.5 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. Black level adjustments can be made with registers 0x4000 through 0x4013.

table 3-7 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x0D	RW	BLC Control 00 Bit[0]: BLC enable
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable BLC update when format changes
0x4003	BLC CTRL03	0x01	RW	Bit[7]: BLC redo enable Write 1 into it will trigger a BLC redo N frames begin, N is 0x4003[5:0] Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4005	BLC CTRL05	0x10	RW	Bit[1]: BLC always update 0: Normal freeze 1: BLC always updated
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: BLC black level target at 10-bit range

3.6 strobe flash

3.6.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. It supports the following flashlight modes (see **table 3-8**).

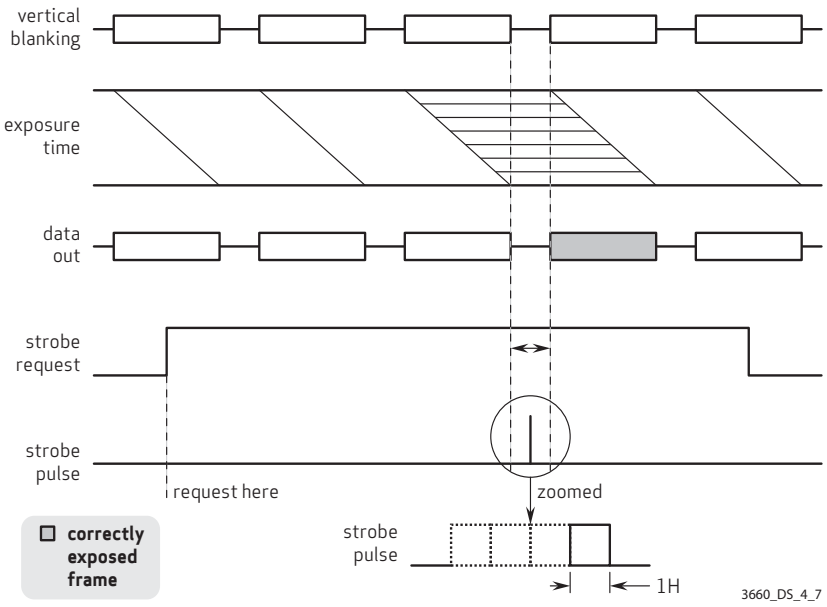
table 3-8 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	pulse	no	no
LED 2	pulse	no	yes
LED 3	continuous	yes	yes

3.6.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 3-7**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[3:2], where H is one row period.

figure 3-7 xenon flash mode



3.6.1.2 LED 1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see **figure 3-8**). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 3-9**). The number of skipped frames is programmable using registers {0x3A1C, 0x3A1D}.

figure 3-8 LED 1 & 2 mode - one pulse output

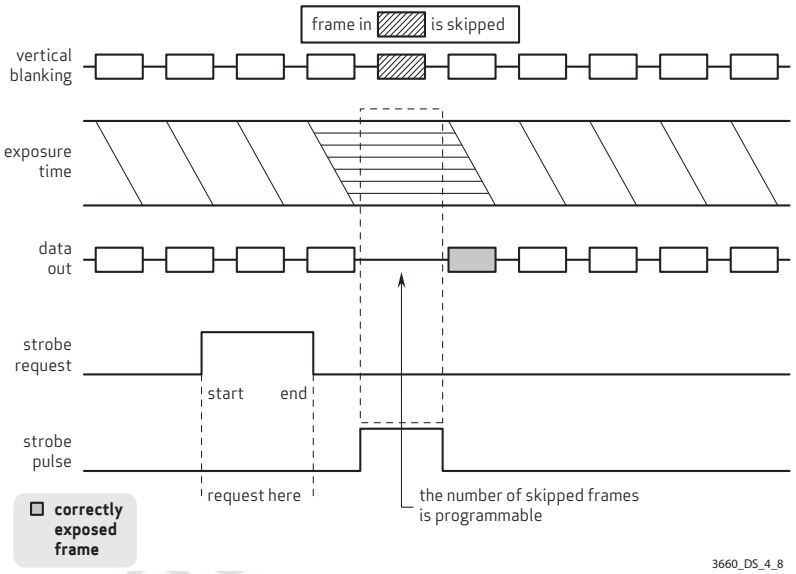
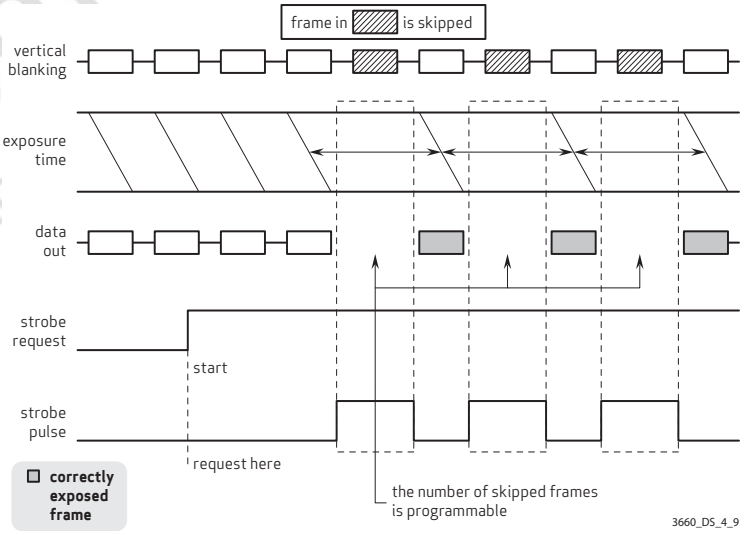


figure 3-9 LED 1 & 2 mode - multiple pulse output



3.6.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 3-10**).

figure 3-10 LED 3 mode

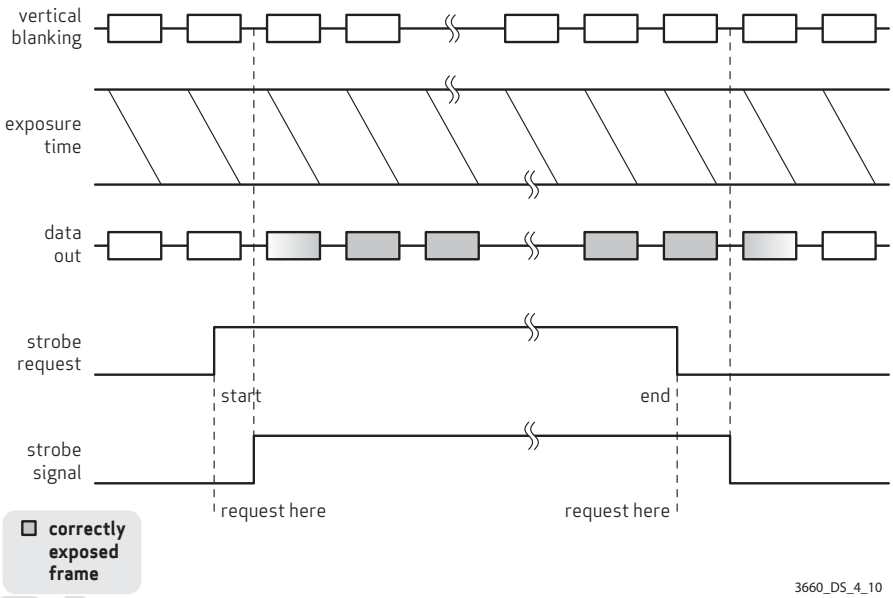


table 3-9 strobe control functions

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon Bit[1:0]: Strobe mode 00: Xenon 01: LED 1 10: LED 2 11: LED 3

3.7 one time programmable (OTP) memory

The OV3660 supports a maximum of 256 bits of one-time programmable (OTP) memory to store chip identification and manufacturing information. OTP memory occupies registers 0x3D00 to 0x3D1F. Typically, registers 0x3D00 to 0x3D04 is reserved for OmniVision and registers 0x3D05 to 0x3D1F is for customer use. Detailed read/write sequences are shown below:

3.7.1 OTP write sequence

```
Write OTP Reg0x3d05-0x3d1f ¡§xx¡¨  //"xx" means the value that customer intends to program
Write Enable:
                78 3000 20  ;Set Bit[4], Reset OTP=0
                78 3004 df  ;Set Bit[4], Enable OTP clk=1
                78 3d20 01  ;OTP Program Enable
Wait time 50mS
End Write Sequence:
                78 3d20 00
                78 3004 cf
                78 3000 30
```

3.7.2 OTP read sequence

```
First, write OTP Reg0x3d05-0x3d1f to be "00"
Read Enable:
                78 3000 20  ;Set Bit[4], Reset OTP=0
                78 3004 df  ;Set Bit[4], Enable OTP clk=1
                78 3d21 01  ;OTP Read Enable
Wait time 50mS
End Read Sequence:
                78 3d21 00
                78 3004 cf
                78 3000 30
Read Reg0x3d00-0x3d1f back. Now, the values are what the customer programmed.
```

table 3-10 OTP control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D20	OTP PROGRAM CTRL	0x00	RW	Bit[7]: OTP program busy Bit[1]: OTP program speed 0: Fast 1: Slow Bit[0]: OTP program enable
0x3D21	OTP READ CTRL	0x00	RW	Bit[7]: OTP read busy Bit[1]: OTP read speed 0: Fast 1: Slow Bit[0]: OTP read enable
0x3D00	OTP DATA00	0x00	RW	OTP Dump/Load Data00
0x3D01	OTP DATA01	0x00	RW	OTP Dump/Load Data01
0x3D02	OTP DATA02	0x00	RW	OTP Dump/Load Data02
0x3D03	OTP DATA03	0x00	RW	OTP Dump/Load Data03
0x3D04	OTP DATA04	0x00	RW	OTP Dump/Load Data04
0x3D05	OTP DATA05	0x00	RW	OTP Dump/Load Data05
0x3D06	OTP DATA06	0x00	RW	OTP Dump/Load Data06
0x3D07	OTP DATA07	0x00	RW	OTP Dump/Load Data07
0x3D08	OTP DATA08	0x00	RW	OTP Dump/Load Data08
0x3D09	OTP DATA09	0x00	RW	OTP Dump/Load Data09
0x3D0A	OTP DATA0A	0x00	RW	OTP Dump/Load Data0a
0x3D0B	OTP DATA0B	0x00	RW	OTP Dump/Load Data0b
0x3D0C	OTP DATA0C	0x00	RW	OTP Dump/Load Data0c
0x3D0D	OTP DATA0D	0x00	RW	OTP Dump/Load Data0d
0x3D0E	OTP DATA0E	0x00	RW	OTP Dump/Load Data0e
0x3D0F	OTP DATA0F	0x00	RW	OTP Dump/Load Data0f
0x3D10	OTP DATA10	0x00	RW	OTP Dump/Load Data10
0x3D11	OTP DATA11	0x00	RW	OTP Dump/Load Data11
0x3D12	OTP DATA12	0x00	RW	OTP Dump/Load Data12
0x3D13	OTP DATA13	0x00	RW	OTP Dump/Load Data13
0x3D14	OTP DATA14	0x00	RW	OTP Dump/Load Data14
0x3D15	OTP DATA15	0x00	RW	OTP Dump/Load Data15
0x3D16	OTP DATA16	0x00	RW	OTP Dump/Load Data16

table 3-10 OTP control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D17	OTP DATA17	0x00	RW	OTP Dump/Load Data17
0x3D18	OTP DATA18	0x00	RW	OTP Dump/Load Data18
0x3D19	OTP DATA19	0x00	RW	OTP Dump/Load Data19
0x3D1A	OTP DATA1A	0x00	RW	OTP Dump/Load Data1a
0x3D1B	OTP DATA1B	0x00	RW	OTP Dump/Load Data1b
0x3D1C	OTP DATA1C	0x00	RW	OTP Dump/Load Data1c
0x3D1F	OTP DATA1D	0x00	RW	OTP Dump/Load Data1d
0x3D1E	OTP DATA1E	0x00	RW	OTP Dump/Load Data1e
0x3D1F	OTP DATA1F	0x00	RW	OTP Dump/Load Data1f

3.8 temperature sensor

The OV3660 supports an on-chip temperature sensor that covers 0~80°C with an error range of 5°C. It can be controlled through the SCCB interface (see **table 3-11**). When the temperature is lower than 0°C, the reading will stop at 0°C.

table 3-11 temperature sensor function

address	register name	default value	R/W	description
0x6719	TPM CTRL19	–	R	Bit[7:0]: Measured temperature

4 image sensor processor digital functions

4.1 ISP general controls

The ISP module provides the following functions:

- lens correction
- gamma control
- de-noise
- AWB
- color matrix
- scaling
- CIP and sharpening

These functions are enabled by registers 0x501D, 0x501F~0x5020, 0x503D, 0x5061~0x5063.

table 4-1 ISP general control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[5]: Gamma enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 4-1 ISP general control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	ISP Control 01 Bit[7]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[5]: Scale enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5003	ISP CONTROL 03	0x08	RW	ISP Control 03 Bit[2]: Bin enable 0: Disable 1: Enable Bit[0]: Solarize enable 0: Disable 1: Enable
0x5004	ISP CONTROL 04	0x08	RW	Bit[3]: Auto size control enable 0: Manual 1: Auto
0x5005	ISP CONTROL 05	0x36	RW	ISP Control 05 Bit[6]: AWB bias manual enable 0: Disable 1: Enable Bit[5]: AWB bias on enable 0: Disable 1: Enable Bit[4]: AWB bias plus enable 0: Disable 1: Enable Bit[3]: Reserved Bit[2]: LENC bias on enable 0: Disable 1: Enable Bit[1]: GMA bias on enable 0: Disable 1: Enable Bit[0]: LENC bias manual enable 0: Disable 1: Enable

table 4-1 ISP general control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x501D	ISP MISC	0x00	RW	Bit[6]: SDE AVG manual enable Bit[5]: AWB YUV2CBCR enable Bit[4]: AVG size manual enable Bit[3:0]: Reserved
0x501F	FORMAT MUX CONTROL	0x03	RW	Format Mux control Bit[5]: Enable option Bit[4]: Reserved Bit[3]: Format v first Bit[2:0]: Format select 000: ISP YUV422 001: ISP RGB 010: ISP dither 011: ISP RAW(DPC) 100: SNR RAW 101: ISP RAW(CIP)
0x5020	DITHER CTRL 0	0x00	RW	Bit[6]: Dither mux Bit[5:4]: R dithering register Bit[3:2]: G dithering register Bit[1:0]: B dithering register
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: Test enable 0: Test disable 1: Color bar enable Bit[6]: Rolling Bit[5]: Transparent Bit[4]: Square black and white Bit[3:2]: Color bar style 00: Standard 8 color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2 Bit[1:0]: Test select 00: Color bar 01: Random data 10: Square data 11: Black image
0x5061	ISP SENSOR BIAS I	–	R	ISP Sensor Bias Input
0x5062	ISP SENSOR GAIN I	–	R	ISP Real Gain Input High Byte
0x5063	ISP SENSOR GAIN I	–	R	ISP Real Gain Input Low Byte

4.2 lens correction (LENC)

The main purpose of the LENC is to compensate for lens imperfection. According to the area where each pixel is located, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the luminance and color distribution due to lens curvature. Also, the LENC supports the subsample function in both horizontal and vertical directions. LENC is performed in the RGB domain. Luminance channel consists of 36 control points while each color channel consists of 25 control points.

figure 4-1 control points of luminance and color channels

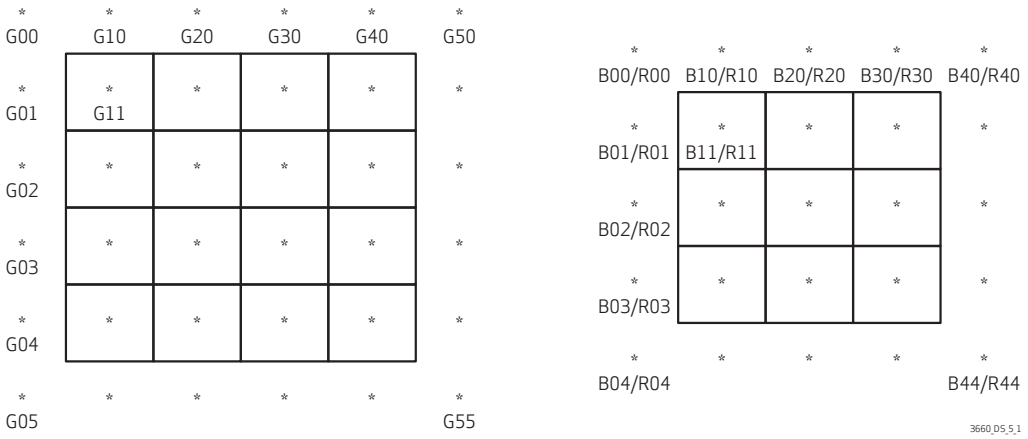


figure 4-2 luminance compensation level calculation

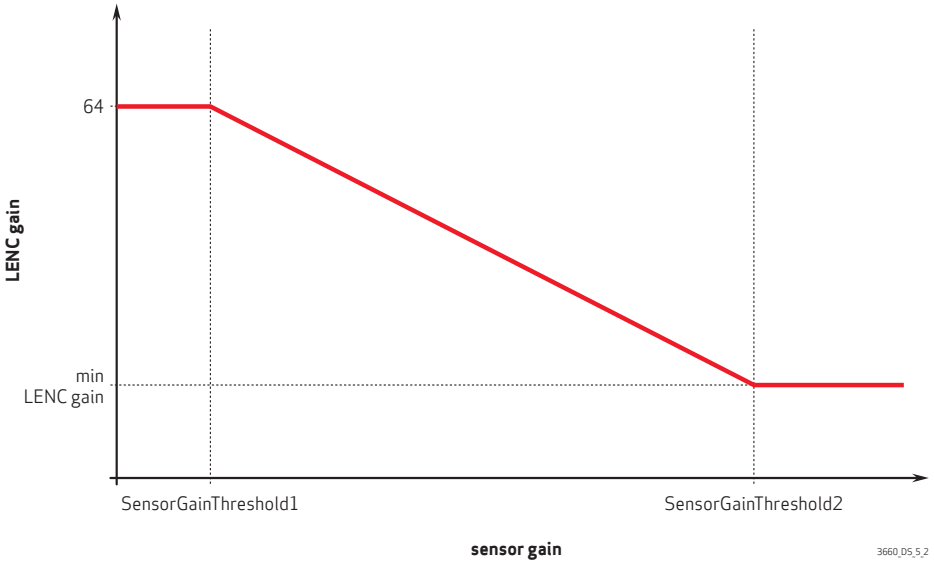


table 4-2 LENC control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable
0x5842	BR HSCALE	0x00	RW	Bit[2:0]: br h scale[10:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5843	BR HSCAL	0xBD	RW	Bit[7:0]: br h scale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5844	BR VSCALE	0x00	RW	Bit[2:0]: br v scale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5845	BR VSCALE	0xFE	RW	Bit[7:0]: br v scale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x00	RW	Bit[2:0]: g h scale[10:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCAL	0xFC	RW	Bit[7:0]: g h scale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x00	RW	Bit[2:0]: g v scale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5849	G VSCALE	0xA9	RW	Bit[7:0]: g v scale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

4.3 auto white balance (AWB)

The main function of Auto White Balance (AWB) is the process of removing unrealistic color casts so that objects which appear white in person are rendered white in the image or video. Thus, the AWB makes sure that the white color is always a white color in different color temperatures. It supports manual white balance and auto white balance. For auto white balance, simple AWB and advanced AWB methods are supplied. Advance AWB takes into account the *color temperature* of a light source. For advanced AWB settings, contact your local OmniVision FAE.

table 4-3 AWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[0]: Auto white balance enable 0: Disable 1: Enable
0x5181	AWB CONTROL 01	0x58	RW	Bit[7:6]: Step local Bit[5:4]: Step fast Bit[3]: Slop 8x Bit[2]: Slop 4x Bit[1]: One zone Bit[0]: AVG all
0x5182	AWB CONTROL 02	0x11	RW	Bit[7:4]: Maximum local counter Bit[3:0]: Maximum fast counter
0x5183	AWB CONTROL 03	0x90	RW	Bit[7]: AWB simple enable 0: AWB advance 1: AWB simple Bit[6]: YUV enable 1: Simple YUV enable Bit[5]: AWB preset Bit[4]: AWB simf Bit[3:2]: AWB win
0x5184	AWB CONTROL 04	0x25	RW	Bit[7:6]: Counter area selection Bit[5]: G enable Bit[4:2]: Counter limit control Bit[1:0]: Counter threshold
0x5185	AWB CONTROL 05	0x24	RW	Bit[7:4]: Stable range unstable Threshold for unstable to stable change Bit[3:0]: Stable range stable Threshold for stable to un-stable change
0x5186~ 0x5190	AWB CONTROL	–	–	Advanced AWB Control Registers
0x5191	AWB CONTROL 17	0xFF	RW	Bit[7:0]: AWB top limit
0x5192	AWB CONTROL 18	0x00	RW	Bit[7:0]: AWB bottom limit
0x5193	AWB CONTROL 19	0xF0	RW	Bit[7:0]: Red limit

table 4-3 AWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5194	AWB CONTROL 20	0xF0	RW	Bit[7:0]: Green limit
0x5195	AWB CONTROL 21	0xF0	RW	Bit[7:0]: Blue limit
0x5196	AWB CONTROL 22	0x03	RW	Bit[5]: AWB freeze Bit[3:2]: AWB simple selection 00: AWB simple from after AWB gain 01: AWB simple from after GMA 10: AWB simple from after GMA 11: AWB simple from after AWB gain Bit[1]: Fast enable Bit[0]: AWB bias stat
0x5197	AWB CONTROL 23	0x02	RW	Bit[7:0]: Local limit
0x519E	AWB CONTROL 30	0x30	RW	Bit[3]: Local limit select Bit[2]: Simple stable select
0x519F~ 0x51D0	AWB G SUM	–	R	AWB Debug Information

4.4 gamma

The main purpose of the Gamma (GMA) function is to accomodate for the non-linear characteristics of the display device. The gamma curve is constructed by 16 linear segments.

table 4-4 gamma control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[5]: Gamma enable 0: Disable GMA 1: Enable GMA
0x5481	GAMMA YST00	0x26	RW	Bit[7:0]: Y yst 00
0x5482	GAMMA YST01	0x35	RW	Bit[7:0]: Y yst 01
0x5483	GAMMA YST02	0x48	RW	Bit[7:0]: Y yst 02
0x5484	GAMMA YST03	0x63	RW	Bit[7:0]: Y yst 03
0x5485	GAMMA YST04	0x6E	RW	Bit[7:0]: Y yst 04
0x5486	GAMMA YST05	0x77	RW	Bit[7:0]: Y yst 05
0x5487	GAMMA YST06	0x80	RW	Bit[7:0]: Y yst 06
0x5488	GAMMA YST07	0x88	RW	Bit[7:0]: Y yst 07

table 4-4 gamma control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5489	GAMMA YST08	0x8F	RW	Bit[7:0]: Y yst 08
0x548A	GAMMA YST09	0x96	RW	Bit[7:0]: Y yst 09
0x548B	GAMMA YST0A	0xA3	RW	Bit[7:0]: Y yst 0A
0x548C	GAMMA YST0B	0xAF	RW	Bit[7:0]: Y yst 0B
0x548D	GAMMA YST0C	0xC5	RW	Bit[7:0]: Y yst 0C
0x548E	GAMMA YST0D	0xD7	RW	Bit[7:0]: Y yst 0D
0x548F	GAMMA YST0E	0xE8	RW	Bit[7:0]: Y yst 0E
0x5490	GAMMA YST0F	0x0F	RW	Bit[7:0]: Y yst 0F

4.5 defect pixel cancellation (DPC)

Due to processes and other reasons, pixel defects in the sensor array will occur.

The value of the defect pixel usually has an abrupt change compared to normal pixels. The DPC function is designed to recover these white or black pixels while maintaining image quality.

table 4-5 DPC control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable

4.6 color interpolation (CIP) and sharpening

The CIP functions include:

- de-noising of raw images
- RAW to RGB interpolation
- edge enhancement

In sensor RAW format, each pixel will be either R, G or B. CIP will calculate the other two color values using the neighboring pixel of the same color. Thus, we can get the full RGB information for each pixel. For edge enhancement, the OV3660 provides both manual and auto modes.

table 4-6 CIP control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[0]: Color interpolation enable 0: Disable 1: Enable
0x5300	CIP SHARPENMT THRESHOLD 1	0x08	RW	Color Interpolation Sharpen MT Threshold 1
0x5301	CIP SHARPENMT THRESHOLD 2	0x48	RW	Color Interpolation Sharpen MT Threshold 2
0x5302	CIP SHARPENMT OFFSET1	0x18	RW	CIP Sharpen MT Offset1 (Y edge mt manual setting when 0x5308[6]=1)
0x5303	CIP SHARPENMT OFFSET2	0x0E	RW	CIP Sharpen MT Offset2
0x5304	CIP DNS THRESHOLD 1	0x08	RW	CIP DNS Threshold 1
0x5305	CIP DNS THRESHOLD 2	0x48	RW	CIP DNS Threshold 2
0x5306	CIP DNS OFFSET1	0x09	RW	CIP DNS Offset1 (DNS threshold manual setting when 0x5308[4]=1)
0x5307	CIP DNS OFFSET2	0x16	RW	CIP DNS Offset2
0x5308	CIP CTRL	0x25	RW	Bit[6]: CIP edge MT manual enable Bit[4]: CIP DNS manual enable Bit[2:0]: CIP threshold for BR sharpen
0x5309	CIP SHARPENTH THRESHOLD 1	0x08	RW	CIP Sharpen TH Threshold 1
0x530A	CIP SHARPENTH THRESHOLD 2	0x48	RW	CIP Sharpen TH Threshold 2
0x530B	CIP SHARPENTH OFFSET1	0x04	RW	CIP Sharpen TH Offset1 (Sharpen threshold manual setting when 0x5308[6]=1)
0x530C	CIP SHARPENTH OFFSET2	0x06	RW	CIP Sharpen TH Offset2
0x530D	CIP EDGE MT AUTO	–	R	CIP Edge MT Auto Read
0x530E	CIP DNS THRESHOLD AUTO	–	R	CIP DNS Threshold Auto Read
0x530F	CIP SHARPEN THRESHOLD AUTO	–	R	CIP Sharpen Threshold Auto Read

4.7 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to cancel out crosstalk and convert color space. Given the color correction matrix, CCM, and RGB to YUV conversion matrix, the combined matrix is:

$$CMX = \begin{bmatrix} cmx1 & cmx2 & cmx3 \\ cmx4 & cmx5 & cmx6 \\ cmx7 & cmx8 & cmx9 \end{bmatrix} = RGB2YUV \times CCM$$

where CCM is the RGB color correction matrix.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = CCM \begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix}$$

note
Color matrix tuning tool is available as part of the OVTATool. Please contact your local FAE for the latest version of the tool.

table 4-7 CMX control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[1]: Color matrix enable 0: Disable 1: Enable
0x5381	CMX1	0x20	RW	Bit[7:0]: CMX1 for Y
0x5382	CMX2	0x64	RW	Bit[7:0]: CMX2 for Y
0x5383	CMX3	0x08	RW	Bit[7:0]: CMX3 for Y
0x5384	CMX4	0x30	RW	Bit[7:0]: CMX4 for U
0x5385	CMX5	0x90	RW	Bit[7:0]: CMX5 for U
0x5386	CMX6	0xC0	RW	Bit[7:0]: CMX6 for U
0x5387	CMX7	0xA0	RW	Bit[7:0]: CMX7 for V
0x5388	CMX8	0x98	RW	Bit[7:0]: CMX8 for V
0x5389	CMX9	0x08	RW	Bit[7:0]: CMX9 for V
0x538A	CMXSIGN	0x01	RW	Cmxsign Bit[0]: CMX9 sign
0x538B	CMXSIGN	0x98	RW	Cmxsign Bit[7]: CMX8 sign Bit[6]: CMX7 sign Bit[5]: CMX6 sign Bit[4]: CMX5 sign Bit[3]: CMX4 sign Bit[2]: CMX3 sign Bit[1]: CMX2 sign Bit[0]: CMX1 sign

4.8 auto color saturation adjust

The main function of the auto color saturation adjust is to adjust the U/V channel value according to sensor gain. It supports both manual and auto modes.

4.8.1 manual mode

By setting 0x5580[1] to 1 and 0x5588[6] to 1, auto color saturation adjust is controlled only by register 0x5583[7:0] and 0x5584[7:0] for U and V gains.

4.8.2 auto mode

When the auto color saturation adjust is set for auto mode (0x5580[1]=1 and 0x5588[6]=0), the auto color saturation adjust curve parameters (see **figure 4-3**) should be entered into the corresponding registers. The auto color saturation adjust parameters, auto color saturation adjust threshold1, auto color saturation adjust threshold2, and offset low, offset high should be entered into the registers to set the curve. To get these values, first set the values of auto color saturation adjust threshold1, auto color saturation adjust threshold2, offset low and offset high. Then, calculate the values of a and k as follows:

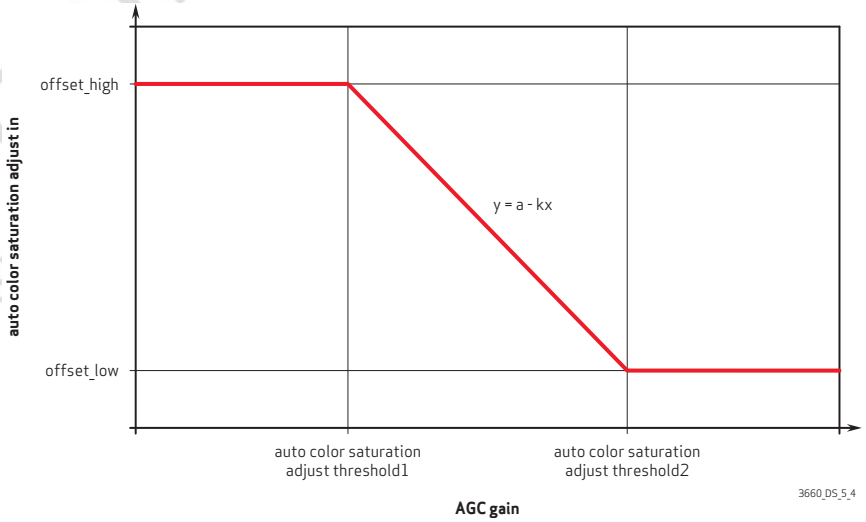
k = (offset high - offset low) / (UV adj th2 - UV adj th1)

a = offset high + (offset high - offset low)/(UV adj th2 - UV adj th1)

Registers to be changed:

- auto color saturation adjust threshold1[8:0] = registers 0x5589[7:0]
- auto color saturation adjust threshold2[8:0] = registers {0x558A[0], 0x558B[7:0]}
- offset high = register 0x5583[7:0] (when 0x5580[1]=1 and 0x5588[6]=0)
- offset low = register 0x5584[7:0] (when 0x5580[1]=1 and 0x5588[6]=0)

figure 4-3 auto color saturation adjust graph



4.9 special digital effects (SDE)

The Special Digital Effects (SDE) functions include:

- hue/saturation control
- brightness control
- contrast control

SDE also supports the following image effects:

- negative
- black/white
- sepia
- greenish
- blueish
- redish
- other image effects

table 4-8 SDE control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Special digital effect enable 0: Disable 1: Enable
0x5581	SDE CTRL1	0x80	RW	Bit[7:0]: Hue cos coefficient
0x5582	SDE CTRL2	0x00	RW	Bit[7:0]: Hue sin coefficient
0x5583	SDE CTRL3	0x40	RW	Bit[7:0]: Saturation U when 0x5580[1]=1 and 0x5588[6]=1, max value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0; or fixed U when 0x5580[3]=1
0x5584	SDE CTRL4	0x40	RW	Bit[7:0]: Saturation V when 0x5580[1]=1 and 0x5588[6]=1, min value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0; or Vreg when 0x5580[4]=1
0x5585	SDE CTRL5	0x00	RW	Bit[7:0]: Yoffset for contrast when 0x5044[3]=1; or fixed Y when 0x5580[7]=1
0x5586	SDE CTRL6	0x20	RW	Bit[7:0]: Y gain for contrast
0x5587	SDE CTRL7	0x00	RW	Bit[7:0]: Y bright for contrast

table 4-8 SDE control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5588	SDE CTRL8	0x01	RW	Bit[6]: Auto color saturation adjust manual enable Bit[5]: Sign5 for hue V, cos Bit[4]: Sign4 for hue U, cos Bit[3]: Sign3 Y bright sign for contrast 0: Keep Y bright sign 1: Negative Y bright sign Bit[2]: Sign2 Y offset sign for contrast when 0x5044[3]=1 0: Keep Y offset sign 1: Negative Y offset sign Bit[1]: Sign1 for hue V, sin Bit[0]: Sign0 for hue U, sin
0x5589	SDE CTRL9	0x01	RW	Bit[7:0]: Auto color saturation adjust threshold 1 Valid when 0x5580[1]=1
0x558A	SDE CTRL10	0x01	RW	Bit[0]: Auto color saturation adjust threshold 2[8] Valid when 0x5580[1]=1
0x558B	SDE CTRL11	0xFF	RW	Bit[7:0]: Auto color saturation adjust threshold 2[7:0] Valid when 0x5580[1]=1
0x558C	SDE CTRL12	–	R	Bit[7:0]: Auto color saturation adjust value read out

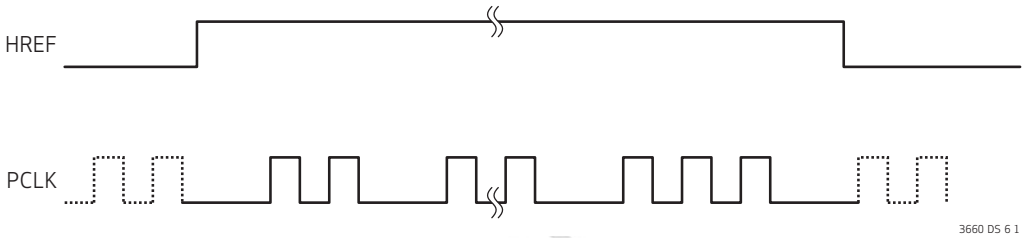
5 image sensor output interface digital functions

5.1 compression engine

5.1.1 compression mode 1 timing

The whole frame has only one line. PCLK will be gated when there is no valid image data transmitted.

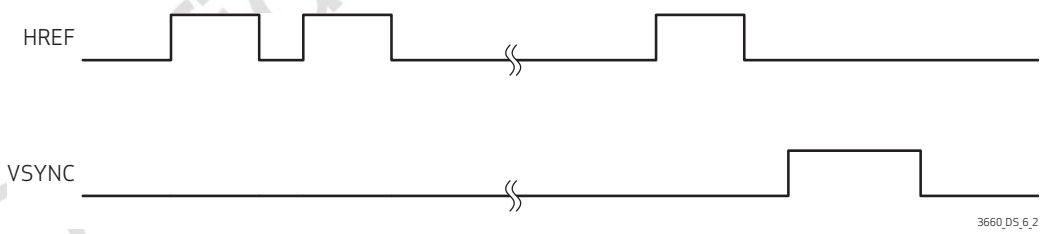
figure 5-1 compression mode 1 timing



5.1.2 compression mode 2 timing

Compression data is transmitted with programmable line width. PCLK is free running. The last line may contain dummy data to match the width. By default, the line number varies from frame to frame. The user can set register 4600[5] (0x4600) to ensure every frame has a fixed line number (programmable).

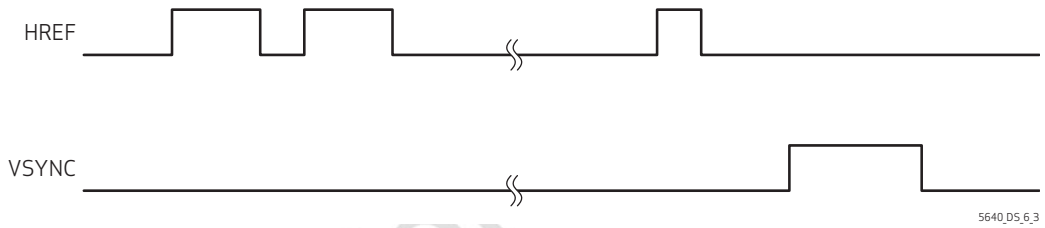
figure 5-2 compression mode 2 timing



5.1.3 compression mode 3 timing

Compression data is transmitted with programmable width. The last line width maybe different from the other line (there is no dummy data). In each frame, the line number may be different.

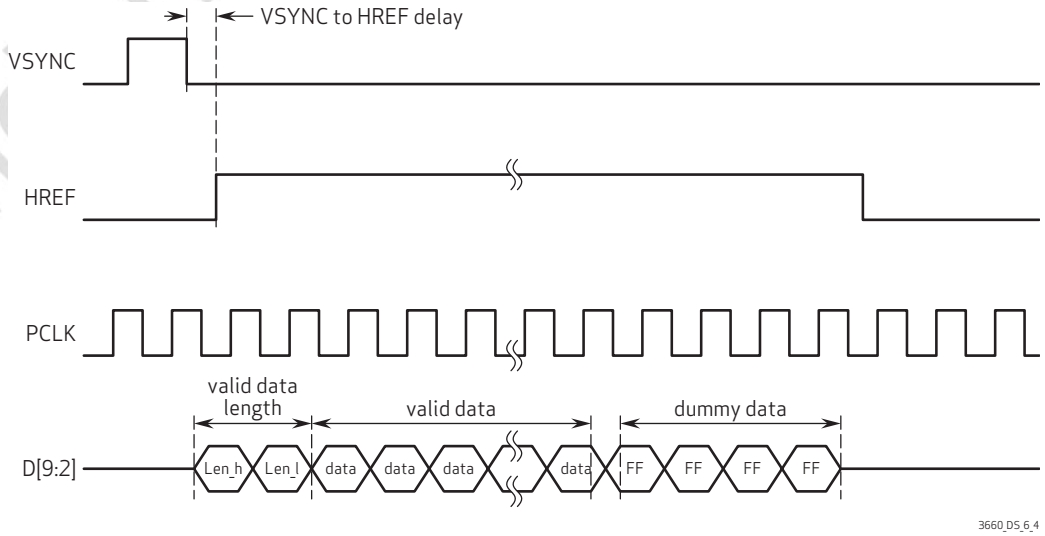
figure 5-3 compression mode 3 timing



5.1.4 compression mode 4 timing

The width and height are fixed in each frame. The first two bytes are valid data length in every line, followed by valid image data. Dummy data (0xFF) may be used as padding at each line end if the current valid image data is less than the line width.

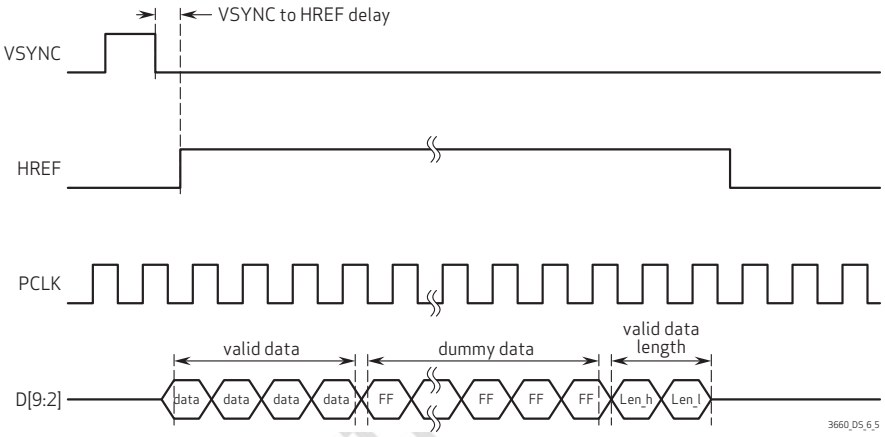
figure 5-4 compression mode 4 timing



5.1.5 compression mode 5 timing

The width and height are fixed in each frame. Every line begins with valid image data. Dummy data may be used as padding at each line end if the current valid image data is less than the line width. The last two bytes of every line is valid data length.

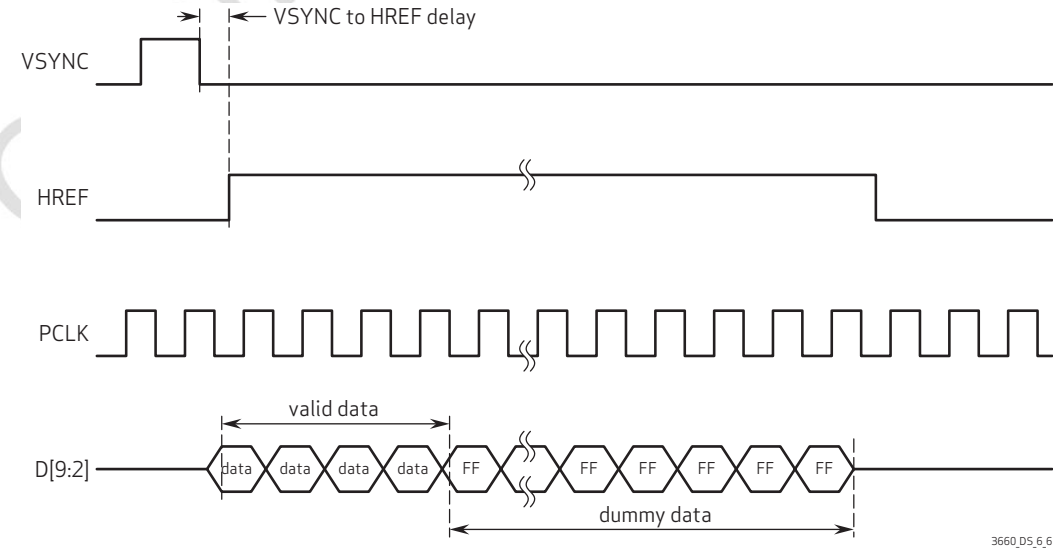
figure 5-5 compression mode 5 timing



5.1.6 compression mode 6 timing

The width and height are fixed in each frame. Every line begins with valid image data. Dummy data may be used as padding at each line end if the current valid image data less than the line width.

figure 5-6 compression mode 6 timing



5.1.7 compression mode control

table 5-1 compression control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3821	COMPRESSION ENABLE	0x00	RW	Bit[5]: Compression enable
0x4600	VFIFO CTRL00	0x80	RW	Bit[5]: Compression output fixed height enable 0: In compression mode2 Compression height is different in each frame 1: In compression mode2 Compression height is fixed in each frame
0x4602	VFIFO HSIZE	0x04	RW	Compression Output Width High Byte
0x4603	VFIFO HSIZE	0x00	RW	Compression Output Width Low Byte
0x4604	VFIFO VSIZE	0x03	RW	Compression Output Height High Byte
0x4605	VFIFO VSIZE	0x00	RW	Compression Output Height Low Byte
0x460C	VFIFO CTRL0C	0x20	RW	Bit[7:4]: Compression dummy data pad speed
0x460D	VFIFO CTRL0D	0x00	RW	Compression Pad Dummy Data
0x4713	COMPRESSION MODE SELECT	0x02	RW	Bit[2:0]: Compression mode select 001: Compression mode 1 010: Compression mode 2 011: Compression mode 3 100: Compression mode 4 101: Compression mode 5 110: Compression mode 6
0x471F	DVP HREF CTRL	0x40	RW	HREF Minimum Blanking in Compression Mode23
0x4723	DVP CTRL23	0x00	RW	DVP Compression Mode456 Skip Line Number
0x4400	COMPRESSION CTRL00	0x81	RW	Bit[7]: input_format 0: YUV420 1: YUV422 Bit[6:0]: JFIFO read speed control

table 5-1 compression control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4401	COMPRESSION CTRL01	0x01	RW	Bit[7:4]: SFIFO output buffer speed control Bit[3]: Read SRAM enable when blanking 0: Disable 1: Enable Bit[2]: Read SRAM at first blanking 0: Disable 1: Enable Bit[1:0]: SFIFO read speed control
0x4404	COMPRESSION CTRL04	0x24	RW	Bit[7]: jfifo_pwrdn Bit[6]: SFIFO pwrdn Bit[5]: Header output enable Bit[4]: Enable gated clock 0: Disable gated clock 1: Enable gated clock Bit[3]: Substitute 0xFF to 0xFE in QT Bit[2:0]: Quantization rounding Bias: set value = Bias/8
0x4417	JFIFO OVERFLOW	–	R	Bit[0]: JFIFO overflow indicator

5.2 parallel digital video port (DVP)

5.2.1 overview

The parallel DVP provides 10-bit parallel data output in all formats supported and extended features including:

- compression mode
- HSYNC mode
- CCIR656 mode
- test pattern output

table 5-2 parallel DVP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4709	DVP VSYNC WIDTH0	0x02	RW	VSYNC WIDTH Line Unit
0x470A	DVP VSYNC WIDTH1	0x00	RW	VSYNC WIDTH PCLK Unit High Byte
0x470B	DVP VSYNC WIDTH2	0x01	RW	VSYNC WIDTH PCLK Unit Low Byte
0x4711	PAD LEFT CTRL	0x00	RW	HSYNC Mode Left Padding Pixel Count Add padding data at start of a line
0x4712	PAD RIGHT CTRL	0x00	RW	HSYNC Mode Right Padding Pixel Count Add padding data at end of a line
0x4713	COMPRESSION MODE SELECT	0x02	RW	Bit[2:0]: Compression mode select 001: Compression mode 1 010: Compression mode 2 011: Compression mode 3 100: Compression mode 4 101: Compression mode 5 110: Compression mode 6
0x4715	656 DUMMY LINE	0x00	RW	Bit[3:0]: CCIR656 dummy line number Control dummy line number at beginning of the frame
0x4719	CCIR656 CTRL	0x01	RW	Bit[1:0]: CCIR656 EAV/SAV option
0x471B	HSYNC CTRL00	0x02	RW	Bit[0]: HSYNC mode enable

table 5-2 parallel DVP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x471D	DVP VSYNC CTRL	0x01	RW	Bit[2]: vsync_sel1_clr Bit[1:0]: vsync_mode 00: VSYNC positive edge trigger by end of field, negative edge trigger by start of frame 01: VSYNC positive edge trigger by end of frame, the width define by register 10: VSYNC positive edge trigger by start of field, the width define by register
0x471F	DVP HREF CTRL	0x40	RW	HREF Minimum Blanking in Compression Mode23
0x4721	VERTICAL START OFFSET	0x01	RW	Bit[3:0]: Vertical start delay between video output and video input
0x4722	VERTICAL END OFFSET	0x00	RW	Bit[3:0]: Vertical end delay between video output and video input
0x4723	DVP CTRL23	0x00	RW	DVP Compression Mode456 Skip Line Number
0x4730	CCIR656 CTRL00	0x00	RW	Bit[7]: SYNC code selection 0: Auto generate sync code 1: Sync code from register setting 0x4732~4735 Bit[6]: F value in CCIR656 SYNC code when fixed f value Bit[5]: Fixed f value Bit[4:3]: Blank toggle data options 00: Toggle data is 1'h040/1'h200 01: Use register setting 0x4736~0x4738 10: Blanking data always keep 0 Bit[2]: Debug mode Bit[1]: Clip data disable Bit[0]: CCIR656 mode enable
0x4731	CCIR656 CTRL01	0x01	RW	Bit[0]: Blanking toggle data order option
0x4732	CCIR656 FS	0x01	RW	CCIR656 SYNC Code Frame Start
0x4733	CCIR656 FE	0x0F	RW	CCIR656 SYNC Code Frame End

table 5-2 parallel DVP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4734	CCIR656 LS	0x00	RW	CCIR6656 SYNC Code Line Start
0x4735	CCIR656 LE	0x00	RW	CCIR656 SYNC Code Line End
0x4736	CCIR656 CTRL6	0x00	RW	Bit[3:2]: Toggle data0[9:8] Bit[1:0]: Toggle data1[9:8]
0x4737	CCIR656 CTRL7	0x00	RW	Bit[7:0]: Toggle data0[7:0]
0x4738	CCIR656 CTRL8	0x00	RW	Bit[7:0]: Toggle data1[7:0]
0x4740	POLARITY CTRL00	0x20	RW	Bit[5]: PCLK polarity 0: Active low 1: Active high Bit[4]: Reserved Bit[3]: Gate PCLK under VSYNC Bit[2]: Gate PCLK under HREF Bit[1]: HREF polarity 0: Active low 1: Active high Bit[0]: VSYNC polarity 0: Active low 1: Active high
0x4741	TEST PATTERN	0x00	RW	Bit[2]: Test pattern enable Bit[1]: Test pattern select 0: Output test pattern 0 1: Output test pattern 1 Bit[0]: Test pattern 8-bit/10-bit 0: 10-bit test pattern 1: 8-bit test pattern
0x4745	DATA ORDER	0x00	RW	Bit[2:1]: DVP order option for debug 00: D[9:0] 10: {D[7:0],D[9:8]} x1: {D[1:0],D[9:2]} Bit[0]: Output data order 0: Normal output 1: Reverse output data bit order

5.2.2 DVP timing

figure 5-7 DVP frame timing diagram

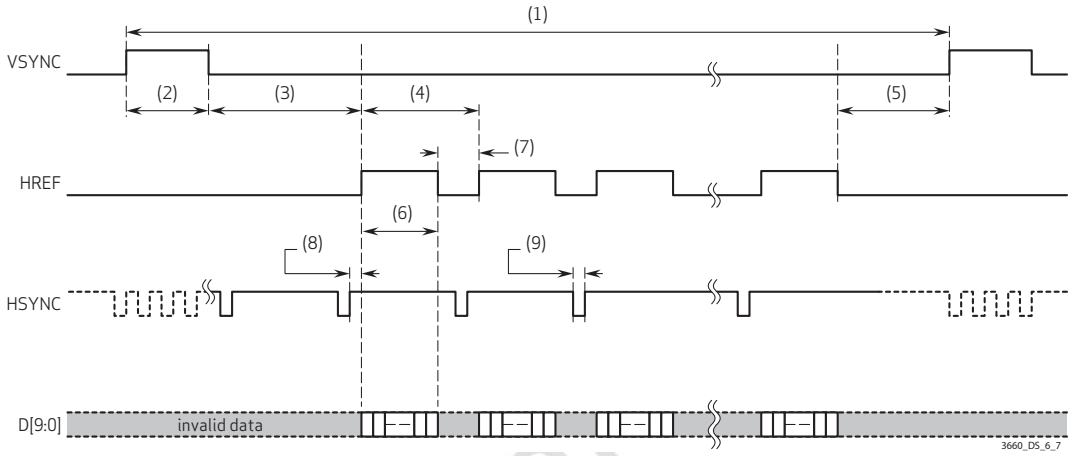


table 5-3 DVP timing specifications (sheet 1 of 2)

mode	timing
3 megapixel 2048x1536	(1) 3,599,434 tp (2) 4,600 tp (3) 32,062 tp (4) 2,300 tp (5) 27,924 tp (6) 2,048 tp (7) 252 tp (8) 0 tp (9) 252 tp where tp = 1 sclk
1080p 1920x1080	(1) 2,702,760 tp (2) 4,788 tp (3) 127,396 tp (4) 2,394 tp (5) 19,476 tp (6) 1,920 tp (7) 474 tp (8) 0 tp (9) 474 tp where tp = 1 sclk

note
The timing values shown in table 5-3 may vary depending upon register settings.

table 5-3 DVP timing specifications (sheet 2 of 2)

mode	timing
720p 1280x720	(1) 1,201,330 tp (2) 3,208 tp (3) 30,410 tp (4) 1,604 tp (5) 13,156 tp (6) 1,280 tp (7) 324 tp (8) 0 tp (9) 324 tp where tp = 1 sclk
XGA 1024x768	(1) 1,210,260 tp (2) 3,068 tp (3) 23,130 tp (4) 1,534 tp (5) 6,460 tp (6) 1,024 tp (7) 510 tp (8) 0 tp (9) 510 tp where tp = 1 sclk
VGA 640x480	(1) 451,010 tp (2) 1,808 tp (3) 9,798 tp (4) 904 tp (5) 5,748 tp (6) 640 tp (7) 264 tp (8) 0 tp (9) 264 tp where tp = 1 sclk
QVGA 320x240	(1) 225,844 tp (2) 1,772 tp (3) 8,130 tp (4) 886 tp (5) 7,412 tp (6) 320 tp (7) 566 tp (8) 0 tp (9) 566 tp where tp = 1 sclk

6 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

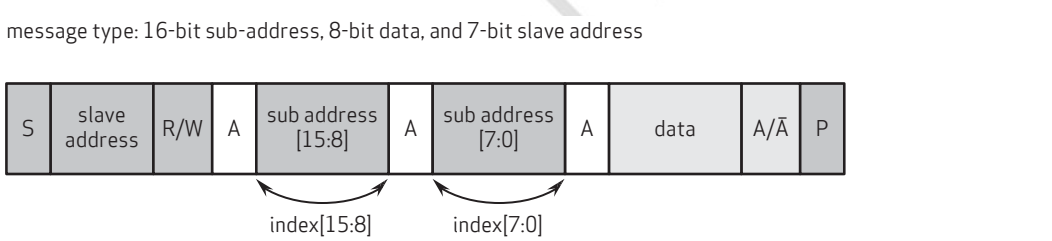
6.1 data transfer protocol

The data transfer of the OV3660 follows the SCCB protocol.

6.2 message format

The OV3660 supports the message format shown in **figure 6-1**. The 7-bit address of the OV3660 is 0x3C by default but can be programmed using register 0x3100[7:1] which has a default of 0x78. The repeated START (Sr) condition is not shown in **figure 6-2**, but is shown in **figure 6-3** and **figure 6-4**.

figure 6-1 message type



6.3 read / write operation

The OV3660 supports four different read operations and two different write operations:

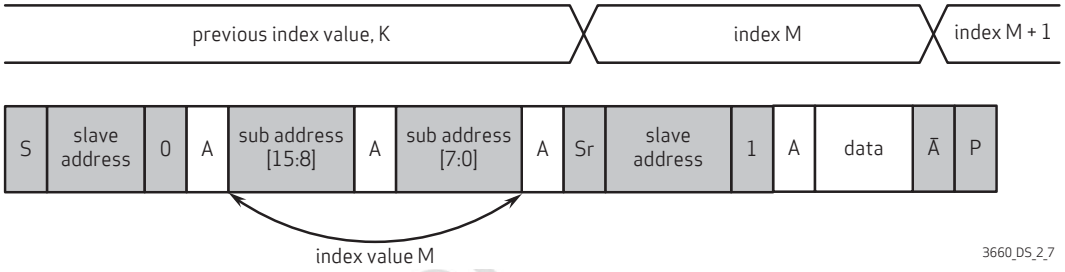
- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave

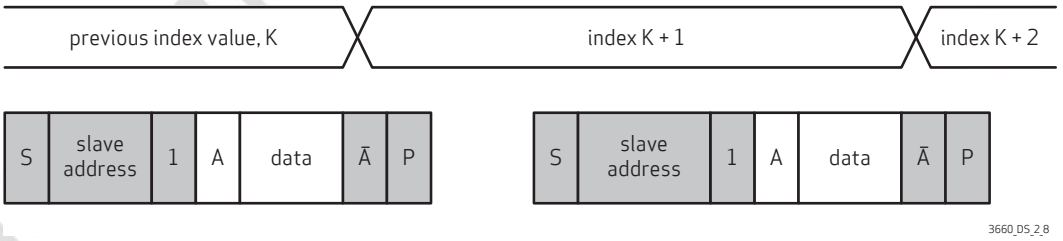
address, the camera starts to output data onto the SDA line as shown in **figure 6-2**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-2 SCCB single read from random location



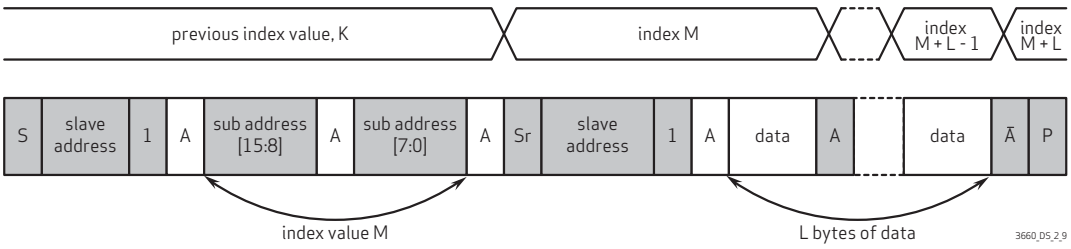
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 6-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-3 SCCB single read from current location



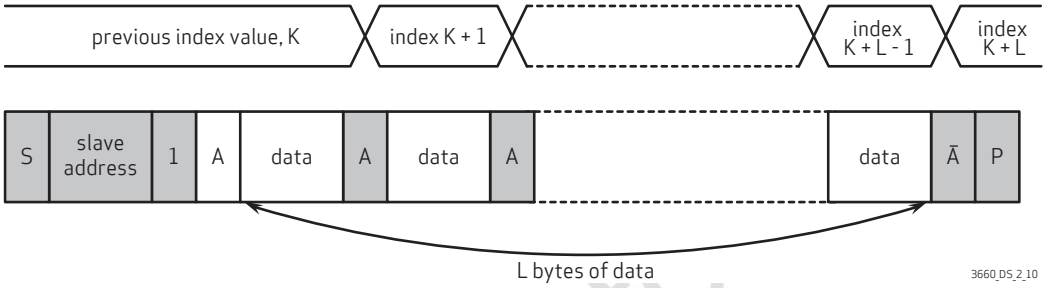
The sequential read from a random location is illustrated in **figure 6-4**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 6-4 SCCB sequential read from random location



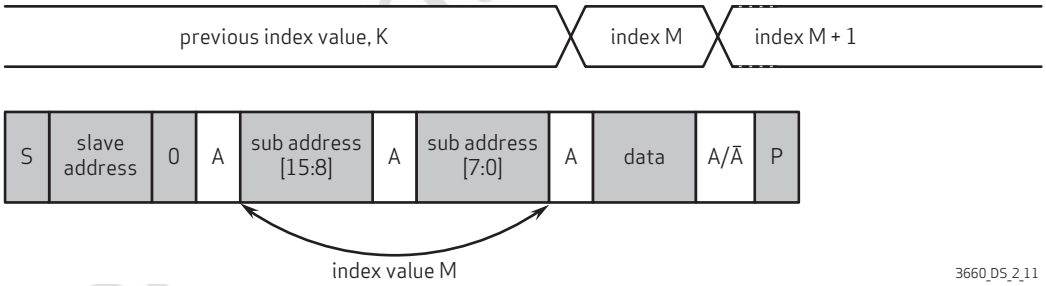
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 6-5**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-5 SCCB sequential read from current location



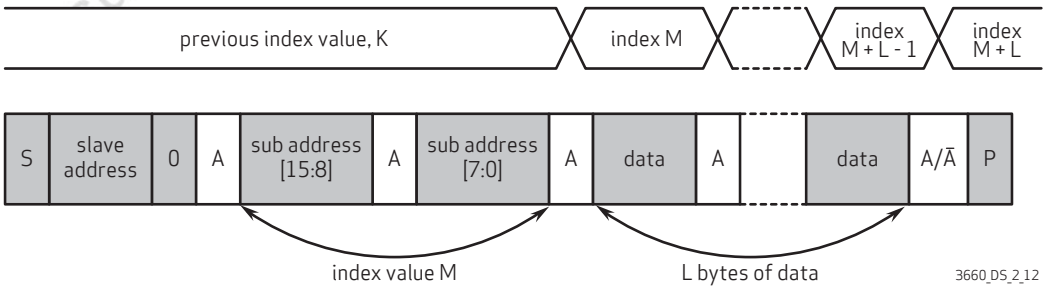
The write operation to a random location is illustrated in **figure 6-6**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 6-6 SCCB single write to random location



The sequential write is illustrated in **figure 6-7**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 6-7 SCCB sequential write to random location



6.4 SCCB timing

figure 6-8 SCCB interface timing

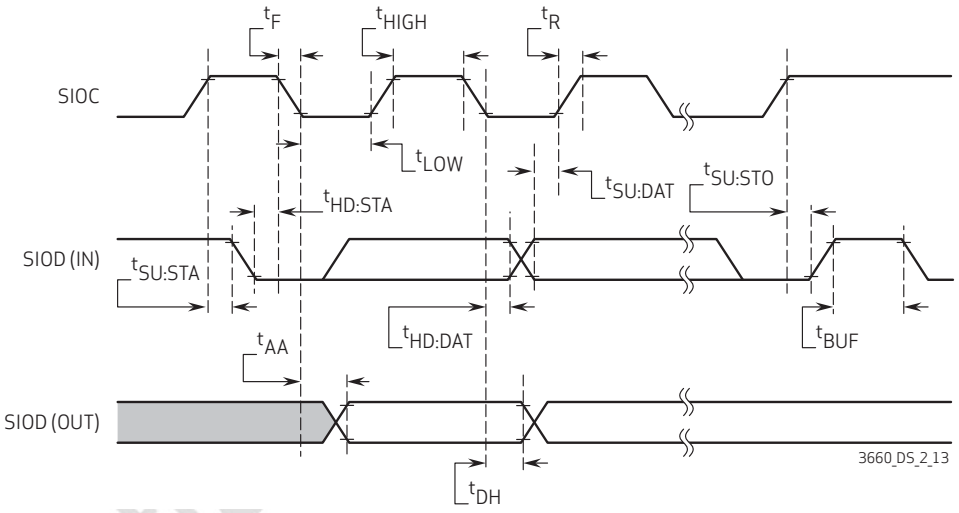


table 6-1 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

7 register tables

The following tables provide descriptions of the device control registers contained in the OV3660. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0.

7.1 system and IO pad control [0x3000 - 0x3052]

table 7-1 system and IO pad control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3000~ 0x3003	SYSTEM RESET00~ SYSTEM RESET03	–	RW	Reset for Individual Blocks
0x3004~ 0x3007	CLOCK ENABLE00	–	RW	Clock Enable Control for Individual Blocks
0x3008	SYSTEM CTROL0	0x02	RW	System Control Bit[7]: Software reset Bit[6]: Software power down Bit[5]: Reserve Bit[4]: SRB clock SYNC enable Bit[3]: Isolation suspend select Bit[2:0]: Not used
0x300A	CHIP ID HIGH BYTE	0x36	R	Chip ID High Byte
0x300B	CHIP ID LOW BYTE	0x60	R	Chip ID Low Byte
0x3016	PAD OUTPUT ENABLE 00	0x22	RW	Input/Output Control (0: input; 1: output) Bit[7:3]: Not used Bit[2]: FSIN output enable Bit[1]: STROBE output enable Bit[0]: Not used
0x3017	PAD OUTPUT ENABLE 01	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: Not used Bit[6]: VSYNC output enable Bit[5]: HREF output enable Bit[4]: PCLK output enable Bit[3:0]: D[9:6] output enable
0x3018	PAD OUTPUT ENABLE 02	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7:2]: D[5:0] output enable Bit[1:0]: GPIO1 output enable
0x3019	PAD OUTPUT VALUE 00	0xF0	RW	PAD Output Value Bit[7:3]: Not used Bit[2]: FSIN Bit[1]: STROBE Bit[0]: Not used

table 7-1 system and IO pad control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x301A	PAD OUTPUT VALUE 01	0x00	RW	GPIO Output Value 01 Bit[7]: Reserved Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x301B	PAD OUTPUT VALUE 02	0x00	RW	GPIO Output Value 02 Bit[7:2]: D[5:0] Bit[1:0]: Not used
0x301C	PAD SELECT 00	0x00	RW	Pad Selection Control Bit[7:3]: Not used Bit[2]: IO FSIN select Bit[1]: IO STROBE select Bit[0]: Not used
0x301D	PAD SELECT 01	0x00	RW	Output Selection for GPIO Bit[7]: Not used Bit[6]: VSYNC select Bit[5]: HREF select Bit[4]: PCLK select Bit[3:0]: IO D[9:6] select
0x301E	PAD SELECT 02	0x00	RW	Pad select control Bit[7:2]: IO D[5:0] select Bit[1:0]: Not used
0x302A	CHIP REVISION	0xB0	R	Bit[7:4]: Process 0xB: BSI Bit[3:0]: Chip revision
0x302C	PAD CONTROL	0x03	RW	Pad Control Bit[7:6]: Pad driving strength 00: 1x 01: 2x 10: 3x 11: 4x Bit[5]: pd_dato_en Bit[4:2]: Reserved Bit[1]: FSIN input enable Bit[0]: STROBE input enable
0x303A	SC PLLS CTRL0	0x00	RW	Bit[7]: PLLS bypass Bit[6:0]: Reserved
0x303B	SC PLLS CTRL1	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: PLLS multiplier
0x303C	SC PLLS CTRL2	0x11	RW	Bit[7]: Not used Bit[6:4]: PLL charge pump control Bit[3:0]: PLL system divider

table 7-1 system and IO pad control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x303D	SC PLLS CTRL3	0x30	RW	Bit[7:6]: Not used Bit[5:4]: PLLS predivider 00: /1 01: /1.5 10: /2 11: /3 Bit[3]: Not used Bit[2]: PLLS root divider 0: /1 1: /2 Bit[1:0]: PLLS seld5 00: /1 01: /1 10: /2 11: /2.5
0x3050	IO PAD VALUE	–	R	Read Pad Value Bit[7:4]: Not used Bit[3]: PWDN Bit[2]: Not used Bit[1]: SIOC Bit[0]: Not used
0x3051	IO PAD VALUE	–	R	Read Pad Value Bit[7]: OTP memory out Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x3052	IO PAD VALUE	–	R	Read Pad Value Bit[7:2]: D[5:0] Bit[1:0]: Not used

7.2 SCCB control [0x3100 - 0x3108]

table 7-2 SCCB control registers

address	register name	default value	R/W	description
0x3100	SCCB_ID	0x78	RW	SCCB Slave ID
0x3102	SCCB SYSTEM CTRL0	0x80	RW	Bit[7:6]: Not used Bit[5]: SRB reset Bit[4]: SCCB slave reset Bit[3]: rst_pon_sccb Bit[2]: Reserved Bit[1]: Not used Bit[0]: PLL reset
0x3103	SCCB SYSTEM CTRL1	0x11	RW	Bit[7:2]: Not used Bit[1]: Select PLL input clock 0: From pad clock 1: From pre divider (clock modulator) Bit[0]: Power up reset disable
0x3108	SYSTEM ROOT DIVIDER	0x16	RW	Bit[7:6]: Not used Bit[5:4]: PCLK root divider 00: PCLK = pll_clki 01: PCLK = pll_clki/2 10: PCLK = pll_clki/4 11: PCLK = pll_clki/8 Bit[3:2]: SCLK2x root divider 00: SCLK2x = pll_clki 01: SCLK2x = pll_clki/2 10: SCLK2x= pll_clki/4 11: SCLK2x= pll_clki/8 Bit[1:0]: SCLK root divider 00: SCLK = pll_clki 01: SCLK = pll_clki/2 10: SCLK= pll_clki/4 11: SCLK= pll_clki/8

7.3 SRB control [0x3200 - 0x3213]

table 7-3 SRB control registers

address	register name	default value	R/W	description
0x3200	GROUP ADDR0	0x40	RW	SRAM Group Address0
0x3201	GROUP ADDR1	0x4A	RW	SRAM Group Address1
0x3202	GROUP ADDR2	0x54	RW	SRAM Group Address2
0x3203	GROUP ADDR3	0x5E	RW	SRAM Group Address3
0x3212	SRM GROUP ACCESS	–	W	SRM Group Access Bit[7]: Group launch enable Bit[6]: Test mode access group Bit[5]: Group launch Bit[4]: Group hold end Bit[3:0]: Group ID 00x: Group for register access 011: Group to hold register address of embedded line SOF 100: Group to hold register address of embedded line EOF 101: Test mode for store register value to memory 110: Test mode for restore register value from memory 111: Group for write mask address
0x3213	SRM GROUP STATUS	–	R	SRM Group Status Bit[7]: Store Bit[6]: Restore Bit[5]: Group hold Bit[4]: Group launch Bit[3]: Group write Bit[2:0]: Group select

7.4 AWB gain control [0x3400 - 0x3406]

table 7-4 AWB gain control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3400	AWB R GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: AWB R gain[11:8]
0x3401	AWB R GAIN	0x00	RW	Bit[7:0]: AWB R gain[7:0]
0x3402	AWB G GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: AWB G gain[11:8]

table 7-4 AWB gain control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3403	AWB G GAIN	0x00	RW	Bit[7:0]: AWB G gain[7:0]
0x3404	AWB B GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: AWB B gain[11:8]
0x3405	AWB B GAIN	0x00	RW	Bit[7:0]: AWB B gain[7:0]
0x3406	AWB MANUAL CONTROL	0x00	RW	Bit[7:1]: Reserved Bit[0]: AWB gain manual enable 0: Auto 1: Manual

7.5 AEC/AGC control [0x3500 - 0x3513]

table 7-5 AEC/AGC control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:4]: Reserved Bit[3:0]: Exposure[19:16]
0x3501	AEC PK EXPOSURE	0x02	RW	Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:0]: Exposure[7:0]
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[7:6]: Reserved Bit[5]: Gain delay option Valid when 0x3503[4]=1'b0 0: Delay one frame latch 1: One frame latch Bit[4:2]: Reserved Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3504	AEC MANUAL SENSOR GAIN	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: AGC manual sensor gain[9:8] Valid when 0x3509[3]=1'b1
0x3505	AEC MANUAL SENSOR GAIN	0x00	RW	Bit[7:0]: AEC manual sensor gain[7:0] Valid when 0x3509[3]=1'b1

table 7-5 AEC/AGC control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3509	AEC GAIN CONTROL MISC	0x10	RW	Bit[7:6]: Reserved Bit[5]: Digital gain manual enable Bit[4]: Reserved Bit[3]: Gain manual enable Bit[2]: Reserved Bit[1:0]: Manual digital gain Valid when 0x3509[5]=1'b1
0x350A	AEC PK REAL GAIN	0x00	RW	Real Gain Bit[7:2]: Reserved Bit[1:0]: Real gain[9:8]
0x350B	AEC PK REAL GAIN	0x10	RW	Real Gain Bit[7:0]: Real gain[7:0]
0x350C	AEC PK ADD VTS	0x00	RW	AEC Add VTS output Bit[7:0]: Add VTS[15:8]
0x350D	AEC PK ADD VTS	0x00	RW	AEC Add VTS output Bit[7:0]: Add VTS[7:0]
0x3512	AEC PK SENSOR GAIN OUTPUT	–	R	Bit[7:2]: Reserved Bit[1:0]: AEC pk sensor gain[9:8]
0x3513	AEC PK SENSOR GAIN OUTPUT	–	R	Bit[7:0]: AEC pk sensor gain[7:0]

7.6 ANA control registers [0x3600 - 0x3634]

table 7-6 ANA control registers

address	register name	default value	R/W	description
0x3600~ 0x3634	RSVD	–	–	Reserved

7.7 sensor control [0x3700 - 0x373C]

table 7-7 sensor control registers

address	register name	default value	R/W	description
0x3700~ 0x373C	RSVD	–	–	Reserved

7.8 timing control [0x3800 - 0x3836]

table 7-8 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X address start[11:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: X address start[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y address start[11:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: Y address start[7:0]
0x3804	TIMING HW	0x08	RW	Bit[7:4]: Not used Bit[3:0]: X address end[11:8]
0x3805	TIMING HW	0x1F	RW	Bit[7:0]: X address end[7:0]
0x3806	TIMING VH	0x06	RW	Bit[7:4]: Not used Bit[3:0]: Y address end[11:8]
0x3807	TIMING VH	0x0B	RW	Bit[7:0]: Y address end[7:0]
0x3808	TIMING DVPHO	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x00	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x06	RW	Bit[7:4]: Not used Bit[3:0]: DVP output vertical height[11:8]
0x380B	TIMING DVPVO	0x00	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING HTS	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Total horizontal size[11:8]
0x380D	TIMING HTS	0xFC	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING VTS	0x06	RW	Bit[7:0]: Total vertical size[15:8]

table 7-8 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x380F	TIMING VTS	0x1C	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFSET	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING HOFFSET	0x10	RW	Bit[7:0]: Horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Vertical offset[10:8]
0x3813	TIMING VOFFSET	0x06	RW	Bit[7:0]: Vertical offset[7:0]
0x3814	TIMING X INC	0x11	RW	Bit[7:4]: Horizontal odd subsample increment Bit[3:0]: Horizontal even subsample increment
0x3815	TIMING Y INC	0x11	RW	Bit[7:4]: Vertical odd subsample increment Bit[3:0]: Vertical even subsample increment
0x3816	HSYNC START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HSYNC start point[11:8]
0x3817	HSYNC START	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	HSYNC WIDTH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HSYNC width[11:8]
0x3819	HSYNC WIDTH	0x00	RW	Bit[7:0]: HSYNC width[7:0]
0x3820	TIMING TC REG20	0x40	RW	Timing Control Bit[7:5]: Reserved Bit[4]: Blackline vflip Bit[3]: Reserved Bit[2]: ISP vflip Bit[1]: Sensor vflip Bit[0]: Vertical binning enable
0x3821	TIMING TC REG21	0x00	RW	Timing Control Bit[7:6]: Reserved Bit[5]: Compression enable Bit[4:3]: Reserved Bit[2]: ISP mirror Bit[1]: Sensor mirror Bit[0]: Horizontal binning enable
0x3835	TIMING TC REG35	0x00	RW	Bit[7:2]: Not used Bit[1]: FSIN reverse Bit[0]: FSIN enable
0x3836	TIMING TC REG36	0x00	RW	Bit[7:4]: Not used Bit[3:0] FSIN output width

7.9 AEC/AGC power down domain control [0x3A00 - 0x3A25]

table 7-9 AEC/AGC power down domain control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x78	RW	AEC System Control (0: disable; 1: enable) Bit[7:6]: Reserved Bit[5]: Band function enable Bit[4]: Less 1 band enable Bit[3]: Start selection Bit[2]: Night mode Bit[1]: New balance function Bit[0]: Freeze
0x3A01	AEC MIN EXPOSURE	0x04	RW	Minimum Exposure Output Limit Bit[7:0]: Minimum exposure
0x3A02	AEC MAX EXPO (60HZ)	0x30	RW	60Hz Maximum Exposure Output Limit Bit[7:0]: Maximum exposure[15:8]
0x3A03	AEC MAX EXPO (60HZ)	0xC0	RW	60Hz Maximum Exposure Output Limit Bit[7:0]: Maximum exposure[7:0]
0x3A04	RSVD	–	–	Reserved
0x3A05	AEC CTRL05	0x30	RW	AEC System Control 2 Bit[7]: Reserved Bit[6]: frame insert 0: In night mode, insert frame disable 1: In night mode, insert frame enable Bit[5]: Step auto enable 0: Step manual mode 1: Step auto mode Bit[4:0]: Step auto ratio In step auto mode, step ratio setting to adjust speed
0x3A06	AEC CTRL06	0x10	RW	AEC System Control 3 Bit[7:5]: Reserved Bit[4:0]: Step manual setting 1 Step manual Increase mode fast step
0x3A07	AEC CTRL07	0x18	RW	AEC Manual Step Register Bit[7:4]: Step manual setting 2 Step manual, slow step Bit[3:0]: Step manual setting 3 Step manual, decrease mode fast step

table 7-9 AEC/AGC power down domain control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3A08	AEC B50 STEP	0x00	RW	50Hz Band Width Bit[7:2]: Reserved Bit[1:0]: B50 step[9:8]
0x3A09	AEC B50 STEP	0xEA	RW	50Hz Band Width Bit[7:0]: B50 step[7:0]
0x3A0A	AEC B60 STEP	0x00	RW	60Hz Band Width Bit[7:2]: Reserved Bit[1:0]: B60 step[13:8]
0x3A0B	AEC B60 STEP	0xC3	RW	60Hz Band Width Bit[7:0]: B60 step[7:0]
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: E1 max Decimal line high limit zone Bit[3:0]: E1 min Decimal line low limit zone
0x3A0D	AEC CTRL0D	0x08	RW	60Hz Max Bands in One Frame Bit[7:6]: Reserved Bit[5:0]: B60 max
0x3A0E	AEC CTRL0E	0x06	RW	50Hz Max Bands in One Frame Bit[7:6]: Debug mode Bit[5:0]: B50 max
0x3A0F	AEC CTRL0F	0x78	RW	Stable Range High Limit (Enter) Bit[7:0]: WPT
0x3A10	AEC CTRL10	0x68	RW	Stable Range Low Limit (Enter) Bit[7:0]: BPT
0x3A11	AEC CTRL11	0xD0	RW	Step Manual Mode, Fast Zone High Limit Bit[7:0]: VPT high
0x3A12	RSVD	–	–	Reserved
0x3A13	AEC CTRL13	0x90	RW	Bit[7]: Pre-gain enable Bit[6:0]: Pre-gain enable 0x10: 1x
0x3A14	AEC MAX EXPO (50HZ)	0x30	RW	50Hz Maximum Exposure Output Limit Bit[7:4]: Reserved Bit[3:0]: Max exposure[15:8]
0x3A15	AEC MAX EXPO (50HZ)	0x72	RW	50Hz Maximum Exposure Output Limit Bit[7:0]: Max exposure[7:0]
0x3A16	RSVD	–	–	Reserved

table 7-9 AEC/AGC power down domain control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3A17	AEC CTRL17	0x01	RW	Gain Base When in Night Mode Bit[7:2]: Reserved Bit[1:0]: Gain night threshold 00: 0x00 01: 0x10 10: 0x30 11: 0x70
0x3A18	AEC GAIN CEILING	0x07	RW	Gain Output Top Limit Bit[7:2]: Reserved Bit[1:0]: AEC gain ceiling[9:8] Real gain format
0x3A19	AEC GAIN CEILING	0xC0	RW	Gain Output Top Limit Bit[7:0]: AEC gain ceiling[7:0] Real gain format
0x3A1A	AEC DIFF MIN	0x00	RW	Reserved Default Value for This Register Bit[7:0]: Difference minimal
0x3A1B	AEC CTRL1B	0x78	RW	Stable Range High Limit (Go Out) Bit[7:0]: WPT2
0x3A1C	LED ADD ROW	0x06	RW	Exposure Values Added When Strobe is On Bit[7:0]: AEC LED add row[15:8]
0x3A1D	LED ADD ROW	0x18	RW	Exposure Values Added When Strobe is On Bit[7:0]: AEC LED add row[7:0]
0x3A1E	AEC CTRL1E	0x68	RW	Stable Range Low Limit (Go Out) Bit[7:0]: BPT2
0x3A1F	AEC CTRL1F	0x40	RW	Step Manual Mode, Fast Zone Low Limit Bit[7:0]: VPT low
0x3A20	AEC CTRL20	0x20	RW	Bit[7:3]: Reserved Bit[2]: Strobe option Bit[1:0]: Reserved
0x3A21	AEC CTRL21	0x78	RW	Bit[7]: Reserved Bit[6:4]: Insert frame number Bit[3:0]: Reserved
0x3A25	AEC CTRL25	0x00	RW	Bit[7:5]: Reserved Bit[4:2]: Freeze count Bit[1:0]: Reserved

7.10 strobe control [0x3B00]

table 7-10 strobe registers

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe request on/off 0: Off 1: On Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon Bit[1:0]: Strobe mode 00: Xenon 01: LED1 10: LED2 11: LED3

7.11 sigmadelta/5060Hz detector [0x3C00 - 0x3C1E]

table 7-11 sigmadelta/5060HZ detector registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3C00	SIGMADELTA CTRL00	0x00	RW	Bit[7:6]: Reserved Bit[5]: Time counter threshold divisor enable Bit[4]: Low limit enable Bit[3]: Reserve sigmaq Bit[2]: Band50 default value Bit[1:0]: Time counter threshold 00: 1s 01: 2s 10: 4s 11: 8s
0x3C01	SIGMADELTA CTRL01	0x00	RW	Bit[7]: Band manual enable Bit[6]: Band begin reset enable Bit[5]: Sum auto mode enable Bit[4]: Band counter enable Bit[3:0]: Band counter Counter threshold for band change
0x3C02	SIGMADELTA CTRL02	0x00	RW	Bit[7:6]: Low light limit mode Bit[5:0]: Low light threshold No detection under low light
0x3C03	SIGMADELTA CTRL03	0x00	RW	Bit[7:0]: Counter threshold for low light
0x3C04	SIGMADELTA CTRL04	0x20	RW	Bit[7:0]: Threshold for low sum

table 7-11 sigmadelta/5060HZ detector registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3C05	SIGMADELTA CTRL05	0x70	RW	Bit[7:0]: Threshold for high sum
0x3C06	LIGHT METER1 THRESHOLD	0x00	RW	Bit[7:0]: Lightmeter1 threshold[15:8]
0x3C07	LIGHT METER1 THRESHOLD	0x00	RW	Bit[7:0]: Lightmeter1 threshold[7:0]
0x3C08	LIGHT METER2 THRESHOLD	0x01	RW	Bit[7:0]: Lightmeter2 threshold[15:8]
0x3C09	LIGHT METER2 THRESHOLD	0x2C	RW	Bit[7:0]: Lightmeter2 threshold[7:0]
0x3C0A	SAMPLE NUMBER	0x4E	RW	Bit[7:0]: Sample number[15:8]
0x3C0B	SAMPLE NUMBER	0x1F	RW	Bit[7:0]: Sample number[7:0]
0x3C0C	SIGMADELTA CTRL0C	–	R	Bit[7:1]: Reserved Bit[0]: Band50/60 0: 60Hz light 1: 50Hz light
0x3C0D	SUM 50	–	R	Bit[7:5]: Not used Bit[4:0]: Sum50[28:24]
0x3C0E	SUM 50	–	R	Bit[7:0]: Sum50[23:16]
0x3C0F	SUM 50	–	R	Bit[7:0]: Sum50[15:8]
0x3C10	SUM 50	–	R	Bit[7:0]: Sum50[7:0]
0x3C11	SUM 60	–	R	Bit[7:5]: Not used Bit[4:0]: Sum60[28:24]
0x3C12	SUM 60	–	R	Bit[7:0]: Sum60[23:16]
0x3C13	SUM 60	–	R	Bit[7:0]: Sum60[15:8]
0x3C14	SUM 60	–	R	Bit[7:0]: Sum60[7:0]
0x3C15	SUM 50 60	–	R	Bit[7:0]: Sum50/60[15:8]
0x3C16	SUM 50 60	–	R	Bit[7:0]: Sum50/60[7:0]
0x3C17	BLOCK COUNTER	–	R	Bit[7:0]: Block counter[15:8]
0x3C18	BLOCK COUNTER	–	R	Bit[7:0]: Block counter[7:0]
0x3C19	B6	–	R	Bit[7:0]: B6[15:8]
0x3C1A	B6	–	R	Bit[7:0]: B6[7:0]
0x3C1B	LIGHTMETER OUTPUT	–	R	Bit[7:4]: Not used Bit[3:0]: Light meter output[19:16]
0x3C1C	LIGHTMETER OUTPUT	–	R	Bit[7:0]: Light meter output[15:8]

table 7-11 sigmadelta/5060HZ detector registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3C1D	LIGHTMETER OUTPUT	–	R	Bit[7:0]: Light meter output[7:0]
0x3C1E	SUM THRESHOLD	–	R	Delta Sum Threshold

7.12 OTP control [0x3D00 - 0x3D21]

table 7-12 OTP control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D00	OTP DATA00	0x00	RW	OTP Dump/Load Data00
0x3D01	OTP DATA01	0x00	RW	OTP Dump/Load Data01
0x3D02	OTP DATA02	0x00	RW	OTP Dump/Load Data02
0x3D03	OTP DATA03	0x00	RW	OTP Dump/Load Data03
0x3D04	OTP DATA04	0x00	RW	OTP Dump/Load Data04
0x3D05	OTP DATA05	0x00	RW	OTP Dump/Load Data05
0x3D06	OTP DATA06	0x00	RW	OTP Dump/Load Data06
0x3D07	OTP DATA07	0x00	RW	OTP Dump/Load Data07
0x3D08	OTP DATA08	0x00	RW	OTP Dump/Load Data08
0x3D09	OTP DATA09	0x00	RW	OTP Dump/Load Data09
0x3D0A	OTP DATA0A	0x00	RW	OTP Dump/Load Data0a
0x3D0B	OTP DATA0B	0x00	RW	OTP Dump/Load Data0b
0x3D0C	OTP DATA0C	0x00	RW	OTP Dump/Load Data0c
0x3D0D	OTP DATA0D	0x00	RW	OTP Dump/Load Data0d
0x3D0E	OTP DATA0E	0x00	RW	OTP Dump/Load Data0e
0x3D0F	OTP DATA0F	0x00	RW	OTP Dump/Load Data0f
0x3D10	OTP DATA10	0x00	RW	OTP Dump/Load Data10
0x3D11	OTP DATA11	0x00	RW	OTP Dump/Load Data11
0x3D12	OTP DATA12	0x00	RW	OTP Dump/Load Data12
0x3D13	OTP DATA13	0x00	RW	OTP Dump/Load Data13
0x3D14	OTP DATA14	0x00	RW	OTP Dump/Load Data14

table 7-12 OTP control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D15	OTP DATA15	0x00	RW	OTP Dump/Load Data15
0x3D16	OTP DATA16	0x00	RW	OTP Dump/Load Data16
0x3D17	OTP DATA17	0x00	RW	OTP Dump/Load Data17
0x3D18	OTP DATA18	0x00	RW	OTP Dump/Load Data18
0x3D19	OTP DATA19	0x00	RW	OTP Dump/Load Data19
0x3D1A	OTP DATA1A	0x00	RW	OTP Dump/Load Data1A
0x3D1B	OTP DATA1B	0x00	RW	OTP Dump/Load Data1B
0x3D1C	OTP DATA1C	0x00	RW	OTP Dump/Load Data1C
0x3D1D	OTP DATA1D	0x00	RW	OTP Dump/Load Data1D
0x3D1E	OTP DATA1E	0x00	RW	OTP Dump/Load Data1E
0x3D1F	OTP DATA1F	0x00	RW	OTP Dump/Load Data1F
0x3D20	OTP PROGRAM CTRL	0x00	RW	Bit[7]: OTP program busy Bit[6:2]: Not used Bit[1]: OTP program speed 0: Fast 1: Slow Bit[0]: OTP program enable
0x3D21	OTP READ CTRL	0x00	RW	Bit[7]: OTP read busy Bit[6:2]: Not used Bit[1]: OTP read speed 0: Fast 1: Slow Bit[0]: OTP read enable

7.13 BLC control [0x4000 - 0x4033]

table 7-13 BLC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x0D	RW	BLC Control 00 (0: disable; 1: enable) Bit[7:4]: Reserved Bit[3]: BGR comp enable Bit[2]: Apply selection Bit[1]: Mid filter enable Bit[0]: BLC enable

table 7-13 BLC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4001	BLC CTRL01	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: BLC start line
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable BLC update when format changes Bit[6]: BLC auto enable 0: Manual 1: Auto Bit[5:0]: Reset frame number Frame number BLC do after reset
0x4003	BLC CTRL03	0x01	RW	Bit[7]: BLC redo enable Write 1 to this bit will trigger a BLC redo N frames begin, where N is 0x4003[5:0] Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4004	BLC CTRL04	0x08	RW	Bit[7:0]: BLC line number Specify the line number BLC process
0x4005	BLC CTRL05	0x10	RW	Bit[7:2]: Reserved Bit[1]: BLC always update 0: Normal freeze 1: BLC always update Bit[0]: Reserved
0x4006	BLC CTRL06	0x08	RW	Bit[7]: Reserved Bit[6]: Black line number manual enable Bit[5:0]: Black number manual
0x4007	BLC CTRL07	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: Window selection 00: Full image 01: A windows not contain the first 16 pixels and the end 16 pixels 10: A windows not contain the first 1/16 image and the end 1/16 image 11: A windows not contain the first 1/8 image and the end 1/8 image Bit[2:0]: Reserved
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: BLC black level target at 10-bit range
0x400A~ 0x402B	RSVD	–	–	Reserved
0x402C	BLACK LEVEL00	0x00	RW	Bit[7:0]: Blacklevel00[15:8] With 3 decimal

table 7-13 BLC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x402D	BLACK LEVEL00	0x00	RW	Bit[7:0]: Blacklevel00[7:0] With 3 decimal
0x402E	BLACK LEVEL01	0x00	RW	Bit[7:0]: Blacklevel01[15:8] With 3 decimal
0x402F	BLACK LEVEL01	0x00	RW	Bit[7:0]: Blacklevel01[7:0] With 3 decimal
0x4030	BLACK LEVEL10	0x00	RW	Bit[7:0]: Blacklevel10[15:8] With 3 decimal
0x4031	BLACK LEVEL10	0x00	RW	Bit[7:0]: Blacklevel10[7:0] With 3 decimal
0x4032	BLACK LEVEL11	0x00	RW	Bit[7:0]: Blacklevel11[15:8] With 3 decimal
0x4033	BLACK LEVEL11	0x00	RW	Bit[7:0]: Blacklevel11[7:0] With 3 decimal

7.14 frame control [0x4201 - 0x4202]

table 7-14 frame control registers

address	register name	default value	R/W	description
0x4201	FRAME CTRL01	0x00	R/W	Control Passed Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Not used Bit[3:0]: Frame ON number
0x4202	FRAME CTRL02	0x00	R/W	Control Masked Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Not used BIT[3:0]: Frame OFF number

7.15 format control [0x4300 - 0x430D]

table 7-15 format control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4300	FORMAT CTRL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format selection 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: Not used 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4~0x5: Not used 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]}

table 7-15 format control registers (sheet 2 of 4)

address	register name	default value	R/W	description
				0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xF: Not allowed 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]} 0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]} 0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]} 0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed 0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]} 0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0}

table 7-15 format control registers (sheet 3 of 4)

address	register name	default value	R/W	description
				0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xF: Not allowed 0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0,g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0,g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0,r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0,b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0,b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0,r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed 0xF: Bypass formatter module Bit[3:0]: Output format 0x8: Raw 0x9: YUV422

table 7-15 format control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4301	FORMAT CTRL 01	0x00	RW	Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 10: Not valid 11: U/V generated from second pixel
0x4302	YMAX VALUE	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Set y max clip value[9:8]
0x4303	YMAX VALUE	0xFF	RW	Bit[7:0]: Set y max clip value[7:0]
0x4304	YMIN VALUE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Set y min clip value[9:8]
0x4305	YMIN VALUE	0x00	RW	Bit[7:0]: Set y min clip value[7:0]
0x4306	UMAX VALUE	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Set u max clip value[9:8]
0x4307	UMAX VALUE	0xFF	RW	Bit[7:0]: Set u max clip value[7:0]
0x4308	UMIN VALUE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Set u min clip value[9:8]
0x4309	UMIN VALUE	0x00	RW	Bit[7:0]: Set u min clip value[7:0]
0x430A	VMAX VALUE	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Set v max clip value[9:8]
0x430B	VMAX VALUE	0xFF	RW	Bit[7:0]: Set v max clip value[7:0]
0x430C	VMIN VALUE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Set v min clip value[9:8]
0x430D	VMIN VALUE	0x00	RW	Bit[7:0]: Set v min clip value[7:0]

7.16 compression control [0x4400 - 0x4458]

table 7-16 compression control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4400	COMPRESSION CTRL00	0x81	RW	Bit[7]: input_format 0: YUV420 1: YUV422 Bit[6:0]: JFIFO read speed control
0x4401	COMPRESSION CTRL01	0x01	RW	Bit[7:4]: SFIFO output buffer speed control Bit[3]: Read SRAM enable when blanking 0: Disable 1: Enable Bit[2]: Read SRAM at first blanking 0: Disable 1: Enable Bit[1:0]: SFIFO read speed control
0x4402	COMPRESSION CTRL02	0x10	RW	Bit[7]: SFIFO output control mode 0: Control by HREF and valid which before scale down 1: Control by input HREF and valid Bit[6:4]: SOF control 001: Start at the first valid HREF 010: Start at the eighth valid HREF Bit[3:0]: SFIFO output buffer speed control at last stripe
0x4403	COMPRESSION CTRL03	0x33	RW	Bit[7]: Memory select 0: Select ROM QT 1: Select SRAM QT Bit[6]: MPEG enable Bit[5]: Enable zero stuff Bit[4]: Enable Huffman table output Bit[3]: Rounding enable for C Bit[2]: Rounding enable for Y Bit[1]: Input shift 128 select for C Bit[0]: Input shift 128 select for Y
0x4404	COMPRESSION CTRL04	0x24	RW	Bit[7]: jfifo_pwrdn Bit[6]: SFIFO power down Bit[5]: Header output enable Bit[4]: Enable gated clock 0: Disable gated clock 1: Enable gated clock Bit[3]: Substitute 0xFF to 0xFE in QT Bit[2:0]: Quantization rounding bias: Set value = Bias/8
0x4405	COMPRESSION CTRL05	0x40	RW	Bit[7:0]: QZ out truncate for Y

table 7-16 compression control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4406	COMPRESSION CTRL06	0x40	RW	Bit[7:0]: QZ out truncate for C
0x4407	COMPRESSION CTRL07	0x0C	RW	Bit[7]: Enable read QTA auto increment Bit[5:0]: QS Quantization scale
0x4408	COMPRESSION ISI CTRL	0x00	RW	Bit[7]: Scalado mode enable 0: Normal 1: Insert 0xFF after EOB Bit[6]: Compression size manual enable Bit[5:4]: Reserved Bit[3]: Replace 0xFF to 0xFE in comment data Bit[2]: Cut 0xD9 at the end of frame Bit[1]: EOI generation enable Bit[0]: ISI insert
0x4409	COMPRESSION CTRL09	0x00	RW	Bit[7:0]: D9 data
0x440A	COMPRESSION CTRL0A	0x4E	RW	Bit[7:0]: JFIFO output delay
0x440B	COMPRESSION CTRL0B	0x16	RW	Bit[7:6]: Not used Bit[5]: Dummy read speed manual mode Bit[4:0]: SFIFO SOF delay
0x440C	COMPRESSION CTRL0C	0x00	RW	Bit[7:0]: Dummy read speed
0x440D	COMPRESSION CTRL0D	0x0A	RW	Bit[7:5]: Not used Bit[4]: JFIFO test1 Bit[3:0]: JFIFO rm
0x440E	COMPRESSION CTRL0E	0x09	RW	Bit[7:5]: Not used Bit[4]: SFIFO test1 Bit[3:0]: SFIFO rm
0x4410	COMPRESSION QT DATA	0x00	RW	Bit[7:0]: QT data
0x4411	COMPRESSION QT ADDR	0x00	RW	Bit[7:0]: QT address
0x4412	COMPRESSION ISI DATA	0x00	RW	Bit[7:0]: ISI data
0x4413	COMPRESSION ISI CTRL	–	R	Bit[7:4]: Not used Bit[3]: D9 odd (read only) Bit[2]: Reset counter write 0: Not valid 1: Reset counter Bit[1]: ISO EOF

table 7-16 compression control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4414	COMPRESSION LENGTH	–	R	Bit[7:0]: Compression length[23:16]
0x4415	COMPRESSION LENGTH	–	R	Bit[7:0]: Compression length[15:8]
0x4416	COMPRESSION LENGTH	–	R	Bit[7:0]: Compression length[7:0]
0x4417	JFIFO OVERFLOW	–	R	Bit[7:1]: Not used Bit[0]: JFIFO overflow indicator
0x4420~ 0x442F	COMPRESSION COMMENT	0x00	RW	Compression Comment Data Embedded in Compression Data
0x4430	COMPRESSION COMMENT	0x00	RW	Comment Length Two bytes align
0x4431	COMPRESSION COMMENT	0xFE	RW	Comment Data Marker
0x4440	COMPRESSION H SIZE MANUAL	0x02	RW	Compression Header Horizontal Size Manual
0x4441	COMPRESSION H SIZE MANUAL	0x80	RW	Compression Header Horizontal Size Manual
0x4442	COMPRESSION V SIZE MANUAL	0x01	RW	Compression Header Vertical Size Manual
0x4443	COMPRESSION V SIZE MANUAL	0xE0	RW	Compression Header Vertical Size Manual
0x4457	DRI HIGH	0x00	RW	Compression Dri High
0x4458	DRI LOW	0x02	RW	Compression Dri Low

7.17 VFIFO control [0x4600 - 0x460D]

table 7-17 VFIFO registers

address	register name	default value	R/W	description
0x4600	VFIFO CTRL00	0x80	RW	Bit[7:6]: Not used Bit[5]: Compression output fixed height enable 0: In compression mode2, Compression height is different in each frame 1: in compression mode2, Compression height is fixed in each frame Bit[4]: Test pattern enable, incremental pattern Bit[3:0]: Debug mode
0x4602	VFIFO HSIZE	0x04	RW	Compression Output Width High Byte
0x4603	VFIFO HSIZE	0x00	RW	Compression Output Width Low Byte
0x4604	VFIFO VSIZE	0x03	RW	Compression Output Height High Byte
0x4605	VFIFO HSIZE	0x00	RW	Compression Output Height Low Byte
0x460C	VFIFO CTRL0C	0x20	RW	Bit[7:4]: Compression dummy data pad speed Bit[2]: Footer disable Compression footer disable 0: In compression mode2 footer will be added in the last six bytes of each frame 1: Disable footer Bit[1]: PCLK manual enable 0: DVP PCLK divider control by auto mode 1: DVP PCLK divider control by 0x3824[4:0] Bit[0]: Not used
0x460D	VFIFO CTRL0D	0x00	RW	Dummy Data

7.18 DVP control [0x4709 - 0x4745]

table 7-18 DVP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4709	DVP VSYNC WIDTH0	0x02	RW	VSYNC Width Line Unit
0x470A	DVP VSYNC WIDTH1	0x00	RW	VSYNC Width PCLK Unit High Byte
0x470B	DVP VSYNC WIDTH2	0x01	RW	VSYNC Width PCLK Unit Low Byte
0x4711	PAD LEFT CTRL	0x00	RW	HSYNC Mode Left Padding Pixel Count Add padding data at start of a line
0x4712	PAD RIGHT CTRL	0x00	RW	HSYNC Mode Right Padding Pixel Count Add padding data at end of a line
0x4713	COMPRESSION MODE SELECT	0x02	RW	Bit[7:3]: Not used Bit[2:0]: Compression mode select 001: Compression mode 1 010: Compression mode 2 011: Compression mode 3 100: Compression mode 4 101: Compression mode 5 110: Compression mode 6
0x4715	656 DUMMY LINE	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CCIR656 dummy line number Control dummy line number at beginning of the frame
0x4719	CCIR656 CTRL	0x01	RW	Bit[7:2]: Not used Bit[1:0]: CCIR656 EAV/SAV option
0x471B	HSYNC CTRL00	0x02	RW	Bit[7:1]: Not used Bit[0]: HSYNC mode enable
0x471D	DVP VSYNC CTRL	0x01	RW	Bit[7:3]: Not used Bit[2]: vsync_sel1_clr Bit[1:0]: vsync_mode 00: VSYNC positive edge trigger by end of field, negative edge trigger by start of frame 01: VSYNC positive edge trigger by end of frame, the width define by register 10: VSYNC positive edge trigger by start of field, the width defined by register

table 7-18 DVP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x471F	DVP HREF CTRL	0x40	RW	HREF Minimum Blanking in Compression Mode23
0x4721	VERTICAL START OFFSET	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical start delay between video output and video input
0x4722	VERTICAL END OFFSET	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Vertical end delay between video output and video input
0x4723	DVP CTRL23	0x00	RW	DVP Compression Mode456 Skip Line Number
0x4730	CCIR656 CTRL00	0x00	RW	Bit[7]: SYNC code selection 0: Auto generate sync code 1: Sync code from register setting 0x4732~4735 Bit[6]: F value in CCIR656 SYNC code when fixed f value Bit[5]: Fixed f value Bit[4:3]: Blank toggle data options 00: Toggle data is 1'h040/1'h200 01: Use register setting 0x4736~0x4738 10: Blanking data always keep 0 Bit[2]: Debug mode Bit[1]: Clip data disable Bit[0]: CCIR656 mode enable
0x4731	CCIR656 CTRL01	0x01	RW	Bit[7:1]: Not used Bit[0]: Blanking toggle data order option
0x4732	CCIR656 FS	0x01	RW	CCIR656 SYNC Code Frame Start
0x4733	CCIR656 FE	0x0F	RW	CCIR656 SYNC Code Frame End
0x4734	CCIR656 LS	0x00	RW	CCIR6656 SYNC Code Line Start
0x4735	CCIR656 LE	0x00	RW	CCIR656 SYNC Code Line End
0x4736	CCIR656 CTRL6	0x00	RW	Bit[7:4]: Not used Bit[3:2]: Toggle data0[9:8] Bit[1:0]: Toggle data1[9:8]
0x4737	CCIR656 CTRL7	0x00	RW	Bit[7:0]: Toggle data0[7:0]
0x4738	CCIR656 CTRL8	0x00	RW	Bit[7:0]: Toggle data1[7:0]

table 7-18 DVP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4740	POLARITY CTRL00	0x20	RW	Bit[7:6]: Not used Bit[5]: PCLK polarity 0: Active low 1: Active high Bit[4]: Reserved Bit[3]: Gate PCLK under VSYNC Bit[2]: Gate PCLK under HREF Bit[1]: HREF polarity 0: Active low 1: Active high Bit[0]: VSYNC polarity 0: Active low 1: Active high
0x4741	TEST PATTERN	0x00	RW	Bit[7:3]: Not used Bit[2]: Test pattern enable Bit[1]: Test pattern select 0: Output test pattern 0 1: Output test pattern 1 Bit[0]: Test pattern 8-bit/10-bit 0: 10-bit test pattern 1: 8-bit test pattern
0x4745	DATA ORDER	0x00	RW	Bit[7:3]: Not used Bit[2:1]: DVP order option for debug 00: D[9:0] 10: {D[7:0],D[9:8]} x1: {D[1:0],D[9:2]} Bit[0]: Output data order 0: Normal output 1: Reverse output data bit order

7.19 ISP frame control [0x4901 - 0x4902]

table 7-19 ISP frame control registers

address	register name	default value	R/W	description
0x4901	FRAME CTRL01	0x00	RW	Control Passed Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Not used Bit[3:0]: Frame ON number
0x4902	FRAME CTRL02	0x00	RW	Control Masked Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Not used Bit[3:0]: Frame OFF number

7.20 ISP top control [0x5000 - 0x5063]

table 7-20 ISP top control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Reserved Bit[5]: Gamma enable 0: Disable 1: Enable Bit[4:3]: Reserved Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation enable 0: Disable 1: Enable

table 7-20 ISP top control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Special digital effect enable 0: Disable 1: Enable Bit[6]: Reserved Bit[5]: Scale enable 0: Disable 1: Enable Bit[4:3]: Reserved Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance enable 0: Disable 1: Enable
0x5003	ISP CONTROL 03	0x08	RW	Bit[7:3]: Reserved Bit[2]: Bin enable 0: Disable 1: Enable Bit[1]: Reserved Bit[0]: Solarize enable 0: Disable 1: Enable
0x5004	ISP CONTROL 04	0x08	RW	Bit[7:4]: Reserved Bit[3]: Size auto control enable 0: Manual 1: Automatic Bit[2:0]: Reserved

table 7-20 ISP top control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5005	ISP CONTROL 05	0x36	RW	Bit[7]: Reserved Bit[6]: AWB bias manual enable 0: Disable 1: Enable Bit[5]: AWB bias ON enable 0: Disable 1: Enable Bit[4]: AWB bias plus enable 0: Disable 1: Enable Bit[3]: Reserved Bit[2]: LENC bias ON enable 0: Disable 1: Enable Bit[1]: GMA bias ON enable 0: Disable 1: Enable Bit[0]: LENC bias manual enable 0: Disable 1: Enable
0x5006~ 0x501C	RSVD	–	–	Reserved
0x501D	ISP MISC	0x00	RW	Bit[7]: Reserved Bit[6]: SDE AVG manual enable Bit[5]: AWB YUV2CBCR enable Bit[4]: Average size manual enable Bit[3:0]: Reserved
0x501E	RSVD	–	–	Reserved
0x501F	FORMAT CTRL	0x03	RW	Format Control Bit[7:6]: Not used Bit[5]: Enable option Bit[4]: Reserved Bit[3]: Format vfirst Bit[2:0]: Format select 000: YUV422 001: RGB 010: Dither 011: RAW after DPC 101: RAW after CIP
0x5020	DITHER CTRL 0	0x00	RW	Bit[7]: Not used Bit[6]: Dither MUX Bit[5:4]: R dithering Bit[3:2]: G dithering Bit[1:0]: B dithering

table 7-20 ISP top control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: Test enable 0: Test disable 1: Color bar enable Bit[6]: Rolling Bit[5]: Transparent Bit[4]: Square black and white Bit[3:2]: Color bar style 00: Standard 8 color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2 Bit[1:0]: Test select 00: Color bar 01: Random data 10: Square data 11: Black image
0x503E~ 0x5060	RSVD	–	–	Reserved
0x5061	ISP SENSOR BIAS I	–	R	ISP Sensor Bias Input
0x5062	ISP SENSOR GAIN I	–	R	ISP Real Gain Input High Byte
0x5063	ISP SENSOR GAIN I	–	R	ISP Real Gain Input Low Byte

7.21 AWB control [0x5180 - 0x51D0]

table 7-21 AWB registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5180	AWB CONTROL 00	0xFF	RW	Bit[7:0]: AWB B block
0x5181	AWB CONTROL 01	0x58	RW	Bit[7:6]: Step local Bit[5:4]: Step fast Bit[3]: Slop 8x Bit[2]: Slop 4x Bit[1]: One zone Bit[0]: AVG all
0x5182	AWB CONTROL 02	0x11	RW	Bit[7:4]: Max local counter Bit[3:0]: Max fast counter

table 7-21 AWB registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5183	AWB CONTROL 03	0x90	RW	Bit[7]: AWB simple enable 0: AWB advance 1: AWB simple Bit[6]: YUV enable 0: YUV enable 1: Simple YUV enable Bit[5]: AWB preset Bit[4]: AWB SIMF Bit[3:2]: AWB win Bit[1:0]: Reserved
0x5184	AWB CONTROL 04	0x25	RW	Bit[7:6]: Count area selection Bit[5]: G enable Bit[4:2]: Count limit control Bit[1:0]: Counter threshold
0x5185	AWB CONTROL 05	0x24	RW	Bit[7:4]: Stable range unstable Threshold for unstable to stable change Bit[3:0]: Stable range stable Threshold for stable to unstable change
0x5186~ 0x5190	AWB CONTROL	–	RW	Advanced AWB Control
0x5191	AWB CONTROL 17	0xFF	RW	Bit[7:0]: AWB top limit
0x5192	AWB CONTROL 18	0x00	RW	Bit[7:0]: AWB bottom limit
0x5193	AWB CONTROL 19	0xF0	RW	Bit[7:0]: Red limit
0x5194	AWB CONTROL 20	0xF0	RW	Bit[7:0]: Green limit
0x5195	AWB CONTROL 21	0xF0	RW	Bit[7:0]: Blue limit
0x5196	AWB CONTROL 22	0x03	RW	Bit[7:6]: Reserved Bit[5]: AWB freeze Bit[4]: Reserved Bit[3:2]: AWB simple selection 00: AWB simple from after AWB gain 01: AWB simple from after GMA 10: AWB simple from after GMA 11: AWB simple from after AWB gain Bit[1]: Fast enable Bit[0]: AWB bias stat
0x5197	AWB CONTROL 23	0x02	RW	Bit[7:0]: Local limit
0x5198~ 0x519D	RSVD	–	–	Reserved
0x519E	AWB CONTROL 30	0x30	RW	Bit[7:4]: Reserved Bit[3]: Local limit select Bit[2]: Simple stable select Bit[1:0]: Reserved

table 7-21 AWB registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x519F~ 0x51D0	AWB G SUM	–	R	AWB Debug Information

7.22 CIP control [0x5300 - 0x530F]

table 7-22 CIP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5300	CIP SHARPENMT THRESHOLD 1	0x08	RW	Color Interpolation Sharpen MT Threshold 1
0x5301	CIP SHARPENMT THRESHOLD 2	0x48	RW	Color Interpolation Sharpen MT Threshold 2
0x5302	CIP SHARPENMT OFFSET1	0x18	RW	CIP Sharpen MT Offset1 (Y edge mt manual setting when 0x5308[6]=1)
0x5303	CIP SHARPENMT OFFSET2	0x0E	RW	CIP Sharpen MT Offset2
0x5304	CIP DNS THRESHOLD 1	0x08	RW	CIP DNS Threshold 1
0x5305	CIP DNS THRESHOLD 2	0x48	RW	CIP DNS Threshold 2
0x5306	CIP DNS OFFSET1	0x09	RW	CIP DNS Offset1 (DNS threshold manual setting when 0x5308[4]=1)
0x5307	CIP DNS OFFSET2	0x16	RW	CIP DNS Offset2
0x5308	CIP CTRL	0x25	RW	Bit[7]: Not used Bit[6]: CIP edge MT manual enable Bit[4]: CIP DNS manual enable Bit[3]: Not used Bit[2:0]: CIP threshold for BR sharpen
0x5309	CIP SHARPENTH THRESHOLD 1	0x08	RW	CIP Sharpen TH Threshold 1
0x530A	CIP SHARPENTH THRESHOLD 2	0x48	RW	CIP Sharpen TH Threshold 2
0x530B	CIP SHARPENTH OFFSET1	0x04	RW	CIP Sharpen TH Offset1 (Sharpen threshold manual setting when 0x5308[6]=1)
0x530C	CIP SHARPENTH OFFSET2	0x06	RW	CIP Sharpen TH Offset2
0x530D	CIP EDGE MT AUTO	–	R	CIP Edge MT Auto Read

table 7-22 CIP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x530E	CIP DNS THRESHOLD AUTO	–	R	CIP DNS Threshold Auto Read
0x530F	CIP SHARPEN THRESHOLD AUTO	–	R	CIP Sharpen Threshold Auto Read

7.23 CMX control [0x5380 - 0x538B]

table 7-23 CMX control registers

address	register name	default value	R/W	description
0x5380	CMX0	0x00	RW	Bit[7:1]: Reserved Bit[0]: gb_cbcr
0x5381	CMX1	0x20	RW	Bit[7:0]: CMX1
0x5382	CMX2	0x64	RW	Bit[7:0]: CMX2
0x5383	CMX3	0x08	RW	Bit[7:0]: CMX3
0x5384	CMX4	0x30	RW	Bit[7:0]: CMX4
0x5385	CMX5	0x90	RW	Bit[7:0]: CMX5
0x5386	CMX6	0xC0	RW	Bit[7:0]: CMX6
0x5387	CMX7	0xA0	RW	Bit[7:0]: CMX7
0x5388	CMX8	0x98	RW	Bit[7:0]: CMX8
0x5389	CMX9	0x08	RW	Bit[7:0]: CMX9
0x538A	CMXSIGN	0x01	RW	Cmxsign Bit[7:1]: Reserved Bit[0]: CMX9 sign
0x538B	CMXSIGN	0x98	RW	Cmxsign Bit[7]: CMX8 sign Bit[6]: CMX7 sign Bit[5]: CMX6 sign Bit[4]: CMX5 sign Bit[3]: CMX4 sign Bit[2]: CMX3 sign Bit[1]: CMX2 sign Bit[0]: CMX1 sign

7.24 gamma control [0x5480 - 0x5490]

table 7-24 gamma control registers

address	register name	default value	R/W	description
0x5480	GAMMA CONTROL00	0x01	RW	Bit[7:2]: Reserved Bit[1]: YSLP15 manual enable Bit[0]: BIAS plus on
0x5481	GAMMA YST00	0x26	RW	Bit[7:0]: Y yst1
0x5482	GAMMA YST01	0x35	RW	Bit[7:0]: Y yst2
0x5483	GAMMA YST02	0x48	RW	Bit[7:0]: Y yst3
0x5484	GAMMA YST03	0x63	RW	Bit[7:0]: Y yst4
0x5485	GAMMA YST04	0x6E	RW	Bit[7:0]: Y yst5
0x5486	GAMMA YST05	0x77	RW	Bit[7:0]: Y yst6
0x5487	GAMMA YST06	0x80	RW	Bit[7:0]: Y yst7
0x5488	GAMMA YST07	0x88	RW	Bit[7:0]: Y yst8
0x5489	GAMMA YST08	0x8F	RW	Bit[7:0]: Y yst9
0x548A	GAMMA YST09	0x96	RW	Bit[7:0]: Y yst10
0x548B	GAMMA YST0A	0xA3	RW	Bit[7:0]: Y yst11
0x548C	GAMMA YST0B	0xAF	RW	Bit[7:0]: Y yst12
0x548D	GAMMA YST0C	0xC5	RW	Bit[7:0]: Y yst13
0x548E	GAMMA YST0D	0xD7	RW	Bit[7:0]: Y yst14
0x548F	GAMMA YST0E	0xE8	RW	Bit[7:0]: Y yst15
0x5490	GAMMA YSLP15	0x0F	RW	Bit[7:0]: Y yslp15 Slope of yst15

7.25 SDE control [0x5580 - 0x558C]

table 7-25 SDE control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580	SDE CTRL0	0x00	RW	Bit[7]: Fixed Y enable 0: Disable 1: Enable Bit[6]: Negative enable 0: Disable 1: Enable Bit[5]: Gray enable 0: Disable 1: Enable Bit[4]: Fixed V enable 0: Disable 1: Enable Bit[3]: Fixed U enable 0: Disable 1: Enable Bit[2]: Contrast enable 0: Disable 1: Enable Bit[1]: Saturation enable 0: Disable 1: Enable Bit[0]: Hue enable 0: Disable 1: Enable
0x5581	SDE CTRL1	0x80	RW	Bit[7:0]: Hue cos coefficient
0x5582	SDE CTRL2	0x00	RW	Bit[7:0]: Hue sin coefficient
0x5583	SDE CTRL3	0x40	RW	Bit[7:0]: Saturation U when 0x5580[1]=1 and 0x5588[6]=1, max value for auto color saturation adjust when 0x5580[1]=1 and 0x5588[6]=0; or fixed U when 0x5580[3]=1
0x5584	SDE CTRL4	0x00	RW	Bit[7:0]: Saturation V when 0x5580[1]=1 and 0x5588[6]=1, min value for auto color saturation adjust when 0x5580[1]=1 and 0x5588[6]=0; or Vreg when 0x5580[4]=1
0x5585	SDE CTRL5	0x00	RW	Bit[7:0]: Y offset for contrast when 0x5044[3]=1; or fixed Y when 0x5580[7]=1
0x5586	SDE CTRL6	0x20	RW	Bit[7:0]: Y gain for contrast
0x5587	SDE CTRL7	0x00	RW	Bit[7:0]: Y bright for contrast

table 7-25 SDE control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5588	SDE CTRL8	0x00	RW	Bit[7]: Reserved Bit[6]: Auto color saturation adjust manual enable Bit[5]: Sign5 for hue V, cos Bit[4]: Sign4 for hue U, cos Bit[3]: Sign3 Y bright sign for contrast 0: Keep Y bright sign 1: Negative Y bright sign Bit[2]: Sign2 Y offset sign for contrast when 0x5044[3]=1 0: Keep Y offset sign 1: Negative Y offset sign Bit[1]: Sign1 for hue V, sin Bit[0]: Sign0 for hue U, sin
0x5589	SDE CTRL9	0x08	RW	Bit[7:0]: Auto color saturation adjust threshold 1 Valid when 0x5580[1]=1
0x558A	SDE CTRL10	0x80	RW	Bit[7:1]: Reserved Bit[0]: Auto color saturation adjust threshold 2[8] Valid when 0x5580[1]=1
0x558B	SDE CTRL11	0x00	RW	Bit[7:0]: Auto color saturation adjust threshold 2[7:0] Valid when 0x5580[1]=1
0x558C	SDE CTRL12	–	R	Bit[7:0]: Auto color saturation adjust value read out

7.26 scale control [0x5600 - 0x5606]

table 7-26 scale control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	SCALE CTRL 0	0x10	RW	Bit[7]: Reserved Bit[6]: V first YUV444 to 422 output U or V first 0: U first 1: V first Bit[5]: UV drop YUV444 to 422 drop mode versus AVG mode selection 0: AVG mode 1: Drop mode Bit[4]: Auto mode Scale auto mode versus manual mode selection 0: Manual mode 1: Auto mode Bit[3]: Horizontal round DCW horizontal rounding 0: No horizontal rounding 1: Horizontal rounding Bit[2]: Horizontal drop DCW horizontal drop mode 0: Horizontal average mode 1: Horizontal drop mode Bit[1]: Vertical round DCW vertical rounding 0: No vertical rounding 1: Vertical rounding Bit[0]: Vertical drop DCW vertical drop mode 0: Vertical average mode 1: Vertical drop mode
0x5601	SCALE CTRL 1	0x00	RW	Bit[7]: Reserved Bit[6:4]: Horizontal div DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 011: DCW 8 time 1xx: DCW 16 time Bit[2:0]: Vertical div DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 011: DCW 8 time 1xx: DCW 16 time

table 7-26 scale control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5602	SCALE CTRL 2	0x02	RW	Bit[7:0]: XSC[15:8]
0x5603	SCALE CTRL 3	0x00	RW	Bit[7:0]: XSC[7:0]
0x5604	SCALE CTRL 4	0x02	RW	Bit[7:0]: YSC[15:8]
0x5605	SCALE CTRL 5	0x00	RW	Bit[7:0]: YSC[7:0]
0x5606	SCALE CTRL 6	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Vertical offset

7.27 average control [0x5680 - 0x56A2]

table 7-27 AVG registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5680	X START	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: X start[11:8] Horizontal start position for average window high byte, valid when 0x501D[4]=1
0x5681	X START	0x00	RW	Bit[7:0]: X start[7:0] Horizontal start position for average window low byte, valid when 0x501D[4]=1
0x5682	Y START	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Y start[10:8] Vertical start position for average window high byte, valid when 0x501D[4]=1
0x5683	Y START	0x00	RW	Bit[7:0]: Y start[7:0] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5684	X WINDOW	0x10	RW	Bit[7:4]: Reserved Bit[3:0]: Window X[11:8] Horizontal end position for average window high byte, valid when 0x501D[4]=1
0x5685	X WINDOW	0xA0	RW	Bit[7:0]: Window X[7:0] Horizontal end position for average window low byte, valid when 0x501D[4]=1
0x5686	Y WINDOW	0x0C	RW	Bit[7:3]: Reserved Bit[2:0]: Window Y[10:8] Vertical end position for average window high byte, valid when 0x501D[4]=1

table 7-27 AVG registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5687	Y WINDOW	0x78	RW	Bit[7:0]: Window Y[7:0] Vertical end position for average window low byte, valid when 0x501D[4]=1
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: Window 01 weight Bit[3:0]: Window 00 weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: Window 03 weight Bit[3:0]: Window 02 weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: Window 11 weight Bit[3:0]: Window 10 weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: Window 13 weight Bit[3:0]: Window 12 weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: Window 21 weight Bit[3:0]: Window 20 weight
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: Window 23 weight Bit[3:0]: Window 22 weight
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: Window 31 weight Bit[3:0]: Window 30 weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: Window 33 weight Bit[3:0]: Window 32 weight
0x5690	AVG CTRL10	0x01	RW	Bit[7:1]: Reserved Bit[0]: AVG option 0: Sum=(4*B+9*G*2+10*R)/8 1: Sum=(B+G*2+R)/4
0x5691	AVG WIN 00	–	R	Bit[7:0]: Average of win 00
0x5692	AVG WIN 01	–	R	Bit[7:0]: Average of win 01
0x5693	AVG WIN 02	–	R	Bit[7:0]: Average of win 02
0x5694	AVG WIN 03	–	R	Bit[7:0]: Average of win 03
0x5695	AVG WIN 10	–	R	Bit[7:0]: Average of win 10
0x5696	AVG WIN 11	–	R	Bit[7:0]: Average of win 11
0x5697	AVG WIN 12	–	R	Bit[7:0]: Average of win 12
0x5698	AVG WIN 13	–	R	Bit[7:0]: Average of win 13
0x5699	AVG WIN 20	–	R	Bit[7:0]: Average of win 20
0x569A	AVG WIN 21	–	R	Bit[7:0]: Average of win 21
0x569B	AVG WIN 22	–	R	Bit[7:0]: Average of win 22
0x569C	AVG WIN 23	–	R	Bit[7:0]: Average of win 23

table 7-27 AVG registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x569D	AVG WIN 30	–	R	Bit[7:0]: Average of win 30
0x569E	AVG WIN 31	–	R	Bit[7:0]: Average of win 31
0x569F	AVG WIN 32	–	R	Bit[7:0]: Average of win 32
0x56A0	AVG WIN 33	–	R	Bit[7:0]: Average of win 33
0x56A1	AVG READOUT	–	R	Bit[7:0]: Average value output
0x56A2	AVG WEIGHT SUM	–	R	Bit[7:0]: Average weight sum

7.28 DPC control [0x5780 - 0x5794]

table 7-28 DPC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5780	DPC CTRL00	0x14	RW	DPC Control Register
0x5781	DPC CTRL01	0x0F	RW	DPC Control Register
0x5782	DPC CTRL02	0x04	RW	DPC Control Register
0x5783	DPC CTRL03	0x02	RW	DPC Control Register
0x5784	DPC CTRL04	0x01	RW	DPC Control Register
0x5785	DPC CTRL05	0x01	RW	DPC Control Register
0x5786	DPC CTRL06	0x00	RW	DPC Control Register
0x5787	DPC CTRL07	0x04	RW	DPC Control Register
0x5788	DPC CTRL08	0x0C	RW	DPC Control Register
0x5789	DPC CTRL09	0x00	RW	DPC Control Register
0x578A	DPC CTRL0A	0x01	RW	DPC Control Register
0x578B	DPC CTRL0B	0x02	RW	DPC Control Register
0x578C	DPC CTRL0C	0x03	RW	DPC Control Register
0x578D	DPC CTRL0D	0x03	RW	DPC Control Register
0x578E	DPC CTRL0E	0x0F	RW	DPC Control Register
0x578F	DPC CTRL0F	0x3F	RW	DPC Control Register
0x5790	DPC CTRL10	0x08	RW	DPC Control Register

table 7-28 DPC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5791	DPC CTRL11	0x04	RW	DPC Control Register
0x5792	DPC CTRL12	0x04	RW	DPC Control Register
0x5793	DPC CTRL13	0x00	RW	DPC Control Register
0x5794	DPC CTRL14	0x03	RW	DPC Control Register

7.29 LENC control [0x5800 - 0x5849]

table 7-29 LENC control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5800	GMTRX00	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 00
0x5801	GMTRX01	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 01
0x5802	GMTRX02	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 02
0x5803	GMTRX03	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 03
0x5804	GMTRX04	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 04
0x5805	GMTRX05	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 05
0x5806	GMTRX10	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 06
0x5807	GMTRX11	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 07
0x5808	GMTRX12	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 08
0x5809	GMTRX13	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 09
0x580A	GMTRX14	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0A
0x580B	GMTRX15	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0B

table 7-29 LENC control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x580C	GMTRX20	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0C
0x580D	GMTRX21	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0D
0x580E	GMTRX22	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0E
0x580F	GMTRX23	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 0F
0x5810	GMTRX24	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 10
0x5811	GMTRX25	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Green matrix 11
0x5812	GMTRX30	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 12
0x5813	GMTRX31	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 13
0x5814	GMTRX32	0x00	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 14
0x5815	GMTRX33	0x00	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 15
0x5816	GMTRX34	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 16
0x5817	GMTRX35	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 17
0x5818	GMTRX40	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 18
0x5819	GMTRX41	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 19
0x581A	GMTRX42	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1A
0x581B	GMTRX43	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1B
0x581C	GMTRX44	0x08	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1C
0x581D	GMTRX45	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1D
0x581E	GMTRX50	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1E

table 7-29 LENC control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x581F	GMTRX51	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 1F
0x5820	GMTRX52	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 20
0x5821	GMTRX53	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 21
0x5822	GMTRX54	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 22
0x5823	GMTRX55	0x10	R/W	Bit[7:6]: Reserved Bit[5:0]: Green matrix 23
0x5824	BRMATRX00	0xAA	R/W	Bit[7:4]: Blue matrix 00 Bit[3:0]: Red matrix 00
0x5825	BRMATRX01	0xAA	RW	Bit[7:4]: Blue matrix 01 Bit[3:0]: Red matrix 01
0x5826	BRMATRX02	0xAA	RW	Bit[7:4]: Blue matrix 02 Bit[3:0]: Red matrix 02
0x5827	BRMATRX03	0xAA	RW	Bit[7:4]: Blue matrix 03 Bit[3:0]: Red matrix 03
0x5828	BRMATRX04	0xAA	RW	Bit[7:4]: Blue matrix 04 Bit[3:0]: Red matrix 04
0x5829	BRMATRX05	0xAA	RW	Bit[7:4]: Blue matrix 05 Bit[3:0]: Red matrix 05
0x582A	BRMATRX06	0x99	RW	Bit[7:4]: Blue matrix 06 Bit[3:0]: Red matrix 06
0x582B	BRMATRX07	0x99	RW	Bit[7:4]: Blue matrix 07 Bit[3:0]: Red matrix 07
0x582C	BRMATRX08	0x99	RW	Bit[7:4]: Blue matrix 08 Bit[3:0]: Red matrix 08
0x582D	BRMATRX09	0xAA	RW	Bit[7:4]: Blue matrix 09 Bit[3:0]: Red matrix 09
0x582E	BRMATRX20	0xAA	RW	Bit[7:4]: Blue matrix 20 Bit[3:0]: Red matrix 20
0x582F	BRMATRX21	0x99	RW	Bit[7:4]: Blue matrix 21 Bit[3:0]: Red matrix 21
0x5830	BRMATRX22	0x88	RW	Bit[7:4]: Blue matrix 22 Bit[3:0]: Red matrix 22
0x5831	BRMATRX23	0x99	RW	Bit[7:4]: Blue matrix 23 Bit[3:0]: Red matrix 23

table 7-29 LENC control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5832	BRMATRX24	0xAA	RW	Bit[7:4]: Blue matrix 24 Bit[3:0]: Red matrix 24
0x5833	BRMATRX30	0xAA	RW	Bit[7:4]: Blue matrix 30 Bit[3:0]: Red matrix 30
0x5834	BRMATRX31	0x99	RW	Bit[7:4]: Blue matrix 31 Bit[3:0]: Red matrix 31
0x5835	BRMATRX32	0x99	RW	Bit[7:4]: Blue matrix 32 Bit[3:0]: Red matrix 32
0x5836	BRMATRX33	0x99	RW	Bit[7:4]: Blue matrix 33 Bit[3:0]: Red matrix 33
0x5837	BRMATRX34	0xAA	RW	Bit[7:4]: Blue matrix 34 Bit[3:0]: Red matrix 34
0x5838	BRMATRX40	0xAA	R/W	Bit[7:4]: Blue matrix 40 Bit[3:0]: Red matrix 40
0x5839	BRMATRX41	0xAA	R/W	Bit[7:4]: Blue matrix 41 Bit[3:0]: Red matrix 41
0x583A	BRMATRX42	0xAA	R/W	Bit[7:4]: Blue matrix 42 Bit[3:0]: Red matrix 42
0x583B	BRMATRX43	0xAA	R/W	Bit[7:4]: Blue matrix 43 Bit[3:0]: Red matrix 43
0x583C	BRMATRX44	0xAA	R/W	Bit[7:4]: Blue matrix 44 Bit[3:0]: Red matrix 44
0x583D	LENC BR OFFSET	0x88	R/W	Bit[7:4]: LENC b offset Bit[3:0]: LENC r offset
0x583E	MAX GAIN	0x40	R/W	Bit[7:0]: Maximum gain
0x583F	MIN GAIN	0x20	R/W	Bit[7:0]: Minimum gain
0x5840	MIN Q	0x18	R/W	Bit[7]: Reserved Bit[6:0]: Minimum Q
0x5841	LENC CTRL59	0x0D	R/W	Bit[7:4]: Reserved Bit[3]: Add BLC enable 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: BLC enable 0: Disable BLC function 1: Enable BLC function Bit[1]: Reserved Bit[0]: Auto Q enable 0: Used constant Q (0x40) 1: Used calculated Q

table 7-29 LENC control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5842	BR HSCALE	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: BR H scale[10:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5843	BR HSCAL	0xBD	RW	Bit[7:0]: BR H scale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5844	BR VSCALE	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: BR V scale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5845	BR VSCALE	0xFE	RW	Bit[7:0]: BR V scale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: G H scale[10:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCAL	0xFC	RW	Bit[7:0]: G H scale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: G V scale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

table 7-29 LENC control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5849	G VSCALE	0xA9	RW	Bit[7:0]: G V scale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

7.30 temperature sensor control [0x6700 - 0x6721]

table 7-30 TPM control registers

address	register name	default value	R/W	description
0x6700~ 0x6705	TPM CTRL00~05	–	–	Temperature Sensor Control Registers
0x6706	TPM CTRL06	0x78	RW	Bit[7:4]: Reserved Bit[3:0]: Sample clock must be around 3MHz If the user has 24 MHz XVCLK, sample clock = XVCLK/clock divisor => 3MHz = 24MHz / 8 (these 4 bits must be 4'b1000) If the user has 12 MHz XVCLK, sample clock = XVCLK/clock divisor => 3MHz = 12MHz / 4 (these 4 bits must be 4'b0100)
0x6707~ 0x6718	TPM CTRL09~18	–	–	Temperature Sensor Control Registers
0x6719	TPM CTRL19	–	R	Bit[7:0]: Measured temperature
0x671A~ 0x6721	TPM CTRL1A~21	–	–	Temperature Sensor Control Registers

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)[b]	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. for negative voltage with respect to ground, V_{DD-A} (-4.5V), V_{DD-C} (-3V), V_{DD-IO} (-4.5V)

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-20°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-20°C < T_A < 70°C) (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
power supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
internal DVDD, DOVDD=1.8V					
I_{DD-A}	active (operating) current		28		mA
I_{DD-IO}[b, c]			70		mA
$I_{DDS-SCCB}$[d]	standby current		20		µA
$I_{DDS-PWDN}$[d]			20		µA
P_O	active (operating) power consumption			TBD	mW
$P_{DDS-SCCB}$	standby power consumption			TBD	µW
$P_{DDS-PWDN}$				TBD	µW
external DVDD, DOVDD=2.8V					
I_{DD-A}	active (operating) current		28		mA
I_{DD-D}[b, c]			64		mA
I_{DD-IO}			6		mA
$I_{DDS-SCCB}$	standby current		40		µA
$I_{DDS-PWDN}$			40		µA
P_O	active (operating) power consumption			TBD	mW
$P_{DDS-SCCB}$	standby power consumption			TBD	µW
$P_{DDS-PWDN}$				TBD	µW
external DVDD, DOVDD=1.8V					
I_{DD-A}	active (operating) current		28		mA
I_{DD-D}[b, c]			64		mA
I_{DD-IO}			4		mA
$I_{DDS-SCCB}$	standby current		40		µA
$I_{DDS-PWDN}$			40		µA
P_O	active (operating) power consumption			TBD	mW
$P_{DDS-SCCB}$	standby power consumption			TBD	µW
$P_{DDS-PWDN}$				TBD	µW

table 8-3 DC characteristics (-20°C < T_A < 70°C) (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs[e]					
V_{IL}	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.26	1.8	3.0	V

a. using the internal DVDD regulator is strongly recommended for minimum power down current

b. active current is based on sensor resolution at full size and at full speed in compression format. For smaller sizes such as 720p or below preview, the total active current will be about half.

c. DOVDD active current is based on loading of 10pF and typical compression format output PCLK (48MHz). For YUV output with higher PCLK, or higher loading, DOVDD current can go up.

d. at room temperature and typical supply voltages

e. based on DOVDD = 1.8V.

8.4 timing characteristics

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	54	MHz
t_r, t_f	clock input rise/fall time[b]			5 (10[c])	ns
f_{PCLK}	parallel port output pixel clock		54	108	MHz

a. for input clock range 6~27MHz, the OV3660 can tolerate input clock jitter up to 1ns, for input clock range to 54MHz, the OV3660 can tolerate input clock jitter up to 500ps

b. if the PLL is bypassed, the delay from input clock to output clock is approximately 4~5ns

c. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

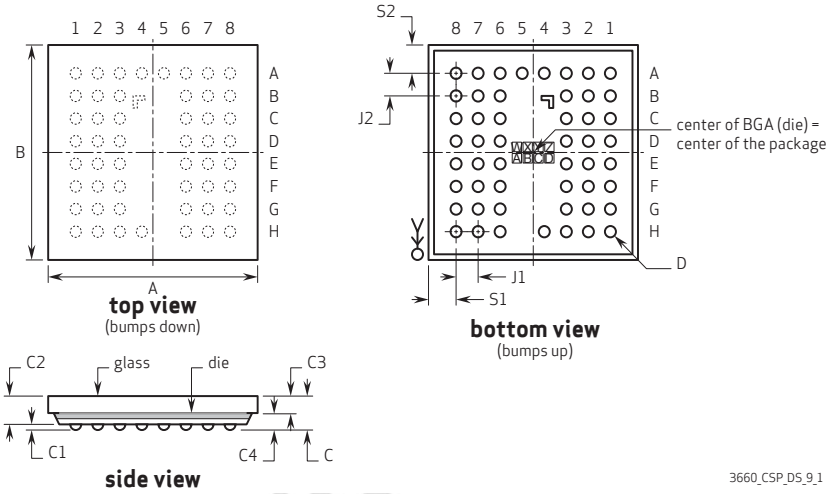


table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	4985	5010	5035	µm
package body dimension y	B	4935	4960	4985	µm
package height	C	690	750	810	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	620	665	µm
cover glass thickness	C3	425	445	465	µm
ball diameter	D	220	250	280	µm
total pin count	N		51 (7 NC)		
pin count x-axis	N1		8		
pin count y-axis	N2		8		
pins pitch x-axis	J1		580		µm
pins pitch y-axis	J2		600		µm
edge-to-pin center distance along x	S1	445	475	505	µm
edge-to-pin center distance along y	S2	350	380	410	µm

9.2 IR reflow specifications

note
The OV3660 uses a lead-free package.

figure 9-2 IR reflow ramp rate requirements

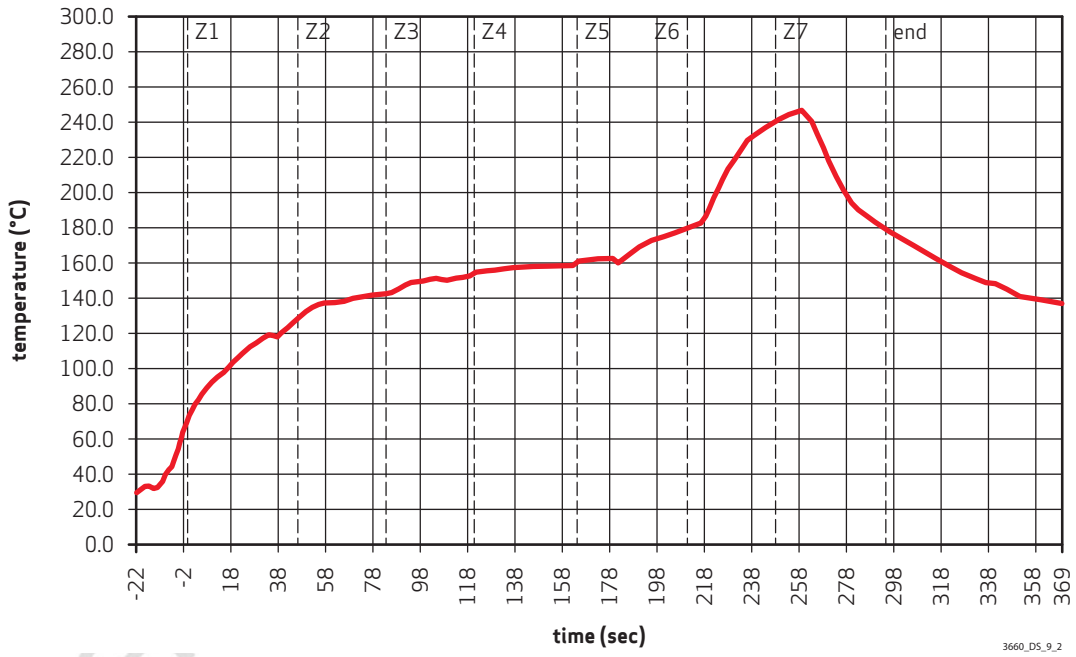


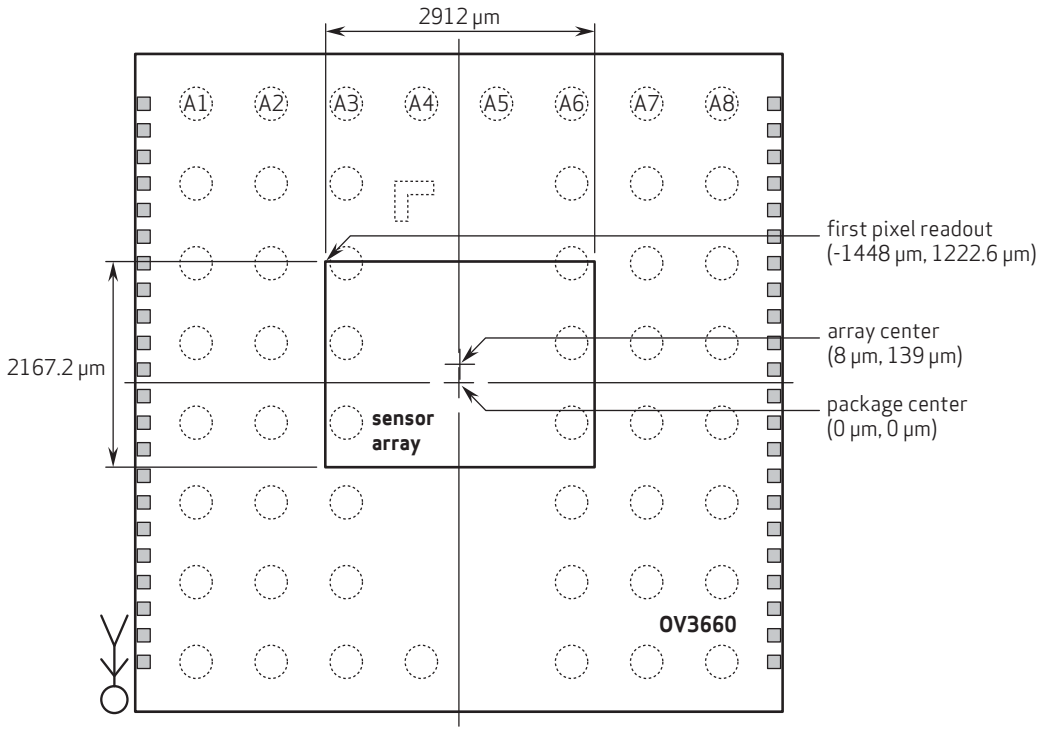
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 to A8 oriented down on the PCB.

3660_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

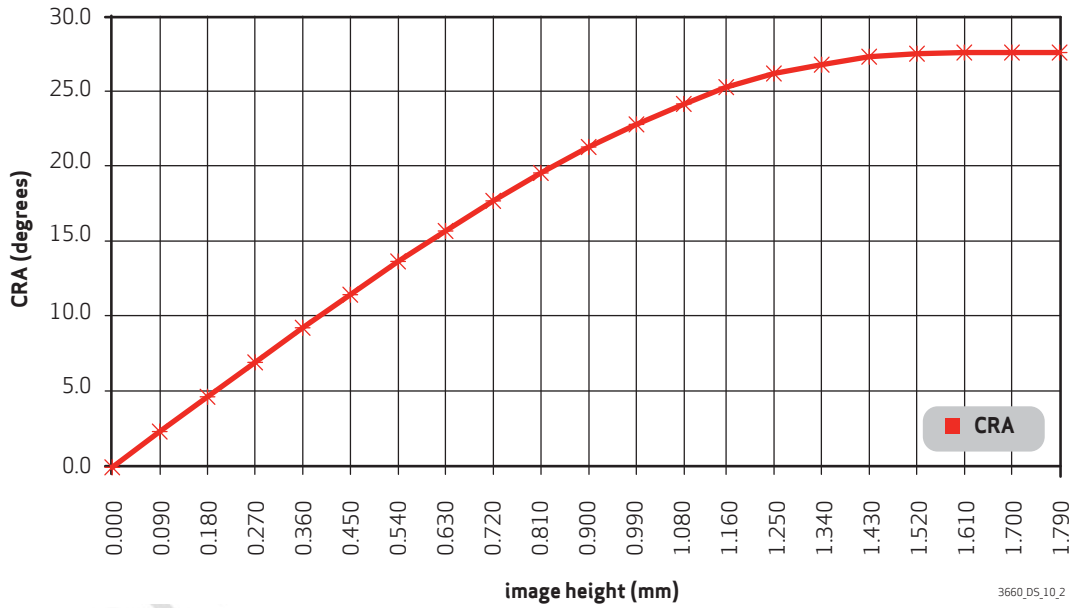


table 10-1 CRA versus image height plot (sheet 1 of 2)

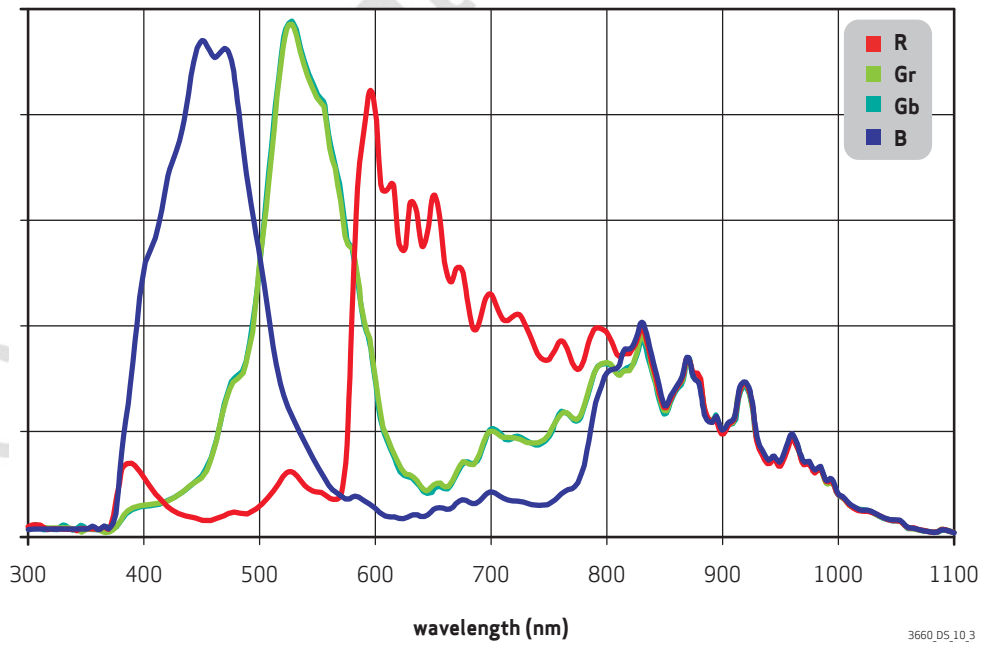
field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.090	2.4
0.1	0.180	4.7
0.15	0.270	7.0
0.2	0.360	9.3
0.25	0.450	11.5
0.3	0.540	13.7
0.35	0.630	15.7
0.4	0.720	17.7
0.45	0.810	19.6
0.5	0.900	21.3
0.55	0.990	22.8

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.6	1.080	24.2
0.65	1.160	25.3
0.7	1.250	26.2
0.75	1.340	26.8
0.8	1.430	27.3
0.85	1.520	27.5
0.9	1.610	27.6
0.95	1.700	27.6
1	1.790	27.6

10.3 spectrum response

figure 10-3 spectrum response graph



revision history

version 1.0 09.23.2010

- initial release

version 1.1 12.16.2010

- on page iii, under key specifications, added "junction temperature" to temperature range and removed well capacity
- on page iii, under key specifications, changed image area from "2080 µm x 1548 µm" to "2912 µm x 2167.2 µm"
- in section 3, updated figure 3-1
- in table 8-2, added "junction temperature" to range
- in section 10, updated figure 10-1

version 1.2 01.31.2011

- in features section on page i, removed "support for video or snapshot operations", "support for internal and external frame synchronization for frame exposure mode", and "support for minimizing artifacts on binned image"
- in features section on page i, added "support 2x2 binning with binning filter to remove binning artifacts"
- in key specifications section on page i, added "(1.8V recommended)" to I/O power supply specification
- in key specifications section on page i, removed "/ frame exposure" from shutter specification
- moved section 3, pixel array structure to section 2.3
- moved section 2.3, format and frame rate to section 2.7
- moved section 2.4, I/O control to section 2.8
- moved section 2.5, system clock control to section 2.9
- moved section 2.6, SCCB interface to chapter 6 and added subsections for data transfer protocol, message format, read/write operation, and SCCB timing
- moved table 2-6, group write registers to new section 2.10, group write
- changed chapter 4, image sensor core digital functions (with all subsections) to chapter 3
- in new chapter 3, added section 3.2.2, scaling
- in new chapter 3, renamed AEC/AGC algorithms section to section 3.4, exposure/gain control and completely re-wrote the section
- removed AEC/AGC steps section (previously section 4.5)
- moved section 4.6, black level calibration to section 3.5
- removed light frequency selection (previously section 4.7) and merged content into new section 3.4
- removed digital gain (previously section 4.8) and merged content into new section 3.4
- moved section 4.9, strobe flash to section 3.6

- moved section 4.10, one time programmable (OTP) memory to section 3.7 and completely re-wrote the section
- moved section 4.11, temperature sensor to section 3.8 and completely re-wrote the section
- changed chapter 5, image sensor processor digital functions (with all subsections) to chapter 4
- moved section 5.6 to section 4.6, renamed section to "color interpolation (CIP) and sharpening", and re-wrote first paragraph
- removed (previously numbered) section 5.8, UV average and (previously numbered) section 5.9, scaling
- moved section 5.10, UV adjust to section 4.8 and renamed section to "auto color saturation adjust"
- moved section 5.11, special digital effects (SDE) to section 4.9
- removed (previously numbered) section 5.12, ISP format and (previously numbered) section 5.13, average
- changed chapter 6, image sensor output interface digital functions (with all subsections) to chapter 5
- removed (previously numbered) section 6.2, system control and (previously numbered) section 6.3, format description
- in chapter 7, added subsection number and title for each register table
- renamed section 8.4 from "AC characteristics" to "timing characteristics" and removed AC characteristics table and SCCB timing figure and table
- in chapter 10, added section 10.3, spectrum response

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