FEATURES

- Easy upgrade to new standards
- Buffered output drivers to antenna
- Advanced integrated demodulator and decoder
- Integrated RF level detector
- Small 59-ball TFBGA (4.5mm x 4.5mm x 1.2mm) package

■ HF RFID Reader
- Supports ISO 15693
- Supports ISO 18000-3, mode 1
- Supports ISO 14443A
- Supports ISO 14443B

■ Near Field Communication
- NFCIP-1, NFCIP-2
- ISO 18092 compliant
- Peer to Peer communication
- Bit rate from 106k up to 1.6Mbps

■ Card Emulation Mode
- Supports power by the RF field when cell phone power is off
- Supports ISO14443A
- Supports ISO14443B
- Supports ISO15693

■ Built-in 8051 Microcontroller
- 32KB Program SRAM
- 32KB Program ROM
- 8KB RAM
- Integrated 128KB non-volatile memory to store data and executable code for customization

■ Security Engine
- True random number generator
- Unique serial number on each die
- DES/3DES accelerator
- AES accelerator

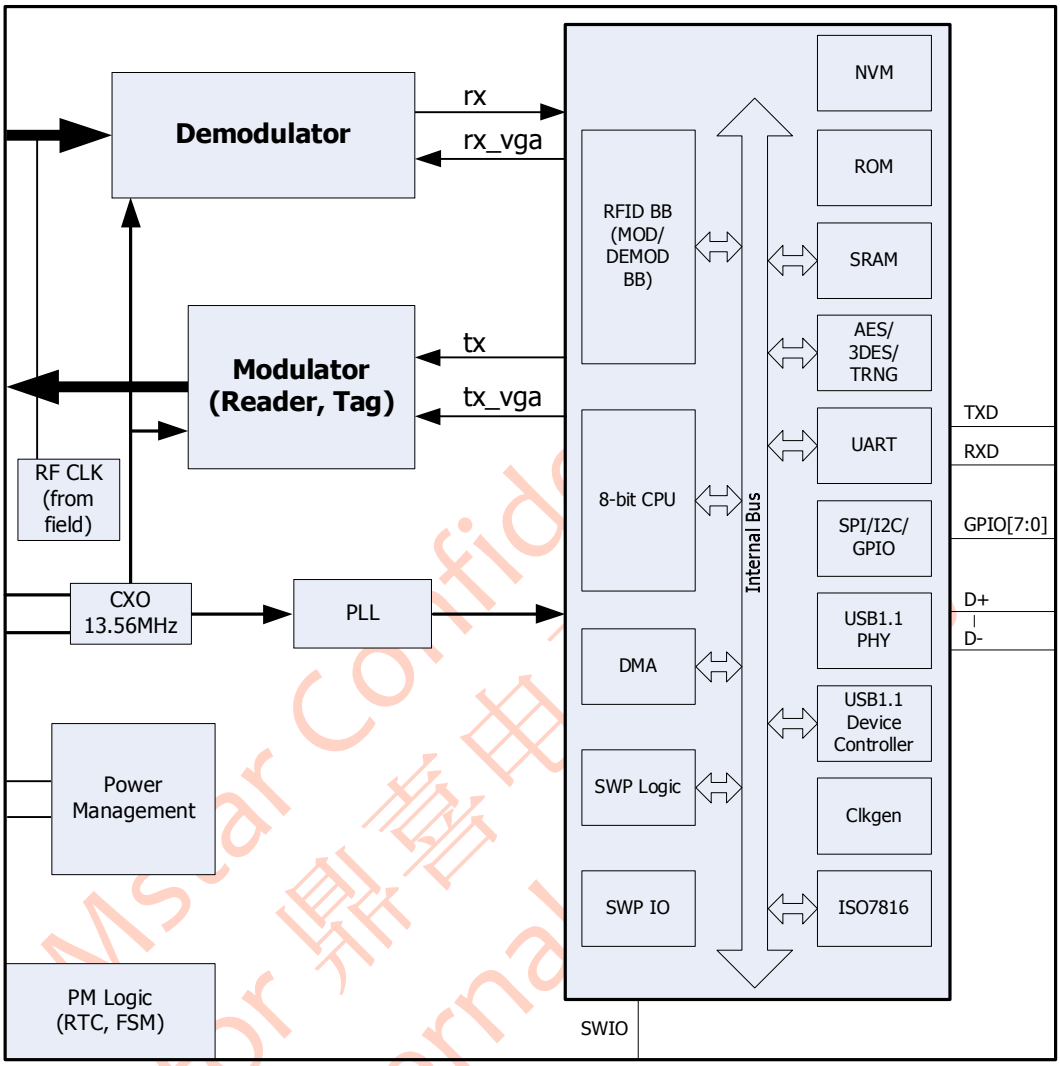
■ Host Interface
- USB1.1
- I^2C
- SPI
- UART

■ Single Wire Protocol (SWP) Interface
- Fully compliant with ETSI TS 102 613 Release 7
- Supports ETSI TS 102 622 Release 7 HCI protocol

■ ISO7816 Master Interface
- Supports T=0 and T=1 protocols

■ Operation
- Frequency: 13.56 MHz ± 7 KHz
- Low power consumption
- Low standby current: <50 μA
- Hard power down current: <5μA

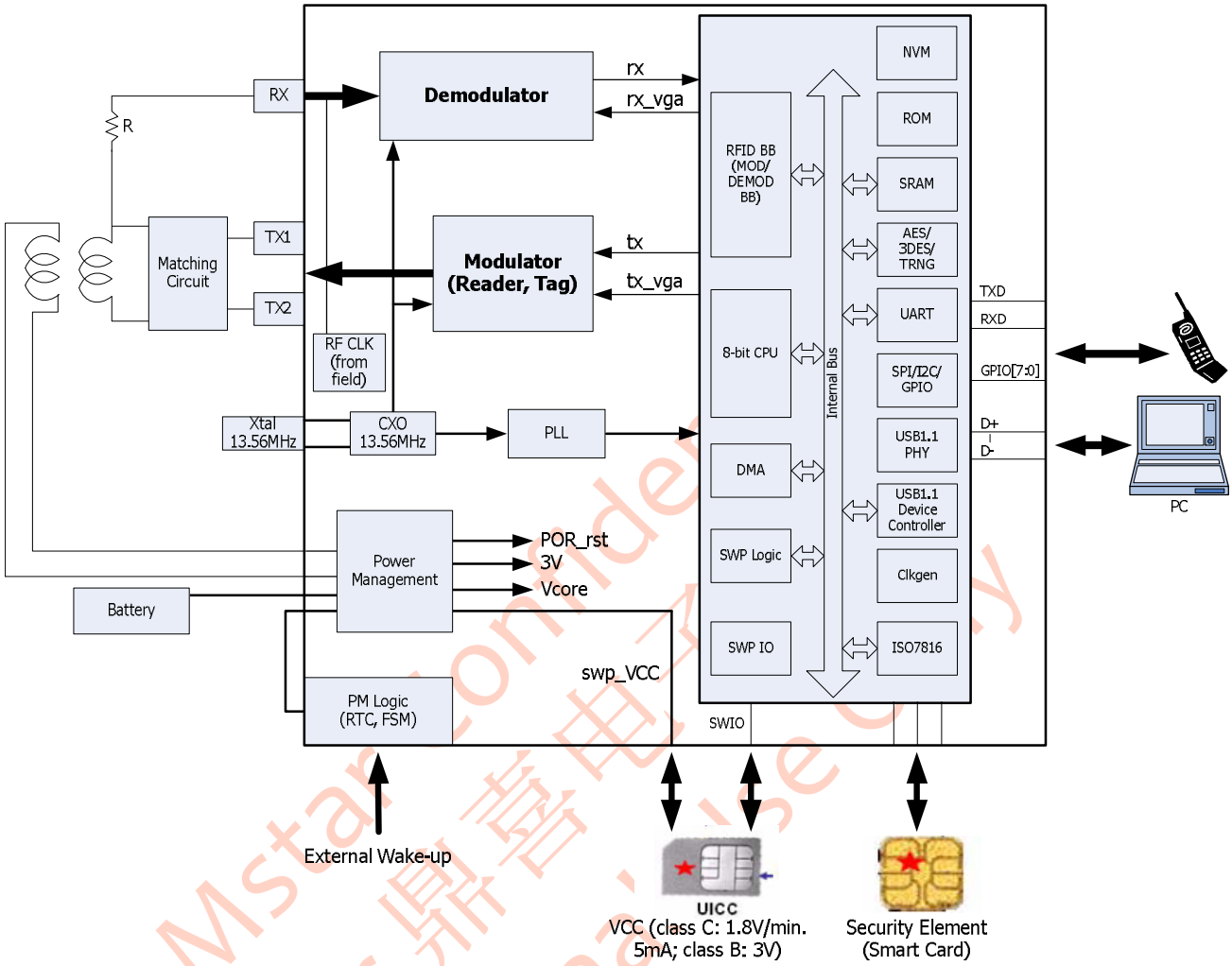
BLOCK DIAGRAM



The modulator and the demodulator are analog circuits. The CXO is a 13.56 MHz crystal oscillator which provides a reference for the internal PLL to generate the 60 MHz clock for the CPU and USB.

GPIO[7:0] can be configured as GPIOs, or used for special Interface such as UART, I^2C, and SPI to interface with different host or device. GPIO[6:4] are used as inputs to configure the BootLoader mode for the MSR3110, details of which being described in the Operation section.

SYSTEM APPLICATION DIAGRAM



GENERAL DESCRIPTION

The MSR3110 HF NFC is a leading chipset which supports 15693 and 14443A/B protocols and provides built-in NFC (Near Field Communication) functions. The HF reader integrates various host interfaces including UART, I²C, SPI and USB, making it very easy to connect to any host with such interface as PC, PDA, and mobile phone.

No additional crystal is needed when connecting the MSR3110 to Host using the USB, which is advantageous in that it saves both cost and space for use on space-limited devices such as mobile phones and PDAs.

The first function of the MSR3110 is the reader/writer; by connecting it to PC via USB or UART interface, users may send ID to PC after detecting tags. The LED shows the status of the reader, while the Buzzer indicates that there is a tag that had been read back.

The MSR3110 integrates an 8051 microprocessor and 32KB programming SRAM.

Moreover, the MSR3110 has built-in NFC function, capable of being used as a contactless communication tool for transferring data, pictures, maps or videos.

GENERAL REQUIREMENTS

The MSR3110 HF NFC is able to read/write multi-standard tags and provide 300 mW power at the inductive antenna. The ASIC general requirements and associated specifications for system implementations are summarized below.

Parameter	Min	Typ	Max	Unit	Condition
3.3V Supply Voltage	2.7	3.3	3.6	V	
Temperature	-40		85	°C	Operation
	-40		125		Storage
Operation Frequency		13.56		MHz	HF band
Transmitter Power		300		mW	On 25 Ohm load
Transmitter Modulation		10	100	%	ASK
Antenna Impedance		25		Ohm	
Receiver Channel		106		kHz	ASK 13.56MHz/128
Receiver Channel		212		kHz	ASK 13.56MHz/64
Receiver Channel		423.75		kHz	ASK 13.56MHz/32
Receiver Channel		847		kHz	ASK 13.56MHz/16
Receiver Channel		1.69		MHz	ASK 13.56MHz/8
Receiver Channel		484.75		kHz	ASK 13.56MHz/28
Receiver Channel	423.75	423.75	484.28	kHz	FSK
Receiver Channel		847		kHz	PSK 13.56MHz/16

FUNCTIONAL DESCRIPTION

The MSR3110 HF Reader is integrated with an 8051 microprocessor, which makes it very easy to implement the code for different standards and protocols. Users could develop codes using their proprietary protocol.

The receiver is implemented using the analog demodulator. This helps improve the detection distance.
The Transmitter uses a push-pull circuit, which boosts the driver capacity.

8051 Core

This 8051 core is for managing the data processes, including collecting data from the demodulator and sending data to external interface or taking instructions from PC through the interface.

Interface

The interfaces include:

- UART:
  This interface could be used for communication with PC or LCD display panel.
- I2C:
  This interface could be used for communication with host device.
- SPI:
  This interface is for communication with host device, or for external programming.
- USB:
  This interface could be used for data transaction between MSR3110 and host device.

When the UART, I^2C and SPI interfaces are not used, these pins could be configured as general I/O ports.

OPERATION

BootLoader Mode

The MSR3110 has internal 32KB ROM, 32KB SRAM, and SPI bus that allow CPU to run program in the following modes:

Mode	GPIO[6]	GPIO[5]	GPIO[4]	Description
SPI Flash	0	0	0	CPU runs the program connected to the SPI Flash
ROM	0	0	1	CPU runs in on-chip ROM BootLoader mode
ROM+Flash	0	1	0	CPU runs from internal 32KB ROM and 32KB Flash
ROM+SRAM	0	1	1	CPU runs from internal 32KB ROM and 32KB SRAM
SRAM	1	0	0	CPU runs from internal SRAM
SPI Flash high bank	1	0	1	CPU runs the program from SPI Flash high bank 0x10000

As a standalone reader/writer, the MSR3110 could run the program from the external SPI Flash.
When used as a device for connecting to a host like a PC, PDA, or mobile phone, the MSR3110 does not require external Flash for storing the program. The host could download the program to the SRAM in MSR3110 and run from the SRAM to thereby save cost and layout space.

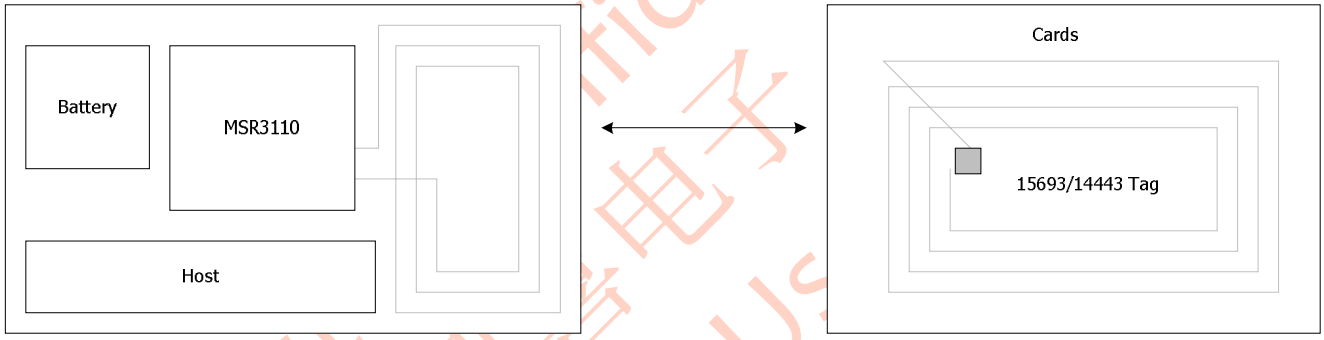
Operation Mode

After the bootloading, the CPU operates in accordance with the program design, in the following modes:

1. Reader/writer mode: Supports read/write ISO15693, 14443A/B tags.
2. Card emulation mode: Acts as an active or passive tag.
3. NFC mode: Data exchange between NFC devices, supporting bit rates of 106 kbit/s, 212 kbit/s, 424 kbit/s, 848 kbit/s and 1.6Mbit/s.
4. MStar proprietary protocol data exchange mode: Users could use the MSR3110 as a contactless device to exchange data, pictures, maps, etc. with higher efficiency and lower overhead.

Reader/Writer Mode

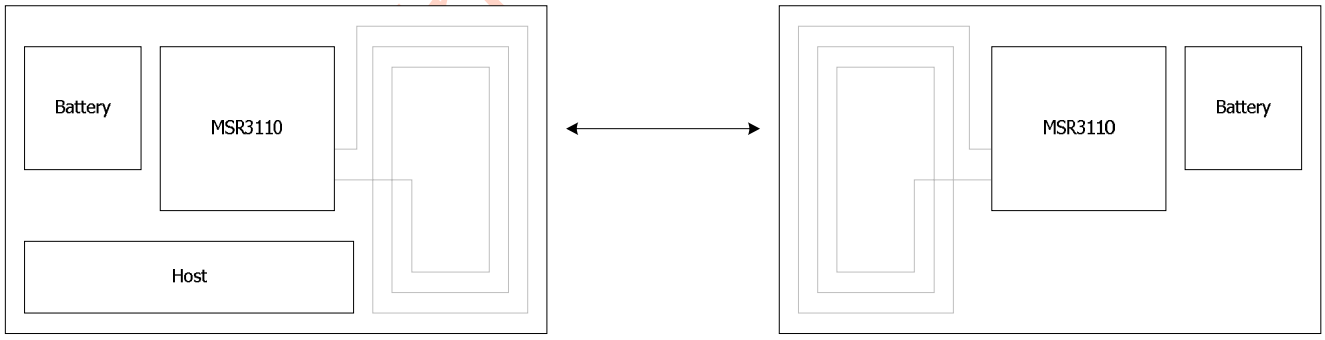
The MSR3110 communicates with cards with ISO15693, 14443A/B tags. Please refer to the following figure for the communication between the reader/writer and the card. The MSR3110 drives the inductive antenna and generates the magnet field coupled by the inductive antenna. The antenna on the card generates electronic voltage for supply to the tag on the card and feedbacks its ID and data to the MSR3110.



Card Emulation Mode

The MSR3110 may function as a tag, and hence an active card, by adding an antenna. The MSR3110 can implement the passive/active RFID protocols just like a tag.

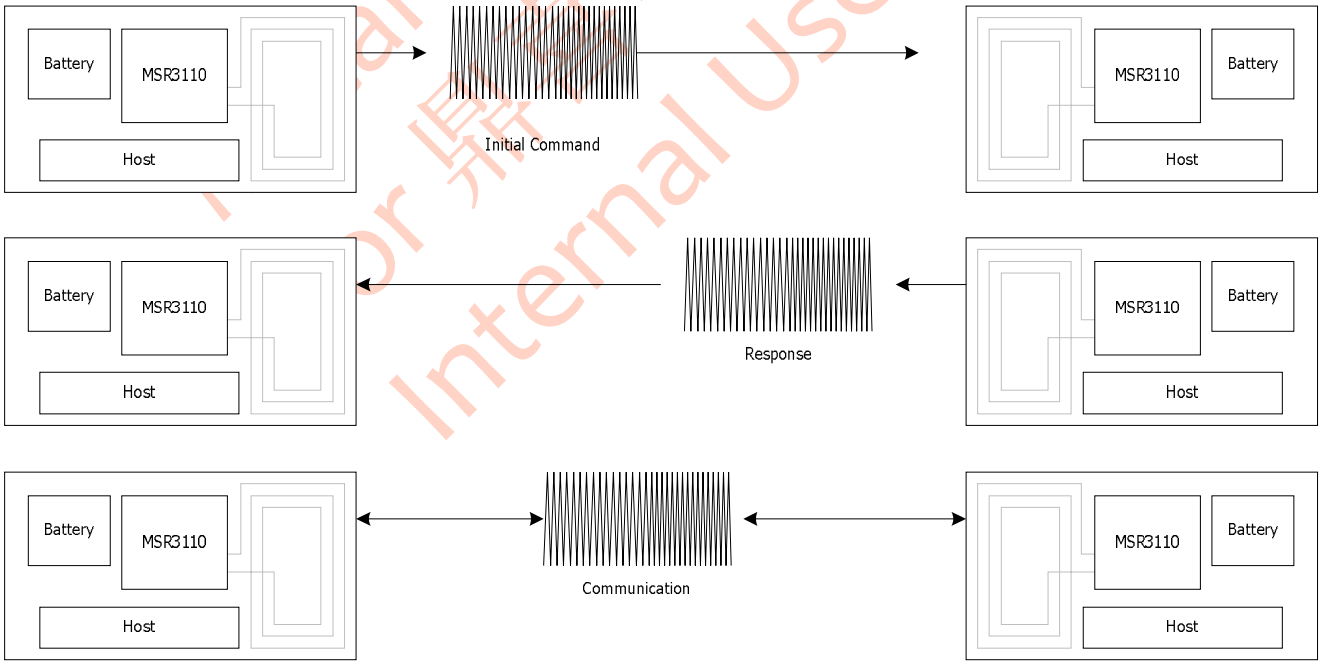
The MSR3110 could act as a passive tag as well.



NFC Mode

Near Field Communication (NFC) is a new, short-range wireless connectivity technology that evolved from a combination of existing contactless identification and interconnection technologies. Products with built-in NFC will dramatically simplify the way consumer devices interact with one another, helping users speed up connections, receive and share information and even make fast and secure payments.
Operating at 13.56 MHz and transferring data at up to 424 Kbits/second, NFC provides intuitive, simple, and safe communication between electronic devices. NFC is both a "read" and "write" technology. Communication between two NFC-compatible devices occurs when they are brought within four centimeters of one another: a simple wave or touch can establish an NFC connection which is then compatible with other known wireless technologies such as Bluetooth or Wi-Fi. The underlying layers of NFC technology follow ISO, ECMA, and ETSI standards. Because the transmission range is so short, NFC-enabled transactions are inherently secure. Also, physical proximity of the device to the reader gives users the reassurance of being in control of the process. NFC can be used with a variety of devices, from mobile phones that enable payment or transfer information to digital cameras that send their photos to a TV set with just a touch. The possibilities are endless, and NFC is sure to take the complexities out of today's increasingly sophisticated consumer devices and make them simpler to use.

Active NFC Mode:
In this mode, the MSR3110 could act as an active NFC device. It drives the inductive antenna to generate the magnet field, and also issues an initial command to the other NFC device through the magnet field, by coupling the magnet field. As long as the other NFC device responds to this initial command, the communication is established.



Passive NFC Mode:
In this mode, the MSR3110 will wait for the active NFC device's initial command, with its antenna sensing the magnet field created by the other NFC device. After the MSR3110 receives the initial command from the active NFC device, it will adjust the transfer speed and sends a response command to the active NFC device, causing the communication to be established.

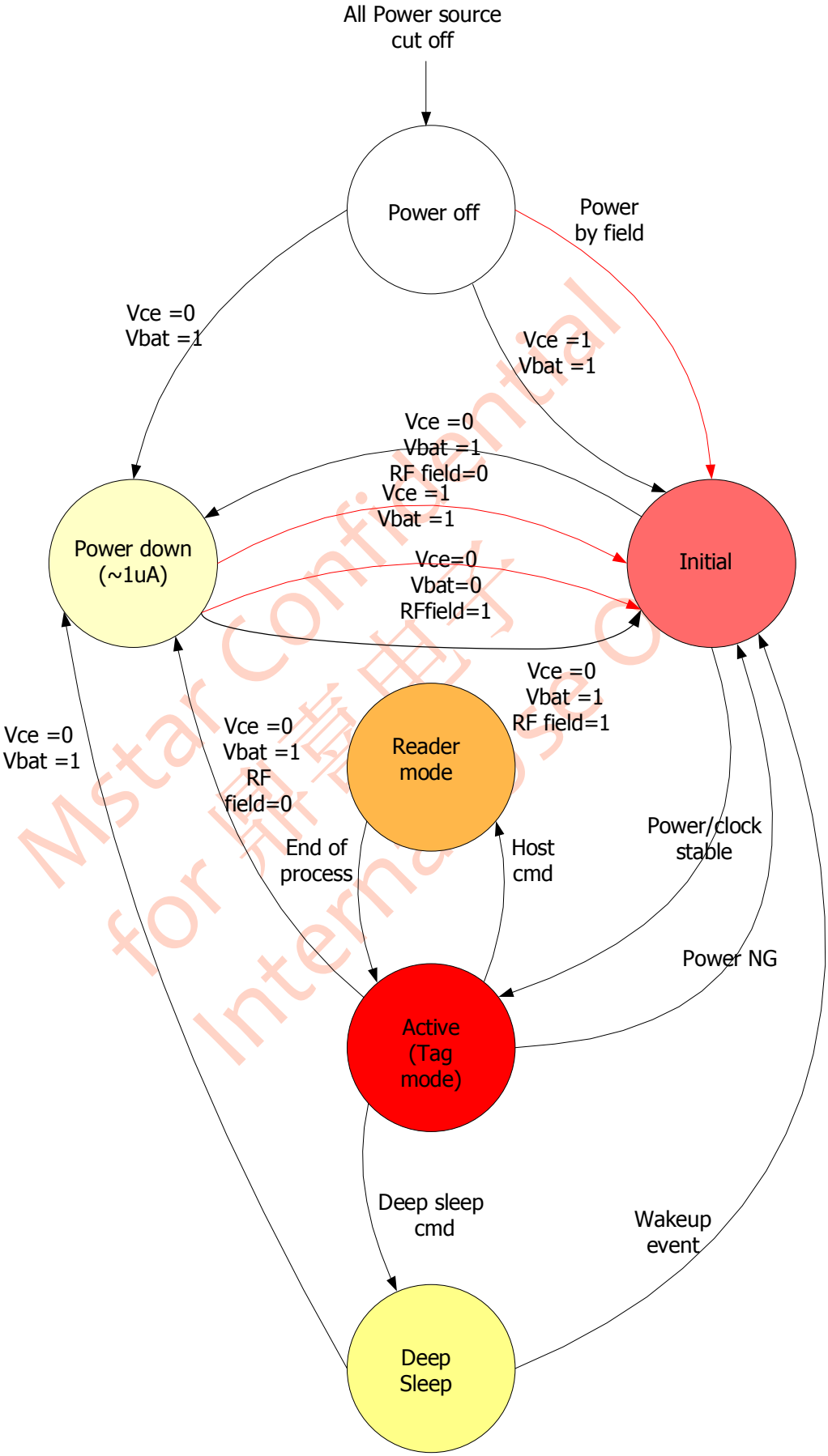
Proprietary Contactless Data Exchange Mode

In this mode, users could define their own protocol, and use the MSR3110 as a contactless communication media to transfer data, images, or maps between devices, for example mobile phones, Cameras, PCs, and others.

Power Modes

The MSR3110 has an enhanced power management unit to support several power supply sources which manages the power management of the device.

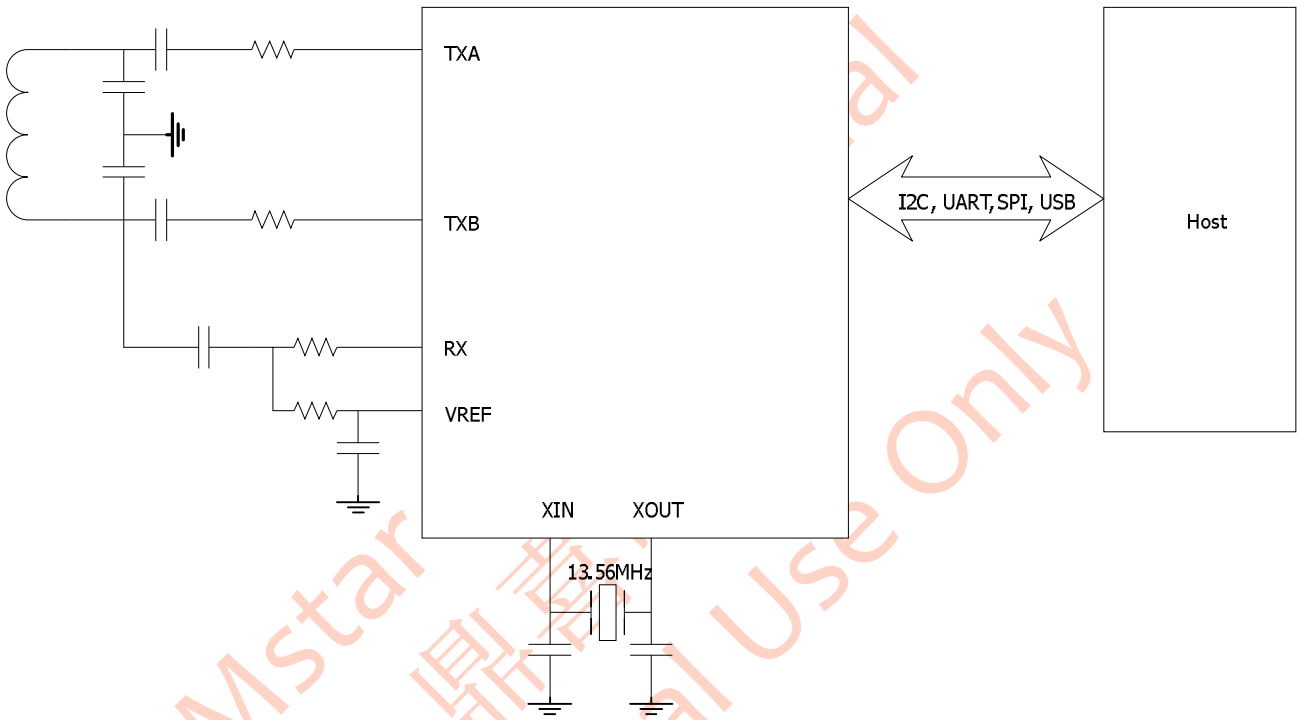
- Hard power down mode:
  Hard power down mode can only be set by host via VEN pin. In this mode power consumption could be less than 5 uA.
- Deep sleep mode:
  Deep sleep mode could be entered by software programming and exited by external wake-up pin, timer and RF field detector. In this mode power consumption could be less than 50 uA.
- Active mode:
  The power in active mode can be supplied by battery or antenna. In this mode, most modules are powered except for TX power.
- Reader mode:
  The power in reader mode can be supplied by battery or antenna. In this mode, all modules are powered.



Typical Test Circuits

The MSR3110 could drive the inductive antenna directly. There is a current-limiting circuit in the MSR3110 which limits the current to 150 mA. If limiting current to 100 mA is necessary, please add serial resistors with reference to the schematic.

The MSR3110 could interface to the Host by any SPI, USB, UART, or I^2C interface. No additional crystal is required for the USB interface.



PIN DIAGRAM (MSR3110)

	1	2	3	4	5	6	7	8	
A	GPIO_P05	GPIO_P04	GPIO_P01	VDDP		SPI_CLK	GND	VDD_FLASH	A
B	GPIO_P06	USB_DM	GPIO_P03	GPIO_P00	GND	SPI_DI	VDDC	GND	B
C		USB_DP	GPIO_P07	GND	USB_VBUS	GPIO_P02	SPI_DO	VDD_FU_SRC	C
D	RSTPD	UART0_TX	SCAN_EN	UART0_RX	WAKEUP	SMD_IO	SPI_CSN	VDDC	D
E	TXB	TXA	PMBYPASS	GND	AVDD_TX		SMD_RSTN		E
F	VREF	GND	XIN	GP2	GP1	PMU_3V	VDD_SMD	SMD_CLK	F
G	RX	AVDD_RX	GND	XOUT	VEN	VOUT_SIM	DVDD_NODIE	SMD_CARD_DET	G
H	RFIN1	RFIN2		AVDD	VOUT_1P2	PMU_SIM	VOUT_1P8	SWIO	H
	1	2	3	4	5	6	7	8	

PIN DESCRIPTION

Serial Flash Interface

Pin Name	Pin Type	Function	Pin
SPI_CSN	I/O	SPI Slave Selection; 8mA Driving Strength	D7
SPI_DI	I/O	SPI Master Data Input; 8mA Driving Strength	B6
SPI_DO	I/O	SPI Master Data Output; 8mA Driving Strength	C7
SPI_CLK	I/O	SPI Master Clock; 8mA Driving Strength	A6

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO_P07	I/O	General Purpose Input/Output #7; 4mA Driving Strength	C3
GPIO_P06	I/O	General Purpose Input/Output #6 / Active Low Reset Output; 4mA Driving Strength	B1
GPIO_P05	I/O	General Purpose Input/Output #5; 4mA Driving Strength	A1
GPIO_P04	I/O	General Purpose Input/Output #4; 4mA Driving Strength	A2
GPIO_P03	I/O	General Purpose Input/Output #3 / SPI Slave Data Input / UART1 TX; 4mA Driving Strength	B3
GPIO_P02	I/O	General Purpose Input/Output #2 / SPI Slave Data Output / UART RX; 4mA Driving Strength	C6
GPIO_P01	I/O	General Purpose Input/Output #1 / SPI Chip Select / I2C SDA; 4mA Driving Strength	A3
GPIO_P00	I/O	General Purpose Input/Output #0 / SPI SCK Clock / I2C SCL Clock; 4mA Driving Strength	B4

SWIO Interface

Pin Name	Pin Type	Function	Pin
SWIO	I/O	Single Wire Protocol Interface	H8

Smartcard Interface

Pin Name	Pin Type	Function	Pin
SMD_CARD_DET	Input	Smartcard Card Detection; 4mA Driving Strength	G8
SMD_CLK	I/O	Smartcard Clock Output; 4mA Driving Strength	F8
SMD_RSTN	I/O	Smartcard Reset; 4mA Driving Strength	E7
SMD_IO	I/O	Smartcard Data IO; 4mA Driving Strength	D6

RF Interface

Pin Name	Pin Type	Function	Pin
TXA	Analog Output	Transmitter TXA: Delivers Modulated Carrier	E2
TXB	Analog Output	Transmitter TXB: Delivers Modulated Carrier	E1
VREF	Analog Input	Internal Reference Voltage	F1
RX	Analog Input	Receiver Input for Reader Mode	G1
RFIN1	Analog Input	Receiver Input 1 for Tag Mode	H1
RFIN2	Analog Input	Receiver Input 2 for Tag Mode	H2
GP1	Analog Input	Getting Power Contact 1	F5
GP2	Analog Input	Getting Power Contact 2	F4

UART Interface

Pin Name	Pin Type	Function	Pin
UART0_RX	I/O	UART0 RX Signal / I2C SCL Signal	D4
UART0_TX	I/O	UART0 TX Signal / I2C SDA Signal	D2

USB Interface

Pin Name	Pin Type	Function	Pin
USB_DP	Analog I/O	USB Non Inverting Data Input/Output	C2
USB_DM	Analog I/O	USB Inverting Data Input/Output	B2
USB_VBUS	Analog I/O	USB VBUS	C5

Misc. Interface

Pin Name	Pin Type	Function	Pin
XIN	Crystal Oscillator Input	TRX_TOP Crystal Oscillator Input	F3
XOUT	Crystal Oscillator Output	TRX_TOP Crystal Oscillator Output	G4
SCAN_EN	Input	Scan Test Enable Pin	D3
WAKEUP	Input	External Signal for Wakeup from Deep Sleep Mode	D5
PMBYPASS	Input	Bypass Power Management Logic Block	E3
RSTPD	Input	Reset; Active High	D1
VEN	Input	Chip Enable; Low for Hard Power Down	G5

Power Pins

Pin Name	Pin Type	Function	Pin
VDDC	1.2V Power Input	Digital Power Supply	D8, B7
AVDD_TX	3.3V Power Input	TRX_TOP TX Power	E5
AVDD_RX	3.3V Power Input	TRX_TOP RX Power / MPLL Power	G2
VDD_SMD	3.3/1.8V Power Input	Smartcard IO Power Supply	F7
VDD_FLASH	1.8V Power Input	Embedded Flash Power Supply	A8
VDD_FU_SRC	3.3V Power Input	EFUSE Power Supply	C8
VDDP	3.3/1.8V Power Input	Pad Power Supply	A4
PMU_3V	3.3V Power Input	Main Power Supply from Host	F6
PMU_SIM	3.3/1.8V Power Input	SIM Power Supply from Host	H6
AVDD	Analog Power Output	Power Output for Analog Block	H4
DVDD_NODIE	1.2V Digital Power Output	Power Output for Digital Power Management Block	G7
VOUT_1P2	1.2V Digital Power Output	Power Output for Digital Core Block	H5
VOUT_SIM	1.8V Power Output	Power Output for External SIM Card	G6
VOUT_1P8	1.8V Power Output	Power Output for 1.8V Device	H7
GND	Ground	Ground	E4, G3, F2, B8, A7, B5, C4

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature	T_A	-40		85	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			125	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Current Consumption

Condition	Symbol	Min	Typ	Max	Unit
Hard Power Down	I_{DVDD} (1.2 V core power)		0		µA
	I_{PVDD} (3.3 V pad power)		0		µA
	I_{AVDD} (3.3 V analog power)		1.5		µA
Deep Sleep	I_{DVDD} (1.2 V core power)		0		µA
	I_{PVDD} (3.3 V pad power)		0		µA
	I_{AVDD} (3.3 V analog power)		50		µA
ISO 14443A Card Mode	I_{DVDD} (1.2 V core power)		2.8		mA
	I_{PVDD} (3.3 V pad power)		0.3		mA
	I_{AVDD} (3.3 V analog power) TX: I_{TVDD}, RX: I_{RVDD}/I_{AVDD}		1.5		mA

Notes:

1. TVDD depends on TVDD and the external circuitry connected to TXA and TXB.

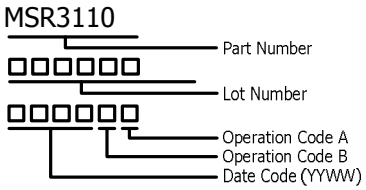
2. DVDD depends on the system application.

3. PVDD depends on the overall load at the digital pins.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MSR3110	-40°C to +85°C	TFBGA	59-ball

MARKING INFORMATION



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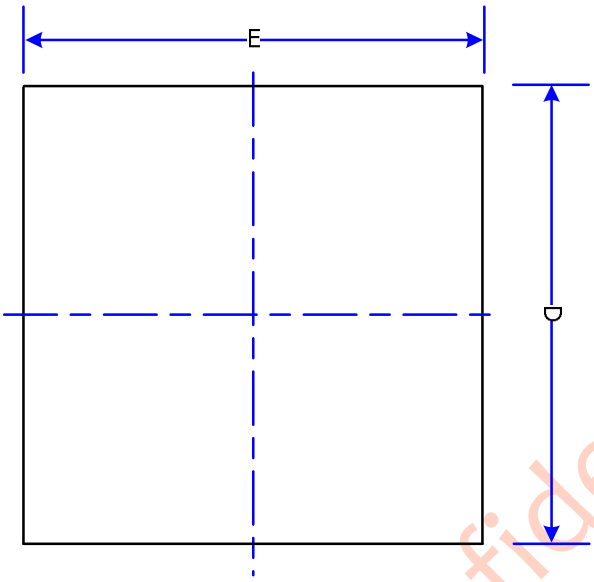
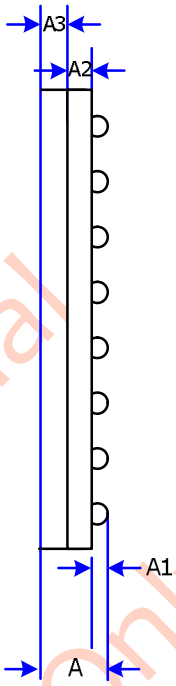
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSR3110 comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

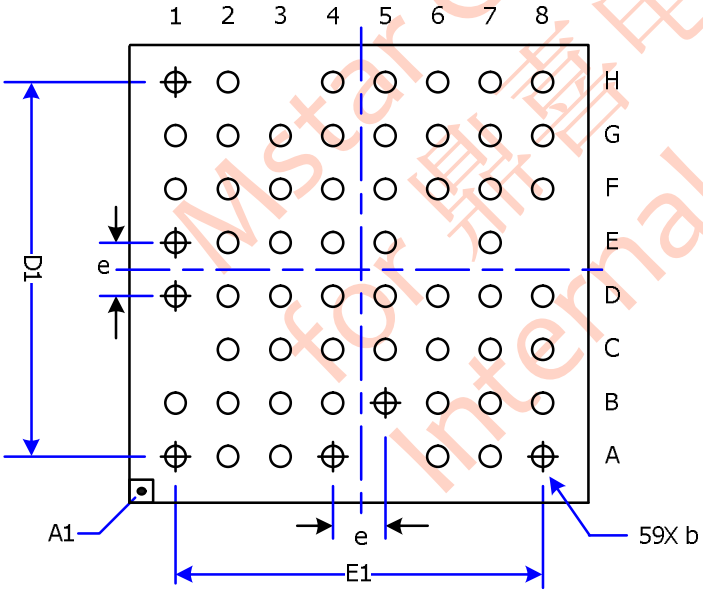
REVISION HISTORY

Document	Description	Date
MSR3110_ds_v01	• Initial release	Apr 2010

MECHANICAL DIMENSIONS







Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.20	-	-	0.047
A1	0.16	-	0.26	0.006	-	0.010
A2	0.21 REF			0.008 REF		
A3	0.70 REF			0.028 REF		
b	0.27	-	0.37	0.011	-	0.015
D	4.50 BSC			0.177 BSC		
E	4.50 BSC			0.177 BSC		
e	0.50 BSC			0.020 BSC		
D1	3.50 BSC			0.138 BSC		
E1	3.50 BSC			0.138 BSC		

REGISTER DESCRIPTION

HK MCU Register

HK_MCU Register 1 (16-bit direct addressing, 0x0800~0x08FF)

HK_MCU Register 1 (16-bit direct addressing, 0x0800~0x08FF)				
Index	**Mnemonic**	**Bit**	**Description**	
00h ~ 2Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
30h	**P0_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OE[7:0]	7:0	MCU Port 0 Output Enable Control.	
31h	**P0_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_CTRL[7:0]	7:0	MCU Port 0 Output Enable.	
32h	**P0_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_IN[7:0]	7:0	MCU Port 0 Output Enable from output data.	
33h	**P1_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OE[7:0]	7:0	MCU Port 1 Output Enable Control.	
34h	**P1_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_CTRL[7:0]	7:0	MCU Port 1 Output Enable.	
35h	**P1_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_IN[7:0]	7:0	MCU Port 1 Output Enable from output data.	
36h	**P2_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OE[7:0]	7:0	MCU Port 2 Output Enable Control.	
37h	**P2_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_CTRL[7:0]	7:0	MCU Port 2 Output Enable.	
38h	**P2_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_IN[7:0]	7:0	MCU Port 2 Output Enable from output data.	
39h	**P3_CTRL / SRAM_DIS**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OE	7:6	MCU Port 3 Output Enable Control.	
	-	5	Reserved.	
	HK_CACHE_CEZ	4	HK 2K cache SRAM Chip Enable. 0: Enable. 1: Disable.	
	P3_OE	3:0	MCU Port 3 Output Enable Control.	
3Ah	**P3_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_CTRL[7:0]	7:0	MCU Port 3 Output Enable.	

HK_MCU Register 1 (16-bit direct addressing, 0x0800~0x08FF)				
Index	**Mnemonic**	**Bit**	**Description**	
3Bh	**P3_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_IN[7:0]	7:0	MCU Port 3 Output Enable from output data.	
3Ch	**P4_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_OE	7:0	MCU Port 4 Output Enable Control.	
3Dh	**P4_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_CTRL	7:0	MCU Port 4 Output Enable.	
3Eh	**P4_IN / WAIT_OPT**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_IN	7:6	MCU Port 4 Output Enable from output data.	
	-	5:4	Reserved.	
	P4_IN	3:0	MCU Port 4 Output Enable from output data.	
3Fh	**SSPI_STS_OP**	**7:0**	**Default : 0x05**	**Access : R/W**
	SPPI_STS_OP[7:0]	7:0	Soft-trigger SPI check status OP code.	
40h	**SSPI_WD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD0[7:0]	7:0	S/W SPI Write Date 0.	
41h	**SSPI_WD_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD1[7:0]	7:0	S/W SPI Write Date 1.	
42h	**SSPI_WD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD2[7:0]	7:0	S/W SPI Write Date 2.	
43h	**SSPI_WD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD3[7:0]	7:0	S/W SPI Write Date 3.	
44h	**SSPI_WD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD4[7:0]	7:0	S/W SPI Write Date 4.	
45h	**SSPI_WD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD5[7:0]	7:0	S/W SPI Write Date 5.	
46h	**SSPI_WD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD6[7:0]	7:0	S/W SPI Write Date 6.	
47h	**SSPI_WD_7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD7[7:0]	7:0	S/W SPI Write Date 7.	
48h	**SSPI_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_TRIG	7	S/W SPI Trigger.	
	SSPI_CHK_BZY	6	Auto Check Busy after soft SPI.	
	SSPI_CHK_BIT[2:0]	5:3	Check busy Bit position.	
	SSPI_LENGTH[2:0]	2:0	SSPI command Length.	
49h	**SSPI_RD1**	**7:0**	**Default : 0x00**	**Access : R/W**

HK_MCU Register 1 (16-bit direct addressing, 0x0800~0x08FF)				
Index	**Mnemonic**	**Bit**	**Description**	
	SSPI_RD1	7:0	SSPI Read byte 1.	
4Ah	**SSPI_RD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD2	7:0	SSPI Read byte 2.	
4Bh	**SSPI_RD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD3	7:0	SSPI Read byte 3.	
4Ch	**SSPI_RD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD4	7:0	SSPI Read byte 4.	
4Dh	**SSPI_RD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD5	7:0	SSPI Read byte 5.	
4Eh	**SSPI_RD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD6	7:0	SSPI Read byte 6.	
4Fh	**SSPI_RD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_RD7	7:0	SSPI Read byte 7.	
50h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**EX_TIMER_MAX_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_0A	7:0	Crystal freq. External timer0 max count. EX_TIMER_MAX_0[31:24].	
01h	**EX_TIMER_MAX_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_0B	7:0	EX_TIMER_MAX_0[23:16].	
02h	**EX_TIMER_MAX_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_0C	7:0	EX_TIMER_MAX_0[15:8].	
03h	**EX_TIMER_MAX_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_0D	7:0	EX_TIMER_MAX_0[7:0].	
04h	**EX_TIMER_MAX_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_1A	7:0	External timer1 max count. EX_TIMER_MAX_1[31:24].	
05h	**EX_TIMER_MAX_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_1B	7:0	EX_TIMER_MAX_1[23:16].	
06h	**EX_TIMER_MAX_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_1C	7:0	EX_TIMER_MAX_1[15:8].	
07h	**EX_TIMER_MAX_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EX_TIMER_MAX_1D	7:0	EX_TIMER_MAX_1[7:0].	
08h	**NEW_WDT_L**	**7:0**	**Default : 0xAA**	**Access : R/W**
	NEW_WDT_L[7:0]	7:0	Watch dog enable/disable register. Enable: {NEW_WDT_H, NEW_WDT_L} != 0xaa55. (default) Disable: {NEW_WDT_H, NEW_WDT_L} == 0xaa55.	
09h	**NEW_WDT_H**	**7:0**	**Default : 0x55**	**Access : R/W**
	NEW_WDT_H[7:0]	7:0	Watch dog enable/disable register. Enable: {NEW_WDT_H, NEW_WDT_L} != 0xaa55. (default) Disable: {NEW_WDT_H, NEW_WDT_L} == 0xaa55.	
0Ah	**WDT_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	NEW_WDT_SEL	7:4	Select watchdog timer interval. 0000 = 16 STEP_TIME 0001 = 15 STEP_TIME 0010 = 14 STEP_TIME .... 1110 = 2 STEP_TIME 1111 = 1 STEP_TIME	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
			One step time = 1/fosc*3*1024*1024/10^6 For fosc=**14.318MHz** **STEP_TIME**=1/14.318*3*1024*1024/10^6=0.2197 second For fosc=**13.56MHz** **STEP_TIME**=1/13.56*3*1024*1024/10^6=0.2320 second For fosc=**12MHz** **STEP_TIME**=1/12*3*1024*1024/10^6=0.2621 second	
	-	3:0	Reserved.	
0Bh	**TIMER_CTRL_0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER0_TR	1	Start count. 0: Hold. 1: Count.	
	TIMER0_EN	0	Enable. 0: Clear. 1: Enable.	
0Ch	**TIMER_CTRL_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER1_TR	1	Start count. 0: Hold. 1: Count.	
	TIMER1_EN	0	Enable. 0: Clear. 1: Enable.	
0Dh	**MISC0**	**7:0**	**Default : 0x60**	**Access : R/W**
	-	7	Reserved.	
	USE_NEW_INT0	6	INT0 uses new 32-bit interrupt controller. 0: Disable. 1: Enable.	
	USE_NEW_INT1	5	INT1 uses new 32-bit interrupt controller. 0: Disable. 1: Enable.	
	SPI_IN_SRAM	4	Code in SRAM. 0: Code not in SRAM. 1: Code in SRAM.	
	DUAL_MODE	3	Winbond dual-output flash.	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	-	2	Reserved.	
	-	1:0	Reserved.	
0Eh ~ 1Fh	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
20h	**P0_OV**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OV	7:0	P0 override by P0_REG. 0: Disable. 1: Enable.	
21h	**P0_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_REG	7:0	Data to override P0.	
22h	**P1_OV**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OV	7:0	P1 override by P1_REG. 0: Disable. 1: Enable.	
23h	**P1_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_REG	7:0	Data to override P1.	
24h	**P2_OV**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OV	7:0	P2 override by P2_REG. 0: Disable. 1: Enable.	
25h	**P2_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_REG	7:0	Data to override P2.	
26h	**P3_OV**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OV	7:0	P3 override by P3_REG. 0: Disable. 1: Enable	
27h	**P3_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_REG	7:0	Data to override P3.	
28h	**P4_OV**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_OV	7:0	P4 override by P4_REG. 0: Disable. 1: Enable.	
29h	**P4_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_REG	7:0	Data to override P4.	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
30h	**MCUPLL_1**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	CLK_EN_SEL	6:4	001: Default.	
	-	3	Reserved.	
	-	2:0	Reserved.	
31h ~ 39h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
40h	**SPI_DMA_START_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_START_ADDR0	7:0	SPI_DMA_START_ADDR[7:0].	
41h	**SPI_DMA_START_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_START_ADDR1	7:0	SPI_DMA_START_ADDR[15:8].	
42h	**SPI_DMA_START_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_START_ADDR2	7:4	SPI_DMA_START_ADDR[19:16].	
		3:1	Reserved.	
	SPI_DMA_DIRECT_MODE	0	Direct access. 0: Indirect access (single port). 1: Direct access (DEST_ADDR increment every write).	
43h	**SPI_DMA_BYTE_CNT**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_BYTE_CNT0	7:0	SPI_DMA_BYTE_CNT[7:0]. If SPI_DMA_BYTE_CNT==0: Move 65536 bytes. Otherwise: Move SPI_DMA_BYTE_CNT bytes.	
44h	**SPI_DMA_BYTE_CNT**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_BYTE_CNT1	7:0	SPI_DMA_BYTE_CNT [15:8].	
45h	**SPI_DMA_MIN_CYCLE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_MIN_CYCLE	7:0	SPI_DMA_MIN_CYCLE.	
46h	**SPI_DMA_DEST_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_DEST_ADDR0	7:0	SPI_DMA_DEST_ADDR0[7:0].	
47h	**SPI_DMA_DEST_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_DEST_ADDR1	7:0	SPI_DMA_DEST_ADDR0 [15:8].	
48h	**SPI_CONFIG**	**7:0**	**Default : 0x70**	**Access : R/W**
	FAST_READ	7	Fast mode.	
	CS_HIGH	6:4	Minimum cycle of CSZ should remain High.	
		3:0	Reserved.	
49h ~	**-**	**7:0**	**Default : -**	**Access : -**

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
BFh	-	7:0	Reserved.	
C0h	**NEW_WDT_CLR**	**7:0**	**Default : -**	**Access : TRIG**
	NEW_WDT_CLR[7:0]	7:0	Write the register to trigger WDT clear (data does not matter).	
C1h	**EX_TIMER0_CLEAR**	**7:0**	**Default : -**	**Access : TRIG**
	EX_TIMER0_CLEAR	7:0	Write the register to trigger timer0 clear (data does not matter).	
C2h	**EX_TIMER0_CAPTURE**	**7:0**	**Default : -**	**Access : TRIG**
	EX_TIMER0_CAPTURE	7:0	Write the register to trigger timer0 capture (data does not matter).	
C3h	**EX_TIMER1_CLEAR**	**7:0**	**Default : -**	**Access : TRIG**
	EX_TIMER1_CLEAR	7:0	Write the register to trigger timer1 clear (data does not matter).	
C4h	**EX_TIMER1_CAPTURE**	**7:0**	**Default : -**	**Access : TRIG**
	EX_TIMER1_CAPTURE	7:0	Write the register to trigger timer1 capture (data does not matter).	
C5h ~ C8h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
C9h	**SPI_DMA_START_TRIG**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_DMA_START_TRIG	7:0	Write the register to trigger SPI DMA transfer.	
CAh	**MCU_RST_TRIG**	**7:0**	**Default : -**	**Access : TRIG**
	MCU_RST_TRIG	7:0	Write the register to trigger CPU reset.	
CBh ~ DFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
E0h	**EX_TIMER0_CAPTURE_CNT_A**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER0_CAPTURE_CNT [31:24]	7:0	EX_TIMER_CNT_CAP_0[31:24].	
E1h	**EX_TIMER0_CAPTURE_CNT_B**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER0_CAPTURE_CNT [23:16]	7:0	EX_TIMER_CNT_CAP_0[23:16].	
E2h	**EX_TIMER0_CAPTURE_CNT_C**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER0_CAPTURE_CNT [15:8]	7:0	EX_TIMER_CNT_CAP_0[15:8].	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
E3h	**EX_TIMER0_CAPTURE_CNT_D**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER0_CAPTURE_CNT [7:0]	7:0	EX_TIMER_CNT_CAP_0[7:0].	
E4h	**EX_TIMER1_CAPTURE_CNT_A**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER1_CAPTURE_CNT [31:24]	7:0	EX_TIMER_CNT_CAP_1[31:24].	
E5h	**EX_TIMER1_CAPTURE_CNT_B**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER1_CAPTURE_CNT [23:16]	7:0	EX_TIMER_CNT_CAP_1[23:16].	
E6h	**EX_TIMER1_CAPTURE_CNT_C**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER1_CAPTURE_CNT [15:8]	7:0	EX_TIMER_CNT_CAP_1[15:8].	
E7h	**EX_TIMER1_CAPTURE_CNT_D**	**7:0**	**Default : -**	**Access : RO**
	EX_TIMER1_CAPTURE_CNT [7:0]	7:0	EX_TIMER_CNT_CAP_1[7:0].	
E8h ~ E9h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
EAh	**M8051_CONFIG**	**7:0**	**Default : -**	**Access : RO**
	BONDING	7:4	Reserved.	
	MODE	3:0	Reserved.	
EBh	**M8051_CONFIG2**	**7:0**	**Default : -**	**Access : RO**
	DISABLE_WAIT_STABLE	7	DISABLE_WAIT_STABLE. 0: Enable wait. 1: Disable wait.	
	STABLE_TIME_SEL	6	STABLE_TIME_SEL.	
		5:1	Reserved.	
	MCU_RST_CNT	3:0	Soft-reset counter.	
ECh	**M8051_CONFIG3**	**7:0**	**Default : -**	**Access : RO**
		7:3	Reserved.	
	BIST_TAG	2	TAG SRAM. 0: Pass.	

HK_MCU Register 1 (16-bit direct addressing, 0x0900~0x09FF)				
Index	**Mnemonic**	**Bit**	**Description**	
			1: Fail.	
	BIST_CACHE	1	CACHE SRAM. 0: Pass. 1: Fail.	
	BIST_IDATA	0	IDATA SRAM. 0: Pass. 1: Fail.	
EDh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

HK_MCU Register 2 (16-bit direct addressing, 0x0A00~0x0AFF)

HK_MCU Register 2 (16-bit direct addressing, 0x0A00~0x0AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**X32KA_CODE_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	X32KA_CODE_ADDR	7:2	1st 32K xdata (0x8000) AS_CODE address adjust, 1K boundary.	
	-	1:0	Reserved.	
01h	**X32KA_MAP_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	X32KA_CODE	7	AS_CODE. 0: Disable. 1: Enable.	
	X32KA_SINGLE_BANK	6	MAP_SINGLE_BANK. 0: Map to common area. 1: Map to bank area.	
	-	5:4	Reserved.	
	X32KA_BANK	3:0	MAP_BANK. MAP_SINGLE_BANK==0: Don't care these bits. MAP_SINGLE_BANK==1: This memory is mapped to MAP_BANK[3:0] bank area.	
02h	**X32KB_CODE_ADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	X32KB_CODE_ADDR	7:2	2nd 32K xdata (0x8000) AS_CODE address adjust, 1K boundary.	
	-	1:0	Reserved.	
03h	**X32KB_MAP_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	X32KB_CODE	7	AS_CODE. 0: Disable. 1: Enable.	
	X32KB_SINGLE_BANK	6	MAP_SINGLE_BANK. 0: Map to common area. 1: Map to bank area.	
	-	5:4	Reserved.	
	X32KB_BANK	3:0	MAP_BANK. MAP_SINGLE_BANK==0: Don't care these bits. MAP_SINGLE_BANK==1: This memory is mapped to MAP_BANK[3:0] bank area.	
04h	**MCU_MISC**	**7:0**	**Default : 0x00**	**Access : R/W**
	XDATA_BANK	7	32k SRAM selection. 0: Select 1st 32K. 1: Select 2nd 32K.	

HK_MCU Register 2 (16-bit direct addressing, 0x0A00~0x0AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
	ROM_BIST	6	ROM BIST enable. 0: Disable. 1: Enable.	
	ROM_PAGE	5:4	16K ROM map to four 4K ROM (0x6000~0x6FFF). 00: 1st 4K. 01: 2nd 4K. 10: 3rd 4K. 11: 4th 4K.	
	ROM_SHIFT	3:0	ROM boot up from offset. 0000: Boot from ROM address 0x0000. 0001: Boot from ROM address 0x0400. 0010: Boot from ROM address 0x0800. 0011: Boot from ROM address 0x0C00. 0100: Boot from ROM address 0x1000. 0101: Boot from ROM address 0x1400. 0110: Boot from ROM address 0x1800. 0111: Boot from ROM address 0x1C00. 1000: Boot from ROM address 0x2000. 1001: Boot from ROM address 0x2400. 1010: Boot from ROM address 0x2800. 1011: Boot from ROM address 0x2C00. 1100: Boot from ROM address 0x3000. 1101: Boot from ROM address 0x3400. 1110: Boot from ROM address 0x3800. 1111: Boot from ROM address 0x3C00.	
05h	**MCU_OVERIDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OV_EN	7	Override enable. 0: Disable. 1: Enable.	
	OV_MODE	6:4	Override mode. Data for overriding pad's mode.	
		3:0	Reserved.	
06h ~ DFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
E0h	**MCU_BIST**	**7:0**	**Default : -**	**Access : RO**
	BIST_MODE	7	BIST. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	

HK_MCU Register 2 (16-bit direct addressing, 0x0A00~0x0AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
	BIST_4K	4	4K SRAM BIST result. 0: Pass. 1: Fail.	
	BIST_32K_A	3	1st 32K SRAM BIST result. 0: Pass. 1: Fail.	
	BIST_32K_B	2	2nd 32K SRAM BIST result. 0: Pass. 1: Fail.	
	ROM_FINISH	1	16K ROM BIST result. 0: Not finish yet. 1: Finish.	
	ROM_PASS	0	16K ROM BIST result. 0: Not pass. 1: Pass.	
E1h	**MCU_MODE**	**7:0**	**Default : 0x00**	**Access : R/W**
		7	Reserved.	
	BOOT_SELECTION	6:4	CPU boot source selection. 000: SPI. 001: ROM. 010: SRAM. 011: SPI. 100~111: Reserved.	
		3:0	Reserved.	
E2h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**INT_STA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA0	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.7, interrupt status of P2.7. [6]: INT1.6, interrupt status of P2.6. [5]: INT1.5, interrupt status of P2.5. [4]: INT1.4, interrupt status of P2.4. [3]: INT1.3, interrupt status of P2.3. [2]: INT1.2, interrupt status of P2.2. [1]: INT1.1, interrupt status of P2.1. [0]: INT1.0, interrupt status of P2.0.	
01h	**INT_ENA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA0[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one; external interrupt enable. 0: Disable. 1: Enable.	
02h	**INT_INV0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV0	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When C093[0] = 0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When C093[0] = 1 (level mode): 0: Normal. 1: Invert.	
03h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
04h	**INT_ACT0**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT0	7:0	Status register of each interrupt source set by hardware.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
			This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
05h	**INT_SW0**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW0	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
06h	**INT_SRC0**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC0	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
07h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
08h	**INT_STA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA1	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.15, reserved. [6]: INT1.14, reserved. [5]: INT1.13, reserved. [4]: INT1.12, reserved. [3]: INT1.11, reserved. [2]: INT1.10, reserved. [1]: INT1.9, interrupt status of EX_TIMER1. [0]: INT1.8, interrupt status of EX_TIMER0.	
09h	**INT_ENA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA1[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
0Ah	**INT_INV1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV1	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=0 (level mode): 0: Normal. 1: Invert.	
0Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ch	**INT_ACT1**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT1	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
0Dh	**INT_SW1**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW1[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
0Eh	**INT_SRC1**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC1	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
0Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
10h	**INT_STA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA2	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width	

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
			should be greater than five times of the CPU clock cycles. [7]: INT1.23, P1.7. [6]: INT1.22, P1.6. [5]: INT1.21, P1.5. [4]: INT1.20, P1.4. [3]: INT1.19, P1.3. [2]: INT1.18, P1.2. [1]: INT1.17, P1.1. [0]: INT1.16, P1.0.	
11h	**INT_ENA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA2[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	
12h	**INT_INV2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV2	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=1 (level mode): 0: Normal. 1: Invert.	
13h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
14h	**INT_ACT2**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT2	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
15h	**INT_SW2**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW2[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
16h	**INT_SRC2**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC2	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
17h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
18h	**INT_STA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA3	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.31, reserved. [6]: INT1.30, USB. [5]: INT1.29, reserved. [4]: INT1.28, reserved. [3]: INT1.27, reserved. [2]: INT1.26, reserved. [1]: INT1.25, reserved. [0]: INT1.24, reserved.	
19h	**INT_ENA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA3[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	
1Ah	**INT_INV3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV3	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=1 (level mode): 0: Normal. 1: Invert.	
1Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
1Ch	**INT_ACT3**	**7:0**	**Default : 0x00**	**Access : RO**

HK_MCU INT1 Register (16-bit direct addressing, 0x1A00~0x1AFF)				
Index	**Mnemonic**	**Bit**	**Description**	
	INT_ACT3	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
1Dh	**INT_SW3**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW3[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
1Eh	**INT_SRC3**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC3	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
1Fh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**INT_STA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA0	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.7, interrupt status of P2.7. [6]: INT1.6, interrupt status of P2.6. [5]: INT1.5, interrupt status of P2.5. [4]: INT1.4, interrupt status of P2.4. [3]: INT1.3, interrupt status of P2.3. [2]: INT1.2, interrupt status of P2.2. [1]: INT1.1, interrupt status of P2.1. [0]: INT1.0, interrupt status of P2.0.	
01h	**INT_ENA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA0[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one; external interrupt enable. 0: Disable. 1: Enable.	
02h	**INT_INV0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV0	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When C093[0] = 0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When C093[0] = 1 (level mode): 0: Normal. 1: Invert.	
03h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
04h	**INT_ACT0**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT0	7:0	Status register of each interrupt source set by hardware.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
			This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
05h	**INT_SW0**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW0	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
06h	**INT_SRC0**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC0	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
07h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
08h	**INT_STA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA1	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.15, reserved. [6]: INT1.14, reserved. [5]: INT1.13, reserved. [4]: INT1.12, reserved. [3]: INT1.11, reserved. [2]: INT1.10, reserved. [1]: INT1.9, interrupt status of EX_TIMER1. [0]: INT1.8, interrupt status of EX_TIMER0.	
09h	**INT_ENA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA1[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
0Ah	**INT_INV1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV1	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=0 (level mode): 0: Normal. 1: Invert.	
0Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ch	**INT_ACT1**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT1	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
0Dh	**INT_SW1**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW1[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
0Eh	**INT_SRC1**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC1	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
0Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
10h	**INT_STA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA2	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width	

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
			should be greater than five times of the CPU clock cycles. [7]: INT1.23, P1.7. [6]: INT1.22, P1.6. [5]: INT1.21, P1.5. [4]: INT1.20, P1.4. [3]: INT1.19, P1.3. [2]: INT1.18, P1.2. [1]: INT1.17, P1.1. [0]: INT1.16, P1.0.	
11h	**INT_ENA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA2[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	
12h	**INT_INV2**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV2	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=1 (level mode): 0: Normal. 1: Invert.	
13h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
14h	**INT_ACT2**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_ACT2	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
15h	**INT_SW2**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW2[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
16h	**INT_SRC2**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC2	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
17h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
18h	**INT_STA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_STA3	7:0	Status register of each source set by hardware and cleared by software. Read: Interrupt request. 0: No. 1: Yes. Write: 0: Clear the status bit. 1: Keep the status bit. Despite edge or level mode, the interrupt's pulse width should be greater than five times of the CPU clock cycles. [7]: INT1.31, reserved. [6]: INT1.30, USB. [5]: INT1.29, reserved. [4]: INT1.28, reserved. [3]: INT1.27, reserved. [2]: INT1.26, reserved. [1]: INT1.25, reserved. [0]: INT1.24, reserved.	
19h	**INT_ENA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_ENA3[7:0]	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt enable. 0: Disable. 1: Enable.	
1Ah	**INT_INV3**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INV3	7:0	The 8-bit mapping to INTSTA1A one by one. External interrupt polarity. When c093[0]=0 (edge mode): 0: Detect rising edge. 1: Detect falling edge. When c093[0]=1 (level mode): 0: Normal. 1: Invert.	
1Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
1Ch	**INT_ACT3**	**7:0**	**Default : 0x00**	**Access : RO**

HK_MCU INT1 Register (16-bit direct addressing, 0x1B00~0x1BFF)				
Index	**Mnemonic**	**Bit**	**Description**	
	INT_ACT3	7:0	Status register of each interrupt source set by hardware. This register is used in ISR( ) to determine which interrupt source occurs. 0: Interrupt inactive. 1: Interrupt active.	
1Dh	**INT_SW3**	**7:0**	**Default : 0x00**	**Access : WO**
	INT_SW3[7:0]	7:0	Emulate interrupt. 0: Interrupt occurs just when individual source is triggered. 1: SW-trigger interrupt, trigger one pulse only.	
1Eh	**INT_SRC3**	**7:0**	**Default : -**	**Access : RO**
	INT_SRC3	7:0	Interrupt source signal. 0: Clear the status bit. 1: Keep the status bit.	
1Fh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

NFC Register

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**REG00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MILLER_T[7:6]	7:6	Modify miller duration time. 00: 32/fc. 01: 16/fc. 10: 8/fc. 11: 4/fc.	
	MILLER_EN	5	Miller mode modification. 0: Disable modify miller mode. 1: Enable modify miller mode.	
	TX_RATE[4:2]	4:2	TX rate. 000: Fc/8. 001: Fc/16. 010: Fc/32. 011: Fc/64. 100: Fc/128. 101: Fc/256. 110: Fc/4. 111: Fc/2. Others: Reserved.	
	TX_MODE	1	TX mode. 0: TX output signal is bypassws from Dout[0]. 1: TX output signal is controlled by buffer control module.	
	TX_EN	0	TX enable. 0: Disable TX. 1: Enable TX output signal to RF.	
04h	**REG04**	**7:0**	**Default : 0x15**	**Access : R/W**
	TX_VGA[7:0]	7:0	TX voltage gain control. Bit[7:0]: MODI_LV.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA[7:0]	7:0	TX data port.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NFC_DCT	7	NFC external RF detected.	
	RX_SYNC_EN	6	RX sync function enable.	
	RX_POLAR	5	0: RX signal active high. 1: RX signal active low.	
	IDLE32_DLY_EN	4	Idle32 delay timer enable.	

NFC Register

Index	Mnemonic	Bit	Description	
	RX_RATE[3:2]	3:2	RX rate. 00: Fc/8. 01: Fc/16. 10: Fc/32. 11: Fc/64.	
	FIFO_EMPTY	1	RX FIFO empty.	
	RX_EN	0	RX enable.	
10h	**REG10**	**7:0**	**Default : 0x06**	**Access : R/W**
	RX_VGA0[7:0]	7:0	RX voltage gain control 0 for DROOP. Bit[7]: Reserved. Bit[6:0]: DROOP.	
14h	**REG14**	**7:0**	**Default : 0x55**	**Access : R/W**
	RX_VGA1[7:0]	7:0	RX voltage gain control 1. Bit[7:6]: GAIN1. Bit[5:4]: GAIN1AC. Bit[3:2]: GAIN2. Bit[1:0]: GAIN2AC.	
18h	**REG18**	**7:0**	**Default : 0x4F**	**Access : R/W**
	RX_VGA2[7:0]	7:0	RX voltage gain control 2. Bit[7]: Reserved. Bit[6:4]: LEVEL. Bit[3:2]: Reserved. Bit[1:0]: INVOUT.	
1Ch	**REG1C**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	RD_STROB	0	Read strobe.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA[7:0]	7:0	RX data port.	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : RO**
	UNI_DECODE_COL_POS0[7:0]	7:0	UNI decode first collision position0.	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : RO**
	UNI_DECODE_COL_POS1[7:0]	7:0	UNI decode first collision position1.	
2Ch	**REG2C**	**7:0**	**Default : 0xA0**	**Access : R/W**
	HF_RESET	7	0: HF reset.	
	MICLK_INV	6	Invert miller clock.	
	MICLK_GAT	5	Gate miller clock.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	TXCLK_INV	4	Invert TX clock.	
	TXCLK_GAT	3	Gate TX clock.	
	RXCLK_INV	2	Invert RX clock (clk13m no inversion).	
	RXCLK_GAT	1	Gate RX clock (clk13m always working).	
	BYPASS_TRX	0	Bypass analog block and pull TX/RX signal to IO.	
30h	**REG30**	**7:0**	**Default : 0x40**	**Access : R/W**
	PWR_CTRL[7:0]	7:0	Analog block power control. Bit[7]: PDN_OC_LV. Bit[6]: TAG_MODE_LV. Bit[5]: FBR_CON_LV. Bit[4]: TX_EN_LV. Bit[3]: PWR_NFC. Bit[2]: PWR. Bit[1]: PWR_RX. Bit[0]: PWR_TX.	
34h	**REG34**	**7:0**	**Default : 0x44**	**Access : R/W**
	UNI_RCLK_INV	7	Invert UNI decode clock (UNI_DECODE).	
	UNI_RCLK_GAT	6	Gate UNI decode clock (UNI_DECODE).	
	SWP_TCLK_INV	5	Invert SWP Timer clock.	
	SWP_TCLK_GAT	4	Gate SWP Timer clock.	
	RXREC_RCLK_INV	3	Invert RX_RECOVERY clock (RX_RECOVERY).	
	RXREC_RCLK_GAT	2	Gate RX_RECOVERY clock (RX_RECOVERY).	
	-	1:0	Reserved.	
38h	**REG38**	**7:0**	**Default : 0x03**	**Access : RO, R/W**
	SWITCH_MD[7:6]	7:6	Serial IN/OUT switch mode. 00: Normal. 01: BB2S. 10: Bypass BB.	
	MM_DECODE_EN	5	Modify Miller decode enable.	
	MM_DECODE_DONE	4	Modify Miller decode done.	
	SOFT_TX	3	Software TX value.	
	SOFT_CFG	2	Software configure TX output value enable.	
	SDD43B_CLKSEL	1	SDD43b clock select (NRZ_DECODE, NRZ_BPSK_ENCODE, SDD43B_CTRL). 0: Fc. 1: Fc/2.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	TAG_CLK13M_SEL	0	Tag mode tag encode clock selection. 0: Clock from crystal. 1: Clock from field.	
3Ch	**REG3C**	**7:0**	**Default : 0x24**	**Access : R/W**
	IDLE32I_DLY_EN	7	Idle32i delay timer enable.	
	TX_POLAR	6	0: TX signal active low. 1: TX signal active high.	
	BUF_CLKSEL	5	0: Clk1356. 1: Clkdiv2.	
	TX_ENCODE	4	TX Manchester encode enable.	
	IDREG_SEL	3	0: NFCID1[55:0] generated by Laser ID, NFCID1[63:56] generated by software. 1: NFCID1[63:0] generated by software.	
	NFC_DIV[2:0]	2:0	000: NFC module needs fc clock (3.2M). 001: NFC module needs fc/2 clock (1.6M). 010: NFC module needs fc/4 clock (848K). 011: NFC module needs fc/8 clock (424K). 100: NFC module needs fc/16 clock (212K). Others: RFU.	
40h	**REG40**	**7:0**	**Default : 0x40**	**Access : RO, R/W**
	SDD106_EBIT_EN	7	SDD106 end bit enable.	
	SDD106_CLKSEL	6	SDD106 clock selection (MM_DECODE, MANSUB106_ENCODE, SDD106_CTRL). 0: Fc. 1: Fc/2.	
	SDD106_COMP2	5	Single device detection 106K RATS complete.	
	SDD106_ST2	4	Single device detection 106K start 2.	
	SDD106_ST1	3	Single device detection 106K start 1.	
	SDD106_COMP1	2	Single device detection 106K SDD complete.	
	SDD106_CLR	1	Clear Single device detection 106K.	
	SDD106_EN	0	Single device detection 106K enable.	
44h	**REG44**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SDD106_DESEL_DET	7	Single device detection 106K DESEL command detection.	
	CB_WADDR_CLR	6	Control buffer CPU write address clear.	
	SDD24_ERR	5	Single device detection error flag happens at 212/424K/848K/1.6M/3.2M.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	MAN_DECODE_EN	4	Data transaction Manchester decode enable at 212/424k/848K/1.6M/3.2M.	
	SDD24_ST	3	Single device detection 212/424K/848K/1.6M/3.2M start.	
	SDD24_COMP	2	Single device detection 212/424K/848K/1.6M/3.2M complete.	
	SDD24_CLR	1	Clear Single device detection 212/424K/848K/1.6M/3.2M.	
	SDD24_EN	0	Single device detection 212/424K/848K/1.6M/3.2M enable.	
48h	**REG48**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID10[7:0]	7:0	NFCID10 register value.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID11[7:0]	7:0	NFCID11 register value.	
50h	**REG50**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID12[7:0]	7:0	NFCID12 register value.	
54h	**REG54**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID13[7:0]	7:0	NFCID13 register value.	
58h	**REG58**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID14[7:0]	7:0	NFCID14 register value.	
5Ch	**REG5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID15[7:0]	7:0	NFCID15 register value.	
60h	**REG60**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID16[7:0]	7:0	NFCID16 register value.	
64h	**REG64**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID17[7:0]	7:0	NFCID17 register value.	
68h	**REG68**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID18[7:0]	7:0	NFCID18 register value.	
6Ch	**REG6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID19[7:0]	7:0	NFCID19 register value.	
70h	**REG70**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID20[7:0]	7:0	NFCID20 register value.	
74h	**REG74**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID21[7:0]	7:0	NFCID21 register value.	
78h	**REG78**	**7:0**	**Default : 0x00**	**Access : R/W**

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	NFCID22[7:0]	7:0	NFCID22 register value.	
7Ch	**REG7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID23[7:0]	7:0	NFCID23 register value.	
80h	**REG80**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID24[7:0]	7:0	NFCID24 register value.	
84h	**REG84**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID25[7:0]	7:0	NFCID25 register value.	
88h	**REG88**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID26[7:0]	7:0	NFCID26 register value.	
8Ch	**REG8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFCID27[7:0]	7:0	NFCID27 register value.	
90h	**REG90**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CRYPTO_CLK_INV	5	Invert Crypto clock (MM_ENCODE clock).	
	CRYPTO_CLK_GAT	4	Gate Crypto clock (MM_ENCODE clock).	
	PPM_TCLK_INV	3	Invert PPM_ENCODE clock (PPM_ENCODE).	
	PPM_TCLK_GAT	2	Gate PPM_ENCODE clock (PPM_ENCODE).	
	-	1:0	Reserved.	
94h	**REG94**	**7:0**	**Default : 0xA0**	**Access : R/W**
	SDD24_SLOT_DELAY[7:0]	7:0	Single device detection 212/424K/848K/1.6M/3.2M slot reply delay (fc).	
98h	**REG98**	**7:0**	**Default : 0x82**	**Access : R/W**
	TST_NC[7:0]	7:0	TST_NC value for analog TRX_TOP setting.	
9Ch	**REG9C**	**7:0**	**Default : 0x03**	**Access : R/W**
	RX_REC_EN	7	RX recovery enable.	
	UNI_DECODE_DAT_PHASE_EN	6	UNI decode data phase detect enable (for gen2 tag detection).	
	RX_REC_TYPE[5:4]	5:4	RX recovery type. 00: One sub-carrier remover (Tag693/Tag43A decode). 01: Two sub-carrier remover (Tag693 decode). 10: BPSK sub-carrier remover (Tag43B decode). 11: BPSK sub-carrier remover (Tag43A 212K/424K decode).	
	RX_REC_FORCE_LOW	3	RX recovery force data low.	
	RX_REC_THRSHD[2:0]	2:0	RX recovery decision threshold.	

NFC Register

Index	Mnemonic	Bit	Description	
A0h	**REGA0**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RX_REC_PERIOD[7:0]	7:0	RX recovery sub-carrier period.	
A4h	**REGA4**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	UNI_DECODE_DONE	7	UNI decode done.	
	UNI_DECODE_COL_FLAG	6	UNI decode collision occur flag. 0: No collision. 1: Collision.	
	UNI_DECODE_DAT_CLKSEL[5:2]	5:2	UNI decode clock select (fs). 0000: Fc. 0001: Fc/2. 0010: Fc/4. 0011: Fc/8. 0100: Fc/16. 0101: Fc/32. 0110: Fc/64. 0111: Fc/128. 1000: Fc/256. 1001: Fc/512. 1010: Fc/1024. 0thers: Reserved.	
	UNI_DECODE_DIR	1	UNI decode direction. 0: MSB first. 1: LSB first.	
	UNI_DECODE_EN	0	UNI decode enable.	
A8h	**REGA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_DELAY0[7:0]	7:0	UNI decode delay0.	
ACh	**REGAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_DELAY1[7:0]	7:0	UNI decode delay1.	
B0h	**REGB0**	**7:0**	**Default : 0x1C**	**Access : R/W**
	UNI_DECODE_TIME_REC_EN	7	UNI decode timing recovery enable.	
	UNI_DECODE_SOF_THD[6:0]	6:0	UNI decode SOF detect threshold.	
B4h	**REGB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_SOF_MASK0[7:0]	7:0	UNI decode SOF mask 0.	
B8h	**REGB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_SOF_MASK1[7:0]	7:0	UNI decode SOF mask 1.	
BCh	**REGBC**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_SOF_MASK2[7:0]	7:0	UNI decode SOF mask 2.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
C0h	**REGC0**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_SOF_MASK3[7:0]	7:0	UNI decode SOF mask 3.	
C4h	**REGC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_BIT0_MASK0[7:0]	7:0	UNI decode bit0 mask 0.	
C8h	**REGC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_BIT0_MASK1[7:0]	7:0	UNI decode bit0 mask 1.	
CCh	**REGCC**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_BIT0_MASK2[7:0]	7:0	UNI decode bit0 mask 2.	
D0h	**REGD0**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_BIT0_MASK3[7:0]	7:0	UNI decode bit0 mask 3.	
D4h	**REGD4**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_BIT1_MASK0[7:0]	7:0	UNI decode bit1 mask 0.	
D8h	**REGD8**	**7:0**	**Default : 0xAA**	**Access : R/W**
	UNI_DECODE_BIT1_MASK1[7:0]	7:0	UNI decode bit1 mask 1.	
DCh	**REGDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_BIT1_MASK2[7:0]	7:0	UNI decode bit1 mask 2.	
E0h	**REGE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_BIT1_MASK3[7:0]	7:0	UNI decode bit1 mask 3.	
E4h	**REGE4**	**7:0**	**Default : 0x7F**	**Access : R/W**
	SDD106_FDT_DELAY[7:0]	7:0	Single device detection 106K FDT delay time (8'h7F: meet spec.).	
E8h	**REGE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_PHASE_EN	7	UNI decode phase detect enable.	
	UNI_DECODE_DAT_IDX[6:4]	6:4	UNI data correlation bit index. 000: 4 bits. 001: 8 bits. 010: 12 bits. 011: 16 bits. 100: 20 bits. 101: 24 bits. 110: 28 bits. 111: 32 bits.	
	DECODE_LEN1[3:0]	3:0	Decode length1 for UNI_DECODE (write) & UNI_DECODE & MM_DECODE.	
ECh	**REGEC**	**7:0**	**Default : 0x00**	**Access : R/W**

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	DECODE_LEN0[7:0]	7:0	Decode length0 for UNI_DECODE (write) & UNI_DECODE & MM_DECODE.	
F0h	**REGF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_TRX[7:0]	7:0	TEST_TRX value for analog TRX_TOP setting.	
F4h	**REGF4**	**7:0**	**Default : 0x41**	**Access : R/W**
	SDD43B_PTLINFO0[7:0]	7:0	Single device detection 43B Protocol Information0.	
F8h	**REGF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PTLINFO1[7:0]	7:0	Single device detection 43B Protocol Information1.	
FCh	**REGFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PTLINFO2[7:0]	7:0	Single device detection 43B Protocol Information2 (1st byte).	
100h	**REG100**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PUPI0[7:0]	7:0	Single device detection 43B PUPI0.	
104h	**REG104**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PUPI1[7:0]	7:0	Single device detection 43B PUPI1.	
108h	**REG108**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PUPI2[7:0]	7:0	Single device detection 43B PUPI2.	
10Ch	**REG10C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_PUPI3[7:0]	7:0	Single device detection 43B PUPI3 (1st byte).	
110h	**REG110**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_APPDAT0[7:0]	7:0	Single device detection 43B Application Data0.	
114h	**REG114**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_APPDAT1[7:0]	7:0	Single device detection 43B Application Data1.	
118h	**REG118**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_APPDAT2[7:0]	7:0	Single device detection 43B Application Data2.	
11Ch	**REG11C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD43B_APPDAT3[7:0]	7:0	Single device detection 43B Application Data3 (1st byte).	
120h	**REG120**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDD43B_COMP_CLR	4	Single device detection 43B complete clear.	
	SDD43B_COMP	3	Single device detection 43B complete.	
	SDD43B_HALT_SDD	2	Set Single device detection 43B to Halt state.	
	SDD43B_CLR	1	Clear Single device detection 43B.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SDD43B_EN	0	Single device detection 43B enable.	
124h	**REG124**	**7:0**	**Default : 0x02**	**Access : R/W**
	SDD106_ATQA0[7:0]	7:0	Single device detection 106K ATQA0.	
128h	**REG128**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD106_ATQA1[7:0]	7:0	Single device detection 106K ATQA1.	
12Ch	**REG12C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD106_SAK[7:0]	7:0	Single device detection 106K SAK.	
130h	**REG130**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NRZ_DECODE_DONE	7	NRZ decode done.	
	-	6:5	Reserved.	
	NRZ_DECODE_EN	4	NRZ decode enable.	
	MAN_DECODE_DONE	3	Manchester decode done.	
	MAN_DECODE_SIGN	2	Manchester decode sign. 0: Reverse. 1: Observe.	
	MAN_DECODE_CRC_PASS	1	Manchester decode CRC check pass.	
	MAN_DECODE_TIME_REC_EN	0	Manchester decode timing recovery enable.	
134h	**REG134**	**7:0**	**Default : 0x3A**	**Access : R/W**
	MAN_DECODE_THRSHD[7:0]	7:0	Manchester decode packet detect threshold.	
138h	**REG138**	**7:0**	**Default : 0x00**	**Access : RO**
	MAN_DECODE_CRC0[7:0]	7:0	Manchester decode CRC0.	
13Ch	**REG13C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAN_DECODE_CRC1[7:0]	7:0	Manchester decode CRC1.	
140h	**REG140**	**7:0**	**Default : 0x00**	**Access : RO**
	RN32_0[7:0]	7:0	TRNG32 byte0.	
144h	**REG144**	**7:0**	**Default : 0x00**	**Access : RO**
	RN32_1[7:0]	7:0	TRNG32 byte1.	
148h	**REG148**	**7:0**	**Default : 0x00**	**Access : RO**
	RN32_2[7:0]	7:0	TRNG32 byte2.	
14Ch	**REG14C**	**7:0**	**Default : 0x00**	**Access : RO**
	RN32_3[7:0]	7:0	TRNG32 byte3.	
150h	**REG150**	**7:0**	**Default : 0x00**	**Access : R/W**
	ENCODE_LEN0[7:0]	7:0	Encoder length0.	
154h	**REG154**	**7:0**	**Default : 0x00**	**Access : R/W**

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	ENCODE_LEN1[3:0]	3:0	Encoder length1.	
158h	**REG158**	**7:0**	**Default : 0x84**	**Access : RO, R/W**
	TIMER_CLK13M_SEL	7	Tag mode timer clock select (TX_ENCODE_TIMER, TX106_ENCODE_TIMER). 0: Clock from crystal. 1: Clock from field.	
	SDD106_COMP3	6	SDD106 CLT complete.	
	MANSUB106_ENCODE_CRC_EN	5	Manchester with subcarrier 106K encode CRC enable.	
	MANSUB106_ENCODE_EN	4	Manchester with subcarrier 106K encode enable.	
	MANSUB106_ENCODE_MODE	3	Manchester with subcarrier 106K encode mode. 0: ISO14443A mode. 1: CLT mode.	
	MAN_ENCODE_SIGN	2	Manchester encode sign. 0: Reverse. 1: Observe.	
	-	1	Reserved.	
	MAN_ENCODE_EN	0	Manchester encode enable.	
15Ch	**REG15C**	**7:0**	**Default : 0xE8**	**Access : RO, R/W**
	BPSK_ENCODE_SOF_EN	7	1: NRZ BPSK encode SOF enable.	
	BPSK_ENCODE_EOF_EN	6	1: NRZ BPSK encode EOF enable.	
	BPSK_ENCODE_TR0_EN	5	1: NRZ BPSK encode TR0 enable.	
	BPSK_ENCODE_EN	4	NRZ BPSK encode enable.	
	MM_DECODE_AUTO_SYNC	3	Modify Miller decode auto sync.	
	MM_DECODE_PARITY_ERROR	2	Modify Miller decode parity error indicator.	
	PPM_ENCODE_SEL	1	PPM encode select (enable with PPM_ENCODE_MODE=0). 0: PPM4. 1: PPM256.	
	PPM_ENCODE_EN	0	PPM encode enable.	
160h	**REG160**	**7:0**	**Default : 0x00**	**Access : R/W**
	MM_ENCODE_CLKSEL[7:6]	7:6	MM encode clock select (fs). 00: Fc/16 (106K). 01: Fc/8 (212K). 10: Fc/4 (424K). 11: Fc/2 (848K).	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	MM_ENCODE_CRC_EN	5	Modify Miller encode CRC enable.	
	MM_ENCODE_EN	4	Modify Miller encode enable.	
	MM_ENCODE_MODE	3	MM encode protocol select. 0: ISO1443A mode. 1: Topaz mode (MM_ENCODE_CLKSEL=2'b11).	
	PPM_ENCODE_MODE	2	PPM encode mode. 0: PPM4/256 encode. 1: EOF encode.	
	TX_ENCODE_DLY_EN	1	Transmit (encode) delay timer enable.	
	RX_DECODE_DLY_EN	0	Receive (decode) delay timer enable.	
164h	**REG164**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_DECODE_DLY0[7:0]	7:0	Receive (decode) delay time0 (count by clk1356).	
168h	**REG168**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_DECODE_DLY1[7:0]	7:0	Response (decode) delay time1.	
16Ch	**REG16C**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_BIT_CYCLE[7:0]	7:0	UNI decode bit cycle (fs).	
170h	**REG170**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	RX_SYNC_SAMPLE_POS[2:0]	2:0	RX sync sample position.	
174h	**REG174**	**7:0**	**Default : 0x7E**	**Access : R/W**
	UNI_DECODE_EOF_THD[7:0]	7:0	UNI decode EOF detect threshold.	
178h	**REG178**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	UNI_DECODE_EOF_IDX[1:0]	1:0	UNI decode EOF mask index. 00: 128 bits EOF mask (EOF_MASK[3:0]). 01: 96 bits EOF mask (EOF_MASK[2:0]). 10: 64 bits EOF mask (EOF_MASK[1:0]). 11: 32 bits EOF mask (EOF_MASK[0]).	
17Ch	**REG17C**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK0_0[7:0]	7:0	UNI decode EOF mask 0_0.	
180h	**REG180**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK0_1[7:0]	7:0	UNI decode EOF mask 0_1.	
184h	**REG184**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK0_2[7:0]	7:0	UNI decode EOF mask 0_2.	
188h	**REG188**	**7:0**	**Default : 0x00**	**Access : R/W**

NFC Register

Index	Mnemonic	Bit	Description	
	UNI_DECODE_EOF_MASK0_3[7:0]	7:0	UNI decode EOF mask 0_3.	
18Ch	**REG18C**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK1_0[7:0]	7:0	UNI decode EOF mask 1_0.	
190h	**REG190**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK1_1[7:0]	7:0	UNI decode EOF mask 1_1.	
194h	**REG194**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK1_2[7:0]	7:0	UNI decode EOF mask 1_2.	
198h	**REG198**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK1_3[7:0]	7:0	UNI decode EOF mask 1_3.	
19Ch	**REG19C**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK2_0[7:0]	7:0	UNI decode EOF mask 2_0.	
1A0h	**REG1A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK2_1[7:0]	7:0	UNI decode EOF mask 2_1.	
1A4h	**REG1A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK2_2[7:0]	7:0	UNI decode EOF mask 2_2.	
1A8h	**REG1A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK2_3[7:0]	7:0	UNI decode EOF mask 2_3.	
1ACh	**REG1AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK3_0[7:0]	7:0	UNI decode EOF mask 3_0.	
1B0h	**REG1B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK3_1[7:0]	7:0	UNI decode EOF mask 3_1.	
1B4h	**REG1B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK3_2[7:0]	7:0	UNI decode EOF mask 3_2.	
1B8h	**REG1B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	UNI_DECODE_EOF_MASK3_3[7:0]	7:0	UNI decode EOF mask 3_3.	
1BCh	**REG1BC**	**7:0**	**Default : 0x00**	**Access : RO**
	SDD24_SLOT[7:4]	7:4	SDD24 response slot.	
	SDD43B_SLOT[3:0]	3:0	SDD43B response slot.	
1C0h	**REG1C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32I_DLY0[7:0]	7:0	Idle32i delay time0 (interrupt) (count by clk1356).	
1C4h	**REG1C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32I_DLY1[7:0]	7:0	Idle32i delay time1.	
1C8h	**REG1C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32I_DLY2[7:0]	7:0	Idle32i delay time2.	

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Index	**Mnemonic**	**Bit**	**Description**	
1CCh	**REG1CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32I_DLY3[7:0]	7:0	Idle32i delay time3.	
1D0h	**REG1D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32_DLY0[7:0]	7:0	Idle32 delay time0 (count by clk1356).	
1D4h	**REG1D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32_DLY1[7:0]	7:0	Idle32 delay time1.	
1D8h	**REG1D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32_DLY2[7:0]	7:0	Idle32 delay time2.	
1DCh	**REG1DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDLE32_DLY3[7:0]	7:0	Idle32 delay time3.	
1E0h	**REG1E0**	**7:0**	**Default : 0x0F**	**Access : R/W**
	BPSK_ENCODE_TR0_DELAY0[7:0]	7:0	NRZ BPSK encode TR0 delay time0 (ETU).	
1E4h	**REG1E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	BPSK_ENCODE_TR0_DELAY1[7:0]	7:0	NRZ BPSK encode TR0 delay time1 (ETU).	
1E8h	**REG1E8**	**7:0**	**Default : 0x0B**	**Access : R/W**
	BPSK_ENCODE_TR1_DELAY0[7:0]	7:0	NRZ BPSK encode TR1 delay time0 (ETU).	
1ECh	**REG1EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	BPSK_ENCODE_TR1_DELAY1[7:0]	7:0	NRZ BPSK encode TR1 delay time1 (ETU).	
1F0h	**REG1F0**	**7:0**	**Default : 0x5A**	**Access : R/W**
	TRX2[7:0]	7:0	TRX2. Bit[7]: HYS_COMP. Bit[6]: HBWNOF. Bit[5]: HBW. Bit[4:3]: PEAKAC. Bit[2:1]: NOFAC. Bit[0]: PD_NOF.	
1F4h	**REG1F4**	**7:0**	**Default : 0x40**	**Access : R/W**
	MM_TCLK_INV	7	Invert MM_ENCODE clock (MM_ENCODE).	
	MM_TCLK_GAT	6	Gate MM_ENCODE clock (MM_ENCODE).	
	SDD106_RCLK_INV	5	Invert SDD106 RX clock (MM_DECODE).	
	SDD106_RCLK_GAT	4	Gate SDD106 RX clock (MM_DECODE).	
	SDD106_TCLK_INV	3	Invert SDD106 TX clock (MANSUB106_ENCODE).	
	SDD106_TCLK_GAT	2	Gate SDD106 TX clock (MANSUB106_ENCODE).	
	SDD106_CCLK_INV	1	Invert SDD106 ctrl clock (SDD106_CTRL).	
	SDD106_CCLK_GAT	0	Gate SDD106 ctrl clock (SDD106_CTRL).	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
1F8h	**REG1F8**	**7:0**	**Default : 0x55**	**Access : R/W**
	TRNG_CLK_INV	7	Invert TRNG clock (TRNG).	
	TRNG_CLK_GAT	6	Gate TRNG clock (TRNG).	
	SDD43B_RCLK_INV	5	Invert SDD43B RX clock (NRZ_DECODE).	
	SDD43B_RCLK_GAT	4	Gate SDD43B RX clock (NRZ_DECODE).	
	SDD43B_TCLK_INV	3	Invert SDD43B TX clock (NRZ_BPSK_ENCODE).	
	SDD43B_TCLK_GAT	2	Gate SDD43B TX clock (NRZ_BPSK_ENCODE).	
	SDD43B_CCLK_INV	1	Invert SDD43B ctrl clock (SDD43B_CTRL).	
	SDD43B_CCLK_GAT	0	Gate SDD43B ctrl clock (SDD43B_CTRL).	
1FCh	**REG1FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MM_DECODE_SPDSEL[7:6]	7:6	SDD106 MM_DECODE speed select. 00: 106K. 01: 212K. 10: 424K. 11: 848K.	
	MANSUB106_ENCODE_SPDSEL[5:4]	5:4	SDD106 MANSUB106_ENCODE speed select. 00: 106K. 01: 212K. 10: 424K. 11: 848K.	
	NRZ_DECODE_SPDSEL[3:2]	3:2	SDD43B NRZ_DECODE speed select. 00: 106K. 01: 212K. 10: 424K. 11: 848K.	
	NRZ_BPSK_ENCODE_SPDSEL[1:0]	1:0	SDD43B NRZ_BPSK_ENCODE speed select. 00: 106K. 01: 212K. 10: 424K. 11: 848K.	
200h	**REG200**	**7:0**	**Default : 0x87**	**Access : R/W**
	MM_DECODE_LENGTH_MODE	7	MM_DECODE length mode. 0: Normal mode report bits with parity. 1: Normal mode report bits without parity. CLT mode report bits are always with parity (which are don't care bits).	
	MM_DECODE_MODE	6	MM_DECODE mode. 0: Normal mode (decode report without parity).	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
			1: CLT mode (decode report with parity).	
	IDLE32I_MODE	5	Idle32i delay timer mode. 0: One-shot mode. 1: Auto-reload mode.	
	IDLE32_MODE	4	Idle32 delay timer mode. 0: One-shot mode. 1: Auto-reload mode.	
	MM_DECODE_PACKET_DELAY[3:0]	3:0	MM_DECODE packet detection sample delay.	
204h	**REG204**	**7:0**	**Default : 0x40**	**Access : R/W**
	MM_DECODE_FDT_OFFSET[7:0]	7:0	MM_DECODE FDT delay offset for last bit equal '1'.	
208h	**REG208**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_ENCODE_DLY0[7:0]	7:0	Transmit (encode) encode delay Time0 (count by clk1356).	
20Ch	**REG20C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_ENCODE_DLY1[7:0]	7:0	Transmit (encode) encode delay Time1.	
210h	**REG210**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_ENCODE_DLY2[7:0]	7:0	Transmit (encode) encode delay Time2.	
214h	**REG214**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_ENCODE_DLY3[7:0]	7:0	Transmit (encode) encode delay Time3.	
218h	**REG218**	**7:0**	**Default : 0x54**	**Access : R/W**
	TX106_ENCODE_DLY_EN	7	ManSub106 encode delay Time enable (SDD106 auto delay).	
	TX106_ENCODE_DLY[6:0]	6:0	ManSub106 encode delay Time (SDD106 auto delay) (TX106_ENCODE_DLY).	
21Ch	**REG21C**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32I_COUNT0[7:0]	7:0	Idle32i count0 (interrupt).	
220h	**REG220**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32I_COUNT1[7:0]	7:0	Idle32i count1.	
224h	**REG224**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32I_COUNT2[7:0]	7:0	Idle32i count2.	
228h	**REG228**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32I_COUNT3[7:0]	7:0	Idle32i count3.	
22Ch	**REG22C**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32_COUNT0[7:0]	7:0	Idle32 count0.	
230h	**REG230**	**7:0**	**Default : 0x00**	**Access : RO**

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	IDLE32_COUNT1[7:0]	7:0	Idle32 count1.	
234h	**REG234**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32_COUNT2[7:0]	7:0	Idle32 count2.	
238h	**REG238**	**7:0**	**Default : 0x00**	**Access : RO**
	IDLE32_COUNT3[7:0]	7:0	Idle32 count3.	
23Ch	**REG23C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RFDET_DEBN_DISABLE	7	RF detection debounce (interrupt) disable.	
	RFDET_DEBN_PERIOD[6:0]	6:0	RF detection debounce period (count with clkdiv2).	
240h	**REG240**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_INDICATOR0[7:0]	7:0	Interrupt indicator0. Bit[7]: MM_ENCODE_INDICATOR. Bit[6]: MANSUB106_ENCODE_INDICATOR. Bit[5]: MAN_ENCODE_INDICATOR. Bit[4]: NRZ_BPSK_ENCODE_INDICATOR. Bit[3]: PPM_ENCODE_INDICATOR. Bit[2]: CB_ENCODE_INDICATOR. Bit[1]: SDD24_INDICATOR. Bit[0]: SDD43B_INDICATOR.	
244h	**REG244**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_MASK0[7:0]	7:0	Interrupt mask0 (0: mask). Bit[7]: MM_ENCODE_MASK. Bit[6]: MANSUB106_ENCODE_MASK. Bit[5]: MAN_ENCODE_MASK. Bit[4]: NRZ_BPSK_ENCODE_MASK. Bit[3]: PPM_ENCODE_MASK. Bit[2]: CB_ENCODE_MASK. Bit[1]: SDD24_MASK. Bit[0]: SDD43B_MASK.	
248h	**REG248**	**7:0**	**Default : 0x04**	**Access : R/W**
	SDD106_CLT_SIM_MODE	7	SDD106 CLT SIM card mode. 0: Gemalto (0x60, 0x61, 0x3000). 1: All mifare mode (0x60, 0x61, 0x30, 0xA0, 0xC0, 0xC1, 0xC2, 0xB0).	
	SDD106_CLT_ADV_ENABLE	6	SDD106 CLT mode advance command enable (not listed in mifare command set). 0: Disable. 1: Enable (SDD106_CLT_SIM_MODE no function).	
	SDD106_RATS_CLR	5	SDD106 RATS command get and clear decode enable.	

NFC Register

Index	Mnemonic	Bit	Description	
	SDD106_CLT_ENABLE	4	SDD106 CLT mode enable.	
	NRZ_DECODE_PACKET_DELAY[3:0]	3:0	NRZ_DECODE packet detection sample delay.	
250h	**REG250**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MM_DECODE_FDT_DELAY1	0	MM_DECODE fdt delay1.	
254h	**REG254**	**7:0**	**Default : 0x33**	**Access : R/W**
	MM_DECODE_FDT_DELAY0[7:0]	7:0	MM_DECODE fdt delay0.	
258h	**REG258**	**7:0**	**Default : 0x10**	**Access : R/W**
	TRX3[7:0]	7:0	TRX3. Bit[7:4]: HYS_TAGDEM. Bit[3:2]: SEL_CLPF. Bit[1:0]: SEL_CENV.	
25Ch	**REG25C**	**7:0**	**Default : 0x15**	**Access : R/W**
	-	7:6	Reserved.	
	SDD24_RCLK_INV	5	Invert SDD24 RX clock (MAN_DECODE).	
	SDD24_RCLK_GAT	4	Gate SDD24 RX clock (MAN_DECODE).	
	SDD24_TCLK_INV	3	Invert SDD24 TX clock (MAN_ENCODE).	
	SDD24_TCLK_GAT	2	Gate SDD24 TX clock (MAN_ENCODE).	
	SDD24_CCLK_INV	1	Invert SDD24 ctrl clock (SDD24_CTRL).	
	SDD24_CCLK_GAT	0	Gate SDD24 ctrl clock (SDD24_CTRL).	
260h	**REG260**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_INDICATOR1[7:0]	7:0	Interrupt indicator1. Bit[7]: MM_DECODE_INDICATOR. Bit[6]: MAN_DECODE_INDICATOR. Bit[5]: NRZ_DECODE_INDICATOR. Bit[4]: UNI_DECODE_INDICATOR. Bit[3]: SDD106_COMP1_INDICATOR. Bit[2]: SDD106_COMP2_INDICATOR. Bit[1]: SDD106_COMP3_INDICATOR. Bit[0]: RFDET_INDICATOR.	
264h	**REG264**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_MASK1[7:0]	7:0	Interrupt mask1 (0: mask). Bit[7]: MM_DECODE_MASK. Bit[6]: MAN_DECODE_MASK. Bit[5]: NRZ_DECODE_MASK. Bit[4]: UNI_DECODE_MASK. Bit[3]: SDD106_COMP1_MASK.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
			Bit[2]: SDD106_COMP2_MASK. Bit[1]: SDD106_COMP3_NEG_MASK. Bit[0]: SDD106_COMP3_POS_MASK.	
268h	**REG268**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	INT_MASK2[2:0]	2:0	Interrupt mask2 (0: mask). Bit[2]: IDLE32I_MASK. Bit[1]: RFDET_POS_MASK. Bit[0]: RFDET_NEG_MASK.	
26Ch	**REG26C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_INDICATOR_CLR[7:2]	7:2	Interrupt indicator clear (1: clear). Bit[7]: MM_ENCODE_INDICATOR clear. Bit[6]: MANSUB106_ENCODE_INDICATOR clear. Bit[5]: MAN_ENCODE_INDICATOR clear. Bit[4]: NRZ_BPSK_ENCODE_INDICATOR clear. Bit[3]: PPM_ENCODE_INDICATOR clear. Bit[2]: CB_ENCODE_INDICATOR clear.	
	-	1:0	Reserved.	
270h	**REG270**	**7:0**	**Default : 0x05**	**Access : R/W**
	TRX4[7:0]	7:0	TRX4. Bit[3]: SEL_DOUT. Bit[2]: PWR_TAGDEM. Bit[1:0]: PWR_CLKRCV.	
274h	**REG274**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD24_TD_DELAY1[7:0]	7:0	SDD24 td delay1 (count by fc).	
278h	**REG278**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD24_TD_DELAY0[7:0]	7:0	SDD24 td delay0 (count by fc).	
27Ch	**REG27C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD24_TS_DELAY1[7:0]	7:0	SDD24 ts delay1 (count by fc).	
280h	**REG280**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDD24_TS_DELAY0[7:0]	7:0	SDD24 ts delay0 (count by fc).	
300h	**REG300**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CRYPTO_CLKSEL[5:4]	5:4	Crypto clock select. 00: Clk1356. 01: Clkdiv2. 10: Clkdiv4.	

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
			11: Clkdiv8.	
	-	3:2	Reserved.	
	PRNG_EN	1	Prng enable.	
	PRNG_INIT	0	Prng load initial value.	
301h	**REG301**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRNG_INIT_DATA3[7:0]	7:0	Prng initial data3.	
302h	**REG302**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRNG_INIT_DATA2[7:0]	7:0	Prng initial data2.	
303h	**REG303**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRNG_INIT_DATA1[7:0]	7:0	Prng initial data1.	
304h	**REG304**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRNG_INIT_DATA0[7:0]	7:0	Prng initial data0.	
305h	**REG305**	**7:0**	**Default : 0x00**	**Access : RO**
	PRNG_OUT3[7:0]	7:0	Prng output data3.	
306h	**REG306**	**7:0**	**Default : 0x00**	**Access : RO**
	PRNG_OUT2[7:0]	7:0	Prng output data2.	
307h	**REG307**	**7:0**	**Default : 0x00**	**Access : RO**
	PRNG_OUT1[7:0]	7:0	Prng output data1.	
308h	**REG308**	**7:0**	**Default : 0x00**	**Access : RO**
	PRNG_OUT0[7:0]	7:0	Prng output data0.	
309h	**REG309**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	KSGEN_FEEDBACK_EN	5	Ksgen data feedback enable.	
	KSGEN_INJECT_EN	4	Ksgen data injection enable.	
	-	3:2	Reserved.	
	KSGEN_EN	1	Ksgen enable.	
	KSGEN_INIT	0	Ksgen load initial value.	
30Ah	**REG30A**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_KEY5[7:0]	7:0	Ksgen key5 (KeyA/B).	
30Bh	**REG30B**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_KEY4[7:0]	7:0	Ksgen key4 (KeyA/B).	
30Ch	**REG30C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_KEY3[7:0]	7:0	Ksgen key3 (KeyA/B).	
30Dh	**REG30D**	**7:0**	**Default : 0x00**	**Access : R/W**

NFC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	KSGEN_KEY2[7:0]	7:0	Ksgen key2 (KeyA/B).	
30Eh	**REG30E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_KEY1[7:0]	7:0	Ksgen key1 (KeyA/B).	
30Fh	**REG30F**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_KEY0[7:0]	7:0	Ksgen key0 (KeyA/B).	
310h	**REG310**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_DATA3[7:0]	7:0	Ksgen injection data3.	
311h	**REG311**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_DATA2[7:0]	7:0	Ksgen injection data2.	
312h	**REG312**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_DATA1[7:0]	7:0	Ksgen injection data1.	
313h	**REG313**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_DATA0[7:0]	7:0	Ksgen injection data0.	
314h	**REG314**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRNG_LEN[7:0]	7:0	Prng operation length.	
315h	**REG315**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSGEN_LEN[7:0]	7:0	Ksgen operation length.	

SWP_LOGIC Register

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**REG00**	**7:0**	**Default : 0x04**	**Access : R/W**
	CKG_SWP_BITCLK[3:0]	7:4	SWP bit clock setting. Bit 3~2: Select clock source. 00,01,10: Select SWP_BIT_CLK. 11: Select xtal clock. Bit 1: Invert clock. Bit 0: Disable clock.	
	SWP_BIT_RATE[2:0]	3:1	SWP bit rate. 000: Fc/8. 001: Fc/16. 010: Fc/32. 011: Fc/64. 100: Fc/128. 101: Fc/256. 110: Fc/512. 111: Fc/1024.	
	SWP_TX_EN	0	SWP TX enable.	
01h	**REG01**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_DATA3_READY_CLR	7	Clear TX data3.	
	TX_DATA2_READY_CLR	6	Clear TX data2.	
	TX_DATA1_READY_CLR	5	Clear TX data1.	
	TX_DATA0_READY_CLR	4	Clear TX data0.	
	TX_DATA_READY[3:0]	3:0	SWP TX data0~3 ready.	
02h	**REG02**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TYPEA_ALIGN_TX	7	Structure of DATA_FIELD in CLT PAYLOAD. 1: TX Data structure Type A aligned. 0: TX Data structure is byte aligned.	
	TYPEA_ALIGN_RX	6	Structure of DATA_FIELD in CLT PAYLOAD. 1: RX Data structure Type A aligned. 0: RX Data structure Byte aligned.	
	ACT_FR	5	ACT FR in ACT LLC control field.	
	ACT_INF	4	ACT INF in ACT LLC control field.	
	ACT_CTRL[2:0]	3:1	ACT Control in ACT LLC control field.	
	ACT_READY	0	ACT READY, sent from UICC to CLF.	
03h	**REG03**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SWP_RXCLK[3:0]	7:4	SWP RX clock setting.	

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
			Bit 3~2: Select clock source. 00,01,10: Select SWP_RX_CLK. 11: Select xtal clock. Bit 1: Invert clock. Bit 0: Disable clock.	
	CKG_SWP_TXCLK[3:0]	3:0	SWP TX clock setting. Bit 3~2: Select clock source. 00,01,10: Select SWP_TX_CLK. 11: Select xtal clock. Bit 1: Invert clock. Bit 0: Disable clock.	
04h	**REG04**	**7:0**	**Default : 0x01**	**Access : R/W**
	ACT_POWER_MODE[7:0]	7:0	ACT power mode. 00: Low power mode. 01: Full power mode. Others: Reserved.	
05h	**REG05**	**7:0**	**Default : 0x00**	**Access : RO**
	ACT_SYNC_ID0[7:0]	7:0	ACT SYNC ID0, sent from UICC to CLF.	
06h	**REG06**	**7:0**	**Default : 0x00**	**Access : RO**
	ACT_SYNC_ID1[7:0]	7:0	ACT SYNC ID1, sent from UICC to CLF.	
07h	**REG07**	**7:0**	**Default : 0x28**	**Access : R/W**
	ACT_VERIFY_ID0[7:0]	7:0	ACT verification data0, stored in CLF.	
08h	**REG08**	**7:0**	**Default : 0x60**	**Access : R/W**
	ACT_VERIFY_ID1[7:0]	7:0	ACT verification data1, stored in CLF.	
09h	**REG09**	**7:0**	**Default : 0x00**	**Access : RO**
	ACT_INFORMATION[7:0]	7:0	ACT INFORMATION field. Bit 0: SWP bit duration up to 10us supported. Bit 1: SWP bit duration down to 590ns supported. Bit 7~2: Reserved.	
0Ah	**REG0A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	DECODE_DELAY	7	Delay one clock of SWP decode strobe.	
	DEACTIVATE	6	Software DEACTIVATE SWP.	
	SWP_STATE[3:0]	5:2	SWP current finite state machine.	
	ACT_SYNC_FAIL	1	ACT SYNC_ID verification fail.	
	ACT_SYNC_FINISH	0	ACT SYNC_ID verification finish.	
0Bh	**REG0B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

SWP_LOGIC Register

Index	Mnemonic	Bit	Description	
	SWP_CLT_INIT	7	SWP CLT init enable.	
	SWP_TX_STOP	6	SWP TX stop enable.	
	ACT_ALL_FINISH	5	ACT SYNC_ID verification finish in low power mode and ACT ready finish in full power mode.	
	SWP_TIMER_EN[4:0]	4:0	SWP timer 0~4 enable.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_T0_LENGTH[7:0]	7:0	SWP timer 0 length.	
0Dh	**REG0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_T1_LENGTH[7:0]	7:0	SWP timer 1 length.	
0Eh	**REG0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_T2_LENGTH[7:0]	7:0	SWP timer 2 length.	
0Fh	**REG0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_T3_LENGTH[7:0]	7:0	SWP timer 3 length.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_T4_LENGTH[7:0]	7:0	SWP timer 4 length.	
11h	**REG11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RXCRC_FORCE_HI	5	SWP RX CRC force high enable.	
	TXCRC_FORCE_HI	4	SWP TX CRC force high enable.	
	SWP_RX_RATE[2:0]	3:1	SWP RX sample rate. 000: Fc. 001: Fc/2. 010: Fc/4. 011: Fc/8. 100: Fc/16. 101: Fc/32. 110: Fc/64. 111: Fc/128.	
	SWP_RX_EN	0	SWP RX enable, cleared by hardware.	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_CRC16_FAIL	7	SWP RX7 CRC16 fail.	
	SWP_RX6_CRC16_FAIL	6	SWP RX6 CRC16 fail.	
	SWP_RX5_CRC16_FAIL	5	SWP RX5 CRC16 fail.	
	SWP_RX4_CRC16_FAIL	4	SWP RX4 CRC16 fail.	
	SWP_RX3_CRC16_FAIL	3	SWP RX3 CRC16 fail.	

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX2_CRC16_FAIL	2	SWP RX2 CRC16 fail.	
	SWP_RX1_CRC16_FAIL	1	SWP RX1 CRC16 fail.	
	SWP_RX_CRC16_FAIL	0	SWP RX CRC16 fail.	
13h	**REG13**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA7_READY	7	RX data7 buffer ready.	
	DATA6_READY	6	RX data6 buffer ready.	
	DATA5_READY	5	RX data5 buffer ready.	
	DATA4_READY	4	RX data4 buffer ready.	
	DATA3_READY	3	RX data3 buffer ready.	
	DATA2_READY	2	RX data2 buffer ready.	
	DATA1_READY	1	RX data1 buffer ready.	
	DATA_READY	0	RX data buffer ready.	
14h	**REG14**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATA7_CLR	7	Clear RX7 length, ready and data.	
	DATA6_CLR	6	Clear RX6 length, ready and data.	
	DATA5_CLR	5	Clear RX5 length, ready and data.	
	DATA4_CLR	4	Clear RX4 length, ready and data.	
	DATA3_CLR	3	Clear RX3 length, ready and data.	
	DATA2_CLR	2	Clear RX2 length, ready and data.	
	DATA1_CLR	1	Clear RX1 length, ready and data.	
	DATA_CLR	0	Clear RX length, ready and data.	
15h	**REG15**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH7[7:0]	7:0	SWP RX bit length7.	
16h	**REG16**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH6[7:0]	7:0	SWP RX bit length6.	
17h	**REG17**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH5[7:0]	7:0	SWP RX bit length5.	
18h	**REG18**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH4[7:0]	7:0	SWP RX bit length4.	
19h	**REG19**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH3[7:0]	7:0	SWP RX bit length3.	
1Ah	**REG1A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH2[7:0]	7:0	SWP RX bit length2.	
1Bh	**REG1B**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_BIT_LENGTH1[7:0]	7:0	SWP RX bit length1.	
1Ch	**REG1C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_BIT_LENGTH[7:0]	7:0	SWP RX bit length.	
1Dh	**REG1D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA0[7:0]	7:0	SWP RX data port 0.	
1Eh	**REG1E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA1[7:0]	7:0	SWP RX data port 1.	
1Fh	**REG1F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA2[7:0]	7:0	SWP RX data port 2.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA3[7:0]	7:0	SWP RX data port 3.	
21h	**REG21**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA4[7:0]	7:0	SWP RX data port 4.	
22h	**REG22**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA5[7:0]	7:0	SWP RX data port 5.	
23h	**REG23**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA6[7:0]	7:0	SWP RX data port 6.	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA7[7:0]	7:0	SWP RX data port 7.	
25h	**REG25**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA8[7:0]	7:0	SWP RX data port 8.	
26h	**REG26**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA9[7:0]	7:0	SWP RX data port 9.	
27h	**REG27**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA10[7:0]	7:0	SWP RX data port 10.	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA11[7:0]	7:0	SWP RX data port 11.	
29h	**REG29**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA12[7:0]	7:0	SWP RX data port 12.	
2Ah	**REG2A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA13[7:0]	7:0	SWP RX data port 13.	
2Bh	**REG2B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA14[7:0]	7:0	SWP RX data port 14.	
2Ch	**REG2C**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX_DATA15[7:0]	7:0	SWP RX data port 15.	
2Dh	**REG2D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA16[7:0]	7:0	SWP RX data port 16.	
2Eh	**REG2E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA17[7:0]	7:0	SWP RX data port 17.	
2Fh	**REG2F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA18[7:0]	7:0	SWP RX data port 18.	
30h	**REG30**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA19[7:0]	7:0	SWP RX data port 19.	
31h	**REG31**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA20[7:0]	7:0	SWP RX data port 20.	
32h	**REG32**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA21[7:0]	7:0	SWP RX data port 21.	
33h	**REG33**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA22[7:0]	7:0	SWP RX data port 22.	
34h	**REG34**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA23[7:0]	7:0	SWP RX data port 23.	
35h	**REG35**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA24[7:0]	7:0	SWP RX data port 24.	
36h	**REG36**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA25[7:0]	7:0	SWP RX data port 25.	
37h	**REG37**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA26[7:0]	7:0	SWP RX data port 26.	
38h	**REG38**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA27[7:0]	7:0	SWP RX data port 27.	
39h	**REG39**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA28[7:0]	7:0	SWP RX data port 28.	
3Ah	**REG3A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX_DATA29[7:0]	7:0	SWP RX data port 29.	
3Bh	**REG3B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA0[7:0]	7:0	SWP RX1 data port 0.	
3Ch	**REG3C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA1[7:0]	7:0	SWP RX1 data port 1.	
3Dh	**REG3D**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX1_DATA2[7:0]	7:0	SWP RX1 data port 2.	
3Eh	**REG3E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA3[7:0]	7:0	SWP RX1 data port 3.	
3Fh	**REG3F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA4[7:0]	7:0	SWP RX1 data port 4.	
40h	**REG40**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA5[7:0]	7:0	SWP RX1 data port 5.	
41h	**REG41**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA6[7:0]	7:0	SWP RX1 data port 6.	
42h	**REG42**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA7[7:0]	7:0	SWP RX1 data port 7.	
43h	**REG43**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA8[7:0]	7:0	SWP RX1 data port 8.	
44h	**REG44**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA9[7:0]	7:0	SWP RX1 data port 9.	
45h	**REG45**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA10[7:0]	7:0	SWP RX1 data port 10.	
46h	**REG46**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA11[7:0]	7:0	SWP RX1 data port 11.	
47h	**REG47**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA12[7:0]	7:0	SWP RX1 data port 12.	
48h	**REG48**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA13[7:0]	7:0	SWP RX1 data port 13.	
49h	**REG49**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA14[7:0]	7:0	SWP RX1 data port 14.	
4Ah	**REG4A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA15[7:0]	7:0	SWP RX1 data port 15.	
4Bh	**REG4B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA16[7:0]	7:0	SWP RX1 data port 16.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA17[7:0]	7:0	SWP RX1 data port 17.	
4Dh	**REG4D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA18[7:0]	7:0	SWP RX1 data port 18.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX1_DATA19[7:0]	7:0	SWP RX1 data port 19.	
4Fh	**REG4F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA20[7:0]	7:0	SWP RX1 data port 20.	
50h	**REG50**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA21[7:0]	7:0	SWP RX1 data port 21.	
51h	**REG51**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA22[7:0]	7:0	SWP RX1 data port 22.	
52h	**REG52**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA23[7:0]	7:0	SWP RX1 data port 23.	
53h	**REG53**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA24[7:0]	7:0	SWP RX1 data port 24.	
54h	**REG54**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA25[7:0]	7:0	SWP RX1 data port 25.	
55h	**REG55**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA26[7:0]	7:0	SWP RX1 data port 26.	
56h	**REG56**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA27[7:0]	7:0	SWP RX1 data port 27.	
57h	**REG57**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA28[7:0]	7:0	SWP RX1 data port 28.	
58h	**REG58**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX1_DATA29[7:0]	7:0	SWP RX1 data port 29.	
59h	**REG59**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA0[7:0]	7:0	SWP RX2 data port 0.	
5Ah	**REG5A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA1[7:0]	7:0	SWP RX2 data port 1.	
5Bh	**REG5B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA2[7:0]	7:0	SWP RX2 data port 2.	
5Ch	**REG5C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA3[7:0]	7:0	SWP RX2 data port 3.	
5Dh	**REG5D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA4[7:0]	7:0	SWP RX2 data port 4.	
5Eh	**REG5E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA5[7:0]	7:0	SWP RX2 data port 5.	
5Fh	**REG5F**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX2_DATA6[7:0]	7:0	SWP RX2 data port 6.	
60h	**REG60**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA7[7:0]	7:0	SWP RX2 data port 7.	
61h	**REG61**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA8[7:0]	7:0	SWP RX2 data port 8.	
62h	**REG62**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA9[7:0]	7:0	SWP RX2 data port 9.	
63h	**REG63**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA10[7:0]	7:0	SWP RX2 data port 10.	
64h	**REG64**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA11[7:0]	7:0	SWP RX2 data port 11.	
65h	**REG65**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA12[7:0]	7:0	SWP RX2 data port 12.	
66h	**REG66**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA13[7:0]	7:0	SWP RX2 data port 13.	
67h	**REG67**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA14[7:0]	7:0	SWP RX2 data port 14.	
68h	**REG68**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA15[7:0]	7:0	SWP RX2 data port 15.	
69h	**REG69**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA16[7:0]	7:0	SWP RX2 data port 16.	
6Ah	**REG6A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA17[7:0]	7:0	SWP RX2 data port 17.	
6Bh	**REG6B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA18[7:0]	7:0	SWP RX2 data port 18.	
6Ch	**REG6C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA19[7:0]	7:0	SWP RX2 data port 19.	
6Dh	**REG6D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA20[7:0]	7:0	SWP RX2 data port 20.	
6Eh	**REG6E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA21[7:0]	7:0	SWP RX2 data port 21.	
6Fh	**REG6F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA22[7:0]	7:0	SWP RX2 data port 22.	
70h	**REG70**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX2_DATA23[7:0]	7:0	SWP RX2 data port 23.	
71h	**REG71**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA24[7:0]	7:0	SWP RX2 data port 24.	
72h	**REG72**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA25[7:0]	7:0	SWP RX2 data port 25.	
73h	**REG73**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA26[7:0]	7:0	SWP RX2 data port 26.	
74h	**REG74**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA27[7:0]	7:0	SWP RX2 data port 27.	
75h	**REG75**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA28[7:0]	7:0	SWP RX2 data port 28.	
76h	**REG76**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX2_DATA29[7:0]	7:0	SWP RX2 data port 29.	
77h	**REG77**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA0[7:0]	7:0	SWP RX3 data port 0.	
78h	**REG78**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA1[7:0]	7:0	SWP RX3 data port 1.	
79h	**REG79**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA2[7:0]	7:0	SWP RX3 data port 2.	
7Ah	**REG7A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA3[7:0]	7:0	SWP RX3 data port 3.	
7Bh	**REG7B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA4[7:0]	7:0	SWP RX3 data port 4.	
7Ch	**REG7C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA5[7:0]	7:0	SWP RX3 data port 5.	
7Dh	**REG7D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA6[7:0]	7:0	SWP RX3 data port 6.	
7Eh	**REG7E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA7[7:0]	7:0	SWP RX3 data port 7.	
7Fh	**REG7F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA8[7:0]	7:0	SWP RX3 data port 8.	
80h	**REG80**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA9[7:0]	7:0	SWP RX3 data port 9.	
81h	**REG81**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX3_DATA10[7:0]	7:0	SWP RX3 data port 10.	
82h	**REG82**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA11[7:0]	7:0	SWP RX3 data port 11.	
83h	**REG83**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA12[7:0]	7:0	SWP RX3 data port 12.	
84h	**REG84**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA13[7:0]	7:0	SWP RX3 data port 13.	
85h	**REG85**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA14[7:0]	7:0	SWP RX3 data port 14.	
86h	**REG86**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA15[7:0]	7:0	SWP RX3 data port 15.	
87h	**REG87**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA16[7:0]	7:0	SWP RX3 data port 16.	
88h	**REG88**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA17[7:0]	7:0	SWP RX3 data port 17.	
89h	**REG89**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA18[7:0]	7:0	SWP RX3 data port 18.	
8Ah	**REG8A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA19[7:0]	7:0	SWP RX3 data port 19.	
8Bh	**REG8B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA20[7:0]	7:0	SWP RX3 data port 20.	
8Ch	**REG8C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA21[7:0]	7:0	SWP RX3 data port 21.	
8Dh	**REG8D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA22[7:0]	7:0	SWP RX3 data port 22.	
8Eh	**REG8E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA23[7:0]	7:0	SWP RX3 data port 23.	
8Fh	**REG8F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA24[7:0]	7:0	SWP RX3 data port 24.	
90h	**REG90**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA25[7:0]	7:0	SWP RX3 data port 25.	
91h	**REG91**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA26[7:0]	7:0	SWP RX3 data port 26.	
92h	**REG92**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX3_DATA27[7:0]	7:0	SWP RX3 data port 27.	
93h	**REG93**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA28[7:0]	7:0	SWP RX3 data port 28.	
94h	**REG94**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX3_DATA29[7:0]	7:0	SWP RX3 data port 29.	
95h	**REG95**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA0[7:0]	7:0	SWP RX4 data port 0.	
96h	**REG96**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA1[7:0]	7:0	SWP RX4 data port 1.	
97h	**REG97**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA2[7:0]	7:0	SWP RX4 data port 2.	
98h	**REG98**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA3[7:0]	7:0	SWP RX4 data port 3.	
99h	**REG99**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA4[7:0]	7:0	SWP RX4 data port 4.	
9Ah	**REG9A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA5[7:0]	7:0	SWP RX4 data port 5.	
9Bh	**REG9B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA6[7:0]	7:0	SWP RX4 data port 6.	
9Ch	**REG9C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA7[7:0]	7:0	SWP RX4 data port 7.	
9Dh	**REG9D**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA8[7:0]	7:0	SWP RX4 data port 8.	
9Eh	**REG9E**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA9[7:0]	7:0	SWP RX4 data port 9.	
9Fh	**REG9F**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA10[7:0]	7:0	SWP RX4 data port 10.	
A0h	**REGA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA11[7:0]	7:0	SWP RX4 data port 11.	
A1h	**REGA1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA12[7:0]	7:0	SWP RX4 data port 12.	
A2h	**REGA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA13[7:0]	7:0	SWP RX4 data port 13.	
A3h	**REGA3**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX4_DATA14[7:0]	7:0	SWP RX4 data port 14.	
A4h	**REGA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA15[7:0]	7:0	SWP RX4 data port 15.	
A5h	**REGA5**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA16[7:0]	7:0	SWP RX4 data port 16.	
A6h	**REGA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA17[7:0]	7:0	SWP RX4 data port 17.	
A7h	**REGA7**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA18[7:0]	7:0	SWP RX4 data port 18.	
A8h	**REGA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA19[7:0]	7:0	SWP RX4 data port 19.	
A9h	**REGA9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA20[7:0]	7:0	SWP RX4 data port 20.	
AAh	**REGAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA21[7:0]	7:0	SWP RX4 data port 21.	
ABh	**REGAB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA22[7:0]	7:0	SWP RX4 data port 22.	
ACh	**REGAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA23[7:0]	7:0	SWP RX4 data port 23.	
ADh	**REGAD**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA24[7:0]	7:0	SWP RX4 data port 24.	
AEh	**REGAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA25[7:0]	7:0	SWP RX4 data port 25.	
AFh	**REGAF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA26[7:0]	7:0	SWP RX4 data port 26.	
B0h	**REGB0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA27[7:0]	7:0	SWP RX4 data port 27.	
B1h	**REGB1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA28[7:0]	7:0	SWP RX4 data port 28.	
B2h	**REGB2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX4_DATA29[7:0]	7:0	SWP RX4 data port 29.	
B3h	**REGB3**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA0[7:0]	7:0	SWP RX5 data port 0.	
B4h	**REGB4**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX5_DATA1[7:0]	7:0	SWP RX5 data port 1.	
B5h	**REGB5**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA2[7:0]	7:0	SWP RX5 data port 2.	
B6h	**REGB6**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA3[7:0]	7:0	SWP RX5 data port 3.	
B7h	**REGB7**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA4[7:0]	7:0	SWP RX5 data port 4.	
B8h	**REGB8**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA5[7:0]	7:0	SWP RX5 data port 5.	
B9h	**REGB9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA6[7:0]	7:0	SWP RX5 data port 6.	
BAh	**REGBA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA7[7:0]	7:0	SWP RX5 data port 7.	
BBh	**REGBB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA8[7:0]	7:0	SWP RX5 data port 8.	
BCh	**REGBC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA9[7:0]	7:0	SWP RX5 data port 9.	
BDh	**REGBD**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA10[7:0]	7:0	SWP RX5 data port 10.	
BEh	**REGBE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA11[7:0]	7:0	SWP RX5 data port 11.	
BFh	**REGBF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA12[7:0]	7:0	SWP RX5 data port 12.	
C0h	**REGC0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA13[7:0]	7:0	SWP RX5 data port 13.	
C1h	**REGC1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA14[7:0]	7:0	SWP RX5 data port 14.	
C2h	**REGC2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA15[7:0]	7:0	SWP RX5 data port 15.	
C3h	**REGC3**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA16[7:0]	7:0	SWP RX5 data port 16.	
C4h	**REGC4**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA17[7:0]	7:0	SWP RX5 data port 17.	
C5h	**REGC5**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX5_DATA18[7:0]	7:0	SWP RX5 data port 18.	
C6h	**REGC6**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA19[7:0]	7:0	SWP RX5 data port 19.	
C7h	**REGC7**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA20[7:0]	7:0	SWP RX5 data port 20.	
C8h	**REGC8**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA21[7:0]	7:0	SWP RX5 data port 21.	
C9h	**REGC9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA22[7:0]	7:0	SWP RX5 data port 22.	
CAh	**REGCA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA23[7:0]	7:0	SWP RX5 data port 23.	
CBh	**REGCB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA24[7:0]	7:0	SWP RX5 data port 24.	
CCh	**REGCC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA25[7:0]	7:0	SWP RX5 data port 25.	
CDh	**REGCD**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA26[7:0]	7:0	SWP RX5 data port 26.	
CEh	**REGCE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA27[7:0]	7:0	SWP RX5 data port 27.	
CFh	**REGCF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA28[7:0]	7:0	SWP RX5 data port 28.	
D0h	**REGD0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX5_DATA29[7:0]	7:0	SWP RX5 data port 29.	
D1h	**REGD1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA0[7:0]	7:0	SWP RX6 data port 0.	
D2h	**REGD2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA1[7:0]	7:0	SWP RX6 data port 1.	
D3h	**REGD3**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA2[7:0]	7:0	SWP RX6 data port 2.	
D4h	**REGD4**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA3[7:0]	7:0	SWP RX6 data port 3.	
D5h	**REGD5**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA4[7:0]	7:0	SWP RX6 data port 4.	
D6h	**REGD6**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX6_DATA5[7:0]	7:0	SWP RX6 data port 5.	
D7h	**REGD7**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA6[7:0]	7:0	SWP RX6 data port 6.	
D8h	**REGD8**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA7[7:0]	7:0	SWP RX6 data port 7.	
D9h	**REGD9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA8[7:0]	7:0	SWP RX6 data port 8.	
DAh	**REGDA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA9[7:0]	7:0	SWP RX6 data port 9.	
DBh	**REGDB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA10[7:0]	7:0	SWP RX6 data port 10.	
DCh	**REGDC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA11[7:0]	7:0	SWP RX6 data port 11.	
DDh	**REGDD**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA12[7:0]	7:0	SWP RX6 data port 12.	
DEh	**REGDE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA13[7:0]	7:0	SWP RX6 data port 13.	
DFh	**REGDF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA14[7:0]	7:0	SWP RX6 data port 14.	
E0h	**REGE0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA15[7:0]	7:0	SWP RX6 data port 15.	
E1h	**REGE1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA16[7:0]	7:0	SWP RX6 data port 16.	
E2h	**REGE2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA17[7:0]	7:0	SWP RX6 data port 17.	
E3h	**REGE3**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA18[7:0]	7:0	SWP RX6 data port 18.	
E4h	**REGE4**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA19[7:0]	7:0	SWP RX6 data port 19.	
E5h	**REGE5**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA20[7:0]	7:0	SWP RX6 data port 20.	
E6h	**REGE6**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA21[7:0]	7:0	SWP RX6 data port 21.	
E7h	**REGE7**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX6_DATA22[7:0]	7:0	SWP RX6 data port 22.	
E8h	**REGE8**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA23[7:0]	7:0	SWP RX6 data port 23.	
E9h	**REGE9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA24[7:0]	7:0	SWP RX6 data port 24.	
EAh	**REGEA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA25[7:0]	7:0	SWP RX6 data port 25.	
EBh	**REGEB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA26[7:0]	7:0	SWP RX6 data port 26.	
ECh	**REGEC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA27[7:0]	7:0	SWP RX6 data port 27.	
EDh	**REGED**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA28[7:0]	7:0	SWP RX6 data port 28.	
EEh	**REGEE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX6_DATA29[7:0]	7:0	SWP RX6 data port 29.	
EFh	**REGEF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA0[7:0]	7:0	SWP RX7 data port 0.	
F0h	**REGF0**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA1[7:0]	7:0	SWP RX7 data port 1.	
F1h	**REGF1**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA2[7:0]	7:0	SWP RX7 data port 2.	
F2h	**REGF2**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA3[7:0]	7:0	SWP RX7 data port 3.	
F3h	**REGF3**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA4[7:0]	7:0	SWP RX7 data port 4.	
F4h	**REGF4**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA5[7:0]	7:0	SWP RX7 data port 5.	
F5h	**REGF5**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA6[7:0]	7:0	SWP RX7 data port 6.	
F6h	**REGF6**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA7[7:0]	7:0	SWP RX7 data port 7.	
F7h	**REGF7**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA8[7:0]	7:0	SWP RX7 data port 8.	
F8h	**REGF8**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX7_DATA9[7:0]	7:0	SWP RX7 data port 9.	
F9h	**REGF9**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA10[7:0]	7:0	SWP RX7 data port 10.	
FAh	**REGFA**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA11[7:0]	7:0	SWP RX7 data port 11.	
FBh	**REGFB**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA12[7:0]	7:0	SWP RX7 data port 12.	
FCh	**REGFC**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA13[7:0]	7:0	SWP RX7 data port 13.	
FDh	**REGFD**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA14[7:0]	7:0	SWP RX7 data port 14.	
FEh	**REGFE**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA15[7:0]	7:0	SWP RX7 data port 15.	
FFh	**REGFF**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA16[7:0]	7:0	SWP RX7 data port 16.	
100h	**REG100**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA17[7:0]	7:0	SWP RX7 data port 17.	
101h	**REG101**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA18[7:0]	7:0	SWP RX7 data port 18.	
102h	**REG102**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA19[7:0]	7:0	SWP RX7 data port 19.	
103h	**REG103**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA20[7:0]	7:0	SWP RX7 data port 20.	
104h	**REG104**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA21[7:0]	7:0	SWP RX7 data port 21.	
105h	**REG105**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA22[7:0]	7:0	SWP RX7 data port 22.	
106h	**REG106**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA23[7:0]	7:0	SWP RX7 data port 23.	
107h	**REG107**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA24[7:0]	7:0	SWP RX7 data port 24.	
108h	**REG108**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA25[7:0]	7:0	SWP RX7 data port 25.	
109h	**REG109**	**7:0**	**Default : 0x00**	**Access : RO**

SWP_LOGIC Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SWP_RX7_DATA26[7:0]	7:0	SWP RX7 data port 26.	
10Ah	**REG10A**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA27[7:0]	7:0	SWP RX7 data port 27.	
10Bh	**REG10B**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA28[7:0]	7:0	SWP RX7 data port 28.	
10Ch	**REG10C**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_RX7_DATA29[7:0]	7:0	SWP RX7 data port 29.	
10Dh	**REG10D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_TX_DATA[7:0]	7:0	SWP TX data port for LPDU of the LLC layers.	
10Eh	**REG10E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_TX1_DATA[7:0]	7:0	SWP TX1 data port for LPDU of the LLC layers.	
10Fh	**REG10F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_TX2_DATA[7:0]	7:0	SWP TX2 data port for LPDU of the LLC layers.	
110h	**REG110**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_TX3_DATA[7:0]	7:0	SWP TX3 data port for LPDU of the LLC layers.	
111h	**REG111**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	BATTERY_OFF_CTRL	5	SWP battery off controlled by register.	
	BATTERY_OFF_AUTO	4	SWP battery off auto mode.	
	-	3:2	Reserved.	
	TX_DATA_CNT[1:0]	1:0	SWP TX data buffer transfer amount.	
114h	**REG114**	**7:0**	**Default : 0x00**	**Access : RO**
	SWP_CLT_MODE	7	SWP enter CLT mode.	
	-	6:5	Reserved.	
	SWP_TIMER_OUT4	4	SWP timer 4 out.	
	SWP_TIMER_OUT3	3	SWP timer 3 out.	
	SWP_TIMER_OUT2	2	SWP timer 2 out.	
	SWP_TIMER_OUT1	1	SWP timer 1 out.	
	SWP_TIMER_OUT0	0	SWP timer 0 out.	
115h	**REG115**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWP_RX_INTR_MASK	7	SWP RX interrupt mask or not.	
	SWP_TX_INTR_MASK	6	SWP TX interrupt mask or not.	
	SWP_TIMER_INTR_MASK	5	SWP timer interrupt mask or not.	
	SWP_CLR_TIMER_OUT4	4	SWP clear timer 4 out.	

SWP_LOGIC Register			
Index	**Mnemonic**	**Bit**	**Description**
	SWP_CLR_TIMER_OUT3	3	SWP clear timer 3 out.
	SWP_CLR_TIMER_OUT2	2	SWP clear timer 2 out.
	SWP_CLR_TIMER_OUT1	1	SWP clear timer 1 out.
	SWP_CLR_TIMER_OUT0	0	SWP clear timer 0 out.

OTG Register

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**FADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FUNCADDR	6:0	USB address.	
01h	**POWER**	**7:0**	**Default : 0x01**	**Access : R/W, RO**
	ISO_UPDATE	7	When set to '1', USB will wait for SOF token from the time TxPktRdy is set before sending a packet. If an IN token is received before an SOF token, a zero length data packet will be sent. Only Valid in isochronous mode (Access: R/W).	
	SOFT_CONN	6	Set '1' to pull up D+ (Access: R/W).	
	HS_EN	5	Set '1' to enable high speed mode (Access: R/W).	
	HS_MODE	4	Set '1' when in high speed mode (Access: RO).	
	RESET	3	Set '1' when USB bus is in USB reset state (Access: RO).	
	RESUME	2	Set '1' when to issue resume state (Access: R/W).	
	SUSPEND_MODE	1	Set '1' when in suspend state (Access: R/W).	
	EN_SUSPENDM	0	Enable SuspendM output (Access: R/W).	
02h	**INTRTX**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	EP4_TX	4	Endpoint4 TX interrupt.	
	EP3_TX	3	Endpoint3 TX interrupt.	
	EP2_TX	2	Endpoint2 TX interrupt.	
	EP1_TX	1	Endpoint1 TX interrupt.	
	EP0	0	Endpoint0 interrupt.	
03h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
04h	**INTRRX**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	EP4_RX	4	Endpoint4 RX interrupt.	
	EP3_RX	3	Endpoint3 RX interrupt.	
	EP2_RX	2	Endpoint2 RX interrupt.	
	EP1_RX	1	Endpoint1 RX interrupt.	
	-	0	Reserved.	
05h	**-**	**7:0**	**Default : -**	**Access : -**

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
	-	7:0	Reserved.	
06h	**INTRTXE**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:5	Reserved.	
	EP4_TXE	4	Endpoint4 TX interrupt enable.	
	EP3_TXE	3	Endpoint3 TX interrupt enable.	
	EP2_TXE	2	Endpoint2 TX interrupt enable.	
	EP1_TXE	1	Endpoint1 TX interrupt enable.	
	EP0_TXE	0	Endpoint0 TX interrupt enable.	
07h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
08h	**INTRRXE**	**7:0**	**Default : 0x0E**	**Access : R/W**
	-	7:5	Reserved.	
	EP4_RXE	4	Endpoint4 RX interrupt enable.	
	EP3_RXE	3	Endpoint3 RX interrupt enable.	
	EP2_RXE	2	Endpoint2 RX interrupt enable.	
	EP1_RXE	1	Endpoint1 RX interrupt enable.	
	-	0	Reserved.	
09h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ah	**INTRUSB**	**7:0**	**Default : -**	**Access : RO**
	VBUS_ERROR	7	VBUS dropped below VBUS valid threshold interrupt. Only valid in A device.	
	SESS_REQ	6	Session request detected interrupt.	
	DISCON	5	Disconnection detected.	
	CONN	4	Connection detected; only valid in host mode.	
	SOF	3	SOF interrupt.	
	RESET_BABBLE	2	Reset/babble interrupt.	
	RESUME	1	Resume interrupt when in suspend mode.	
	SUSPEND	0	Suspend interrupt.	
0Bh	**INTRUSBE**	**7:0**	**Default : 0x06**	**Access : R/W**
	VBUS_ERROR	7	VBUS error interrupt enable.	
	SESS_REQ	6	SESSREQ interrupt enable.	
	DISCON	5	DISCON interrupt enable.	
	CONN	4	CONN interrupt enable.	

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
	SOF	3	SOF interrupt enable.	
	RST_BABBLE	2	Reset/babble interrupt enable.	
	RESUME	1	Resume interrupt enable.	
	SUSPEND	0	Suspend interrupt enable.	
0Ch	**FRAME_L**	**7:0**	**Default : -**	**Access : RO**
	FRAME[7:0]	7:0	The last Frame number received, low byte	
0Dh	**FRAME_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	FRAME[10:8]	2:0	The last Frame number received, higher 3 bits.	
0Eh	**INDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EP_SEL	3:0	Before access EP1~EP4 registers, EP_SEL must be set to the corresponding endpoint (18h~27h).	
0Fh	**TESTMODE**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCE_HOST	7	Set to force entering host mode.	
	FIFO_ACCESS	6	Set to transfer EP0 TX to EP0 RX. Cleared automatically (Access: Self-clearing).	
	FORCE_FS	5	Set to force entering full speed.	
	FORCE_HS	4	Set to force entering high speed.	
	TEST_PACKET	3	Set to enter test packet defined in USB2.0 test mode.	
	TEST_K	2	Set to enter TEST_K defined in USB2.0 test mode.	
	TEST_J	1	Set to enter TEST_J defined in USB2.0 test mode.	
	TEST_SE0_NAK	0	Set to enter TEST_SE0_NAK defined in USB2.0 test mode.	
10h	**TXMAP_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXMAP[7:0]	7:0	Defines the max. amount of the data that can be transferred through the select TX endpoint in a single operation; low byte.	
11h	**TXMAP_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXMAP[15:11]	7:3	Defines the multiplier for the max data bytes in a transaction. The maximum data transferred in a transaction is $(2^m)*$TXMAP; higher 5 bits.	
	TXMAP[10:8]	2:0	Defines the max. amount of the data that can be transferred through the select TX endpoint in a single operation; middle 3 bits.	
For EP_SEL=0, 12h~1Fh				

OTG Register

Index	Mnemonic	Bit	Description	
12h	**CSR0**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	SERVICED_SETUPEND	7	Set to clear SETUPEND (Access: WO, auto-clear).	
	SERVICED_EXPKTRDY	6	Set to clear RXPKTRDY (Access: WO, auto-clear).	
	SENDSTALL	5	Set to terminate current transaction and transfer a stall packet (Access: WO, auto-clear).	
	SETUPEND	4	Set when a control transaction ends (Access: RO).	
	DATAEND	3	Set when loading the last transmit packet or unloading the last received packet (Access: WO, auto-clear).	
	SENTSTALL	2	EP0 send stall (Access: RO).	
	TXPKTRDY	1	EP0 transmit ready (Access: WO, auto-clear).	
	RXPKTRDY	0	EP0 receive packet ready (Access: RO).	
13h	**CSR0_FLSH**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FLUSHFIFO	0	Set to flush the packet to be transmitted/read from the EP0 FIFO (Access: WO, auto-clear).	
14h ~ 17h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:1	Reserved.	
18h	**COUNT0**	**7:0**	**Default : -**	**Access : RO**
	-	7	Reserved.	
	ENDPOINT0_EX_COUNT	6:0	Received endpoint 0 RX count.	
19h ~ 1Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:1	Reserved.	
For EP_SEL≠0, 12h~1Fh: (EP1~EP4)				
12h	**TXCSR1**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7	Reserved.	
	CLRDATATOG	6	Set to reset the data toggle of the corresponding endpoint to 0 (Access: WO).	
	SENTSTALL	5	Set when the stall is sent (Access: RO, auto-clear).	
	SENDSTALL	4	Set to send a stall for the IN packet of the corresponding TX endpoint (Access: R/W).	
	FLUSHFIFO	3	Set to flush the last packet in the corresponding TX FIFO (Access: R/W, auto-clear).	
	UNDERRUN	2	Set when transmitted data (TXPKTRDY) is not ready (Access: RO, auto-clear).	
	FIFONOTEMPTY	1	Set when at least 1 packet in the FIFO (Access: RO,	

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
			auto-clear).	
	TXPKTRDY	0	Set when a packet is loaded to the TX FIFO (Access: R/W, auto-clear).	
13h	**TXCSR2**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOSET	7	Set '1' to make TXPKTRDY be auto-set.	
	-	6	Reserved.	
	MODE	5	0: Set as RX FIFO. 1: Set as TX FIFO.	
	DMAREQENAB	4	Set to enable DMA transfer for the corresponding TX endpoint.	
	FRCDATATOG	3	Set to force the data toggle switched for the TX endpoint.	
	DMAREQMODE	2	DMA mode.	
	-	1:0	Reserved.	
14h	**RXMAP_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	RXMAP[7:0]	7:0	Max packet size of RX packet for EP1~4, lower 8 bits.	
15h	**RXMAP_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	RXMAP[15:11]	7:3	Defines the multiplier for the max data bytes in a transaction. The maximum data transferred in a transaction is $(2^m)*$RXMAP.	
	RXMAP[10:8]	2:0	Max packet size of RX packet for EP1~4, middle 3 bits.	
16h	**RXCSR1**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	CLRDATATOG	7	Set to reset the RX data toggle to 0 for the corresponded endpoint (Access: R/W).	
	SENTSTALL	6	Set when the stall is transmitted (Access: RO).	
	SENDSTALL	5	Set to respond a stall for the OUT packet (Access: R/W).	
	FLUSHFIFO	4	Set to flush the data in the RX FIFO (Access: R/W).	
	DATAERROR	3	Set when received data has CRC or bit-stuffing error (Access: R/W).	
	OVERRUN	2	Set when out data packet can't be loaded to RX FIFO (Access: R/W, write for clear).	
	FIFOFULL	1	Set when FIFO is full (Access: RO).	
	RXPKTRDY	0	Set when a packet is received (Access: R/W, write for clear).	
17h	**RXCSR2**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOCLR	7	Sign bit of blue color.	

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
			0: Increase. 1: Decrease.	
	-	6	Reserved.	
	DMAREQEN	5	DMA request enable for the RX FIFO.	
	DISNYET	4	Set to disable sending NYET for handshaking.	
	DMAREQMD	3	DMA mode setting.	
	-	2:0	Reserved.	
18h	**RXCOUNT_L**	**7:0**	**Default : -**	**Access : RO**
	RXCOUNT[7:0]	7:0	Received endpoint RX count, low byte.	
19h	**RXCOUNT_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	RXCOUNT[12:8]	4:0	Received endpoint RX count, high byte.	
1Ah ~ 1Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
1Fh	**FIFOSIZE**	**7:0**	**Default : -**	**Access : RO**
	RXFIFOSIZE[3:0]	7:4	Size of the related RX FIFO (Default: Application Dependent).	
	TXFIFOSIZE[3:0]	3:0	Size of the related TX FIFO (Default: Application Dependent).	
20h	**EP0_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[7:0]	7:0	EP0 FIFO access port, low byte.	
21h	**EP0_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[15:8]	7:0	EP0 FIFO access port, middle byte.	
22h	**EP0_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[23:16]	7:0	EP0 FIFO access port, middle byte.	
23h	**EP0_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[31:24]	7:0	EP0 FIFO access port, high byte.	
24h	**EP1_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[7:0]	7:0	EP1 FIFO access port, low byte.	
25h	**EP1_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[15:8]	7:0	EP1 FIFO access port, middle byte.	
26h	**EP1_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[23:16]	7:0	EP1 FIFO access port, middle byte.	
27h	**EP1_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**

OTG Register

Index	Mnemonic	Bit	Description	
	EP1_FIFO_ACCESS[31:24]	7:0	EP1 FIFO access port, high byte.	
28h	**EP2_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[7:0]	7:0	EP2 FIFO access port, low byte.	
29h	**EP2_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[15:8]	7:0	EP2 FIFO access port, middle byte.	
2Ah	**EP2_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[23:16]	7:0	EP2 FIFO access port, middle byte.	
2Bh	**EP2_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[31:24]	7:0	EP2 FIFO access port, high byte.	
2Ch	**EP3_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[7:0]	7:0	EP3 FIFO access port, low byte.	
2Dh	**EP3_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[15:8]	7:0	EP3 FIFO access port, middle byte.	
2Eh	**EP3_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[23:16]	7:0	EP3 FIFO access port, middle byte.	
2Fh	**EP3_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[31:24]	7:0	EP3 FIFO access port, high byte.	
30h	**EP4_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[7:0]	7:0	EP4 FIFO access port, low byte.	
31h	**EP4_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[15:8]	7:0	EP4 FIFO access port, middle byte.	
32h	**EP4_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[23:16]	7:0	EP4 FIFO access port, middle byte.	
33h	**EP4_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[31:24]	7:0	EP4 FIFO access port, high byte.	
34h ~ 5Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
60h	**DEVCTL**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	B_DEVICE	7	0: A device. 1: B device. (Access: RO)	
	FSDEV	6	Set when high or full speed is attached. Only act in host mode (Access: RO).	
	LSDEV	5	Set when low speed device is attached. Only act in host	

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
			mode (Access: RO).	
	VBUS[1:0]	4:3	00: VBUS power Below SESSIONEND. 01: VBUS power Above SESSIONEND, below AVALID. 10: VBUS power Above AVALID, below VBUSVALID. 11: VBUS power Above VBUSVALID. (Access: RO)	
	HOST_MD	2	Set when act as a host.	
	HOST_REQ	1	Set in initialize the host negotiation when suspend mode is entered. Cleared when host negotiation is completed (Access: R/W).	
	SESSION	0	Set/cleared when session starts/ends (Access: R/W).	
80h	**USB_CFG0_L**	**7:0**	**Default: 0x01**	**Access: R/W**
	DEBUG_SEL	5:2	Select Debug Group	
	OTG_TM1	1	Test Mode Enable	
	SRST_N	0	Soft Reset, Low Active (default set as 1)	
81h	**USB_CFG0_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	XCVR_TEST	7:0	USB PHY Test	
82h	**USB_CFG1_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_DISCHRGVBUS	7	Discharge vbus loop back	
	LB_IDPULLUP	6	Idpull up loop back	
	LB_PDCON	5	Pdcon loop back	
	LB_PUCON	4	Pucon loop back	
	LB_NDOE	3	Usb output enable loop back	
	LB_VMO	2	VM output loop back	
	LB_VPO	1	VP output loop back	
	LOOPBACK	0	Enable USB PHY Loop Back Test	
83h	**USB_CFG1_H**	**7:0**	**Default: 0x40**	**Access: R/W**
	REG_USBOTG	7	Overwrite enable for device mode	
	IN_VBUSDET_PDN	6	VBUSDET, default suspend (default set as 1)	
	USB2MI_RPRI	5	MIU write priority	
	USB2MI_WPRI	4	MIU read priority	
	LB_PU_LO	3	Pu_lo loop back	
	LB_SPEED	2	Usb speed loop back	
	LB_SUSPEND	1	Suspend loop back	
	LB_CHRGVBUS	0	Charge vbus loop back	

OTG Register				
Index	**Mnemonic**	**Bit**	**Description**	
84h	**USB_CFG2_L**	**7:0**	**Default: 0x06**	**Access: R/W**
		7:2	Reserved.	
	REG_SUSPEND	1	suspend, default set as 1 in suspend mode	
	REG_FT_CLK	0	testing MPLL 60Mhz clock	
86h	**USB_CFG3_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	EP_BULKOUT	3:0	For mode 1 send NAK (Access: R/W)	
87h	**USB_CFG3_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:0	Reserved.	
88h	**USB_CFG4_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:0	Reserved.	
89h	**USB_CFG4_H**	**7:0**	**Default: 0x00**	**Access: RO**
	OTG_DIP	7	Single ended DP input value	
	OTG_DIM	6	Single ended DM input value	
	OTG_DIDIFF	5	USB differential signal	
	OTG_VBUSVALID	4	Vbusvalid input	
	OTG_AVALID	3	Avalid input	
	OTG_CID	2	cid input	
	OTG_VBUSLO	1	Vbuslo input	
8A	**USB_CFG5_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	Rx_Pkt_Cnt[7:0]	7:0	For mode 1 send NAK, RX packet count	
8Bh	**USB_CFG5_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	SET_OK2RCV	7	Data phase enable for bulk out transfer	
	SET_ALLOW_ACK	6	command phase enable for bulk out transfer	
	ECO4NAK_EN	5	ECO enable for bulk out bug	
	Rx_Pkt_Cnt[12:8]	4:0	For mode 1 send NAK, RX packet count	
8Ch	**USB_CFG6_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	Vbus_lo_overwrite	4	Overwrite vbus_lo	
	cid_overwrite	3	Overwrite cid	
	Avalid_overwrite	2	Overwrite avalid	
	Vbusvalid_overwrite	1	Overwrite vbusvalid	
	Miu_mode	0	AFIFO bug ECO enable	
8Dh	**USB_CFG6_H**	**7:0**	**Default: 0x00**	**Access: R/W**

OTG Register			
Index	**Mnemonic**	**Bit**	**Description**
	-	7:0	Reserved.

OTG Register (16-bit direct addressing, 0x0D00~0x0EFF)				
Index	**Mnemonic**	**Bits**	**Description**	
00h ~ 07h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
08h	**DMA_INTR**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	DMA_CH1_INTR	0	DMA Channel 1 interrupt.	
09h ~ 0Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ch	**CH1_DMA_CNTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	ENDPOINT_NO	7:4	Endpoint number to be used in this DMA channel.	
	INTERRUPT_EN	3	DMA mode interrupt enable.	
	DMA_MODE	2	DMA mode setting. 0: DMA manual mode. 1: DMA auto mode.	
	DIRECTION	1	0: DMA RX direction. 1: DMA TX direction.	
	EN_DMA	0	Set to enable DMA channel 1.	
0Dh	**CH1_DMA_CNTL**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	-	7:3	Reserved.	
	BURST_MODE	2:1	00: Burst of unspecified length. 01: INCR4. 10: INCR8. 11: Burst of unspecified length. (Access: R/W)	
	BUS_ERROR	0	AHB bus error (Access: RO).	
10h	**CH1_DMA_ADDR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[7:0]	7:0	Start address of DMA channel 1, low byte.	
11h	**CH1_DMA_ADDR_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[15:8]	7:0	Start address of DMA channel 1, middle byte.	
12h	**CH1_DMA_ADDR_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[23:16]	7:0	Start address of DMA channel 1, middle byte.	
13h	**CH1_DMA_ADDR_H**	**7:0**	**Default : 0x00**	**Access : R/W**

OTG Register (16-bit direct addressing, 0x0D00~0x0EFF)				
Index	**Mnemonic**	**Bits**	**Description**	
	CH1_DMA_ADDR[31:24]	7:0	Start address of DMA channel 1, high byte.	
14h	**CH1_DMA_CNT_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CUNT[7:0]	7:0	Byte count of DMA channel 1, low byte.	
15h	**CH1_DMA_CNT_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[15:8]	7:0	Byte count of DMA channel 1, middle byte.	
16h	**CH1_DMA_CNT_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[23:16]	7:0	Byte count of DMA channel 1, middle byte.	
17h	**CH1_DMA_CNT_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[31:24]	7:0	Byte count of DMA channel 1, high byte.	
18h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

CHIP Register

CHIP Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**REG00**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_VERSION[3:0]	7:4	Chip version.	
	CHIP_REVISION[3:0]	3:0	Chip revision.	
01h	**REG01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_RIU[3:0]	3:0	Clock settings for generating RIU write clock. Bit [3:2]: Select clock source. 00: Select RIU_W. 01: Select RIU_W. 10: Select RIU_W. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
02h	**REG02**	**7:0**	**Default : 0x10**	**Access : R/W**
	CKG_USB[3:0]	7:4	Clock settings for generating USB clock. Bit [3:2]: Select clock source. 00: Select USB60m. 01: Select USB60m. 10: Select USB60m. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
	-	3:0	Reserved.	
03h	**REG03**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	SOFT_RST	5	Software reset.	
	SW_MCU_CLK	4	Switch xtal clock to MCU clock.	
	CKG_MCU[3:0]	3:0	Clock settings for generating MCU clock. Bit [3:2]: Select clock source. 00: 60 MHz. 01: 30 MHz. 10: 100 KHz. 11: Reserved. Bit [1]: Invert clock. Bit [0]: Disable clock.	
04h	**REG04**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIP Register				
Index	**Mnemonic**	**Bit**	**Description**	
	MPLLPD	7	PLL power down.	
	RSTNOUT	6	Test select for rstn output.	
	CLKOUT	5	Test select for clock output.	
	-	4:0	Reserved.	
05h	**REG05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MPLL_ICTRL[2:0]	2:0	PLL ICTRL pin control.	
06h	**REG06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_M[7:0]	7:0	PLL M ratio control.	
07h	**REG07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_TEST[7:0]	7:0	PLL TEST pin control.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	IO_CONFIG[1:0]	5:4	Test select for I/O config, GPIO/I2C/SPI. 00: GPIO[3:0]. 01: I2C clock/data. 10: SPI clock/control/data.	
	-	3:0	Reserved.	
09h	**REG09**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_SMDIF[3:0]	7:4	Clock settings for generating SMDIF clock. Bit [3:2]: Select clock source. 00: Select CLK_7M5. 01: Select CLK_15M. 10: Select CLK_15M. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
	CKG_SECURITY[3:0]	3:0	Clock settings for generating security clock. Bit [3:2]: Select clock source. 00: Select PLL_CLK_BUF. 01: Select PLL_CLK_BUF. 10: Select PLL_CLK_BUF. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
0Bh	**REG0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

CHIP Register

Index	Mnemonic	Bit	Description	
	FUSE_MUX_IN	3	EFUSE input signal controlled by external pin.	
	PROG_FUSE_EN	2	EFUSE enable pin for blowing eFUSE; active high. In read operation mode, the PROG_FUSE_EN is always low.	
	FU_EN	1	If low, no eFUSE will be blown. In sensing and disable mode, the FU_EN is always low.	
	SENSE_PULSE	0	Sense pulse pin in the sensing operation. The programmed data sense out from the eFUSE macro at the falling edge of the SENSE_PULSE signal.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID0[7:0]	7:0	EFUSE ID0.	
0Dh	**REG0D**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID1[7:0]	7:0	EFUSE ID1.	
0Eh	**REG0E**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID2[7:0]	7:0	EFUSE ID1.	
0Fh	**REG0F**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID3[7:0]	7:0	EFUSE ID2.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID4[7:0]	7:0	EFUSE ID3.	
11h	**REG11**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID5[7:0]	7:0	EFUSE ID4.	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID6[7:0]	7:0	EFUSE ID5.	
13h	**REG13**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_ID7[7:0]	7:0	EFUSE ID6.	
14h	**REG14**	**7:0**	**Default : 0x00**	**Access : R/W**
	PM_REG0[7:0]	7:0	PM control register 0. Bit[7:6]: LDO_2P8_LVL_12. Bit[5:4]: LDO_SIM_LVL_12. Bit[3:2]: LDO_1P2_LVL_12. Bit[1:0]: SHUNT_LEVEL_12.	
15h	**REG15**	**7:0**	**Default : 0x00**	**Access : R/W**
	PM_REG1[7:0]	7:0	PM control register 1. Bit[7:6]: Reserved. Bit[5]: LDO_SIM_PD_12. Bit[4]: LDO_2P8_PD_12. Bit[3]: BIAS_TST_12.	

CHIP Register				
Index	**Mnemonic**	**Bit**	**Description**	
			Bit[2:0]: DEGLITCH_12.	
16h	**REG16**	**7:0**	**Default : 0x00**	**Access : R/W**
	PM_REG2[7:0]	7:0	PM control register 2. Bit[7:3]: Reserved. Bit[2:1]: LDO_1P8_LVL_12. Bit[0]: LDO_1P8_PD_12.	
17h	**REG17**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	PG1P8_12	5	LDO_1P8 supply power good. 1: Power good.	
	PG2P8_12	4	LDO_2P8 supply power good. 1: Power good.	
	PGSWP_12	3	LDO_SIM supply power good. 1: Power good.	
	PG1P2_12	2	LDO_1P2 supply power good. 1: Power good.	
	PWR_BAT_12	1	AVDD power from Battery or Coil. 1: Power from Battery.	
	V3P0_PWRG_12	0	AVDD supply power good. 1: Power good.	
18h	**REG18**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_IN_DIV_2[7:0]	7:0	LPLL input divider second.	
19h	**REG19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_IN_DIV_1[1:0]	1:0	LPLL input divider first.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_LOOP_DIV_2[7:0]	7:0	LPLL loop divider second.	
21h	**REG21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_LOOP_DIV_1[1:0]	1:0	LPLL loop divider first.	
22h	**REG22**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_OUT_DIV_2[7:0]	7:0	LPLL output divider second.	
23h	**REG23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_OUT_DIV_1[1:0]	1:0	LPLL output divider first.	

CHIP Register

Index	Mnemonic	Bit	Description	
24h	**REG24**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	LPLL_PORST	6	LPLL porst.	
	LPLL_RESET	5	LPLL reset.	
	LPLL_VCO_OFFSET	4	LPLL VCO offset.	
	LPLL_ICTRL[2:0]	3:1	LPLL ICTRL.	
	LPLL_PD	0	LPLL power down.	
25h	**REG25**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_TEST[7:0]	7:0	LPLL TESTA.	
26h	**REG26**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	LPLL_HIGH_FLAG	1	LPLL high flag.	
	LPLL_LOCK	0	LPLL lock.	
27h	**REG27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SWIO_PD	0	SWIO power down.	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	SMCARD_DET	6	Smart card insert detection.	
	JUMP_ST[2:0]	5:3	Jumper setting status.	
	-	2:0	Reserved.	
29h	**REG29**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_SDO_DRV[1:0]	7:6	Driving control bit C0 C1 for SPI_SDO.	
	SPI_SDI_DRV[1:0]	5:4	Driving control bit C0 C1 for SPI_SDI.	
	SPI_SCK_DRV[1:0]	3:2	Driving control bit C0 C1 for SPI_SCK.	
	SPI_CSZ_DRV[1:0]	1:0	Driving control bit C0 C1 for SPI_CSZ.	
30h	**REG30**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	CTRLMODE_GPIO	3	Pin mux control bit.	
	CTRLMODE_SPI	2	Pin mux control bit.	
	CTRLMODE_SM	1	Pin mux control bit: chip GPIO and smart card interface switch (GPMODE_SM, CTRLMODE_SM). 00: Smart card interface control. 01: Chip GPIO mode.	

CHIP Register				
Index	**Mnemonic**	**Bit**	**Description**	
			10: 8051 p2 GPIO control. 11: Undefined.	
	GPMODE_SM	0	Pin mux control bit: 8051 p2 GPIO and smart card interface switch (GPMODE_SM, CTRLMODE_SM). 00: Smart card interface control. 01: Chip GPIO mode. 10: 8051 p2 GPIO mode. 11: Undefined.	
31h	**REG31**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SMD_IO_IN	7	Pad control bit: PAD_SMD_IO input data in chip GPIO mode.	
	SMD_RSTN_IN	6	Pad control bit: PAD_SMD_RSTN input data in chip GPIO mode.	
	SMD_CLK_OUT	5	Pad control bit: PAD_SMD_CLK output data in chip GPIO mode.	
	SMD_IO_OUT	4	Pad control bit: PAD_SMD_IO output data in chip GPIO mode.	
	SMD_RSTN_OUT	3	Pad control bit: PAD_SMD_RSTN output data in chip GPIO mode.	
	SMD_CLK_OE	2	Pad control bit: PAD_SMD_CLK oe control in chip GPIO mode.	
	SMD_IO_OE	1	Pad control bit: PAD_SMD_IO oe control in chip GPIO mode.	
	SMD_RSTN_OE	0	Pad control bit: PAD_SMD_RSTN oe control in chip GPIO mode.	
32h	**REG32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPI_CSZ_IN	7	Pad control bit.	
	SPI_SDI_OUT	6	Pad control bit.	
	SPI_SCK_OUT	5	Pad control bit.	
	SPI_CSZ_OUT	4	Pad control bit.	
	SPI_SDI_OE	3	Pad control bit.	
	SPI_SCK_OE	2	Pad control bit.	
	SPI_CSZ_OE	1	Pad control bit.	
	SMD_CLK_IN	0	Pad control bit: PAD_SMD_CLK input data in chip GPIO mode.	
33h	**REG33**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	SPI_SDI_IN	2	Pad control bit.	

CHIP Register

Index	Mnemonic	Bit	Description	
	SPI_SDO_IN	1	Pad control bit.	
	SPI_SCK_IN	0	Pad control bit.	
34h	**REG34**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_OE[7:0]	7:0	Pad control bit.	
35h	**REG35**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_OUT[7:0]	7:0	Pad control bit.	
36h	**REG36**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_IN[7:0]	7:0	Pad control bit.	
37h	**REG37**	**7:0**	**Default : 0x80**	**Access : R/W**
	OSC_100K[7:0]	7:0	Bit [0]: OSC 100k power down. Bit [6:1]: OSC 100k I control. Bit [7]: Xtal enable.	
38h	**REG38**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_SCK[3:0]	7:4	Clock settings for generating sck clock. Bit [3:2]: Select clock source. 00: Select sck. 01: Select sck. 10: Select sck. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
	CKG_TCK[3:0]	3:0	Clock settings for generating tck clock. Bit [3:2]: Select clock source. 00: Select tck. 01: Select tck. 10: Select tck. 11: Select xtal clock. Bit [1]: Invert clock. Bit [0]: Disable clock.	
39h	**REG39**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_TRIM[1:0]	7:6	Efuse mux selection.	
	PM_TRIM[5:0]	5:0	PM trim parameter.	
40h	**REG40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ROSC_IN_EN	1	Delay chain input enable.	
	ROSC_IN_SEL	0	Delay chain input selection.	
41h	**REG41**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIP Register				
Index	**Mnemonic**	**Bit**	**Description**	
	ROM_CRC16_EXP_0[7:0]	7:0	ROM CRC expect.	
42h	**REG42**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_CRC16_EXP_1[7:0]	7:0	ROM CRC expect.	
43h	**REG43**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_CRC16_0[7:0]	7:0	ROM CRC.	
44h	**REG44**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_CRC16_1[7:0]	7:0	ROM CRC.	

AES Register

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**REG00**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_0[7:0]	7:0	Data input byte 0 for encryption/decryption.	
01h	**REG01**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_1[7:0]	7:0	Data input byte 1 for encryption/decryption.	
02h	**REG02**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_2[7:0]	7:0	Data input byte 2 for encryption/decryption.	
03h	**REG03**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_3[7:0]	7:0	Data input byte 3 for encryption/decryption.	
04h	**REG04**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_4[7:0]	7:0	Data input byte 4 for encryption/decryption.	
05h	**REG05**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_5[7:0]	7:0	Data input byte 5 for encryption/decryption.	
06h	**REG06**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_6[7:0]	7:0	Data input byte 6 for encryption/decryption.	
07h	**REG07**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_7[7:0]	7:0	Data input byte 7 for encryption/decryption.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_8[7:0]	7:0	Data input byte 8 for encryption/decryption.	
09h	**REG09**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_9[7:0]	7:0	Data input byte 9 for encryption/decryption.	
0Ah	**REG0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_10[7:0]	7:0	Data input byte 10 for encryption/decryption.	
0Bh	**REG0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_11[7:0]	7:0	Data input byte 11 for encryption/decryption.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_12[7:0]	7:0	Data input byte 12 for encryption/decryption.	
0Dh	**REG0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_13[7:0]	7:0	Data input byte 13 for encryption/decryption.	
0Eh	**REG0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_14[7:0]	7:0	Data input byte 14 for encryption/decryption.	
0Fh	**REG0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_IN_15[7:0]	7:0	Data input byte 15 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_0_S0[7:0]	7:0	Key byte 0 for encryption/decryption.	
11h	**REG11**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_1_S0[7:0]	7:0	Key byte 1 for encryption/decryption.	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_2_S0[7:0]	7:0	Key byte 2 for encryption/decryption.	
13h	**REG13**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_3_S0[7:0]	7:0	Key byte 3 for encryption/decryption.	
14h	**REG14**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_4_S0[7:0]	7:0	Key byte 4 for encryption/decryption.	
15h	**REG15**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_5_S0[7:0]	7:0	Key byte 5 for encryption/decryption.	
16h	**REG16**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_6_S0[7:0]	7:0	Key byte 6 for encryption/decryption.	
17h	**REG17**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_7_S0[7:0]	7:0	Key byte 7 for encryption/decryption.	
18h	**REG18**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_8_S0[7:0]	7:0	Key byte 8 for encryption/decryption.	
19h	**REG19**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_9_S0[7:0]	7:0	Key byte 9 for encryption/decryption.	
1Ah	**REG1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_10_S0[7:0]	7:0	Key byte 10 for encryption/decryption.	
1Bh	**REG1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_11_S0[7:0]	7:0	Key byte 11 for encryption/decryption.	
1Ch	**REG1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_12_S0[7:0]	7:0	Key byte 12 for encryption/decryption.	
1Dh	**REG1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_13_S0[7:0]	7:0	Key byte 13 for encryption/decryption.	
1Eh	**REG1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_14_S0[7:0]	7:0	Key byte 14 for encryption/decryption.	
1Fh	**REG1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_15_S0[7:0]	7:0	Key byte 15 for encryption/decryption.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_16_S0[7:0]	7:0	Key byte 16 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
21h	**REG21**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_17_S0[7:0]	7:0	Key byte 17 for encryption/decryption.	
22h	**REG22**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_18_S0[7:0]	7:0	Key byte 18 for encryption/decryption.	
23h	**REG23**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_19_S0[7:0]	7:0	Key byte 19 for encryption/decryption.	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_20_S0[7:0]	7:0	Key byte 20 for encryption/decryption.	
25h	**REG25**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_21_S0[7:0]	7:0	Key byte 21 for encryption/decryption.	
26h	**REG26**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_22_S0[7:0]	7:0	Key byte 22 for encryption/decryption.	
27h	**REG27**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_23_S0[7:0]	7:0	Key byte 23 for encryption/decryption.	
28h	**REG28**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_24_S0[7:0]	7:0	Key byte 24 for encryption/decryption.	
29h	**REG29**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_25_S0[7:0]	7:0	Key byte 25 for encryption/decryption.	
2Ah	**REG2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_26_S0[7:0]	7:0	Key byte 26 for encryption/decryption.	
2Bh	**REG2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_27_S0[7:0]	7:0	Key byte 27 for encryption/decryption.	
2Ch	**REG2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_28_S0[7:0]	7:0	Key byte 28 for encryption/decryption.	
2Dh	**REG2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_29_S0[7:0]	7:0	Key byte 29 for encryption/decryption.	
2Eh	**REG2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_30_S0[7:0]	7:0	Key byte 30 for encryption/decryption.	
2Fh	**REG2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_31_S0[7:0]	7:0	Key byte 31 for encryption/decryption.	
30h	**REG30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_0_S0[7:0]	7:0	Initial vector byte 0 for encryption/decryption.	
31h	**REG31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_1_S0[7:0]	7:0	Initial vector byte 1 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
32h	**REG32**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_2_S0[7:0]	7:0	Initial vector byte 2 for encryption/decryption.	
33h	**REG33**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_3_S0[7:0]	7:0	Initial vector byte 3 for encryption/decryption.	
34h	**REG34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_4_S0[7:0]	7:0	Initial vector byte 4 for encryption/decryption.	
35h	**REG35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_5_S0[7:0]	7:0	Initial vector byte 5 for encryption/decryption.	
36h	**REG36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_6_S0[7:0]	7:0	Initial vector byte 6 for encryption/decryption.	
37h	**REG37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_7_S0[7:0]	7:0	Initial vector byte 7 for encryption/decryption.	
38h	**REG38**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_8_S0[7:0]	7:0	Initial vector byte 8 for encryption/decryption.	
39h	**REG39**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_9_S0[7:0]	7:0	Initial vector byte 9 for encryption/decryption.	
3Ah	**REG3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_10_S0[7:0]	7:0	Initial vector byte 10 for encryption/decryption.	
3Bh	**REG3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_11_S0[7:0]	7:0	Initial vector byte 11 for encryption/decryption.	
3Ch	**REG3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_12_S0[7:0]	7:0	Initial vector byte 12 for encryption/decryption.	
3Dh	**REG3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_13_S0[7:0]	7:0	Initial vector byte 13 for encryption/decryption.	
3Eh	**REG3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_14_S0[7:0]	7:0	Initial vector byte 14 for encryption/decryption.	
3Fh	**REG3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_15_S0[7:0]	7:0	Initial vector byte 15 for encryption/decryption.	
40h	**REG40**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_0[7:0]	7:0	Data output byte 0 for encryption/decryption.	
41h	**REG41**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_1[7:0]	7:0	Data output byte 1 for encryption/decryption.	
42h	**REG42**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_2[7:0]	7:0	Data output byte 2 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
43h	**REG43**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_3[7:0]	7:0	Data output byte 3 for encryption/decryption.	
44h	**REG44**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_4[7:0]	7:0	Data output byte 4 for encryption/decryption.	
45h	**REG45**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_5[7:0]	7:0	Data output byte 5 for encryption/decryption.	
46h	**REG46**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_6[7:0]	7:0	Data output byte 6 for encryption/decryption.	
47h	**REG47**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_7[7:0]	7:0	Data output byte 7 for encryption/decryption.	
48h	**REG48**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_8[7:0]	7:0	Data output byte 8 for encryption/decryption.	
49h	**REG49**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_9[7:0]	7:0	Data output byte 9 for encryption/decryption.	
4Ah	**REG4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_10[7:0]	7:0	Data output byte 10 for encryption/decryption.	
4Bh	**REG4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_11[7:0]	7:0	Data output byte 11 for encryption/decryption.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_12[7:0]	7:0	Data output byte 12 for encryption/decryption.	
4Dh	**REG4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_13[7:0]	7:0	Data output byte 13 for encryption/decryption.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_14[7:0]	7:0	Data output byte 14 for encryption/decryption.	
4Fh	**REG4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXET_OUT_15[7:0]	7:0	Data output byte 15 for encryption/decryption.	
50h	**REG50**	**7:0**	**Default : 0x20**	**Access : R/W**
	DECRYPT_S0	7	Encrypt/decrypt: 0: Encrypt. 1: Decrypt.	
	MODE_S0[2:0]	6:4	Operation mode: 000: ECB mode. 001: CBC mode. 010: CTR mode. 011: CFB8 mode.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
			100: CFB mode. 101: OFB mode.	
	KEY_SIZE_S0[1:0]	3:2	Key size for AES algorithm: 00: 128 bits. 01: 192 bits. 10: 256 bits. 11: Reserved.	
	CRYPT_S0[1:0]	1:0	Encrypt/decrypt algorithm: 00: AES. 01: DES. 10: 3DES. 11: Reserved.	
51h	**REG51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FIRST	1	FIRST block indicator: 0: Non FIRST block. 1: FIRST block, load iv.	
	START	0	START operation, write one to activate.	
52h	**REG52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CRYPT_BUSY	3	Encrypt/decrypt operation status. 0: Idle. 1: Operation busy in progress.	
	PCHK	2	Parity check enable. 0: Enable parity check. 1: Disable parity check.	
	SESSION[1:0]	1:0	SESSION selection. 0: SESSION 0. 1: SESSION 1.	
60h	**REG60**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_0_S1[7:0]	7:0	Key byte 0 for encryption/decryption.	
61h	**REG61**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_1_S1[7:0]	7:0	Key byte 1 for encryption/decryption.	
62h	**REG62**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_2_S1[7:0]	7:0	Key byte 2 for encryption/decryption.	
63h	**REG63**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_3_S1[7:0]	7:0	Key byte 3 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
64h	**REG64**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_4_S1[7:0]	7:0	Key byte 4 for encryption/decryption.	
65h	**REG65**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_5_S1[7:0]	7:0	Key byte 5 for encryption/decryption.	
66h	**REG66**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_6_S1[7:0]	7:0	Key byte 6 for encryption/decryption.	
67h	**REG67**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_7_S1[7:0]	7:0	Key byte 7 for encryption/decryption.	
68h	**REG68**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_8_S1[7:0]	7:0	Key byte 8 for encryption/decryption.	
69h	**REG69**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_9_S1[7:0]	7:0	Key byte 9 for encryption/decryption.	
6Ah	**REG6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_10_S1[7:0]	7:0	Key byte 10 for encryption/decryption.	
6Bh	**REG6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_11_S1[7:0]	7:0	Key byte 11 for encryption/decryption.	
6Ch	**REG6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_12_S1[7:0]	7:0	Key byte 12 for encryption/decryption.	
6Dh	**REG6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_13_S1[7:0]	7:0	Key byte 13 for encryption/decryption.	
6Eh	**REG6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_14_S1[7:0]	7:0	Key byte 14 for encryption/decryption.	
6Fh	**REG6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_15_S1[7:0]	7:0	Key byte 15 for encryption/decryption.	
70h	**REG70**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_16_S1[7:0]	7:0	Key byte 16 for encryption/decryption.	
71h	**REG71**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_17_S1[7:0]	7:0	Key byte 17 for encryption/decryption.	
72h	**REG72**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_18_S1[7:0]	7:0	Key byte 18 for encryption/decryption.	
73h	**REG73**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_19_S1[7:0]	7:0	Key byte 19 for encryption/decryption.	
74h	**REG74**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_20_S1[7:0]	7:0	Key byte 20 for encryption/decryption.	

AES Register				
Index	**Mnemonic**	**Bit**	**Description**	
75h	**REG75**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_21_S1[7:0]	7:0	Key byte 21 for encryption/decryption.	
76h	**REG76**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_22_S1[7:0]	7:0	Key byte 22 for encryption/decryption.	
77h	**REG77**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_23_S1[7:0]	7:0	Key byte 23 for encryption/decryption.	
78h	**REG78**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_24_S1[7:0]	7:0	Key byte 24 for encryption/decryption.	
79h	**REG79**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_25_S1[7:0]	7:0	Key byte 25 for encryption/decryption.	
7Ah	**REG7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_26_S1[7:0]	7:0	Key byte 26 for encryption/decryption.	
7Bh	**REG7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_27_S1[7:0]	7:0	Key byte 27 for encryption/decryption.	
7Ch	**REG7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_28_S1[7:0]	7:0	Key byte 28 for encryption/decryption.	
7Dh	**REG7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_29_S1[7:0]	7:0	Key byte 29 for encryption/decryption.	
7Eh	**REG7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_30_S1[7:0]	7:0	Key byte 30 for encryption/decryption.	
7Fh	**REG7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEY_IN_31_S1[7:0]	7:0	Key byte 31 for encryption/decryption.	
80h	**REG80**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_0_S1[7:0]	7:0	Initial vector byte 0 for encryption/decryption.	
81h	**REG81**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_1_S1[7:0]	7:0	Initial vector byte 1 for encryption/decryption.	
82h	**REG82**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_2_S1[7:0]	7:0	Initial vector byte 2 for encryption/decryption.	
83h	**REG83**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_3_S1[7:0]	7:0	Initial vector byte 3 for encryption/decryption.	
84h	**REG84**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_4_S1[7:0]	7:0	Initial vector byte 4 for encryption/decryption.	
85h	**REG85**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_5_S1[7:0]	7:0	Initial vector byte 5 for encryption/decryption.	

AES Register

Index	Mnemonic	Bit	Description	
86h	**REG86**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_6_S1[7:0]	7:0	Initial vector byte 6 for encryption/decryption.	
87h	**REG87**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_7_S1[7:0]	7:0	Initial vector byte 7 for encryption/decryption.	
88h	**REG88**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_8_S1[7:0]	7:0	Initial vector byte 8 for encryption/decryption.	
89h	**REG89**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_9_S1[7:0]	7:0	Initial vector byte 9 for encryption/decryption.	
8Ah	**REG8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_10_S1[7:0]	7:0	Initial vector byte 10 for encryption/decryption.	
8Bh	**REG8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_11_S1[7:0]	7:0	Initial vector byte 11 for encryption/decryption.	
8Ch	**REG8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_12_S1[7:0]	7:0	Initial vector byte 12 for encryption/decryption.	
8Dh	**REG8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_13_S1[7:0]	7:0	Initial vector byte 13 for encryption/decryption.	
8Eh	**REG8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_14_S1[7:0]	7:0	Initial vector byte 14 for encryption/decryption.	
8Fh	**REG8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IV_15_S1[7:0]	7:0	Initial vector byte 15 for encryption/decryption.	
90h	**REG90**	**7:0**	**Default : 0x20**	**Access : R/W**
	DECRYPT_S1	7	Encrypt/decrypt: 0: Encrypt. 1: Decrypt.	
	MODE_S1[2:0]	6:4	Operation mode: 000: ECB mode. 001: CBC mode. 010: CTR mode. 011: CFB mode. 100: CFB8 mode. 101: OFB mode.	
	KEY_SIZE_S1[1:0]	3:2	Key size for AES algorithm: 00: 128 bits. 01: 192 bits. 10: 256 bits. 11: Reserved.	

AES Register			
Index	**Mnemonic**	**Bit**	**Description**
	CRYPT_S1[1:0]	1:0	Encrypt/decrypt algorithm: 00: AES. 01: DES. 10: 3DES. 11: Reserved.

SMDCIF Register

SMDCIF Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**REG00**	**7:0**	**Default : 0x00**	**Access : R/W**
	GUARD_EXTRA[7:0]	7:0	Number of extra guard time.	
01h	**REG01**	**7:0**	**Default : 0x33**	**Access : R/W**
	REPEAT_CNT[3:0]	7:4	TX/RX parity error interrupt threshold. Interrupt occurs when successive parity error exceeds this value.	
	GUARD_DEF[3:0]	3:0	Default guard time parameter.	
02h	**REG02**	**7:0**	**Default : 0x40**	**Access : R/W**
	ATR_TIMEOUT_CNT_0[7:0]	7:0	ATR timeout value, low byte. Interrupt occurs if ATR does not respond before the specified clock cycle. ATR timeout period parameter [7:0].	
03h	**REG03**	**7:0**	**Default : 0x9C**	**Access : R/W**
	ATR_TIMEOUT_CNT_1[7:0]	7:0	ATR timeout value, high byte. Interrupt occurs if ATR does not respond before the specified clock cycle. ATR timeout period parameter [15:8].	
04h	**REG04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SMDC[4:0]	4:0	Clock control: clock invert, clock gate, clock frequency selection. [0]: Gate smart card interface internal clock. [1]: Invert clock. [3:2]: Clock selection. 00: /2. 01: /4. 10: /8. 11: /1. [4]: Gate smart card clock.	
05h	**REG05**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETU_TIMER_MODE	7	ETU timer mode. 0: ETU based timer. 1: Smartcard clock cycle based timer.	
	CARD_DET	6	Read only card detection status. 0: No card inserted. 1: Card inserted.	
	DIR_CONV_MODE[1:0]	5:4	Direct convention mode setting.	

SMDCIF Register				
Index	**Mnemonic**	**Bit**	**Description**	
			00: Convention mode auto detected. 01: Direct convention mode. 10: Inverse convention mode. 11: Reserved.	
	TS_DETECT	3	TS byte received from ATR. 0: Indicate 'h3F, inverse convention. 1: Indicate 'h3B, direct convention.	
	SMDC_PROTOCOL	2	Transmission protocol T. 0: Protocol T=0. 1: Protocol T=1.	
	CLK_STOP_IDTR[1:0]	1:0	Smart card clock stop indicator X. [1:0]. 00: Clock stop not supported. 01: State L. 10: State H. 11: No preference.	
06h	**REG06**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETU_TIMER_LOAD	7	ETU timer load, reload the down counter, write one active reload.	
	TRX_STOP	6	TRX stop. Write operation: White 1 to disable "load TX data", "mask RX data"; write 0 to enable "load TX data", "unmask RX data". Read operation: 0: "Load TX data" enable status. 1: "Load TX data" disable status.	
	WARMRST	5	Warm reset, write one active.	
	DEACT	4	Deactivation, write one active.	
	ACT	3	Activation, write one active.	
	SMDC_RST	2	Reset smart card interface controller, write one reset.	
	RXFIFO_CLR	1	Clear RX FIFO, write one clear.	
	TXFIFO_CLR	0	Clear TX FIFO, write one clear.	
07h	**REG07**	**7:0**	**Default : 0x51**	**Access : R/W**
	RX_FULL	7	TX FIFO full indicator.	
	RX_EMPTY	6	TX FIFO empty indicator.	
	TX_FULL	5	TX FIFO full indicator.	
	TX_EMPTY	4	TX FIFO empty indicator.	
	ST_ACTOK	3	Activate complete state.	

SMDCIF Register				
Index	**Mnemonic**	**Bit**	**Description**	
	ST_RST	2	Reset active state.	
	ST_PWREN	1	Power enable state.	
	ST_IDLE	0	Idle state.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ATR_TIMEOUT	6	ATR timeout event.	
	RX_UNDERFLOW	5	RX FIFO underflow.	
	TX_OVERFLOW	4	TX FIFO overflow.	
	TS_UNKNOWN	3	Unknown TS character.	
	RX_OVERFLOW	2	RX FIFO overflow.	
	-	1	Reserved.	
	PARRITY_ERR	0	RX parity error occurs.	
09h	**REG09**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXFIFO[7:0]	7:0	TX FIFO port.	
0Ah	**REG0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RXFIFO[7:0]	7:0	RX FIFO port.	
0Bh	**REG0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RXFIFO_THRESHOLD[5:0]	5:0	RX FIFO threshold trigger level. Interrupt occurs when data count in RX FIFO reaches this value. Value 0 means no interrupt occurs.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RXFIFO_CNT[5:0]	5:0	RX FIFO counter.	
0Dh	**REG0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TXFIFO_CNT[5:0]	5:0	TX FIFO counter.	
0Eh	**REG0E**	**7:0**	**Default : 0x74**	**Access : R/W**
	FD_RATIO_0[7:0]	7:0	F/D ratio [7:0].	
0Fh	**REG0F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	FD_RATIO_1[5:0]	5:0	F/D ratio [13:8].	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETU_TIMER_VAL_0[7:0]	7:0	ETU based timer value byte 0, low byte [7:0].	

SMDCIF Register				
Index	**Mnemonic**	**Bit**	**Description**	
			Write operation: Write value is the reload value of the down counter. Read operation: Read value is the reset value of the down counter.	
11h	**REG11**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETU_TIMER_VAL_1[7:0]	7:0	ETU based timer value byte1, middle byte [15:8]. Write operation: Write value is the reload value of the down counter. Read operation: Read value is the reset value of the down counter.	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETU_TIMER_VAL_2[7:0]	7:0	ETU based timer value byte1, high byte [23:16]. Write operation: Write value is the reload value of the down counter. Read operation: Read value is the reset value of the down counter.	
13h	**REG13**	**7:0**	**Default : 0xFF**	**Access : R/W**
	INTR_MSK[7:0]	7:0	Interrupt mask: 1 for disable interrupt event, 0 for enable interrupt event. [0]: Parity error interrupt disable. [1]: ATR TS byte error interrupt disable. [2]: TX overflow/RX underflow interrupt disable. [3]: ATR reset timeout interrupt disable. [4]: RX input data receive indication interrupt disable. [5]: RX data overflow interrupt disable. [6]: TX FIFO data complete interrupt disable. [7]: ETU based timer timeout interrupt disable.	
14h	**REG14**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTR_SOFT[7:0]	7:0	Software trigger interrupt write trigger. [0]: Trigger parity error interrupt. [1]: Trigger ATR TS byte error interrupt. [2]: Trigger TX overflow/RX underflow interrupt. [3]: Trigger ATR reset timeout interrupt. [4]: Trigger RX input data receive indication interrupt. [5]: Trigger RX data overflow interrupt. [6]: Trigger TX FIFO data complete interrupt. [7]: Trigger ETU based timer timeout interrupt.	

PMU Register

PMU Register				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
01h	**REG01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PM_DEEP	0	Enter deep sleep command.	
02h	**REG02**	**7:0**	**Default : 0x5A**	**Access : R/W**
	RTC_EN[7:0]	7:0	Wakeup RTC timer enable. !0x5a: Disable RTC timer and reset timer counter, and clear timeout wakeup event. 0x5a: Enable RTC timer and start to increment counter.	
03h	**REG03**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RTC_THLD_0[7:0]	7:0	RTC timeout threshold low byte.	
04h	**REG04**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_THLD_1[7:0]	7:0	RTC timeout threshold middle byte.	
05h	**REG05**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_THLD_2[7:0]	7:0	RTC timeout threshold high byte.	
06h	**REG06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DEEP_FLAG	0	Deep sleep flag, to record the deep sleep status when entering deep sleep mode. Write one to clear the flag.	
07h	**REG07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	EXT_WAKEUP_INT_ST	2	External wakeup interrupt status.	
	RF_DETECT_INT_ST	1	RF detect interrupt status.	
	TIMEOUT_INT_ST	0	RTC timeout interrupt status.	
08h	**REG08**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	XTAL_STABLE	3		
	RING_OSC_STABLE	2		
	PM_STATE[1:0]	1:0	Current power state status. [1:0]. 00: Initial state.	

PMU Register				
Index	**Mnemonic**	**Bit**	**Description**	
			01: Active state. 10: Sleep state. 11: Deep sleep state.	
09h	**REG09**	**7:0**	**Default : 0x5A**	**Access : R/W**
	RFDETECT_EN[7:0]	7:0	RF detect wakeup event enable. 0x5a: Enable RF detect function. When both RTC and external wakeup are disabled, RF detect will be enabled.	
0Ah	**REG0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SWIO_PD	5	Swio power down control.	
	DEGLITCH[2:0]	4:2	DEGLITCH setting.	
	-	1	Reserved.	
	SHUNT_SW_PD	0	Shunt regulator software control power down.	
0Bh	**REG0B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	V3P0_PWR_GOOD	6	V3p0 power good status.	
	PMUSIM_PWR_GOOD	5	PMU supply power good status.	
	ALIVE_PWR_GOOD	4	Alive power good status.	
	CORE_PWR_GOOD	3	Core power good status.	
	SIM_PWR_GOOD	2	SIM card power good status.	
	LDOCORE_EN_ST	1	Core power enable status.	
	LDOSIM_EN_ST	0	SIM card power enable status.	
0Ch	**REG0C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	SIM_PWR_FLAG	1	SIM power flag. 1: 2.8V. 0: 1.8V or no power.	
	GP_MODE	0	Power supply from RF indication. 1: Get power mode. 0: Normal mode.	
0Dh	**REG0D**	**7:0**	**Default : 0x5A**	**Access : R/W**
	EXTWAKEUP_EN[7:0]	7:0	External wakeup event enable. 0x5a: Enable external wakeup event.	
0Eh	**REG0E**	**7:0**	**Default : 0x01**	**Access : R/W**

PMU Register				
Index	**Mnemonic**	**Bit**	**Description**	
	-	7:1	Reserved.	
	LDOSIM_SW_EN	0	SIM card LDO software control power enable.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	BIAS_TST	7	Enable for BG current test.	
	BRIDGE_TST	6	Used to short the bridge by software.	
	TR_BG[5:0]	5:0	Bandgap trim control.	
13h	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
02/08/10		Created first version.

APPENDIX

Abbreviations

ADC	Analog to Digital Converter
AFI	Application Family Identifier
ASIC	Application Specific Integrated Circuits
ASK	Amplitude Shift Keying
BB	Baseband
BER	Bit Error Rate
BW	Band width
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital to Analog Converter
DSFID	Data Storage Format Identifier
DSP	Digital Signal Processing
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable and Programmable read Only memory
EMI	Electromagnetic Interference
ENOB	ADC Effective Number Of Bits
EOF	End of Frame
FSK	Frequency Shift Keying
IC	Integrated Circuit
I2C	Inter-IC (control interface)
LSB	Least Significant Bit or Byte
LO	Local Oscillator
MCU	Micro-Controller Unit
MSB	Most Significant Bit or Byte
MTBF	Mean Time Between Failure
PPM	Part Per Million
PRC	Pseudo Random Code
PRN	Pseudo Random Number
PWM	Pulse Width Modulation
RTF	Reader Talk First
SNR	Serial Number
SOC	System On a Chip
SOF	Start of Frame
TCXO	Temperature Compensated Crystal Oscillator
UID	Unique Identifier
VCD	Vicinity Coupling Device

References

[1] Auto-ID center, "13.56 MHz ISM Band Class 1 Radio Frequency Identification Tag Interface Specification."
[2] Klaus Finkenzeller, "RFID Handbook: Fundamentals and Applications in Contactless Smartcards and Identification."
[3] Datasheet, "MCRF450/451/452/455," Microchip.
[4] Datasheet, "Tag-it HF," Texas Instruments.
[5] Application Note, "I Code1 System Design Guide," Philips Semiconductors.
[6] Nedap: "System model for inductive ID systems."

Manufacturer	Product	Further Information
Infineon	SLE 44R35 S (Mifare Standard)	www.infineon.com
	SLE 66R35 (Mifare NRG)	www.infineon.com
	SLE 55R04 (my-d proximity)	www.infineon.com
	SLE 55R16 (my-d proximity)	www.infineon.com
	SRF 55V10P (my-d vicinity)	www.infineon.com
Legic	MIM 1024 *	Flyer
	MIM 256 *	Flyer
Philips	MF1 IC S50 (Mifare Standard)	www.semiconductors.philips.com
	MF1 IC S70 (Mifare 4K)	www.semiconductors.philips.com
	MF3 IC D40 (Mifare DESFire)	www.semiconductors.philips.com
	MF0 IC U1001 (Mifare UltraLight 16,9pF)	www.semiconductors.philips.com
	MF0 IC U1101 (Mifare UltraLight 50pF)	www.semiconductors.philips.com
	SL1 IC S3001 (I-Code 27,5pF)	www.semiconductors.philips.com
	SL1 IC S3101 (I-Code 97pF)	www.semiconductors.philips.com
	SL2 IC S1001 (I-Code EPC)	www.semiconductors.philips.com
	SL2 IC S1101 (I-Code UID)	www.semiconductors.philips.com
	SL2 IC S2001 (I-Code SL2)	www.semiconductors.philips.com
	SL3 IC S3001 (U-Code HSL)	www.semiconductors.philips.com
	SL3 IC S3101 (U-Code EPC)	www.semiconductors.philips.com
STMicroelectronics	SR176	www.st.com/contactless
	SRIX4K	www.st.com/contactless
	SRIX512	www.st.com/contactless
	LRI64	www.st.com/contactless
	CTS	www.st.com/contactless