CI-MCP Specification

4GB eNAND (x8, MMC)
+ 4Gb LPDDR2-S4B (x32)

Document Title

CI-MCP
4GB(x8) e-NAND / 4Gb (x32) LPDDR2-S4B

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft - 4GB e-NAND - 4Gb(4Gb LPDDR2 M-Die) LPDDR2	Aug. 2011	Preliminary
0.2	Editorial Change	Sep. 2011	Preliminary

FEATURES

[CI-MCP]

- Operation Temperature
  - -25°C ~ 85°C
- Packcage
  - 162-ball FBGA - 11.5x13mm^2, 1.0t, 0.5mm pitch
  - Lead & Halogen Free

[e-NAND Flash]

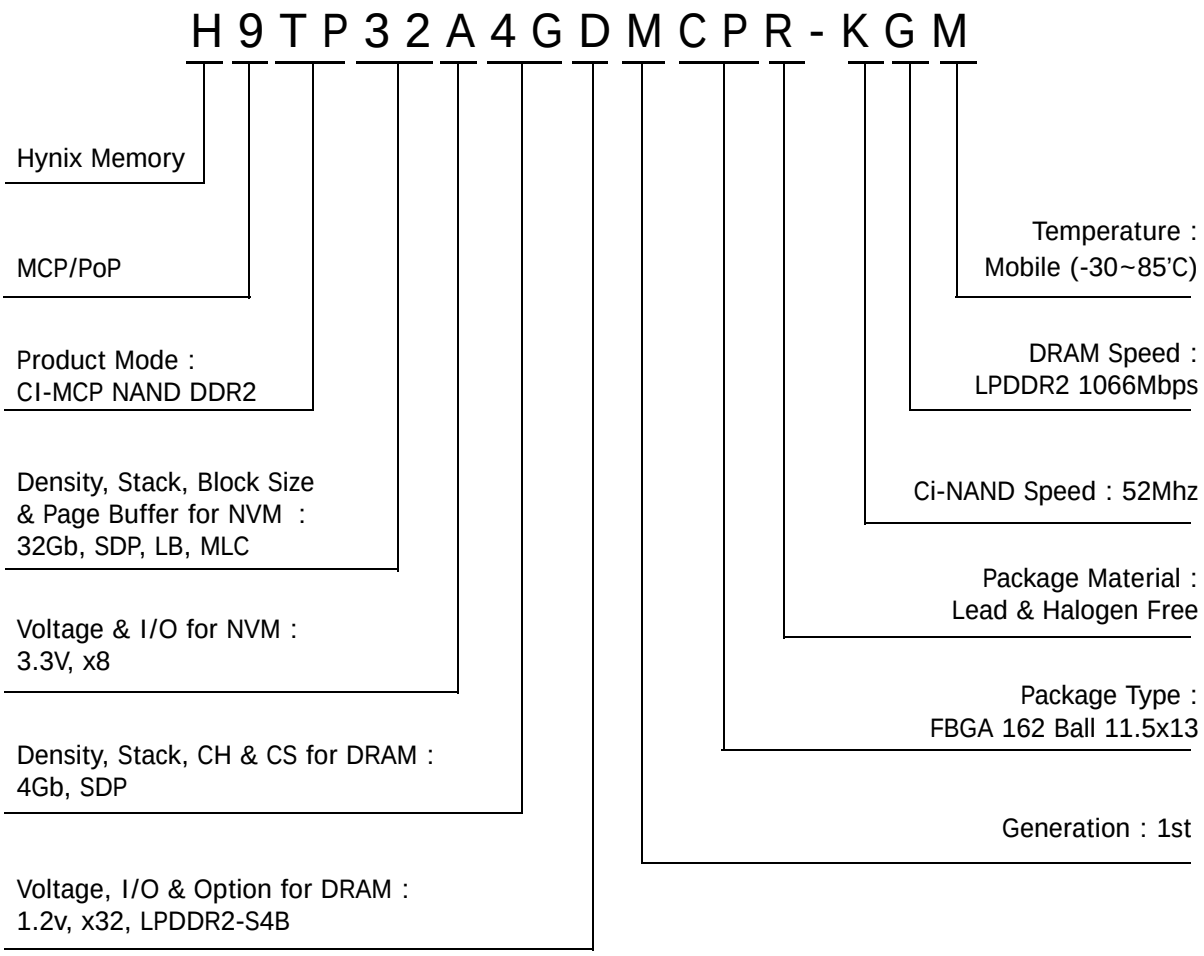
- Packaged NAND flash memory with MultiMediaCard interface
- High capacity memory access
- eMMC/MultiMediaCard system specification, compliant with V4.41
- Full backward compatibility with previous MultiMediaCard system specification
- Bus mode
  - High-speed MultiMediaCard protocol.
  - Three different data bus widths: 1 bit, 4 bits,8 bits.
  - Data transfer rate: up to 104Mbyte/s
  - DDR mode supported
- Operating voltage range:
  - V_{CCQ} = 1.7~1.95V/2.7V~3.6V
  - V_{CC} = 3.3V
- Error free memory access
  - Internal error correction code
  - Internal enhanced data management algorithm (wear levelling, bad block management, garbage collection)
  - Possibility for the host to make sudden power failure safe-update operations for data content
- Security
  - Password protection of data
  - Security Erase
  - Security Trim
  - Secure bad block management
  - Built-in write protection
- Boot
  - Simple boot sequence method
- Power saving
  - Enhanced power saving method by introducing sleep functionality
- Partition management with enhanced storage.
- Hardware reset supported

[LPDDR2 S4B]

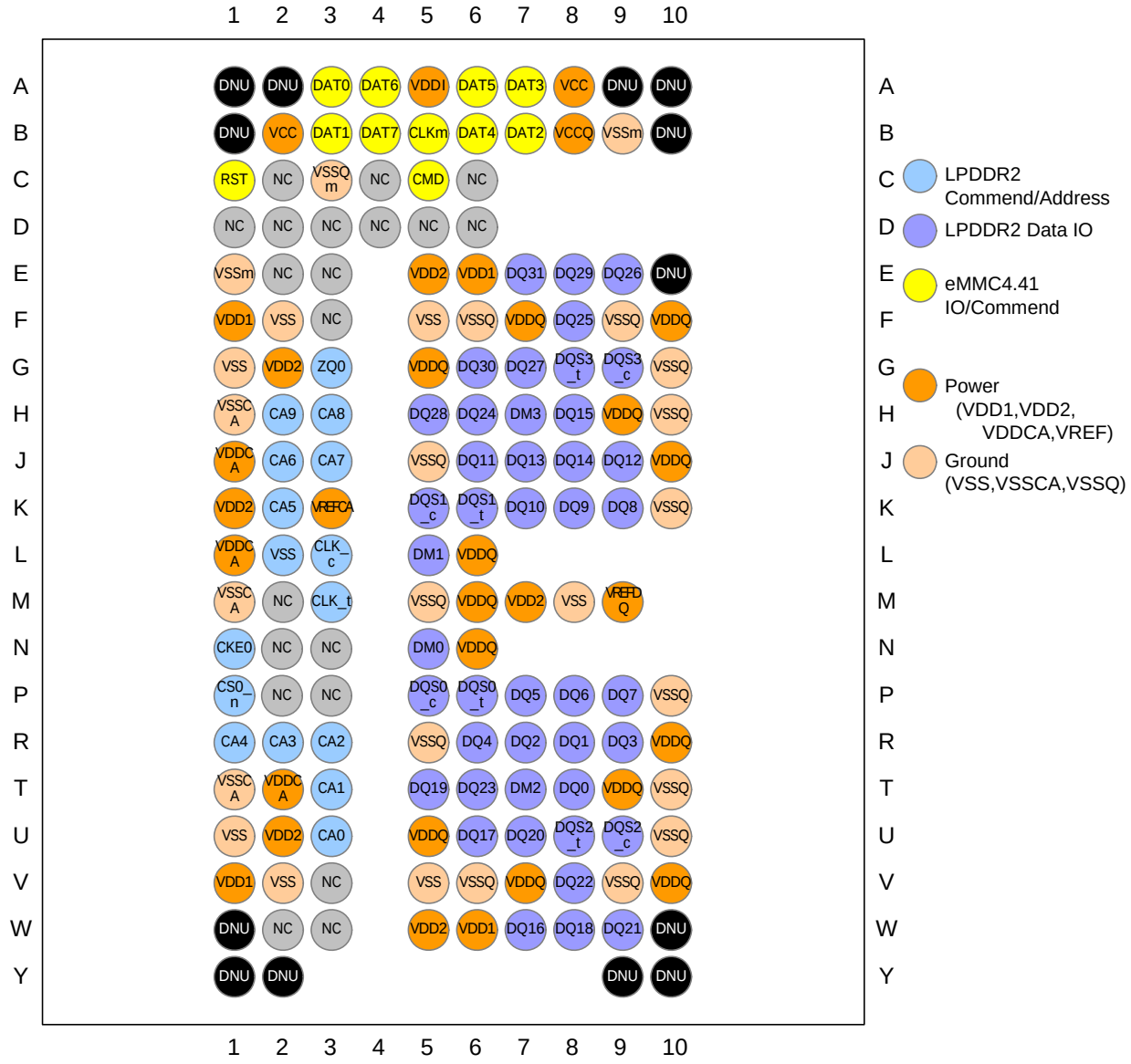
- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2, VDDCA and VDDQ = 1.2V (1.14V to 1.30)
- HSUL_12 interface (High Speed Unterminated Logic 1.2V)
- Double data rate architecture for command, address and data Bus;
  - all control and address except CS_n, CKE latched at both rising and falling edge of the clock
  - CS_n, CKE latched at rising edge of the clock
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
  - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)
  - Data outputs aligned to the edge of the data strobe (DQS_t, DQS_c) when READ operation
  - Data inputs aligned to the center of the data strobe (DQS_t, DQS_c) when WRITE operation
- DM masks write data at the both rising and falling edge of the data strobe
- Programmable RL (Read Latency) and WL (Write Latency)
- Programmable burst length: 4, 8 and 16
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Clock Stop Mode
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- DS (Drive Strength)
- DPD (Deep Power Down)
- ZQ (Calibration)

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H9TP32A4GDMCPR-KDM	e-NAND mobile DDR2 S4B	3.3V 1.8V/1.2/1.2/1.2	4GB (x8) 4Gb (x32)	52Mhz DDR2 800	162Ball FBGA (Lead & Halogen Free)
H9TP32A4GDMCPR-KGM	e-NAND mobile DDR2 S4B	3.3V 1.8V/1.2/1.2/1.2	4GB (x8) 4Gb (x32)	52Mhz DDR2 1066	162Ball FBGA (Lead & Halogen Free)



162Ball ASSIGNMENT - (4GB+4Gb / eMMC4.41 + x32 LPDDR2 1CH, 1CS/ch)



Top View

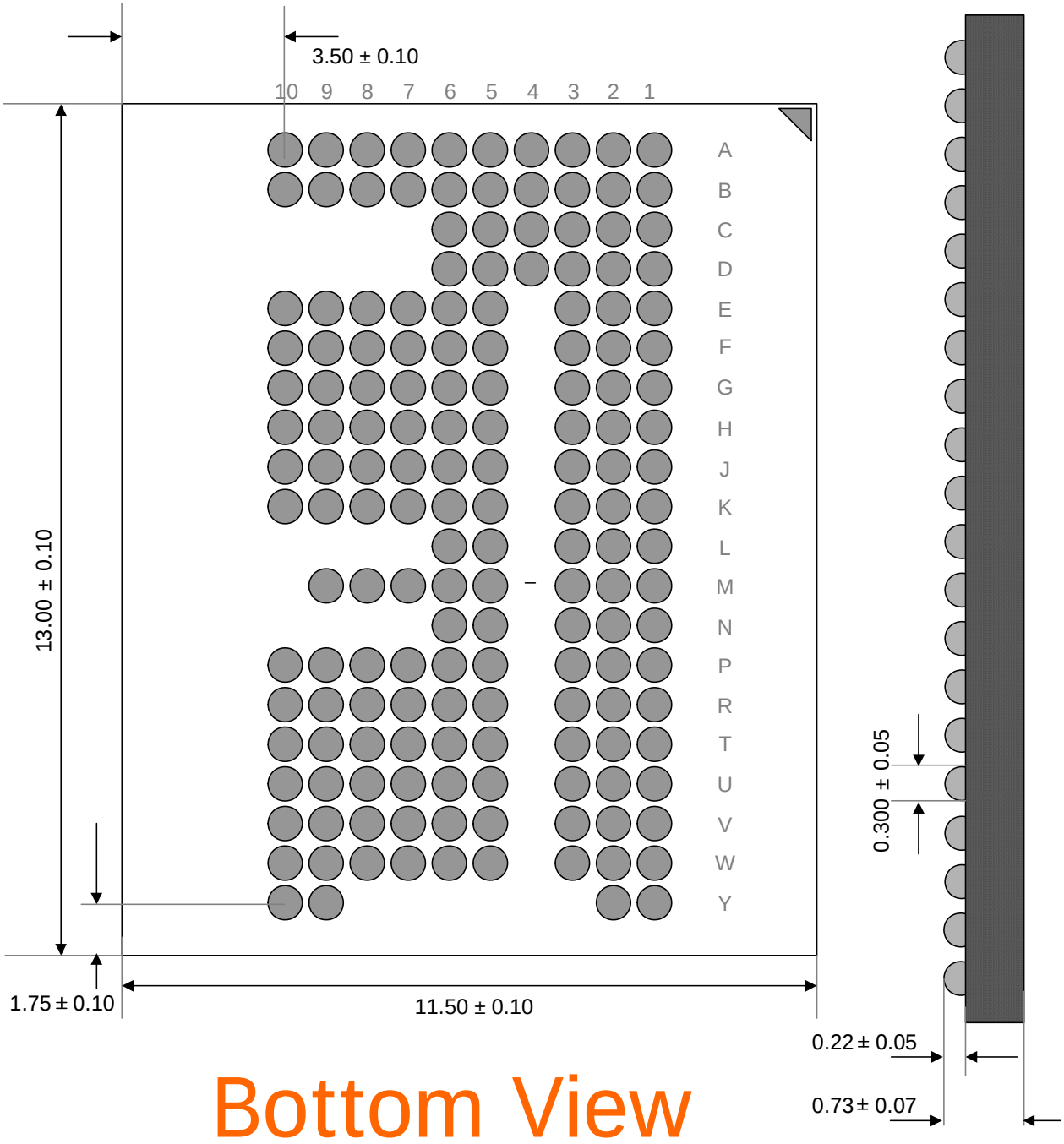
162ball 11.5x13 MCP
eMMC + x32 LPDDR2 (1CH)

Pin Description

SYMBOL	DESCRIPTION	Type
< 4GB (x8, MMC) e-NAND >		
CLK	Clock	Input
CMD	Command	Input/Output
DAT0~DAT7	Data Input/Output	Input/Output
VCC	Core Power Supply	Power
VCCQ	I/O Power Supply	Power
VSS	Ground	Ground
VDDI	By pass	Power
< 4Gb (x32) LPDDR2-S4B >		
CS0_n	Chip Select	Input
CK_c, CK_t	Differential Clocks	Input
CKE0	Clock Enable	Input
CA0 ~ CA9	Command / Address	Input
DQ0 ~ DQ15	Data I/O	Input/Output
DM0 ~ DM1	Input Data Mask	Input/Output
DQS0_t ~ DQS1_t	Differential Data Strobe (pos.)	Input/Output
DQS0_c ~ DQS1_c	Differential Data Strobe (neg.)	Input/Output
ZQ	Drive Strength Calibration	Input/Output
VDD1	Core Power Supply	Power
VDD2	Core Power Supply	Power
VSS	Ground	Ground
VDDQ	I/O Power Supply	Power
VDDCA	CA Power Supply	Power
VSSCA	CA Ground	Ground
VSSQ	I/O Ground	Ground
VREF(CA) / VREF(DQ)	Reference Voltage	Power

PACKAGE INFORMATION

162 Ball 0.5mm pitch 11.5mm x 13.0mm FBGA *[t = 1.0mm max]*



Bottom View

4GB(x8) e-NAND Flash

1. Description

The Hynix e-NAND is an embedded flash memory storage solution with MultiMediaCard™ interface (eMMC™). The eMMC™ was developed for universal low cost data storage and communication media. The Hynix e-NAND is fully compatible with MMC bus and hosts.

The Hynix e-NAND communications are made through an advanced 11-pin bus.
The bus can be either 1-bit, 4-bit, or 8-bit in width. The device operates in high-speed mode at clock frequencies equal to or higher than 20MHz, which is the MMC standard. The communication protocol is defined as a part of this MMC standard and referred to as MultiMediaCard mode.

The device is designed to cover a wide area of applications such as smart phones, cameras, organizers, PDA, digital recorders, MP3 players, pagers, electronic toys, etc. They feature high performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, the Hynix e-NAND supports both 3.3V supply voltage (V_{CC}), and 3.3V/1.8V input/output voltage (V_{CCQ}).

The address argument for the Hynix e-NAND is the sector address (512-byte sectors) instead of the byte address. This means that Hynix e-NAND is not backward compatible with devices of density lower than 2 Gbytes. If there is no indication by the host to the memory that the host is capable of handling sector type of addressing, the Hynix e-NAND will change its state to inactive.

The device has a built-in intelligent controller which manages interface protocols, data storage and retrieval, wear leveling, bad block management, garbage collection, and
internal ECC.

The Hynix e-NAND makes available to the host sudden power failure safe-update operations for the data content, by supporting reliable write features.

The device supports boot operation with enhance area and sleep/awake commands.
In particular, during the sleep state the host power regulator for VCC can be switched off, thus minimizing the power consumption of the Hynix e-NAND.

1.1 e-NAND Standard Specification

The Hynix e-NAND device is fully compatible with the JEDEC Standard Specification No. JESD84-A441.
This datasheet describes the key and specific features of the Hynix e-NAND device. Any additional information required to interface the device to a host system and all the practical methods for card detection and access can be found in the proper sections of the JEDEC Standard Specification.

2. System features

The following list identifies the main features of the MultiMediaCard System, which:

- Is targeted for portable and stationary applications
- Has these System Voltage (VDD) Ranges:

	Voltage
Communication	1.7 - 1.95 or 2.7 - 3.6
Memory Access	2.7 - 3.6

- Is designed for read-only, read/write and I/O cards
- Supports card clock frequencies of 0-20MHz, 0-26MHz or 0-52MHz
- Has a maximum data rate up to 832Mbits/sec.
- Has a defined minimum performance
- Maintains card support for three different data bus width modes: 1-bit (default), 4-bit, and 8-bit
- Includes definition for higher than 2GB of density of memories
- Includes password protection of data
- Supports basic file formats for high data interchangeability
- Includes application specific commands
- Enables correction of memory field errors
- Has built-in write protection features for the boot and user areas, which may be permanent,power-on, or temporary
- Includes a simple erase mechanism
- Maintains full backward compatibility with previous MultiMediaCard systems
- Provides a possibility for the host to make sudden power failure safe-update operations for the data content.
- Enhanced power saving method by introducing a sleep functionality.
- Introduces Boot Operation Mode to provide a simple boot sequence method.
- Provides a new CID Register setting to recognize *e-NAND*.
- Obsoletes the SPI Mode.
- Defines I/O voltage (VCCQ) and core voltage (VCC) separately for *e-NAND*.
- Defines Erase-unit size and Erase timeout for high-capacity memory.
- Provides access size register indicating one (or multiple) programmable boundary unit(s) of device.
- Obsoletes the Absolute Minimum Performance.
- Introduces *e-NAND* OCR setting and response.
- Defines WP group size for high-capacity devices.
- Introduces Alternate Boot Operation Mode.
- Introduces Secure Erase & Trim to enhance data security.
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Signed access to a Replay Protected Memory Block.
- Introduces dual data rate transfer.
- Introduces high speed boot.
- Enhanced Write Protection with Permanent and Partial protection options.
- Introduces hardware reset signa.

2.1 Operating Conditions

Temperature	Operating	-25℃~85℃
	Non-Operating	-40℃~85℃

3. Device physical description

The Hynix e-NAND contains a single chip controller and flash memory module, see the below *Figure 1 Device block diagram.* The microcontroller interfaces with a host system allowing data to be written to and read from the flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

Figure2 shows the package connections. See *Table1: Signal names* for the description of the signals corresponding to the balls.

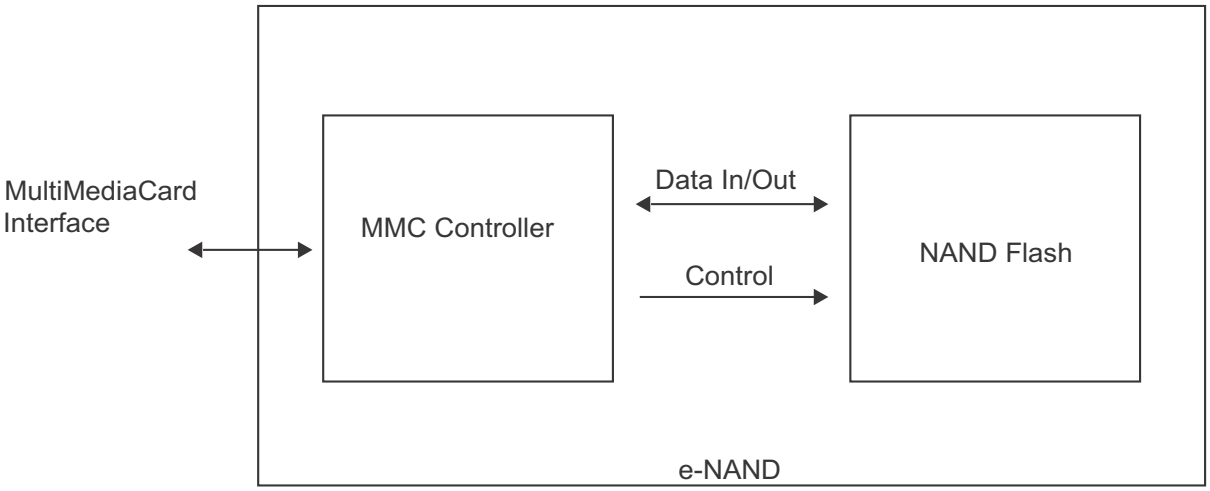


Figure 1: Device block diagram

4. MultiMediaCard interface

The signal/pin assignments are listed in *Table1.* Refer to this table in conjunction with *Figure2* and *Figure3: Form factor.*

4.1 Signals description

4.1.1 Clock (CLK)

The Clock input, CLK, is used to synchronize the memory to the host during command and data transfers. Each clock cycle gates one bit on the command and on all the data lines. The Clock frequency, fPP, may vary between zero and the maximum clock frequency.

4.1.2 Command (CMD)

The CMD signal is a bidirectional command channel used for device initialization and command transfer. The CMD signal has two operating modes: open-drain and push-pull.
The open-drain mode is used for initialization, while the push-pull mode is used for fast command transfer. Commands are sent by the MultiMediaCard bus master (or host) to the device who responds by sending back responses.

4.1.3 Input/outputs (DAT0-DAT7)

DAT0 to DAT7 are bidirectional data channels. The signals operate in push-pull mode. The Hynix e-NAND includes internal pull ups for all data lines. These signals cannot be driven simultaneously by the host and the Hynix e-NAND device. Right after entering the 4-bit mode, the card disconnects the internal pull ups of lines DAT1 and DAT2. Correspondingly right after entering the 8-bit mode, the card disconnects the internal pull ups of lines DAT1, DAT2 and DAT4-DAT7.By default, after power-up or hardware reset, only DAT0 is used for data transfers. The host can configure the device to use a wider data bus, DAT0, DAT0-DAT3 or DAT0-DAT7, for data transfer.

4.1.4 VCC core supply voltage

VCC provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase). The core voltage (VCC) can be within 2.7V and 3.6V.

4.1.5 VSS ground

Ground, VSS, is the reference for the power supply. It must be connected to the system ground.

4.1.6 VCCQ input / output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}. The input/output voltage (V_{CCQ}) can be either within 1.7V and 1.95V (low voltage range) or 2.7V and 3.6V (high voltage range).

4.1.7 VSSQ supply voltage

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}.

4.1.8 Reset

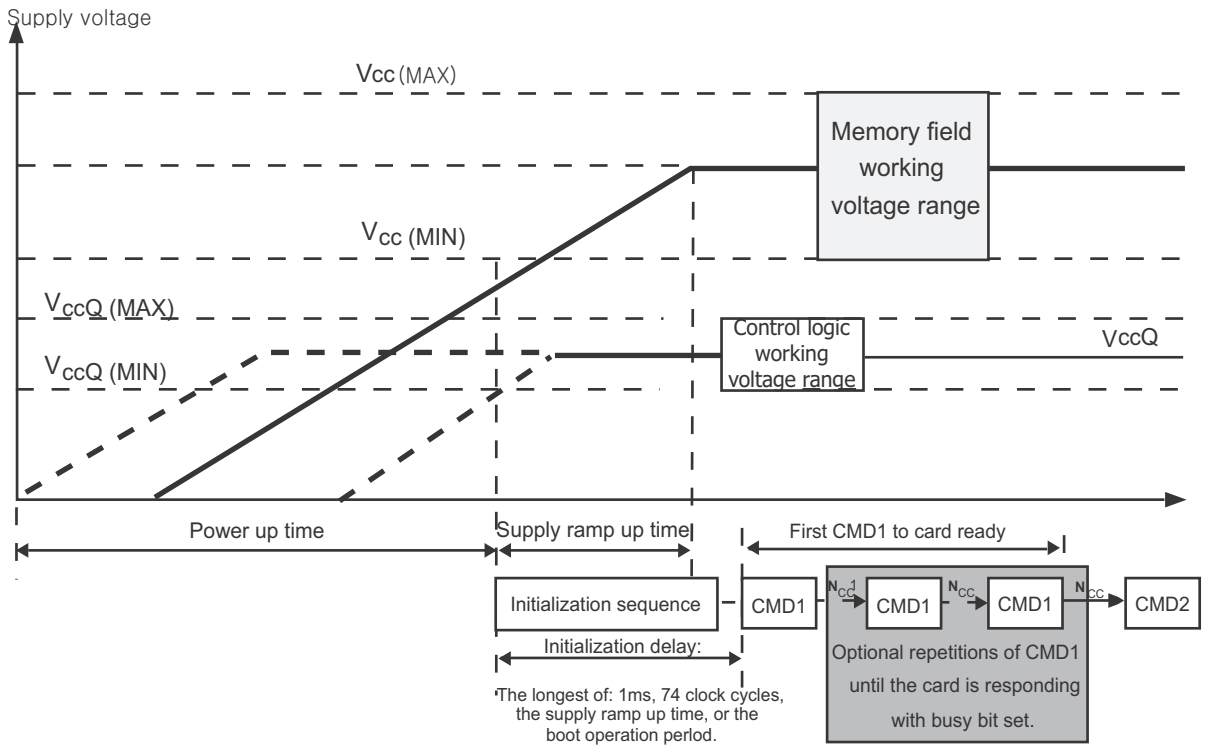
Reset signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. Host need to set bit[0:1] in the extended CSD register [162] to 0x1 to enable this functionality before the host uses.

4.2 Bus Topology

The Hynix e-NAND device supports the MMC protocol. For more details, refer to section 6.4 of the JEDEC Standard Specification No. JESD84-A441. The section 12 of the JEDEC Standard Specification contains a bus circuitry diagram for reference.

4.3 Power up

Figure 3: e-NAND power-up diagram



An *e-NAND* power-up must adhere to the following guidelines:

• When power-up is initiated, either VCC or VCCQ can be ramped up first, or both can be ramped up simultaneously.

• After power up, the *e-NAND* enters the *pre-idle* state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

• If the *e-NAND* does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, the *e-NAND* moves immediately to the *idle* state. While in the *idle* state, the *e-NAND* ignores all bus transactions until CMD1 is received. If the *e-NAND* supports only specification v4.2 or earlier versions, the device enters the *idle* state immediately following power-up.

• If the BOOT_PARTITION_ENABLE bit is set, the *e-NAND* moves to the *pre-boot* state, and the *e-NAND* waits for the boot-initiation sequence. Following the boot operation period, the *e-NAND* enters the *idle* state. During the *pre-boot* state, if the *e-NAND* receives any CMD-line transaction other than the boot initiation sequence (keeping CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA) and CMD1, the *e-NAND* moves to the *Idle* state. If *e-NAND* receives theboot initiation sequence (keeping the CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA), the *e-NAND* begins boot operation. If boot acknowledge is enabled, the *e-NAND* shall send acknowledge pattern “010” to the host within the specified time. After boot operation is terminated, the *e-NAND* enters the *idle* state and shall be ready for CMD1 operation. If the *e-NAND* receives CMD1 in the *pre-boot* state, it begins responding to the command and moves to the card identification mode.

• While in the *idle* state, the *e-NAND* ignores all bus transactions until CMD1 is received.

• CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the device until it is out of its power-up sequence. In addition to the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.

• If the *e-NAND* device was successfully partitioned during the previous power up session (bit 0 of EXT_CSD byte [155] PARTITION_SETTING_COMPLETE successfully set) then the initialization delay is (instead of 1s) calculated from INI_TIMEOUT_PA (EXT_CSD byte [241]). This timeout applies only for the very first initializastion after successful partitioning. For all the consequtive initialization 1sec timeout will apply.

• The bus master moves the device out of the *idle* state. Because the power-up time and the supply ramp up time depend on application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

• After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

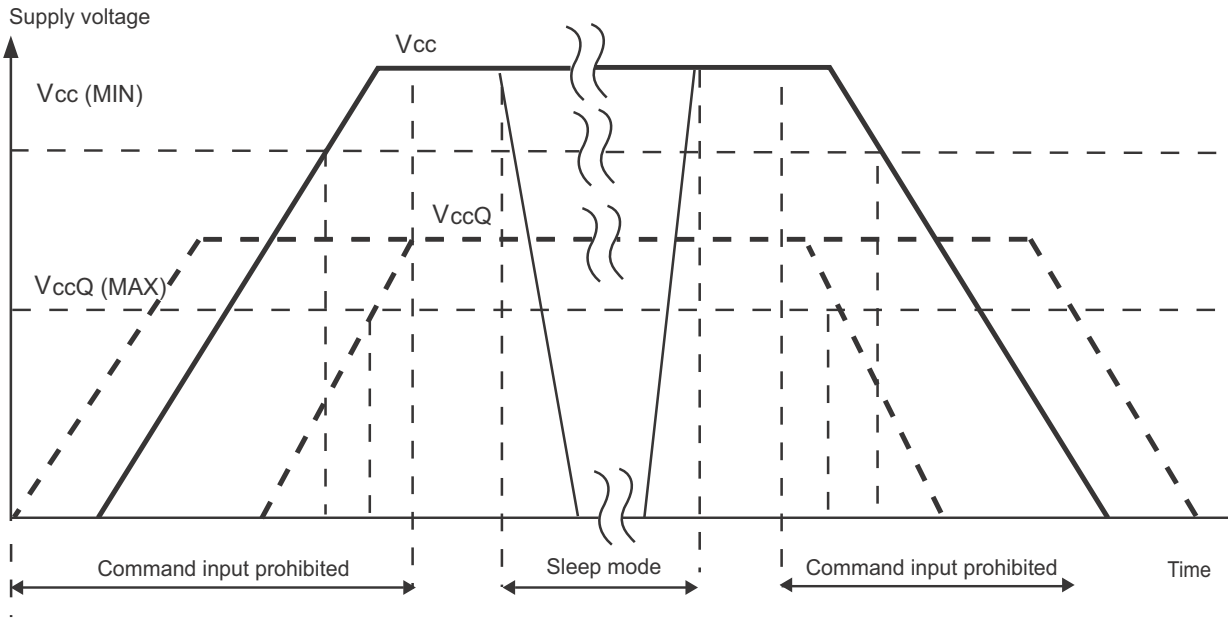
• Every bus master must implement CMD1.

4.4 e-NAND power cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.

If VCC or VCCQ are below 0.5 V for longer than 1 ms, the slave shall always return to the *pre-idle* state,and perform the appropriate boot behavior, as appropriate. The slave will behaves as in a standard powerupcondition once the voltages have returned to their functional ranges.

Figure 5: e-NAND power cycle



4.5 Bus operating conditions

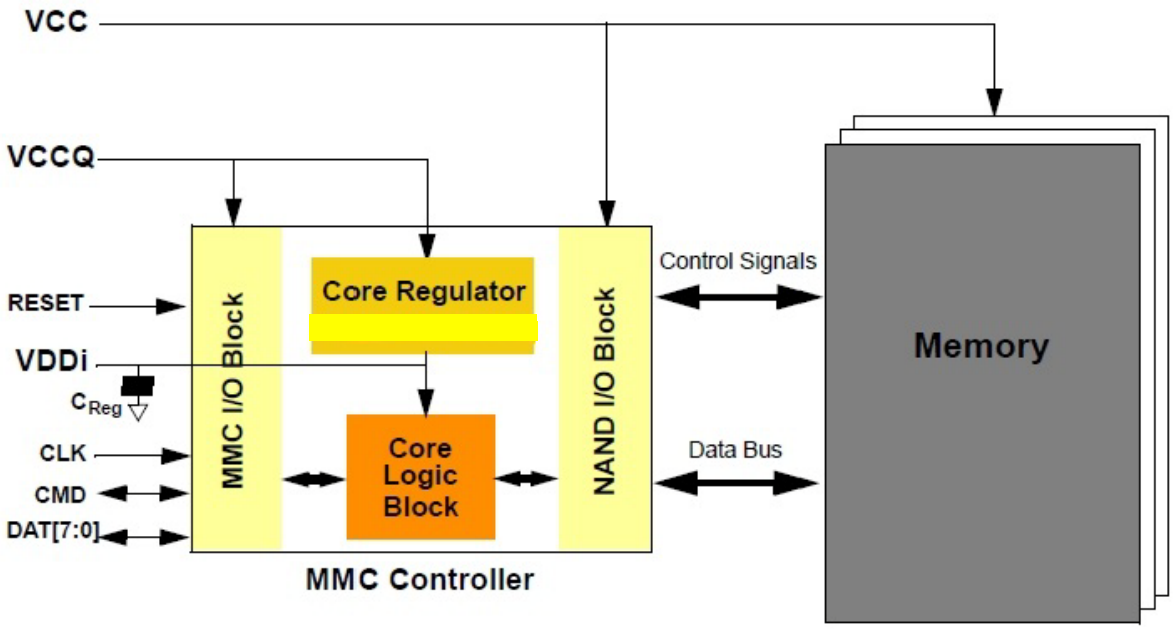
Table 2 : General operation conditions

Parameter		Symbol	Min	Max.	Unit	Remark
Peak voltage on lines	fBGA		-0.5	VccQ+0.5	V	
All Inputs						
Input Leakage Current(before initialization sequenceand/or the internal pull up resistors connected)			-100	100	μA	
Input Leakage Current(after initialization sequence and the internal pull up resistors disconnected)			-2	2	μA	
All Inputs						
Output Leakage CurrentCurrent (before initialization sequence)			-100	100	μA	
Output Leakage Current(after initialization sequence)			-2	2	μA	

4.5.1 Power supply

In the *e-NAND*, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage. The core regulator is optional and only required when VCCQ is in the 3V range. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 6: e-NAND internal power diagram



The *e-NAND* supports one or more combinations of VCC and VCCQ as shown in Table. The VCCQ must be defined at equal to or less than VCC.

Table 3 : e-NAND power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply voltage (NAND)	Vcc	2.7	3.6	V	
Supply voltage (I/O)	Vccq	2.7	3.6	V	
		1.70	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	

The *e-NAND* must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations

Table 4 : e-NAND voltage combinations

		VCCQ	
		1.70V~1.95V	2.7V~3.6V
VCC	2.7V~3.6V	Valid	Valid

4.5.2 Bus signal line load

The total capacitance C_L of each line of the e-NAND bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{BGA} of the card connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{BGA}$$

and requiring the sum of the host and bus capacitances not to exceed 20 pF:

Table 5 : e-NAND Capacitance

Parameter	Symbol	Min	Max.	Recommand	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	kohm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10	50	50	kohm	to prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	50	kohm	It is not necessary to put pull-up resistance on RST_n(H/W reset) line if host does not use H/W reset.
Impedence on CLK/CMD/ DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_CLK	0	47	22	ohm	
Serial's resistance on CMD/ DAT0~7 Line	SR_CMD SR_DAT 0~7	0	47	0	ohm	
VDDQ Capacitor value	C1 & C2	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDDQ and VSSQ as closely as possible
VDD Capacitor value(≤ 4Stack)	C3 & C4	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDD and VSS as closely as possible
VDD Capacitor value(≥ 4Stack)	C3 & C4	2.2 + 0.1	4.7 + 0.22	4.7+0.22	uF	
VDDi capacitor value	C_{reg}	1	4.7 + 0.1	1 +0.1	uF	Coupling capacitor should be connected with VDDi and VSSi as closely as possible

4.6 Bus timing

Figure 6: Timing diagram: data input / output

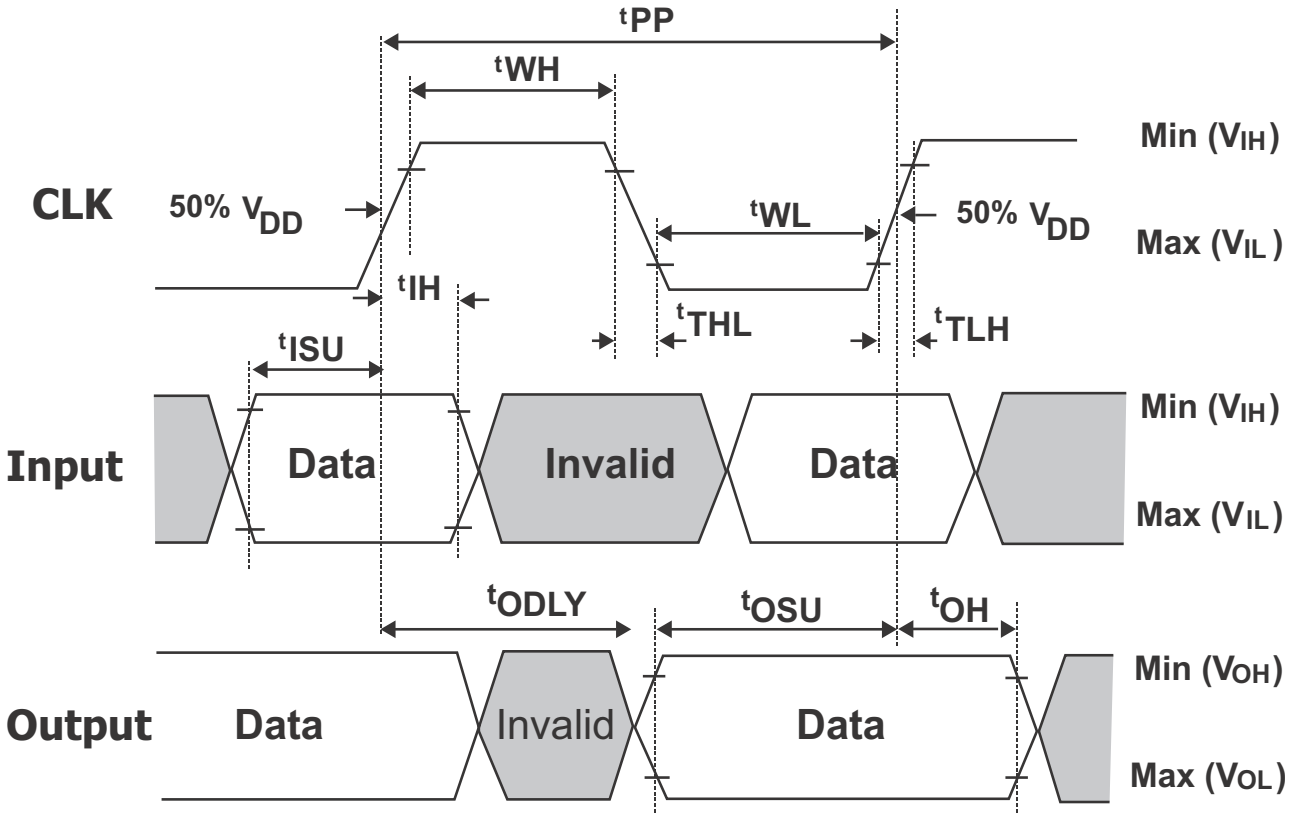


Figure 6: Timing diagram: data input / output

Data must always be sampled on the rising edge of the clock.

4.6.1 Card interface timings

Table 6 : High-speed card interface timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK(1)					
Clock frequency Data Transfer Mode (PP)(2)	f_{PP}	0	52(3)	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock rise time(4)	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	C_L <= 30 pF
Output hold time	t_{OH}	2.5		ns	C_L <= 30 pF
Signal rise time(5)	t_{rise}		3	ns	C_L <= 30 pF
Signal fall time	t_{fall}		3	ns	C_L <= 30 pF

NOTE 1. CLK timing is measured at 50% of VDD.
NOTE 2. A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
NOTE 3. Card can operate as high-speed card interface timing at 26 MHz clock frequency.
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 7 : Backward-compatible card interface timing

Parameter	Symbol	Min	Max.	Unit	Remark(1)
Clock CLK(2)					
Clock frequency Data Transfer Mode (PP)(3)	f_{PP}	0	26	MHz	CL <= 30 pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10		ns	CL <= 30 pF
Clock rise time(4)	t_{TLH}		10	ns	CL <= 30 pF
Clock fall time	t_{THL}		10	ns	CL <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	CL <= 30 pF
Input hold time	t_{IH}	3		ns	CL <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time(5)	t_{OSU}	11.7		ns	CL <= 30 pF
Output hold time(5)	t_{OH}	8.3		ns	CL <= 30 pF

NOTE 1. The card must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

NOTE 2. CLK timing is measured at 50% of VDD.

NOTE 3. For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.

NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

NOTE 5. tOSU and tOH are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the systemor to use slow clock frequency, so that host could have data set up margin for those devices.
In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

4.7 Bus timing for DAT signals during 2X data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. the CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 12.7, therefore there is no timing change for the CMD signal.

Figure 7: Timing diagram: data input/output in dual data rate mode

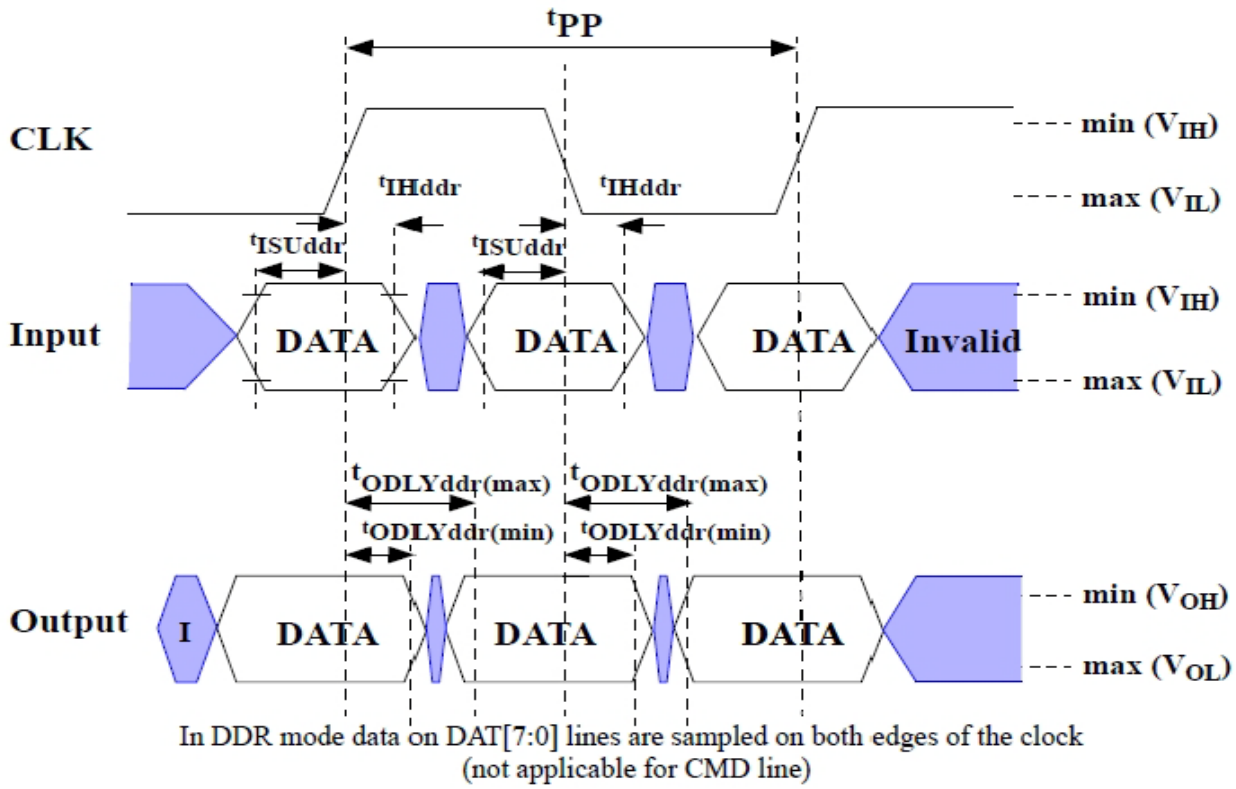


Table 8 : Dual data rate interface timings

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK(1)					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Inputs CMD, DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUDDR}	2.5		ns	C_L <= 20 pF
Input hold time	t_{IHDDR}	2.5		ns	C_L <= 20 pF
Outputs CMD, DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYDDR}$	1.5	7	ns	C_L <= 20 pF
Signal rise time(all signal)2	t_{RISE}		2	ns	C_L <= 20 pF
Signal fall time (all signal)	t_{FALL}		2	ns	C_L <= 20 pF

NOTE 1. CLK timing is measured at 50% of VDD.

NOTE 2. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

5. MultimediaCard functional description

All communication between the host and the device is controlled by the host (master). The following section provides an overview of the identification and data transfer modes, commands, dependencies, various operation modes and restrictions for controlling the clock signal. For detailed information, refer to section 7 of the JEDEC Standard Specification No. JESD84-A441.

5.1 General

All communication between host and card is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

- **Broadcast commands**

Broadcast commands are intended for all cards in a MultiMediaCard system2. Some of these commands require a response.

- **Addressed (point-to-point) commands**

The addressed commands are sent to the addressed card and cause a response from this card.

- **Boot mode**

The card will be in boot mode after power cycle, reception of CMD0 with arguement of 0xF0F0F0F0 or (*e*-NAND only) assertion of hardware reset signal.

- **Card identification mode**

The card will be in card identification mode after boot operation mode is finished or if host and /or card does not support boot operation mode. The card will be in this mode, until the SET_RCA command (CMD3) is received.

- **Interrupt mode**

Host and card enter and exit interrupt mode simultaneously. In interrupt mode there is no data transfer.
The only message allowed is an interrupt service request from the card or the host.

- **Data transfer mode**

The card will enter data transfer mode once an RCA is assigned to it. The host will enter data transfer mode after identifying the card on the bus.

- **Inactive mode**

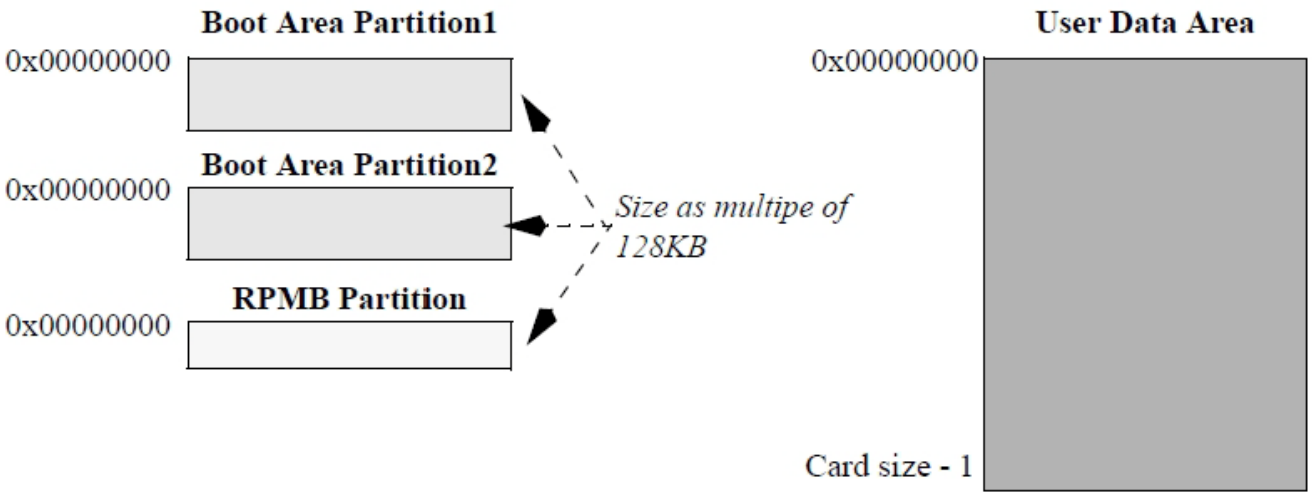
The card will enter inactive mode mode either card operating voltage range or access mode is not valid. The card can also enter inactive mode with Go_INACTIVE_STATE command (CMD15). The card will reset to *Pre-idle* state with power cycle.

5.2 Partition Management

The default area of the memory device consists of a User Data Area to store data, two possible boot area partitions for booting and the Replay Protected Memory Block Area Partition to manage data in an authenticated and replay protected manner. For detailed information regarding Command restrictions, configure partitions and Access partitions , refer to section 7.2 of the JEDEC Standard Specification No. JESD84-A441 .

The memory configuration initially consists (before any partitioning operation) of the User Data Area and RPMB Area Partitionsm and Boot Area Partitions (whose dimensions and technology features are defined by Hynix).

Figure 8: e-NAND memory organization at time zero



The embedded device offers also the possibility of configuring by the host additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block Area scan be classified as follows:

- Two Boot Area Partitions, whose size is multiple of 128 KB and from which booting from *e-NAND* can be performed.
- One RPMB Partition accessed through a trusted mechanism, whose size is defined as multiple of 128 KB.
- Four General Purpose Area Partitions to store sensitive data or for other host usage models and whose size is multiple of a Write Protect Group.

Each of the General Purpose Area Partitions can be implemented with enhanced technological features (such as better reliability*) that distinguish them from the default storage media. If the enhanced storage media feature is supported by the device, boot and RPMB Area Partitions shall be implemented as enhanced storage media by default.

Boot and RPMB Area Partitions' sizes and attributes are defined by the memory manufacturer (read-only), while General Purpose Area Partitions' sizes and attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

5.3 Boot operation mode

In boot operation mode, the master (MultiMediaCard host) can read boot data from the slave (e-NAND device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For detailed information regarding card reset to Pre-idle state, boot partition, boot operation, alternative boot operation, access boot partition, boot bus width and data access configuration and boot partition write protection refer to section 7.3 of the JEDEC Standard Specification No. JESD84-A441 .

5.4 Card identification mode

While in card identification mode the host resets the card, validates operation voltage range and access mode, identifies the card and assigns a Relative Card Address (RCA) to the card on the bus. All data communication in the Card Identification Mode uses the command line (CMD) only. For detailed information regarding card reset, operating voltage range validation, access mode validation, From busy to ready and Card identification process, refer to section 7.4 of the JEDEC Standard Specification No. JESD84-A441.

5.5 Interrupt mode

The interrupt mode on the MultiMediaCard system enables the master (MultiMediaCard host) to grant the transmission allowance to the slaves (card) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a card request for service. Supporting MultiMediaCard interrupt mode is an option, both for the host and the card. For detailed information, refer to section 7.5 of the JEDEC Standard Specification No. JESD84-A441.

5.6 Data transfer mode

When the card is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. Until the contents of the CSD register is known by the host, the fPP clock rate must remain at fOD. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g., block length, card storage capacity, maximum clock rate, etc. For detailed information regarding command sets and extended settings, High-speed mode selection, power class selection,bus testing procedure, bus width selection, data read, data write, erase, secure erase, secure trim, TRIM, write protect management, Card lock/unlock operation, application-specific commands, Sleep(CMD5), Replay Protected Memory Block, Dual data rate mode selection and Dual data rate mode operation, refer to section 7.6 of the JEDEC Standard Specification No. JESD84-A441.

5.7 Clock control

The MultiMediaCard bus clock signal can be used by the host to put the card into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For detailed information refer to section 7.7 of the JEDEC Standard Specification No. JESD84-A441.

5.8 Error conditions

For detailed information refer to section 7.8 of the JEDEC Standard Specification No. JESD84-A441.

5.9 Minimum performance

For detailed information refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A441.

5.10 Commands

For detailed information refer to section 7.10 of the JEDEC Standard Specification No. JESD84-A441.

5.11 State transition

For detailed information refer to section 7.11 and 7.13 of the JEDEC Standard Specification No. JESD84-A441.

5.12 Response

For detailed information refer to section 7.12 of the JEDEC Standard Specification No. JESD84-A441.

5.13 Memory array partitioning

The basic unit of data transfer to/from the e-NAND is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.
For block oriented commands, the following definition is used:

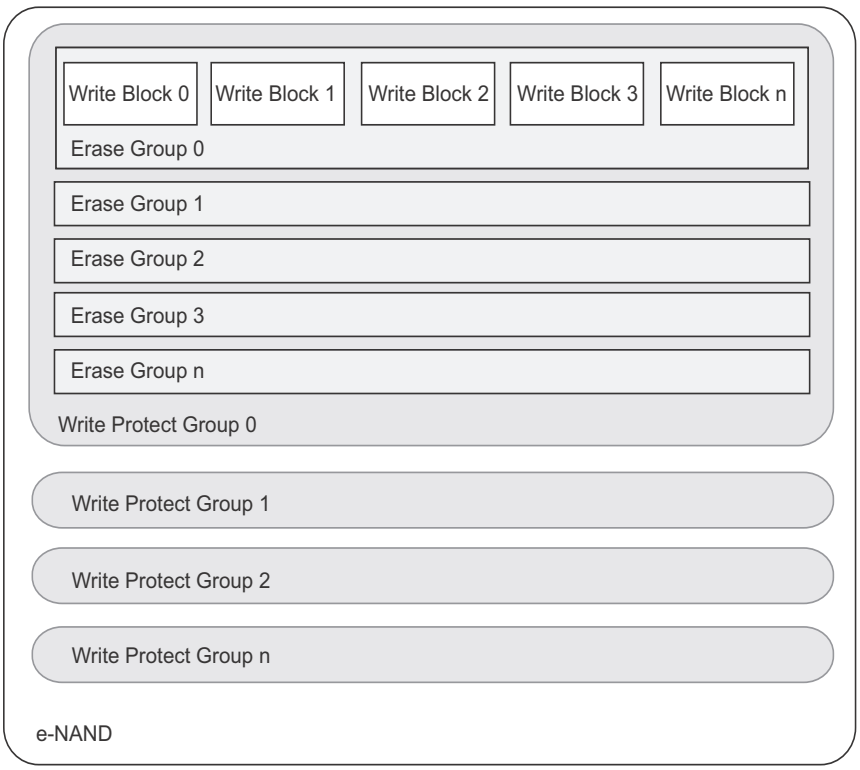
• **Block**: is the unit which is related to the block oriented read and write commands. Its size is the number of bytes which will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.

For R/W cards, special erase and write protect commands are defined:

• The granularity of the erasable units is the **Erase Group:** The smallest number of consecutive write blocks which can be addressed for erase. The size of the Erase Group is card specific and stored in the CSD when ERASE_GROUP_DEF is disabled, and in the EXT_CSD when ERASE_GROUP_DEF is enabled.

• The granularity of the Write Protected units is the **WP-Group:** The minimal unit which may be individually write protected. Its size is defined in units of erase groups. The size of a WP-group is card specific and stored in the CSD when ERASE_GROUP_DEF is disabled, and in the EXT_CSD when ERASE_GROUP_DEF is enabled.

Figure 9: Memory array partitioning



5.14 Timings

For detailed information refer to section 7.15 of the JEDEC Standard Specification No. JESD84-A441.

6. Device registers

There are five different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (driver stage register)
- Extended card specific data register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands (refer to section 8 of the JEDEC Standard Specification No. JESD84-A441. The device does not implement the DSR register.

The MultiMediaCard has a status register to provide information about the device current state and completion codes for the last host command.

6.1 Operation conditions register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the card and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by all cards. For detailed information, refer to section 8.1 of the JEDEC Standard Specification No. JESD84-A441.

If the host tries to change the OCR values during an initialization procedure the changes in the OCR content will be ignored.

The level coding of the OCR register is as follows:

- Restricted voltage windows = Low
- Device busy = Low

Table 9 : OCR register definition

OCR bit	Description	MultiMediaCard
6 to 0	Reserved	000 0000b
7	V_{CCQ}	1b
14 to 8	2.0 - 2.6	000 0000b
23 to 15	2.7 - 3.6 (High VCCQ range)	1 1111 1111b
28 to 24	Reserved	0 0000b
30 to 29	Access mode	10b (sector mode)
31	Power-up status bit (busy)(1)	

1. This bit is set to Low if the device has not finished the power-up routine.

6.2 Card identification (CID) register

The CID register is 16-byte long and contains a unique card identification number used during the card identification procedure. It is a 128-bit wide register with the content as defined in *Table11*. It is programmed during device manufacturing and can not be changed by MultiMediaCard hosts. For details, refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A441.

Table 10 : Card identification (CID) register

Name	Field	Width	CID - slice	CID - value				Note
				4GB	8GB	16B	32GB	
Manufacturer ID	MID	8	[127:120]	90h				
Reserved		6	[119:114]	00_0000b				
Card/BGA	CBX	2	[113:112]	01b				BGA
OEM/application ID	OID	8	[111:104]	4ah				
Product name	PNM	48	[103:56]	4e495820h				HYNIX
Product revision	PRV	8	[55:48]	70h				
Product serial number	PSN	32	[47:16]					
Manufacturing date	MDT	8	[15:8]					
CRC7 checksum	CRC	7	[7:1]					
Not used, always '1'	Reserved	1	[0:0]	TBD				

6.3 Card specific data register(CSD)

All the configuration information required to access the device data is stored in the CSD register. The MSB bytes of the register contain the manufacturer data and the two least significant bytes contains the host controlled data (the device copy, write protection and the user ECC register).

The host can read the CSD register and alter the host controlled data bytes using the SEND_CSD and PROGRAM_CSD commands.

In *Table12,* the cell type column defines the CSD field as read only (R), one time programmable (R/W) or erasable (R/W/E). The programmable part of the register (entries marked by W or E) can be changed by command CMD27.

The copy bit in the CSD can be used to mark the device as an original or a copy. Once set it cannot be cleared. The device can be purchased with the copy bit set (copy) or cleared, indicating the device is a master.

The one time programmable (OTP) characteristic of the copy bit is implemented in the MultiMediaCard controller firmware and not with a physical OTP cell.

For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A441.

Table 11 : Card specific data register

Name	Field	Width	Cell Type	CID - slice	CID - value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
MultiMediaCard protocol version	SPEC_VERS	4	R	[125:122]	4h
Reserved		2	R	[121:120]	0
Data read access-time-1	TAAC	8	R	[119:112]	4fh
Data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. data transfer rate	TRAN_SPEED	8	R	[103:96]	32h
Command classes	CCC	12	R	[95:84]	f5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved		2	R	[75:74]	0
Device size	C_SIZE	12	R	[73:62]	fffh
Max. read current at VCC(min)	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current at VCC(max)	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current at VCC(min)	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current at VCC(max)	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	7h/fh/1fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved				[20:20]	0
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GROUP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h

Table 12 : Card specific data register (continued)

Name	Field	Width [bits]	Cell Type	CID - slice	CID - value
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code 2 R/W/E none 0	ECC	2	R/W/E	[9:8]	0h
CRC	CRC	7	R/W/E	[7:1]	28h/30h/00h
Not used, always '1'		1	-	[0:0]	1h

6.4 Extended CSD register

The extended CSD register defines the device properties and selected modes. It is 512-byte long. The 320 most significant bytes are the properties segment that defines the device capabilities and cannot be modified by the host. The 192 lower bytes are the modes segment that defines the configuration the device is working in. For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A441.These modes can be changed by the host by means of the Switch command.

Table 13. Extended CSD(1)

Name	Field	Size (bytes)	Cell Type	CID - slice	CID - slice value			
					4GB	8GB	16GB	32GB
Properties segment								
Reserved[1]		7	TBD	[511:505]				
Supported command sets	S_CMD_SET	1	R	[504]	01h			
HPI features	HPI_FEATURES	1	R	[503]	03h			
Background operations support	BKOPS_SUPPORT	1	R	[502]	01h			
Reserved[1]		255	TBD	[501:247]				
Background operations status	BKOPS_STATUS	1	R	[246]	00h			
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	00000000h			
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	6eh	6eh	dah	TBD
Reserved[1]		1	TBD	[240]				
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	00h			
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	00h			
Reserved[1]		2	TBD	[237:236]				
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	00h			
Reserved[1]		1	TBD	[233]				
TRIM Multiplier	TRIM_MULT	1	R	[232]	0fh			
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	15h			
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	06h			
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	09h			
Boot information	BOOT_INFO	1	R	[228]	07h			
Reserved[1]		1	TBD	[227]				
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	10h	10h	20h	TBD
Access size	ACC_SIZE	1	R	[225]	06h	07h	07h	TBD
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	8h	10h	10h	TBD
High_capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	01h			
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	08h			
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	01h	01h	02h	TBD
Sleep current(VCC)	S_C_VCC	1	R	[220]	08h			
Sleep current(VCCQ)	S_C_VCCQ	1	R	[219]	08h			
Reserved[1]		1	TBD	[218]				
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	10h			
Reserved[1]		1	TBD	[216]				
Sector Count	SEC_COUNT	4	R	[215:212]	7380 00h	e740 00h	01d74 000h	TBD
Reserved[1]		1	TBD	[211]				
Minimum Write Performance for 8bit at52MHz	MIN_PERF_W_8_52	1	R	[210]	08h			
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	08h			
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	08h			
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	08h			
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	08h			
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	08h			
Reserved[1]		1	TBD	[204]				
Power class for 26MHz at 3.6V	PWR_CL_26_360	1	R	[203]	00h			
Power class for 52MHz at 3.6V	PWR_CL_52_360	1	R	[202]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Power class for 26MHz at 1.95V	PWR_CL_26_195	1	R	[201]	00h			
Power class for 52MHz at 1.95V	PWR_CL_52_195	1	R	[200]	00h			
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	01h			
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	02h			
Reserved[1]		1	TBD	[197]				
Card type	CARD_TYPE	1	R	[196]	0Fh			
Reserved[1]		1	TBD	[195]				
CSD structure version	CSD_STRUCTURE	1	R	[194]	02h			
Reserved[1]		1	TBD	[193]				
Extended CSD revision	EXT_CSD_REV	1	R	[192]	05h			
Modes Segment								
Command set	CMD_SET	1	R/W/E_P	[191]	00h			
Reserved[1]		1	TBD	[190]				
Command set revision	CMD_SET_REV	1	R	[189]	00h			
Reserved[1]		1	TBD	[188]				
Power class	POWER_CLASS	1	R/W/E_P	[187]	00h			
Reserved[1]		1	TBD	[186]				
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	00h			
Reserved[1]		1	TBD	[184]				
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	00h			
Reserved[1]		1	TBD	[182]				
Erased memory content	ERASED_MEM_CONT	1	R	[181]	00h			
Reserved[1]		1	TBD	[180]				
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/ WE_P	[179]	00h			
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/ C_P	[178]	00h			
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	00h			
Reserved[1]		1	TBD	[176]				
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Reserved[1]		1	TBD	[174]				
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	00h			
Reserved[1]		1	TBD	[172]				
User area write protection register	USER_WP	1	R/W,R/W/C_P & R/W/E_P	[171]	00h			
Reserved[1]		1	TBD	[170]				
FW configuration	FW_CONFIG	1	R/W	[169]	00h			
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	10h	10h	20h	TBD
Write reliability setting register	WR_REL_SET	1	R/W	[167]	00h			
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	00h			
Reserved[1]		1	TBD	[165]				
Manually start background operations	BKOPS_START	1	W/E_P	[164]	00h			
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	00h			
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	00h			
HPI management	HPI_MGMT	1	R/W/E_P	[161]	00h			
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	03h			
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	00019Ah	00019Ah	00019Ah	TBD
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h			
Paritioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h			
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	00h			
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	00h			
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	00h			
Reserved[1]		1	TBD	[135]				
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h			
Reserved[1]		1	TBD	[133:0]				

NOTE 1. Reserved bits should read as “0.”

6.5 RCA (relative card address)

registerThe writable 16-bit relative card address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-card communication after the device identification procedure. The default value of the RCA register is '0x0001'. The value '0x0000' is reserved to set all cards into the standby statewith CMD7. For details refer to section 8.5 of the JEDEC Standard Specification No. JESD84-A441.

6.6 DSR (driver stage register) register

The 16-bit driver stage register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices on the bus). The CSD register contains the information concerning the DSR register usage.

The default value of the DSR register is '0x404'. For details refer to section 8.6 of the JEDEC Standard Specification No. JESD84-A441.

Appendix

1. User data area size

Density	Sec_Count	Memory Capacity
16GB	01D74000h	15080MB

2. Boot & RPMB Size

Density	Boot partition 1	Boot partition 2	RPMB
16GB	4MB	4MB	4MB

3. Erase unit & Write protect group size

Density	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	ERASE unit size(MB)	Write protect Group Size(MB)
16GB	10h	02h		

4Gb (128Mb x 32)

4Gb LPDDR2-S4B SDRAM M-Die

Addressing Table

Parameter	4Gb	
	x16	x32
Configuration	32Mb x 8banks x 16	16Mb x 8banks x 32
Bank Address	BA0 ~ BA2	BA0 ~ BA2
Row Address	R0 ~ R13	R0 ~ R13
Column Address	C0 ~ C10	C0 ~ C9

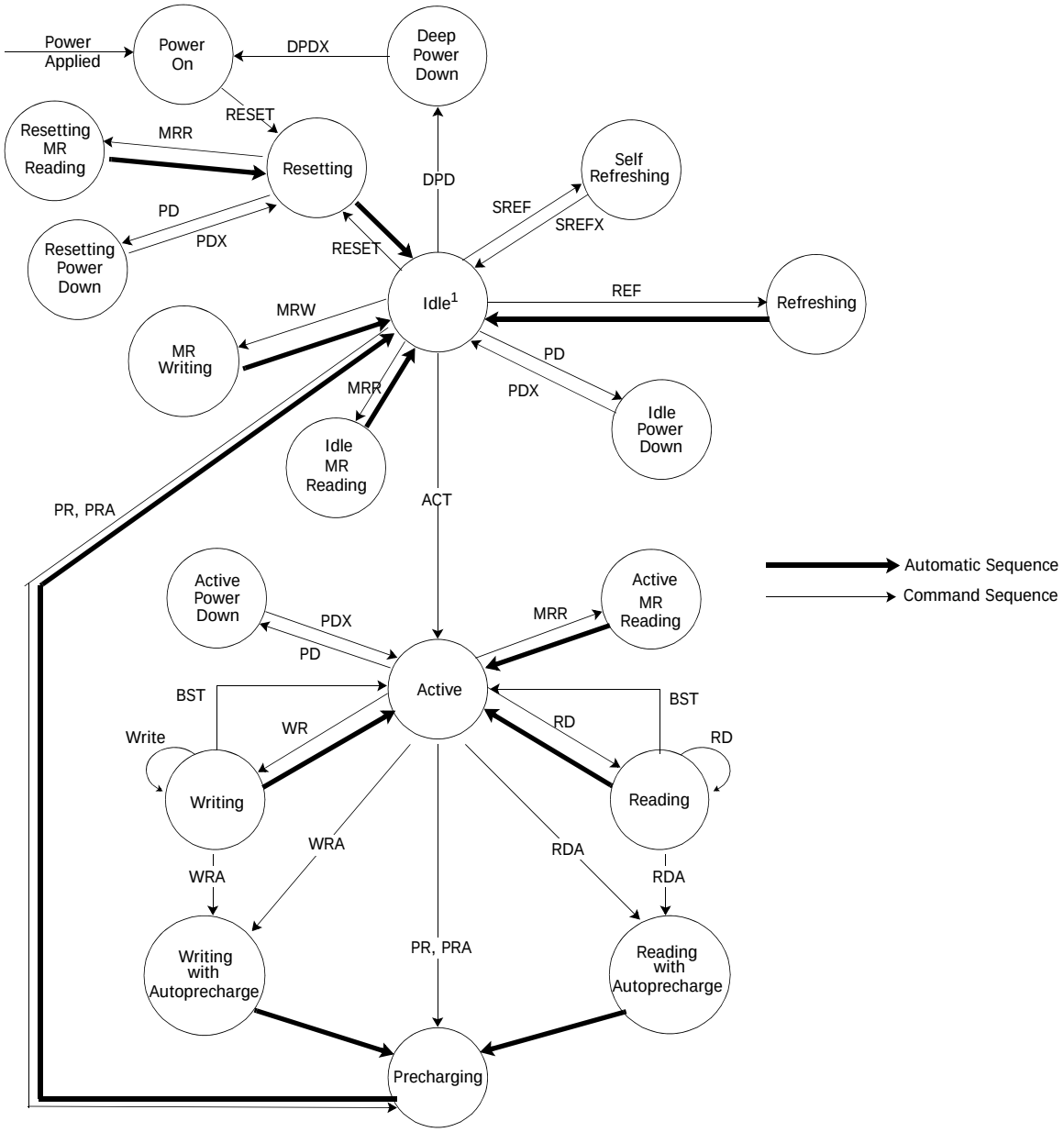
Note:
1. The least-significant column address CA0 is not transmitted on the CA bus, and is implied to be zero.
2. Row and Column Address values on the CA bus that are not used don't care.

LPDDR2 SDRAM PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ0-DQ15 (x16) DQ0-DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
DQS0_t -DQS1_t, DQS0_c - DQS1_c (x16) DQS0_t -DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7 and DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t. For x32, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0-DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a WRITE access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c) loading. DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1**
VDD2	Supply	**Core Power Supply 2**
VDDCA	Supply	**Input Receiver Power Supply**: Power for CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply**: Power supply for data input/output buffers.
VREFCA	Supply	**Reference Voltage for CA Command and Control Input Receiver**: Reference voltage for all CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VREFDQ	Supply	**Reference Voltage for DQ Input Receiver**: Reference voltage for all Data input buffers.
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

Note 1. Data includes DQ and DM

STATE DIAGRAM



PD = Enter Power Down
PDX = Exit Power Down
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
PR(A) = Precharge (All)
MRW = Mode Register Write
MRR = Mode Register Read

SREF = Enter Self Refresh
SREFX = Exit Self Refresh
REF = Refresh
BST = Burst Terminate
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
RESET = Reset is achieved through MRW command

Note 1. For LPDDR2 SDRAM in the Idle state, all banks are precharged.

POWER-UP, INITIALIZATION and POWER-OFF

LPDDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to the device.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.
On or before the completion of the power ramp (Tb) CKE must be held low.
DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up.
CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

The following conditions apply:
Ta is the point where any power supply first reaches 300 mV.
After Ta is reached, VDD1 must be greater than VDD2 - 200 mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200 mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
After Ta is reached, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.
The above conditions apply between Ta and power-off (controlled or uncontrolled).
Tb is the point when all supply voltages and reference voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.
For supply and reference voltage operating conditions, see the section of AC and DC Operating Condition.
Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.

Note: VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

2. CKE and clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100 ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK} prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).
The clock period shall be within the range defined for tCKb (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.
While keeping CKE high, issue NOP commands for at least tINIT3 = 200 us. (Td).

3. Reset command

After tINIT3 is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW(Reset) command. Wait for at least tINIT4 = 1 us while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.
Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see the section of "Power-down").
The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.
As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.
After the DAI-bit (MR0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0.

The SDRAM will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (see the section of "Mode Register Definition").

5. ZQ Calibration:

After tINIT5 (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For LPDDR2 devices which do not support the ZQ Calibration command (meaning that RON is connected to VDDCA), this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:

After tZQINIT (Tg), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2 and MR3 shall be set to configure the memory for the target frequency and memory configuration.
To support simple boot from the NVM, some Mode Registers are reset to default values during Device Auto-Initialization. See the Mode Register section of this specification for default values.
The LPDDR2 device will now be in IDLE state and ready for any valid command.
After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section "Input clock stop and frequency change".

Table. Timing Parameters for initialization

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Power Ramp Time	-	20	ms
tINIT1	Minimum CKE low time after completion of power ramp	100	-	ns
tINIT2	Minimum stable clock before first CKE high	5	-	tCK
tINIT3	Minimum idle time after first CKE assertion	200	-	us
tINIT4	Minimum idle time after Reset command	1	-	us

Symbol	Parameter	Value		Unit
		min	max	
tINIT5	Maximum duration of Device Auto-Initialization	-	10	us
tZQINIT	ZQ Initial Calibration for LPDDR2-S4 devices	1		us
tCKb	Clock cycle time during boot	18	100	ns

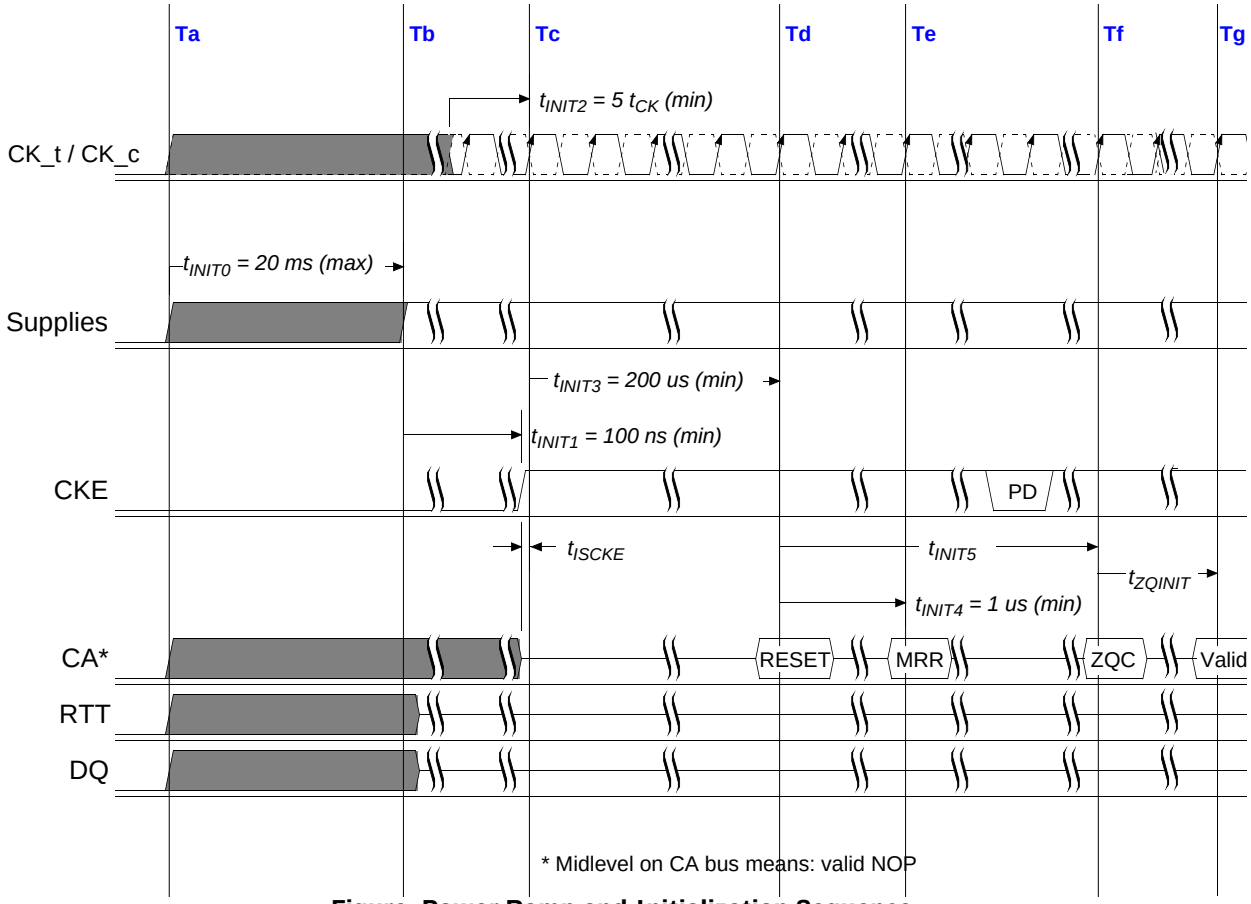


Figure. Power Ramp and Initialization Sequence

Initialization After Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the re-installation procedure shall begin with step 3 (Td).

Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to the devices.

While removing power, CKE shall be held at a logic low level (≤ 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.
Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.
The time between Tx and Tz(tPOFF) shall be less than 2s.
The following conditions apply:
- Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.
- Between Tx and Tz, VDD1 and VDD2 must be greater than VDDCA - 200 mV.
- Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
- Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.
For supply and reference voltage operating conditions, see the section of AC and DC Operating Conditions.

Note: VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

Table. Timing Parameters for Uncontrolled Power-off

Symbol	Parameter	Value		Unit
		min	max	
tPOFF	Maximum Power-off ramp time	-	2	s

Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition. Unless specified otherwise, these steps are mandatory and apply to the devices.
Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.
Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.
VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.
Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

Mode Register Definition

Table below shows the mode registers for LPDDR2 SDRAM.
Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.
Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table. Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	(RFU)			RZQI (Optional)		DNVI	DI	DAI	go to MR0
1	01H	Device Feature1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02H	Device Feature 2	W	(RFU)					RL & WL			go to MR2
3	03H	I/O Config-1	W	(RFU)					DS			go to MR3
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			go to MR4
5	05H	Basic Config-1	R	Manufacturer ID								go to MR5
6	06H	Basic Config-2	R	Revision ID1								go to MR6
7	07H	Basic Config-3	R	Revision ID2								go to MR7
8	08H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	0AH	IO Calibration	W	Calibration Code								go to MR10
16	10H	PASR_Bank	W	Bank Mask								go to MR16
17	11H	PASR_Segment	W	Segment Mask								go to MR17
32	20H	DQ Calibration Pattern A	R	See the section of DQ Calibration								go to MR32
40	28H	DQ Calibration Pattern B	R	See the section of DQ Calibration								go to MR40
63	3FH	Reset	W	X								go to MR63

Note:
1. RFU bits shall be set to `0' during Mode Register writes.
2. RFU bits shall be read as `0' during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impacts on the functionality of the device.

MR0 Device Information (MA<7:0> = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI (Optional)		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0B: DAI complete	
			1B: DAI still in progress	
DI (Device Information)	Read-only	OP1	0B: SDRAM	
DNVI (Data Not Valid Information)	Read-only	OP2	0B: DNV not supported	
RZQI (Built in Self Test for RZQ Information)	Read-only	OP4:OP3	00B: ZQ self test not supported 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD or float nor short to GND)	

Note:
1. LPDDR2 SDRAM will not implement DNV functionality.
2. If DNV functionality is not implemented, the device shall not drive the DM/DNV signals.
3. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
4. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
5. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
6. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm +/-1%).

MR1 Device Feature 1 (MA<7:0> = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	010B: BL4 (default)	
			011B: BL8	
			100B: BL16	
			All others: reserved	
BT	Write-only	OP<3>	0B: Sequential (default)	1
			1B: Interleaved	
WC	Write-only	OP<4>	0B: Wrap (default)	
			1B: No wrap (allowed for BL4 only)	

nWR	Write-only	OP<7:5>	001B: nWR=3 (default)	2
			010B: nWR=4	
			011B: nWR=5	
			100B: nWR=6	
			101B: nWR=7	
			110B: nWR=8	
			All others: reserved	

Note:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU (tWR/tCK).

Table. Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0B	0B	wrap	any	4	0	1	2	3												
X	X	1B	0B				2	3	0	1												
X	X	XB	0B	nw	any		y	y+1	y+2	y+3												
X	0B	0B	0B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0B	1B	0B				2	3	4	5	6	7	0	1								
X	1B	0B	0B				4	5	6	7	0	1	2	3								
X	1B	1B	0B				6	7	0	1	2	3	4	5								
X	0B	0B	0B		int		0	1	2	3	4	5	6	7								
X	0B	1B	0B				2	3	0	1	6	7	4	5								
X	1B	0B	0B				4	5	6	7	0	1	2	3								
X	1B	1B	0B				6	7	4	5	2	3	0	1								
X	X	X	0B	nw	any		illegal (not allowed)															
0B	0B	0B	0B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B	0B	1B	0B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0B	1B	0B	0B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0B	1B	1B	0B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1B	0B	0B	0B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1B	0B	1B	0B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1B	1B	0B	0B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1B	1B	1B	0B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0B		int		illegal (not allowed)															
X	X	X	0B	nw	any		illegal (not allowed)															

Note:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table. Non Wrap Restrictions below for the respective density and bus width combinations.
6. 'nw' means Non Wrap. 'any' means Sequential and interleaved. 'seq' means sequential and 'int' means interleaved.

Table. Non Wrap Restrictions

4Gb	
Not across full page boundary	
x16	7FE,7FF,000,001
x32	3FE,3FF,000,001
Not across sub page boundary	
x16	3FE,3FF,400,401
x32	None

Note: Non-wrap BL=4 data-orders shown above are prohibited.

MR2 Device Feature 2 (MA<7:0> = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	0001B: RL3/WL1(default)	
			0010B: RL4/WL2	
			0011B: RL5/WL2	
			0100B: RL6/WL3	
			0101B: RL7/WL4	
			0110B: RL8/WL4	
			All others: reserved	

MR3 I/O Configuration 1 (MA<7:0> = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	0000B: reserved	
			0001B: 34.3Ω	
			0010B: 40Ω (default)	
			0011B: 48Ω	
			0100B: 60Ω	
			0101B: reserved	
			0110B: 80Ω	
			0111B: 120Ω	
			All others: reserved	

MR4 Refresh Mode (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

Refresh Rate	Read-only	OP<2:0>	000B: reserved
			001B: 4 x tREFI, 4 x tREFIpb, 4 x tREFW
			010B: 2 x tREFI, 2 x tREFIpb, 2 x tREFW
			011B: 1 x tREFI, 1 x tREFIpb, 1 x tREFW (≤ 85°C)
			100B: reserved
			101B: 0.25 x tREFI, 0.25 x tREFIpb, 0.25 x tREFW, do not de-rate AC timing
			110B: 0.25 x tREFI, 0.25 x tREFIpb, 0.25 x tREFW, de-rate AC timing
			111B: 0.25X tREFI, High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<2:0>	0B: OP<2:0> value has not changed since last read of MR4 1B: OP<2:0> value has changed since last read of MR4

Note:
1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up
3. If OP2 equals `1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000B or 111B.
6. See the section of Temperature Sensor for information on the recommended frequency of reading MR4.
7. Some of the code for Refresh rate are not supported. Please ask Hynix office in detail.
8. LPDDR2-S4 devices shall be de-rated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in "AC timing table". Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

MR5 Basic Configuration1 (MA<7:0> = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Company ID	Read-only	OP<7:0>	0000 0110B: Hynix Semiconductor	

MR6 Basic Configuration2 (MA<7:0> = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 1							

Revision ID1	Read-only	OP<7:0>	00000001B: A-version	

MR7 Basic Configuration3 (MA<7:0> = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 2							

Revision ID2	Read-only	OP<7:0>	00000000B: A-version	

MR8 Basic Configuration4 (MA<7:0> = 08BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	00B: S4 SDRAM
Density	Read-only	OP<5:2>	0110B: 4Gb
I/O width	Read-only	OP<7:6>	00B: x32
			01B: x16

MR9 Test Mode (MA<7:0> = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 ZQ Calibration (MA<7:0> = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write Only	OP<7:0>	1111 1111B: Calibration command after initialization
			1010 1011B: Long Calibration
			0101 0110B: Short Calibration
			1100 0011B: ZQ Reset
			others: reserved

Note:
1. Host processor shall not write MR10 with "reserved" values
2. LPDDR2 devices shall ignore calibration command when a "reserved" value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see the section of "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQRESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR16 PASR Bank Mask (MA<7:0> = 10H)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Bank Mask							

S4 SDRAM

Bank Mask	Write-only	OP<7:0>	0B: refresh enable to the bank (default) 1B: refresh blocked (masked)

Note: For 4bank S4 SDRAM (64Mb ~ 512Mb), only OP<3:0> are used.

OP	Bank Mask	4-Bank LPDDR2-S4	8-Bank LPDDR2-S4
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

MR17 PASR Segment Mask (MA<7:0> = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment Mask	Write-only	OP<7:0>	0B: refresh enable to the segment (default) 1B: refresh blocked (masked)

Segment	OP	Segment Mask	4Gb
			R<13:11>
0	0	XXXXXXX1	000B
1	1	XXXXXX1X	001B
2	2	XXXXX1XX	010B
3	3	XXXX1XXX	011B
4	4	XXX1XXXX	100B
5	5	XX1XXXXX	101B
6	6	X1XXXXXX	110B
7	7	1XXXXXXX	111B

Note: This table indicates the range of row address in each masked segment. X is do not care for a particular segment.

MR32 DQ Calibration Pattern A (MA<7:0> = 20H): MRR only

Reads to MR32 return DQ Calibration Pattern A. See the section of DQ Calibration.

MR40 DQ Calibration Pattern B (MA<7:0> = 28H): MRR only

Reads to MR40 return DQ Calibration Pattern B. See the section of DQ Calibration.

MR63 Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: For additional information on MRW RESET, see Mode Register Write Command section.

TRUTH TABLE

Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

COMMAND TRUTH TABLE

Command	SDR Command Pins (2)			DDR CA Pins (10)										CK_t edge
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	falling
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	X								falling
Refresh (per bank)[11]	H	H	L	L	L	H	L	X						rising
			X	X										falling
Refresh (all bank)	H	H	L	L	L	H	H	X						rising
			X	X										falling
Enter Self Refresh	H	L	L	L	L	H	X							rising
	X		X	X										falling
Active (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	rising
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	falling
Write (bank)	H	H	L	H	L	L	X	X	C1	C2	BA0	BA1	BA2	rising
			X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Read (bank)	H	H	L	H	L	H	X	X	C1	C2	BA0	BA1	BA2	rising
			X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB[2]	X	X	BA0	BA1	BA2	rising
			X	X	X	X	X	X	X	X	X	X	X	falling
BST	H	H	L	H	H	L	L	X						rising
			X	X										falling
Enter Deep Power Down	H	L	L	H	H	L	X							rising
	X		X	X										falling
NOP	H	H	L	H	H	H	X							rising
			X	X										falling
Maintain SREF, PD, DPD (NOP)	L	L	L	H	H	H	X							rising
			X	X										falling
NOP	H	H	H	X										rising
			X	X										falling
Maintain SREF, PD, DPD (NOP)	L	L	H	X										rising
			X	X										falling
Enter Power Down	H	L	H	X										rising
	X		X	X										falling
Exit SREF, PD, DPD	L	H	H	X										rising
	X		X	X										falling

Note:
1. All commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP is significant only to SDRAM.
4. AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
5. “X” means “H or L (but a defined logic level)”
6. Self refresh exit and Deep Power Down exit are asynchronous.
7. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
8. CAxr refers to command/address bit “x” on the rising edge of clock.
9. CAxf refers to command/address bit “x” on the falling edge of clock.
10. CS_n and CKE are sampled at the rising edge of clock.
11. Per Bank Refresh is only allowed in devices with 8 banks.
12. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
13. AB “high” during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

CKE TRUTH TABLE

Current State*3	CKEn-1 *1	CKEn *1	CS_n *2	Command n *4	Operation n *4	Next State	Note
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter SELF REFRESH	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

Note:
1. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
2. "CS_n" is the logic state of CS_n at the clock rising edge n;
3. "Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7. SELF REFRESH exit time (tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least twice during the tXP period.
10. The clock must toggle at least twice during the tXSR time.
11. 'X' means `Don't care'.
12. Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	AUTO REFRESH(Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	AUTO REFRESH(All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7,8
	Precharge	Deactive row in bank or banks	Precharging	9, 15
Row Active	READ	Select Column, and start read burst	Reading	
	WRITE	Select Column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	READ	Select column, and start new read burst	Reading	10,11
	WRITE	Select column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	WRITE	Select Column, and start new write burst	Writing	10,11
	READ	Select column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: The bank or banks have been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
   Reading: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table “Current State Bank n - Command to Bank n”, and according to Table “Current State Bank n - Command to Bank m”.
   Precharging: starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the ‘Active’ state.
   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing (Per Bank): starts with registration of a REFRESH (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
Refreshing (All Bank): starts with registration of a REFRESH(All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
Precharging All: starts with the registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through MODE REGISTER WRITE command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BST must be used to end the READ prior to asserting a WRITE command.
13. Not bank-specific. BURST TERMINATE command affects the most recent read/write burst started by the most recent READ/WRITE command, regardless of bank.
14. A READ command may be applied after the completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting a READ command.
15. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Pre-charging	ACTIVATE	Select and activate row in Bank m	Row Active	7
	READ	Select column, and start read burst from Bank m	Reading	8
	WRITE	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10,11,13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	READ	Select column, and start read burst from Bank m	Reading	8
	WRITE	Select column, and start write burst to Bank m	Writing	8,14
	ACTIVATE	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	READ	Select column, and start read burst from Bank m	Reading	8,16
	WRITE	Select column, and start write burst to Bank m	Writing	8
	ACTIVATE	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	READ	Select column, and start read burst from Bank m	Reading	8,15
	WRITE	Select column, and start write burst to Bank m	Writing	8,14,15
	ACTIVATE	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	READ	Select column, and start read burst from Bank m	Reading	8,15,16
	WRITE	Select column, and start write burst to Bank m	Writing	8,15
	ACTIVATE	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Device Auto-Initialization	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: the bank has been precharged, and tRP has been met.
   Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

Reading: a READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Writing: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4. REFRESH, SELF REFRESH, and MODE REGISTER write commands may only be issued when all bank are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
7. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. MRR is allowed during the Row Activating state and MRW is prohibited during the Row Activating state. (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
14. A WRITE command may be applied after the completion of the READ burst, otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in the section of Precharge and Auto Precharge clarification are followed.
16. A READ command may be applied after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting a READ command.
17. Reset command is achieved through MODE REGISTER WRITE command.
18. BST is allowed only if a Read or Write burst is ongoing

DATA MASK TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Rating	Unit	Notes
Voltage on VDD1 relative to VSS	VDD1	-0.4 ~ 2.3	V	1
Voltage on VDD2 relative to VSS	VDD2	-0.4 ~ 1.6	V	1
Voltage on VDDCA relative to VSS	VDDCA	-0.4 ~ 1.6	V	1, 3
Voltage on VDDQ relative to VSS	VDDQ	-0.4 ~ 1.6	V	1, 2
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.4 ~ 1.6	V	
Storage Temperature	TSTG	-55 ~ 125	^{o}C	4

Note:
1. See "Power-Ramp" section in "Power-up, Initialization, and Power-Off" for relationships between power supplies.
2. VREFDQ ≤ 0.6 x VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.
3. VREFCA ≤ 0.6 x VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.
4. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power 1	VDD1	1.70	1.80	1.95	V
Core Power 2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

Note: 1. VDD1 uses significantly less power than VDD2.

Input Leakage Current

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage current For CA, CKE, CS_n, CK_t, CK_c Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	IL	-2	2	uA	2
VREF supply leakage current; VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	IVREF	-1	1	uA	1

Note:
1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

Operating Temperature

Parameter		Symbol	Min	Max	Unit	Note
Operating Temperature	Standard	T_{OPER}	-30	85	°C	1
	Extended		85	105		1

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard. Please ask to Hynix for the availability of Extended temperature range products.
2. Either the device case temperature rating or the temperature sensor may be issued to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

AC and DC Logic Input Levels for Single-Ended CA and CS_n Signals

Parameter	Symbol	LPDDR2 200 to 400		LPDDR2 533 to 1066		Unit	Note
		Min	Max	Min	Max		
CA and CS_n Inputs							
AC Input Logic High	VIHCA(AC)	VREF+0.3	Note 2	VREF+0.22	Note 2	V	1, 2
AC Input Logic Low	VILCA(AC)	Note 2	VREF - 0.3	Note 2	VREF - 0.22	V	1, 2
DC Input Logic High	VIHCA(DC)	VREF+0.2	VDDCA	VREF+0.13	VDDCA	V	1
DC Input Logic Low	VILCA(DC)	VSSCA	VREF - 0.2	VSSCA	VREF - 0.13	V	1
Reference Voltage for CA and CS_n Inputs	VREFCA(DC)	0.49*VDDCA	0.51*VDDCA	0.49*VDDCA	0.51*VDDCA	V	3, 4

Note:
1. For CA and CS_n input only pins. VREF = VREFCA(DC).
2. See the section of Overshoot and Undershoot Specifications.
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDCA/2 +/- 12 mV.

AC and DC Logic Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Note
CKE Inputs					
CKE Input High Level	VIHCKE	0.8*VDDCA	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.2*VDDCA	V	1

Note: 1. See the section of Overshoot and Undershoot Specifications.

AC and DC Logic Input Levels for Single-Ended Data (DQ and DM) Signals

Parameter	Symbol	LPDDR2 200 to 400		LPDDR2 533 to 1066		Unit	Note
		Min	Max	Min	Max		
Data Inputs (DQ and DM)							
AC Input High Voltage	VIHDQ(AC)	VREF+0.3	Note 2	VREF+0.22	Note 2	V	1, 2
AC Input Low Voltage	VILDQ(AC)	Note 2	VREF-0.3	Note 2	VREF-0.22	V	1, 2
DC Input High Voltage	VIHDQ(DC)	VREF+0.2	VDDQ	VREF+0.13	VDDQ	V	1
DC Input Low Voltage	VILDQ(DC)	VSSQ	VREF-0.2	VSSQ	VREF-0.13	V	1
Reference Voltage for DQ and DM Inputs	VREFDQ(DC)	0.49*VDDQ	0.51*VDDQ	0.49*VDDQ	0.51*VDDQ	V	3, 4

Note:
1. For DQ input only pins. VREF = VREFDQ(DC).
2. See the section of Overshoot and Undershoot Specifications.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDQ/2 +/- 12 mV.

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in Figure below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise). VDD stands for VDDCS for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDCA or VDDQ also over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table “Electrical Characteristics and Operating Conditions”. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD. VREF(t) cannot track noise on VDDQ or VDDCA if this would send VREF outside these specifications.

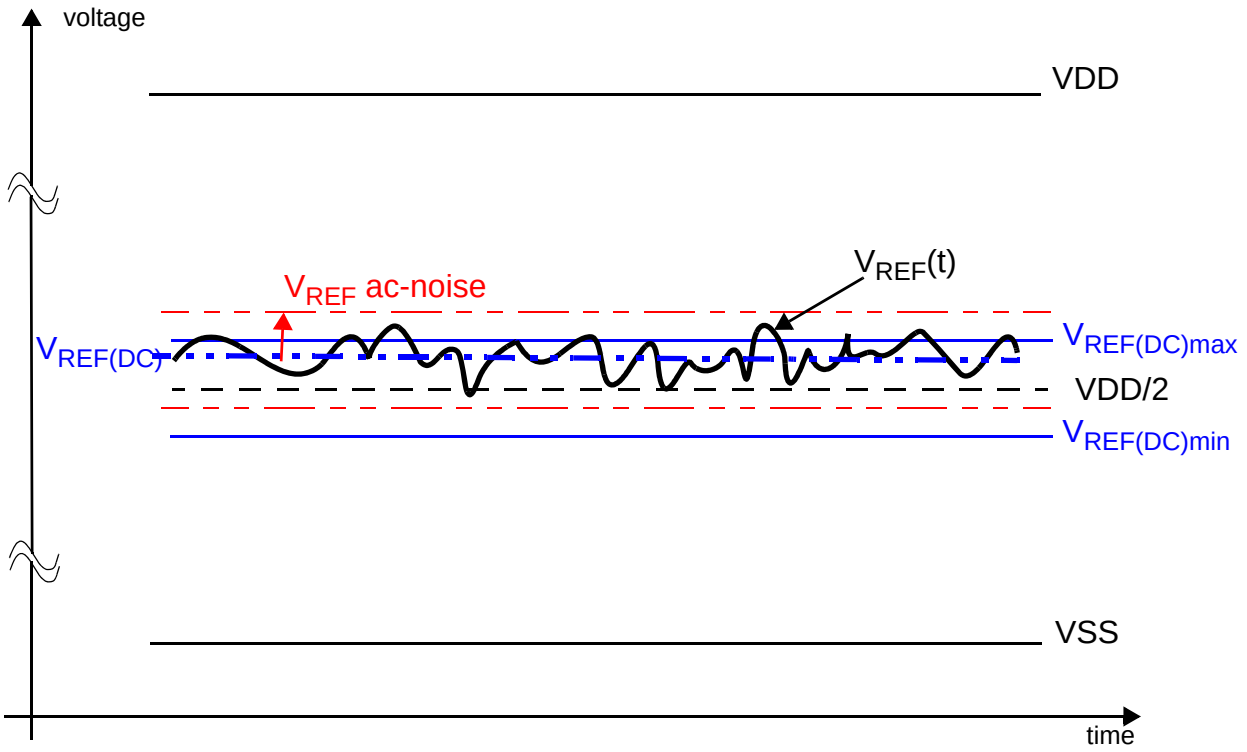


Figure. Illustration of VREF(DC) tolerance and VREF ac-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.
"VREF " shall be understood as VREF(DC), as defined in Figure above.
This clarifies that dc-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as VREF is maintained between 0.44 x VDDQ (or VDDCA) and 0.56 x VDDQ (or VDDCA) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VREF (see the Electrical Characteristics and Operating Conditions.) Therefore, system timing and voltage budgets need to account for VREF deviations outside of this range.
This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with VREF ac-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals (Clock and Strobe)

Differential Signal Definition

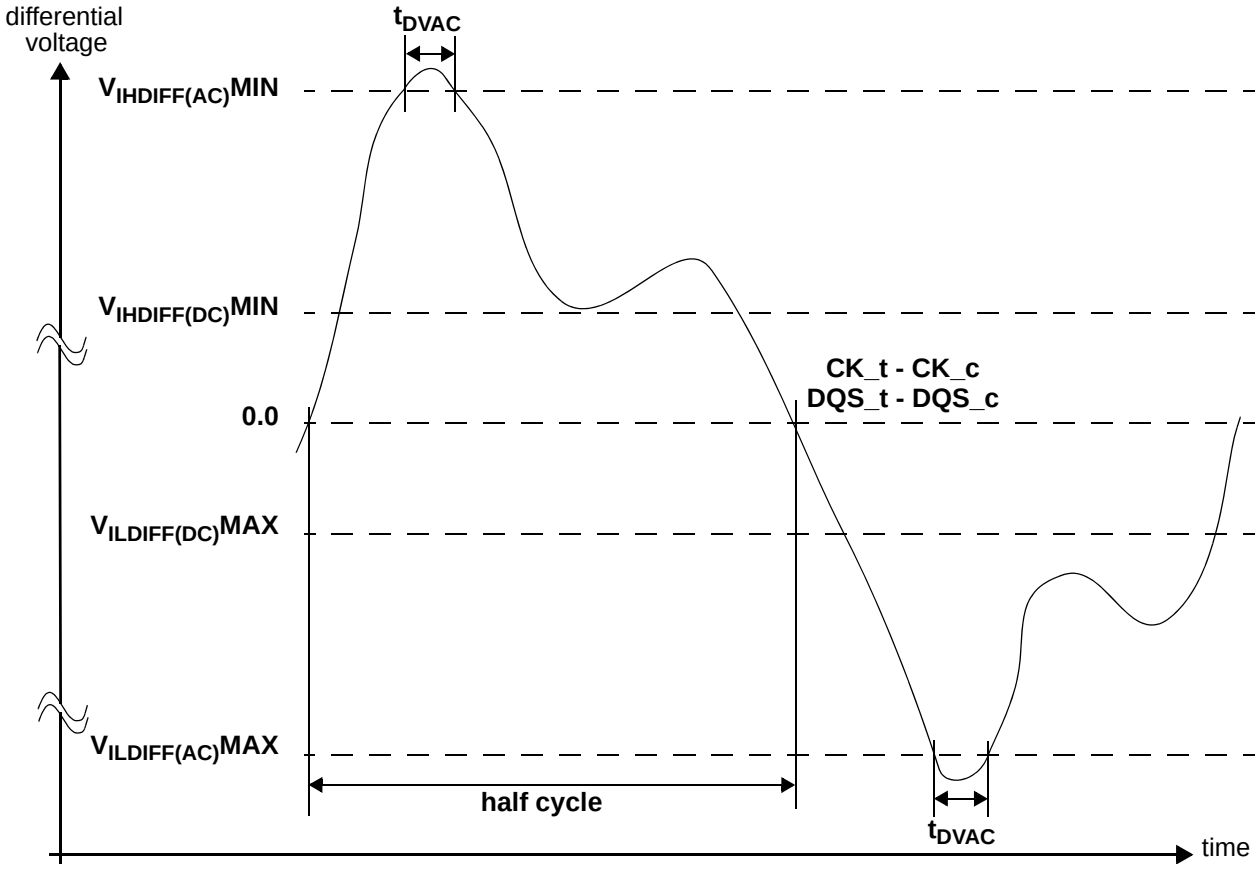


Figure. Definition of differential ac-swing and Time above ac-level tDVAC

Differential AC and DC Input Levels for Clock and Strobe

Parameter	Symbol	LPDDR2 200 to 400		LPDDR2 533 to 1066		Unit	Note
		Min	Max	Min	Max		
Clock (CK_t - CK_c) and Strobe(DQS_t - DQS_c)							
DC Differential Input High	VIHDIFF(DC)	2 x (VIH(DC) - VREF)	Note 3	2 x (VIH(DC) - VREF)	Note 3	V	1
DC Differential Input Low	VILDIFF(DC)	Note 3	2 x (VIL(DC) - VREF)	Note 3	2 x (VIL(DC) - VREF)	V	1
AC Differential Input High	VIHDIFF(AC)	2 x (VIH(AC) - VREF)	Note 3	2 x (VIH(AC) - VREF)	Note 3	V	2
AC Differential Input Low	VILDIFF(AC)	Note 3	2 x (VIL(AC) - VREF)	Note 3	2 x (VIL(AC) - VREF)	V	2

Note:
1. Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(DC) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(DC) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t - CK_c use VIH/VIL(AC) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section "Overshoot and Undershoot Specifications".
4. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF = VREFDQ(DC).

Table. Allowed time before ringback (tDVAC) for CK_t - CK_c and DQS_t - DQS_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 440mV	tDVAC [ps] @ |VIH/Ldiff(ac)| = 600mV
	MIN	MIN
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
<1.0	150	0

Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.
CK_t and CK_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle.
DQS_t, DQS_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle proceeding and following a valid transition.
Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

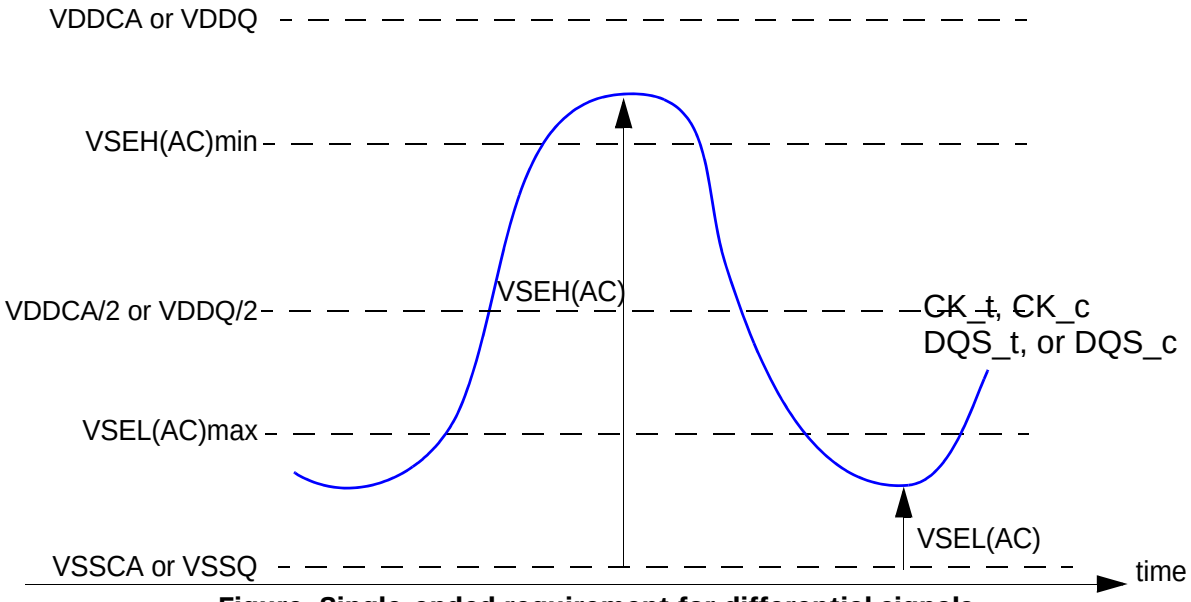


Figure. Single-ended requirement for differential signals

Note that while CA and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_C and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended Levels for Clock and Strobe

Parameter	Symbol	LPDDR2 200 to 400		LPDDR2 533 to 1066		Unit	Note
		Min	Max	Min	Max		
Clock (CK_t - CK_c) and Strobe(DQS_t - DQS_c)							
Single-ended High Level for CK_t and CK_c	VSEH(AC)	(VDDCA/2)+0.3	Note 3	(VDDCA/2)+0.22	Note 3	V	1, 2
Single-ended High Level for DQS_t and DQS_c		(VDDQ/2)+0.3	Note 3	(VDDQ/2)+0.22	Note 3	V	1, 2
Single-ended Low Level for CK_t and CK_c	VSEL(AC)	Note 3	(VDDCA/2)-0.3	Note 3	(VDDCA/2)-0.22	V	1, 2
Single-ended Low Level for DQS_t and DQS_c		Note 3	(VDDQ/2)-0.3	Note 3	(VDDQ/2)-0.22	V	1, 2

Note:
1. For CK_t, CK_c use VSEH/VSEL(AC) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(AC) of DQs.

2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section of Overshoot and Undershoot Specifications.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in "Single-ended Levels for Clock and Strobe". The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

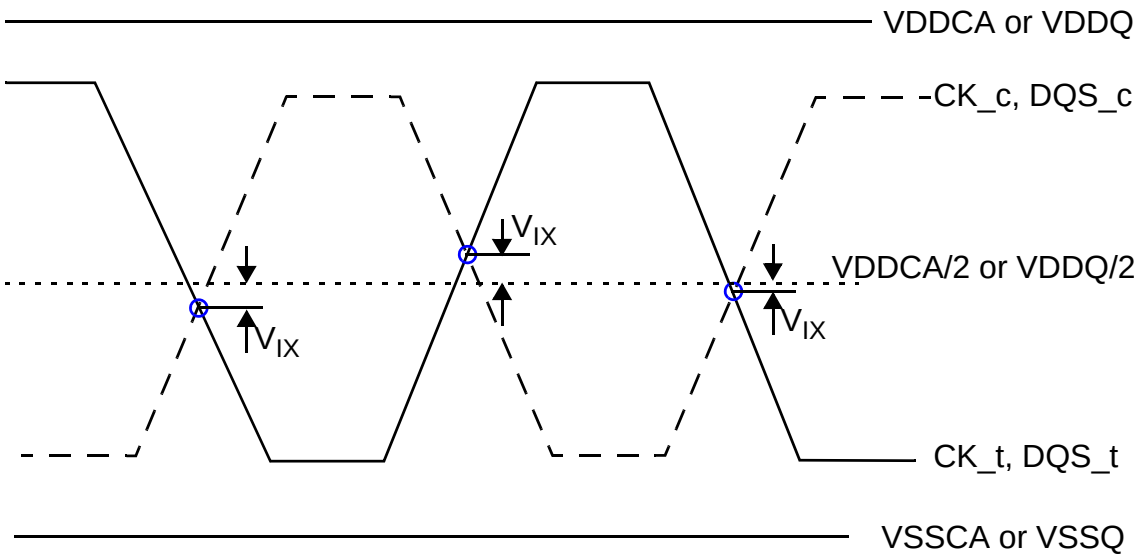


Figure. VIX definition

Cross Point Voltage for Differential Input Signals (Clock and Strobe)

Parameter	Symbol	LPDDR2 200 to 1066		Unit	Note
		Min	Max		
Clock (CK_t - CK_c) and Strobe(DQS_t - DQS_c)					
Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t and CK_c	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t and DQS_c	VIXDQ	-120	120	mV	1, 2

Note:
1. The typical value of VIX(AC) is expected to be about 0.5 x VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF = VREFDQ(DC).

Slew Rate Definitions for Single-ended Input Signals

See "CA and CS_n Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in below Table and Figure.

Differential Input Slew Rate Definition

Parameter	Measured		Defined by
	From	To	
Clock (CK_t - CK_c) and Strobe(DQS_t - DQS_c)			
Differential Input Slew Rate for Rising Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{ILDIFFmax}$	$V_{IHDIFFmin}$	[$V_{IHDIFFmin}$ - $V_{ILDIFFmax}$] / Delta tRDIFF
Differential Input Slew Rate for Falling Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{IHDIFFmin}$	$V_{ILDIFFmax}$	[$V_{IHDIFFmin}$ - $V_{ILDIFFmax}$] / Delta tFDIFF

Note: 1. The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

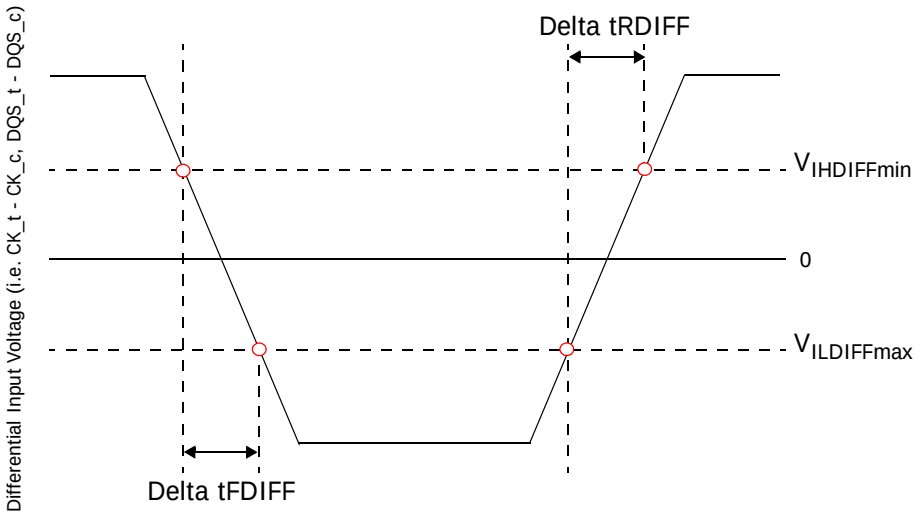


Figure. Differential Input Slew Rate Definition for CK_t, CK_c and DQS_t, DQS_c

AC and DC Logic Output Levels

Single Ended AC and DC Output Levels

Parameter	Symbol		LPDDR2 200 to 1066	Unit	Note
DC Output Logic High Level (for IV curve linearity)	VOH(DC)		0.9 x VDDQ	V	1
DC Output Logic Low Level (for IV curve linearity)	VOL(DC)		0.1 x VDDQ	V	2
AC Output Logic High Level (for output slew rate)	VOH(AC)		VREF+0.12	V	
AC Output Logic Low Level (for output slew rate)	VOL(AC)		VREF-0.12	V	
Output Leakage current For DQ, DM, DQS_t and DQS_c (DQ, DQS_t and DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ)	I_{OZ}	Min.	-5	uA	
		Max.	5	uA	

Note: 1. IOH = -0.1mA, 2. IOL = 0.1mA

Differential AC and DC Output Levels (DQS_t, DQS_c)

Parameter	Symbol	LPDDR2 200 to 1066	Unit	Note
AC Differential Output High Level (for Output SR)	VOHDIFF(AC)	+ 0.20 x VDDQ	V	
AC Differential Output Low Level (for Output SR)	VOLDIFF(AC)	- 0.20 x VDDQ	V	

Note: 1. IOH = -0.1mA, 2. IOL = 0.1mA

Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Single Ended Output Slew Rate for Rising Edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / Delta tRSE
Single Ended Output Slew Rate for Falling Edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / Delta tFSE

Note: Output slew rate is verified by design and characterization and may not be subject to production test.

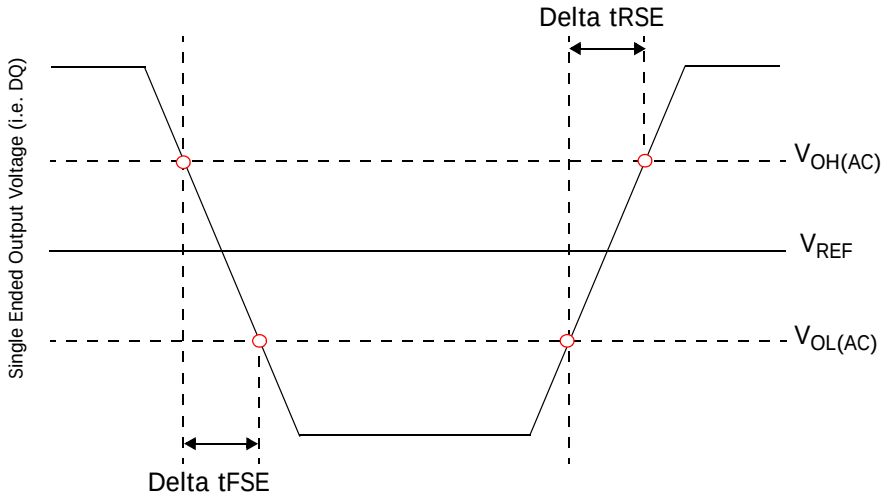


Figure. Single Ended Output Slew Rate Definition

Output Slew Rate (Single Ended)

Parameter	Symbol	LPDDR2 200 to 1066		Unit	Note
		Min	Max		
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	3.5	V/ns	
Single-ended Output Slew Rate (RON = 60Ω +/- 30%)	SRQse	1.0	2.5	V/ns	
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4		

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

Note:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLDIFF(AC) and VOHDIFF(AC) for differential signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Differential Output Slew Rate for Rising Edge	$V_{OLDIFF(AC)}$	$V_{OHDIFF(AC)}$	$[V_{OHDIFF(AC)} - V_{OLDIFF(AC)}]$ / Delta tRDIFF
Differential Output Slew Rate for Falling Edge	$V_{OHDIFF(AC)}$	$V_{OLDIFF(AC)}$	$[V_{OHDIFF(AC)} - V_{OLDIFF(AC)}]$ / Delta tFDIFF

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

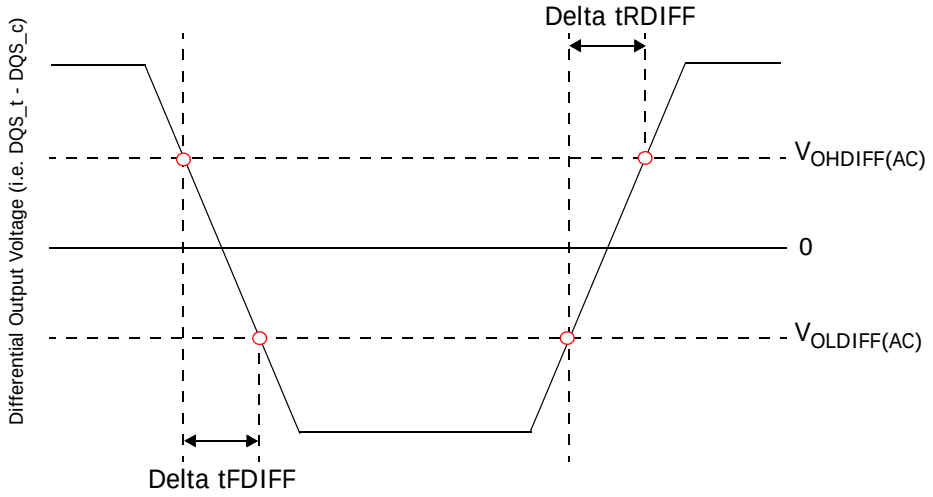


Figure. Differential Output Slew Rate Definition

Output Slew Rate (Differential)

Parameter	Symbol	LPDDR2 200 to 1066		Unit	Note
		Min	Max		
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns	
Differential Output Slew Rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns	

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

Note:

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Overshoot and Undershoot Specifications

Parameter	800	667	533	400	333	266	200	Units
CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM								
Maximum peak amplitude allowed for overshoot	0.35							V
Maximum peak amplitude allowed for undershoot	0.35							V
Maximum overshoot area above VDDCA or VDDQ	0.20	0.24	0.30	0.40	0.48	0.60	0.80	V-ns
Maximum undershoot area below VSSCA or VSSQ	0.20	0.24	0.30	0.40	0.48	0.60	0.80	V-ns

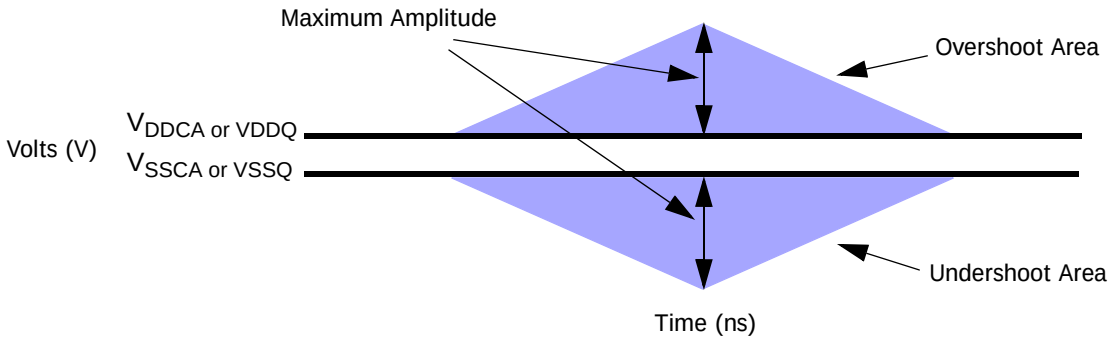
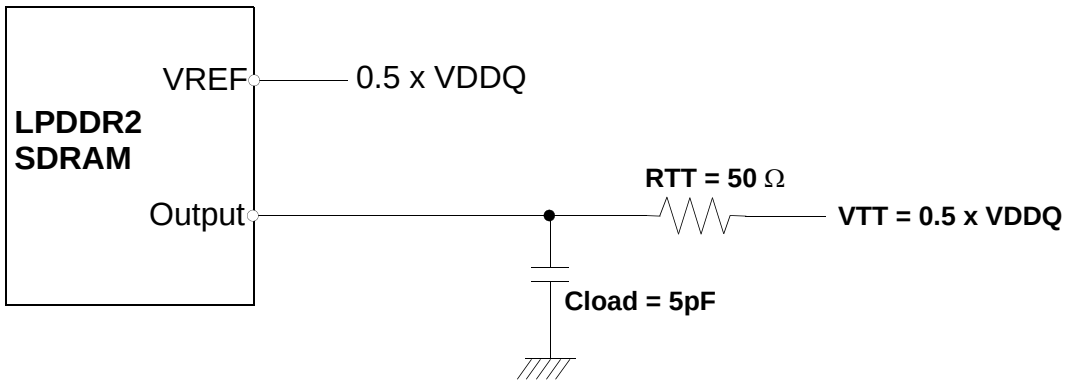


Figure. Overshoot and Undershoot Definition

Output Buffer Characteristics

HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Note: 1. All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

RON_{PU} and RON_{PD} Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PU} is turned off

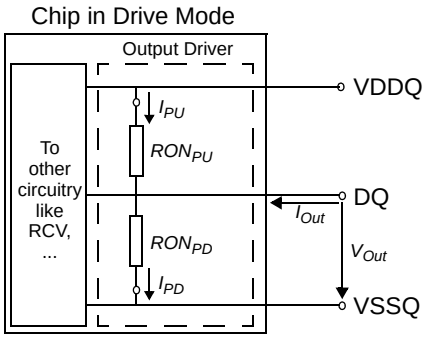


Figure. Output Driver: Definition of Voltages and Currents

RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table - Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Typ	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0Ω	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

Note:
1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down,
   MMPUPD: Measure RON_{PU} and RON_{PD}, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	$.5-(dRONdT\times\lvert\Delta T\rvert)-(dRONdV\times\lvert\Delta V\rvert$	$.15+(dRONdT\times\lvert\Delta T\rvert)+(dRONdV\times\lvert\Delta V$	%	1,2
RONPU					

Note

1. ($\Delta T = T - T$@ calibration), $\Delta V = V - V$(@ calibration)
2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table. Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON40PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON40PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1
120.0Ω	RON120PD	0.5 x VDDQ	84	120	156	Ω	1
	RON120PU	0.5 x VDDQ	84	120	156	Ω	1

Note:

1. Across entire operating temperature range, without calibration.

RZQ I-V Curve

Table. RZQ I-V Curve

Voltage(V)	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ω]				Current [mA] / RON [Ω]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.31	3.16	-2.02	-3.83	-2.31	-3.16
0.70	2.11	4.08	2.44	3.38	-2.11	-4.08	-2.44	-3.38
0.75	2.19	4.31	2.54	3.59	-2.19	-4.31	-2.54	-3.59
0.80	2.25	4.54	2.65	3.79	-2.25	-4.54	-2.65	-3.79
0.85	2.30	4.74	2.74	3.98	-2.30	-4.74	-2.74	-3.98
0.90	2.34	4.92	2.81	4.15	-2.34	-4.92	-2.81	-4.15
0.95	2.37	5.08	2.87	4.34	-2.37	-5.08	-2.87	-4.34
1.00	2.41	5.20	2.93	4.49	-2.41	-5.20	-2.93	-4.49
1.05	2.43	5.31	2.96	4.63	-2.43	-5.31	-2.96	-4.63
1.10	2.46	5.41	3.00	4.76	-2.46	-5.41	-3.00	-4.76
1.15	2.48	5.48	3.03	4.87	-2.48	-5.48	-3.03	-4.87
1.20	2.50	5.55	3.06	4.98	-2.50	-5.55	-3.06	-4.98

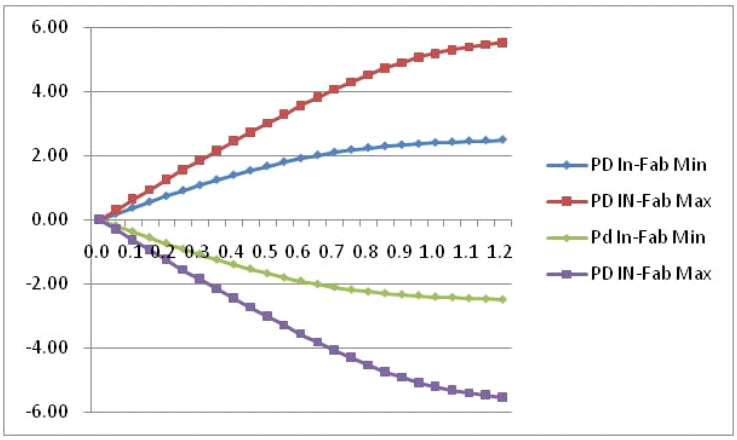


Figure. RON = 240 Ohms I-V Curve after ZQReset

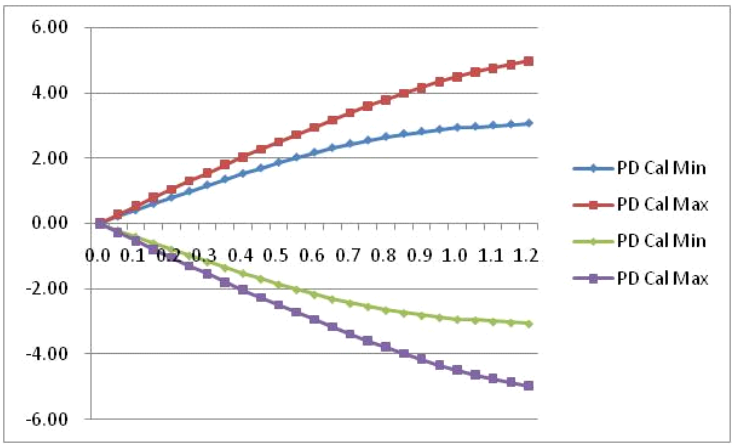


Figure. RON = 240 Ohms I-V Curve after calibration

Input/Output Capacitance

Die Only[1]

Parameter	Symbol	Min	Max	Unit
Input capacitance, CK_t and CK_c	CCK	1.0	2.0	pF
Input capacitance delta, CK_t and CK_c	CDCK	0	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	pF
Input capacitance delta, all other input-only pins	CDI	-0.50	0.50	pF
		-0.40	0.40	pF
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	1.25	2.5	pF
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	0	0.30	pF
Input/output capacitance delta, DQ and DM	CDIO	-0.6	0.6	pF
Input/Output Capacitance ZQ	CZQ	0	2.5	pF

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:
1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA9.
5. CDI = CI - 0.5 * (CCK_t + CCK_c)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8. Absolute value of CDQS_t and CDQS_c.
9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.
10. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5pF.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX; HIGH: VIN $\geq V_{IH}$(DC) MIN; STABLE: Inputs are stable at a HIGH or LOW level; SWITCHING: See tables below.

Table. Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:

1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

Table. Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0 - CA2	CA3 - CA9	All DQs
Rising	HIGH	LOW	N	Read	HLH	LHLHLHL	L
Falling	HIGH	LOW			LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH			HLH	HLHLLHL	L
Rising	HIGH	LOW	N+2	Read	HLH	HLHLLHL	H
Falling	HIGH	LOW			LLL	HHHHHHH	H
Rising	HIGH	HIGH	N+3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH			HLH	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1, ...) is used continuously during IDD measurement for IDD4R.

Table. Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0 - CA2	CA3 - CA9	All DQs
Rising	HIGH	LOW	N	Write	HLL	LHLHLHL	L
Falling	HIGH	LOW			LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH			HLH	HLHLLHL	L
Rising	HIGH	LOW	N+2	Write	HLL	HLHLLHL	H
Falling	HIGH	LOW			LLL	HHHHHHH	H
Rising	HIGH	HIGH	N+3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH			HLH	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

DC Parameters and Operating Conditions (for x32 devices - sheet 1 of 2)

- All values are based on a single die. Total current consumption is dependent to user operating condition

Parameter	Test Condition	Symbol	Power Supply	Max				Unit	Note
				DDR 800	DDR 667	DDR 533	DDR 400		
Operating one bank active-precharge current	tCK = tCK(min); tRC = tRC(min); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	VDD1	TBD				mA	3
		$IDD0_2$	VDD2	TBD				mA	3
		$IDD0_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Idle power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	VDD1	TBD				mA	3
		$IDD2P_2$	VDD2	TBD				mA	3
		$IDD2P_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Idle power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2PS_1$	VDD1	TBD				mA	3
		$IDD2PS_2$	VDD2	TBD				mA	3
		$IDD2PS_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Idle non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH, all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	VDD1	TBD				mA	3
		$IDD2N_2$	VDD2	TBD				mA	3
		$IDD2N_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Idle non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2NS_1$	VDD1	TBD				mA	3
		$IDD2NS_2$	VDD2	TBD				mA	3
		$IDD2NS_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Active power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	VDD1	TBD				mA	3
		$IDD3P_2$	VDD2	TBD				mA	3
		$IDD3P_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Active power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_1$	VDD1	TBD				mA	3
		$IDD3PS_2$	VDD2	TBD				mA	3
		$IDD3PS_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Active non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	TBD				mA	3
		$IDD3N_2$	VDD2	TBD				mA	3
		$IDD3N_{IN}$	VDDCA VDDQ	TBD				mA	3, 4

DC Parameters and Operating Conditions (for x32 devices - sheet 2 of 2)

- All values are based on a single die. Total current consumption is dependent to user operating condition

Parameter	Test Condition	Symbol	Power Supply	Max				Unit	Note
				DDR 800	DDR 667	DDR 533	DDR 400		
Active non power-down standby current with clock stop	CK_t=LOW; CK_c=HIGH; CKE is HIGH CS_n is HIGH One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3NS_1$	VDD1	TBD				mA	3
		$IDD3NS_2$	VDD2	TBD				mA	3
		$IDD3NS_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Operating burst read current	tCK = tCK(min); CS_n is HIGH between valid commands; one bank active; BL=4; RL=RLmin; CA bus inputs are SWITCHING, 50% data change each burst transfer	$IDD4R_1$	VDD1	TBD				mA	3
		$IDD4R_2$	VDD2	TBD	TBD	TBD	TBD	mA	3
		$IDD4R_{IN}$	VDDCA	TBD				mA	3
		$IDD4R_Q$	VDDQ	TBD	TBD	TBD	TBD	mA	3, 6
Operating burst write current	tCK = tCK(min); CS_n is HIGH between valid commands; one bank active; BL=4; WL=WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	TBD				mA	3
		$IDD4W_2$	VDD2	TBD	TBD	TBD	TBD	mA	3
		$IDD4W_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
All Bank Auto Refresh Burst Current	tCK=tCK(min); CS_n is HIGH between valid commands; tRC=tRFCab(min); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5_1$	VDD1	TBD				mA	3
		$IDD5_2$	VDD2	TBD				mA	3
		$IDD5_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
All Bank Auto Refresh Average Current	tCK=tCK(min); CKE is HIGH between valid commands; tRC=tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5ab_1$	VDD1	TBD				mA	4
		$IDD5ab_2$	VDD2	TBD	TBD	TBD	TBD	mA	4
		$IDD5ab_{IN}$	VDDCA VDDQ	TBD				mA	3, 4
Per Bank Auto Refresh Average Current	tCK=tCK(min); CKE is HIGH between valid commands; tRC=tREFI/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5pb_1$	VDD1	TBD				mA	1, 3
		$IDD5pb_2$	VDD2	TBD	TBD	TBD	TBD	mA	1, 3
		$IDD5pb_{IN}$	VDDCA VDDQ	TBD				mA	1,3,4
Self Refresh Current (Standard Temperature Range -30'C ~ 85'C)	CK_t=LOW; CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1 x Self-refresh rate	$IDD6_1$	VDD1	TBD				mA	2, 3
		$IDD6_2$	VDD2	TBD				mA	2, 3
		$IDD6_{IN}$	VDDCA VDDQ	TBD				mA	2,3,4
Self Refresh Current (Extended Temperature Range: 85'C ~ 105'C)	CK_t=LOW; CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD6ET_1$	VDD1	TBD				mA	2, 3
		$IDD6ET_2$	VDD2	TBD				mA	2, 3
		$IDD6ET_{IN}$	VDDCA VDDQ	TBD				mA	2,3,4
Deep Power Down Current	CK_t=LOW; CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD8_1$	VDD1	TBD				uA	3
		$IDD8_2$	VDD2	TBD				uA	3
		$IDD8_{IN}$	VDDCA VDDQ	TBD				uA	3, 4

Note:
1. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities.
2. This is the general definition that applies to full array Self Refresh. Refer to IDD6 Partial Array Self-Refresh Current on next table.
3. IDD values published are the maximum of the distribution of the arithmetic mean.
4. Measured currents are the summation of VDDQ and VDDCA.
5. To calculate total current consumption, the currents of all active operations must be considered.
6. Guaranteed by design with output load of 5pF and RON = 40Ohm.
7. IDD current specifications are tested after the device is properly initialized.
8. 1 x Self-refresh rate is the rate at which the LPDDR2-S4 device is refreshed internally during Self-refresh before going into the Extended temperature range.

IDD6 Partial Array Self Refresh Current

Temp. (^oC)	Memory Array				Unit
	8 Banks	4 Banks	2 Banks	1 Bank	
45	TBD	TBD	TBD	TBD	mA
85	TBD	TBD	TBD	TBD	mA
105	TBD	TBD	TBD	TBD	mA

Note:
1. Related numerical values in this 45^{o}C and 105^{o}C are examples for reference sample value only.
2. With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.
3. LPDDR2-S4 SDRAM uses the same IDD6 current value categorization as LPDDR2-S2 SDRAM. Some LPDDR2-S4 SDRAM densities support both bank masking and segment masking. The IDD6 currents are measured using bank-masking only.
4. IDD values published are the maximum of the distribution of the arithmethic mean.

AC TIMING PARAMETERS (Sheet 1 of 4)

Parameter	Symbol	min tCK	DDR2 800		DDR2 667		DDR2 533		DDR2 400		Unit	Note
			min	max	min	max	min	max	min	max		
Clock Timing												
Average Clock Period	tCK(avg)		2.5	100	3	100	3.75	100	5	100	ns	
Average high pulse width	tCH(avg)		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	
Average low pulse width	tCL(avg)		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	
Absolute Clock Period	tCK(abs)		min{tCK(avg),min + tJIT(per),min}								ps	
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed		0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed		0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed		-100	100	-110	110	-120	120	-140	140	ps	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed		-	200	-	220	-	240	-	280	ps	
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed		min{ min((tCH(abs),min - tCH(avg),min), (tCH(abs),min - tCH(avg),min)) * tCK(avg) } min{ -0.02 * tCK(avg) }								ps	
			max{ max((tCH(abs),max - tCH(avg),max), (tCH(abs),max - tCH(avg),max)) * tCK(avg) } max{ 0.02 * tCK(avg) }									
Cumulative error across 2 cycles	tERR(2per), allowed		-147	147	-162	162	-177	177	-206	206	ps	
Cumulative error across 3 cycles	tERR(3per), allowed		-175	175	-192	192	-210	210	-245	245	ps	
Cumulative error across 4 cycles	tERR(4per), allowed		-194	194	-214	214	-233	233	-272	272	ps	
Cumulative error across 5 cycles	tERR(5per), allowed		-209	209	-230	230	-251	251	-293	293	ps	
Cumulative error across 6 cycles	tERR(6per), allowed		-222	222	-244	244	-266	266	-311	311	ps	
Cumulative error across 7 cycles	tERR(7per), allowed		-232	232	-256	256	-279	279	-325	325	ps	
Cumulative error across 8 cycles	tERR(8per), allowed		-241	241	-256	256	-290	290	-338	338	ps	
Cumulative error across 9 cycles	tERR(9per), allowed		-249	249	-274	274	-299	299	-349	349	ps	
Cumulative error across 10 cycles	tERR(10per), allowed		-257	257	-282	282	-308	308	-359	359	ps	
Cumulative error across 11 cycles	tERR(11per), allowed		-263	263	-289	289	-316	316	-368	368	ps	
Cumulative error across 12 cycles	tERR(12per), allowed		-269	269	-296	296	-323	323	-377	377	ps	
Cumulative error across n cycles (n = 13, 14 . . . 49, 50)	tERR(nper), allowed		min{ tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min }								ps	
			max{ tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max }									

AC TIMING PARAMETERS (Sheet 2 of 4)

Parameter	Symbol	min	DDR2 800		DDR2 667		DDR2 533		DDR2 400		Unit	Note
		tCK	min	max	min	max	min	max	min	max		
ZQ Calibration Parameters												
Initialization Calibration Time	tZQINIT		1		1		1		1		us	
Long Calibration Time	tZQCL	6	360		360		360		360		ns	
Short Calibration Time	tZQCS	6	90		90		90		90		ns	
Calibration Reset Time	tZQRESET	3	50		50		50		50		ns	
Read Parameters												
DQS output access time from CK/CK#	tDQSCK		2.5	5.5	2.5	5.5	2.5	5.5	2.5	5.5	ns	
DQSCK Delta short	tDQSCKDS			450		540		670		900	ps	14
DQSCK Delta Medium	tDQSCKDM			900		1050		1350		1800	ps	15
DQSCK Delta Long	tDQSCKDL			1200		1400		1800		2400	ps	16
DQS-DQ skew	tDQSQ			240		280		340		400	ps	
Data hold skew factor	tQHS			280		340		400		480	ps	
DQ/DQS output hold time from DQS	tQH		min{ tQHP-tQHS }								ps	
Data Half Period	tQHP		min(tQSH, tQSL)								tCK(avg)	
DQS Output High Pulse Width	tQSH		min{ tCH(abs) - 0.05 }								tCK(avg)	
DQS Output Low Pulse Width	tQSL		min{ tCL(abs) - 0.05 }								tCK(avg)	
Read preamble	tRPRE		0.9		0.9		0.9		0.9		tCK(avg)	11,12
Read postamble	tRPST		min{ tCL(abs)-0.05 }								tCK(avg)	11,13
DQS low-Z from clock	tLZ(DQS)		min{tDQSCK(min) - 300}								ps	11
DQ low-Z from clock	tLZ(DQ)		min{tDQSCK(min) - (1.4 x tQHSmax)}								ps	11
DQS high-Z from clock	tHZ(DQS)		max{tDQSCK(max) - 100}								ps	11
DQ high-Z from clock	tHZ(DQ)		max{tDQSCK(max) + (1.4 x tDQSQmax)}								ps	11
Write Parameters												
DQ and DM input setup time (VREF based)	tDS		270		350		430		480		ps	
DQ and DM input hold time(VREF based)	tDH		270		350		430		480		ps	
DQ and DM input pulse width	tDIPW		0.35		0.35		0.35		0.35		tCK(avg)	
Write command to 1st DQS latching transition	tDQSS		0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK(avg)	
DQS input high-level width	tDQSH		0.4		0.4		0.4		0.4		tCK(avg)	
DQS input low-level width	tDQSL		0.4		0.4		0.4		0.4		tCK(avg)	
DQS falling edge to CK setup time	tDSS		0.2		0.2		0.2		0.2		tCK(avg)	
DQS falling edge hold time from CK	tDSH		0.2		0.2		0.2		0.2		tCK(avg)	
Write postamble	tWPST		0.4		0.4		0.4		0.4		tCK(avg)	
Write preamble	tWPRE		0.35		0.35		0.35		0.35		tCK(avg)	
CKE Input Parameters												
CKE min. pulse width (high/low pulse width)	tCKE	3	3		3		3		3		tCK(avg)	
CKE input setup time	tISCKE		0.25		0.25		0.25		0.25		tCK(avg)	2
CKE input hold time	tIHCKE		0.25		0.25		0.25		0.25		tCK(avg)	3
Command Address Input Parameters												
Address and control input setup time (Vref based)	tIS		290		370		460		600		ps	1,10
Address and control input hold time (Vref based)	tIH		290		370		460		600		ps	1,10
Address and control input pulse width	tIPW		0.40		0.40		0.40		0.40		tCK(avg)	

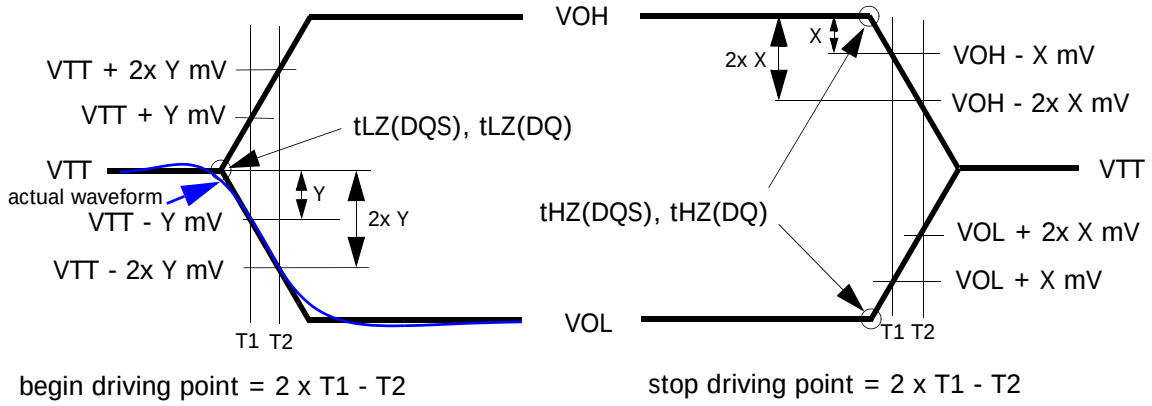
AC TIMING PARAMETERS (Sheet 3 of 4)

Parameter	Symbol	min tCK	DDR2 800		DDR2 667		DDR2 533		DDR2 400		Unit	Note
			min	max	min	max	min	max	min	max		
Boot Parameters (10MHz-55MHz)												
Clock Cycle Time	tCKb		18	100	18	100	18	100	18	100	ns	4,6,7
CKE Input Setup Time	tISCKEb		2.5		2.5		2.5		2.5		ns	4,6,7
CKE Input Hold Time	tIHCKEb		2.5		2.5		2.5		2.5		ns	4,6,7
Address & Control Input Setup Time	tISb		1150		1150		1150		1150		ps	4,6,7
Address & Control Input Hold Time	tIHb		1150		1150		1150		1150		ps	4,6,7
DQS Output Data Access Time from CK/CK#	tDQSCKb		2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns	4,6,7
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb			1.2		1.2		1.2		1.2	ns	4,6,7
Data Hold Skew Factor	tQHSb			1.2		1.2		1.2		1.2	ns	4,6,7
Mode Register Parameters												
MODE REGISTER Write command period	tMRW	5	5		5		5		5		tCK(avg)	
MODE REGISTER Read command period	tMRR	2	2		2		2		2		tCK(avg)	
Core Parameters												
Read Latency	RL	3	6		5		4		3		tCK(avg)	
Write Latency	WL	1	3		2		2		1		tCK(avg)	
ACTIVE to ACTIVE command period	tRC		min{tRAS+tRPab(all-bank)} min{tRAS+tRPpb(per-bank)}								ns	
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	3	15		15		15		15		ns	
Self refresh exit to next valid command delay	tXSR	2	tRFCab +10		tRFCab +10		tRFCab +10		tRFCab +10		ns	
Exit power down to next valid command delay	tXP	2	7.5		7.5		7.5		7.5		ns	
LPDDR2-S4 CAS to CAS delay	tCCD	2	2		2		2		2		tCK(avg)	
Internal Read to Precharge command delay	tRTP	2	7.5		7.5		7.5		7.5		ns	
RAS to CAS Delay	tRCD	3	18		18		18		18		ns	
Row Precharge Time (single bank)	tRPpb	3	18		18		18		18		ns	
Row Precharge Time (all banks) - 4-bank	tRPab	3	18		18		18		18		ns	
Row Precharge Time (all banks) - 8-bank	tRPab	3	21		21		21		21		ns	
Row Active Time	tRAS		42	70,000	42	70,000	42	70,000	42	70,000	ns	
Write Recovery Time	tWR	3	15		15		15		15		ns	
Internal Write to Read Command Delay	tWTR	2	7.5		7.5		7.5		10		ns	
Active bank A to Active bank B	tRRD	2	10		10		10		10		ns	
Four Bank Activate Window	tFAW	8	50		50		50		50		ns	
Minimum Deep Power Down Time	tDPD		500		500		500		500		us	

AC TIMING PARAMETERS (Sheet 4 of 4)

Parameter	Symbol	min tCK	DDR2 800		DDR2 667		DDR2 533		DDR2 400		Unit	Note
			min	max	min	max	min	max	min	max		
Temperature De-Rating												17
tDQSCK De-Rating	tDQSCK (Derated)			6000		6000		6000		6000	ps	
Core Timings Temperature De-Rating	tRCD (Derated)		min{tRCD + 1.875}								ns	
	tRC (Derated)		min{tRC + 1.875}								ns	
	tRAS (Derated)		min{tRAS + 1.875}								ns	
	tRP (Derated)		min{tRP + 1.875}								ns	
	tRRD (Derated)		min{tRRD + 1.875}								ns	

Note:
1. Input set-up/hold time for signal(CA0 ~ 9, CS_n)
2. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.
3. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level.
4. To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
5. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
6. The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition".
7. The output skew parameters are measured with Ron default settings into the reference load.
8. The min tCK column applies only when tCK is greater than 6ns for LPDDR2-S4 devices. In this case, both min tCK values and analog timings (ns) shall be satisfied.
9. All AC timings assume an input slew rate of 1V/ns.
10. Read, Write, and Input Setup and Hold values are referenced to VREF.
11. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure below shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.

Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

12. Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.
13. Measured from the from start driving the last falling strobe edge to the stop driving DQS_t - DQS_c.
14. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10C/s. Values do not include clock jitter.
15. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10C/s. Values do not include clock jitter.
16. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10C/s. Values do not include clock jitter.
17. It is applied when Self Refresh Rate OP<2:0> = 110B in MR4. LPDDR2-S4 devices shall be de-rated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in "AC timing table". Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \quad N = 200$$

Unit `tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit `nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \quad N = 200$$

Definition for tJIT(per)

Symbol	Definition
tJIT(per)	The single period jitter defined as the largest deviation of any signal tCK from tCK(avg). tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act	The actual clock jitter for a given system.
tJIT(per),allowed	The specified allowed clock period jitter.

Note:
1. tJIT(per) is not subject to production test.

Definition for tJIT(cc)

Symbol	Definition
tJIT(cc)	Defined as the absolute difference in clock period between two consecutive clock cycles. tJIT(cc) = Max of |{tCKi +1 - tCKi}|. Defines the cycle to cycle jitter.

Note:
1. tJIT(cc) is not subject to production test.

Definition for tERR(nper)

Symbol	Definition
tERR(nper)	Defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act	The actual clock jitter over n cycles for a given system.
tERR(nper),allowed	The specified allowed clock period jitter over n cycles.

Note:
1. tERR(nper) is not subject to production test.

tERR(nper) can be calculated by the formula shown below:

$$tERR(nper) = \left(\sum_{j=j}^{j+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68\,LN(n)) \times tJIT(per), min$$

tERR(nper),max can be caculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68\,LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value

Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

tJIT(duty),min can be caculated by the formula shown below:

$$tJIT(duty),min = MIN((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) \times tCK(avg)$$

tJIT(duty),max can be caculated by the formula shown below:

$$tJIT(duty),max = MAX((tCH(abs),max - tCH(avg),max),(tCL(abs),max - tCL(avg),max)) \times tCK(avg)$$

Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Note:
1. tCK(avg),min is expressed in ps for this table
2. tJIT(duty),min is a negative value

Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in “AC timing table” and how to determine cycle time de-rating and clock cycle de-rating.

Clock period jitter effects on core timing parameters
(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$Cycle\ Time\ Derating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters
(tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters

tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,
if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max = + 193 ps, then,
tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg)
= 0.9 - (193 - 100)/2500= .8628 tCK(avg)

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0-31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.
tQSH(abs)min = tCH(abs)min - 0.05
tQSL(abs)min = tCL(abs)min - 0.05
These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @ LPDDR2 device pin =
min { (tQSH(abs)min * tCK(avg)min - tDQSQmax - tQHSmax), (tQSL(abs)min * tCK(avg)min - tDQSQmax - tQHSmax)}

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.
tRPST(abs)min = tCL(abs)min - 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameters

tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 -31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

tDQSS(min,derated) can be caculated by the formula shown below:

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

tDQSS(max,derated) can be caculated by the formula shown below:

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,
if the measured jitter into a LPDDR2-800 device has
tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then
tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)
and
tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded `VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded `VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded `DC to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded `DC to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in Table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table. CA and CS_n Setup and Hold Base-Values for 1V/ns

Unit [ps]	LPDDR2				Reference
	800	667	533	466	
tIS(base)	70	150	240	300	VIH/L(AC)=VREF(DC)+/-220mV
tIH(base)	160	240	330	390	VIH/L(DC)=VREF(DC)+/-130mV

Unit [ps]	LPDDR2				Reference
	400	333	266	200	
tIS(base)	300	440	600	850	VIH/L(AC)=VREF(DC)+/-300mV
tIH(base)	400	540	700	950	VIH/L(DC)=VREF(DC)+/-200mV

Note 1: AC/DC referenced for 1V/ns CA and CS_n slew rate and 2V/ns differential CK_t-CK_c slew rate.

Table. Derating values LPDDR2 tIS/tIH - AC/DC based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based AC220 Threshold -> VIH(AC)=VREF(DC)+220mV, VIL(AC)=VREF(DC)-220mV DC130 Threshold -> VIH(DC)=VREF(DC)+130mV, VIL(DC)=VREF(DC)-130mV																	
		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note 1: Cell contents shaded in red are defined as ‘not supported’

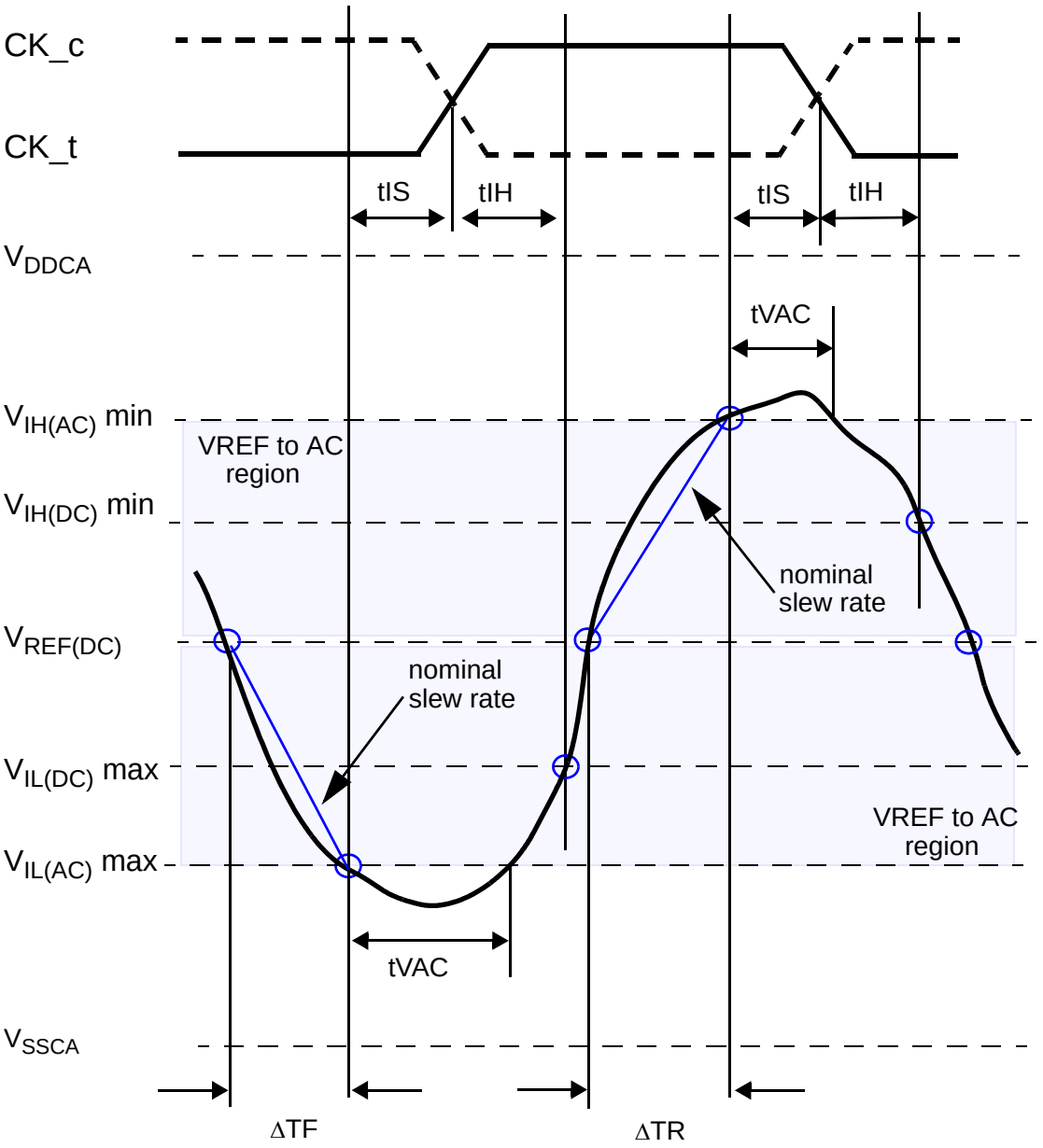
Table. Derating values LPDDR2 tIS/tIH - AC/DC based AC300

ΔtIS, ΔtIH derating in [ps] AC/DC based AC300 Threshold -> VIH(AC)=VREF(DC)+300mV, VIL(AC)=VREF(DC)-300mV DC200 Threshold -> VIH(DC)=VREF(DC)+200mV, VIL(DC)=VREF(DC)-200mV																	
		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

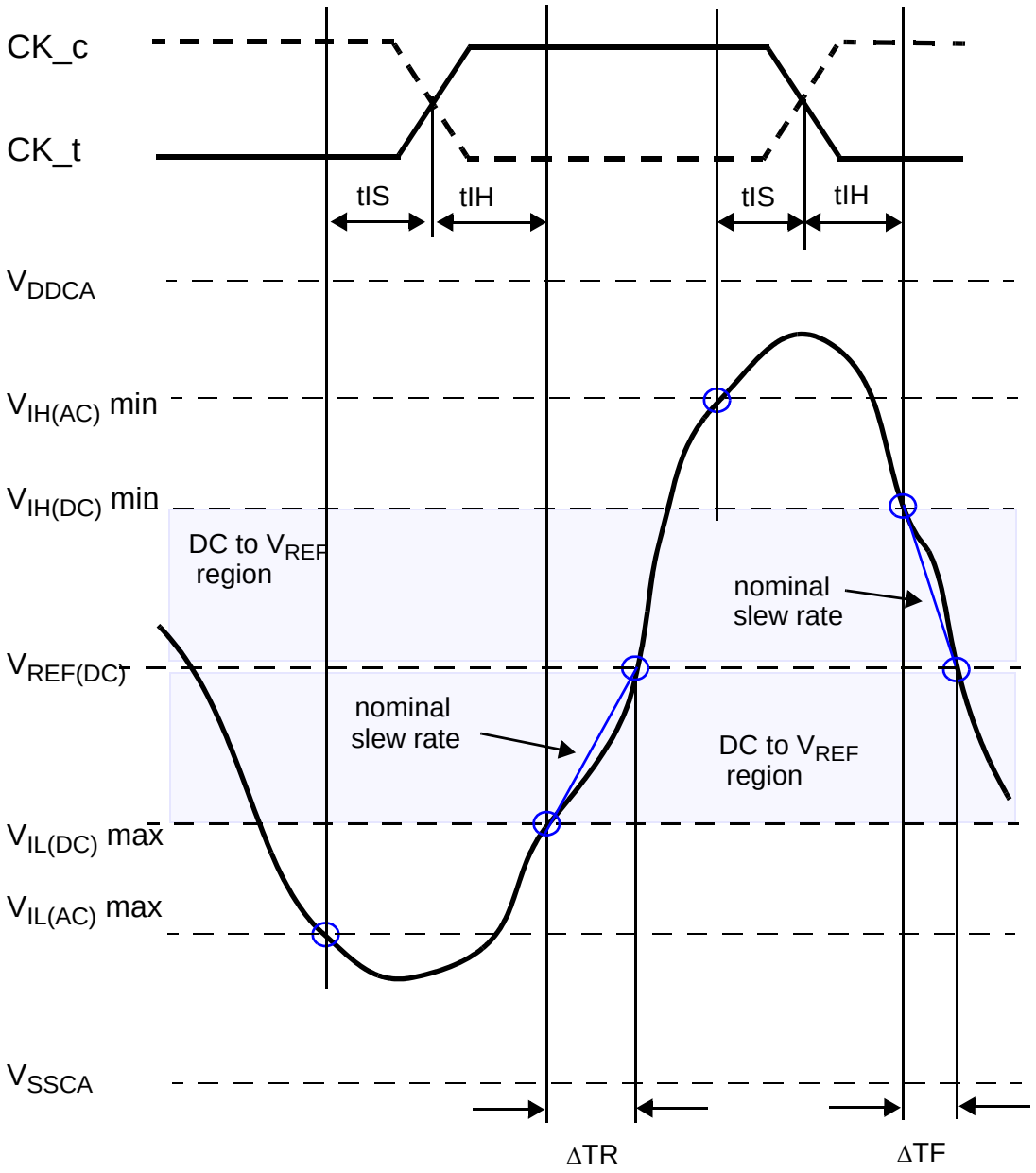
Slew Rate [V/ns]	t_{VAC}@ 300mV [ps]		t_{VAC}@220mV [ps]	
	MIN	MAX	MIN	MAX
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{REF(DC)}}{\Delta TR}$$

Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time tIH for CA and CS_n with respect to clock

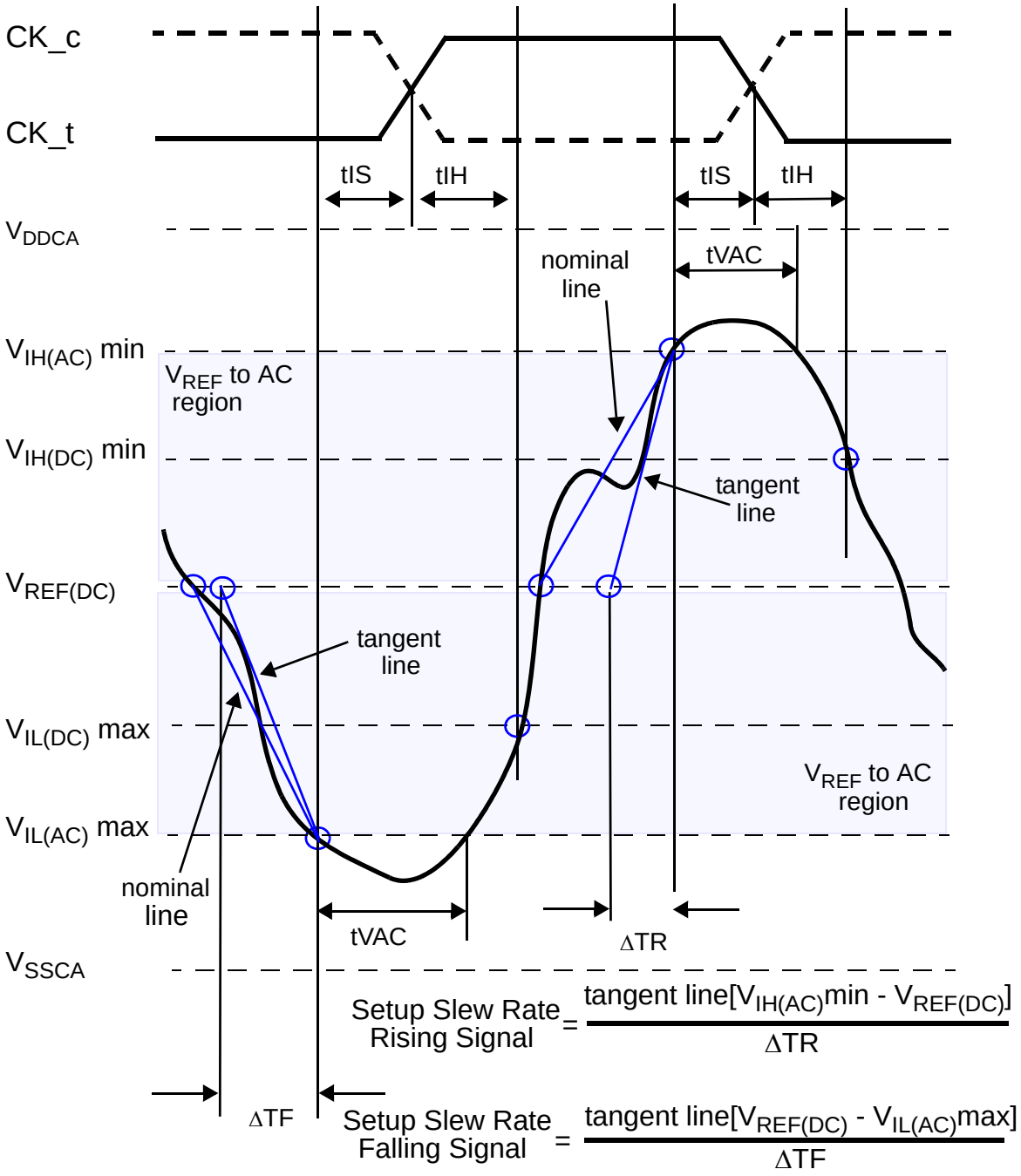
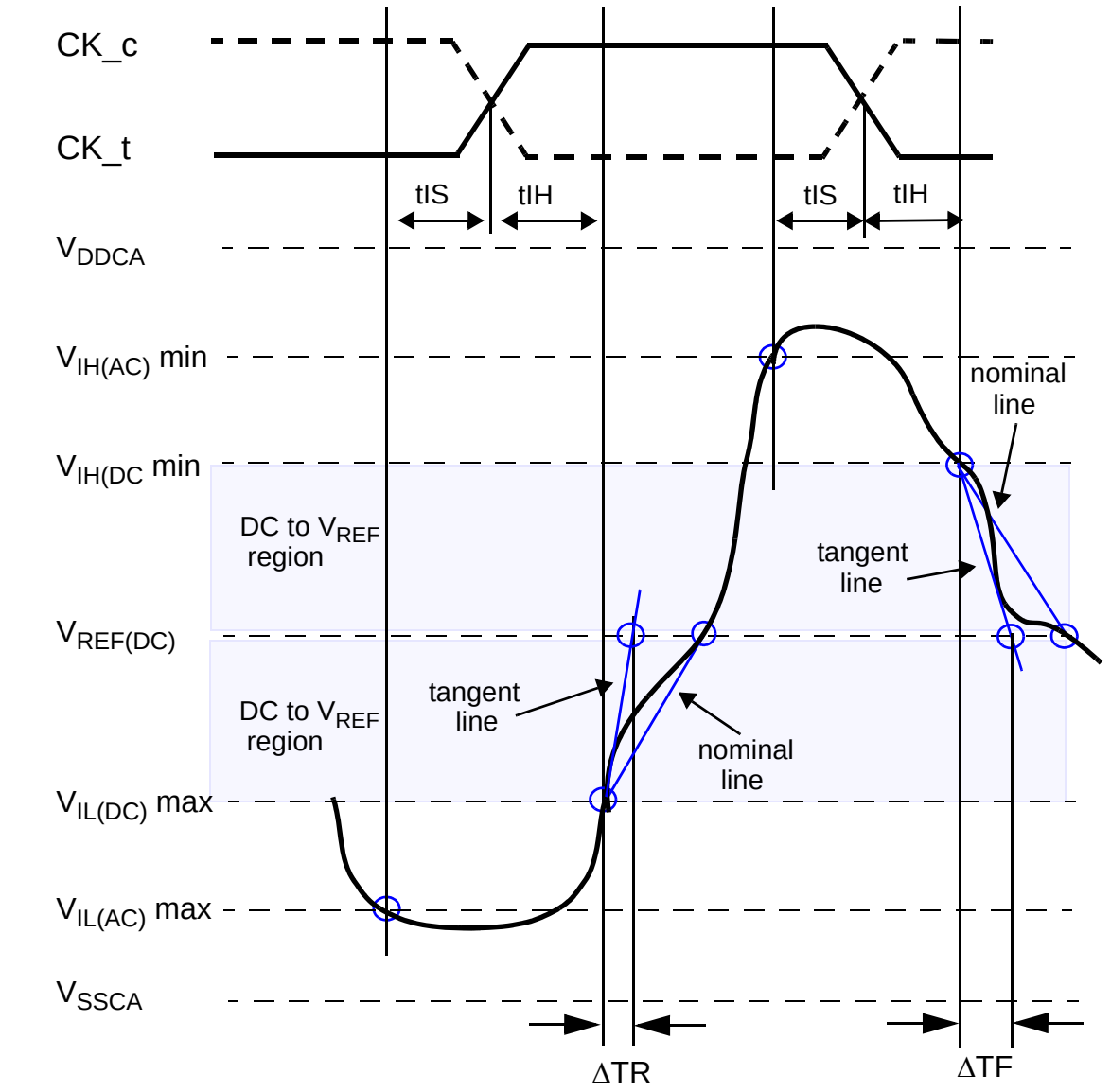


Figure. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta TF}$$

Figure. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded `VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded `VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded `dc level to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded `dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table. Data Setup and Hold Base-Values

Unit [ps]	LPDDR2				Reference
	800	667	533	466	
tDS(base)	50	130	210	230	VIH/L(AC)=VREF(DC)+/-220mV
tDH(base)	140	220	300	320	VIH/L(DC)=VREF(DC)+/-130mV

Unit [ps]	LPDDR2				Reference
	400	333	266	200	
tDS(base)	180	300	450	700	VIH/L(AC)=VREF(DC)+/-300mV
tDH(base)	280	400	550	800	VIH/L(DC)=VREF(DC)+/-200mV

Note 1: AC/DC referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS_t-DQS_c slew rate.

Table. Derating values LPDDR2 tDS/tDH - AC/DC based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based AC220 Threshold -> VIH(AC)=VREF(DC)+220mV, VIL(AC)=VREF(DC)-220mV DC130 Threshold -> VIH(AC)=VREF(DC)+130mV, VIL(DC)=VREF(DC)-130mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ,DM Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Note 1: Cell contents shaded in red are defined as ‘not supported’

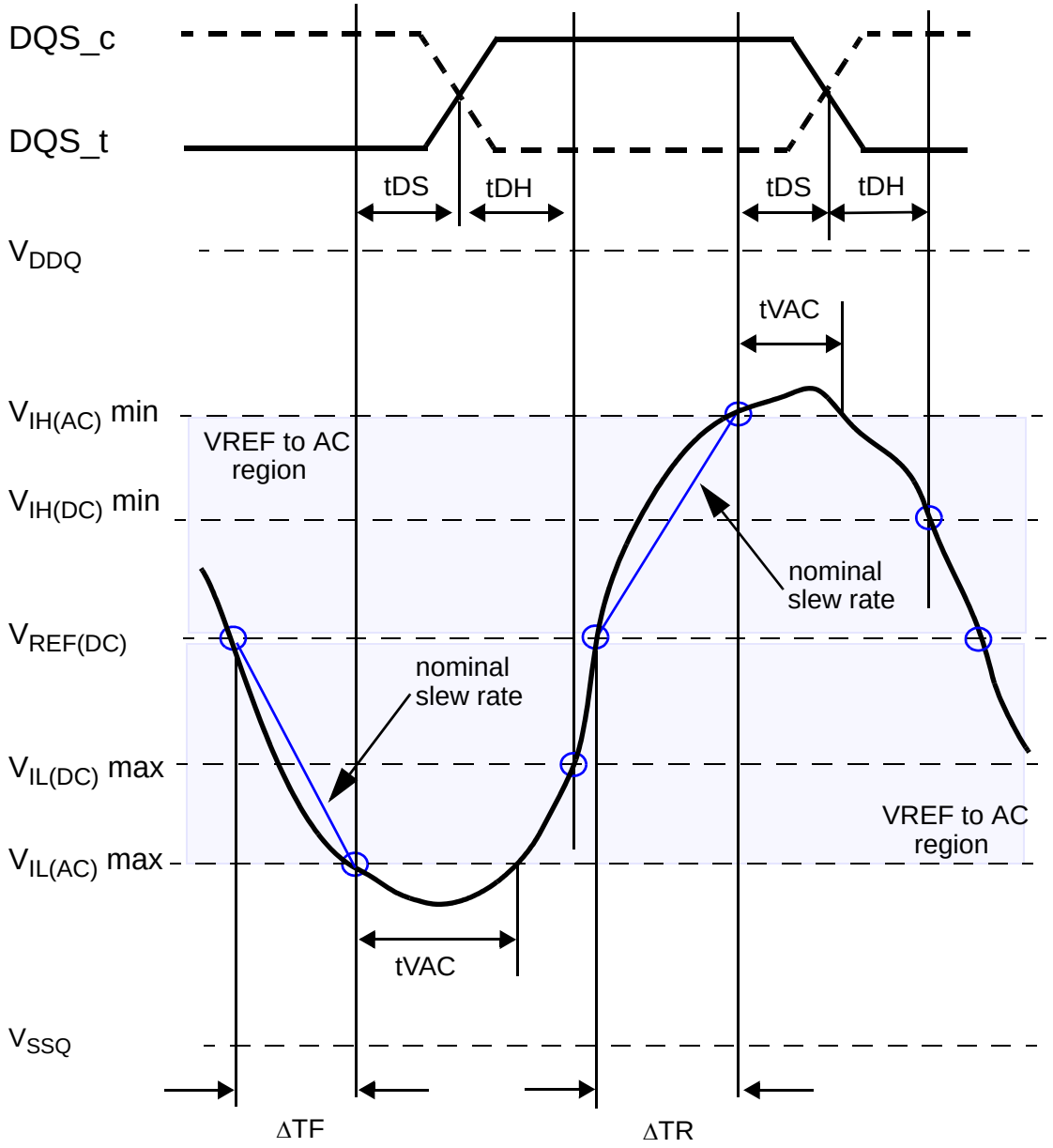
Table. Derating values LPDDR2 tDS/tDH - AC/DC based AC300

ΔtDS, ΔDH derating in [ps] AC/DC based AC300 Threshold -> VIH(AC)=VREF(DC)+300mV, VIL(AC)=VREF(DC)-300mV DC200 Threshold -> VIH(DC)=VREF(DC)+200mV, VIL(DC)=VREF(DC)-200mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ,DM Slew rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	-5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

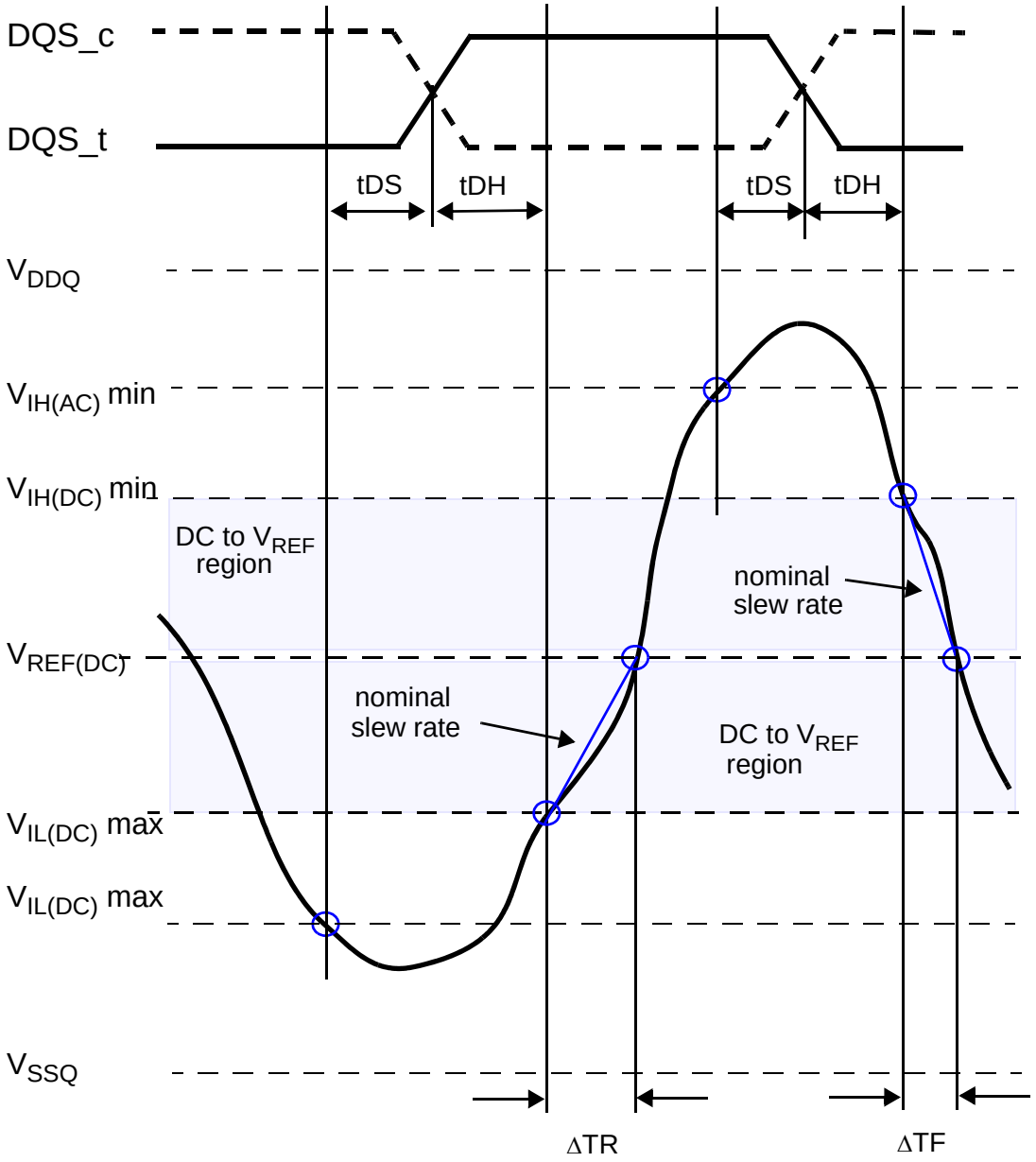
Slew Rate [V/ns]	t_{VAC}@ 300mV [ps]		t_{VAC}@220mV [ps]	
	MIN	MAX	MIN	MAX
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{REF(DC)}}{\Delta TR}$$

Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

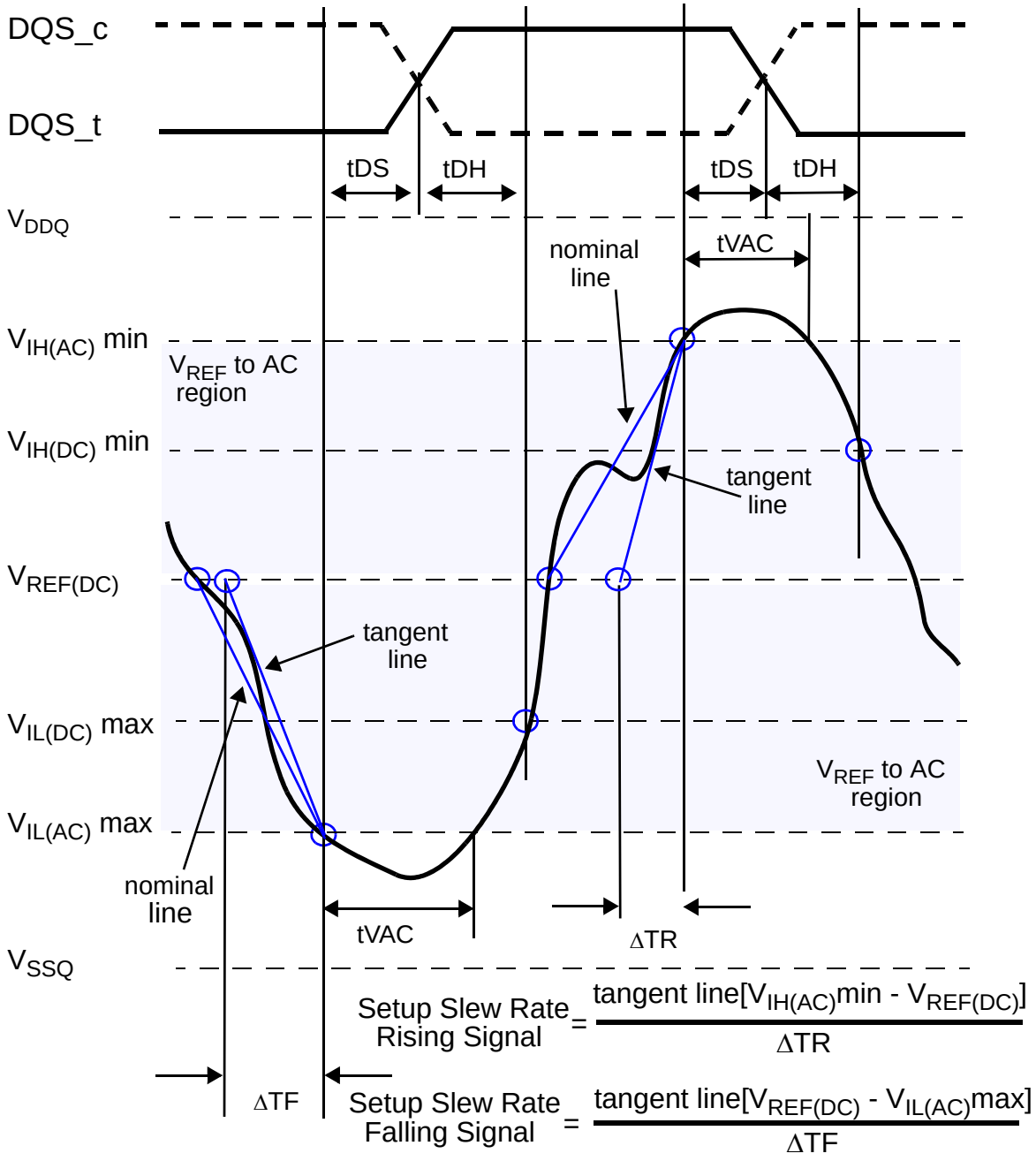


Figure. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

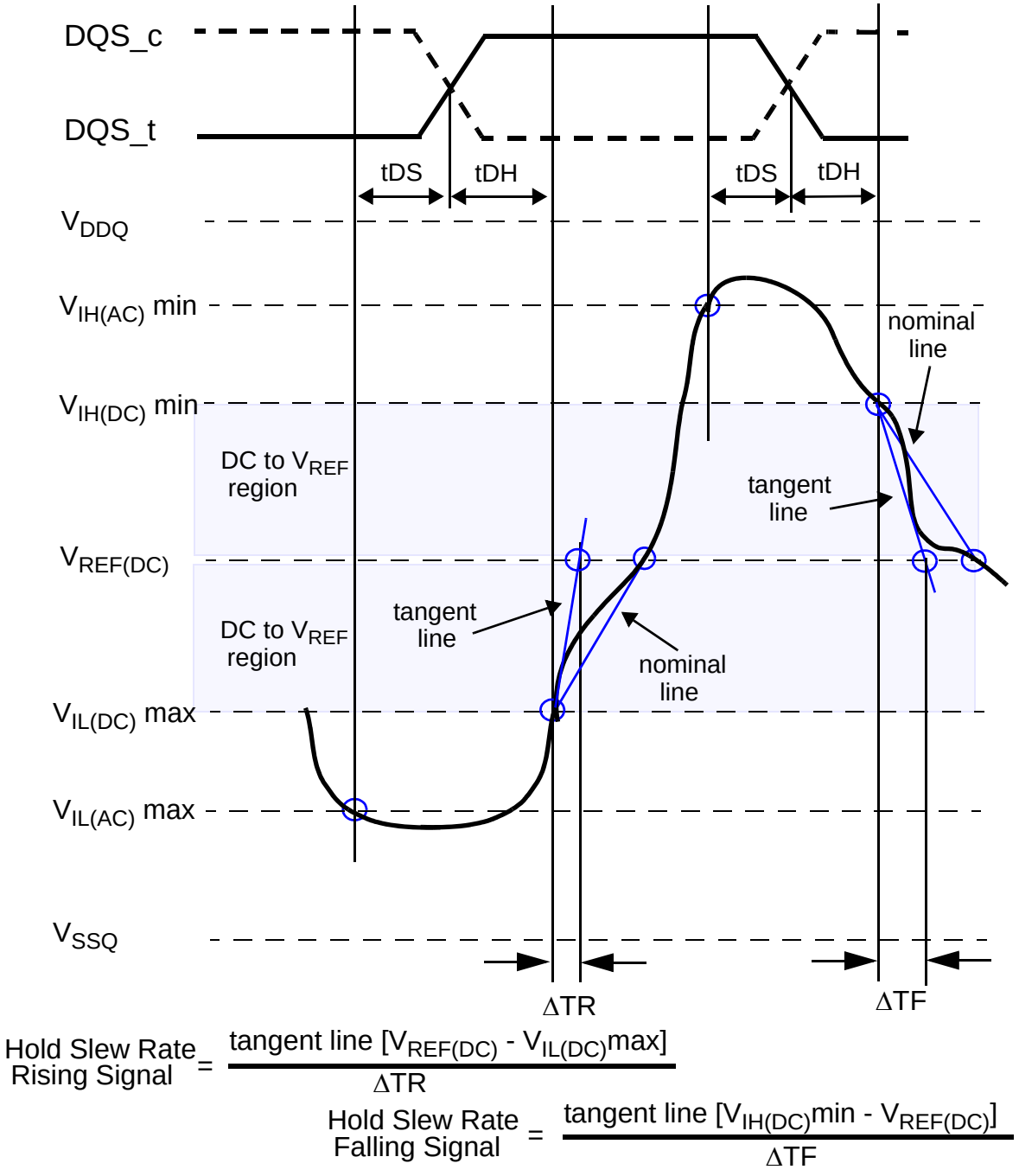


Figure. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

Command Definitions

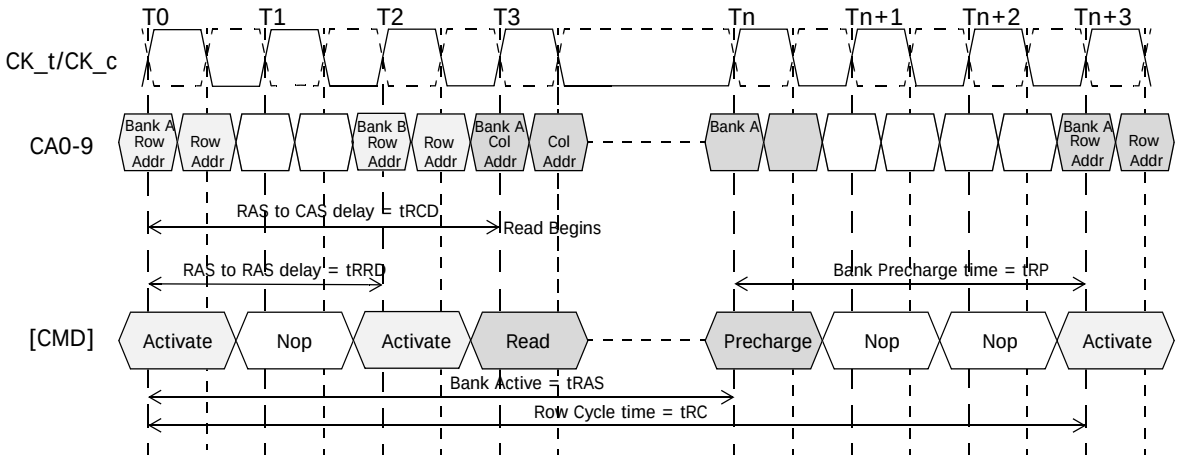
Activate command

The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

Certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

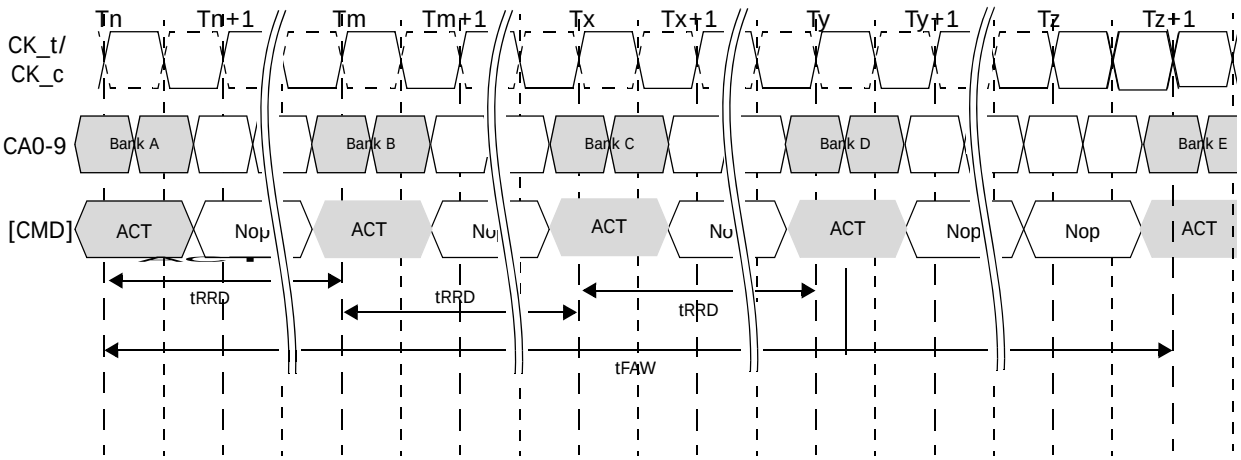
- 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by dividing tFAW [ns] by tCK [ns], and rounding up to next integer value. As an example of the rolling window, if RU {(tFAW / tCK)} is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

- 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device shall equal to tRPab, which is greater than tRPpb.



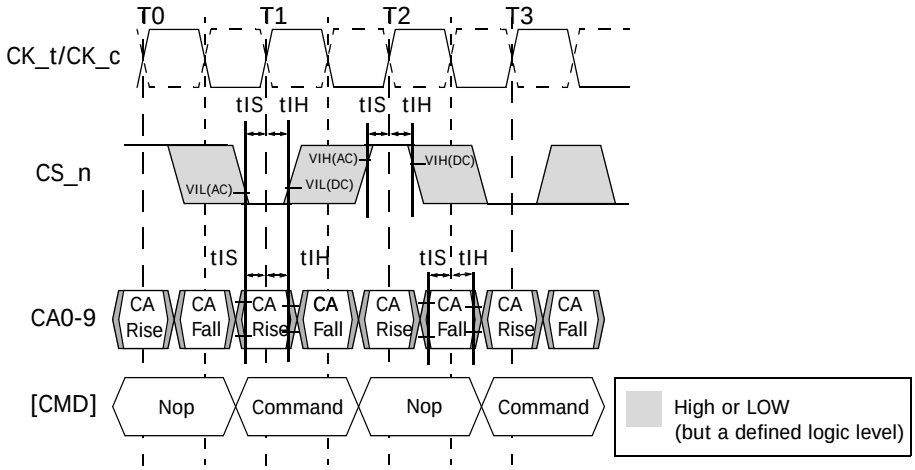
Note:
1. A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge.

Figure. LPDDR2-S4: Activate command cycle tRCD = 3, tRP = 3, tRRD = 2



Note: 1. For 8-bank devices only. No more than 4 banks may be activated in a rolling tFAW window.

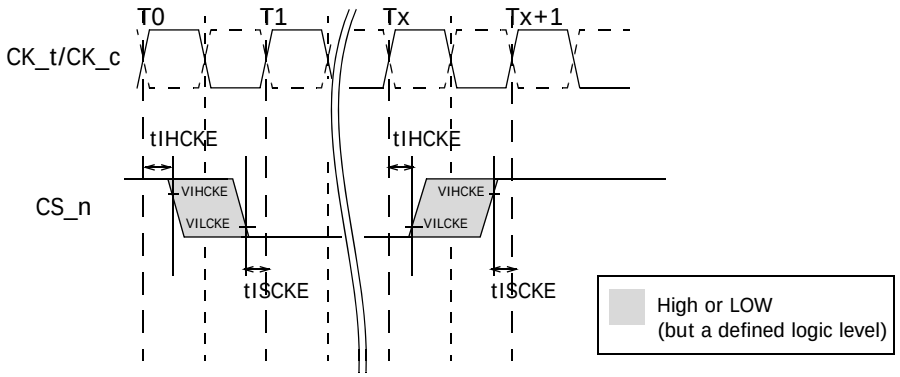
Figure. LPDDR2-S4: tFAW timing



Note:

1. Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure. LPDDR2-S4 Command Input Setup and Hold timing



Note:
1. After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

Figure. LPDDR2-S4 CKE Input Setup and Hold timing

Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).
The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.
For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL=16 settings, reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and tCCD is met. The Minimum CAS to CAS delay is defined by tCCD

Burst read command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available (RL x tCK) + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers. Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

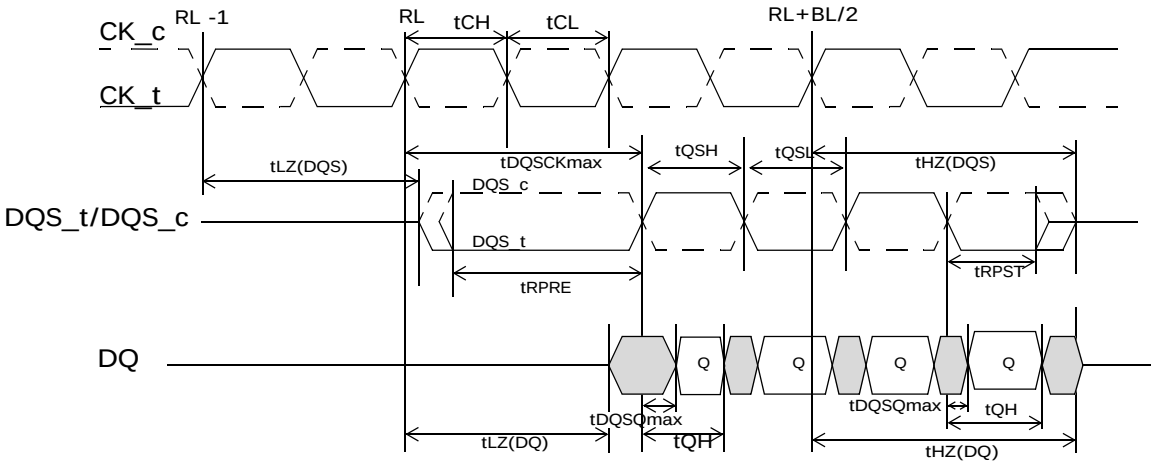


Figure. LPDDR2-S4: Data Output (Read) Timing (tDQSCKmax)

Note:

1. tDQSCK may span multiple clock periods.
2. An effective Burst Length of 4 is shown.

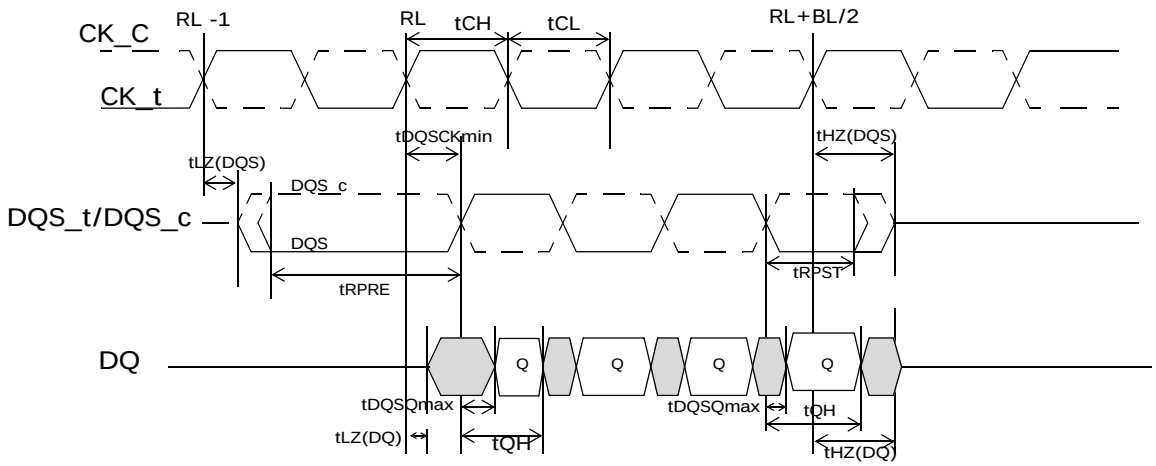


Figure. LPDDR2-S4: Data Output (Read) Timing (tDQSCKmin)

Note:

1. An effective Burst Length of 4 is shown.

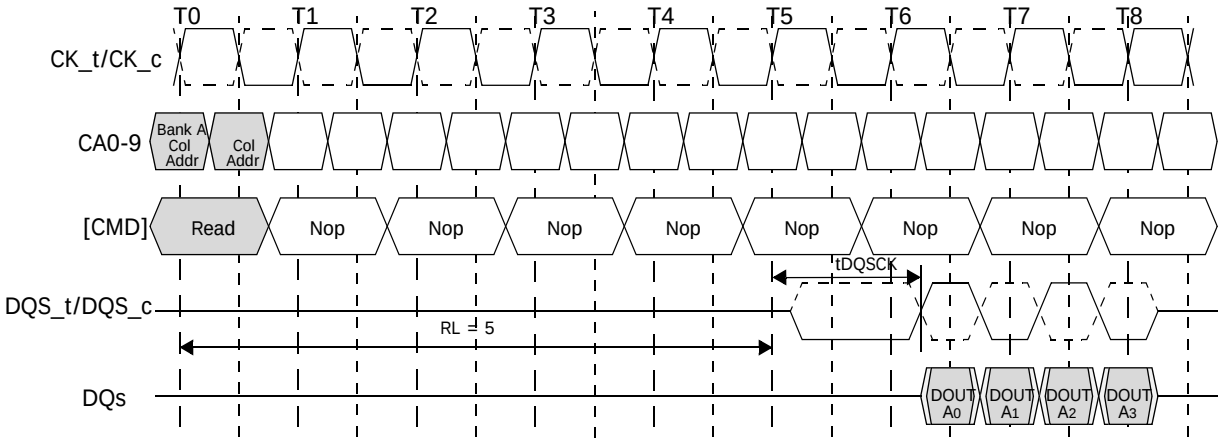


Figure. LPDDR2-S4: Burst read: RL = 5, BL = 4, tDQSCK>tCK

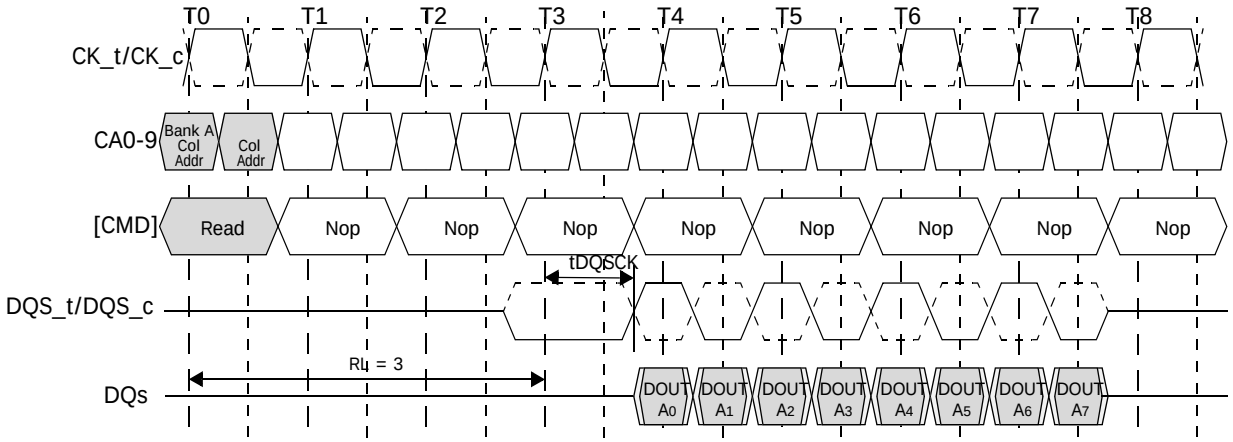


Figure. LPDDR2-S4: Burst read: RL = 3, BL = 8, tDQSCK<tCK

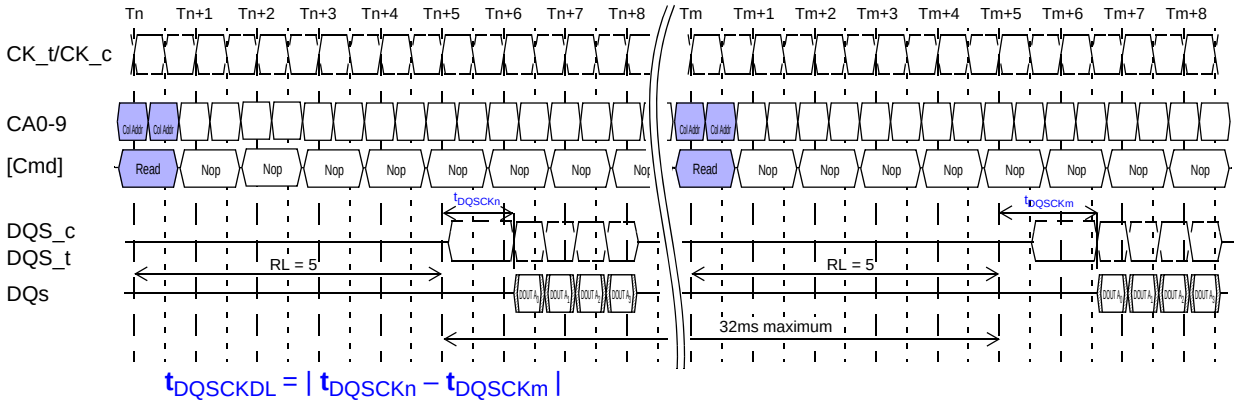


Figure. LPDDR2-S4: tDQSCKDL Timing

Note: 1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 32ms rolling window.

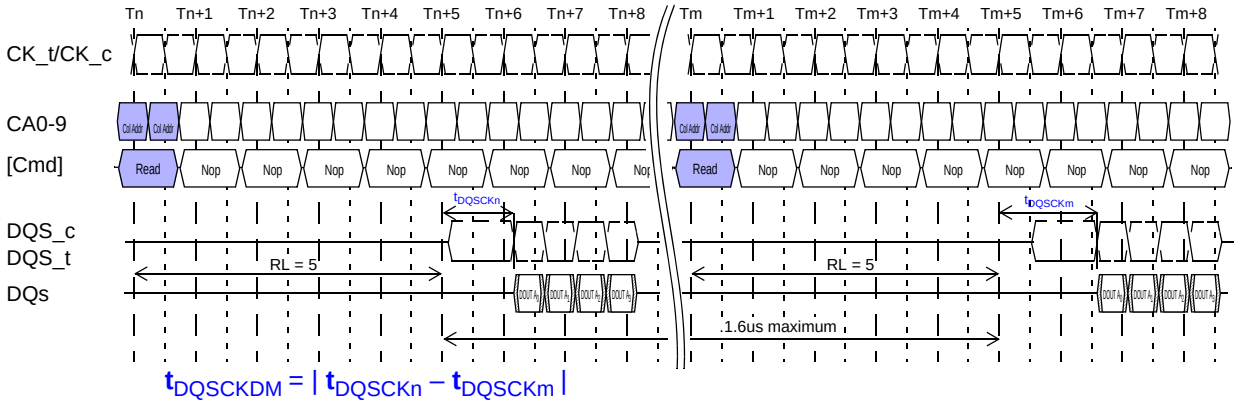


Figure. LPDDR2-S4: tDQSCKDM Timing

Note: 1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6us rolling window.

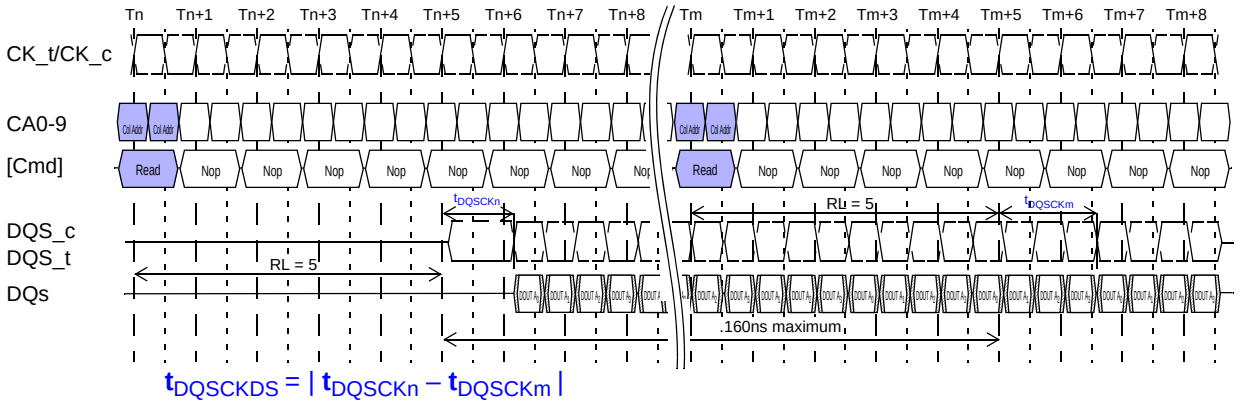


Figure. LPDDR2-S4: tDQSCKDS Timing

Note 1: tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.

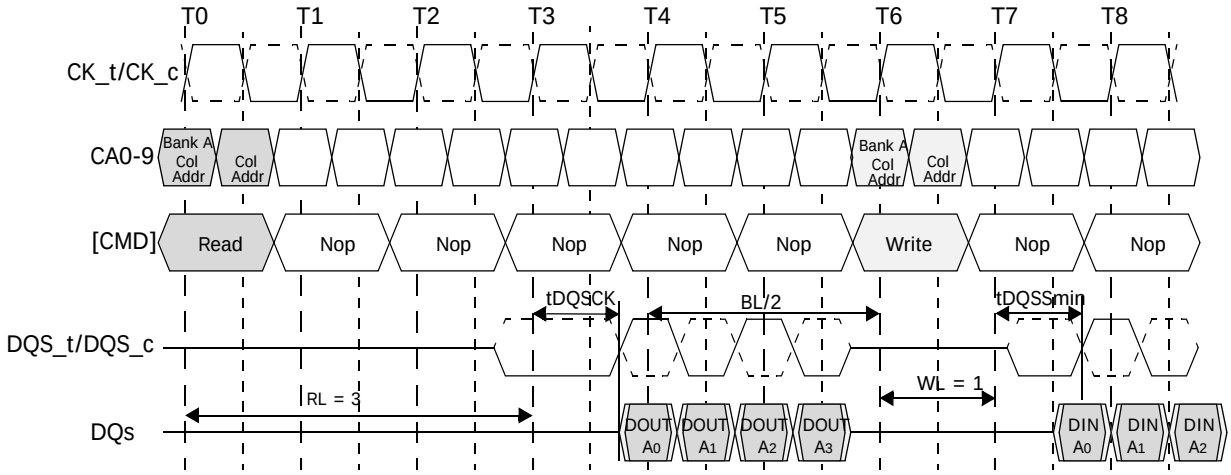


Figure. LPDDR2-S4: Burst read followed by burst write: RL = 3, WL = 1, BL = 4

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU (tDQSCKmax/tCK) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective BL of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

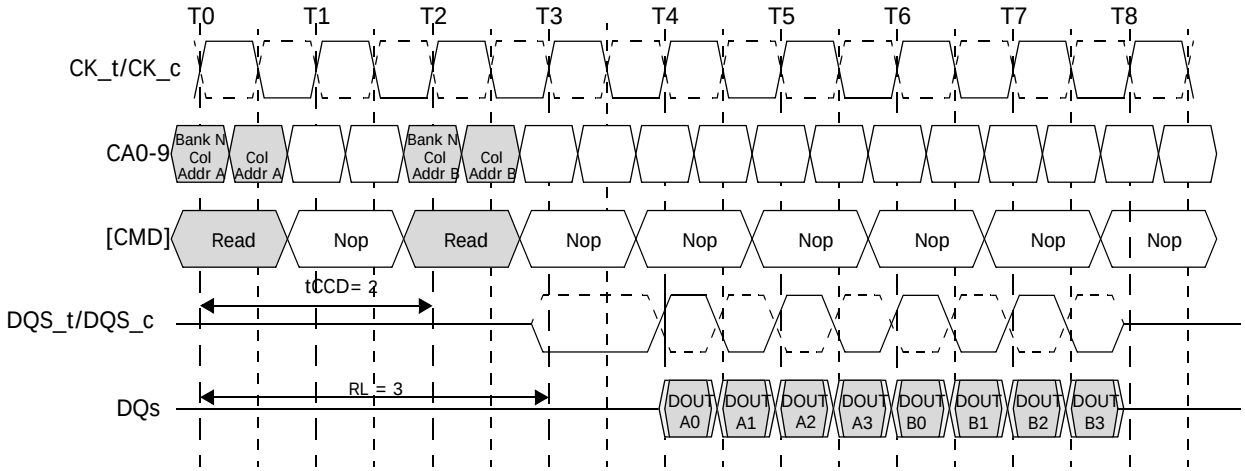
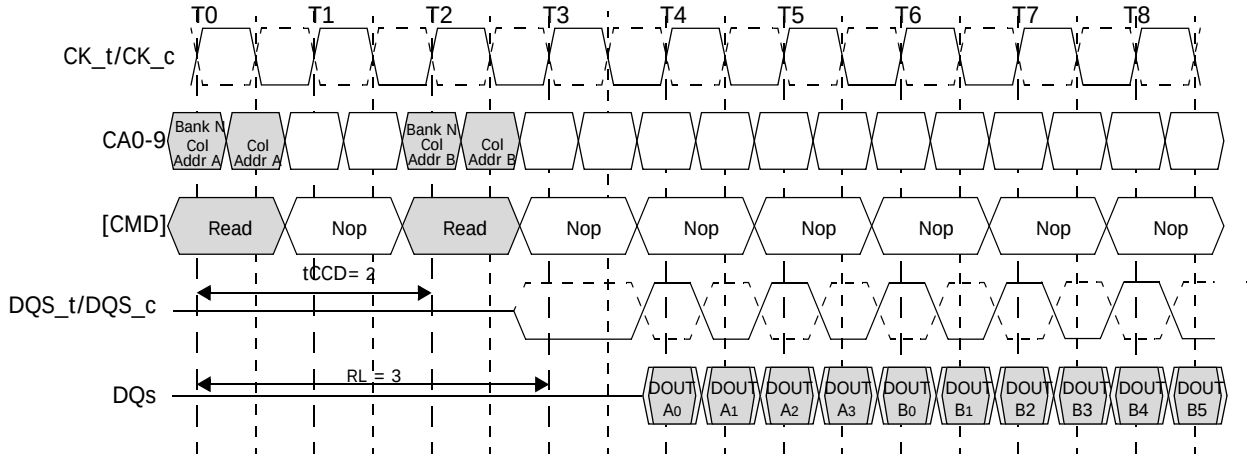


Figure. LPDDR2-S4: Seamless burst read: RL = 3, BL = 4 tCCD=2

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation. For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

Reads interrupted by a read

For LPDDR2-S4 devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met.



Note:

1. For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that tCCD is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Figure. LPDDR2-S4: Read burst interrupt example: RL = 3, BL = 8 tCCD=2

Burst write operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs CA5r-CA6r and CA1f-CA9f determine the starting column address for the burst. The Write latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid datum shall be driven WL * tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW tWPRE prior to the data input. The data bits of the burst cycle must be applied to the DQ pins tDS prior to the respective edge of the DQS_t, DQS_c and held valid until tDH after that edge. The burst data are sampled on successive edges of the DQS_t, DQS_c until the burst length is completed, which is 4, 8, or 16 bit burst.
For LPDDR2 SDRAM devices, tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation.
Input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

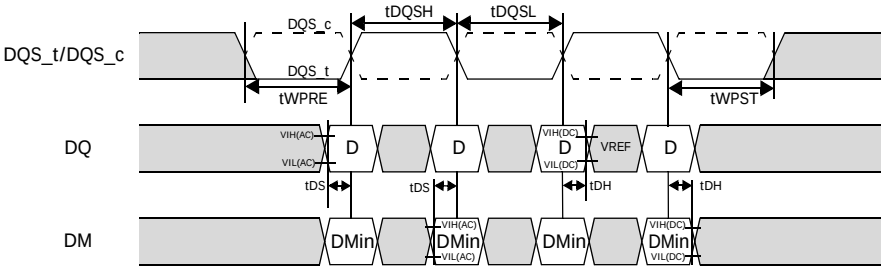


Figure. LPDDR2-S4: Data input (Write) timing

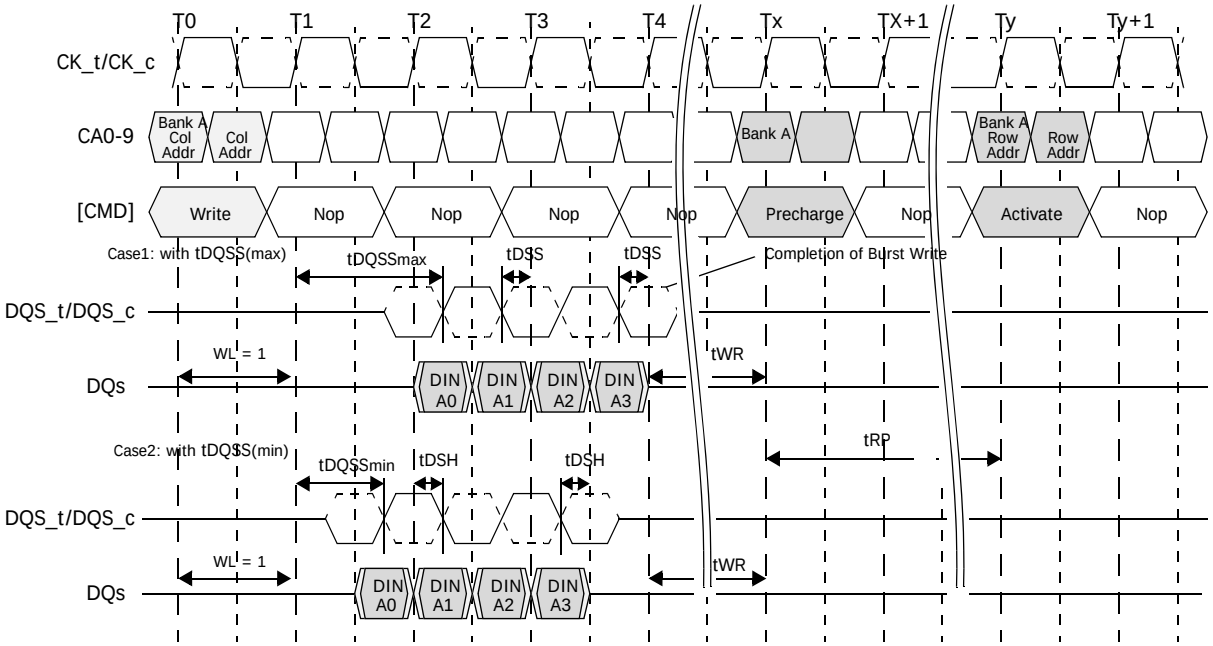
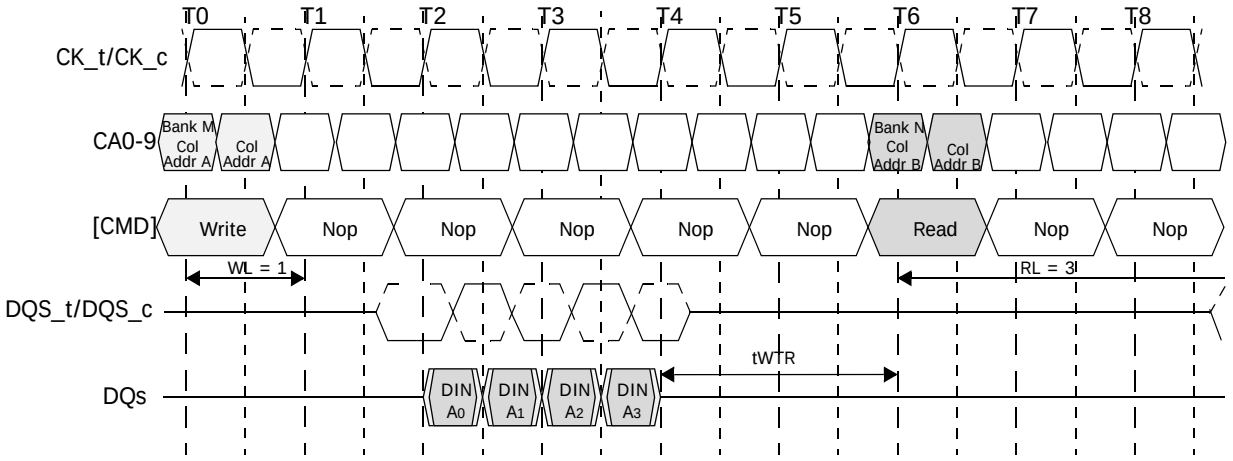


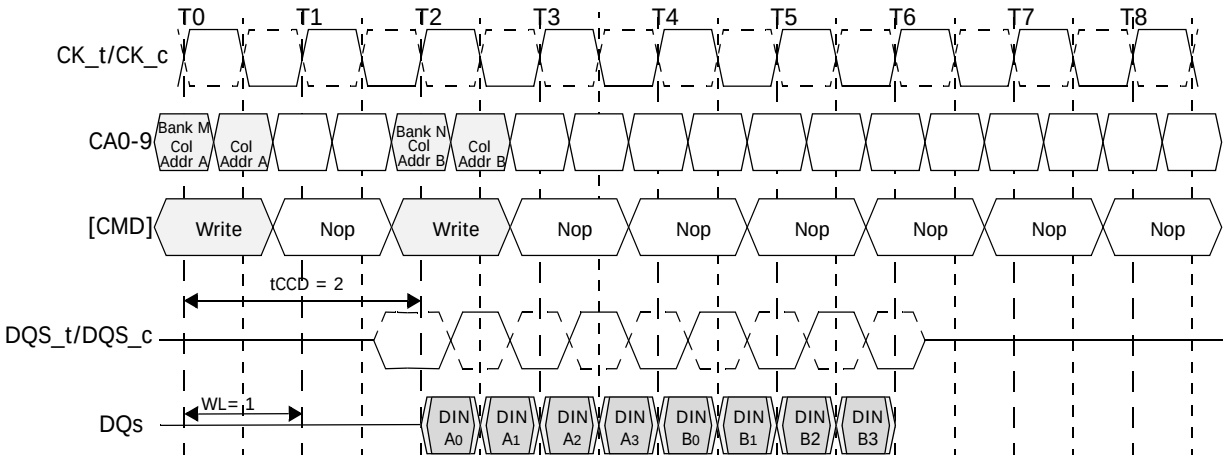
Figure. LPDDR2-S4: Burst write WL = 1, BL = 4



Note:

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

Figure. LPDDR2-S4: Burst write followed by burst Read: RL = 3, WL = 1, BL = 4



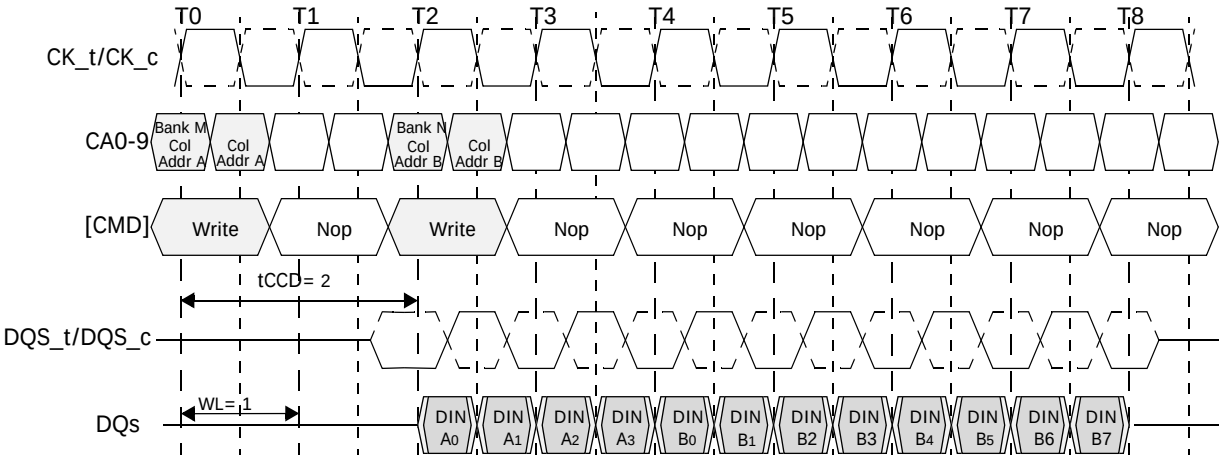
Note:

1. The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure. LPDDR2-S4: Seamless burst write: WL = 1, BL = 4, tCCD=2

Writes interrupted by a write

For LPDDR2-S4 devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that tCCD(min) is met.



Note:

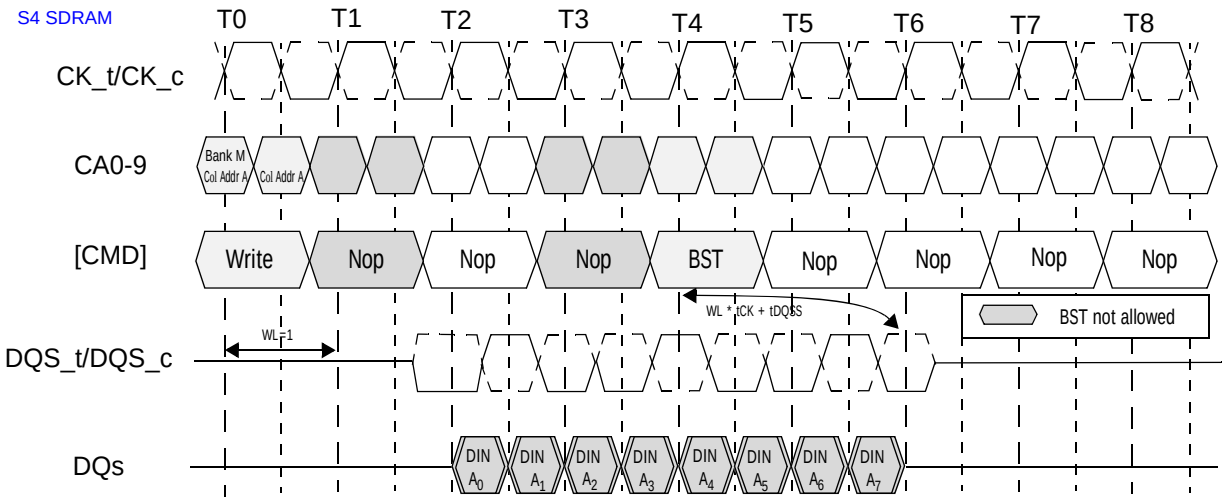
1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

Figure. LPDDR2-S4: Write burst interrupt timing: WL = 1, BL = 8, tCCD=2

Burst Terminate

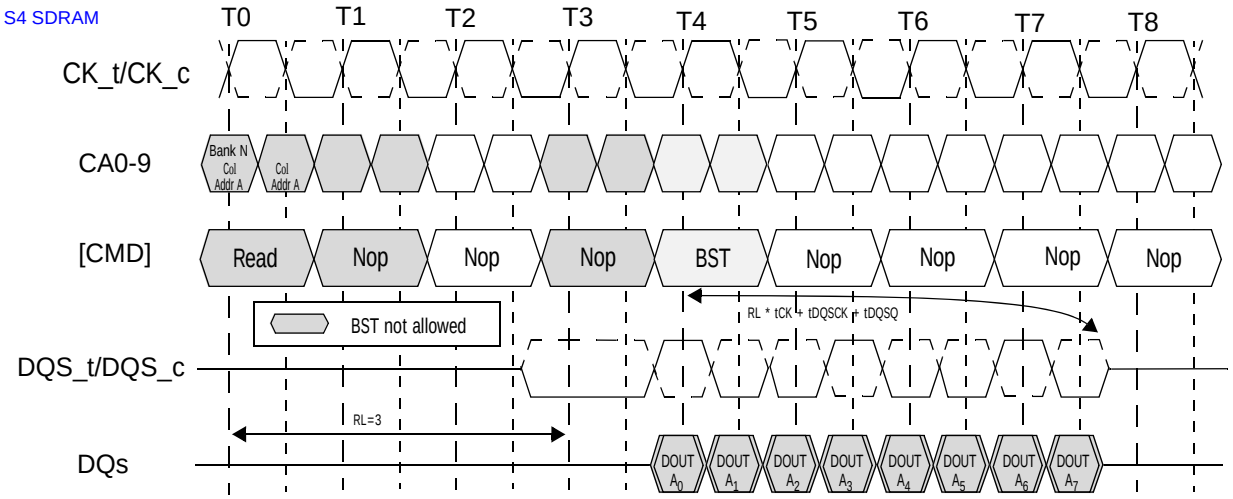
The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Terminate command may only be issued to terminate an active Read or Write burst.

Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:
Effective BL = 2 x {Number of clocks from the Read or Write Command to the BST command}
Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.
The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
The BST command truncates an on going write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an interger multiple of 4.



Note:
1. The BST command truncates an on going write burst WL *tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Figure. LPDDR2-S4: Burst Write truncated by BST: WL = 1, BL =16

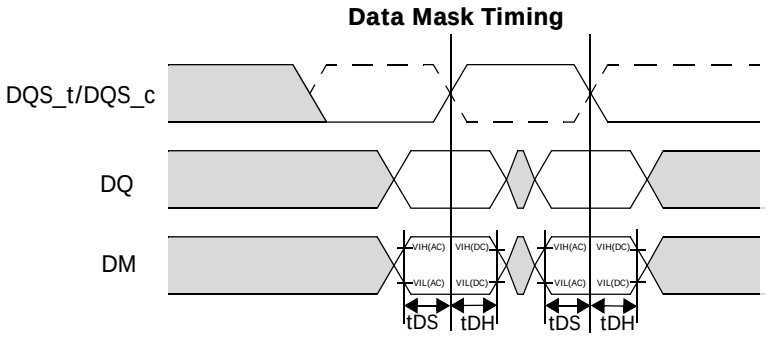


Note.
1. The BST command truncates an on going read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Figure. LPDDR2-S4: Burst Read truncated by BST: RL = 3, BL =16

Write data mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAM. Each data mask(DM) may mask its respective data byte(DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.



Data Mask Function: WL = 2, BL = 4 shown, second DQ masked

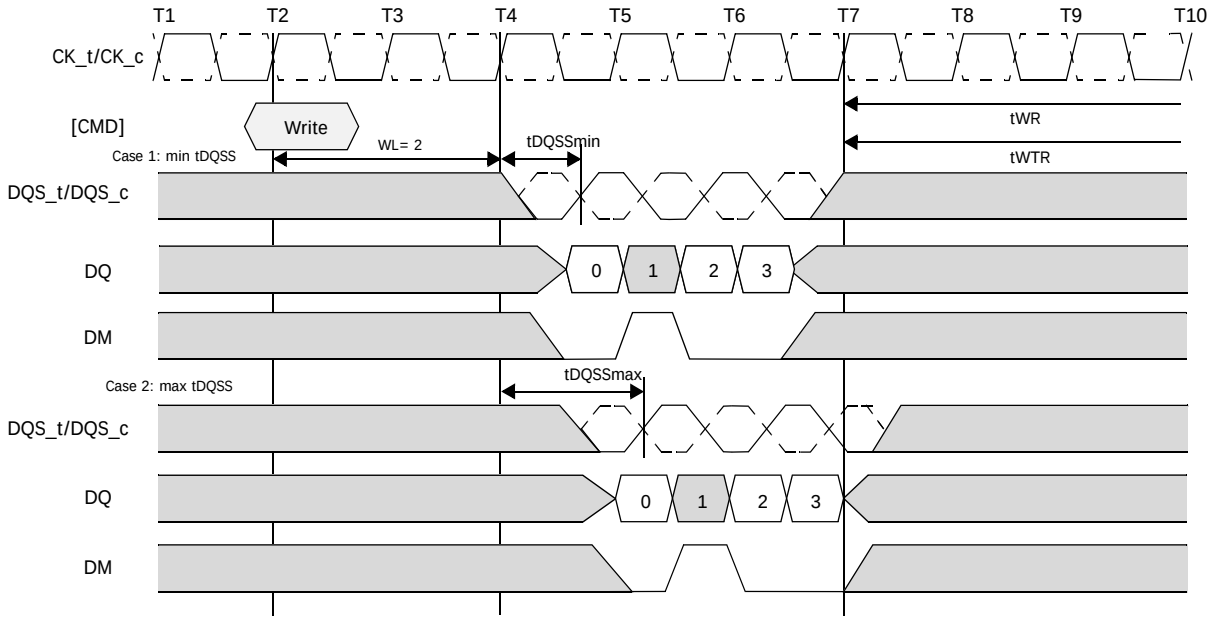


Figure. LPDDR2-S4: Write data mask

Precharge

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge for 8-bank devices (tRPab) will be longer than the Row Precharge time for a Single-Bank Precharge (tRPpb). For 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge (tRPab) is equal to the Row Precharge time for a Single-Bank Precharge (tRPpb).

Table. Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don’t Care	Don’t Care	Don’t Care	All Banks	All Banks

Burst read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A pre-charge command cannot be issued until after tRAS is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called tRTP (Read to Precharge). For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when tRTP begins.

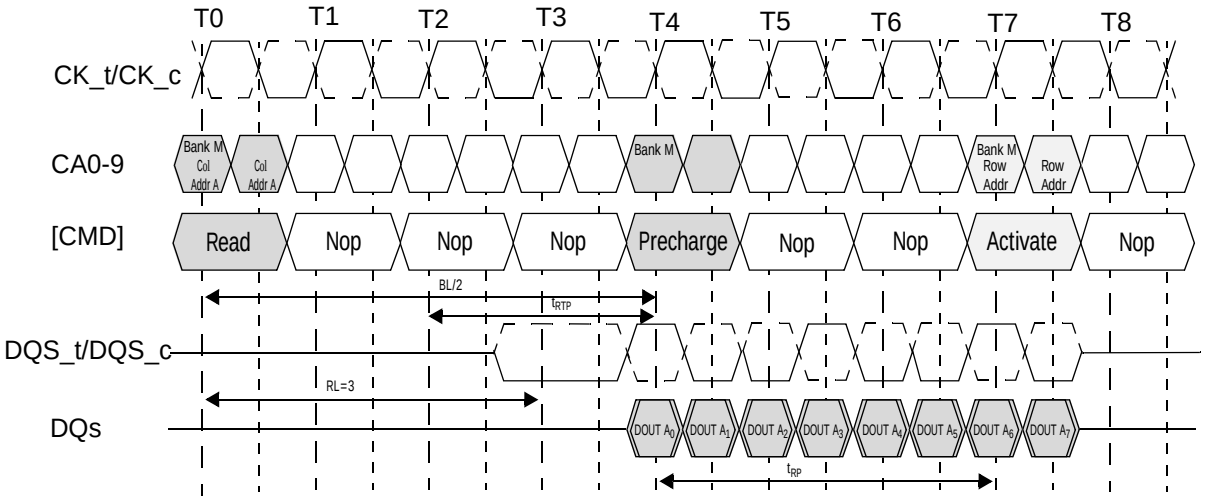


Figure. LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL =8, RU(tRTP(min)/tCK) = 2

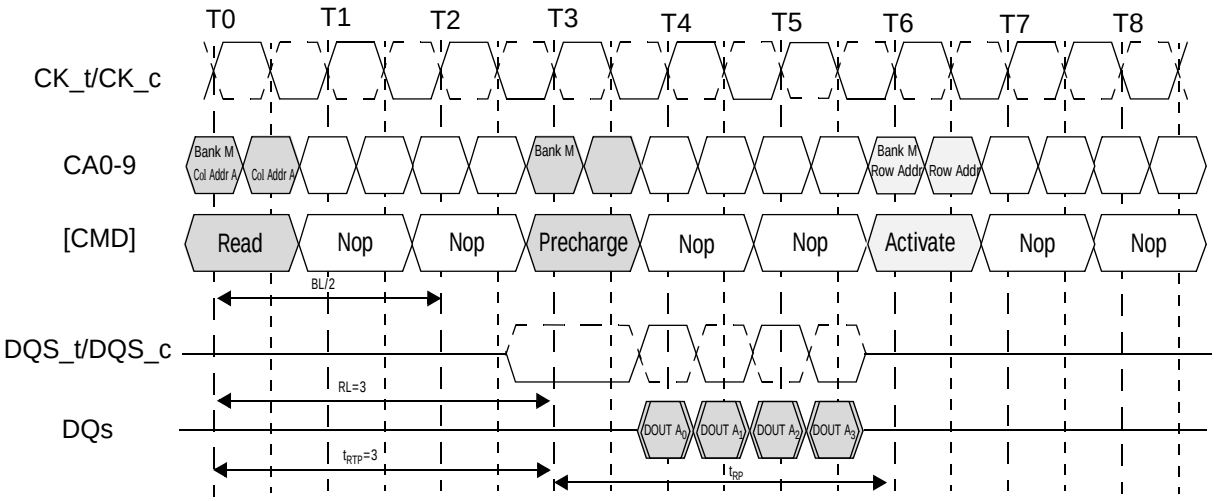


Figure. LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL =4, RU(tRTP(min)/tCK) = 3

Burst write followed by precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the tWR delay. LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely.

For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

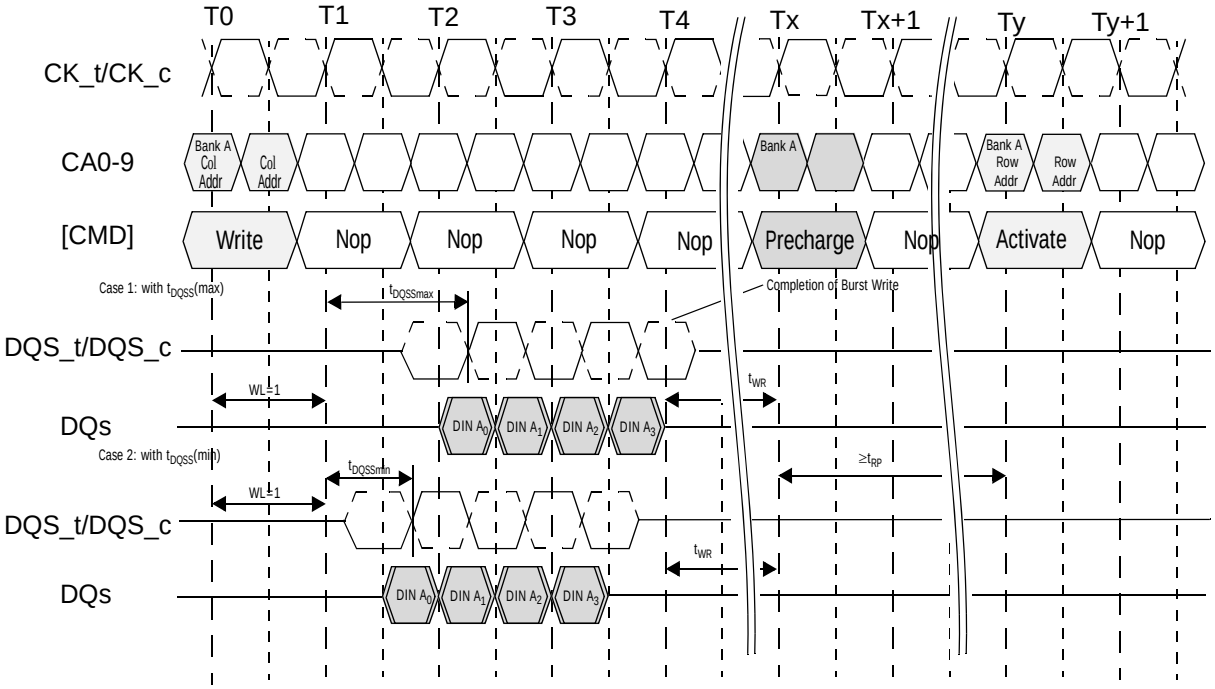


Figure. LPDDR2-S4: Burst write followed by Precharge: WL = 1, BL =4

Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

Burst Read with Auto Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater. Refer to the table of Precharge and Auto Precharge clarification for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (tRC) from the previous bank activation has been satisfied.

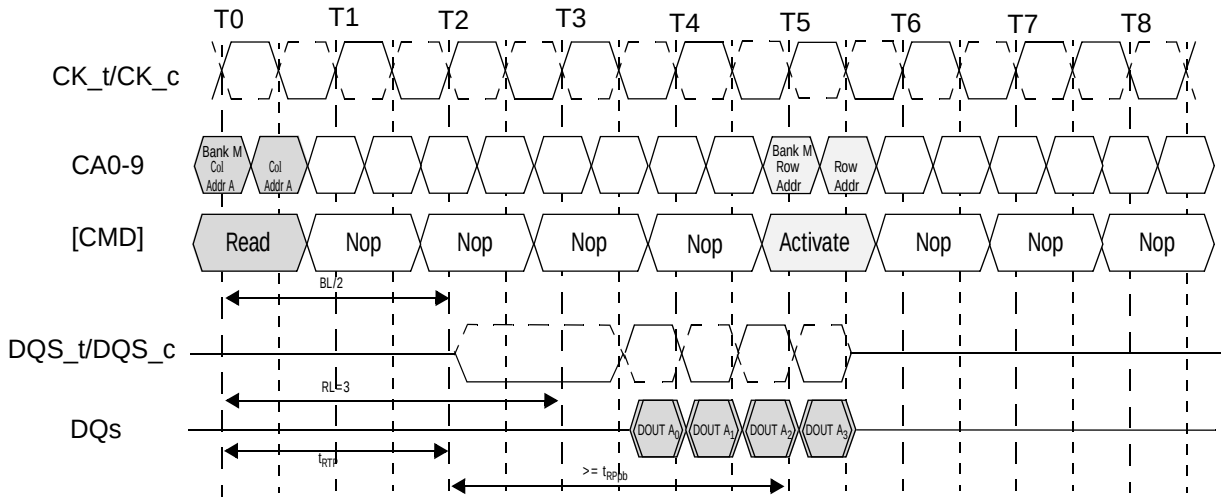


Figure. LPDDR2-S4: Burst read with Auto-Precharge:
RL = 3, BL =4, RU (t_{RTP}(min) / t_{CK}) =2

Burst Write with Auto Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied. The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

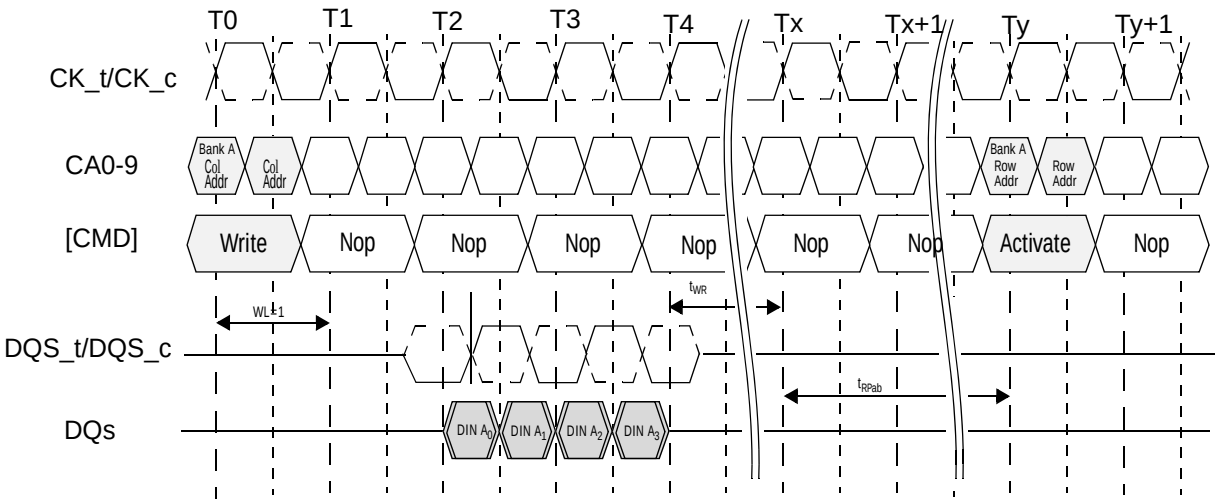


Figure. LPDDR2-S4: Burst write with Auto Precharge: WL = 1, BL =4

Table. LPDDR2-S4: Precharge and auto precharge clarification

From command	To command	Minimum delay between From command to To command	Unit	Notes
Read	Precharge (to same bank as read)	BL/2 + max(2, RU (tRTP/tCK)) - 2	CLK	1
	Precharge All	BL/2 + max(2, RU (tRTP/tCK)) - 2	CLK	1
BST (for Reads)	Precharge (to same bank as read)	1	CLK	1
	Precharge All	1	CLK	1
Read w/ AP	Precharge (to same bank as read w/ AP)	BL/2 + max(2, RU (tRTP/tCK)) - 2	CLK	1
	Precharge (to different bank)	1	CLK	1
	Precharge All	BL/2 + max(2, RU (tRTP/tCK)) - 2	CLK	1
	Activate (to same bank as read w/ AP)	BL/2 + max(2, RU (tRTP/tCK)) - 2 + RU(tRPpb/tCK)	CLK	1
	Activate (to different bank)	1	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) -WL + 1	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	BL/2	CLK	3
Write	Precharge (to same bank as write)	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
BST (for Writes)	Precharge (to same bank as Write)	WL + RU(tWR/tCK) + 1	CLK	1
	Precharge All	WL + RU(tWR/tCK) + 1	CLK	1
Write w/ AP	Precharge (to same bank as write w/ AP)	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Activate (to same bank as write w/ AP)	WL + BL/2 + RU (tWR/tCK) + 1 + RU(tRPpb/tCK)	CLK	1
	Activate (to different bank)	1	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	BL/2	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	CLK	3
Precharge	Precharge (to same bank as precharge)	1	CLK	1
	Precharge All	1	CLK	1
Precharge All	Precharge	1	CLK	1
	Precharge All	1	CLK	1

Note:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified in Table above is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

Refresh Command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command.

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

As shown in Table of Command Scheduling Separations related to Refresh, the REFpb command may not be issued to the memory until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior Precharge command to that given bank

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessible during the Per Bank Refresh cycle time (tRFCpb), however other banks within the device are accessible and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.

As shown in Table of Command Scheduling Separations related to Refresh, after issuing REFpb:

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in Table of Command Scheduling Separations related to Refresh, the REFab command may not be issued to the memory until the following conditions have been met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in Table of Command Scheduling Separations related to Refresh, after issuing REFab:

- the tRFCab latency must be satisfied before issuing an ACTIVATE command
- the tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table. Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb affecting an idle bank (different bank than Activate)	1
		Activate command to different bank than prior Activate	

Note:
1. A bank must be in the Idle state before it is refreshed. Therefore, after ACTIVATE, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.

LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh Commands:

The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within any rolling Refresh Window (tREFW=32ms @ MR4[2:0] = "011" or Tcase ≤ 85°C). See Table "Refresh Requirement Parameters (per density)" for actual numbers per density. The resulting average refresh interval (tREFI) is given in Table below.

For LPDDR2-SDRAM devices supporting Per Bank-Refresh, a REFab command may be replaced by a full cycle of eight REFpb commands.

(2) Burst Refresh limitation:

To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling tREFBW (tREFBW=4 x 8 x tRFCab). This condition does not apply if REFpb commands are used.

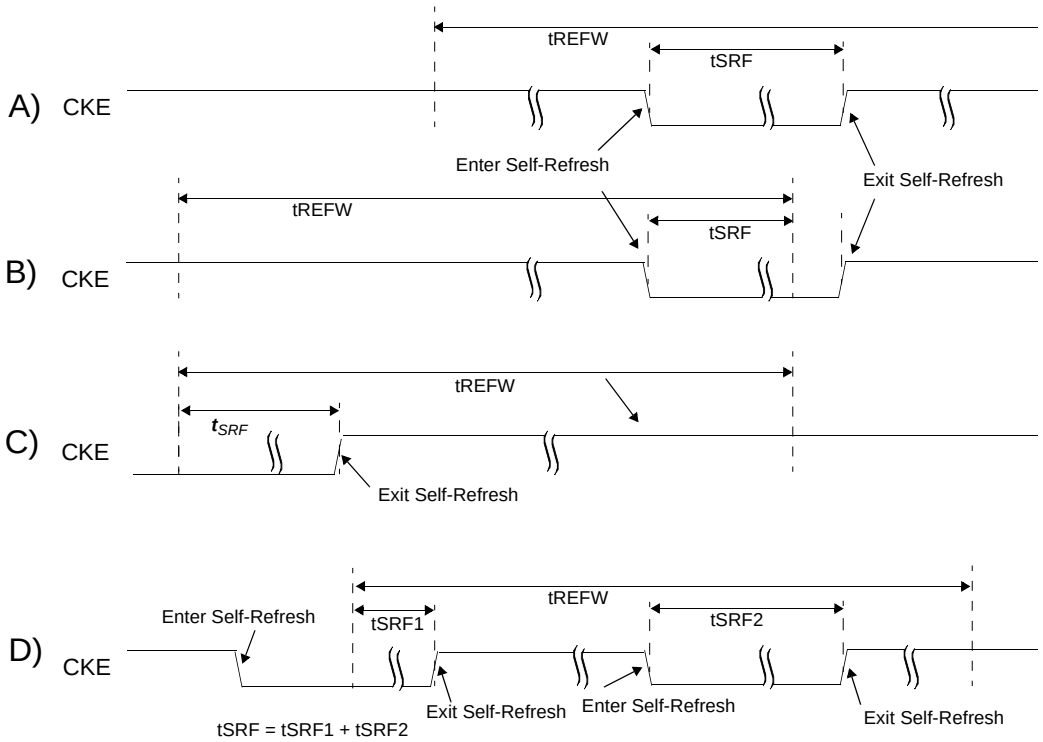
(3) Refresh Requirements and Self-Refresh:

If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R* = R - RU{tSRF/tREFI} = R - RU{R * tSRF/tREFW}; where RU stands for the round-up function.

Table. LPDDR2-S4: Refresh Requirement Parameters (per density)

Parameter		Symbol	4Gb	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Refresh Window 85°C <Tcase ≤ 105°C		t_{REFW}	8	ms
Required number of REFRESH commands (min)		R	8,192	
Average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	us



Several examples on how to tSRF is calculated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (tREFW)
B: at Self-Refresh entry
C: at Self-Refresh exit
D: with several different intervals spent in Self Refresh during one tREFW interval

Figure. Definition of tSRF

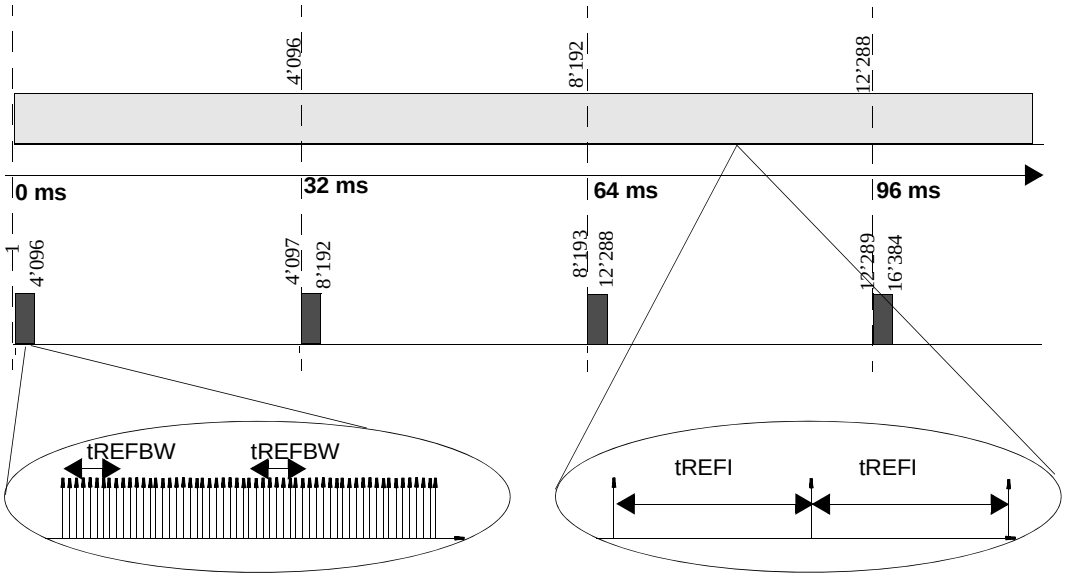
In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-S4 devices allow significant flexibility in scheduling REFRESH commands, as long as the boundary conditions above are met.

In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., 1Gb) the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achievable time without REFRESH commands is given by tREFW - R / 8 * tREFBW = tREFW - R * 4 * tRFCab. (e.g., for a 1Gb device @ Tcase ≤ 85°C this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms).

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition. Figure "Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern" shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transi-

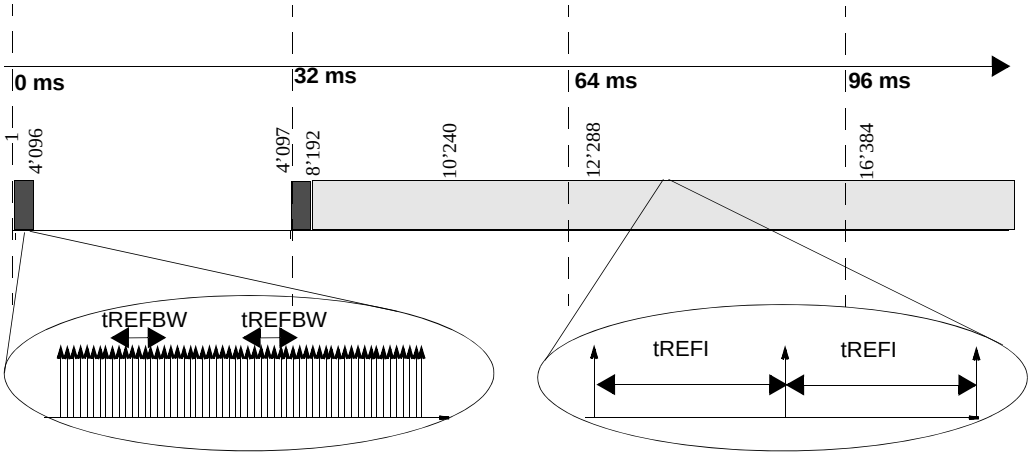
tion happens directly after the burst refresh phase, all rolling tREFW intervals will have at least the required number of refreshes. Figure “NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern” shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimum number of REFRESH commands is not satisfied. The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure “Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns.” and begin with the burst phase upon exit from Self-Refresh.



Note.

1. For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85°C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~32 ms without any REFRESH command.

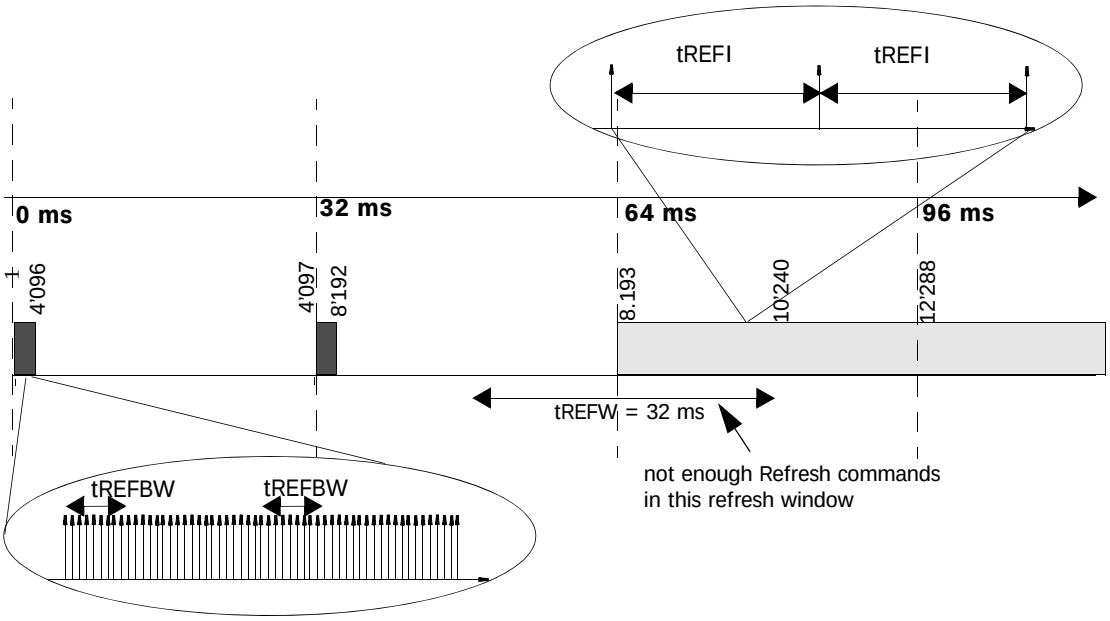
Figure. Regular, Distributed Refresh Pattern
vs. Repetitive Burst Refresh with Subsequent Refresh Pause



Note.

1. For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85°C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~32 ms without any REFRESH command.

Figure. Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



Note.

1. Only ~2048 REFRESH commands in the indicated tREFW window.

Figure. NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent

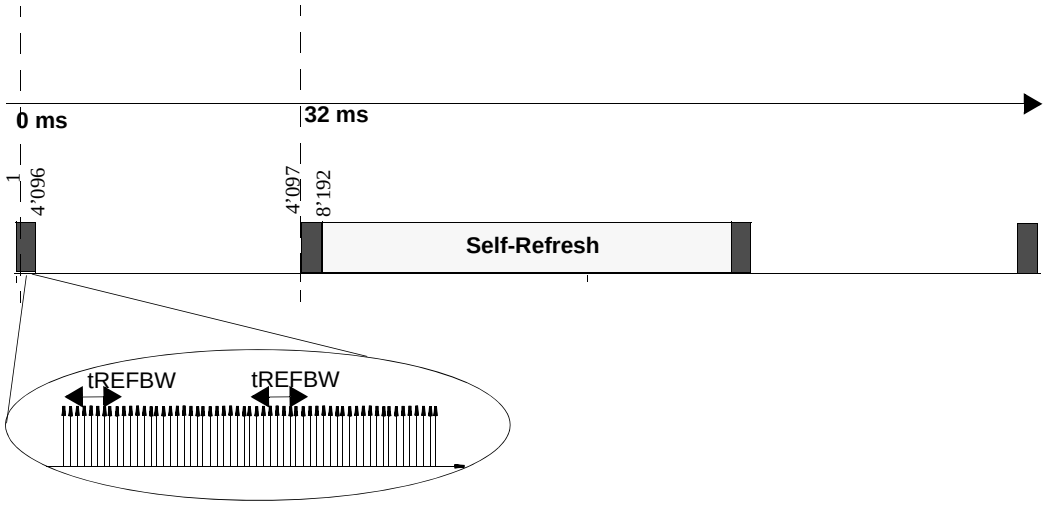


Figure. Recommended Self-refresh entry and exit in conjunction with a Burst / Pause Refresh patterns

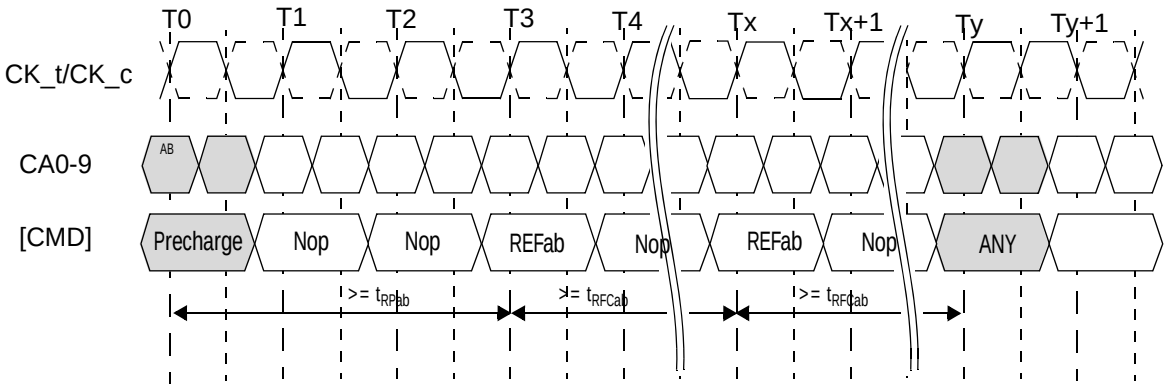
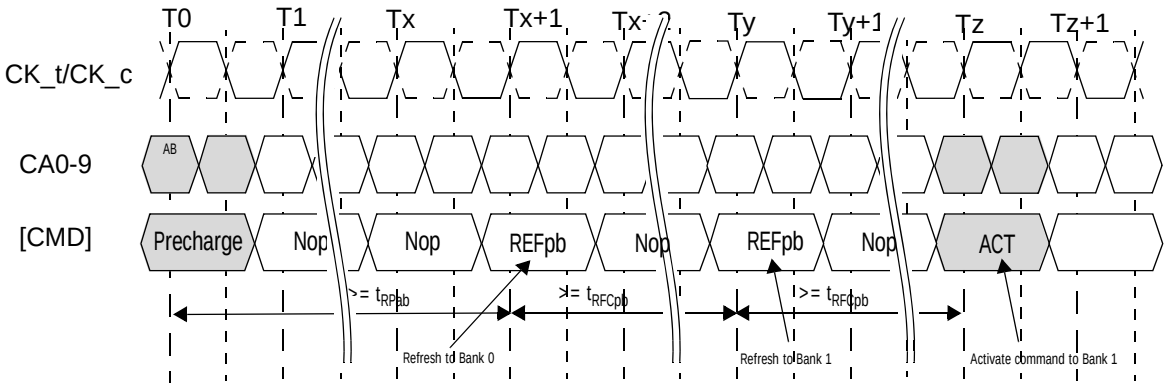


Figure. LPDDR2-S4: All Bank Refresh Operation



Note:
1. In the beginning of this example, the REFpb bank is pointing to Bank 0.
2. Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

Figure. LPDDR2-S4: Per Bank Refresh Operation

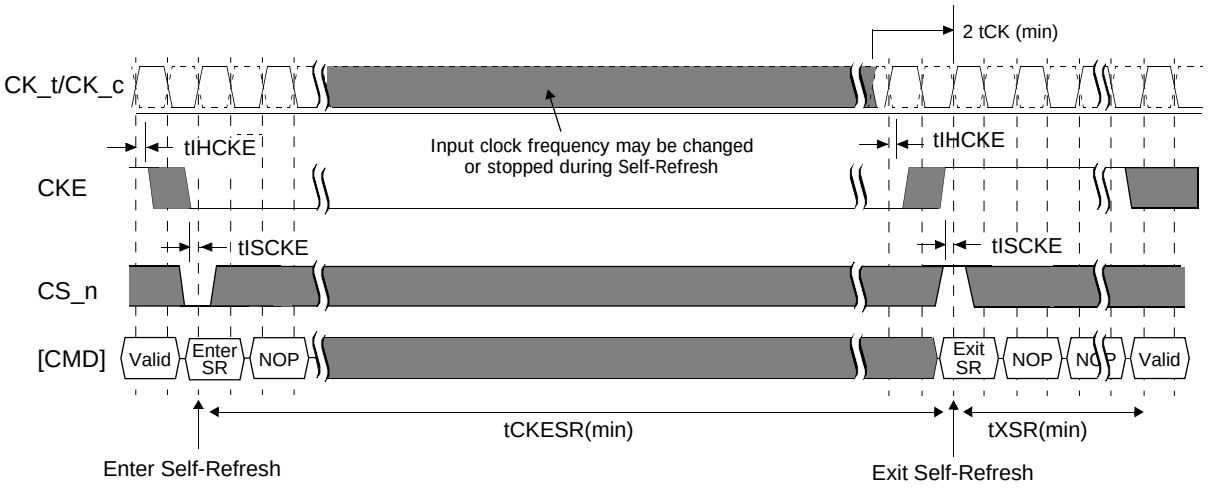
Self refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures. See "IDD Specification Parameters and Operating Conditions" for details.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are "don't care". For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits.
VREFDQ may be at any level between 0 and VDDQ and VREFCA may be at any level between 0 and VDDCA during Self-Refresh, however before exiting Self-Refresh, VREFDQ and VREFCA must be within specified limits. The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.
The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.
The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section "LPDDR2 SDRAM Refresh Requirements", since no refresh operations are performed in power-down mode.



Note:

1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

Figure. Self Refresh Operation

Partial Array Self Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following chapter.

Partial Array Self Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, "masked". Programming of segment mask bits is similar to the one of bank mask bits. For 4Gb density, 8 segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. These 2 mode register units are noted as "not used" for low-density LPDDR2-S4 SDRAM and a programming of mask bits has no effect on the device operation.

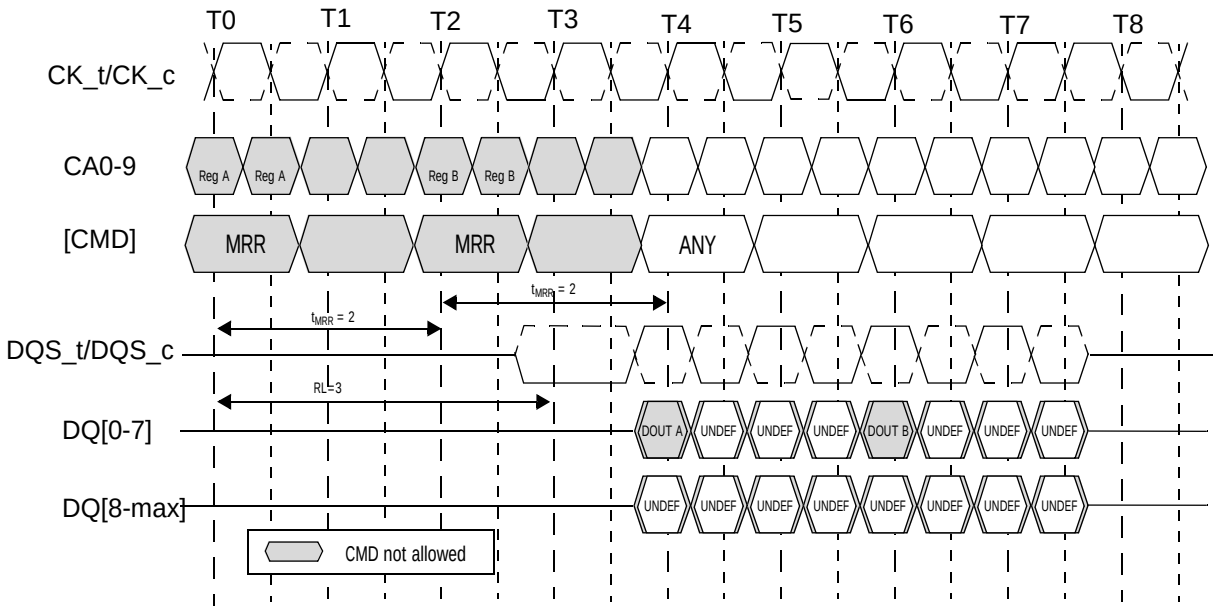
Table: Example of Bank and Segment Masking use in LPDDR2-S4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
Segment 0	**0**		**M**						**M**
Segment 1	**0**		**M**						**M**
Segment 2	**1**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**
Segment 3	**0**		**M**						**M**
Segment 4	**0**		**M**						**M**
Segment 5	**0**		**M**						**M**
Segment 6	**0**		**M**						**M**
Segment 7	**1**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**

Note: 1. This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL *tCK + tDQSCK +tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in section of DQ Calibration. All DQS_t, DQS_c shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS_t, DQS_c shall be toggled.

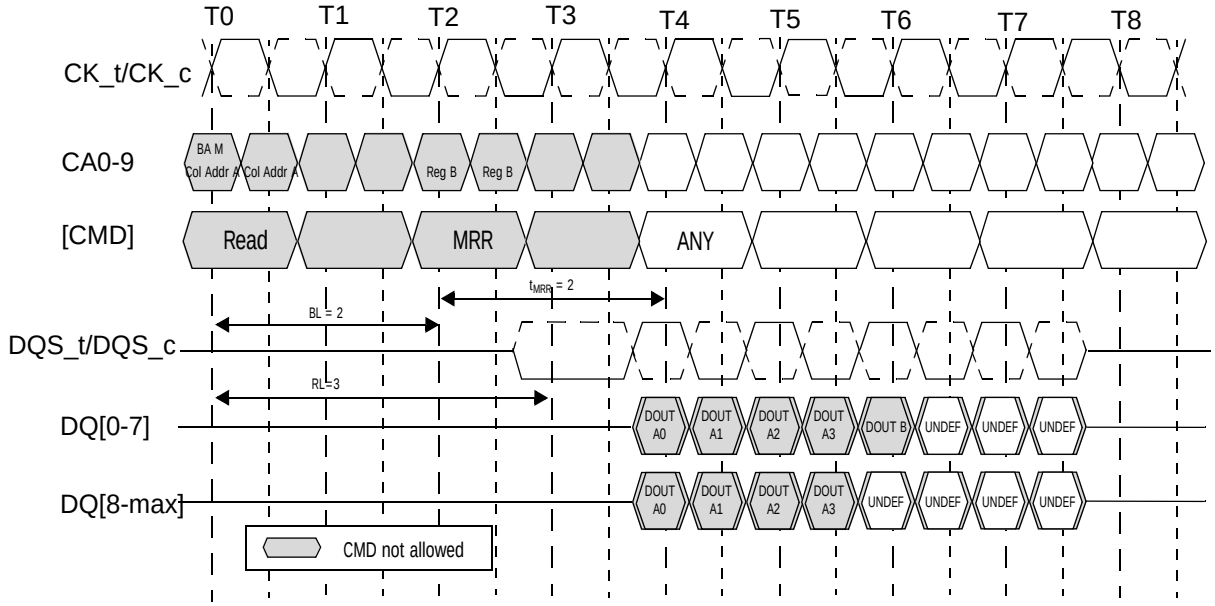


Note:

1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in section of DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Regfister Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1clock cycles.

Figure. LPDDR2-S4: Mode Register Read timing example: RL = 3, tMRR = 2

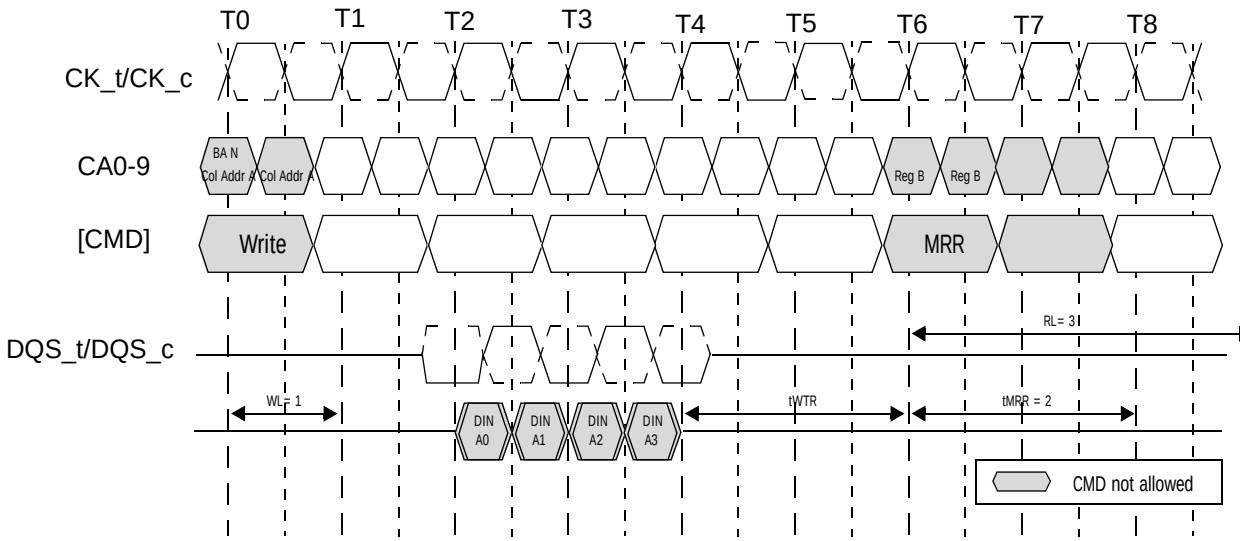
The MRR command shall not be issued earlier than BL/2 clock cycles after a prior READ command and WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”



Note:

1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

Figure. LPDDR2-S4: Read to MRR timing example: RL = 3, tMRR = 2



Note:

1. The Minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL+1+BL/2 + RU(tWTR/tCK)].
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

Figure. LPDDR2-S4: Burst Write Followed by MRR: RL=3, WL=1, BL=4

Temperature Sensor

LPDDR2-S4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the Extended Temperature Range and/or monitor the operating temperature. Either the temperature sensor or the device TOPER (See Operating Temperature Range) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85^{o}C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications should consider the following factors:
TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2^{o}C.

ReadInterval is the time period between MR4 reads from the system.
TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
SysRespDelay is the maximum time between a read of MR4 and the response by the system.
LPDDR2 deives shall allow for a 2^{o}C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.
In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation.

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2^{o}C$$

Paramter	Sysmbol	Min	Max	Unit	Note
System Temperature Gradient	TempGradient	-	Note 1	^{o}C/s	1
MR4 Read Interval	ReadInterval	-	Note 1	ms	1
Temperature Sensor Interval	tTSI	-	32	ms	
System Response Delay	SysRespDelay	-	Note 1	ms	1
MR4 Temp Margin	TempMargin	-	2	2^{o}C	

Note: 1. The values are system dependent.

For example, if TempGradient is 10^{o}C/s and the SysRespDelay is 1ms:

$$10^{o}C/s \times (ReadInterval + 32ms + 1ms) <= 2^{o}C$$

In this case, ReadInterval shall be no greater than 167ms.

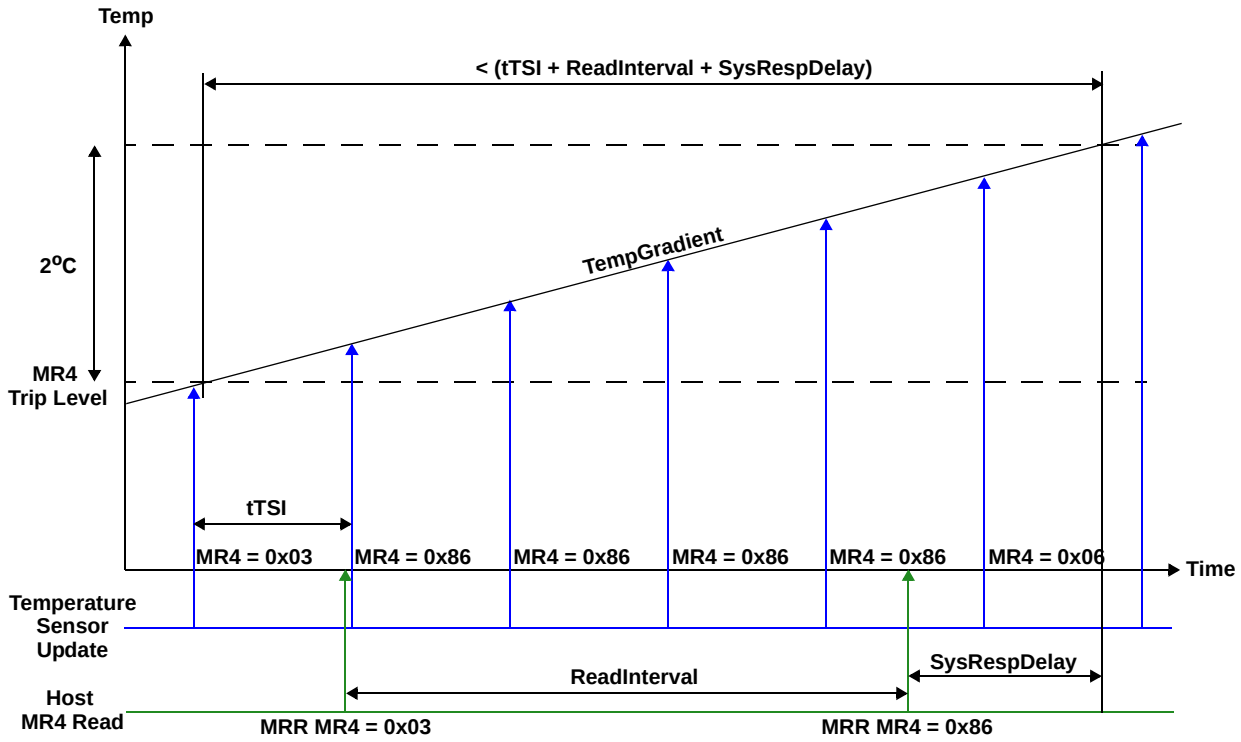


Figure. Temp Sensor Timing

DQ Calibration

LPDDR2-S4 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern A) or MR40 (Pattern B) will return the specified pattern on DQ[0] for x8 devices, DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x16 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

Table. Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit TIme 2	Bit Time 3
Pattern A (MR32)	1	0	1	0
Pattern B (MR40)	0	0	1	1

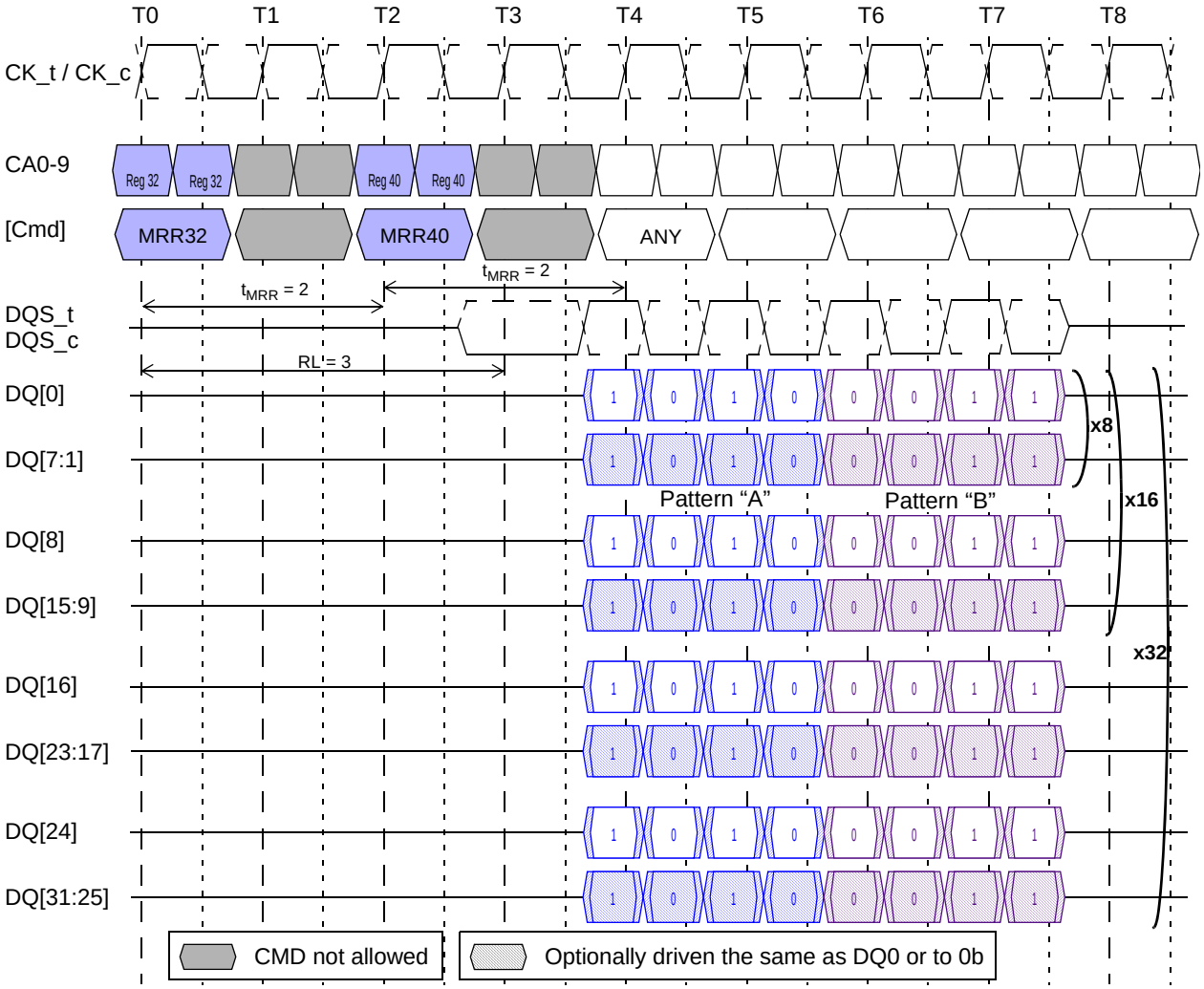


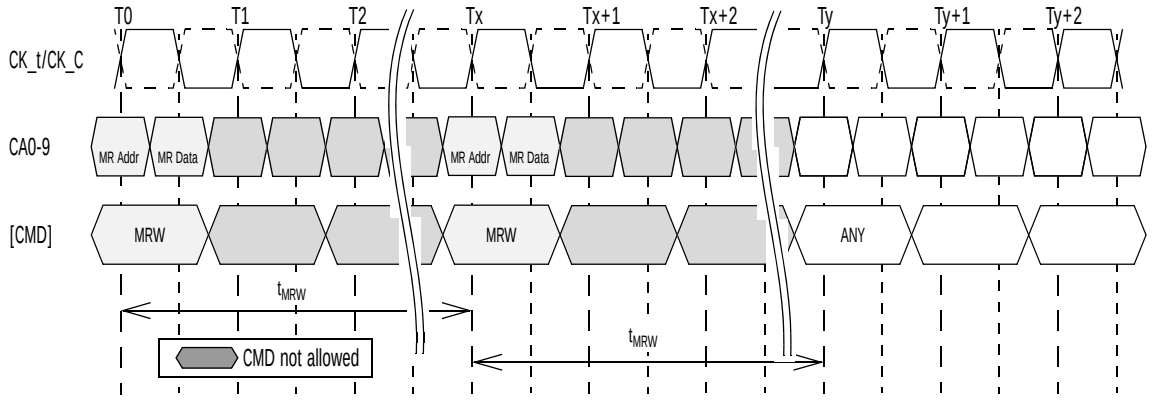
Figure. MR32 and MR40 DQ Calibration timing example: RL = 3, tMRR = 2

Note:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
4. For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
5. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.

Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

For LPDDR2 SDRAM, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.



Note:

1. The Mode Register Write Command period is tMRW. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

Figure. LPDDR2-S4: Mode Register Write timing example: RL = 3, tMRW = 5

Table: Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Initialization)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

Mode Register Write Reset (MRW Reset)

The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence. The MRW Reset command may be issued from the Idle state for LPDDR2-S4 devices. This command resets all Mode Registers to their default values. After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-S4 devices are undefined after the MRW Reset command.

Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 output drivers (RON) over process, temperature, and voltage.

There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Section TBD for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQRESET Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the `Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

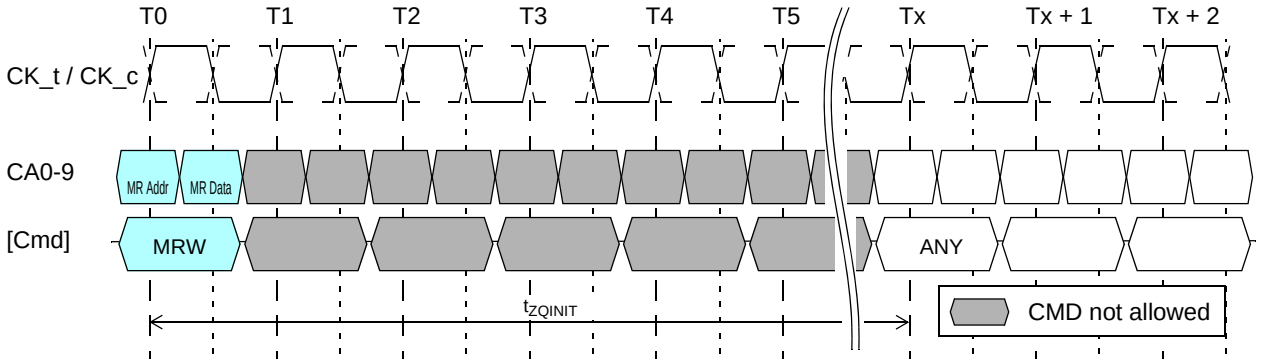
where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / °C, VSens = 0.20% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

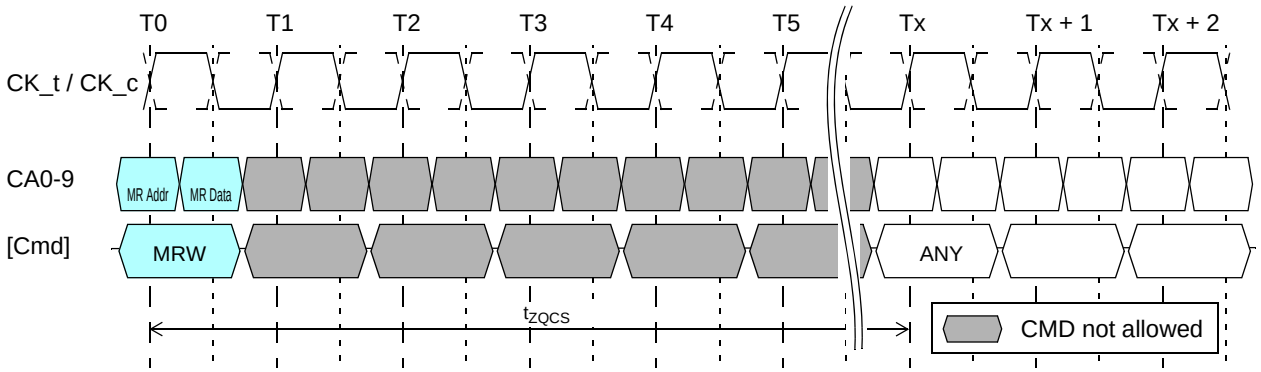
For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See "Output Driver DC Electrical Characteristics without ZQ Calibration")



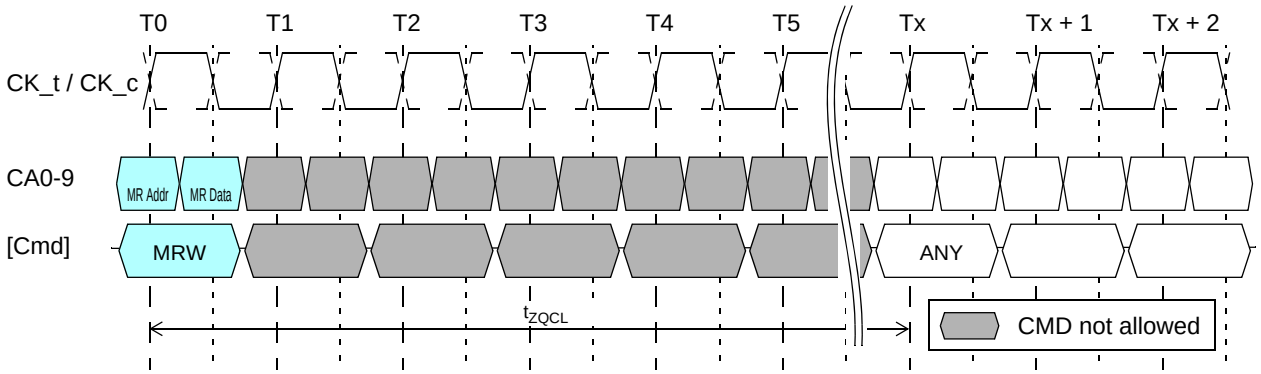
Note:
1. The ZQ Calibration Initialization period is tZQINIT. No command (other than NOP) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure. LPDDR2-S4: ZQ Calibration Initialization timing example

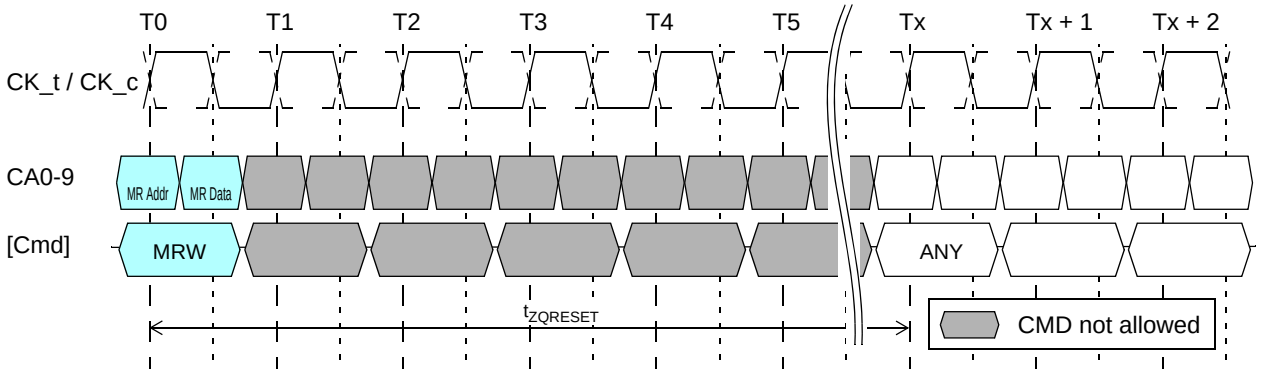


Note:
1. The ZQ Calibration Short period is tZQCS. No command (other than NOP) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure. LPDDR2-S4: ZQ Calibration Short timing example



Note:
1. The ZQ Calibration Long period is tZQCL. No command (other than NOP) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.



Note:
1. The ZQ Calibration Reset period is tZQRESET. No command (other than NOP) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure. LPDDR2-S4: ZQ Calibration Reset timing example

ZQ External Resistor Value, Tolerance and Capacitive Loading

To use the ZQ calibration functions, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See the section of Input/Output capacitance).

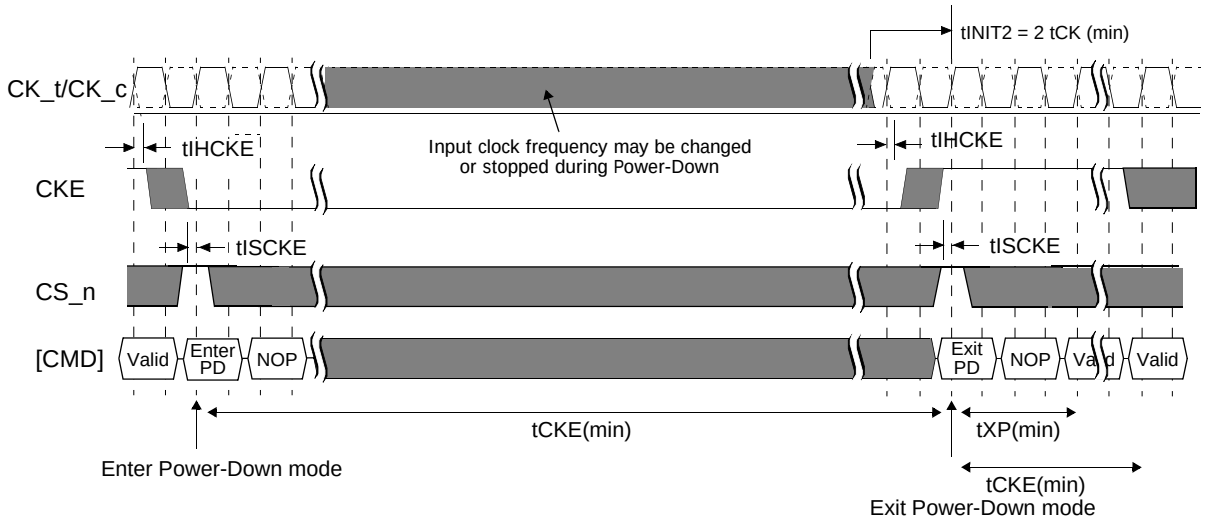
Power-down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, auto-precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.
Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until tCKE has been satisfied. VREF must be maintained at a valid level during power down.

VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges.
For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section “LPDDR2 SDRAM Refresh Requirements”, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.



Note:
1. Input clock frequency may be changed or stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure. LPDDR2-S4: Basic power down entry and exit timing diagram

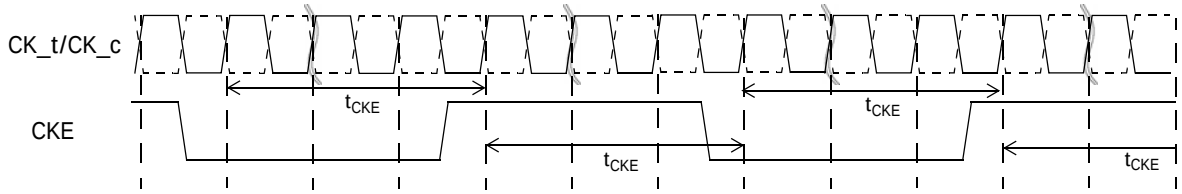
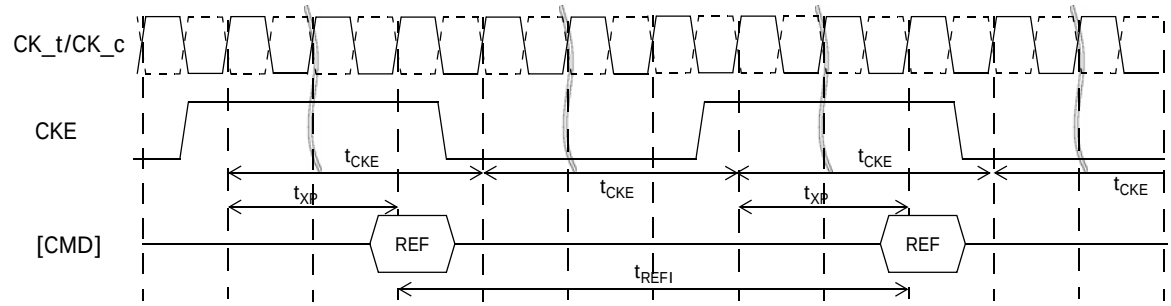
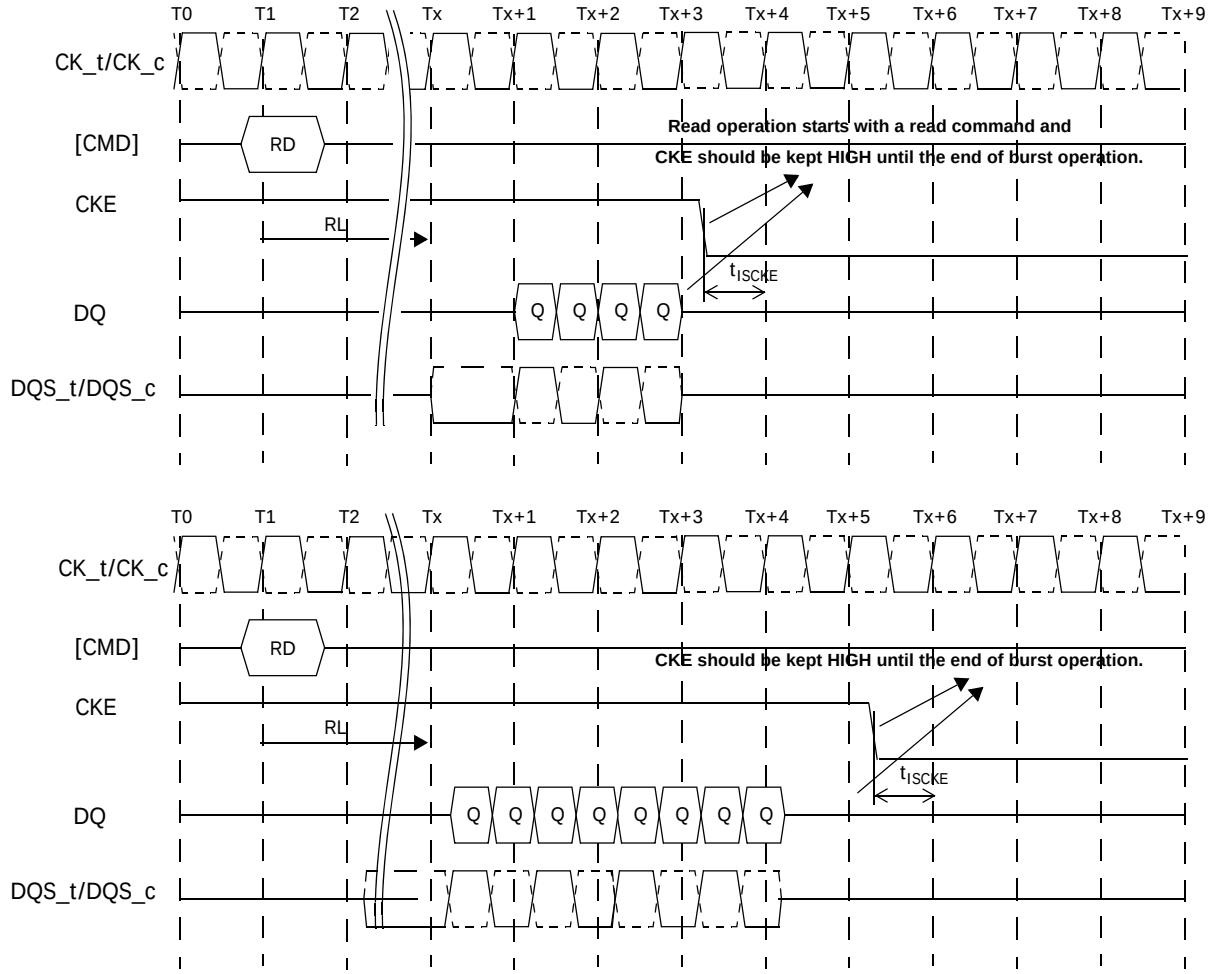


Figure. LPDDR2-S4: Example CKE intensive environment



Note:
1. The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift.

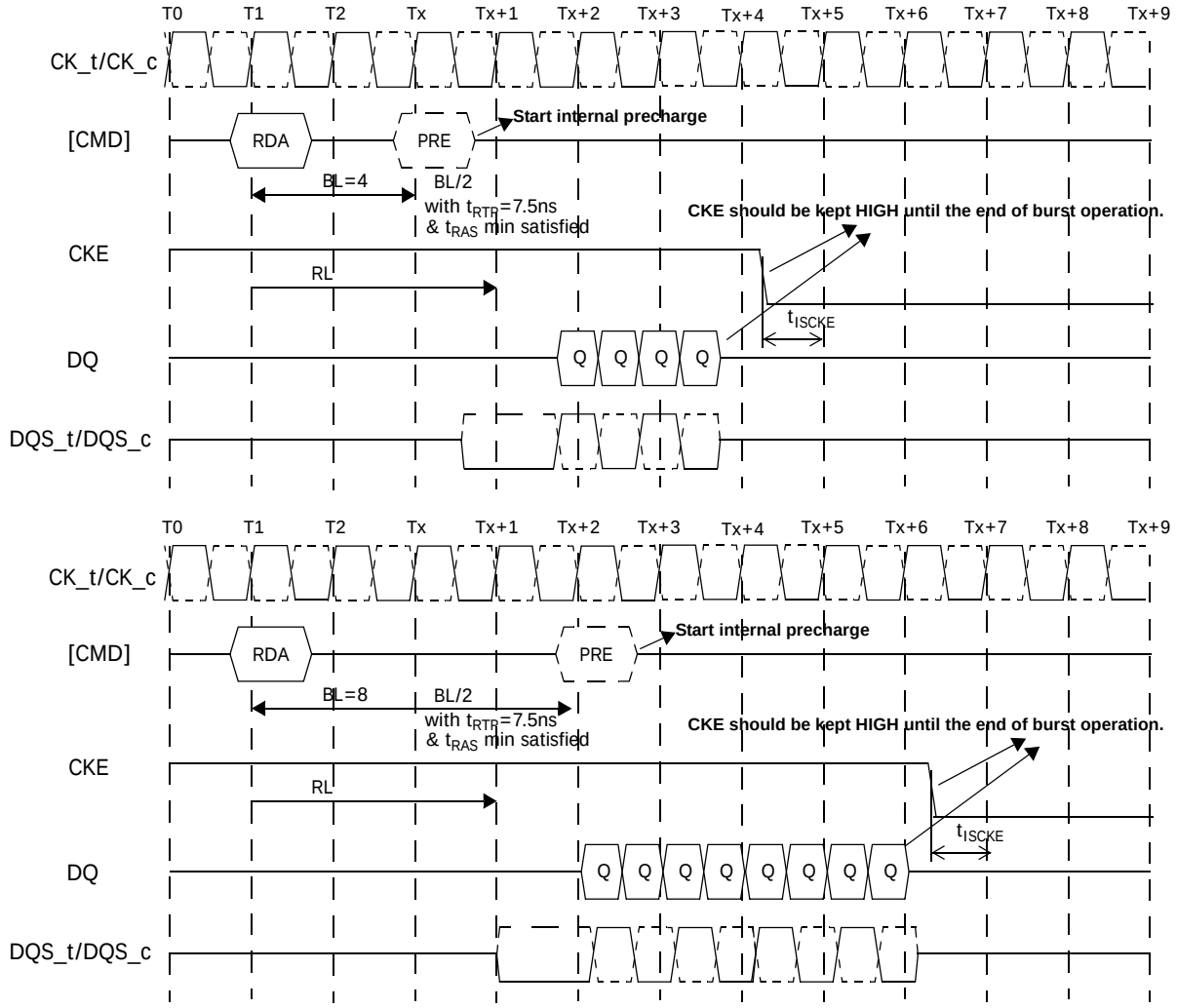
Figure. LPDDR2-S4: REF to REF timing with CKE intensive environment



Note:

1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

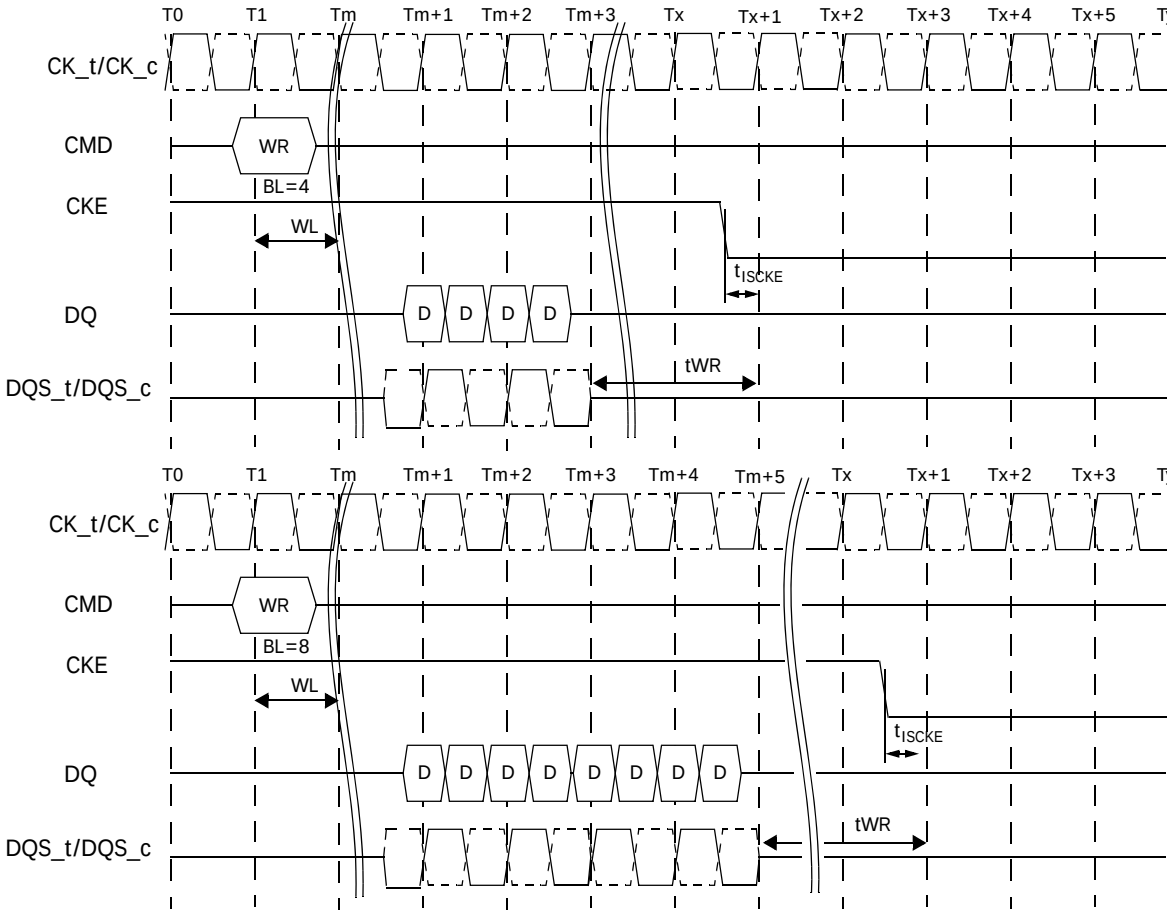
Figure. LPDDR2-S4: Read to power-down entry



Note:

1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

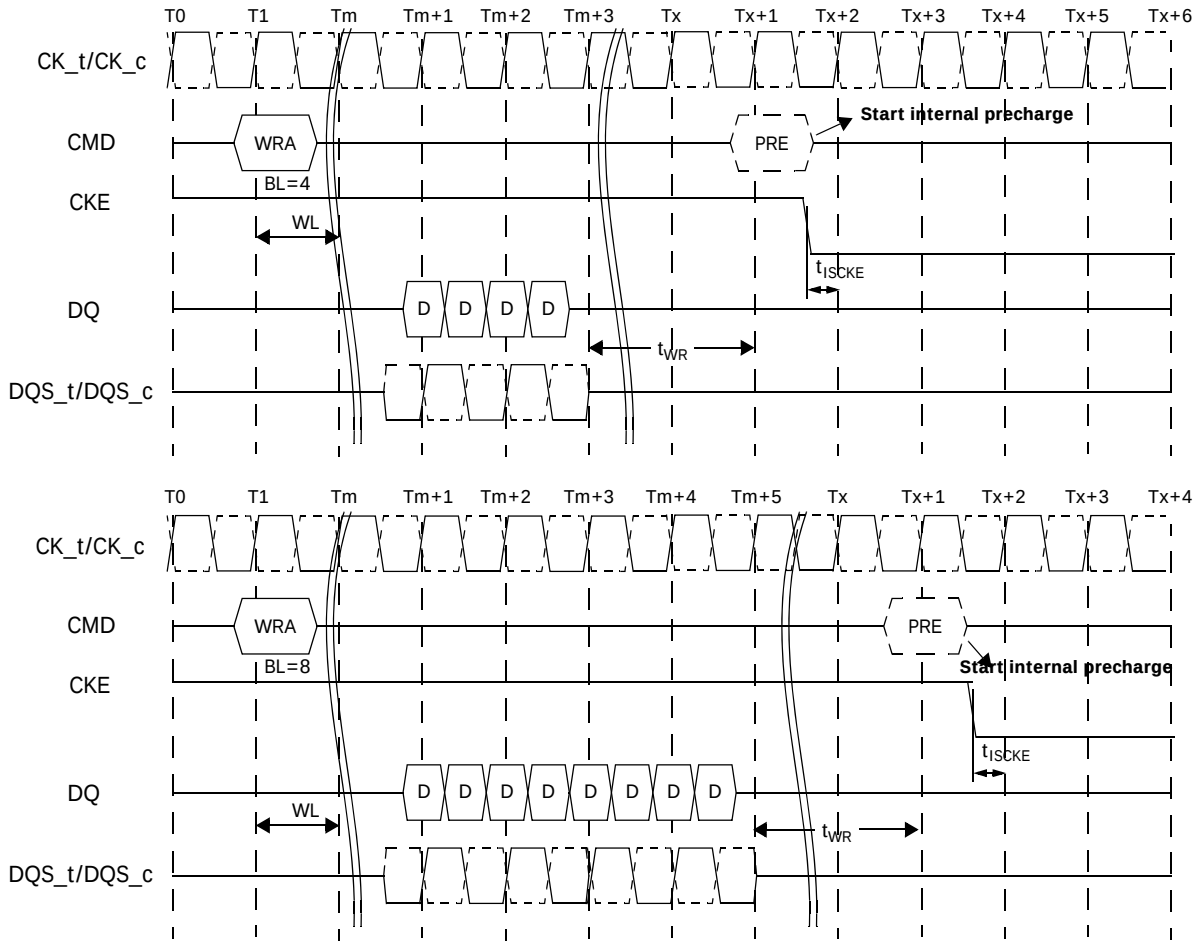
Figure. LPDDR2-S4: Read with autoprecharge to power-down entry



Note:

1. CKE may be registered LOW WL + 1 + BL/2 + RU(tWT/tCK) clock cycles after the clock on which the Write command is registered.

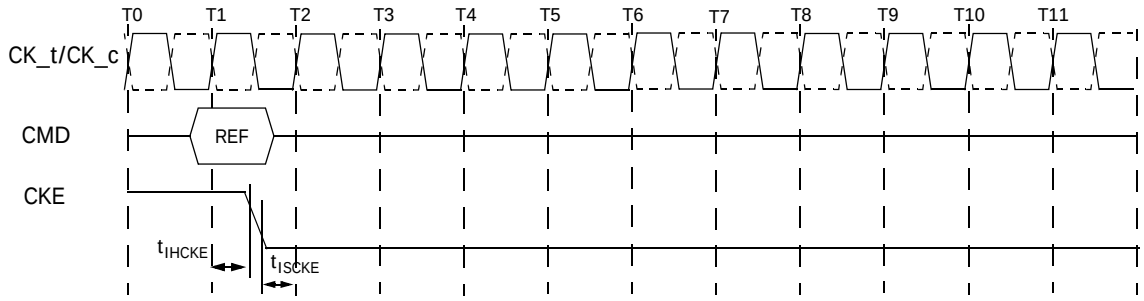
Figure. LPDDR2-S4: Write to power-down entry



Note:

1. CKE may be registered LOW WL+1+BL/2+RU(tWR/tCK)+1 clock cycles after the Write command is registered.

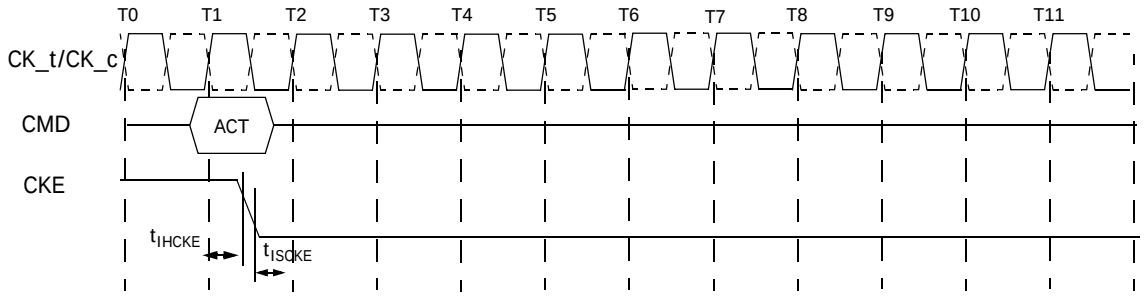
Figure. LPDDR2-S4: Write with auto precharge to power-down entry



Note.

1. CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.

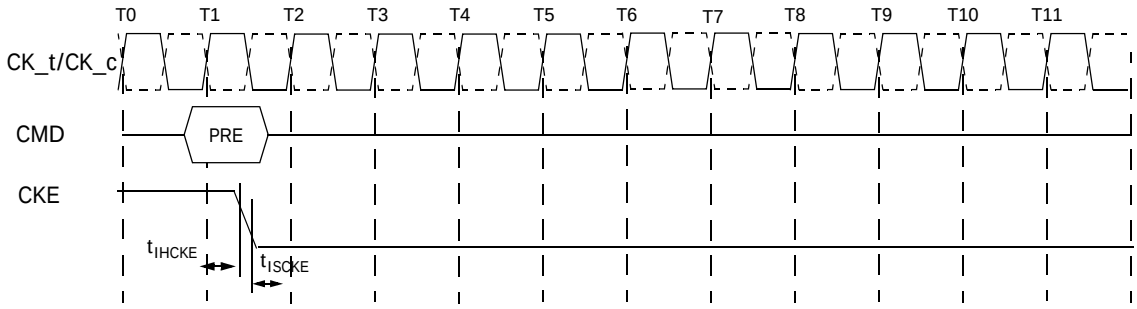
Figure. LPDDR2-S4: Refresh command to power-down entry



Note.

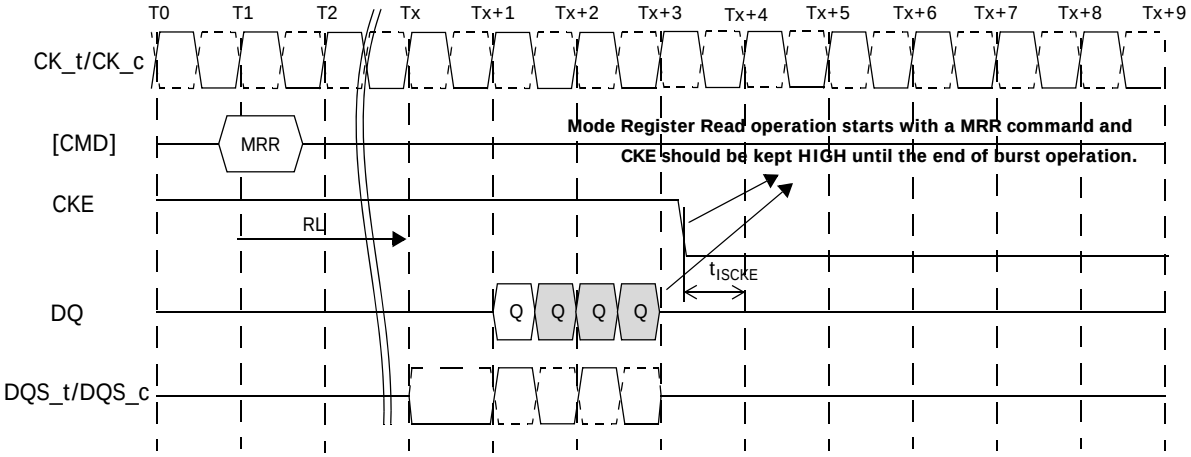
1. CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

Figure. LPDDR2-S4: Activate command to power-down entry



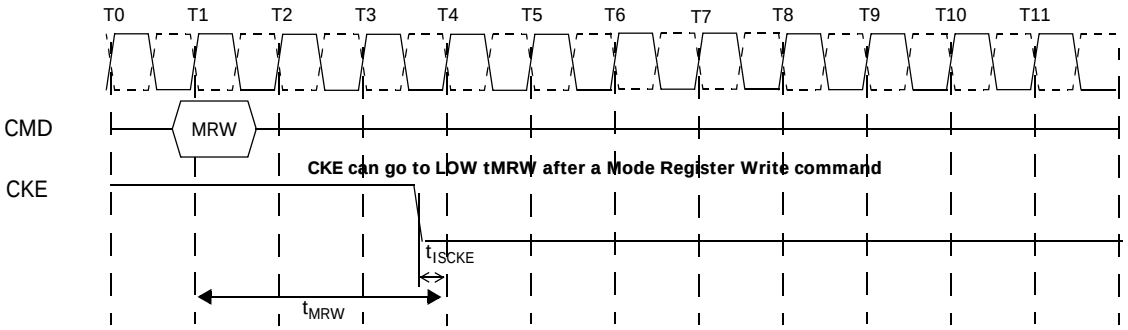
Note. 1. CKE may go LOW tIHCKE after the clock on which the Precharge/Precharge-All command is registered.

Figure. LPDDR2-S4: Precharge/Precharge-all command to power-down entry



Note. 1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ 4/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

Figure. LPDDR2-S4: Mode Register Read to power-down entry



Note. 1. CKE may be registered LOW tMRW after the clock on which the Mode Register Write command is registered.

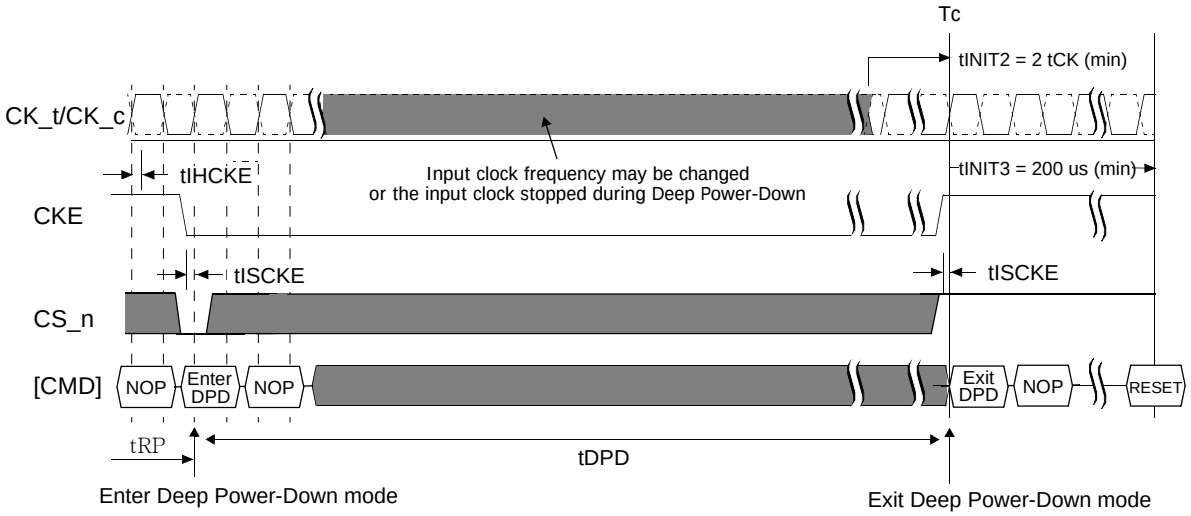
Deep Power Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW

In Deep Power Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled with the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VREFDQ may be at any level between 0 and VDDQ and VREFCA may be at any level between 0 and VDDCA during Deep Power Down, however before exiting Deep Power-Down, VREF must be within specified limits.

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.



Note:

1. Initialization sequence may start at any time after Tc.
2. tINIT3, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see "Power-up and initialization".
3. Input clock frequency may be changed or stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure. Deep power down entry and exit timing diagram

Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- tCK(MIN) and tCK(MAX) are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(MIN) and tCK(MAX) are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any ACT, RD, WR, PR, MRW or MRR commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any ACT, RD, WR, PR, MRW or MRR commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum or 2tCK + tXP.

No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.