MCP Specification

4Gb NAND Flash + 2Gb Mobile DDR

Document Title

Multi-Chip Package MEMORY

4Gb (256M x16) NAND Flash Memory / 2Gb (64M x32) Mobile DDR SDRAM

1. Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue. - 4Gb NAND Flash W-die_ Ver 0.0 - 2Gb M-DDR SDRAM B-die_Ver 1.0	May. 8, 2009	Preliminary
1.0	<NAND>_Ver 1.0 - Corrected Errata - ECC requirement updated - Final issue <DRAM>_Ver 1.2 Ver 1.1 - Corrected errata. Ver 1.2 - Finalized. <Common> - Finalized	Aug. 17, 2009	Final
1.1	<NAND>_Ver 1.01 1. ECC requirement updated	Sep. 03, 2009	Final
1.2	<NAND>_Ver 1.1 1. ECC requirement updated 2. Chapter 3.10 : Updated note for Random data input <M-DDR>_Ver 1.3	Oct. 8, 2009	Final
1.3	<Common> - Added DDR333.	Nov. 26, 2009	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

Multi-Chip Package MEMORY

4Gb (256M x16) NAND Flash Memory / 2Gb (64M x32) Mobile DDR SDRAM

2. FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 137-ball FBGA Type - 10.5 x 13 x 1.2mmt, 0.8mm pitch

<NAND Flash>
- Voltage Supply : 1.7V ~ 1.95V
- Organization
  - Memory Cell Array :
    (256M + 8M) x 16bit for 4Gb
    (512M + 16M) x 16bit for 8Gb DDP
  - Data Register : (1K + 32) x 16bit
- Automatic Program and Erase
  - Page Program : (1K + 32)Word
  - Block Erase : (64K + 2K)Word
- Page Read Operation
  - Page Size : (1K + 32)Word
  - Random Read : 40μs(Max.)
  - Serial Access : 42ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 250μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  -Endurance : 100K Program/Erase Cycles
  with 1bit/256Word ECC for x16
- Command Driven Operation
- Unique ID for Copyright Protection

<Mobile DDR>
- VDD/VDDQ = 1.8V/1.8V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- MRS cycle with address key programs
  - CAS Latency (3)
  - Burst Length (2, 4, 8, 16)
  - Burst Type (Sequential & Interleave)
- EMRS cycle with address key programs
  - Partial Array Self Refresh (Full, 1/2, 1/4 Array)
  - Output Driver Strength Control
  (Full, 1/2, 1/4, 1/8, 3/4, 3/8, 5/8, 7/8)
- Internal Temperature Compensated Self Refresh
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK).
- Data I/O transactions on both edges of data strobe, DM for masking.
- Edge aligned data output, center aligned data input.
- No DLL; CK to DQS is not synchronized.
- DM0 - DM3 for write masking only.
- Auto refresh duty cycle
  - 7.8us
- Clock stop capability

Operating Frequency

	DDR333	DDR400
Speed @CL3[1)]	166MHz	200MHz

Note:
1) CAS Latency

Address configuration

Organization	Bank	Row	Column
64Mx32	BA0,BA1	A0 - A13	A0 - A9

- DM is internally loaded to match DQ and DQS identically.

3. GENERAL DESCRIPTION

The K524G2GACB is a Multi Chip Package Memory which combines 4Gbit NAND Flash Memory an 2Gbit DDR synchronous high data rate Dynamic RAM.

NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 250μs on the (1K+32)Word page and an erase operation can be performed in typical 2ms on a (64K+2K)Word block. Data in the data register can be read out at 42ns cycle time per Word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the device's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The device is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

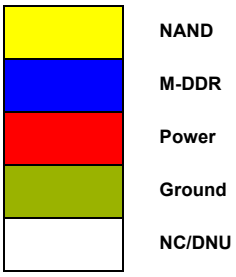
In 2Gbit Mobile DDR, Synchronous design make a device controlled precisely with the use of system clock. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The K524G2GACB is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 137-ball FBGA Type.

4. Pin CONFIGURATION

	1	2	3	4	5	6	7	8	9	10
A		DNU							DNU	DNU
B	NC	NC	/REn	CLEn	VCCn	/CEn	/WEn	VDDd	VSSd	NC
C	VSSd	A4d	/WPn	ALEn	VSSn	R/$\overline{B}$n	DQ31d	DQ30d	VDDQd	VSSQd
D	VDDd	A5d	A7d	A9d	DQ25d	DQ27d	DQ29d	DQ28d	VSSQd	VDDQd
E	A6d	A8d	CKEd	DQ18d	DQS3d	DQ22d	DM3d	DQ26d	VDDQd	VSSQd
F	A12d	A11d	NC	DQ17d	DQ19d	DQ24d	DQ23d	DM2d	VSSQd	VDDQd
G	NC	/RASd	DQ15d	DQ16d	DQS1d	DM1d	DQ9d	CKd	VDDQd	VSSQd
H	VDDd	/CASd	DQ20d	DQ21d	DQ13d	DQ12d	DQS2d	/CKd	VSSd	VDDd
J	VSSd	/CSd	BA0d	DQ14d	DQ11d	DQ10d	DQS0d	DM0d	VSSQd	VDDQd
K	/WEd	BA1d	A10d	A0d	DQ7d	DQ8d	DQ6d	DQ4d	VDDQd	VSSQd
L	A1d	A2d	A3d	DQ0d	DQ1d	DQ2d	DQ3d	DQ5d	VDDQd	VSSQd
M	VDDd	VSSd	A13d	NC	IO3n	IO5n	IO14n	IO7n	VSSQd	VDDQd
N	IO0n	IO1n	IO2n	IO10n	VCCn	IO6n	IO13n	IO15n	VDDQd	VSSQd
P	NC	IO8n	IO9n	IO11n	IO12n	VSSn	IO4n	VDDd	VSSd	NC
R	DNU	DNU							DNU	DNU

137 FBGA: Top View (Ball Down)



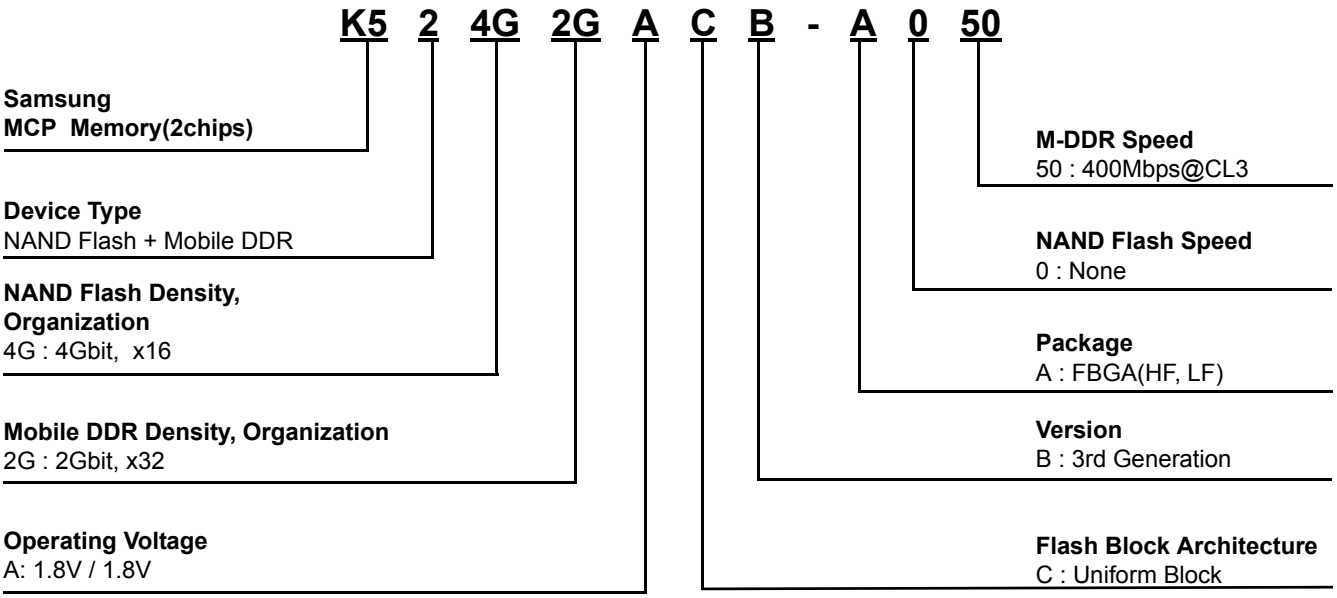
5. PIN DESCRIPTION

Pin Name	Pin Function(M-DDR)
CKd,/CKd	System Clock & Differential Clock
CKEd	Clock Enable
/CSd	Chip Selection
/RASd	Row Address Strobe
/CASd	Column Address Strobe
/WEd	Write Enable
A0d ~ A13d	Address Input
BA0d ~ BA1d	Bank Address Input
DM0d ~ DM3d	Input Data Mask
DQS0d~DQS3d	Data Input / Output
DQ0d ~ DQ31d	Data Input / Output
VDDd	Power Supply
VDDQd	Data Out Power
VSSd	Ground
VSSQd	DQ Ground

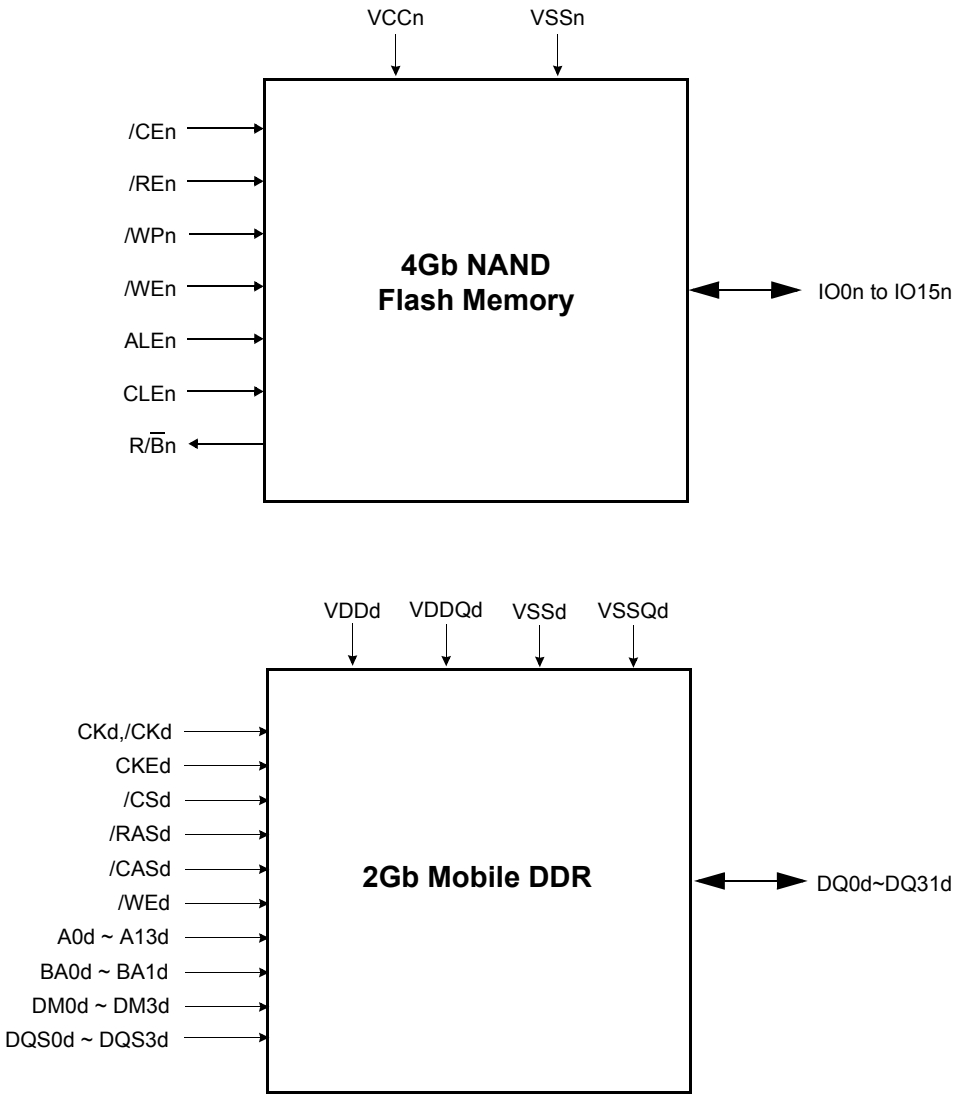
Pin Name	Pin Function(NAND Flash)
/CEn	Chip Enable
/REn	Read Enable
/WPn	Write Protection
/WEn	Write Enable
ALEn	Address Latch Enable
CLEn	Command Latch Enable
R/$\overline{B}$n	Ready/Busy Output
IO0n ~ IO15n	Data Input/Output
VCCn	Power Supply
VSSn	Ground

Pin Name	Pin Function
NC	No Connection
DNU	Do Not Use

6. ORDERING INFORMATION

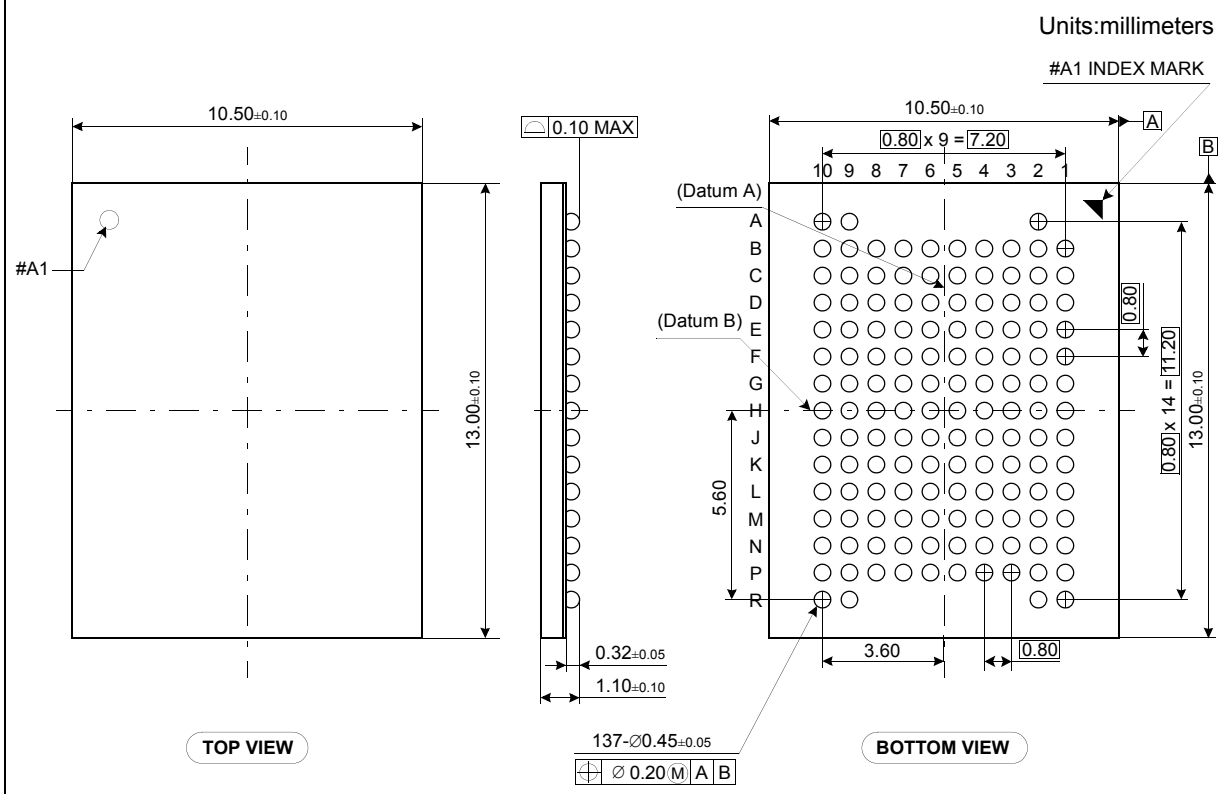


7. FUNCTIONAL BLOCK DIAGRAM



8. PACKAGE DIMENSION

137-Ball Fine pitch Ball Grid Array Package (measured in millimeters)



4Gb (256M x16) NAND Flash W-die

Figure 1. Functional Block Diagram(x8)

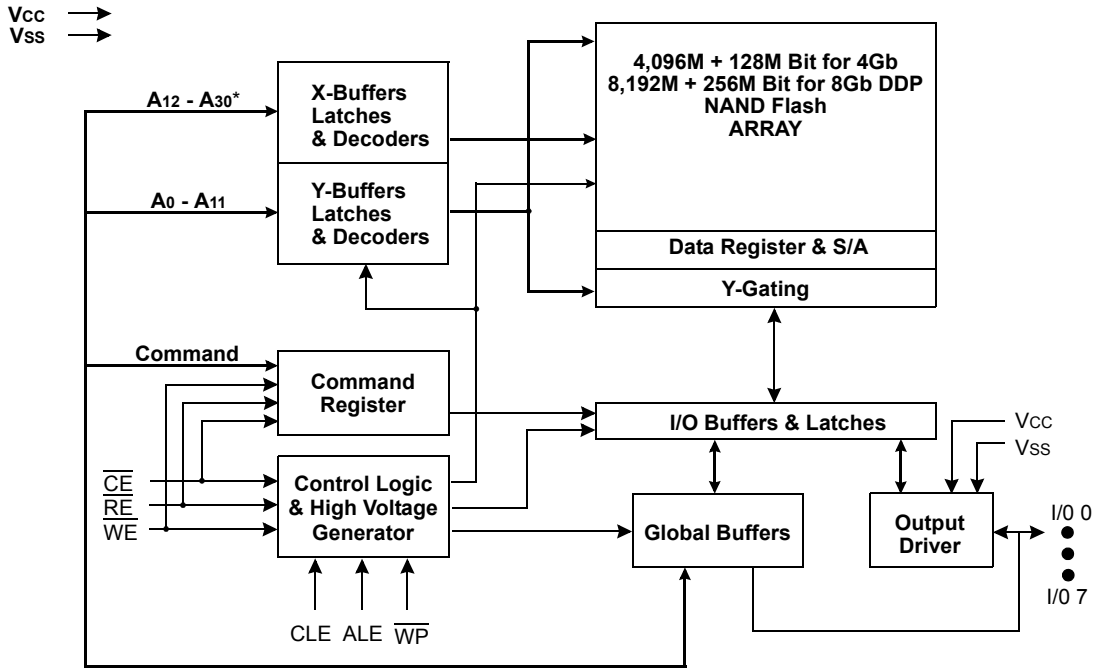


Figure 2. Array Organization(x8)

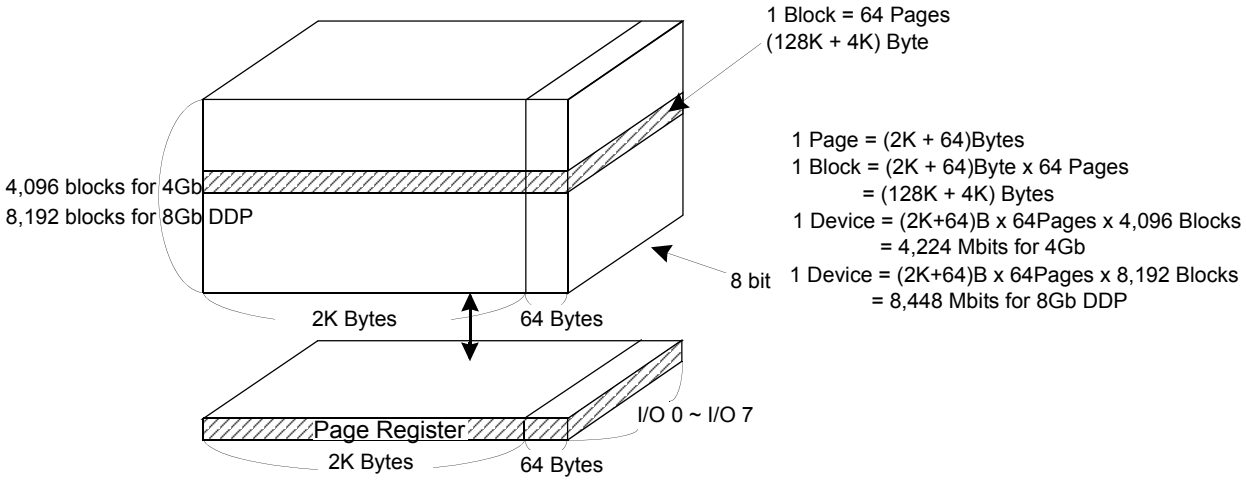


Table 1. Array address : (x8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	Row Address
5th Cycle	A28	A29	*A30	*L	*L	*L	*L	*L	Row Address

NOTE :

Column Address : Starting Address of the Register.

* L must be set to "Low".
* The device ignores any additional input of address cycles than required.
* A30 is Row address for 8G DDP.
In case of 4G Mono, A30 must be set to "Low"

Figure 3. Functional Block Diagram(x16)

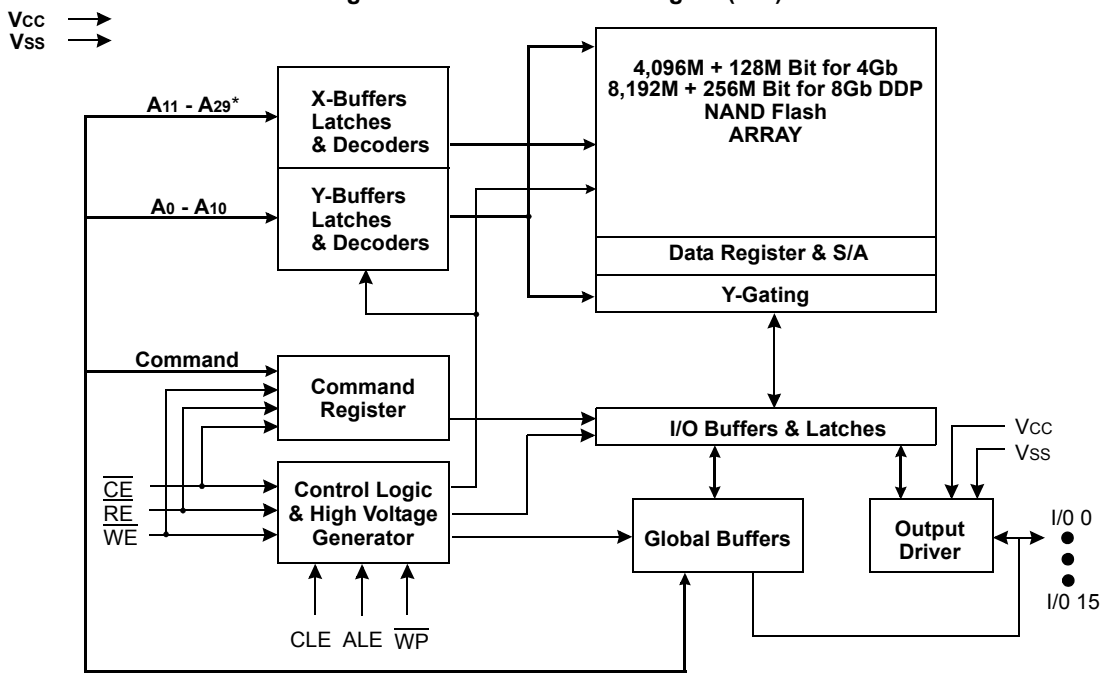


Figure 4. Figure 2-2. Array Organization(x16)

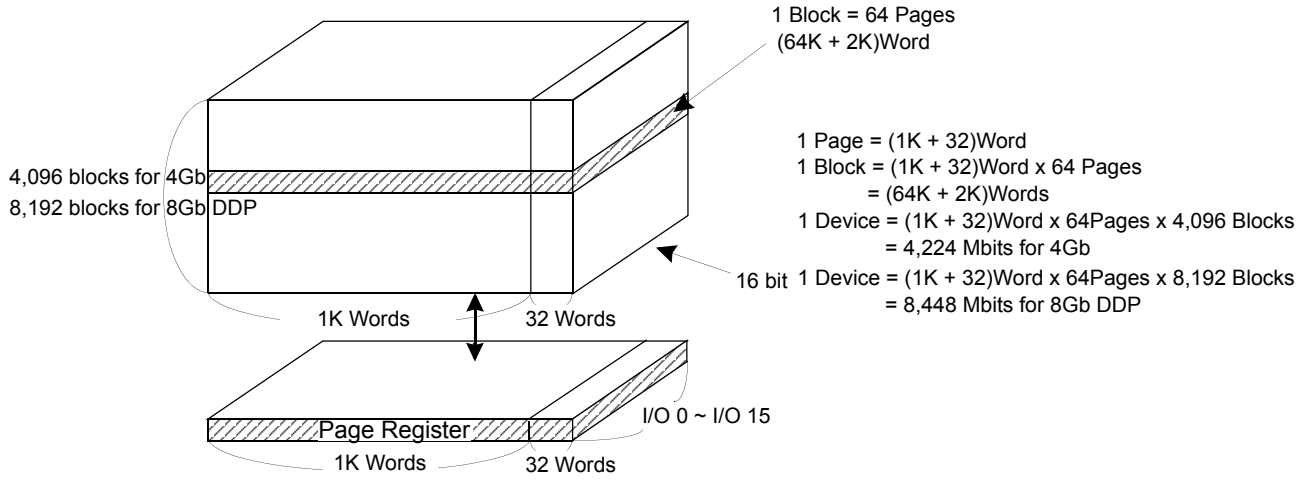


Table 2. Array address : (x16)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O 8~I/O 15	Address
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	*L	Column Address
2nd Cycle	A8	A9	A10	*L	*L	*L	*L	*L	*L	Column Address
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	*L	Row Address
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	*L	Row Address
5th Cycle	A27	A28	*A29	*L	*L	*L	*L	*L	*L	Row Address

NOTE :

Column Address : Starting Address of the Register.

* L must be set to "Low".
* The device ignores any additional input of address cycles than required.
* A29 is Row address for 8G DDP.
In case of 4G Mono, A29 must be set to "Low"

1.0 Product Introduction

NAND Flash Memory has addresses multiplexed into 8 I/Os(x16 device case : lower 8 I/Os). This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 3 defines the specific commands of the KF94GxxQ2W/KF88GxxQ2W.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 3. Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read ID	90h	-	
Read for Copy Back	00h	35h	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Status	70h	-	O

NOTE :

1) Random Data Input/Output can be executed in a page.

Caution :

Any undefined command inputs are prohibited except for above command set of Table 3.

1.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	V_{CC}	-0.6 to + 2.45	V
	V_{IN}	-0.6 to + 2.45	
	$V_{I/O}$	-0.6 to Vcc + 0.3 (< 2.45V)	
Temperature Under Bias	T_{BIAS}	-30 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	I_{OS}	5	mA

NOTE :
1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1.2 RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

1.3 DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	tRC=42ns $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	25	mA
	Program	I_{CC2}	-	-			
	Erase	I_{CC3}	-	-			
Stand-by Current(TTL)		I_{SB1}	4Gb,$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
			8Gb DDP,$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	2	
Stand-by Current(CMOS)		I_{SB2}	4Gb,$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
			8Gb DDP, $\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	20	100	
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Input High Voltage		V_{IH}(1)	-	0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}(1)	-	-0.3	-	0.2xVcc	
Output High Voltage Level		V_{OH}	I_{OH}=-100µA	Vcc-0.1	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=100uA	-	-	0.1	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.1V	3	4	-	mA

NOTE :
1) V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.
2) Typical value is measured at Vcc=1.8V, T_A=25°C. Not 100% tested.

1.4 VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
4Gb	N_{VB}	4,016	-	4,096	Blocks
8Gb DDP	N_{VB}	8.032	-	8,192	Blocks

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with x8 : 1bit/ 512Byte, x16 : 1bit/ 256Word ECC.
3) Each mono chip in th KF88GxxQ2W has maximum 40 invalid blocks.

1.5 AC TEST CONDITION

(TA=-25 to 85°C, Vcc=1.7V~1.95V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=30pF

1.6 CAPACITANCE (TA=25°C, VCC=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance (Mono)	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance (Mono)	C_{IN}	V_{IN}=0V	-	10	pF
Input/Output Capacitance (DDP)	$C_{I/O}$	V_{IL}=0V	-	20	pF
Input Capacitance (DDP)	C_{IN}	V_{IN}=0V	-	20	pF

NOTE :
Capacitance is periodically sampled and not 100% tested.

1.7 MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⌐¬	H	X	Read Mode	Command Input
L	H	L	⌐¬	H	X		Address Input(5clock)
H	L	L	⌐¬	H	H	Write Mode	Command Input
L	H	L	⌐¬	H	H		Address Input(5clock)
L	L	L	⌐¬	H	H	Data Input	
L	L	L	H	¬⌐	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

1.8 Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	250	750	μs
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	t_{BERS}	-	2	10	ms

NOTE :
1) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V Vcc and 25°C temperature.

1.9 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}(1)	21	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
$\overline{CE}$ Setup Time	t_{CS}(1)	21	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	21	-	ns
ALE Setup Time	t_{ALS}(1)	21	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}(1)	20	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	40	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	-	ns
Address to Data Loading Time	t_{ADL}(2)	100	-	ns

NOTE :
1) The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low
2) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle

1.10 AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	40	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	21	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
$\overline{WP}$ Low to $\overline{WE}$ Low (disable mode)	t_{WW}	100	-	ns
$\overline{WP}$ High to $\overline{WE}$ Low (enable mode)				
Read Cycle Time	t_{RC}	42	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{CE}$ Access Time	t_{CEA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	0	-	ns
$\overline{RE}$ High to Output Hold	t_{ROH}	15	-	ns
$\overline{CE}$ High to Output Hold	t_{COH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	10	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

2.0 NAND Flash Technical Notes

2.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with x8:1bit/ 512Byte, x16:1bit/256Word ECC.

2.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte(1st word) in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048(x16:1024). Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 5). Any intentional erasure of the original initial invalid block information is prohibited.

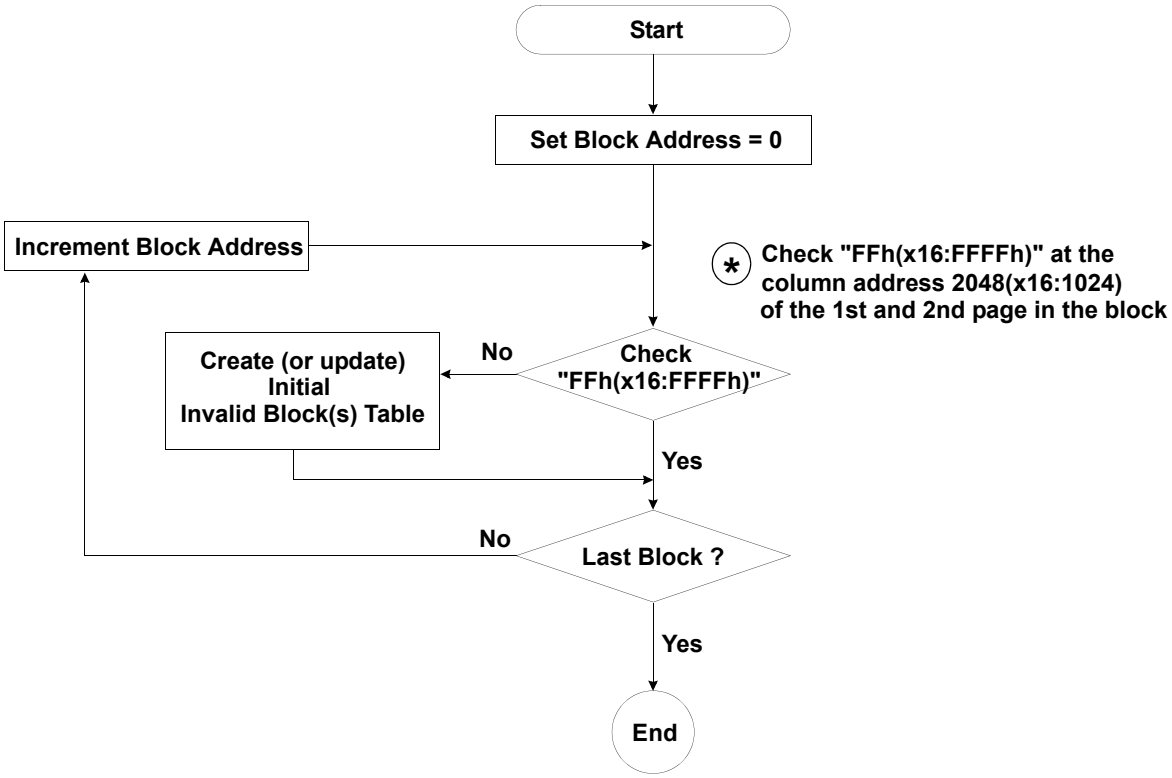


Figure 5. Flow chart to create initial invalid block table

NAND Flash Technical Notes *(Continued)*

2.3 Error in write or read operation

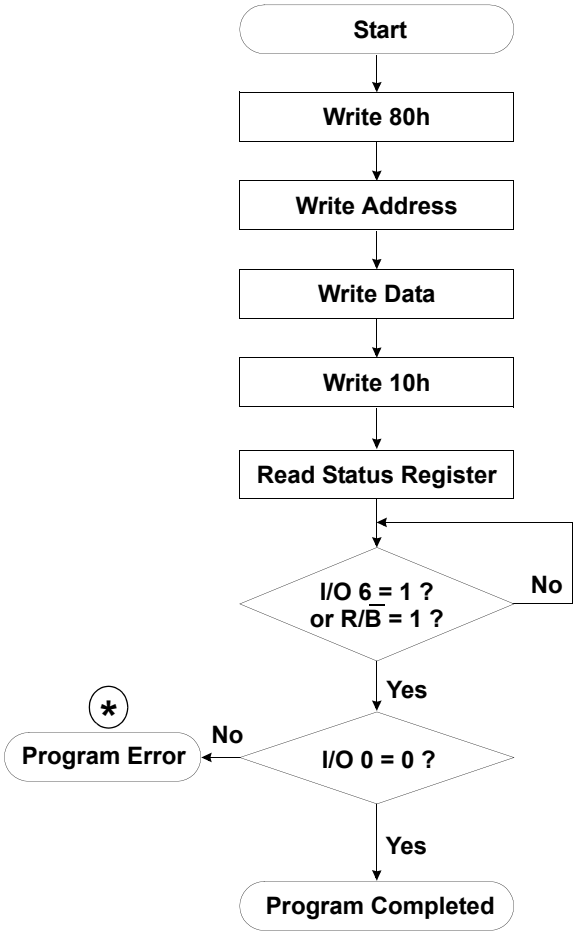
Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to 1 Bit-Failure	Verity ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming code
Example) 1bit correction & 512-byte

Note) A repetitive page read operation on the same block without erase may cause bit errors, which could be accumulated over time and exceed the coverage of ECC. Software scheme such as caching into RAM is recommended.

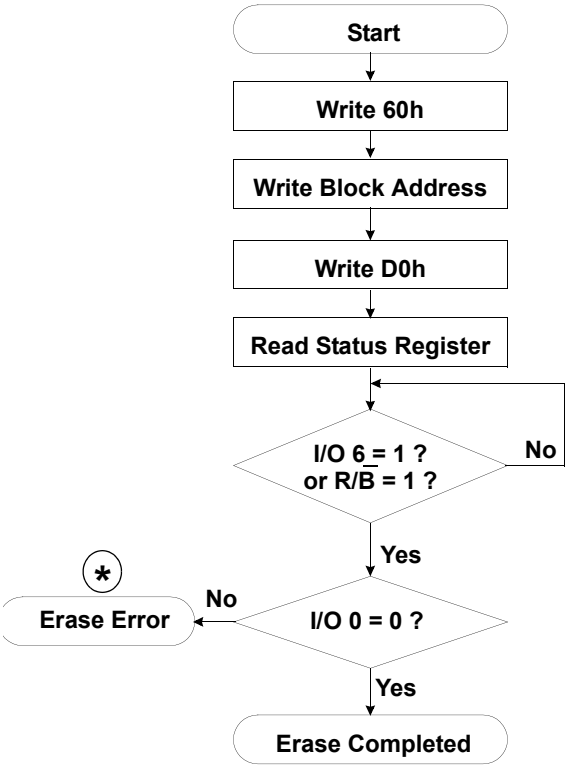
Program Flow Chart



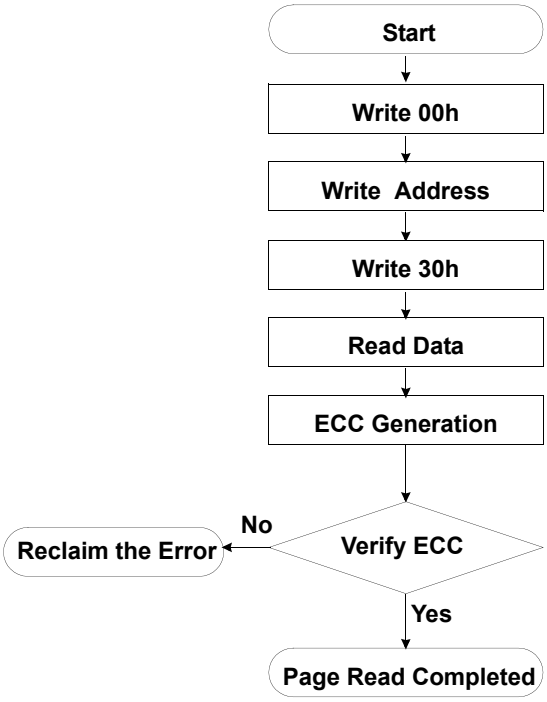
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

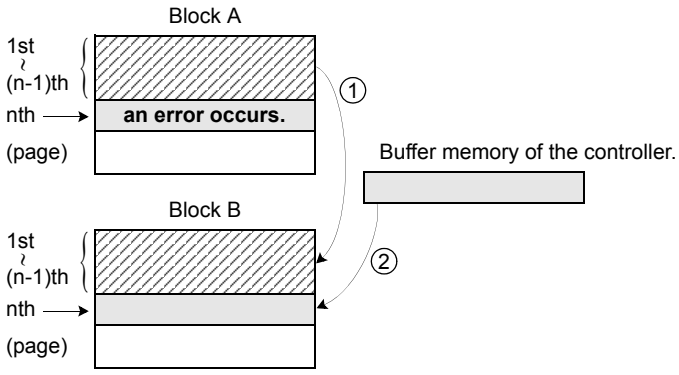


Read Flow Chart



(*) : **If erase operation results in an error, map out the failing block and replace it with another block.**

Block Replacement

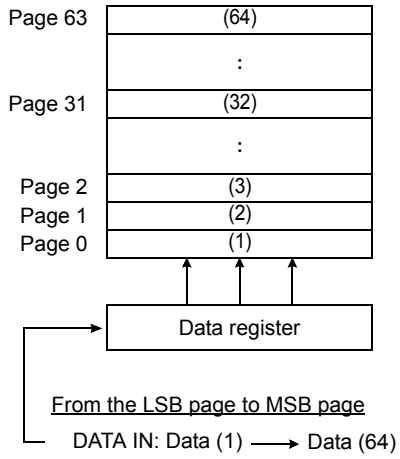


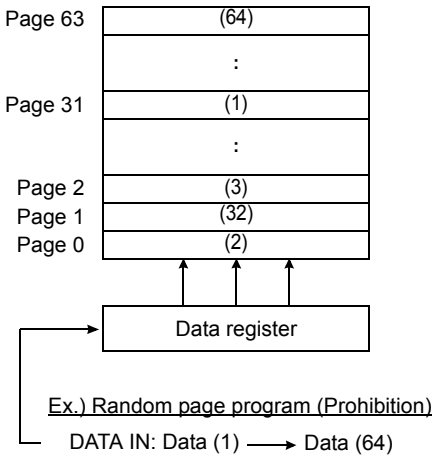
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

NAND Flash Technical Notes *(Continued)*

2.4 Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.





2.5 System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2,112byte(1,056Word) data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 6. Program Operation with $\overline{CE}$ don't-care.

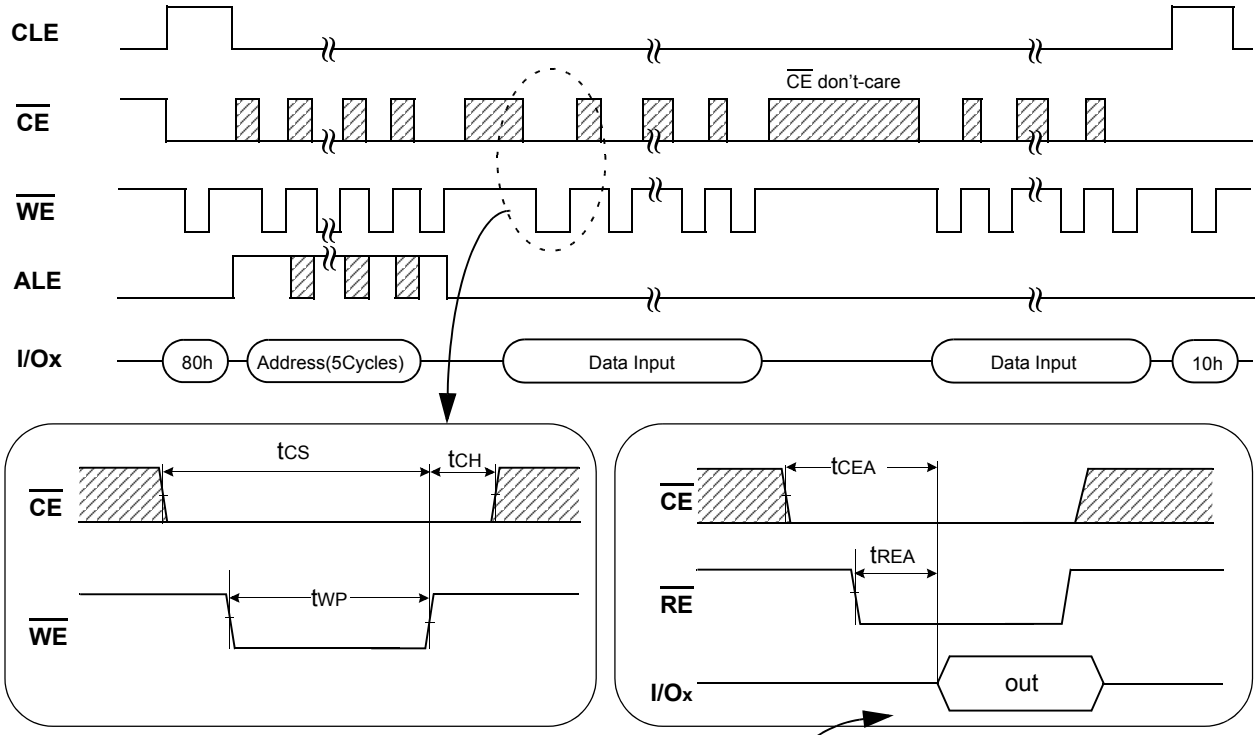
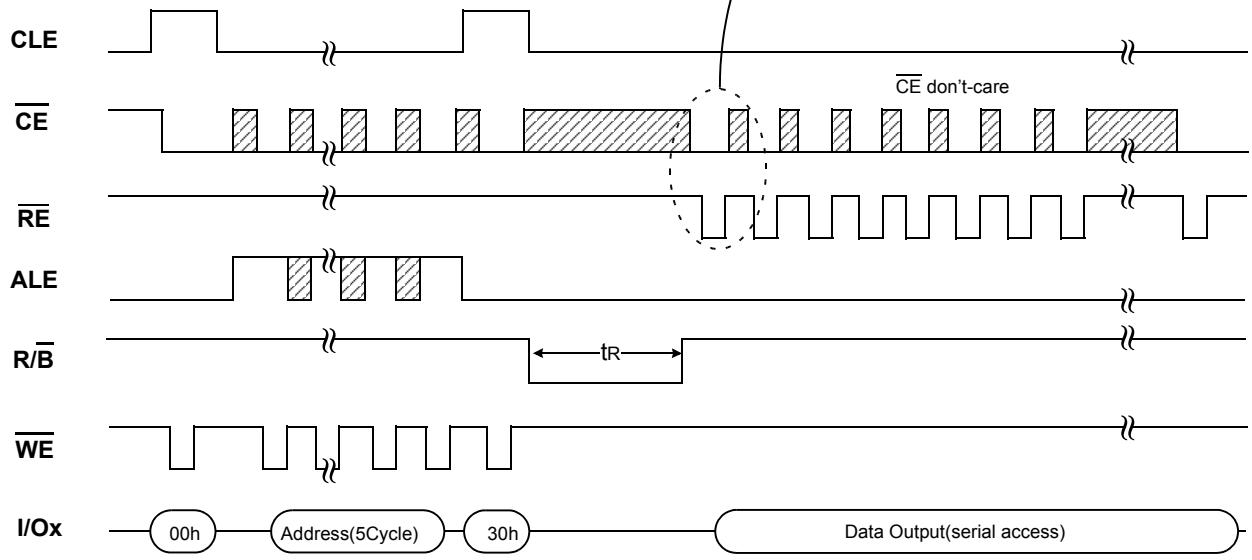


Figure 7. Read Operation with $\overline{CE}$ don't-care.

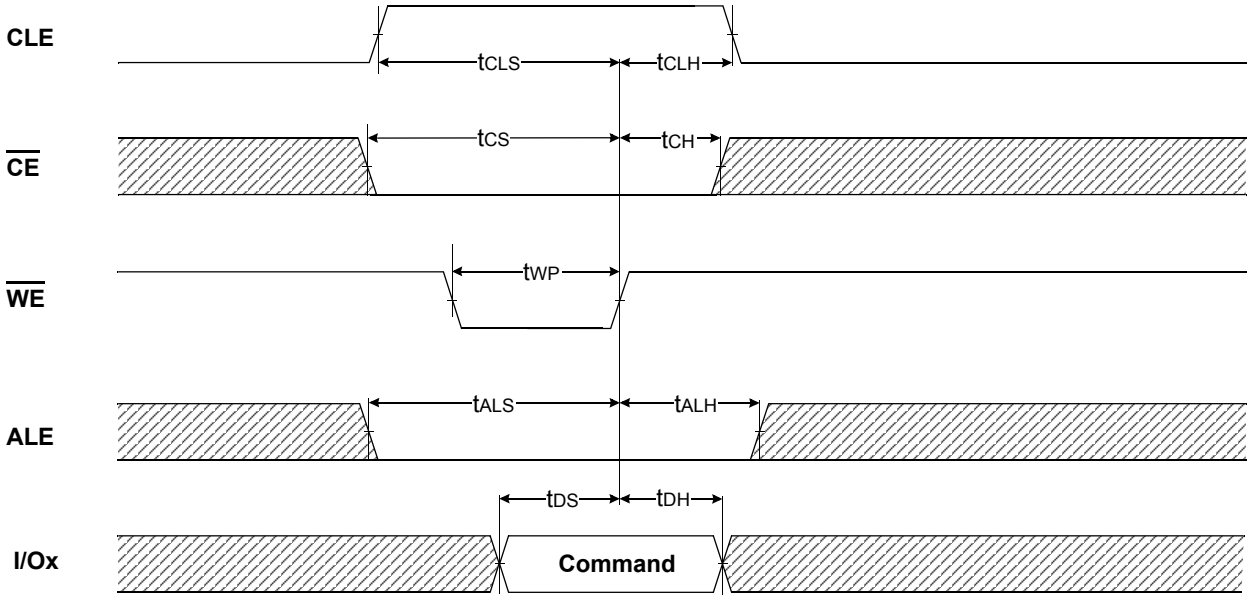


NOTE :

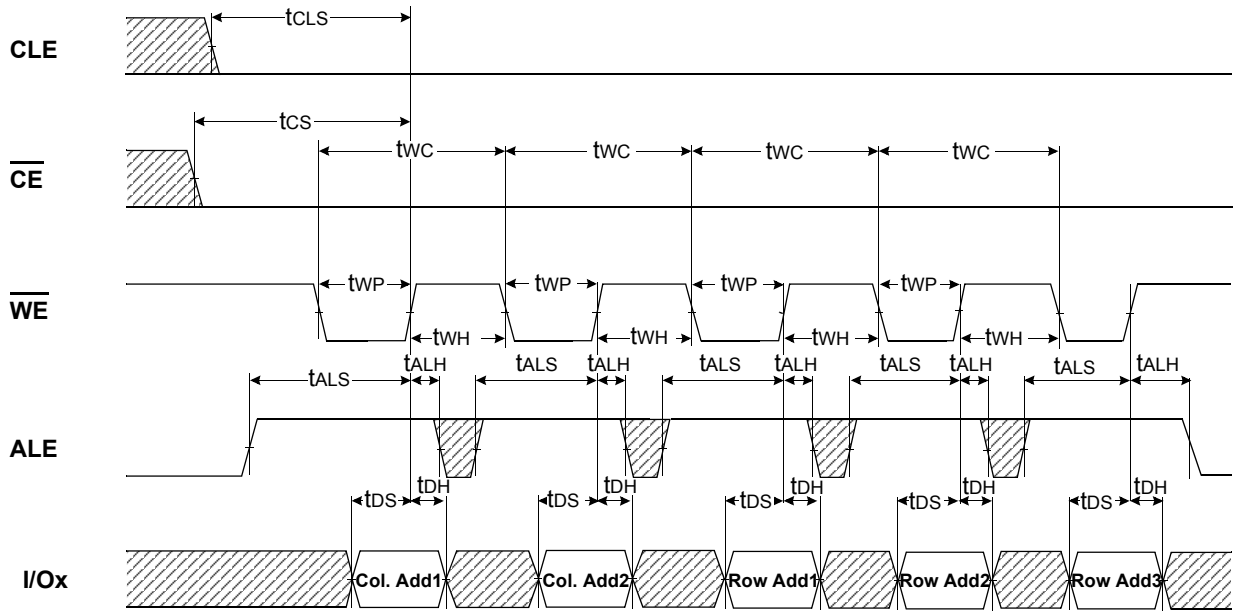
Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
4Gb(x8)	I/O 0 ~ I/O 7	~2,112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A29
8Gb DDP(x8)	I/O 0 ~ I/O 7	~2,112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A30
4Gb(x16)	I/O 0 ~ I/O 15	~1,056Word	A0~A7	A8~A10	A11~A18	A19~A26	A27~A28
8Gb DDP(x16)	I/O 0 ~ I/O 15	~1,056Word	A0~A7	A8~A10	A11~A18	A19~A26	A27~A29

3.0 TIMING DIAGRAMS

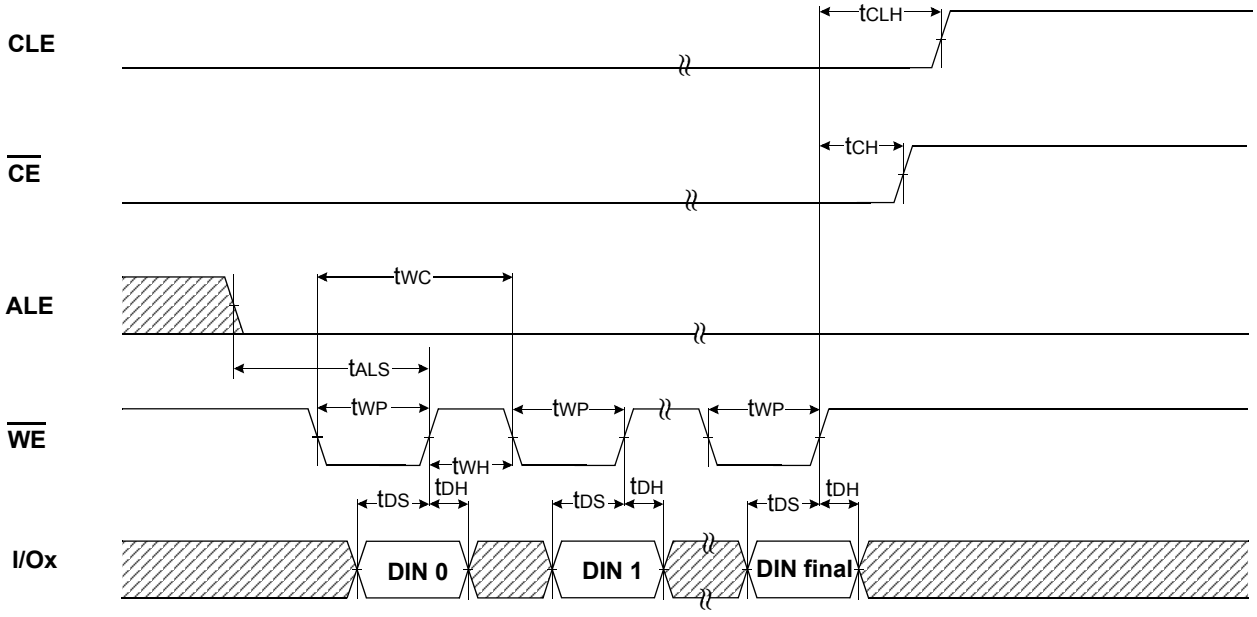
3.1 Command Latch Cycle



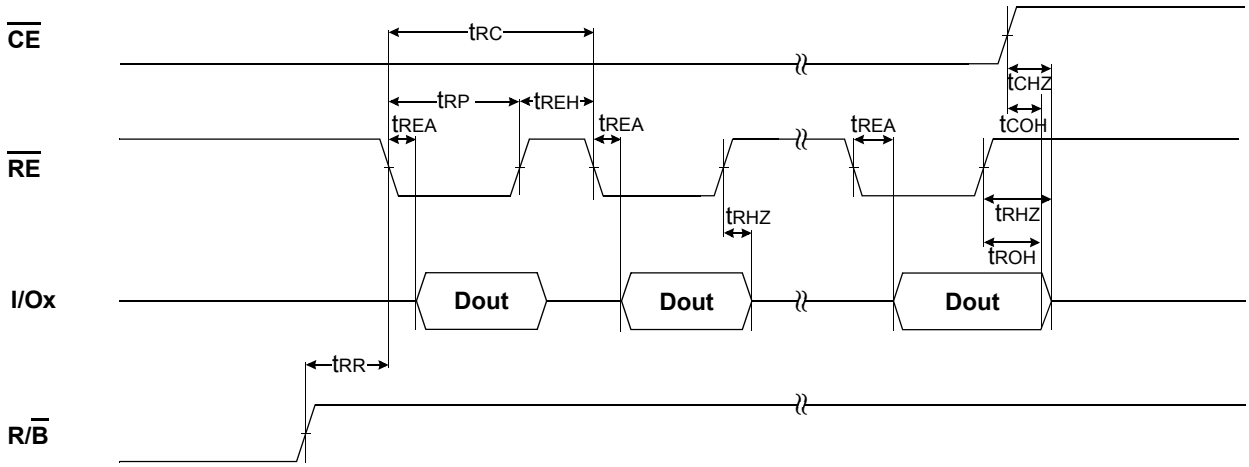
3.2 Address Latch Cycle



3.3 Input Data Latch Cycle

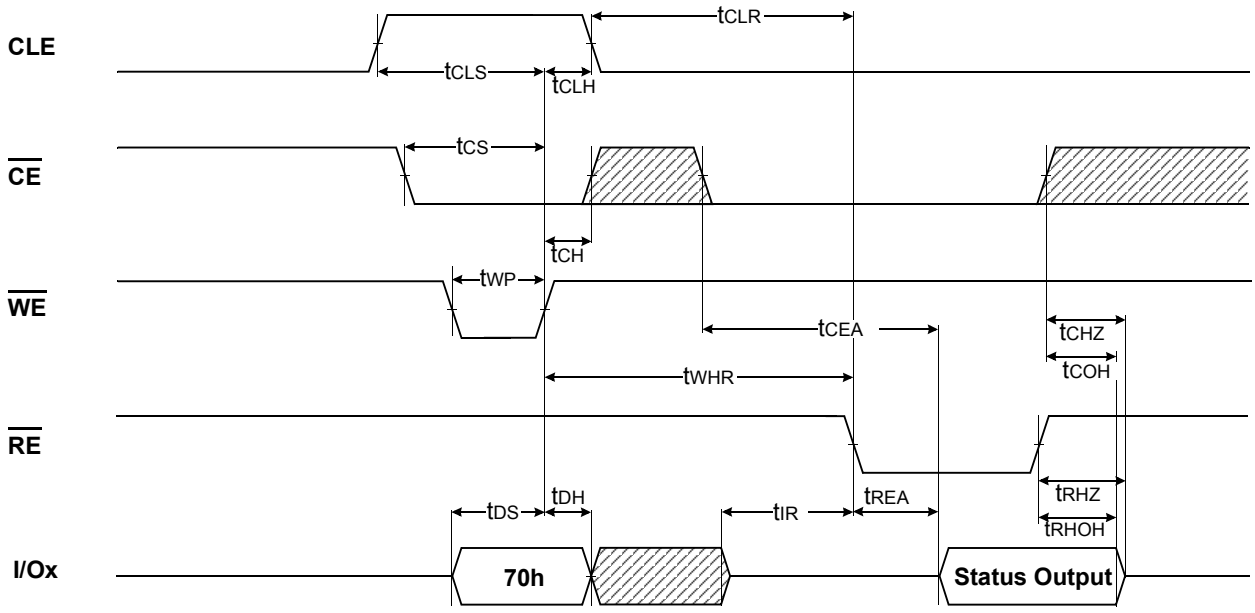


3.4 * Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

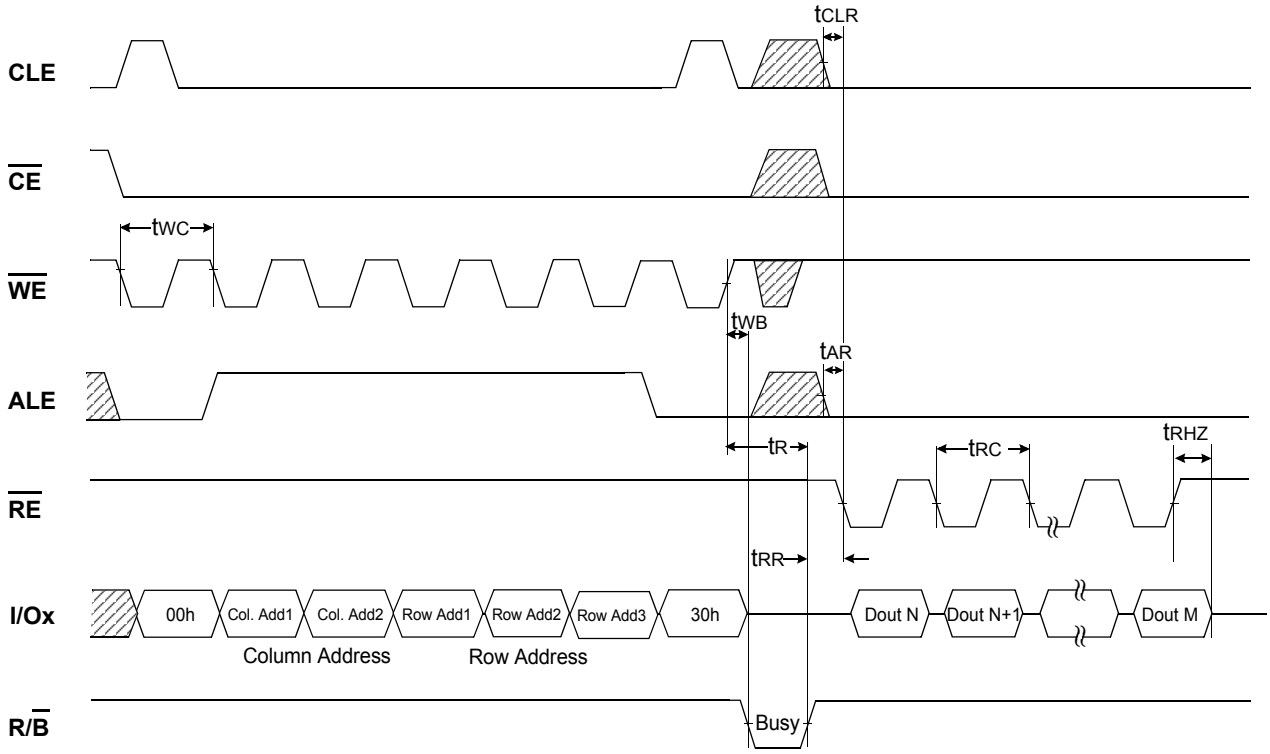


NOTE :
Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

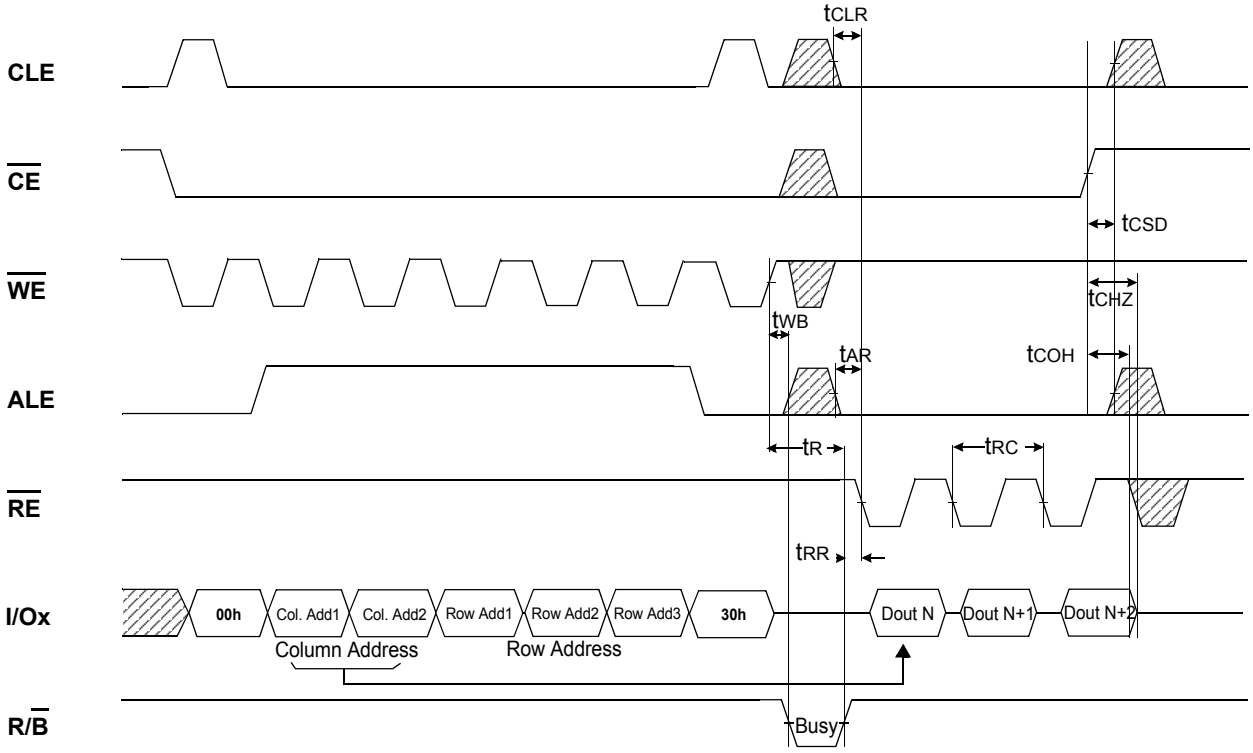
3.5 Status Read Cycle



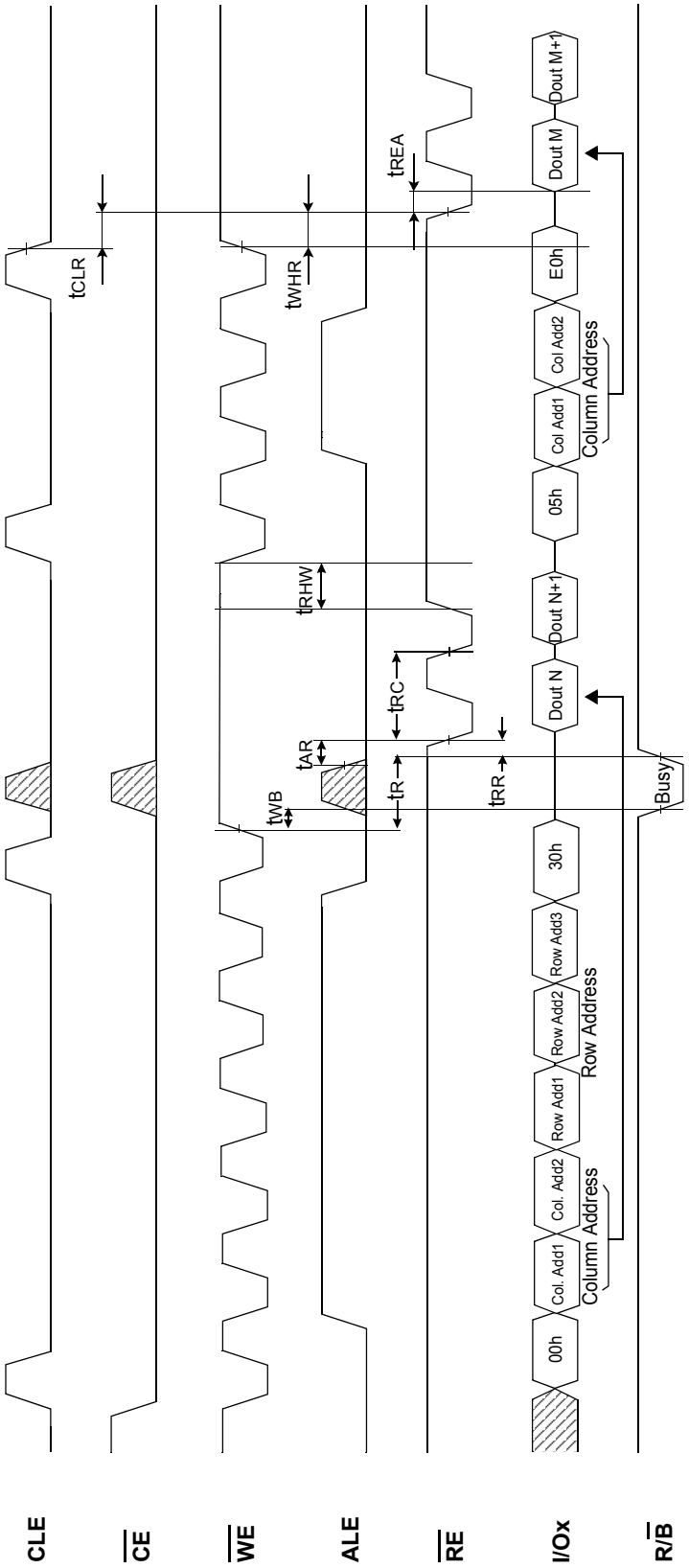
3.6 Read Operation



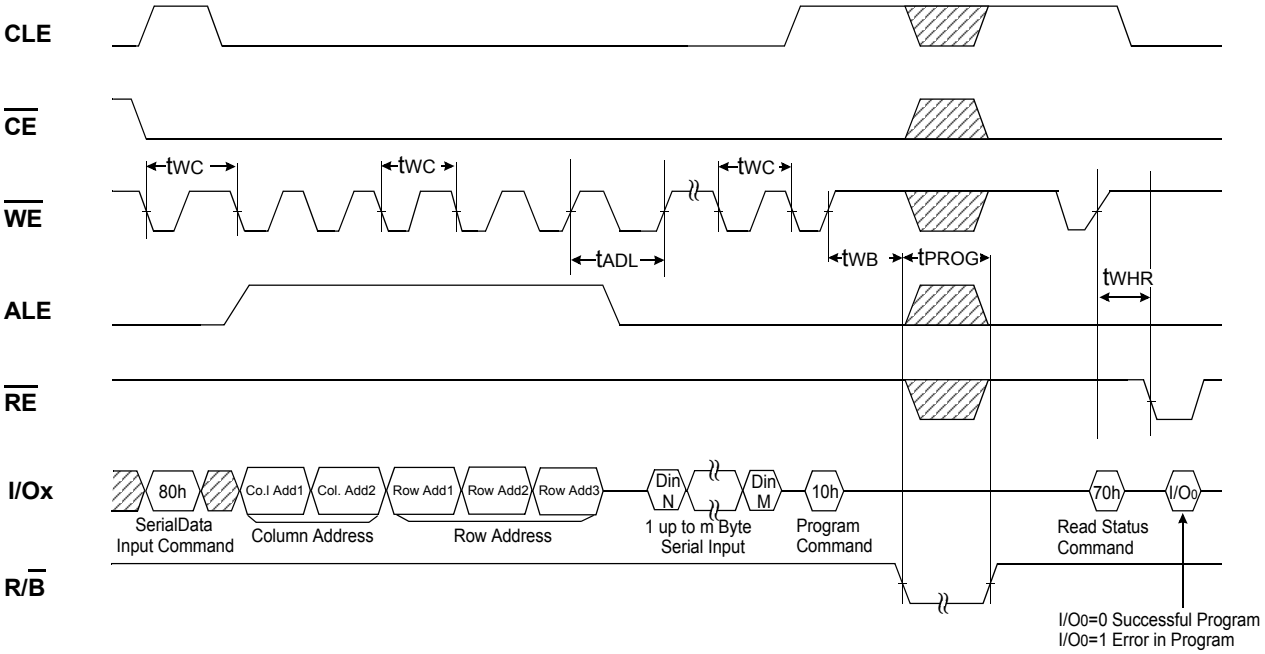
3.7 Read Operation(Intercepted by CE)



3.8 Random Data Output In a Page

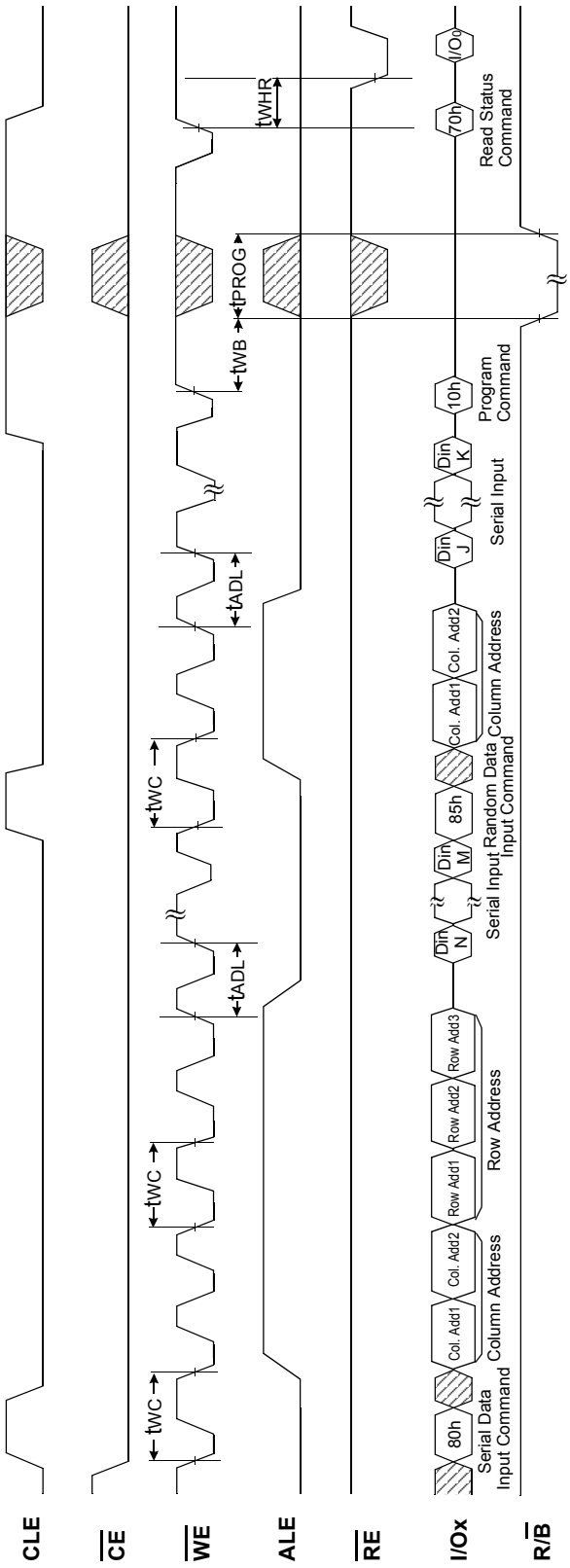


3.9 Page Program Operation



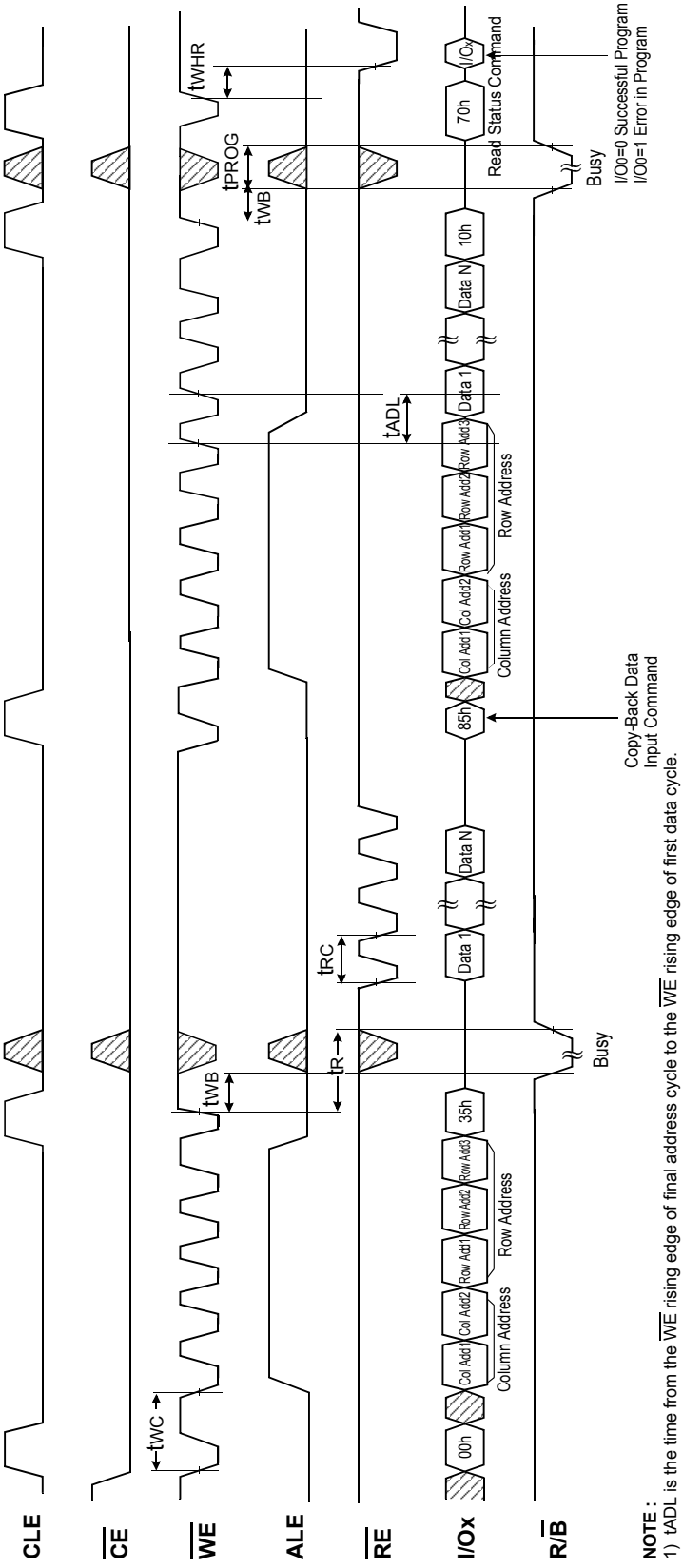
NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

3.10 Page Program Operation with Random Data Input



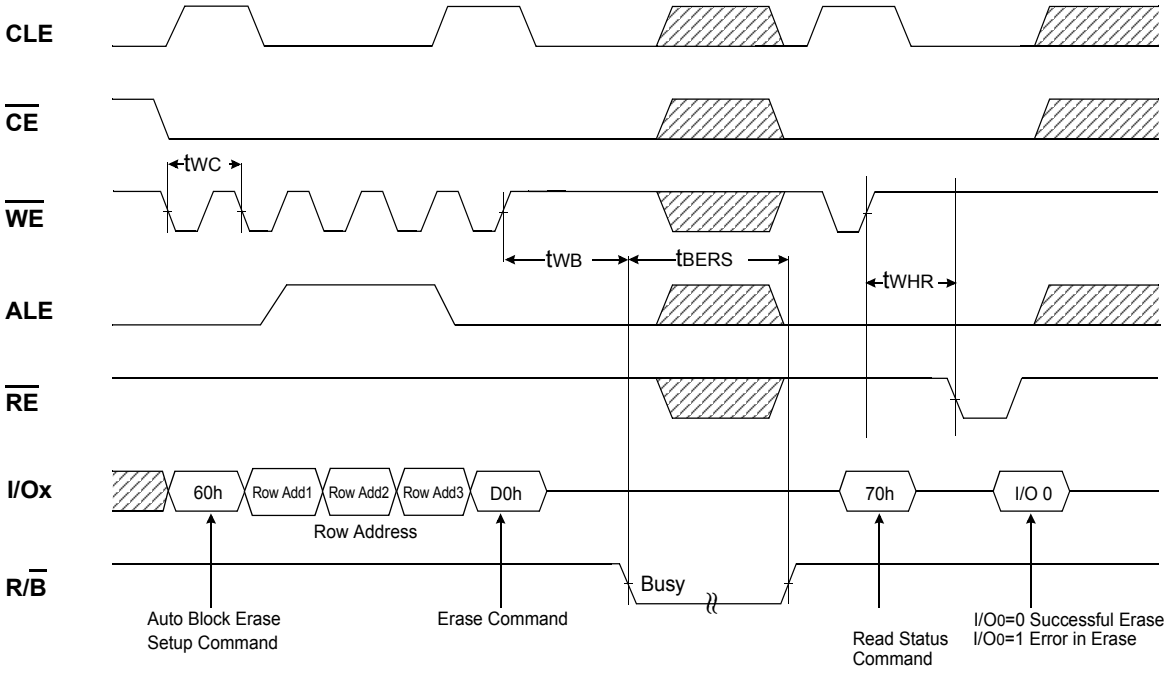
NOTE :
1) tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.
2) After serial input of data for random data input, status read(70h) command can be issued for reading status, and only status bit(I/O 6) is valid.

3.11 Copy-Back Program Operation with Random Data Input

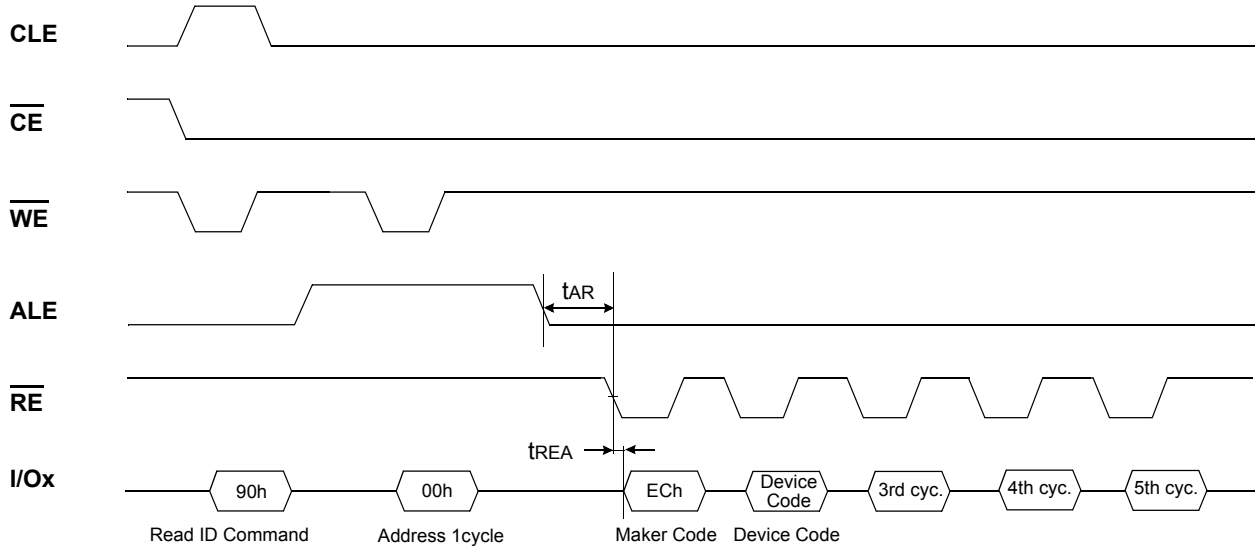


NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

3.12 Block Erase Operation



3.13 Read ID Operation



Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
4Gb(x8)	ACh	00h	15h	56h
8Gb DDP(x8)	A3h	01h	15h	5Ah
4Gb(x16)	BCh	00h	55h	56h
8Gb DDP(x16)	B3h	01h	55h	5Ah

3.13.1 ID Definition Table

90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number
4th Byte	Page Size, Block Size,Redundant Area Size, Organization
5th Byte	Plane Number, Plane Size, ECC Level

3rd ID Data

ITEM	Description	I/O #							
		7	6	5	4	3	2	1	0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between Multii-Chips	Not supported supported		0 1						
Cache Program	Not supported supported	0 1							

4th ID Data

ITEM	Description	I/O #							
		7	6	5	4	3	2	1	0
Page Size (without Redundant Area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (without Redundant Area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (Byte/512byte)	8 16 Reserved Reserved					0 0 1 1	0 1 0 1		
Organization	X8 X16		0 1						
Reserved		0 or 1							

5th ID Data

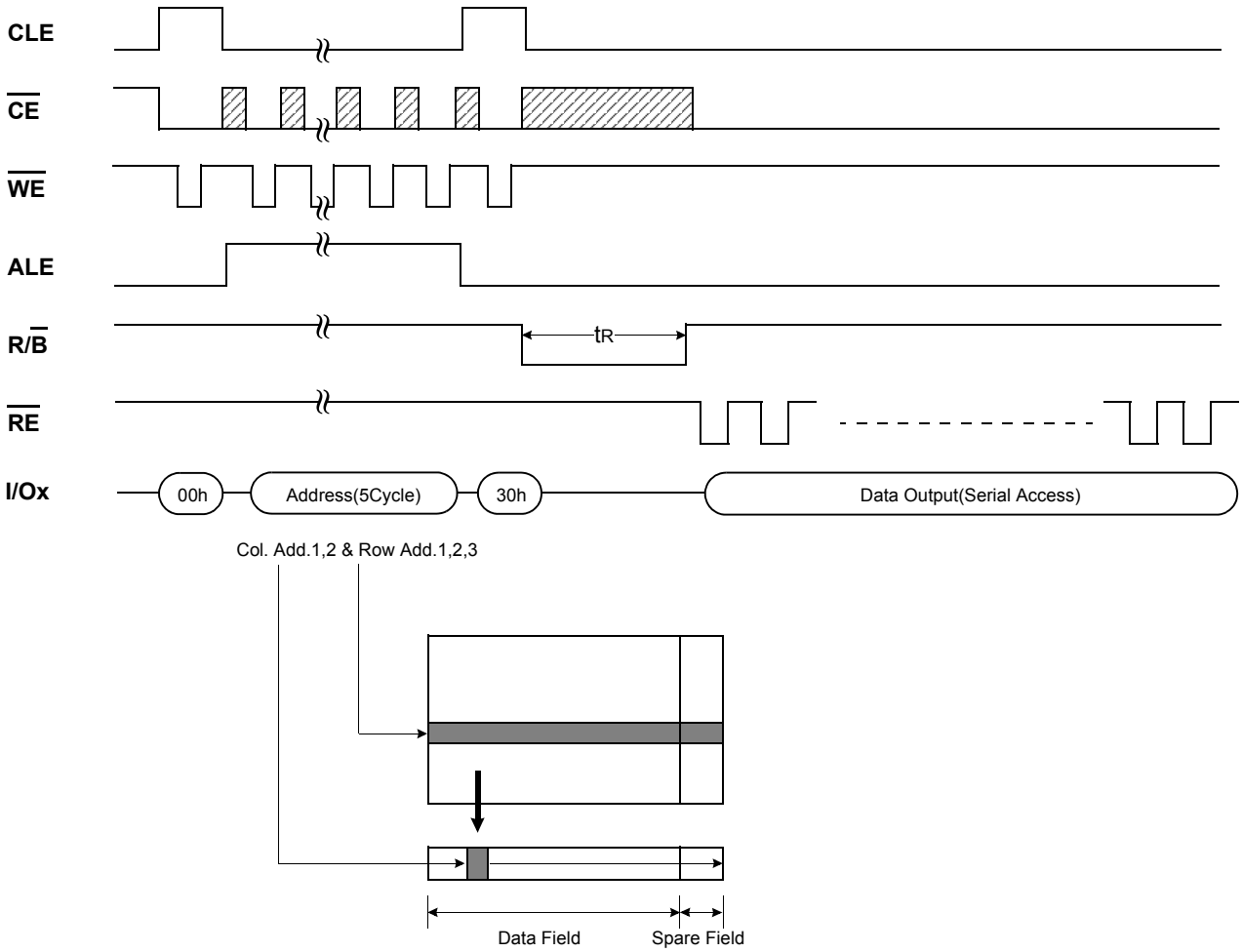
ITEM	Description	I/O #							
		7	6	5	4	3	2	1	0
ECC level	1bit ECC/512Byte 2bit ECC/512Byte 4bit ECC/512Byte Reserved							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (without Redundant Area)	64KB 128KB 256KB 512KB 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reseved	Reserved	0							

4.0 Device Operation

4.1 PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes(1,056 Wrods) of data within the selected page are transferred to the data registers in 40μs(tR) typically. The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 42ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 8. Read Operation



4.2 PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte(a word) or consecutive byte up to 2,112 bytes(1,056 Wrods), in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for a single page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112 bytes(1,056 Wrods) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The bytes(words) other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 9). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 9. Program & Read Status Operation

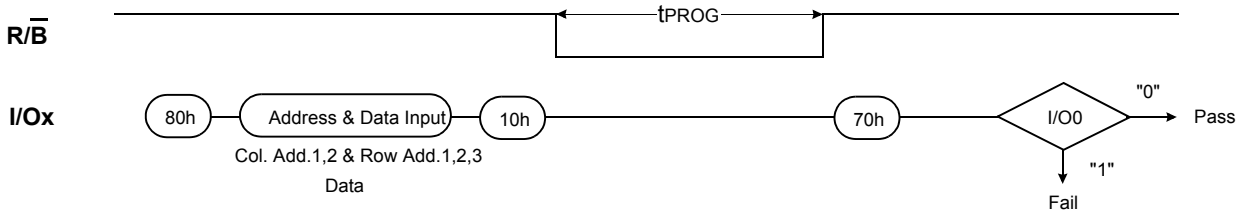
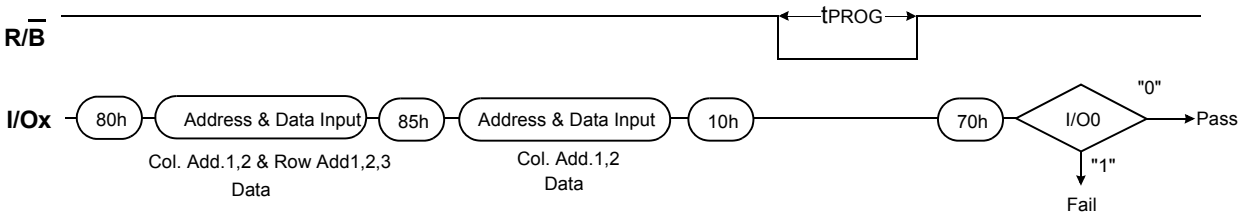


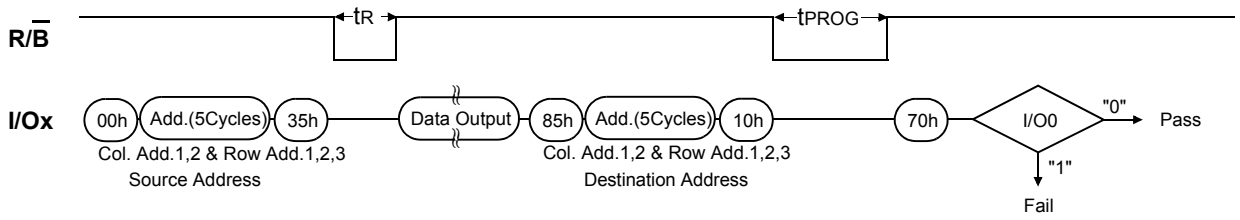
Figure 10. Random Data Input In a Page



4.3 COPY-BACK PROGRAM

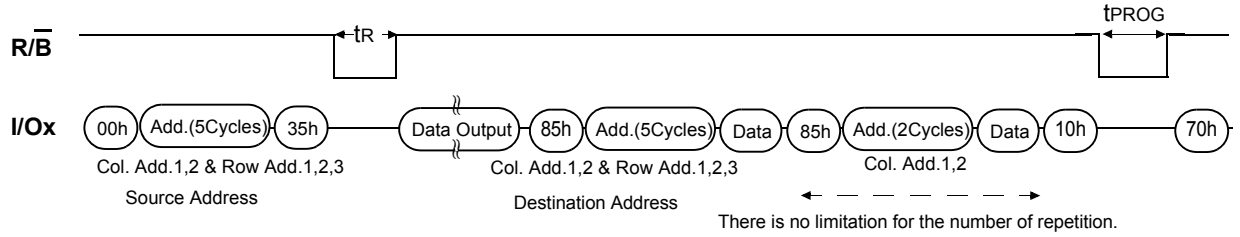
Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112 bytes(1,056 Wrods) data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 11 & Figure 12). The command register remains in Read Status command mode until another valid command is written to the command register.
During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 12.

Figure 11. Page Copy-Back Program Operation



NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.

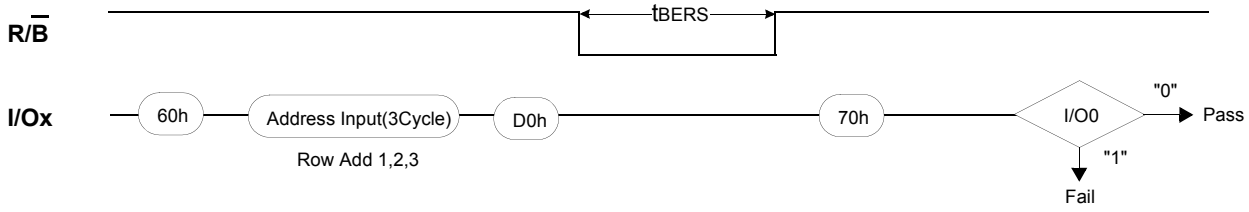
Figure 12. Page Copy-Back Program Operation with Random Data Input



4.4 BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only Block address is valid while page address is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation



4.5 READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table 4. Status Register Definition for 70h Command

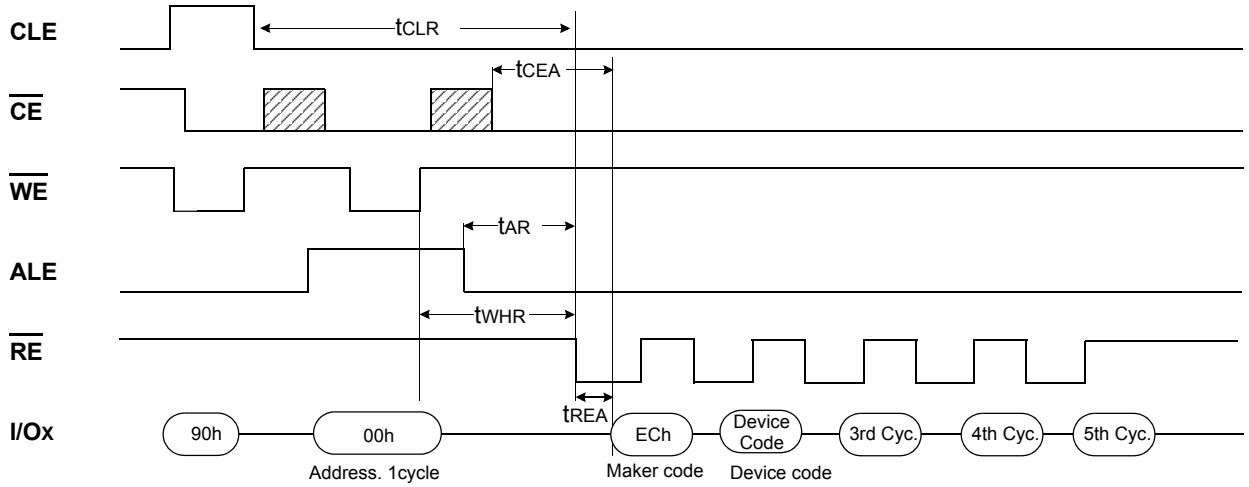
I/O	Page Program	Block Erase	Read	Definition	
I/O 0	Pass/Fail	Pass/Fail	Not Use	Pass : "0"	Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared	
I/O 2	Not use	Not use	Not use	Don't -cared	
I/O 3	Not Use	Not Use	Not use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Not Use	Not Use	Not Use	Don't -cared	
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

4.6 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 14 shows the operation sequence.

Figure 14. Read ID Operation



Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
4Gb(x8)	ACh	00h	15h	54h
8Gb DDP(x8)	A3h	01h	15h	58h
4Gb(x16)	BCh	00h	55h	54h
8Gb DDP(x16)	B3h	01h	55h	58h

4.7 RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 15 below.

Figure 15. RESET Operation

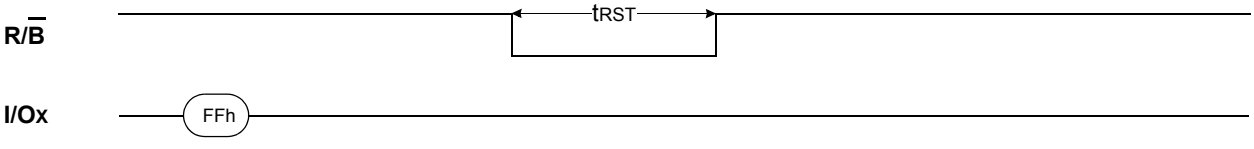


Table 5. Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

4.8 READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig.17). Its value can be determined by the following guidance.

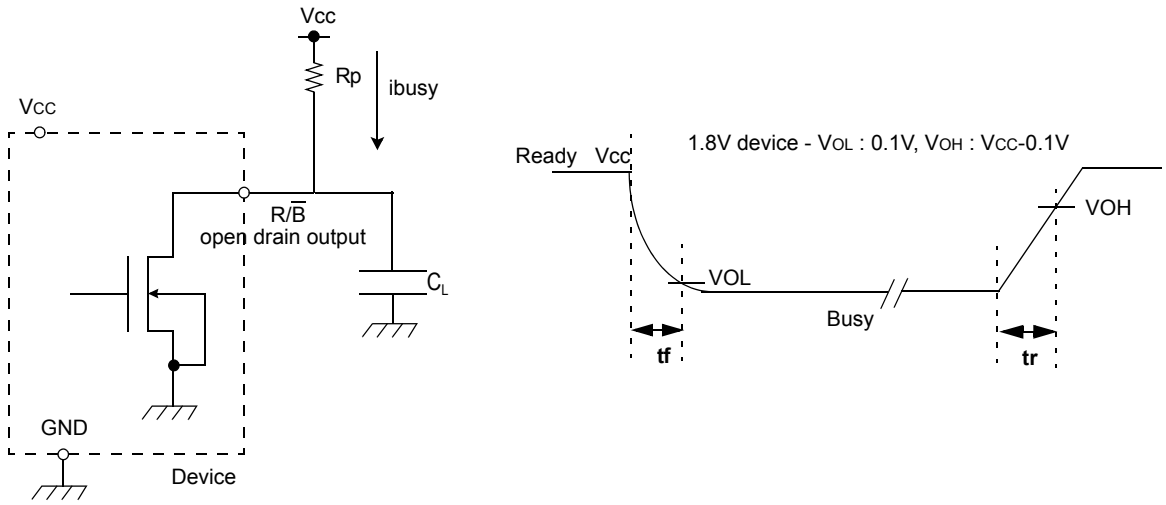
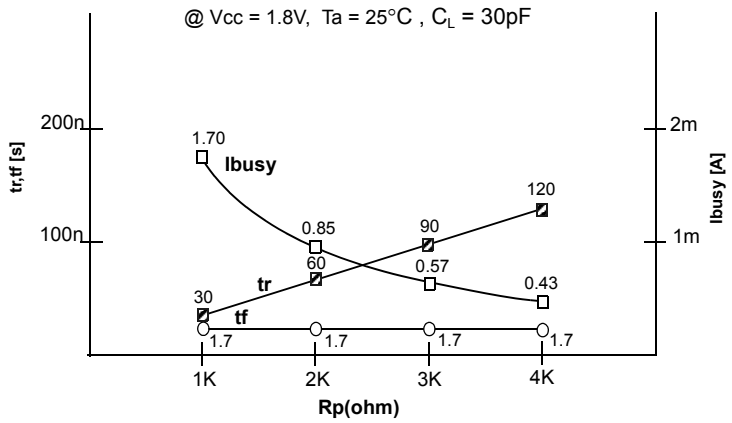


Figure 16. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

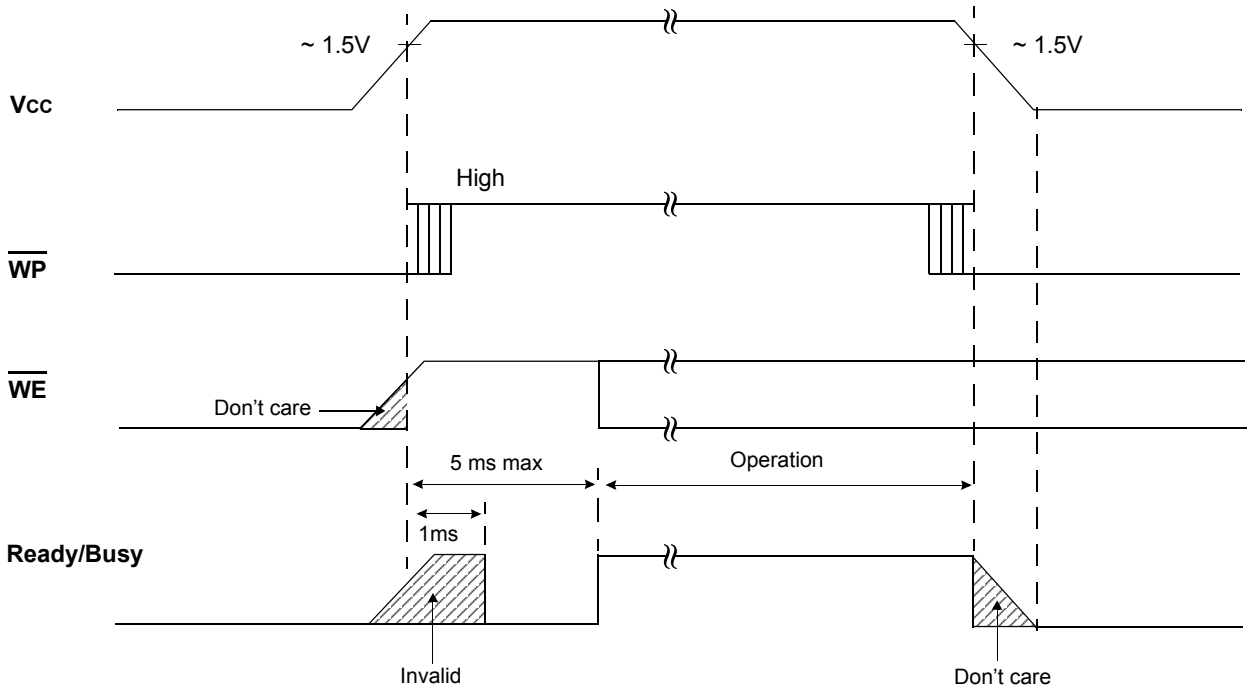
$$Rp(min, 1.8V\ part) = \frac{Vcc(Max.) - VOL(Max.)}{IOL + \Sigma IL} = \frac{1.85V}{3mA + \Sigma IL}$$

where IL is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

5.0 DATA PROTECTION & POWER UP SEQUENCE

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two step command sequence for program/erase provides additional software protection.

Figure 17. AC Waveforms for Power Transition



5.1 $\overline{WP}$ AC TIMING GUIDE

Enabling $\overline{WP}$ during erase and program busy is prohibited.
The erase and program operations are enabled and disabled as follows:

Figure 18. Program Operation

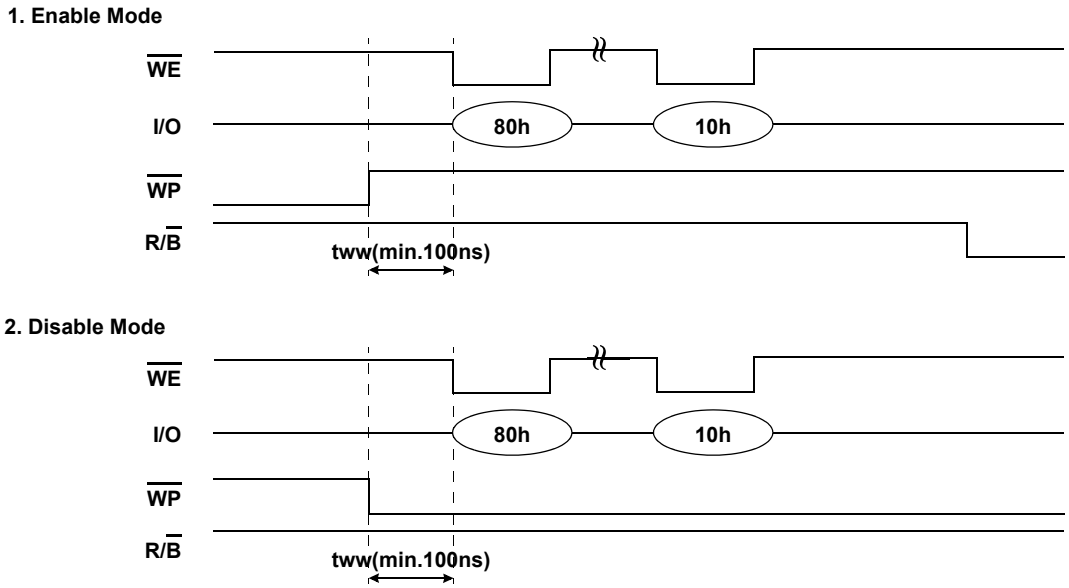
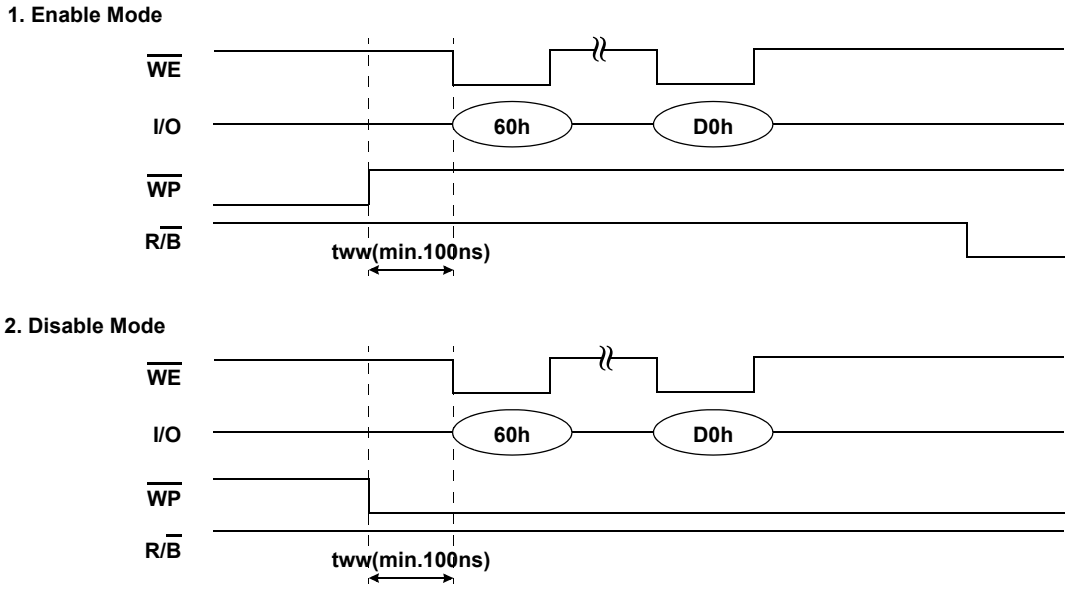


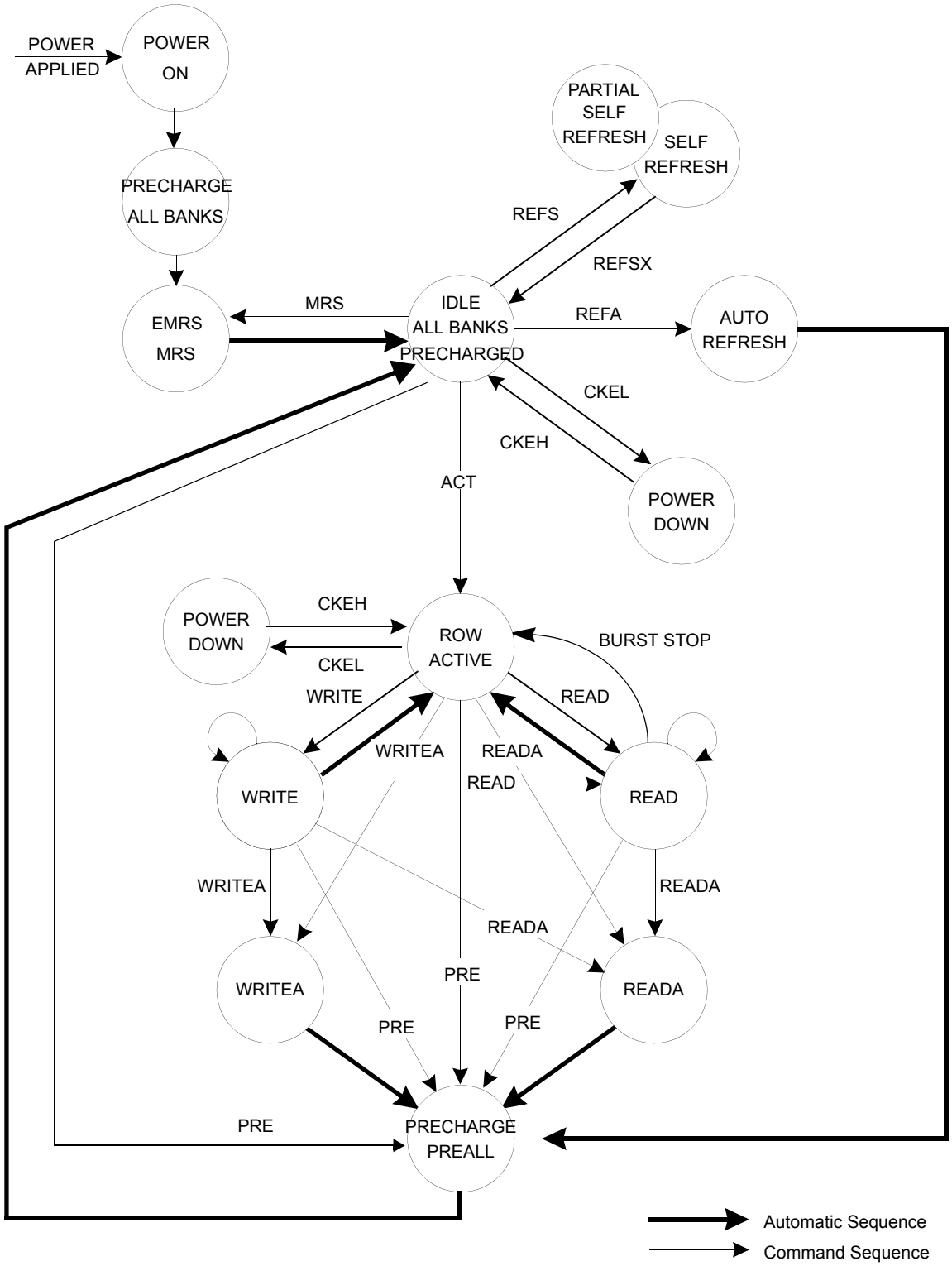
Figure 19. Erase Operation



2Gb (64M x32) M-DDR SDRAM B-die

1. Functional Description

Figure 1. State diagram

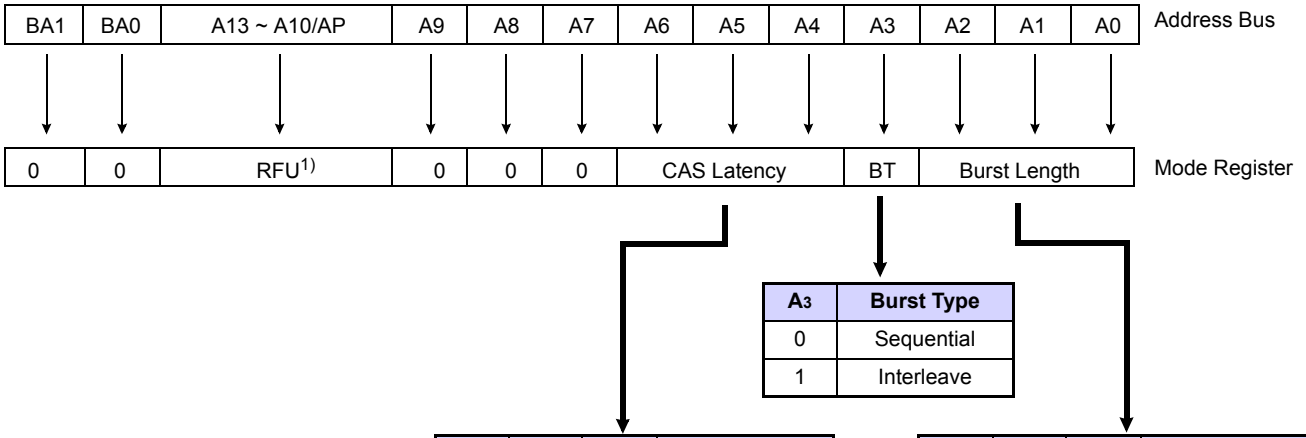


2. Mode Register Definition

2.1 Mode Register Set(MRS)

The mode register is designed to support the various operating modes of Mobile DDR SDRAM. It includes Cas latency, addressing mode, burst length, test mode and vendor specific options to make Mobile DDR SDRAM useful for variety of applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$(The Mobile DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The states of address pins A0 ~ A13 and BA0, BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the mode register. Two clock cycles are required to complete the write operation in the mode register. Even if the power-up sequence is finished and some read or write operation is executed afterward, the mode register contents can be changed with the same command and two clock cycles. This command must be issued only when all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, Cas latency(read latency from column address) uses A4 ~ A6, A7 ~ A13 is used for test mode. BA0 and BA1 must be set to low for proper MRS operation.

Figure 2. Mode Register Set



A_3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Type
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during MRS cycle

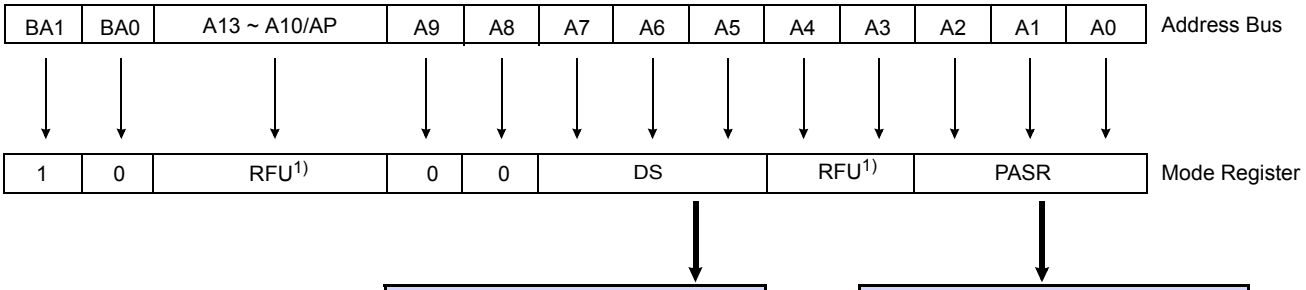
Table 1. Burst address ordering for burst length

Burst Length	Starting Address (A3, A2, A1, A0)	Sequential Mode	Interleave Mode
2	xxx0	0, 1	0, 1
	xxx1	1, 0	1, 0
4	xx00	0, 1, 2, 3	0, 1, 2, 3
	xx01	1, 2, 3, 0	1, 0, 3, 2
	xx10	2, 3, 0, 1	2, 3, 0, 1
	xx11	3, 0, 1, 2	3, 2, 1, 0
8	x000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	x001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	x010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	x011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	x100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	x101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	x110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	x111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0000	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15
	0001	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11,10,13,12,15,14
	0010	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1	2, 3, 0, 1, 6, 7, 4, 5,10,11, 8, 9, 14,15,12,13
	0011	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4,11,10, 9, 8, 15,14,13,12
	0100	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3,12,13,14,15, 8, 9, 10,11
	0101	5, 6, 7,8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2,13,12,15,14, 9, 8,11,10
	0110	6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1,14,15,12,13,10,11, 8, 9
	0111	7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, 15,14,13,12,11,10, 9, 8
	1000	8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7	8, 9,10,11,12,13,14,15, 0, 1, 2, 3, 4, 5, 6, 7
	1001	9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, 11,10,13,12,15,14,1, 0, 3, 2, 5, 4, 7, 6
	1010	10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	10,11, 8, 9, 14,15,12,13, 2, 3, 0, 1, 6, 7, 4, 5
	1011	11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11,10, 9, 8, 15,14,13,12, 3, 2, 1, 0, 7, 6, 5, 4
	1100	12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	12,13,14,15, 8, 9, 10,11, 4, 5, 6, 7, 0, 1, 2, 3
	1101	13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11,12	13,12,15,14, 9, 8,11,10, 5, 4, 7, 6, 1, 0, 3, 2
	1110	14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	14,15,12,13,10,11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
	1111	15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	15,14,13,12,11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

2.2 Extended Mode Register Set(EMRS)

The extended mode register is designed to support for the desired operating modes of DDR SDRAM. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1 ,low on BA0(The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A13 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and two clock cycles. But this command must be issued only when all banks are in the idle state. A0 - A2 are used for partial array self refresh and A5 - A7 are used for driver strength control. "High" on BA1 and"Low" on BA0 are used for EMRS. All the other address pins except A0,A1,A2,A5,A6, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.

Figure 3. Extended Mode Register Set



DS			
A_7	A_6	A_5	Driver Strength
0	0	0	Full
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	3/4
1	0	1	3/8
1	1	0	5/8
1	1	1	7/8

PASR			
A_2	A_1	A_0	Refreshed Area
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during EMRS cycle

2.3 Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, this Mobile DRAM includes the internal temperature sensor and control units to control the self refresh-cycle automatically according to the real device temperature.

2. TCSR ranges for IDD6 shown in the table are as an example only. Max IDD6 valus for 45°C, 85°C are guaranteed. Typical values for 85 °C, 70 °C, 45 °C and 15 °C are obtained from device characterization.

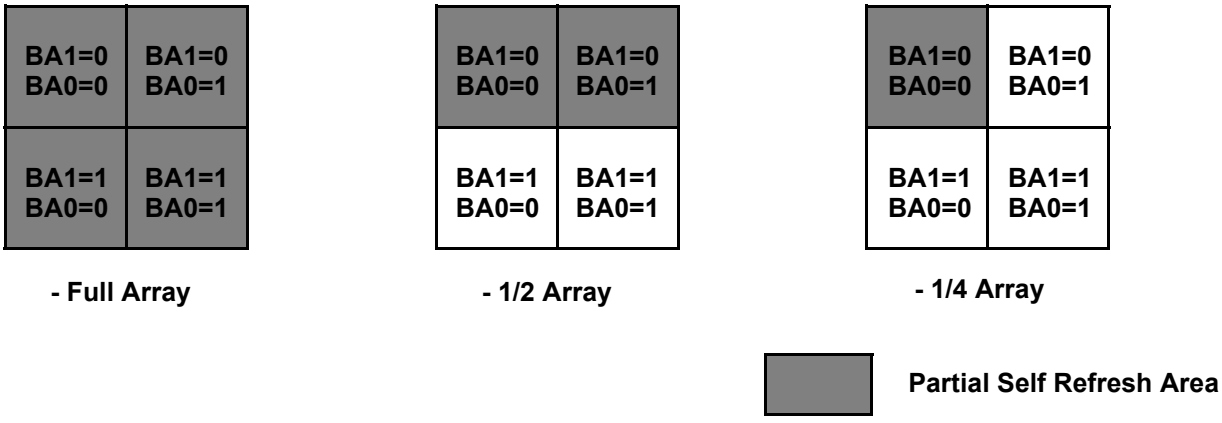
3. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (IDD6)						Unit
	Full Array		1/2 Array		1/4 Array		
	Typ.	Max	Typ.	Max	Typ.	Max	
85 °C	1100	1800	700	1500	500	1300	uA
70 °C	750		500		350		
45 °C	450	900	300	750	250	650	
15 °C	300		250		200		

2.4 Partial Array Self Refresh (PASR)

1. In order to save power consumption, Mobile DDR SDRAM includes PASR option.
2. Mobile DDR SDRAM supports three kinds of PASR in self refresh mode; Full array, 1/2 Array, 1/4 Array.

Figure 4. EMRS code and TCSR , PASR



3. Absolute maximum ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.7	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.7	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTE :
1) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2) Functional operation should be restricted to recommend operation condition.
3) Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

4. DC Operating Conditions

Recommended operating conditions(Voltage referenced to VSS=0V, Tc = -25°C to 85°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 1.8V)	VDD	1.7	1.95	V	1
I/O Supply voltage	VDDQ	1.7	1.95	V	1
Input logic high voltage (for Add.)	VIH(DC)	0.8 x VDDQ	VDDQ+0.3	V	2
Input logic high voltage (for Data)		0.7 x VDDQ	VDDQ+0.3	V	
Input logic low voltage (for Add.)	VIL(DC)	-0.3	0.2 x VDDQ	V	2
Input logic low voltage (for Data)		-0.3	0.3 x VDDQ	V	
Output logic high voltage	VOH(DC)	0.9 x VDDQ	-	V	IOH = -0.1mA
Output logic low voltage	VOL(DC)	-	0.1 x VDDQ	V	IOL = 0.1mA
Input leakage current	II	-2	2	uA	3
Output leakage current	IOZ	-5	5	uA	

NOTE :
1) Under all conditions, VDDQ must be less than or equal to VDD.
2) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
3) Any input 0V ≤ VIN ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.

5. DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, Tc = -25 to 85°C)

Parameter	Symbol	Test Condition	DDR 400	DDR 333	Unit	Note
Operating Current (One Bank Active)	IDD0	tRC=tRCmin; tCK=tCKmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	85	70	mA	
Precharge Standby Current in power-down mode	IDD2P	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	1.0		mA	
	IDD2PS	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	1.0			
Precharge Standby Current in non power-down mode	IDD2N	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	8		mA	
	IDD2NS	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	4			
Active Standby Current in power-down mode	IDD3P	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	6		mA	
	IDD3PS	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	5			
Active Standby Current in non power-down mode (One Bank Active)	IDD3N	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	15		mA	
	IDD3NS	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	10			
Operating Current (Burst Mode)	IDD4R	one bank active; BL=4; CL=3; tCK = tCKmin; continuous read bursts; I_{OUT} =0 mA address inputs are SWITCHING; 50% data change each burst transfer	115	100	mA	
	IDD4W	one bank active; BL = 4; tCK = tCKmin ; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	100	80		
Refresh Current	IDD5	tRC ≥ tRFC; tCK = tCKmin ; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	170	170	mA	1

Self Refresh Current	IDD6	CKE is LOW; t CK = t CKmin ; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	TCSR Range		Values Typ	Values Max		
			Full Array	85°C	1100	1800	uA	
				70°C	750			
				45°C	450	900		
				15°C	300			
			1/2 Array	85°C	700	1500	uA	
				70°C	500			
				45°C	300	750		
				15°C	250			
			1/4 Array	85°C	500	1300	uA	
				70°C	350			
				45°C	250	650		
				15°C	200			

NOTE :

1) IDD5 is measured in the below test condition.

Density	128Mb	256Mb	512Mb	1Gb	2Gb	Unit
tRFC	80	80	110	140	140	ns

2) IDD specifications are tested after the device is properly intialized.

3) Input slew rate is 1V/ns.

4) Definitions for IDD: LOW is defined as $V_{IN} \leq 0.1 * VDDQ$;
HIGH is defined as $V_{IN} \geq 0.9 * VDDQ$;
STABLE is defined as inputs stable at a HIGH or LOW level ;
SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles ;
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

5) DPD(Deep Power Down) function is an optional feature, and it will be enabled upon request.
Please contact Samsung for more information.

6. AC Operating Conditions & Timming Specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, all inputs	VIH(AC)	0.8 x VDDQ	VDDQ+0.3	V	1
Input Low (Logic 0) Voltage, all inputs	VIL(AC)	-0.3	0.2 x VDDQ	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(AC)	0.4 x VDDQ	0.6 x VDDQ	V	2

NOTE :
1) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2) The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

7. AC Timming Parameters & Specifications

Parameter		Symbol	DDR400		DDR333		Unit	Note
			Min	Max	Min	Max		
Clock cycle time	CL=3	tCK	5		6		ns	1,2
Row cycle time		tRC	55		60		ns	
Row active time		tRAS	40	70,000	42	70,000	ns	
RAS to CAS delay		tRCD	20		18		ns	
Row precharge time		tRP	15		18		ns	
Row active to Row active delay		tRRD	10		12		ns	
Write recovery time		tWR	12		12		ns	
Last data in to Active delay		tDAL	-		-		-	3
Last data in to Read command		tCDLR	2		1		tCK	
Col. address to Col. address delay		tCCD	1		1		tCK	
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQ Output data access time from CK/CK	CL=3	tAC	2	5	2	5.5	ns	4
DQS Output data access time from CK/CK	CL=3	tDQSCK	2	5	2	5.5	ns	
Data strobe edge to ouput data edge		tDQSQ		0.4		0.5	ns	
Read Preamble	CL=3	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		ns	5
DQS-in hold time		tWPREH	0.25		0.25		tCK	
DQS-in high level width		tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width		tDQSL	0.4	0.6	0.4	0.6	tCK	
DQS falling edge to CK setup time		tDSS	0.2		0.2		tCK	
DQS falling edge hold time from CK		tDSH	0.2		0.2		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time	fast slew rate	tIS	0.9		1.1		ns	7
	slow slew rate		1.1		1.3			8
Address and Control Input hold time	fast slew rate	tIH	0.9		1.1		ns	7
	slow slew rate		1.1		1.3			8
Address & Control input pulse width		tIPW	2.2		2.2			
DQ & DM setup time to DQS	fast slew rate	tDS	0.48		0.6		ns	6,7
	slow slew rate		0.58		0.7			6,8
DQ & DM hold time to DQS	fast slew rate	tDH	0.48		0.6		ns	6,7
	slow slew rate		0.58		0.7			6,8
DQ & DM input pulse width		tDIPW	1.2		1.2		ns	
DQ & DQS low-impedence time from CK/$\overline{CK}$		tLZ	1.0		1.0		ns	
DQ & DQS high-impedence time from CK/$\overline{CK}$		tHZ		5		5.5	ns	
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	tCK	

Parameter	Symbol	DDR400		DDR333		Unit	Note
		Min	Max	Min	Max		
DQS write preamble time	tWPRE	0.25		0.25		tCK	
Refresh interval time	tREF		64		64	ms	
Mode register set cycle time	tMRD	2		2		tCK	
Power down exit time	tPDEX	2		1		tCK	
CKE min. pulse width(high and low pulse width)	tCKE	2		2		tCK	
Auto refresh cycle time	tRFC	120		120		ns	9
Exit self refresh to active command	tXSR	120		120		ns	
Data hold from DQS to earliest DQ edge	tQH	tHPmin - tQHS		tHPmin - tQHS		ns	
Data hold skew factor	tQHS		0.5		0.65	ns	
Clock half period	tHP	tCLmin or tCHmin		tCLmin or tCHmin		ns	

NOTE :

1) tCK(max) value is measured at 100ns.

2) The only time that the clock Frequency is allowed to be changed is during clock stop, power-down, self-refresh modes.

3) In case of below 33MHz (tCK=30ns) condition, SEC could support tDAL(=2*tCK).
tDAL =(tWR/tCK) + (tRP/tCK)

4) tAC(min) value is measured at the high Vdd(1.95V) and cold temperature(-25°C).
tAC(max) value is measured at the low Vdd(1.7V) and hot temperature(85°C).
tAC is measured in the device with half driver strength and under the AC output load condition (Fig.6 in next Page).

5) The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

6) I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Data Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

7) Input slew rate 1.0 V/ ns.

8) Input slew rate 0.5V/ns and < 1.0V/ns.

9) Maximum burst refresh cycle : 8

8. AC Operating Test Conditions (VDD = 1.7V to 1.95V, TC = -25°C to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Figure 6	

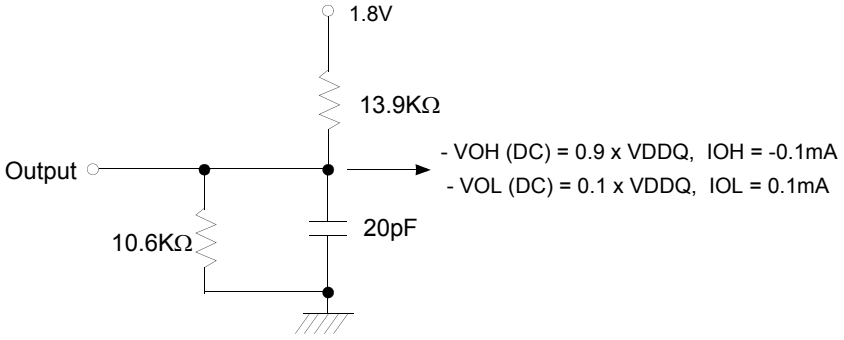


Figure 5. DC Output Load Circuit

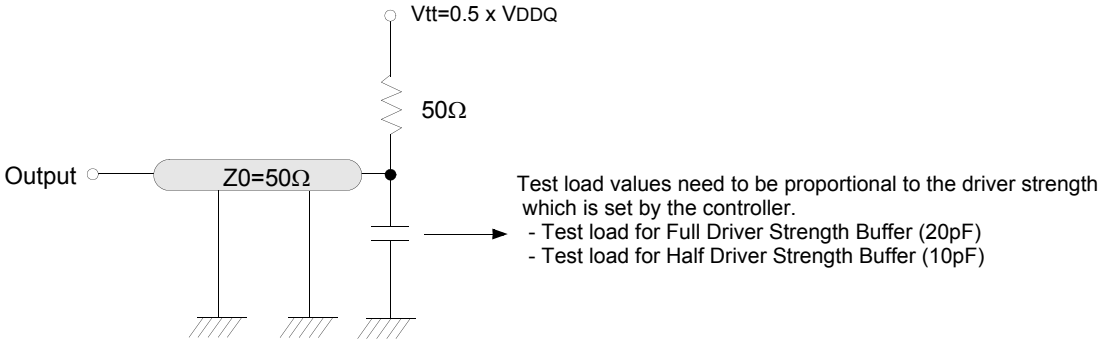


Figure 6. AC Output Load Circuit [1), 2)]

NOTE :

1) The circuit shown above represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will used IBIS or other simulations tools to correlate the timing reference load to system environment. Manufacturers will correlate to their poduction test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in ther same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tolls for system design validation is suggested.

2) Based on nominal impedance at 0.5 x VDDQ.
The impedence for Half(1/2) Driver Strength is designed 55ohm. And for other Driver Strength, it is designed proportionally.

9. Input/Output Capacitance(VDD=1.8, VDDQ=1.8V, TC = 25°C, f=100MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A13, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	1.5	3.0	pF
Input capacitance(CK, $\overline{CK}$)	CIN2	1.5	3.5	pF
Data & DQS input/output capacitance	COUT	2.0	4.5	pF
Input capacitance(DM)	CIN3	2.0	4.5	pF

10. AC Overshoot/Undershoot Specification for Address & Control Pins

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDD	3V-ns
Maximum undershoot area below VSS	3V-ns

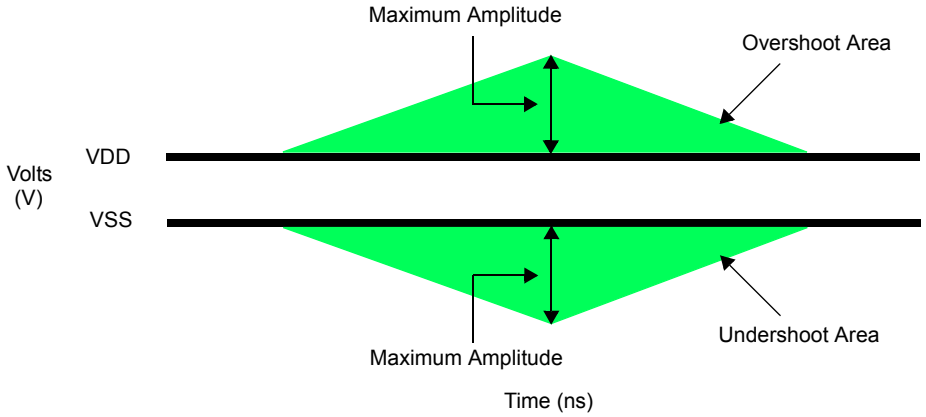


Figure 7. AC Overshoot and Undershoot Definition for Address and Control Pins

11. AC Overshoot/Undershoot Specification for CLK, DQ, DQS and DM Pins

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDDQ	3V-ns
Maximum undershoot area below VSSQ	3V-ns

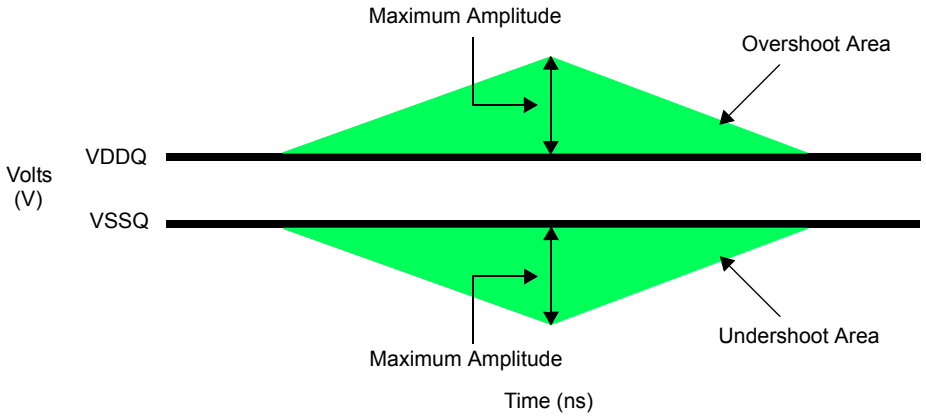


Figure 8. AC Overshoot and Undershoot Definition for CLK, DQ, DQS and DM Pins

12. Command Truth Table

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A13,A11, A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	X	X	X	X				
Precharge Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	H	H	H				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

NOTE :
1) OP Code : Operand Code. A0 ~ A13 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2) EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3) Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4) BA0 ~ BA1 : Bank select addresses.
5) If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6) During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
7) Burst stop command is valid at every burst length.
8) DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9) This combination is not defined for any function, which means "No Operation(NOP)" in Mobile DDR SDRAM.

13. Functional Truth Table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL[2)]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL[2)]
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL[4)]
	L	L	L	H	X	Refresh	AUTO-Refresh[5)]
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set[5)]
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL[2)]
	L	L	H	L	BA, A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge[3)]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL[2)]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst, Precharge[10)]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge[3)]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge[3)]
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL[2)]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge[10)]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE[6)] (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	6)
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	6)
	L	L	H	L	BA, A10	PRE/PREA	6)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE with AUTO RECHARGE[7] (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	7)
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	7)
	L	L	H	H	BA, RA	Active	7)
	L	L	H	L	BA, A10	PRE/PREA	7)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING (DURING tRP)	L	H	H	L	X	Burst Stop	ILLEGAL[2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL[2]
	L	L	H	H	BA, RA	Active	ILLEGAL[2]
	L	L	H	L	BA, A10	PRE/PREA	NOP[4](Idle after tRP)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO tRCD)	L	H	H	L	X	Burst Stop	ILLEGAL[2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL[2]
	L	L	H	H	BA, RA	Active	ILLEGAL[2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL[2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING tWR OR tCDLR)	L	H	H	L	X	Burst Stop	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	READ	ILLEGAL[2]
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL[2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL[2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING[8]	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down(Idle after tPDEX)
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE[9]	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State=Power Down

(H=High Level, L=Low level, X=Don't Care)

NOTE :
1) All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2) ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
(ILLEGAL = Device operation and/or data integrity are not guaranteed.)
3) Must satisfy bus contention, bus turn around and write recovery requirements.
4) NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5) ILLEGAL if any bank is not idle.
6) Refer to "Read with Auto Precharge Timing Diagram" for detailed information.
7) Refer to "Write with Auto Precharge Timing Diagram" for detailed information.
8) CKE Low to High transition will re-enable CK, $\overline{CK}$ and other inputs asynchronously.
A minimum setup time must be satisfied before issuing any command other than EXIT.
9) Power-Down, Self-Refresh can be entered only from All Bank Idle state.

MOBILE DDR SDRAM

Device Operations & Timing Diagram

Device Operations

1. Precharge

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

Table 1. Bank selection for precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

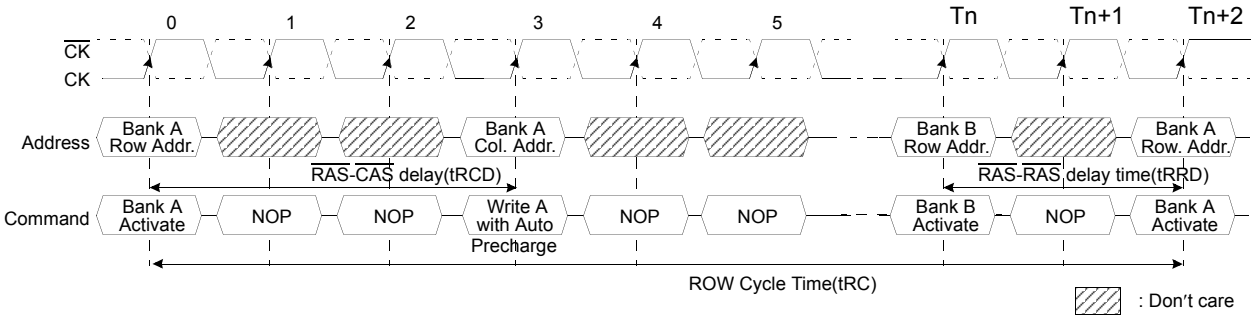
2. No Operation(NOP) & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode, Mobile DDR SDRAM should ignore all the control inputs. The Mobile DDR SDRAM is put in NOP mode when $\overline{CS}$ is activated and $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are deactivated. Both Device Deselect and NOP command can not affect operation already in progress. So even if the device is deselected or NOP command is issued under operation, the operation will be completed.

3. Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock(CK). The Mobile DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time, tRCD(min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time, tRRD(min).
Any system or application incorporating random access memory products should be properly designed, tested and qulified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

Figure 1. Bank Activation Command Cycle timing <tRCD=3CLK , tRRD=2CLK>



4. Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS cycle.

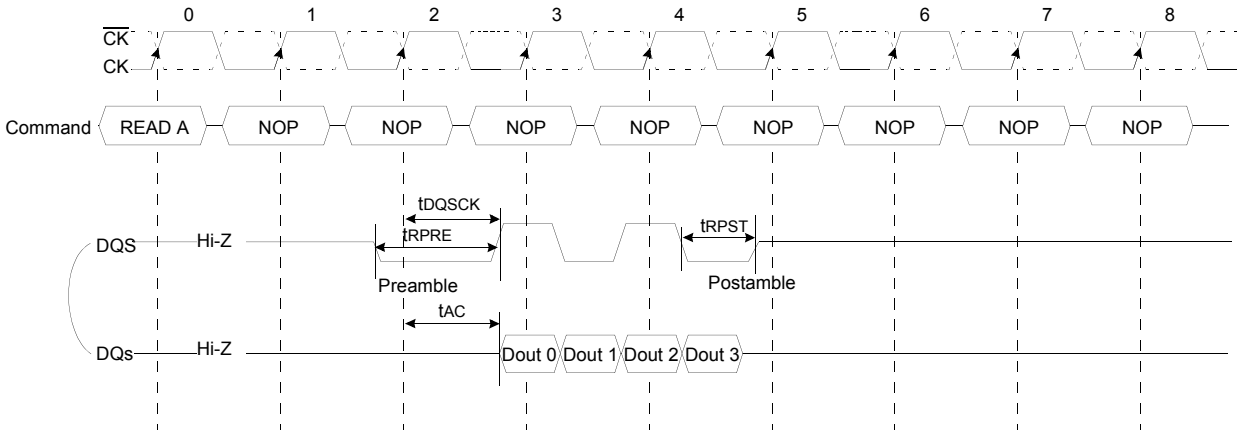
5. Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS cycle.

6. Burst Read Operation

Burst Read operation in Mobile DDR SDRAM is in the same manner as the Mobile SDR SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs determine the starting address for the Burst. The Mode Register sets type of burst(Sequential or interleave) and burst length(2, 4, 8, 16). The first output data is available with a CAS Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe(DQS) adopted by Mobile DDR SDRAM until the burst length is completed.

Figure 2. Burst read operation timing

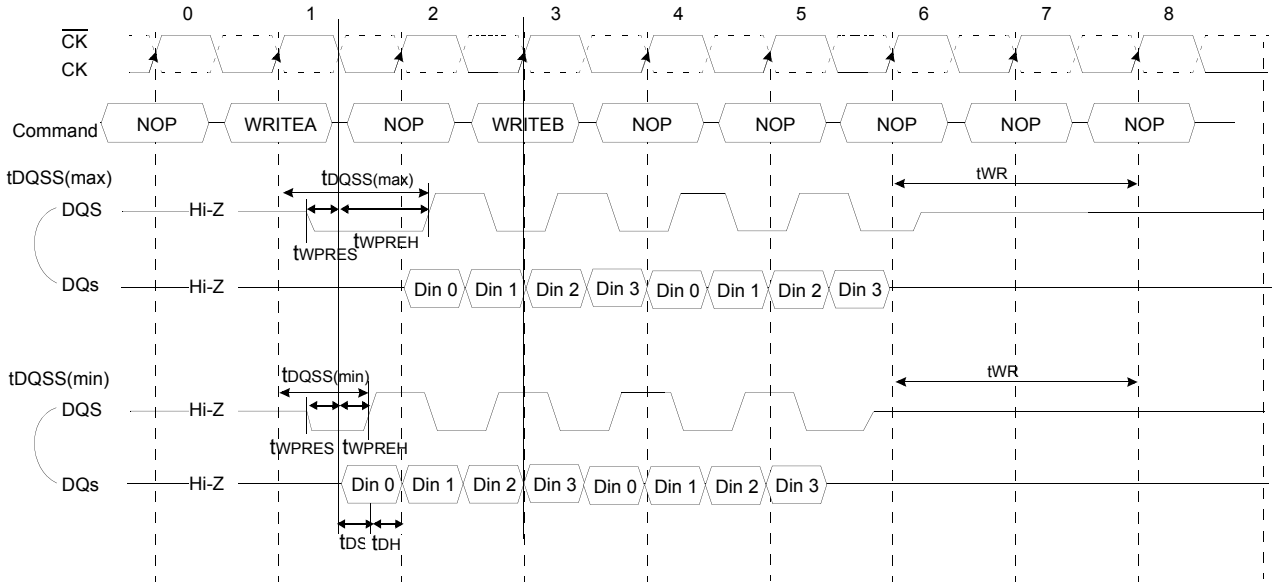


NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency= 3

7. Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock(CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS(Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock(CK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

Figure 3. Burst write operation timing

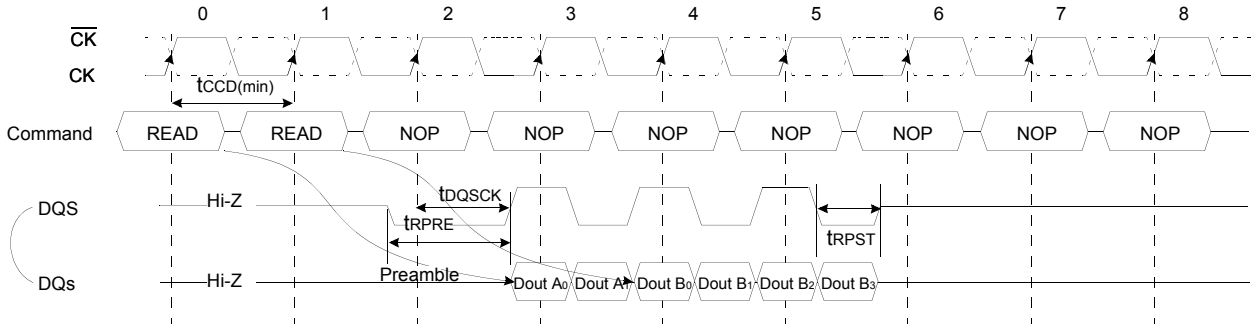


NOTE :
1) Burst Length=4
2) The specific requirement is that DQS be valid(High or Low) on or before this CK edge.
The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus.

8. Read Interrupted by a Read

A Burst Read can be interrupted by new Read command of any bank before completion of the burst. When the previous burst is interrupted, the new address with the full burst length override the remaining address. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.

Figure 4. Read interrupted by a read timing

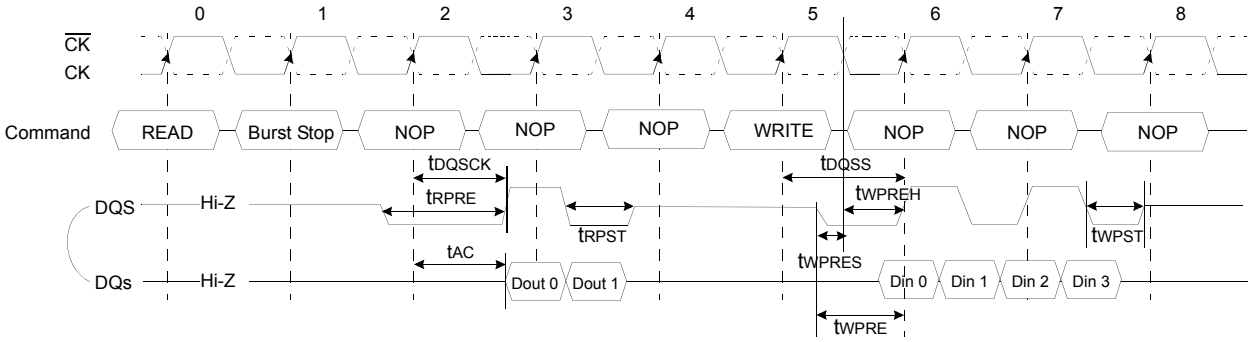


NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency=3

9. Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQs(Output drivers) in a high impedance state.

Figure 5. Read interrupted by a write and burst stop timing.



NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency=3

The following functionality establishes how a Write command may interrupt a burst Read.

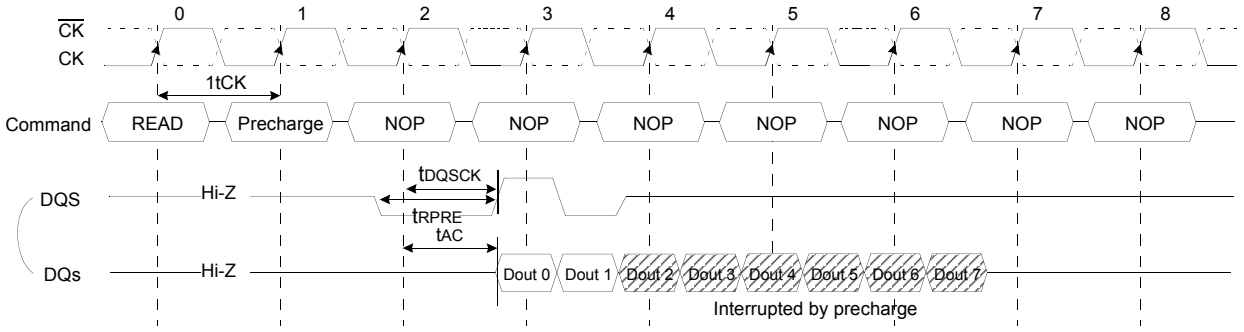
1. For Write commands interrupting a burst Read, a Burst Terminate command is required to stop the burst read and tri-state the DQ bus prior to valid input write data. Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=3 before the Write command.

2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

10. Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. The latency from a precharge command to invalid output is equivalent to the CAS latency.

Figure 6. Read interrupted by a precharge timing



NOTE :
1) Burst Length=8, $\overline{\text{CAS}}$ Latency=3

When a burst Read command is issued to a Mobile DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is completed. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a burst Read, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (Row Precharge time).

2. When a Precharge command interrupts a burst Read operation, the Precharge command given on a rising clock edge terminates the burst with the last valid data word presented on DQ pins at CL-1(CL=CAS Latency) clock cycles after the command has been issued. Once the last data word has been output, the output buffers are tri-stated. A new Bank Activate command may be issued to the same bank after tRP.

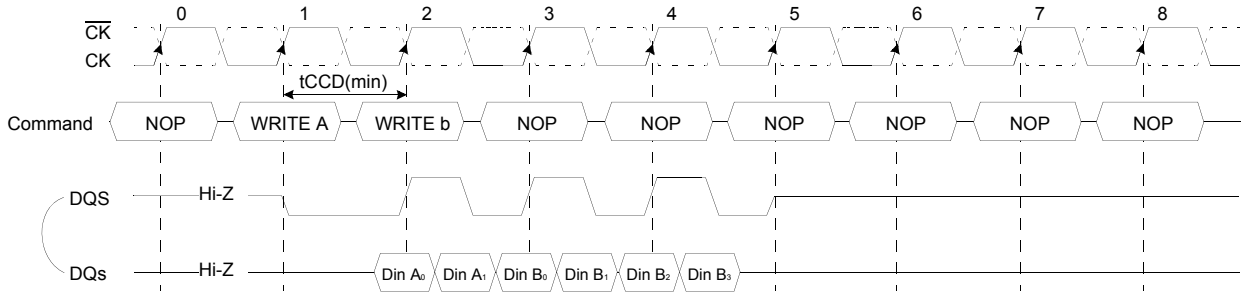
3. For a Read with Autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP from rising clock that comes CL(CL=CAS Latency) clock cycles before the end of the Read burst. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a rising clock edge).In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

11. Write Interrupted by a Write

A Burst Write can be interrupted by a new Write command before completion of the burst, where the interval between the successive Write commands must be at least one clock cycle(tCCD(min)). When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

Figure 7. Write interrupted by a write timing

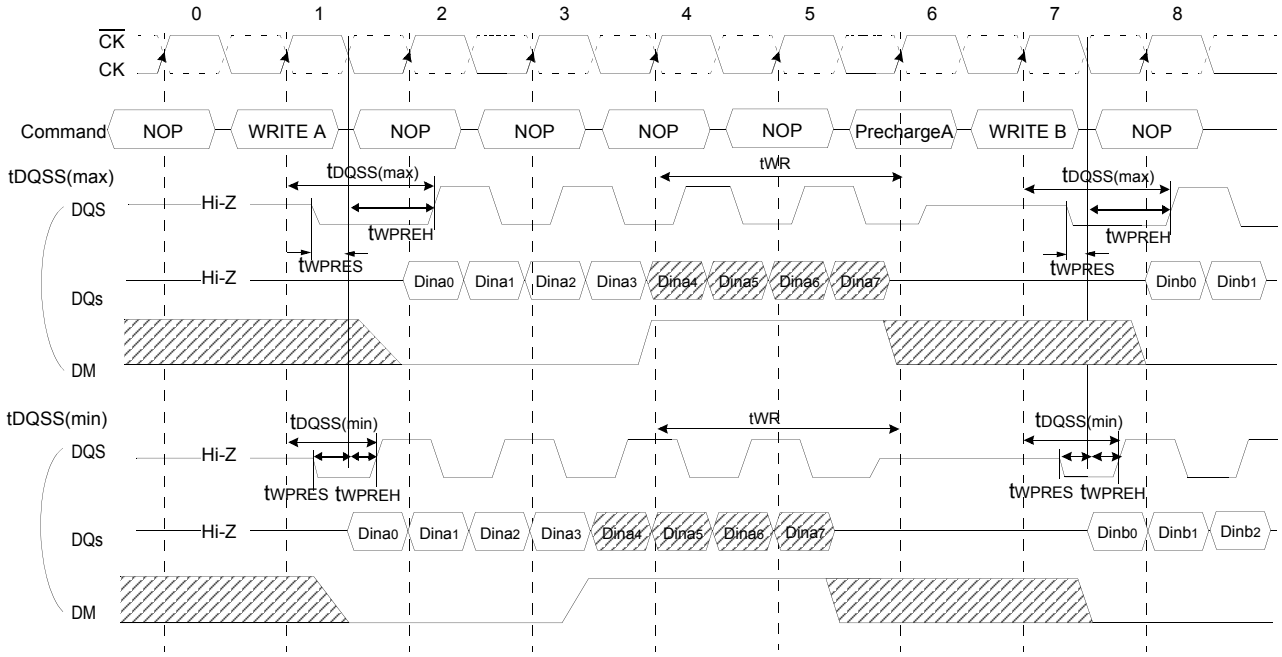


NOTE :
1) Burst Length=4

12. Write Interrupted by a Precharge & DM

A burst write operation can be interrupted by a precharge of the same bank before completion of the burst. Random column access is allowed. A write recovery time(tWR) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

Figure 8. Write interrupted by a precharge and DM timing



NOTE :
1) Burst Length=8

Precharge timing for Write operations in Mobile DDR SDRAM requires enough time to allow ”write recovery” which is the time required by a Mobile DDR SDRAM core to properly store a full ”0” or ”1” level before a Precharge operation. For Mobile DDR SDRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the Mobile DDR SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must make reference to only the clock domain that affects internal write operation, i.e., the input clock domain.

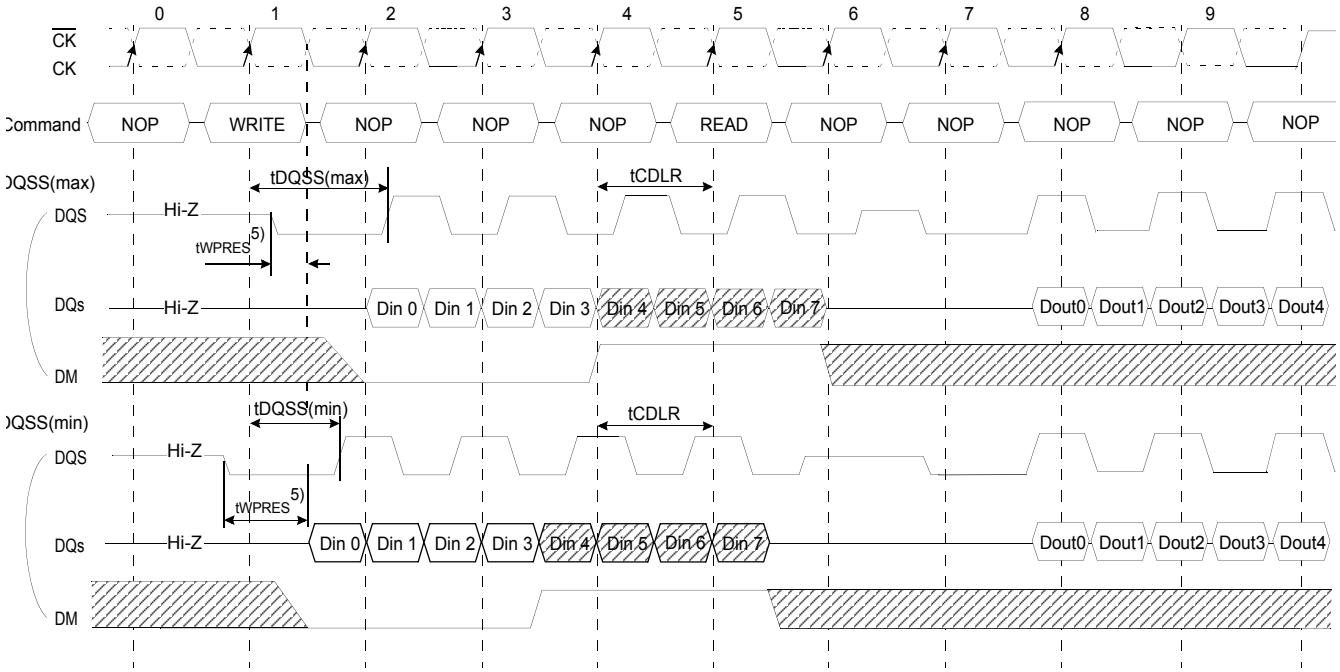
tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a burst Write without interrupting the burst, the minimum time for write recovery is defined by tWR.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

13. Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention Mobile DDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

Figure 9. Write interrupted by a Read and DM timing



NOTE :
1) Burst Length=8, $\overline{CAS}$ Latency=3

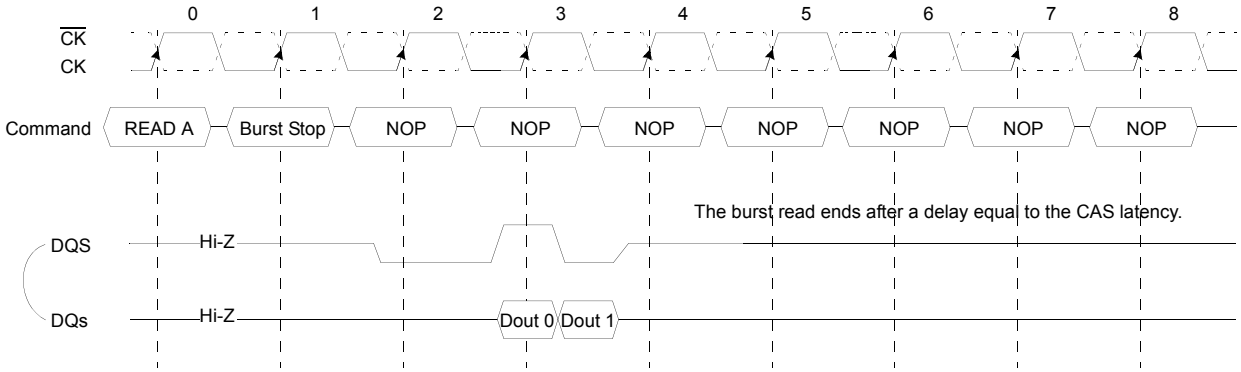
The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a burst Write, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For Read commands interrupting a burst Write, the DM pin must be used to mask the input data words whcich immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the Mobile DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the Mobile DDR SDRAM.
5. Refer to Burst write operation.

14. Burst Stop

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock(CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. However, the burst stop command is not supported during a burst write operation.

Figure 10. Burst stop timing



NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency= 3

The Burst Stop command is a mandatory feature for Mobile DDR SDRAM. The following functionality is required:

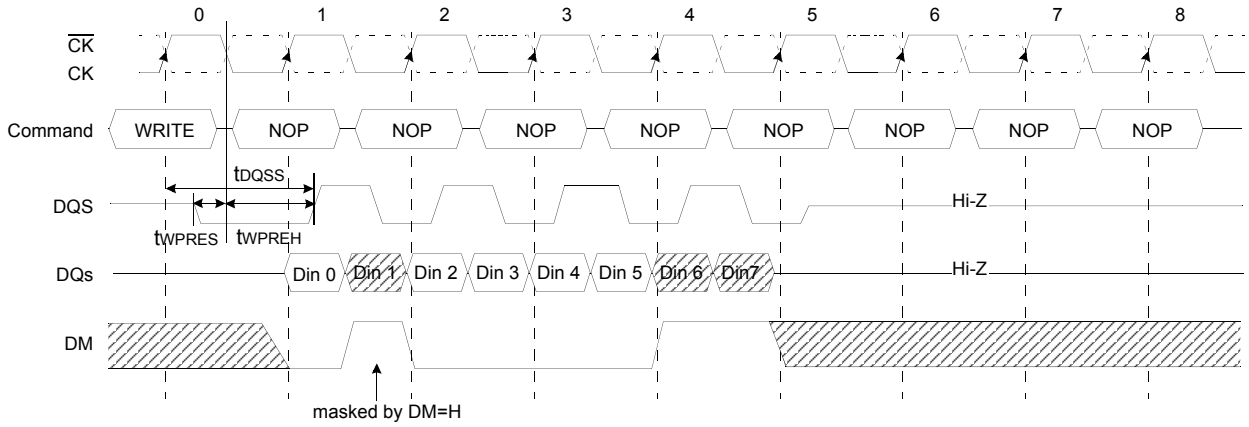
1. The Burst Stop command may only be issued on the rising edge of the input clock, CK.
2. Burst Stop is only a valid command during Read bursts.
3. Burst Stop during a Write burst is undefined and shall not be used.
4. Burst Stop applies to all burst lengths.
5. Burst Stop is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the CAS latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The Burst Stop command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

15. DM masking

The Mobile DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated(DM high) during write operation, Mobile DDR SDRAM does not accept the corresponding data.(DM to data-mask latency is zero). DM must be issued at the rising or falling edge of data strobe.

Figure 11. DM masking timing

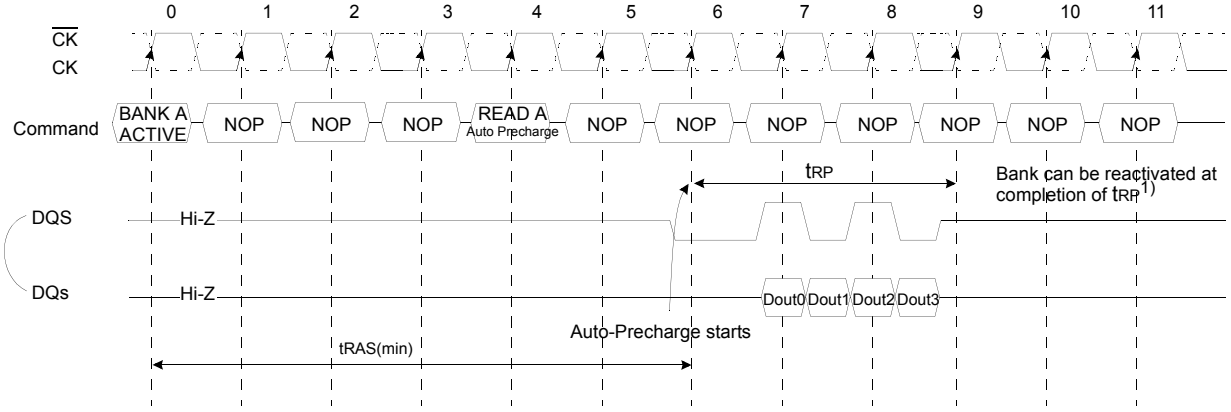


NOTE :
1) Burst Length=8

16. Read With Auto Precharge

If A10/AP is high when read command is issued , the read with auto-precharge function is performed. If a read with auto-precharge command is issued, the Mobile DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the precharge time(tRP) has been satisfied.

Figure 12. Read with auto precharge timing



NOTE :
1) Burst Length=4, CAS Latency= 3
2) The row active command of the precharge bank can be issued after tRP from this point.

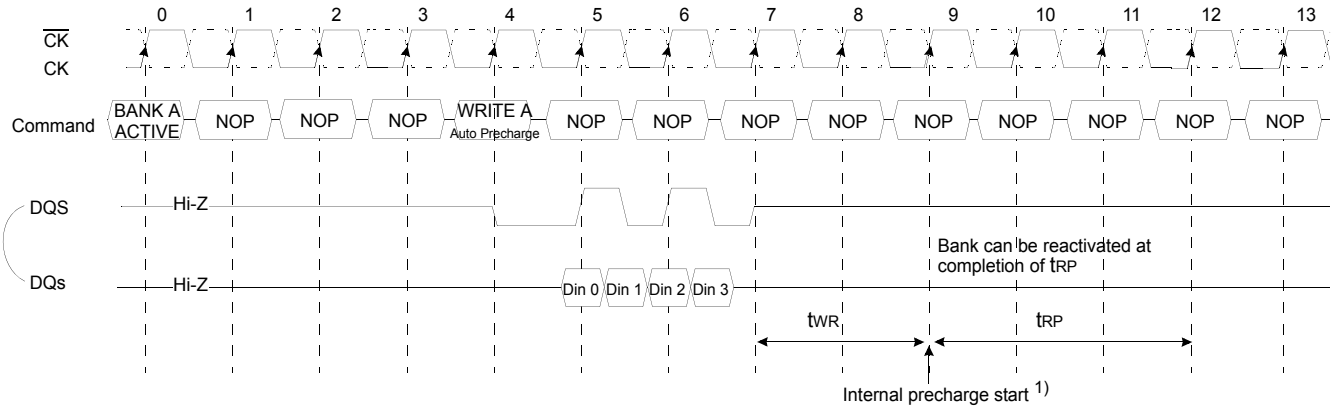
Asserted command	For same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ +No AP[1)]	READ+No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

NOTE :
1) AP = Auto Precharge

17. Write with Auto Precharge

If A10/AP is high when write command is issued , the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

Figure 13. Write with auto precharge timing



NOTE :
1) Burst Length=4
2) The row active command of the precharge bank can be issued after tRP from this point.

Asserted command	For same Bank						For Different Bank				
	5	6	7	8	9	10	5	6	7	8	9
WRITE	WRITE+ No AP[1)]	WRITE+ No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ+ NO AP+DM[2)]	READ+ NO AP+DM	READ+ NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ+AP	Illegal	READ + AP+DM	READ + AP+DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

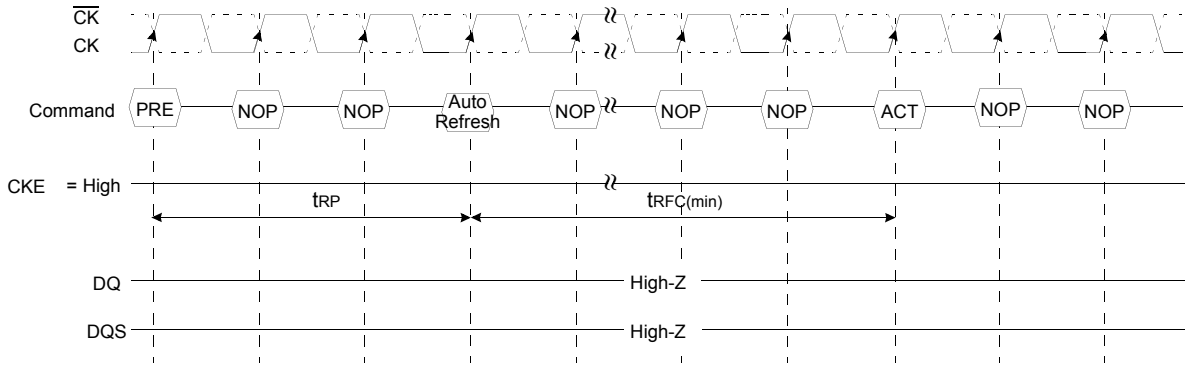
NOTE :
1) AP = Auto Precharge
2) DM : Refer to "27. *Write Interrupted by Precharge & DM* ".

18. Auto Refresh & Self Refresh

18.1. Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. Once this cycle has been started, no control of the external address pins are required because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tRFC(min).

Figure 14. Auto refresh timing

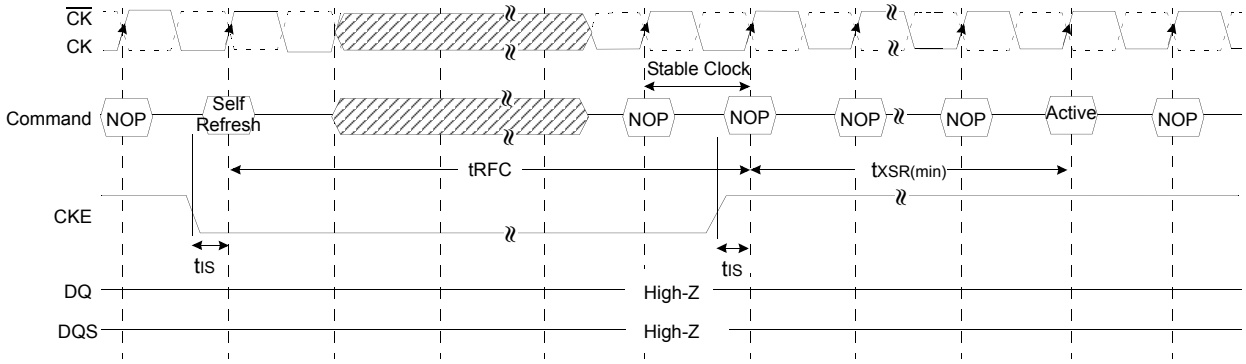


NOTE :
1) tRP=3CLK
2) Device must be in the all banks idle state prior to entering Auto refresh mode.

18.2. Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CK, $\overline{CK}$) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. Before returning CKE high to exit the Self Refresh mode, apply stable clock input signal with Deselect or NOP command asserted.

Figure 15. Self refresh timing

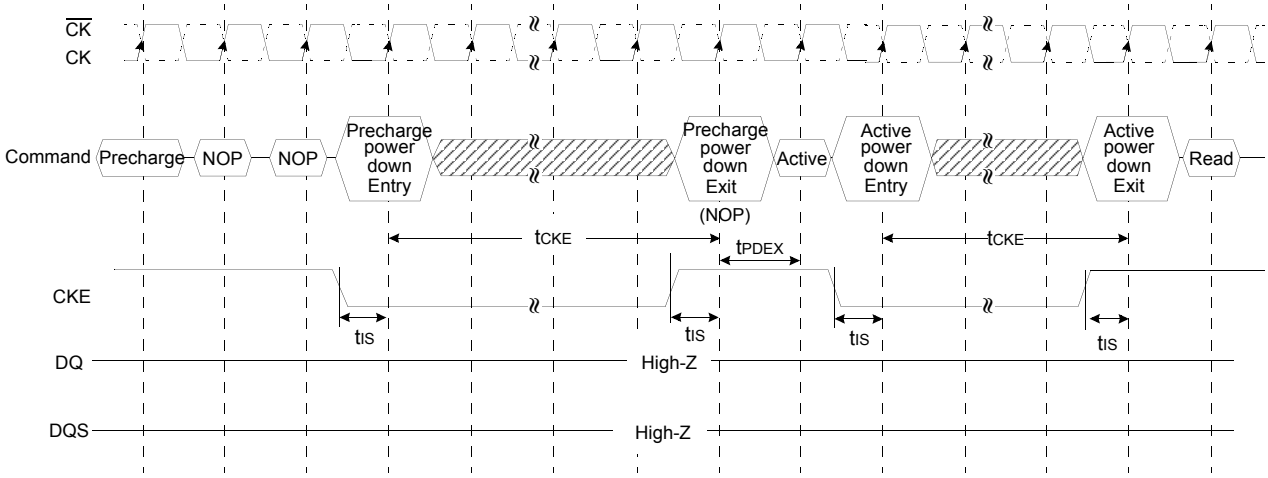


NOTE :
1) Device must be in the all banks idle state prior to entering Self Refresh mode.
2) The minimum time that the device must remain in Self Refresh mode si tRFC.

19. Power down

The device enters power down mode when CKE Low,and it exits when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set in high for at least tPDEX prior to Row active command. Refresh operations cannot be performed during power down mode, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.

Figure 16. Power down entry and exit timing



NOTE :
1) Device must be in the all banks idle state prior to entering Power Down mode.
2) The minimum power down duration is specified by tCKE.

20. Clock Stop

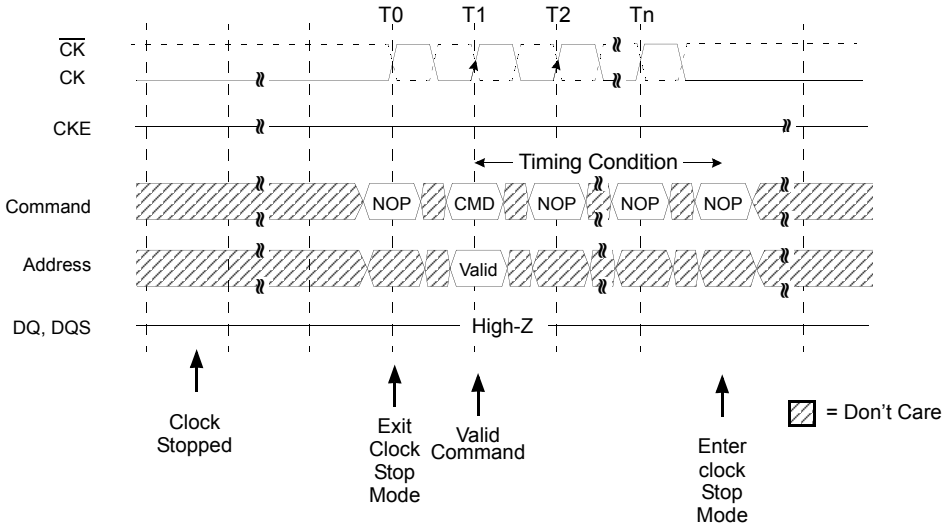
Stopping a clock during idle periods is an effective method of reducing power consumption.

The LPDDR SDRAM supports clock stop under the following conditions :
- the last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock requency;
- the related timing conditions(tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held High

When all conditions have been met, the device is either in "idle state"or "row active state" and clock stop mode may be entered with CK held Low and $\overline{CK}$ held Hight.
Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command any be applied. Additional clock pulses might be required depending on the system characteristics.

Figure 17 shows clock stop mode entry and exit.
- Initially the device is in clock stop mode
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command is completed.
- Tn is the last clock pulse required by the access command latched with T1
- The clock can be stopped after Tn.

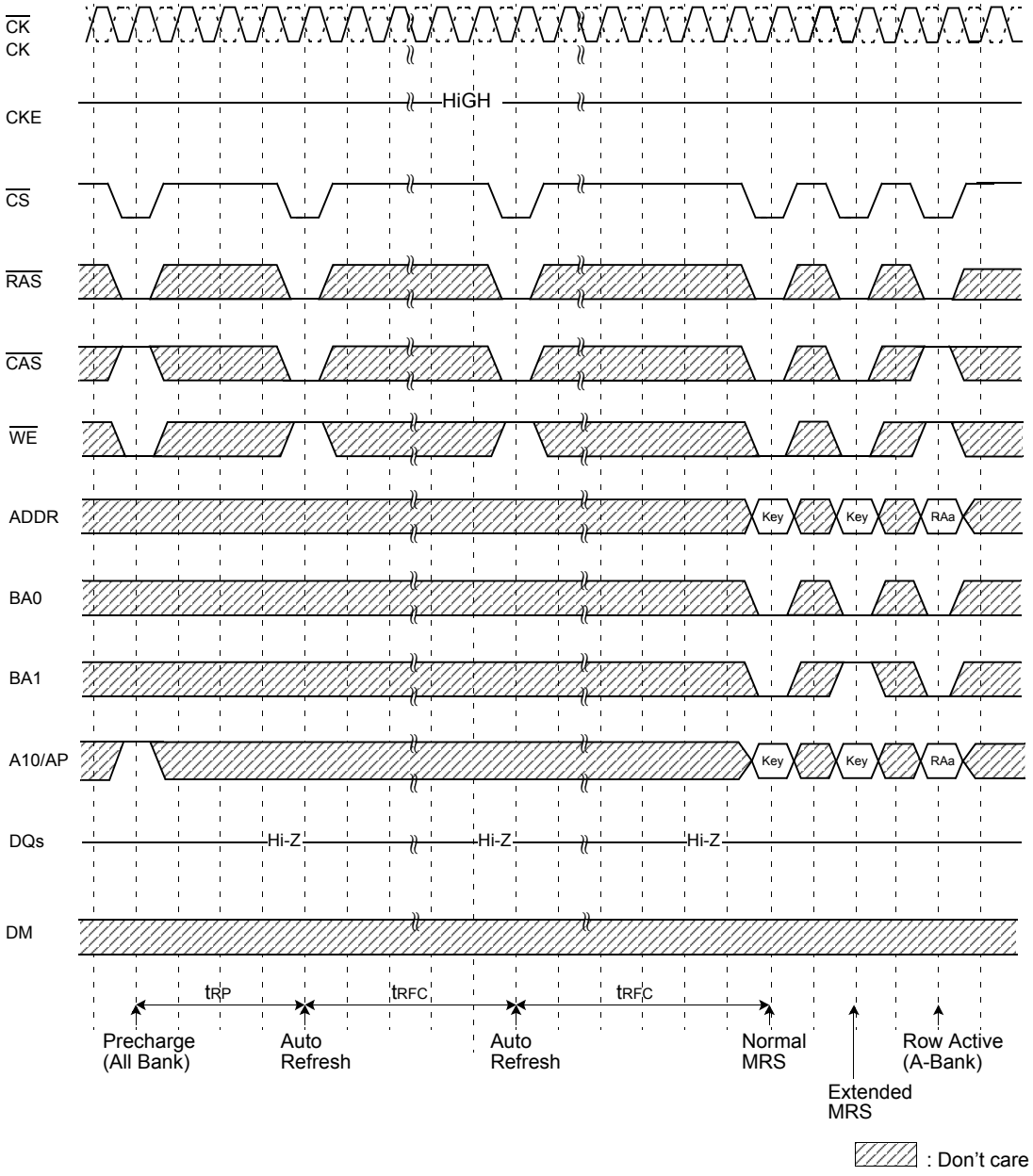
Figure 17. Clock Stop Mode Entry and Exit



Timing Diagram

21. Power Up Sequence for Mobile DDR SDRAM

Figure 18. Power Up Sequence for Mobile DDR SDRAM

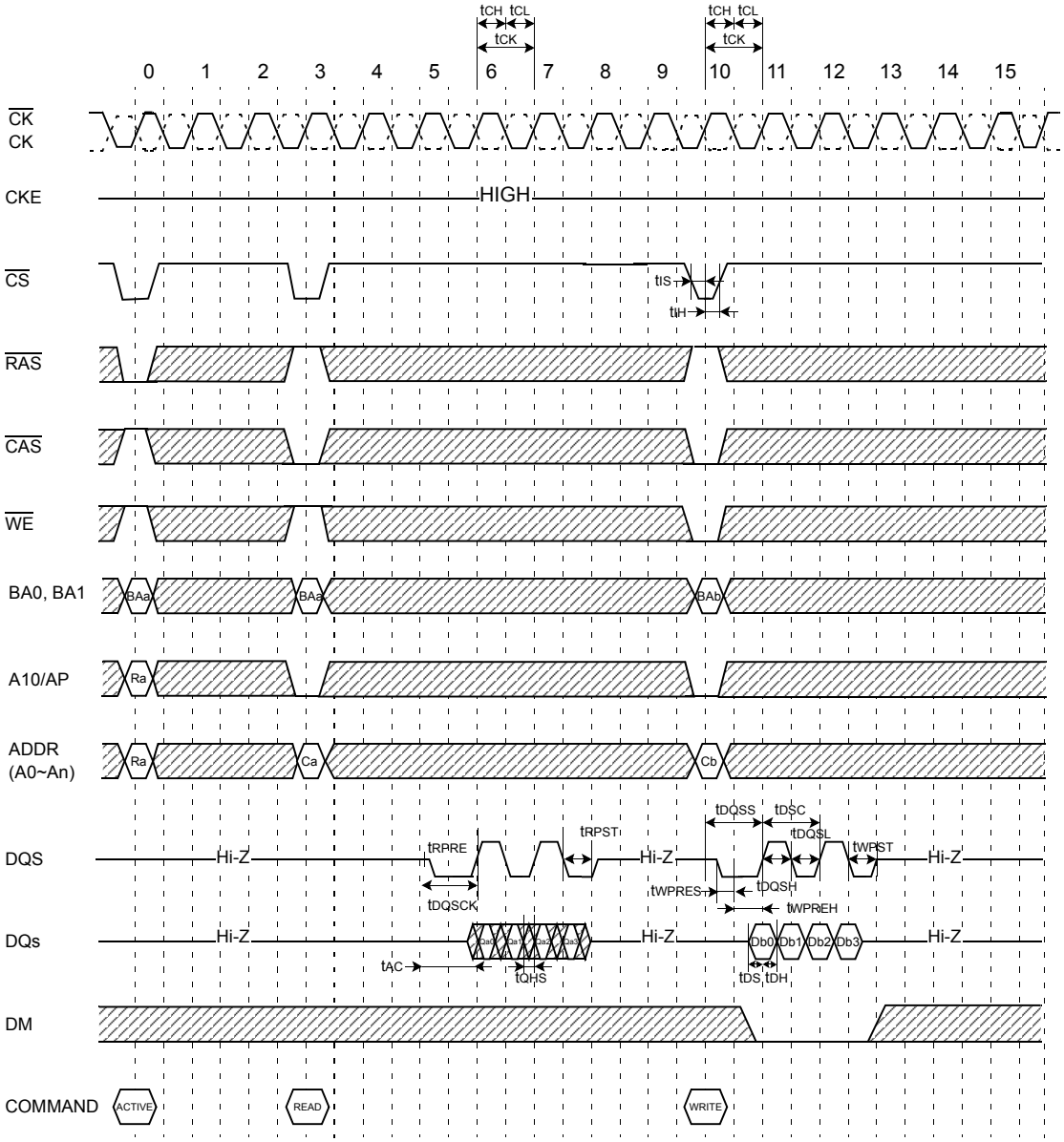


NOTE :
1) Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
 - Apply VDD before or at the same time as VDDQ.
2) Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3) Issue precharge commands for all banks of the devices.
4) Issue 2 or more auto-refresh commands.
5) Issue a mode register set command to initialize the mode register.
6) Issue a extended mode register set command for the desired operating modes after normal MRS.

The Mode Register and Extended Mode Register do not have default values.
If they are not programmed during the initialization sequence, it may lead to unspecified operation.
All banks have to be in idle state prior to adjusting MRS and EMRS set.

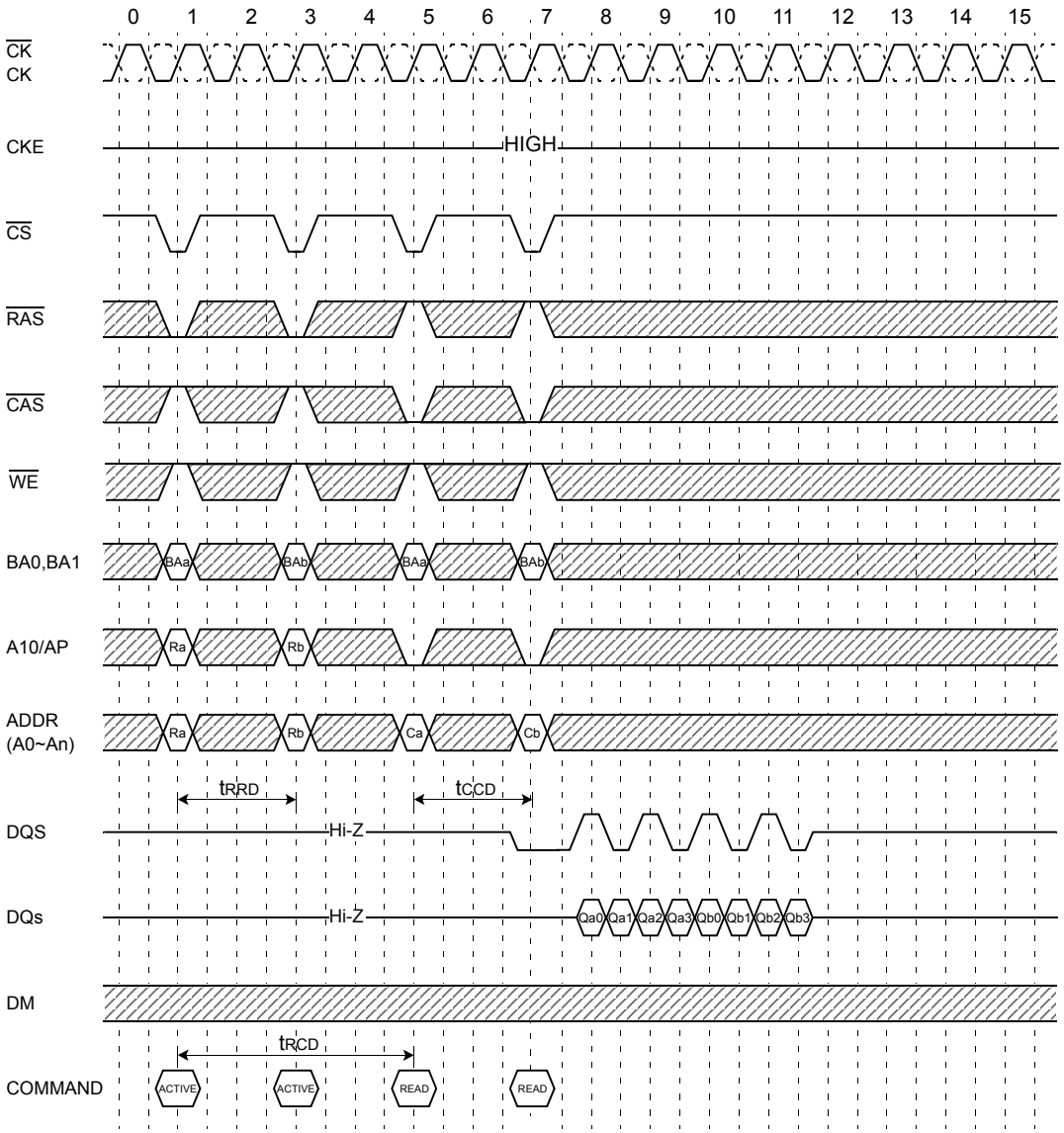
22. Basic Timing

Figure 19. Basic Timing (Setup, Hold and Access Time @BL=4, CL=3)



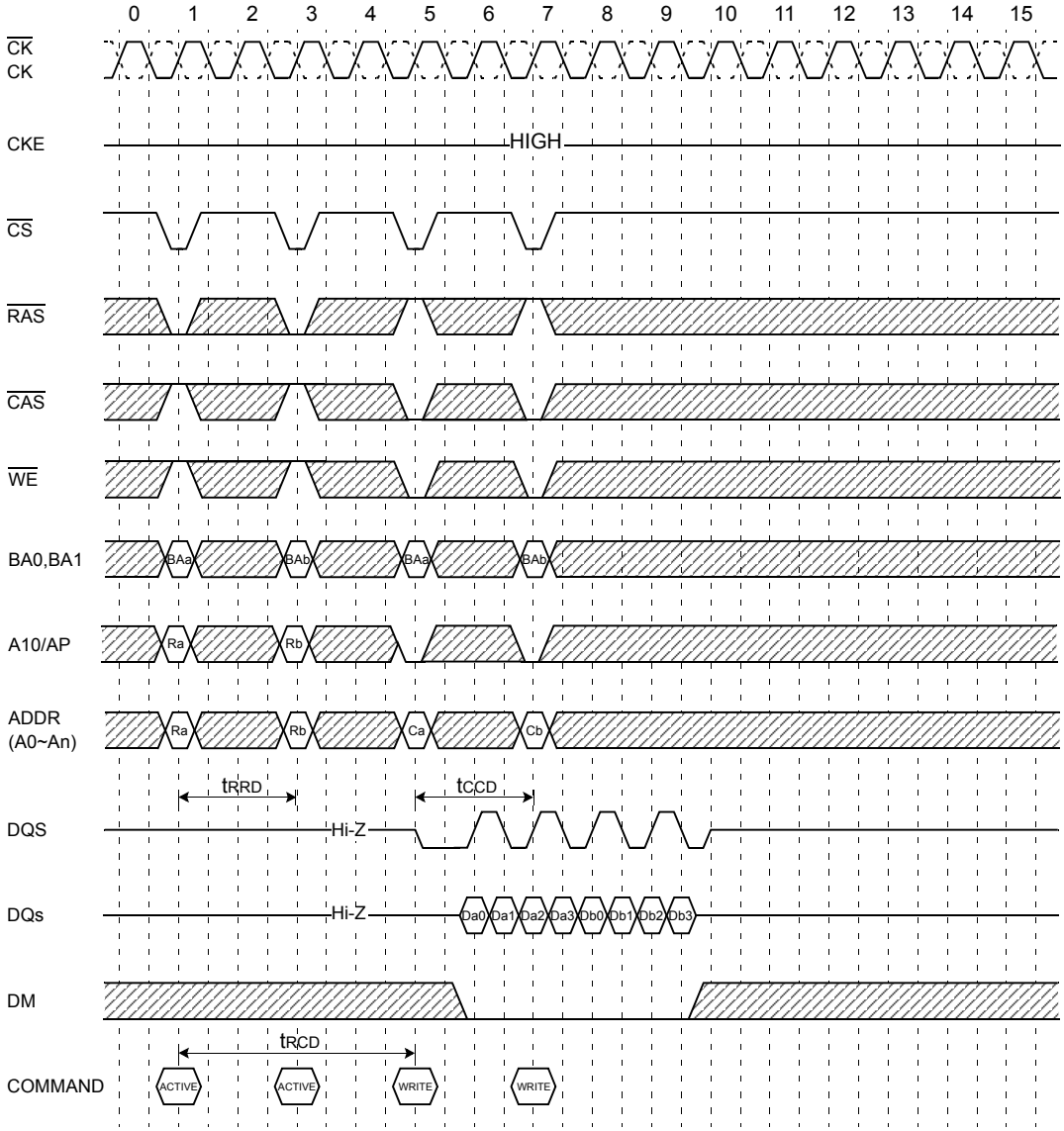
23. Multi Bank Interleaving READ

Figure 20. Multi Bank Interleaving READ (@BL=4, CL=3)



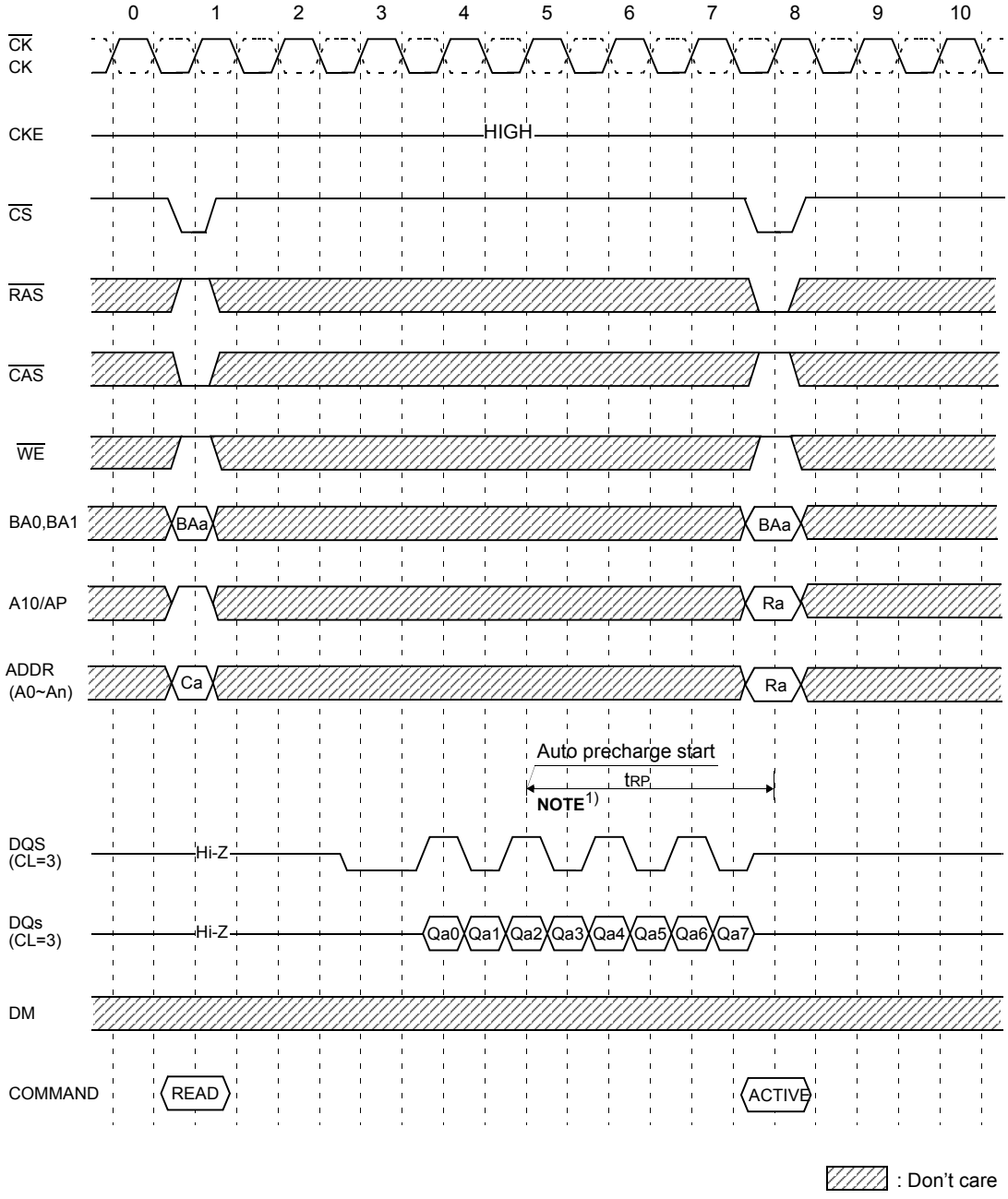
24. Multi Bank Interleaving WRITE

Figure 21. Multi Bank Interleaving WRITE (@BL=4)



25. Read with Auto Precharge

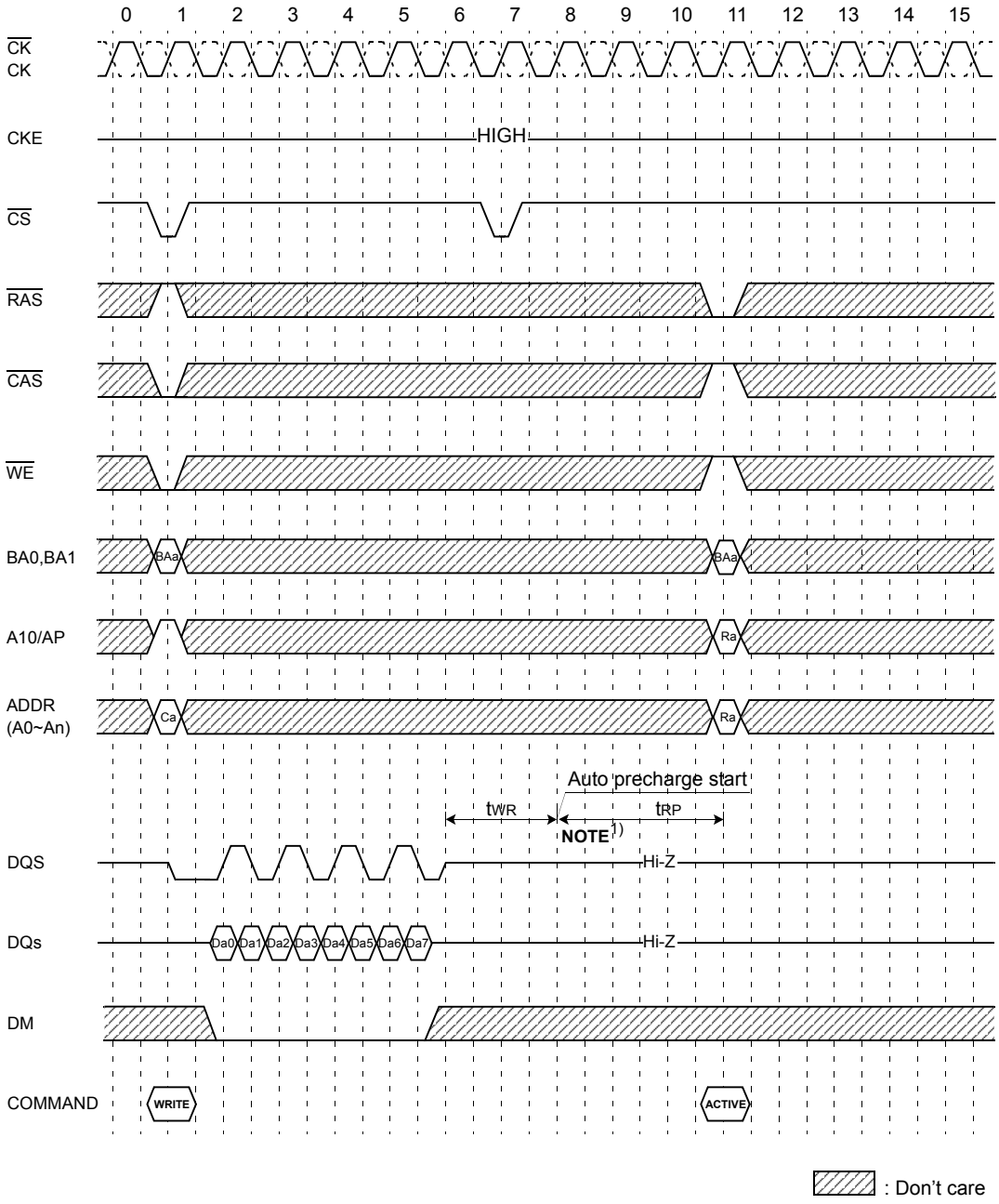
Figure 22. Read with Auto Precharge (@BL=8)



NOTE :
1) The row active command of the precharge bank can be issued after tRP from this point.

26. Write with Auto Precharge

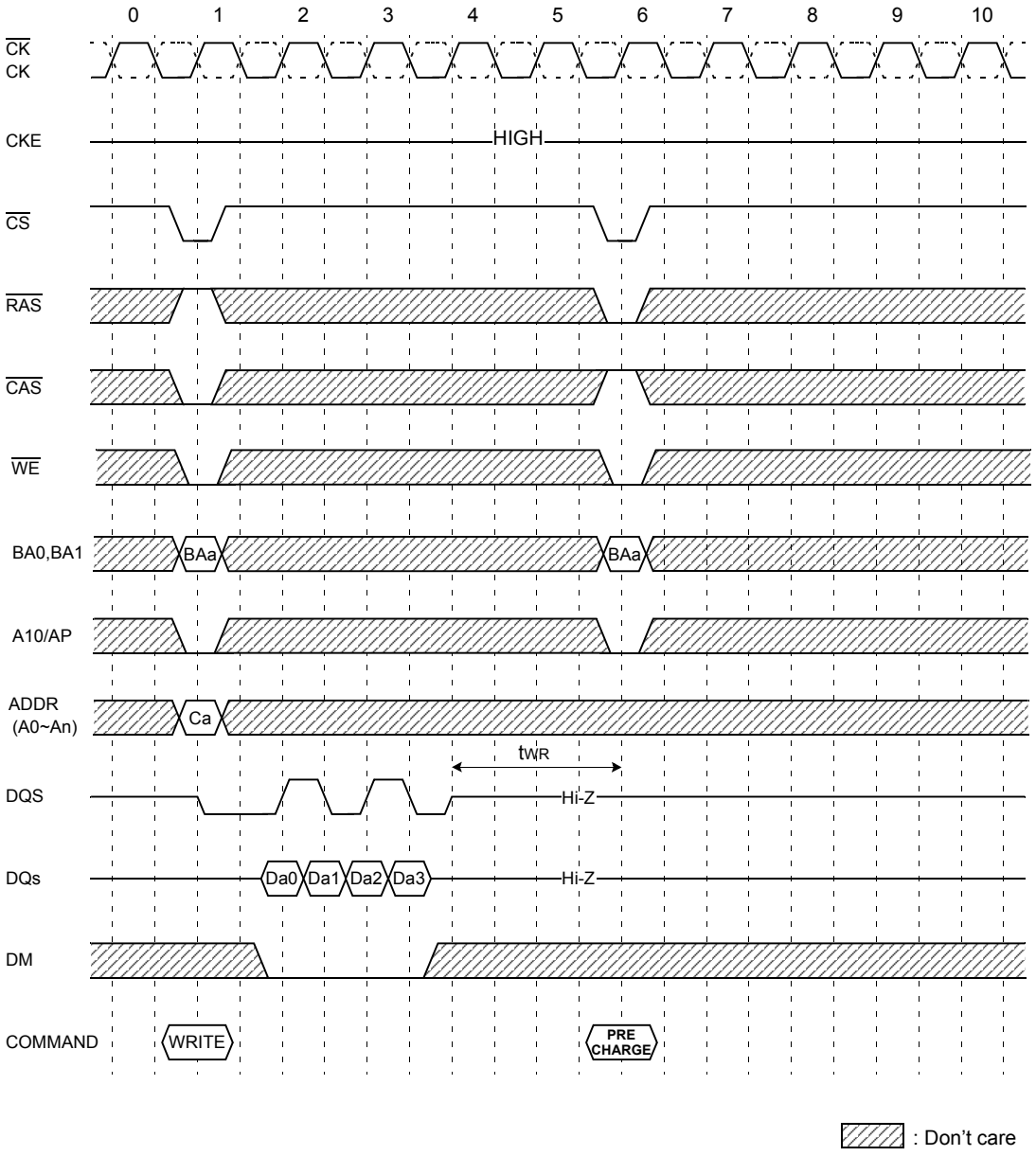
Figure 23. Write with Auto Precharge (@BL=8)



NOTE :
1) The row active command of the precharge bank can be issued after tRP from this point

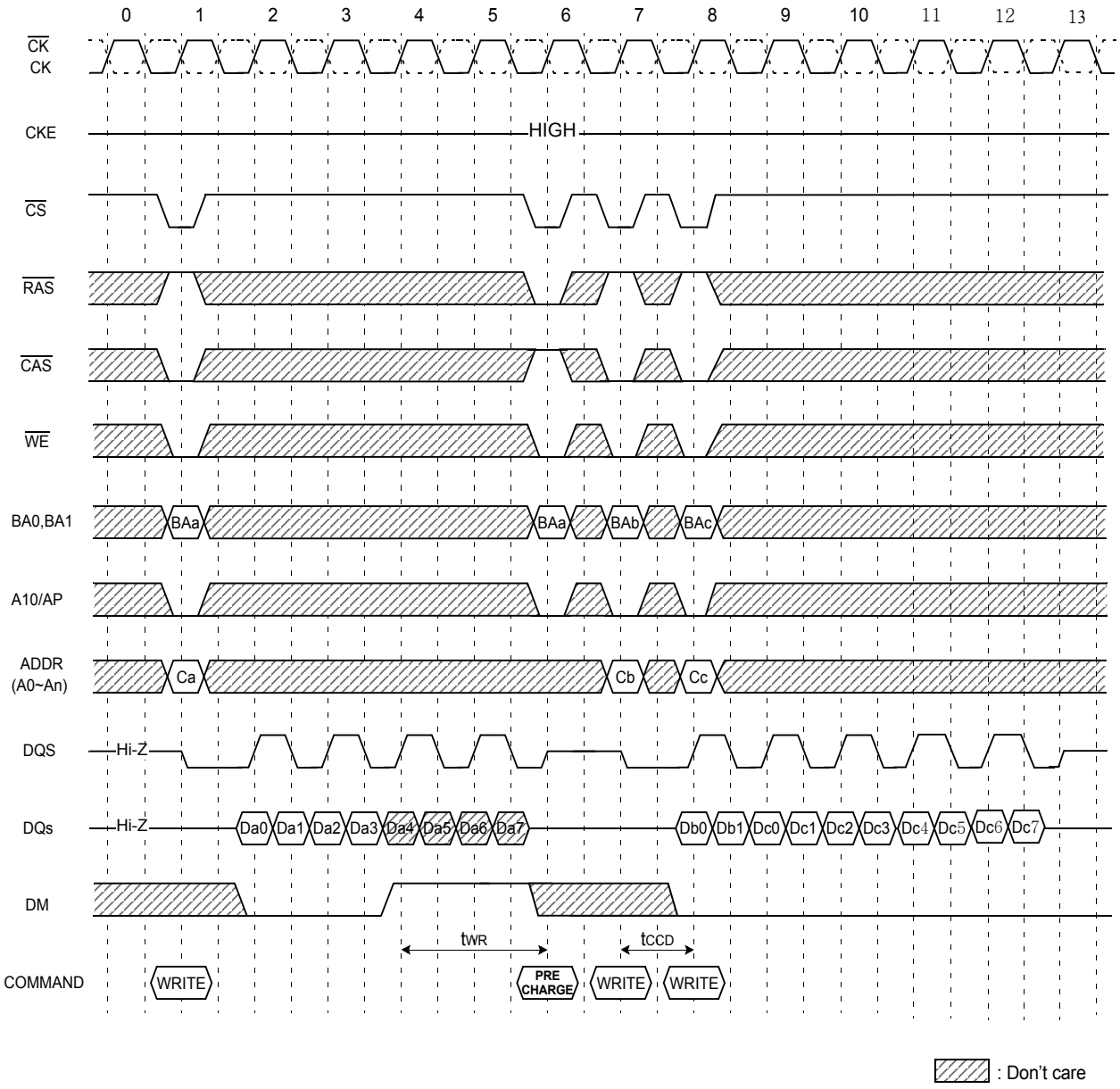
27. Write followed by Precharge

Figure 24. Write followed by Precharge (@BL=4)



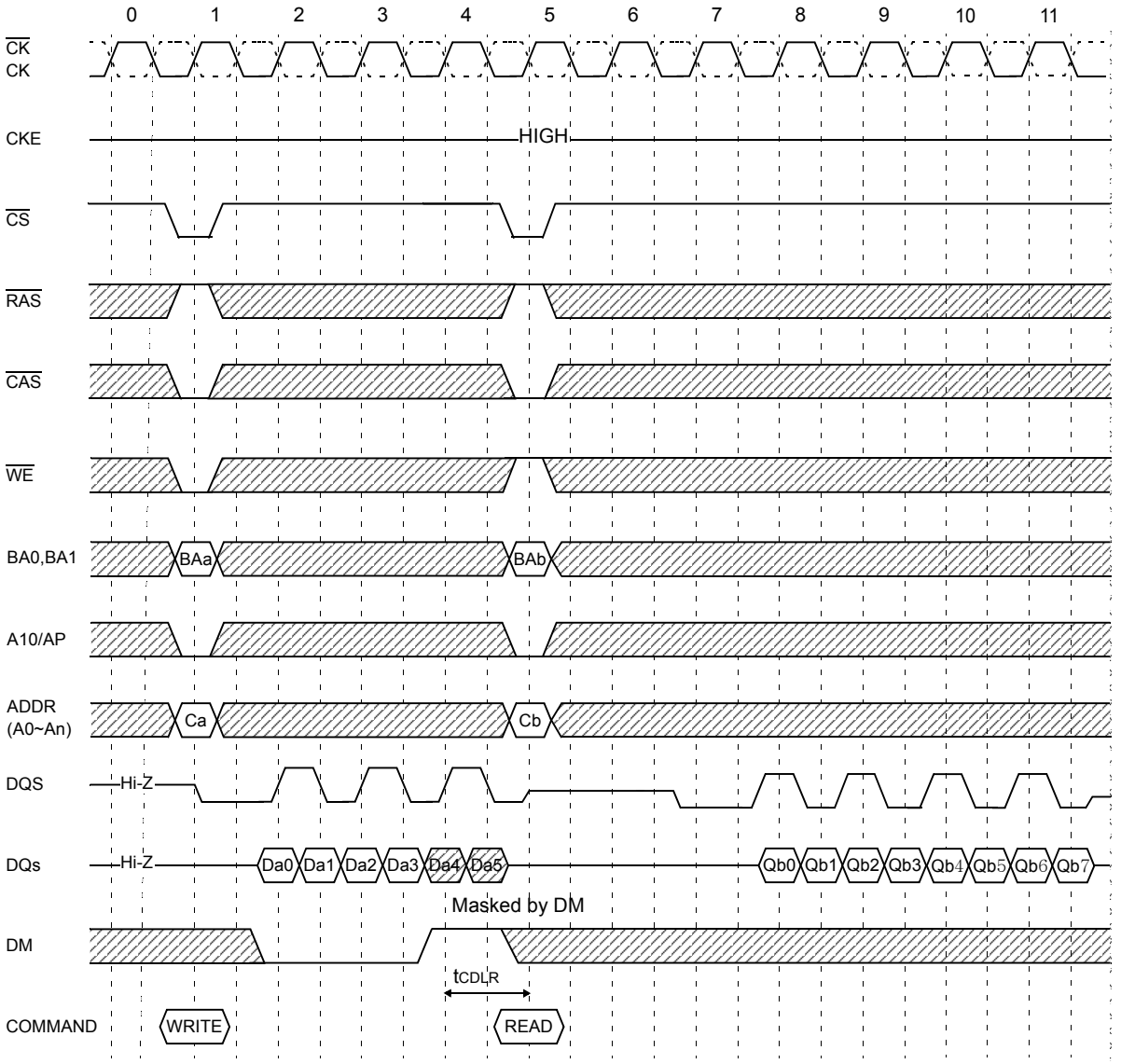
28. Write Interrupted by Precharge & DM

Figure 25. Write Interrupted by Precharge & DM (@BL=8)



29. Write Interrupted by a Read

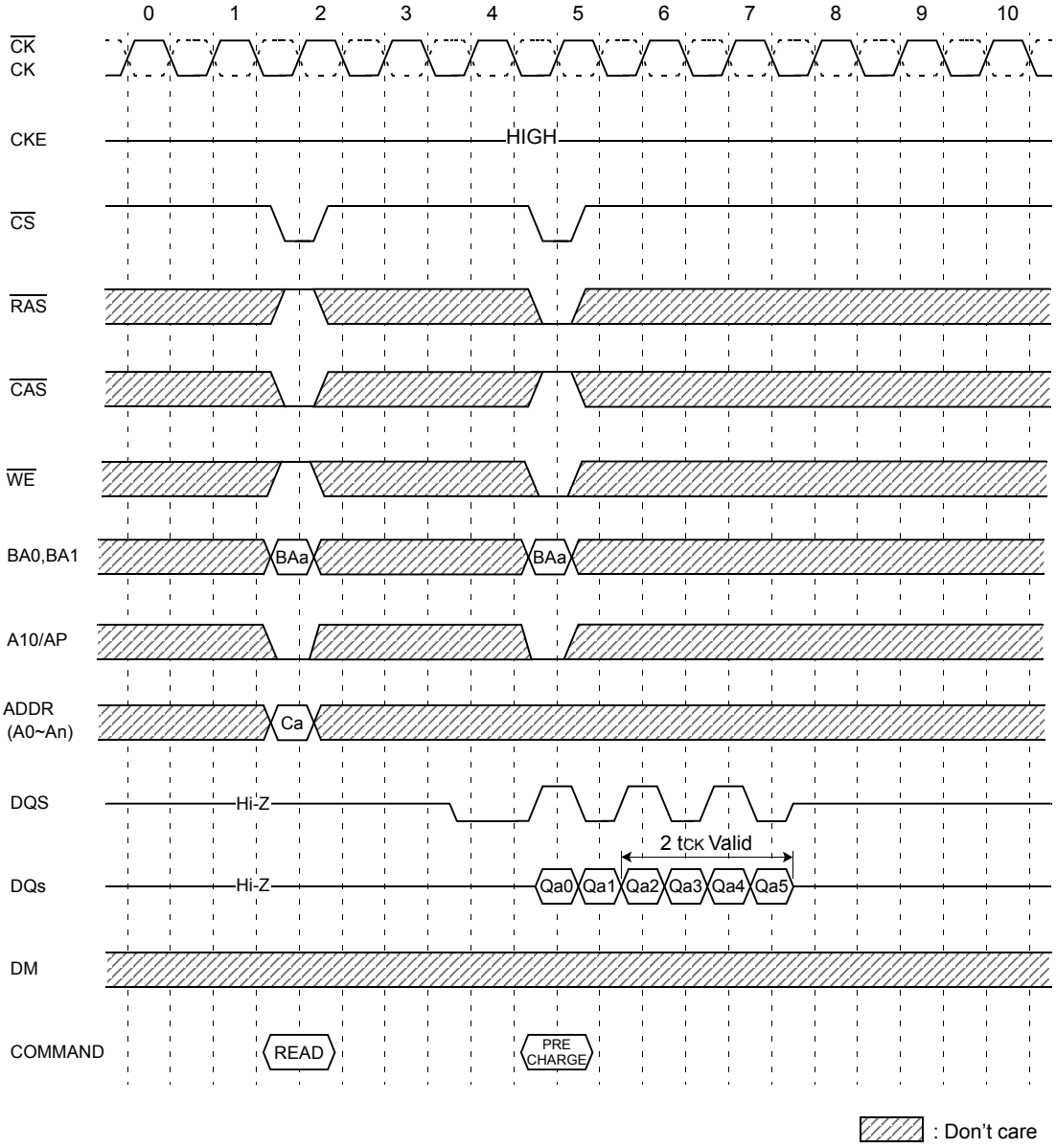
Figure 26. Write Interrupted by a Read (@BL=8, CL=3)



: Don't care

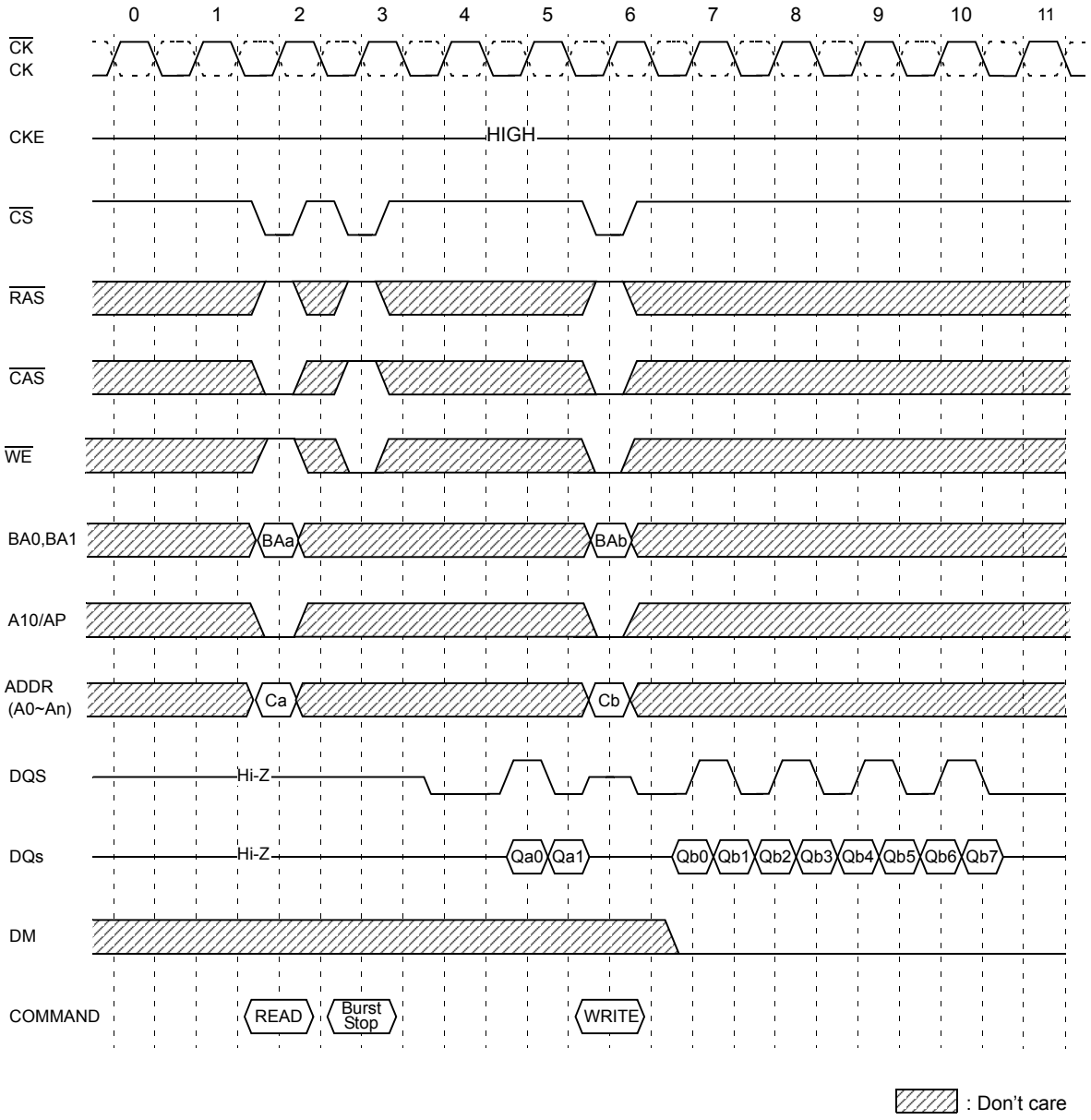
30. Read Interrupted by Precharge

Figure 27. Read Interrupted by Precharge (@BL=8, CL=3)



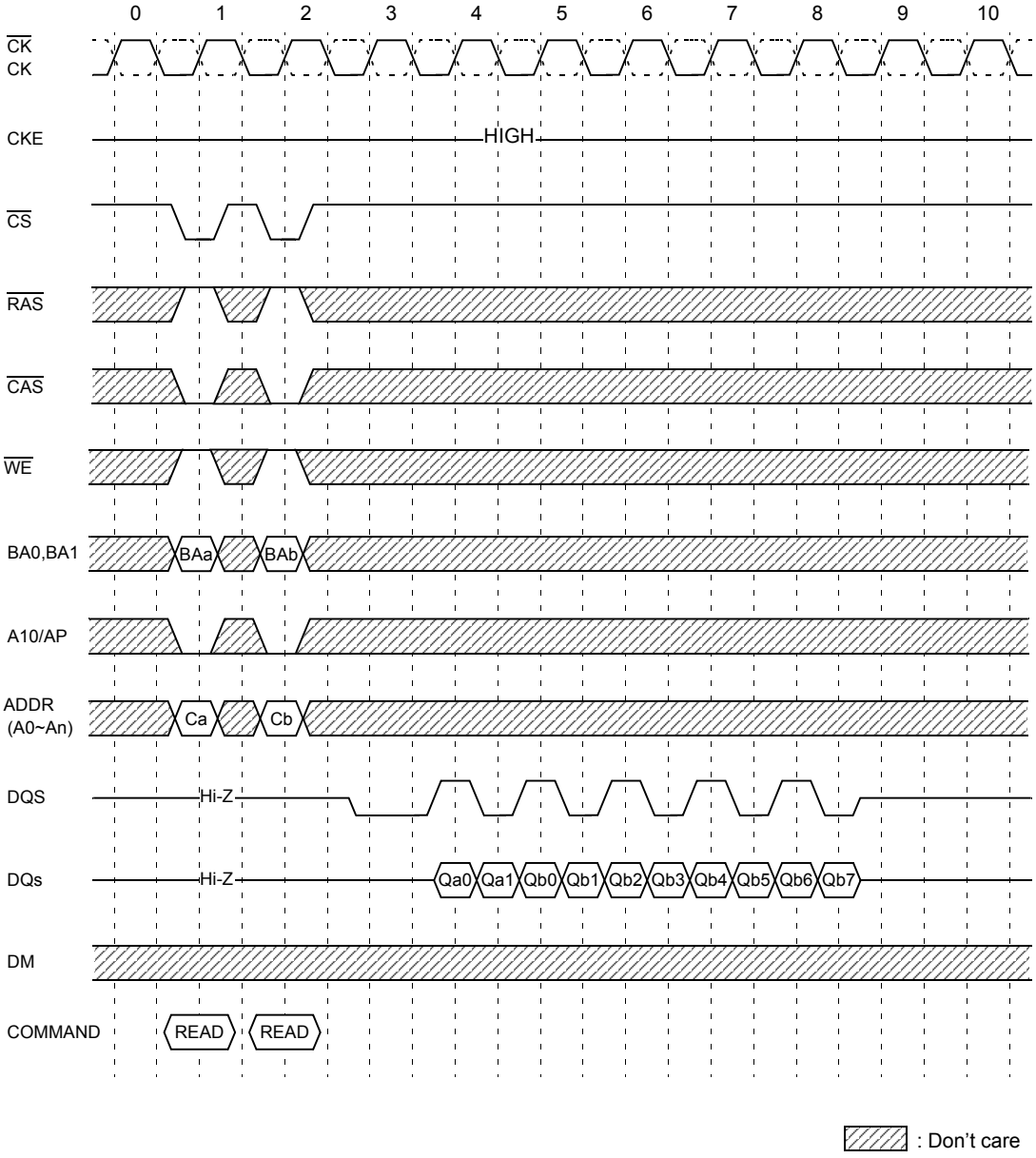
31. Read Interrupted by a Write & Burst Stop

Figure 28. Read Interrupted by a Write & Burst Stop (@BL=8, CL=3)



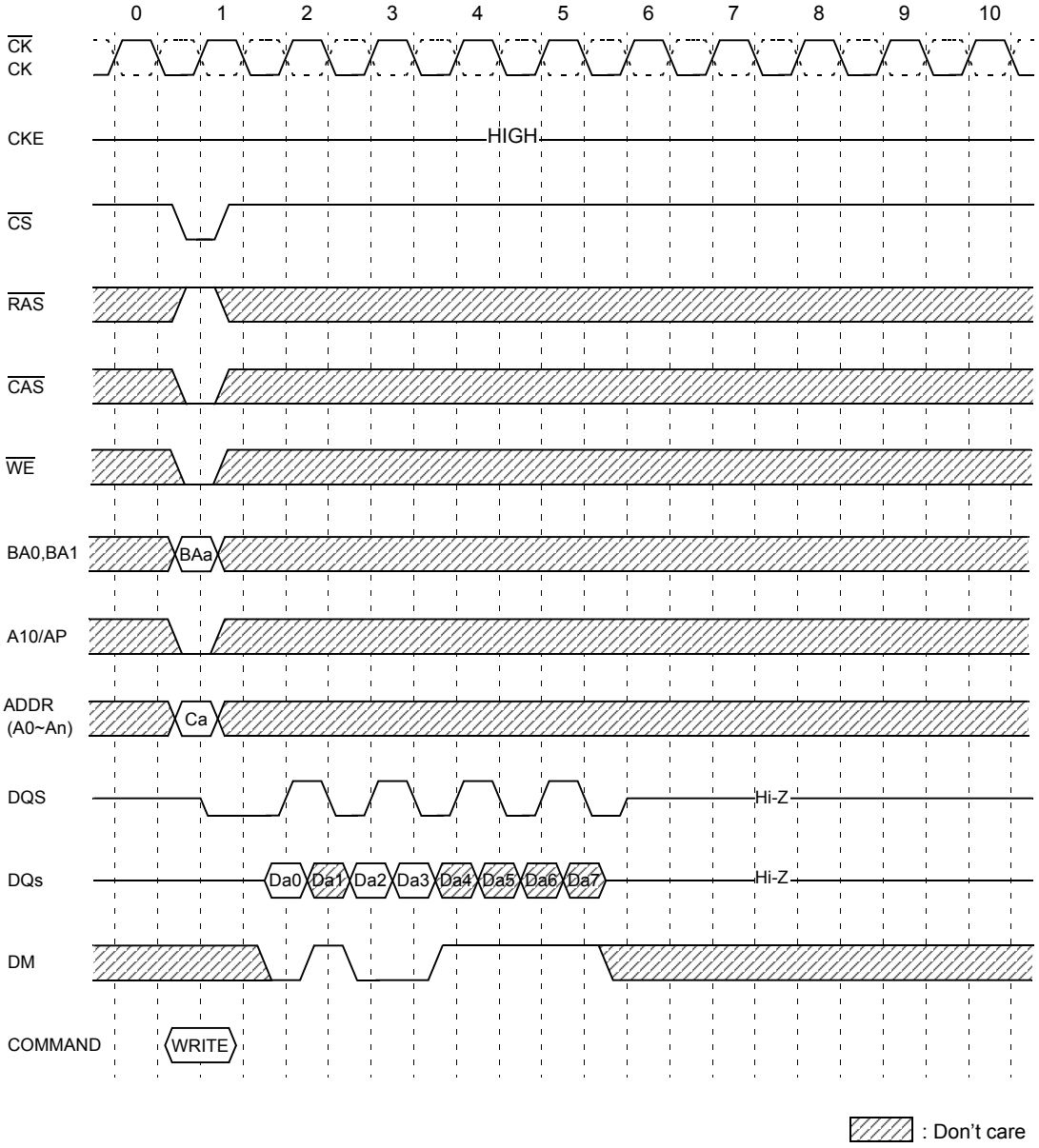
32. Read Interrupted by a Read

Figure 29. Read Interrupted by a Read (@BL=8, CL=3)



33. DM Function

Figure 30. DM Function (@BL=8) only for write



34. Mode Register Set

Figure 31. Mode Register Set