DATA SHEET

(DOC No. HX8262-A-DS)

HX8262-A

1200 CH TFT LCD Source Driver with TCON

Preliminary version 00 December, 2007

Himax Technologies, Inc.
http://www.himax.com.tw

1. General Description

HX8262-A is a 1200 channel outputs source driver with TCON, and 3-wire Serial Port Interface. It also supports 2-chip cascade mode to extend source channel to be 2400 channels (resolution: 800RGB x 600).

The interface follows digital 24-bit parallel RGB input format. The TCON generates the 400x240, 800x480 and 800x600 resolutions and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales.

The source driver receives 6-bit by 3 dots of digital display data per clock from TCON and generates corresponding 64-level gray scale voltage output. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation. Therefore, a high quality display with less crosstalk can be achieved.

2. Features

TCON

- Support display resolution 400x240, 800x480 and 800x600.
- Support digital 24-bit parallel RGB input mode
- Internal dithering 8-bit data to 6-bit data for Source Driver Circuit
- Only support stripe types of panel group
- Operation frequency: 40 MHz max
- Provide source and gate drivers control timing
- Provide flip and mirror scan control
- Operation Voltage Level 2.7V to 3.6V

Source Driver

- 1200 channels output source driver for TFT LCD panel
- Dynamic output range: 0.1 to VDDA-0.1V
- Dot inversion driving scheme
- Right and left shift capability
- LCD power: 6.5 to 13.5V
- Programmable gamma correction curve
- Support OTP function for gamma setting

PWM

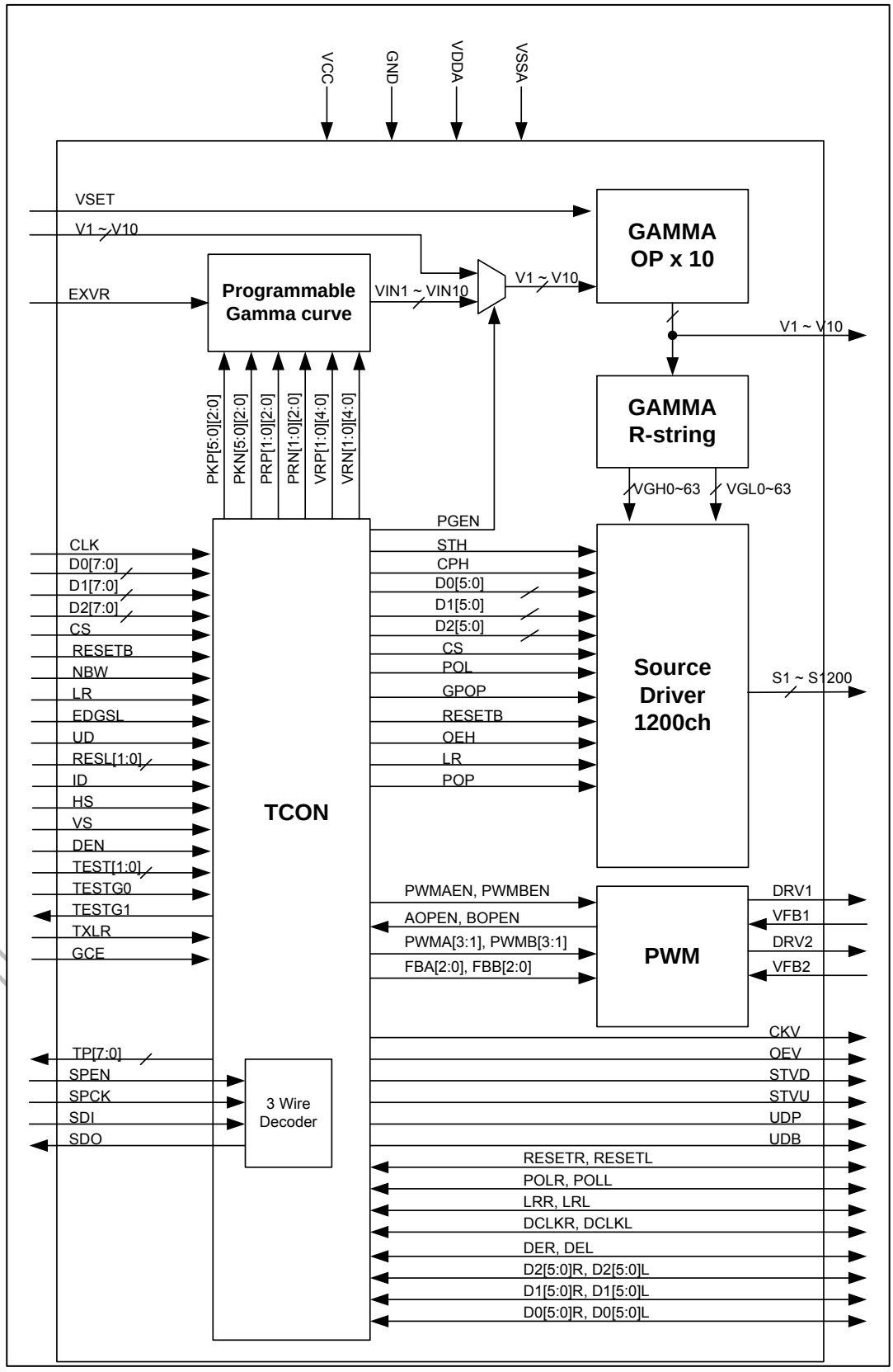
- 1st PWM to generate power for LED backlight
- 2nd PWM to generate VDDA power

Others

- COG package

3. Block Diagram

3.1 Whole chip block diagram



3.2 Source driver block diagram

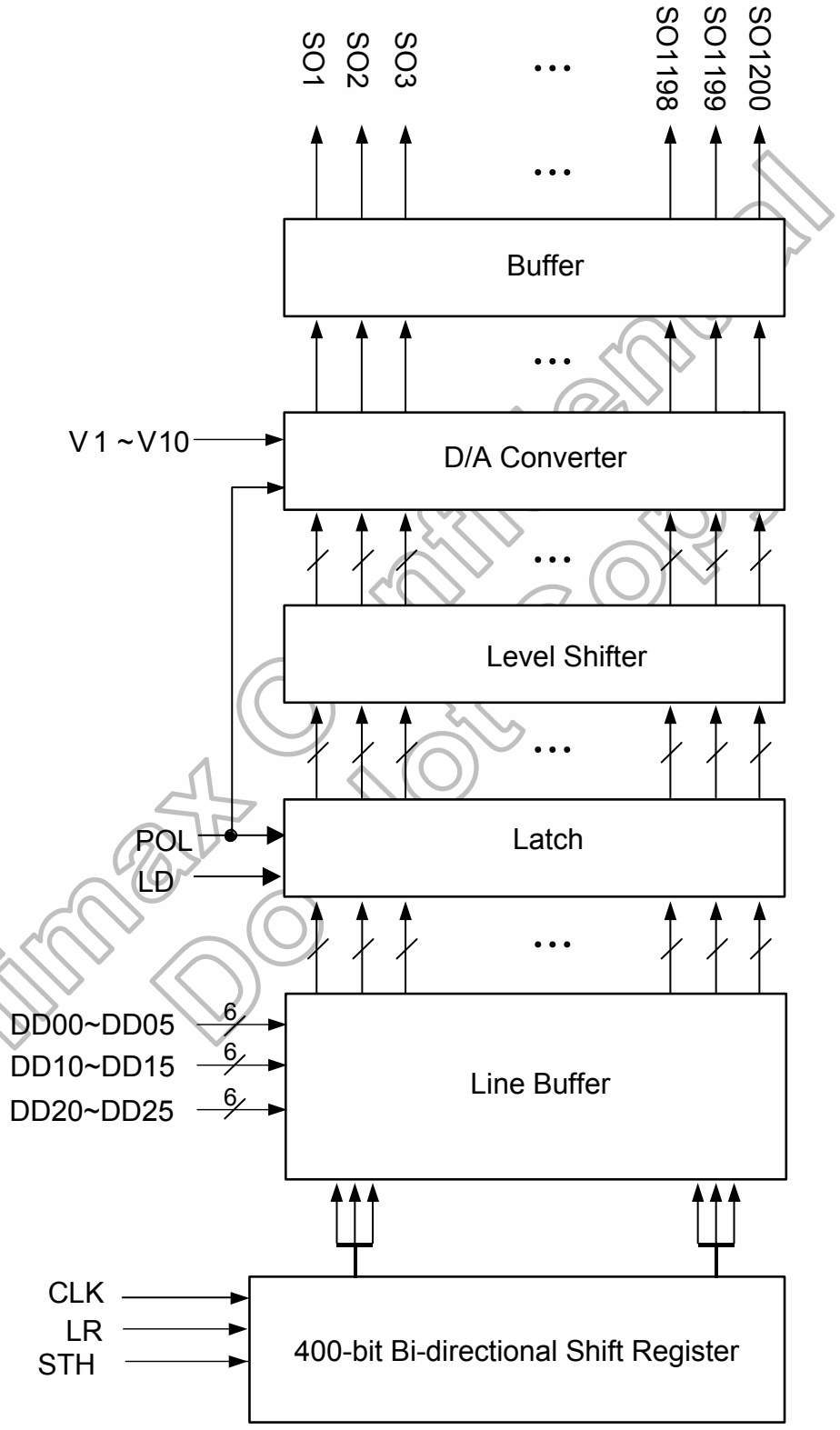


Figure 3. 2 Source driver block diagram

4. Pin description

Pin name	I/O	Description
CLK	I	Clock signal. User can input different polarity CLK by EDGSL setting. (Default pull low)
DCLKR	I/O	Cascade clock signal. User can input different polarity CLK by EDGSL setting. Detail refer to Table5.3
DCLKL	I/O	Cascade clock signal. User can input different polarity CLK by EDGSL setting. Detail refer to Table5.3
D07~D00 D17~D10 D27~D20	I	Digital data input. Dx0 is LSB and Dx7 is MSB. (Default pull low). D0x, D1x, and D2x indicate R, G, and B data in turn. When disable dithering function, please use Dx7~Dx2 as 6-bit input.
D05R~D00R D15R~D10R D25R~D20R	I/O	Cascade digital data input. Dx0R is LSB and Dx5R is MSB. D0xR, D1xR, and D2xR indicate R, G, and B data in turn. Detail refer to Table5.3
D05L~D00L D15L~D10L D25L~D20L	I/O	Cascade digital data input. Dx0L is LSB and Dx5L is MSB. D0xL, D1xL, and D2xL indicate R, G, and B data in turn. Detail refer to Table5.3
DE	I	Input data enable control. When DE mode, active High to enable data input. (Default pull low).
DER	I/O	Cascade DE signal Detail refer to Table5.3
DEL	I/O	Cascade DE signal Detail refer to Table5.3
RESETB	I	Hardware global reset. Low active. (Default pull high).
CKV_RESETR	I/O	CKV output or RESET I/O, detail refer to Table5.3
CKV_RESETL	I/O	CKV output or RESET I/O, detail refer to Table5.3
UDP_POLR	I/O	UDP output or POL I/O, referring to Table5.3 for the detail. If it is used as UDP output, then UDP equal to UD.
UDB_POLL	I/O	UDB output or POL I/O, referring to Table5.3 for the detail. If it is used as UDP output, then UDP equal to inverse UD.
LR	I	Shift direction of HX8262-A Source Driver internal shift register is controlled by this pin as shown below: LR=H: SO1→• • •→SO1200 (default pull high) LR=L: SO1200→• • •→SO1
OEV_LRR	I/O	OEV output or LR I/O, detail refer to Table5.3
OEV_LRL	I/O	OEV output or LR I/O, detail refer to Table5.3

TXLR	I	TXLR=H, DxxL -> DxxR. (default pull high) TXLR=L, DxxL <- DxxR.
NBW	I	NBW=H, normally black panel. NBW=L, normally white panel. (default pull low)
UD	I	Gate Driver Up/down scan setting. When UD=H, reverse scan. When UD=L, normal scan. (Default pull low).
CS	I	Charge share function control. CS=L, disable charge share function. CS=H, enable charge share function. (Default pull high).
HS	I	Horizontal sync input in digital parallel RGB. (Default pull high)
VS	I	Vertical sync input in digital parallel RGB. (Default pull high).
RESL[1:0]	I	Control the resolution selection. RESL[1:0] / Resolution 00 / 800x480 (Default) 01 / 800x600 1x / 400x240
VSET	I	Gamma correction voltage can be set to input 4 voltage levels or 10 voltage levels externally. VSET=L, only externally input V1, V5, V6 and V10 reference voltage are available, others are generated by internal resistors. VSET=H, externally input V1~V10 reference voltage are available. No matter what setting, it doesn't need OPA buffer to the reference inputs. (default pull high)
GCE	I	Gamma V1~V10 cascade enable. L: Direct connect V1 ~ V10 from FPC. H: Enable Master to Slave cascade V1~V10.
EDGSL	I	Define input clock polarity When EDGSL=L, latch data by rising edge of CLK. (default pull low) When EDGSL=H, CLK polarity is inverted, latch data by falling edge of CLK.
V1~V10	I/O	Used as reference voltage input pins. Holding the reference voltage fixed during the period of LCD driving output. To ensure the correct analog voltage is output from D/A converter, the V1~V10 must be stable before D/A conversion. VDDA>V1>V2>V3>V4>V5>V6>V7>V8>V9>V10>VSSA.

<table>
<tr><td>ID</td><td>I</td><td>Working with RESL[1:0], LR, TXLR
<table>
<tr><th colspan="6">TXLR=L</th></tr>
<tr><th colspan="2" rowspan="2">RESL[1:0]</th><th rowspan="2">ID</th><th colspan="2">Sample cycle</th><th rowspan="2">Channel Number</th></tr>
<tr><th>LR = H</th><th>LR = L</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1 ~ 400</td><td>401 ~ 800</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>401 ~ 800</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1 ~ 400</td><td>401 ~ 800</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>401 ~ 800</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
</table>
<table>
<tr><th colspan="6">TXLR=H</th></tr>
<tr><th colspan="2" rowspan="2">RESL[1:0]</th><th rowspan="2">ID</th><th colspan="2">Sample cycle</th><th rowspan="2">Channel Number</th></tr>
<tr><th>LR = H</th><th>LR = L</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>401 ~ 800</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1 ~ 400</td><td>401 ~ 800</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>401 ~ 800</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1 ~ 400</td><td>401 ~ 800</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
</table></td></tr>
<tr><td>SPCK</td><td>I</td><td>Serial port Clock. (Default pull high).</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial port Data input. (Default pull high).</td></tr>
<tr><td>SPEN</td><td>I</td><td>Serial port Data Enable Signal. (Default pull high) and active low.</td></tr>
<tr><td>SDO</td><td>O</td><td>3-Wire serial bus data output</td></tr>
<tr><td>CKV</td><td>O</td><td>Gate driver clock.</td></tr>
<tr><td>OEV</td><td>O</td><td>Enable output control of gate driver.</td></tr>
<tr><td>STVD</td><td>O</td><td>Start pulse for gate driver.
When UD=L, STVD is output.
When UD=H, STVD is Hi-Z.</td></tr>
<tr><td>STVU</td><td>O</td><td>Start pulse for gate driver.
When UD=L, STVU is Hi-Z.
When UD=H, STVU is output.</td></tr>
<tr><td>SO1~SO1200</td><td>O</td><td>Output driver signal.</td></tr>
<tr><td>TEST[1:0]</td><td>I</td><td>Test pins. (Default pull low).</td></tr>
<tr><td>TESTG0</td><td>O</td><td>Test pins, it has to be pull low. (Default pull low)</td></tr>
<tr><td>TESTG1</td><td>I</td><td>Test pin and let it open.</td></tr>
</table>

DRV1	O	Power transistor gate signal for the boost converter 1. 1st PWM can be used for LED backlight power.
DRV2	O	Power transistor gate signal for the boost converter 2. 2nd PWM can be used to generate VDDA power if needed.
VFB1	I	Main booster regulator feedback input 1. Connect feedback resistive divider to GND. VFB default threshold is 0.6V
VFB2	I	Main booster regulator feedback input 2. Connect feedback resistive divider to GND. VFB default threshold is 0.6V
TP[7:0]	O	Test pins. These pins must be open.
VDDA	I	Analog power. 6.5V to 13.5V.
VSSA	I	Analog ground.
VCC	I	Digital power. 2.7V to 3.6V.
GND	I	Digital ground.
SHIELD	–	Connect to ground for noise shielding.
EXVR	I/O	Gamma reference voltage (default = 1/2 x VDDA)
PASS[4:1]	–	Internal link path

Note: (1) Please following the sequence to power on HX8262: VCC → logic input → VDDA and V1 ~ V10 and reverse the sequence to shut it down.

(2) To stabilize the supply voltages, please be sure to connect a 0.1uF bypass capacitor between VCC-GND and VDDA-VSSA. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01uF is also advised between the gamma-corrected power supply terminals (V1, V2, …, V10) and VSSA.

(3) Please keep V1~V10 not cross to the toggle signals as possible to avoid the AC coupling on the DC V1~V10 voltage. When used as cascade mode, please keep the coupled amount of V1~V10 are the same between the two chip.

(4) The input wiring resistance values affect power consumption, signal integrity and the display quality. Please ensure the total wiring resistance values that do not exceed those recommended as below.

Pin Name	Wiring RC value
VCC(3.3V)	R< 30 Ω
GND(0V)	R< 30 Ω
VDDA(8.4V)	R< 5 Ω
VSSA(0V)	R< 5 Ω
V1 ~ V10	R< 100 Ω
CLK	R< 100 Ω
Dx7 ~ Dx0	R< 100 Ω
HS	R< 200 Ω
VS	R< 200 Ω
DE	R< 200 Ω
Dx[5:0]R, Dx[5:0]L, x=2,1,0	R< 200 Ω and C<10pF
DCLKR, DCLKL	R< 200 Ω and C<10pF
DER, DEL	R< 200 Ω and C<10pF
OEV_LRR to OEV_LRL	R< 200 Ω and C<10pF
UDP_POLR to UDB_POLL	R< 200 Ω and C<10pF
CKV_RESETR to CKV_RESETL	R< 200 Ω and C<10pF
Others	R< 1000 Ω

5. Operation description

5.1 Relationship between input data and output channels

- **Source Driver**

LR	First					→		Last		
H	Out1	Out2	Out3	•••	•••	•••	•••	Out1198	Out1199	Out1200

LR	Last					←		First		
L	Out1200	Out1199	Out1198	•••	•••	•••	•••	Out3	Out2	Out1

Table 5. 1 Relationship between input data and output channels

5.2 HX8262-A configuration with TXLR, LR, ID, RESL0, RESL1

HX8262-A supports timing controllers for five resolutions. Since HX8262-A has 1200 channels, for example, two pieces of HX8262-A source drivers are cascaded and extended to 2400 channels of 800RGB. The configuration examples of the HX8262-A are illustrated as figure 5.1 ~ 5.12.

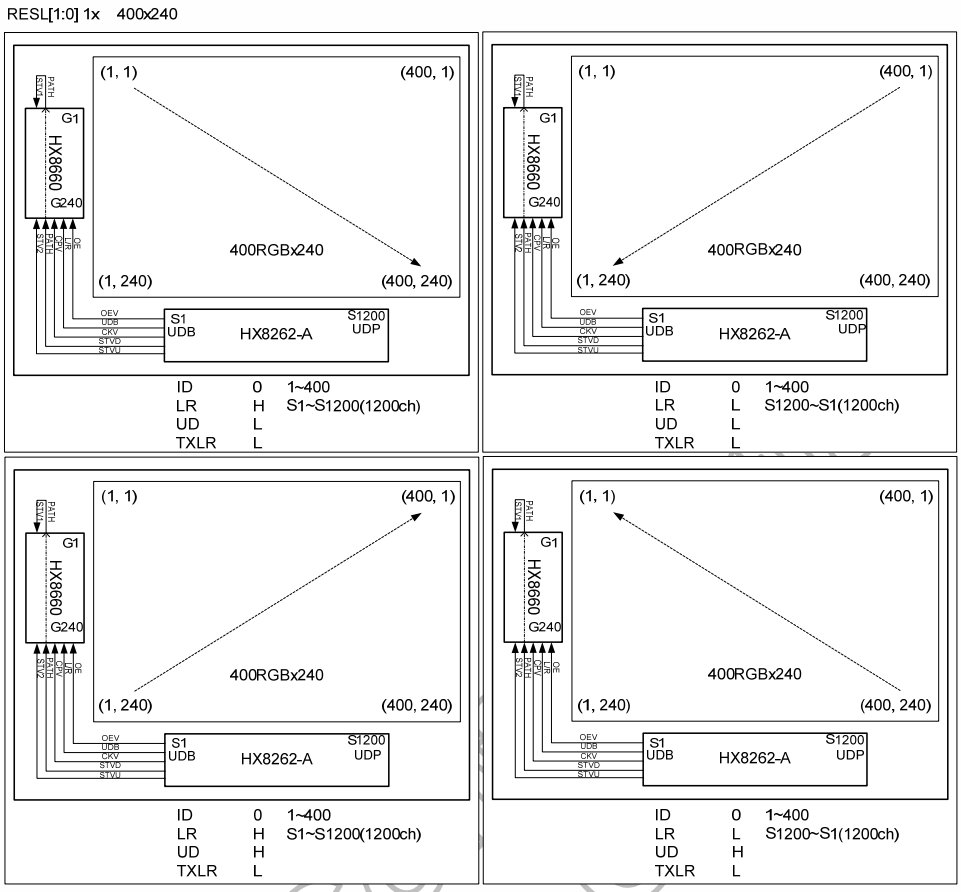


Figure 5.1 HX8262-A put down side and HX8660 put left side for 400RGB X 240

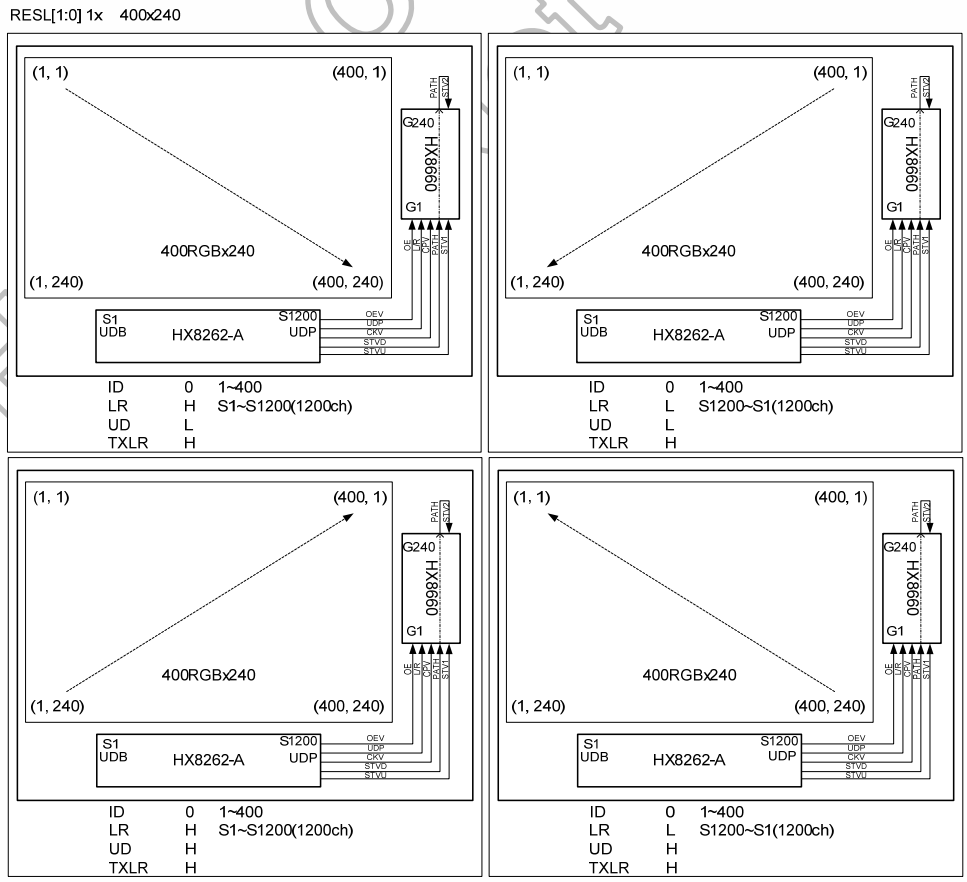


Figure 5.2 HX8262-A put down side and HX8660 put right side for 400RGB X 240

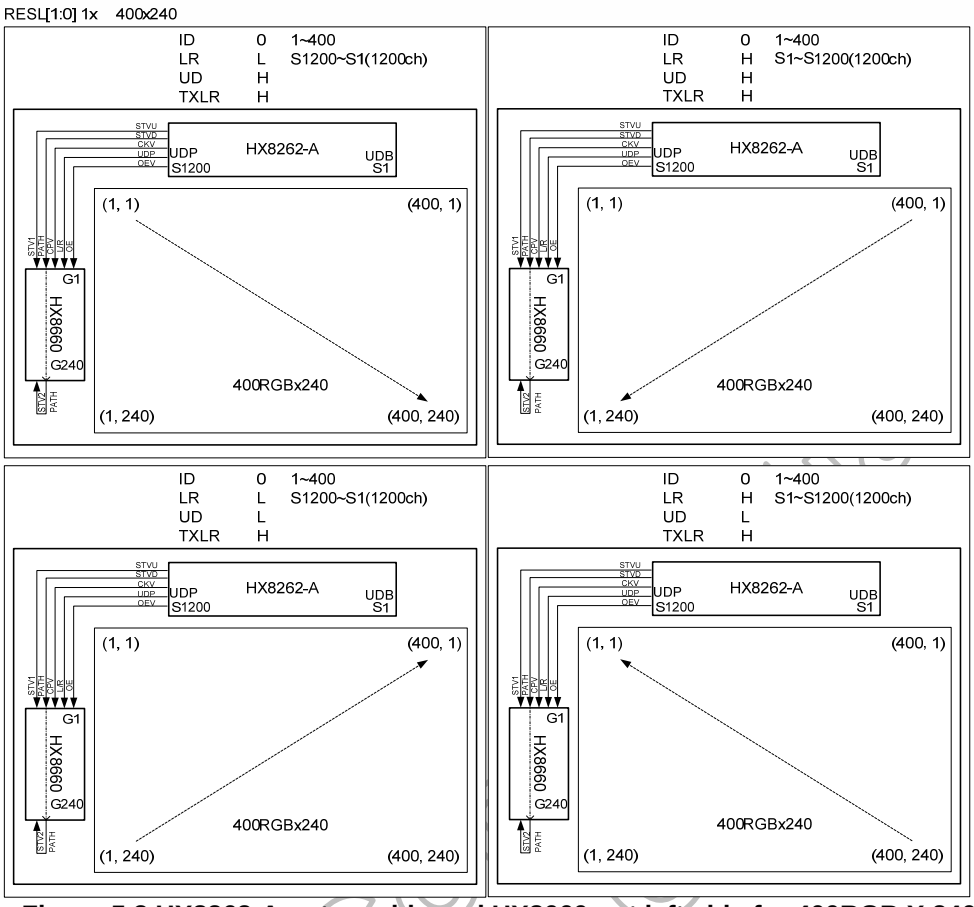


Figure 5.3 HX8262-A put up side and HX8660 put left side for 400RGB X 240

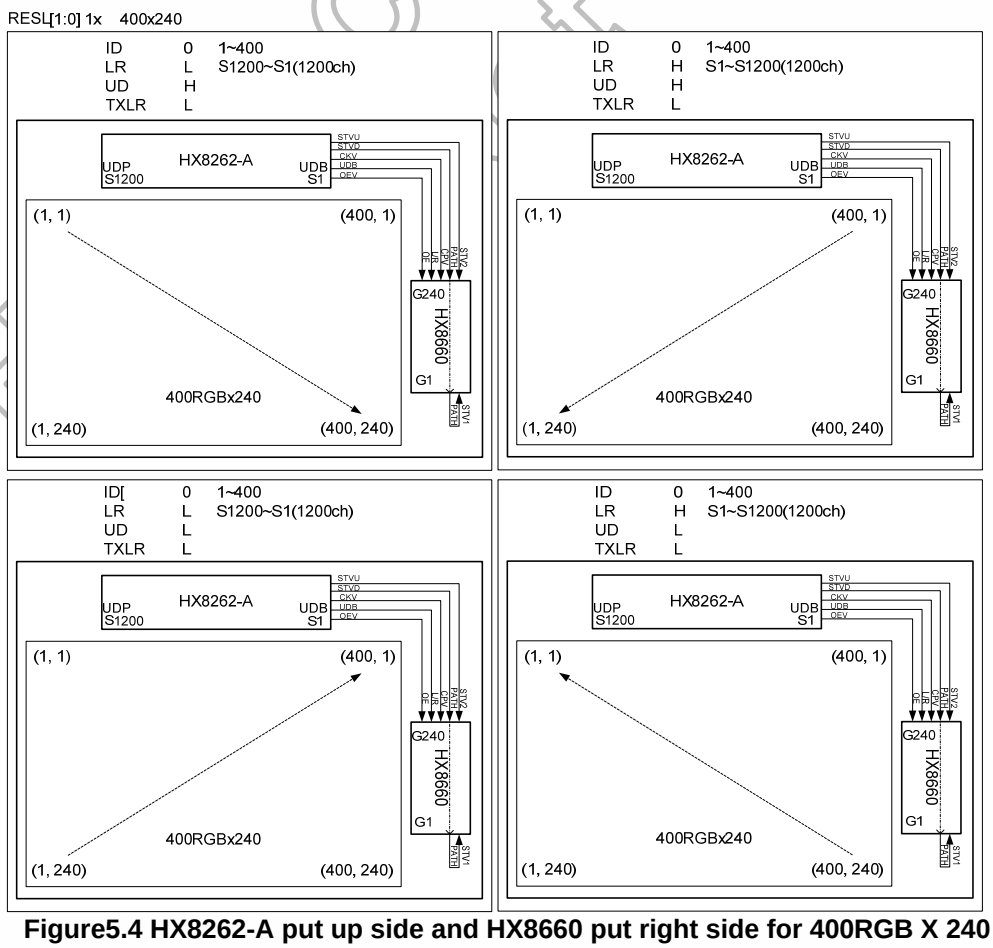


Figure5.4 HX8262-A put up side and HX8660 put right side for 400RGB X 240

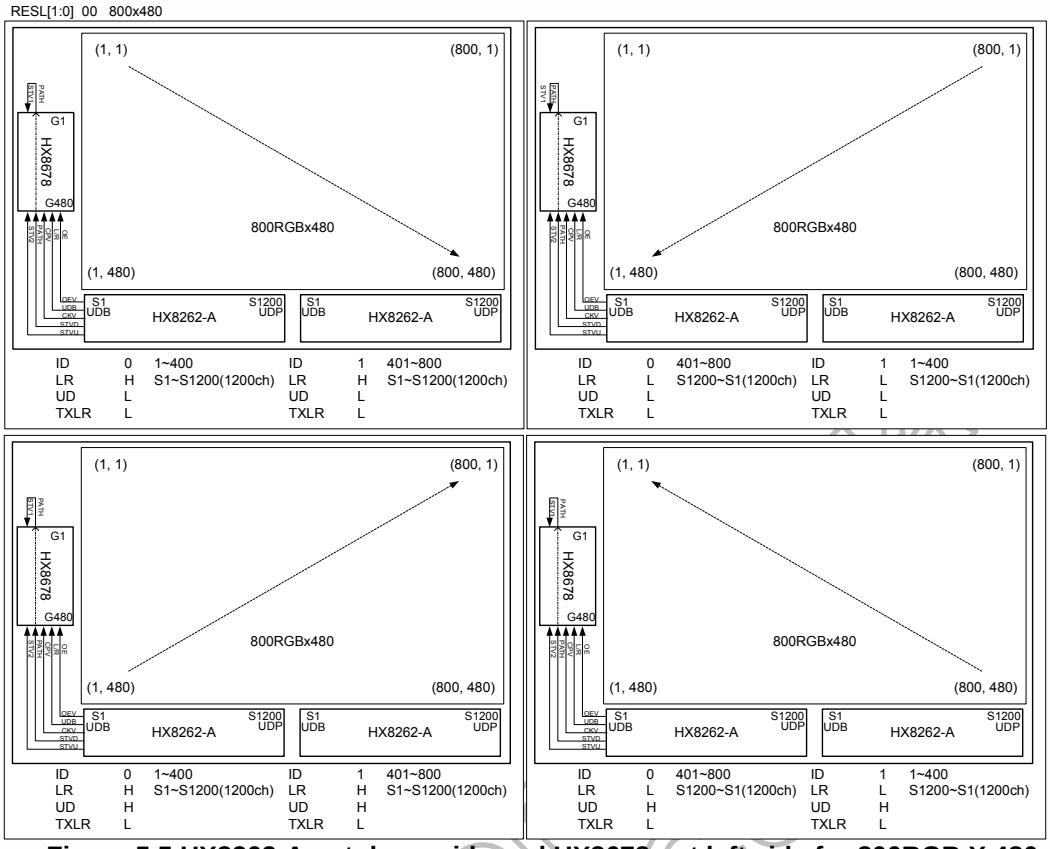


Figure 5.5 HX8262-A put down side and HX8678 put left side for 800RGB X 480

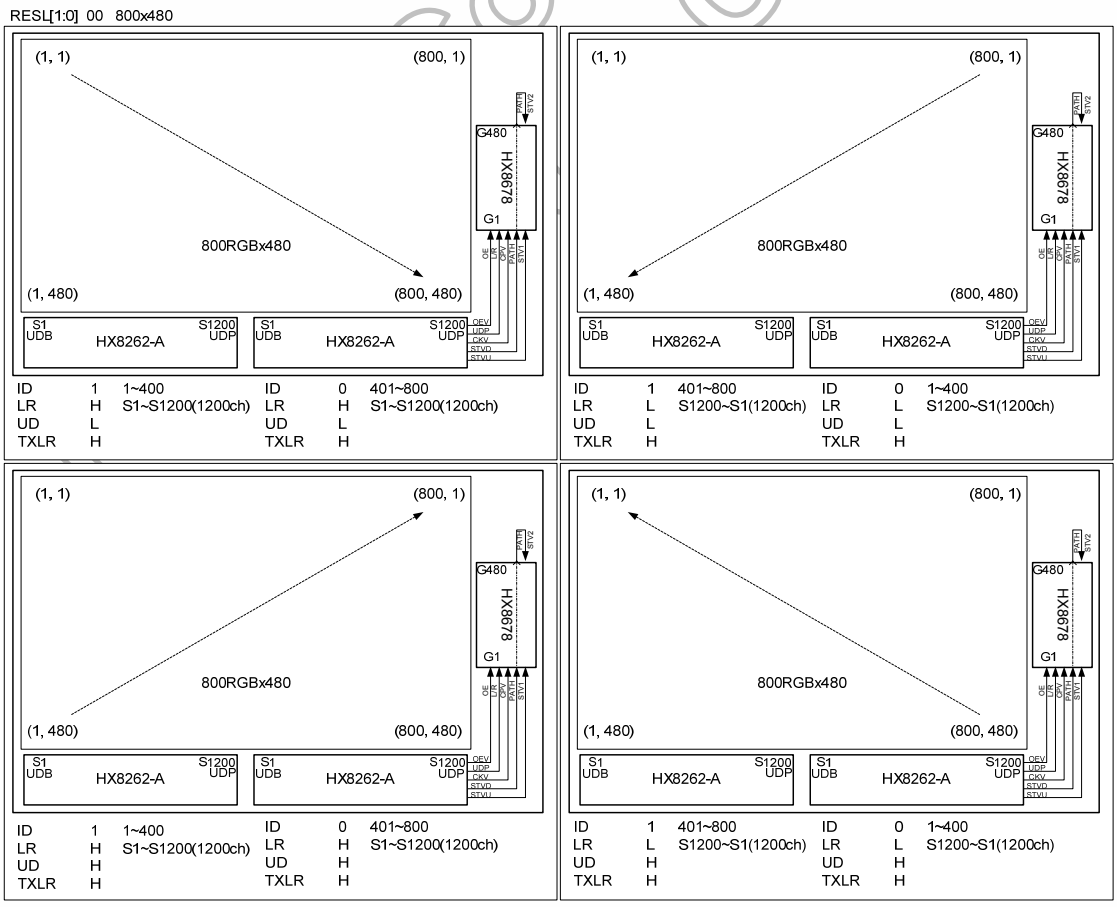


Figure 5.6 HX8262-A put down side and HX8678 put right side for 800RGB X 480

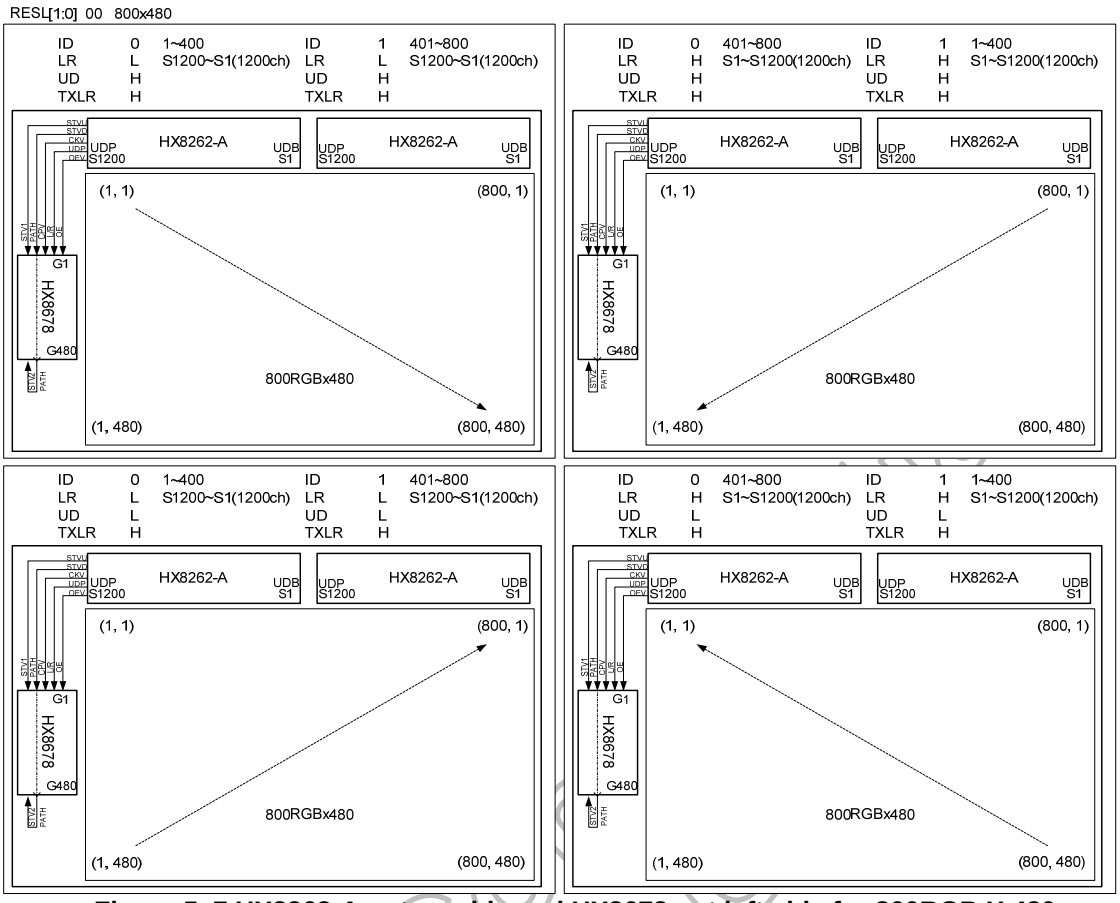


Figure 5. 7 HX8262-A put up side and HX8678 put left side for 800RGB X 480

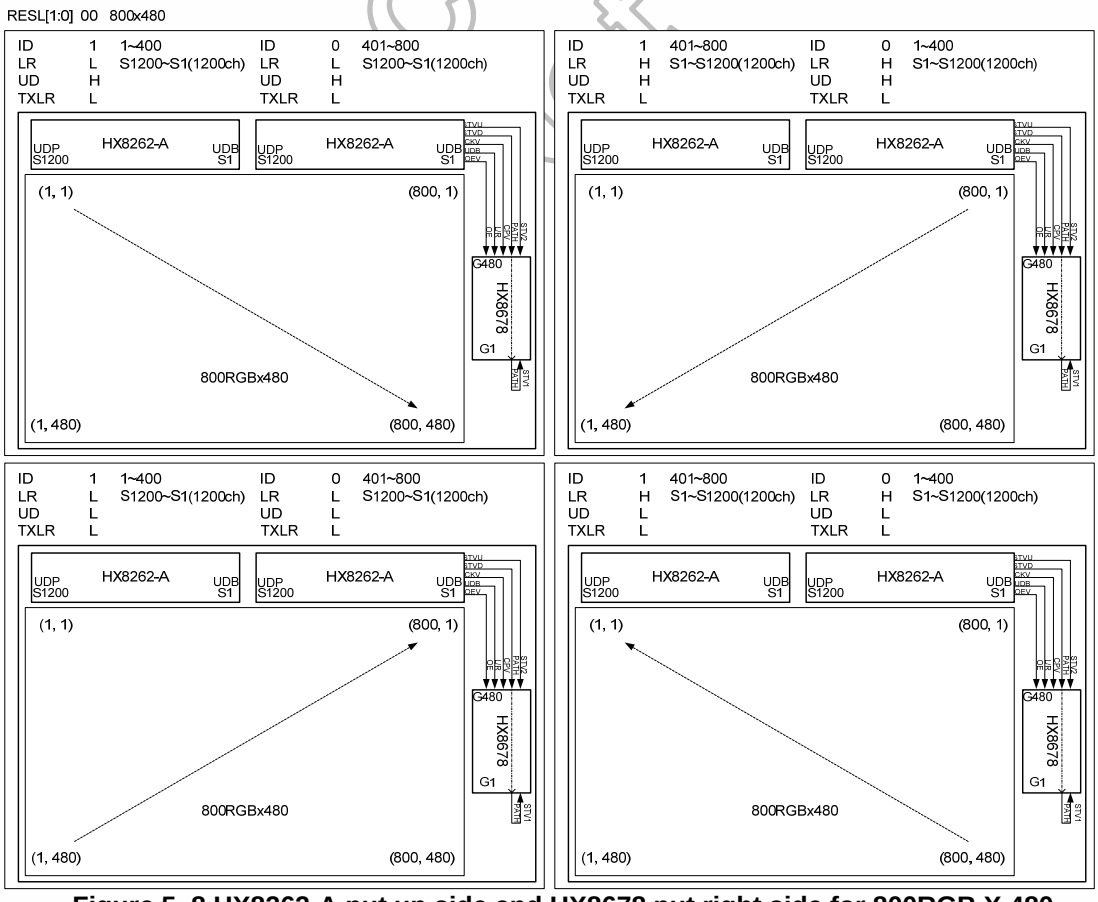


Figure 5. 8 HX8262-A put up side and HX8678 put right side for 800RGB X 480

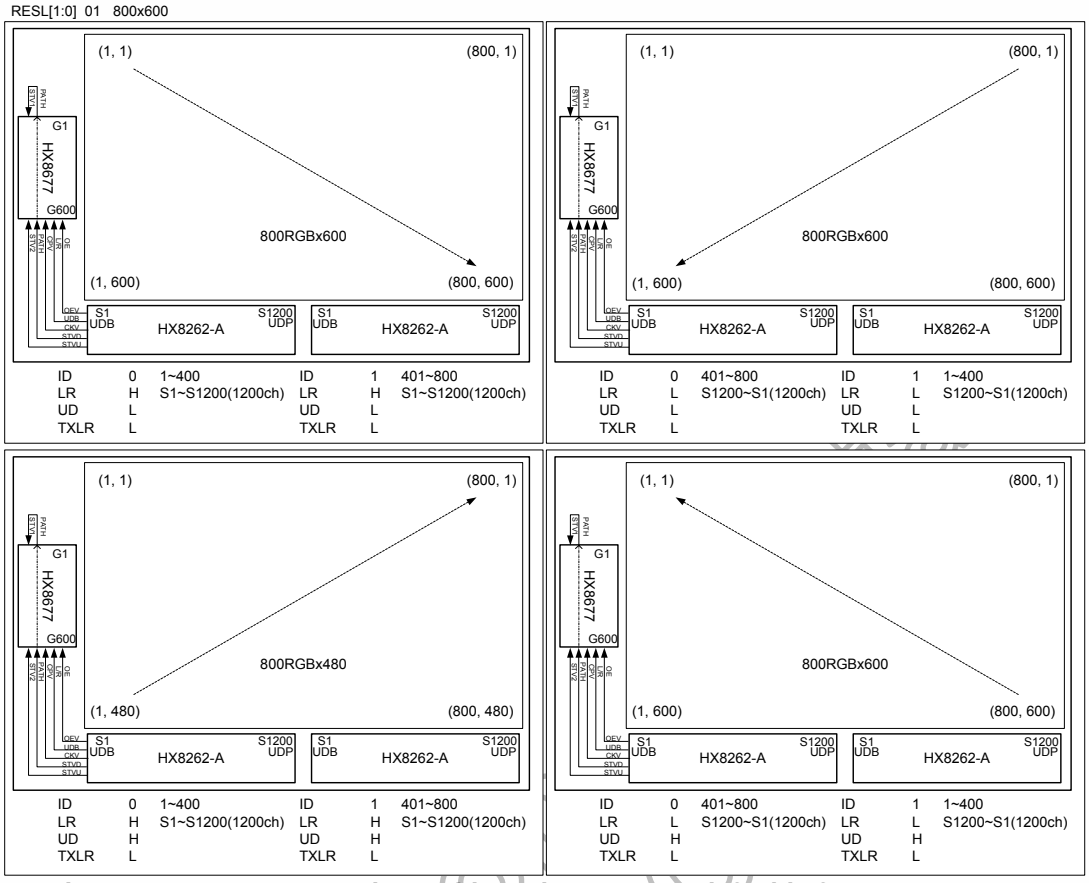


Figure 5.9 HX8262-A put down side and HX8677 put left side for 800RGB X 600

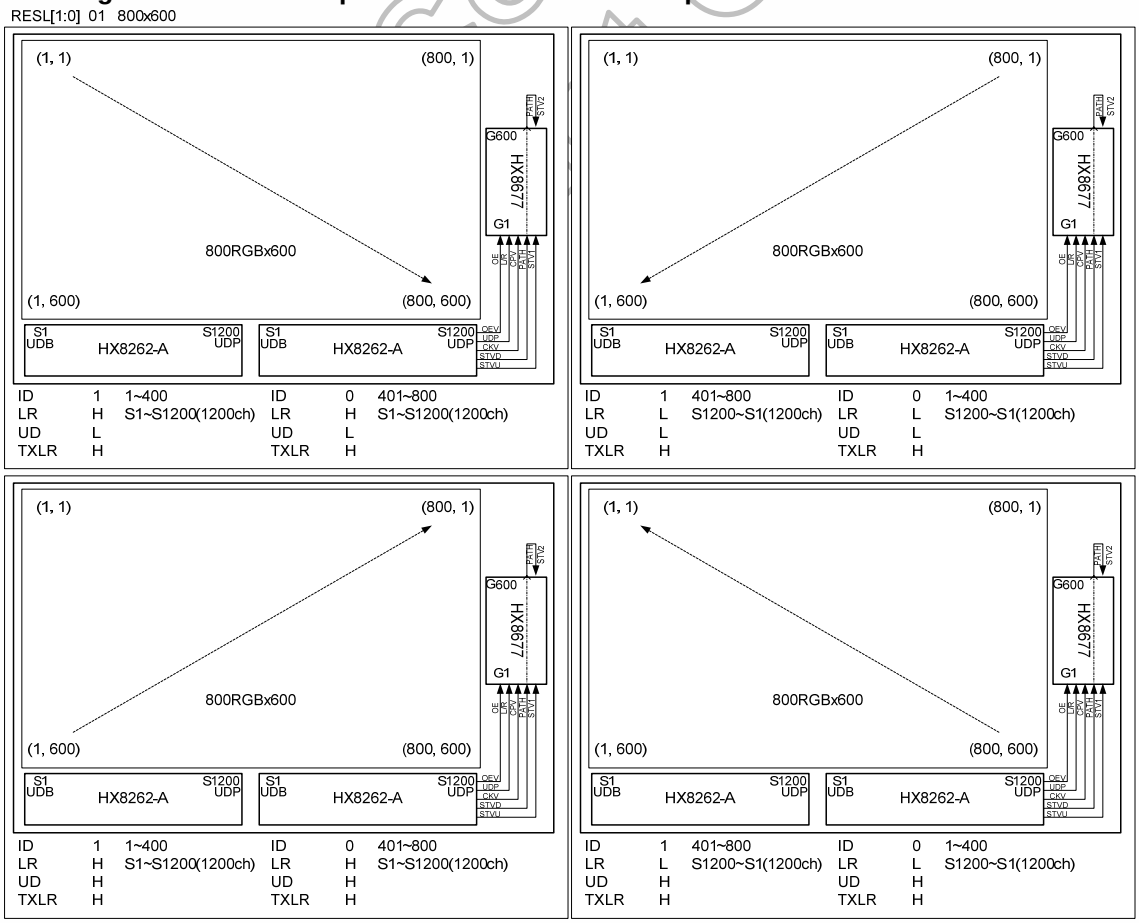


Figure 5.10 HX8262-A put down side and HX8677 put right side for 800RGB X 600

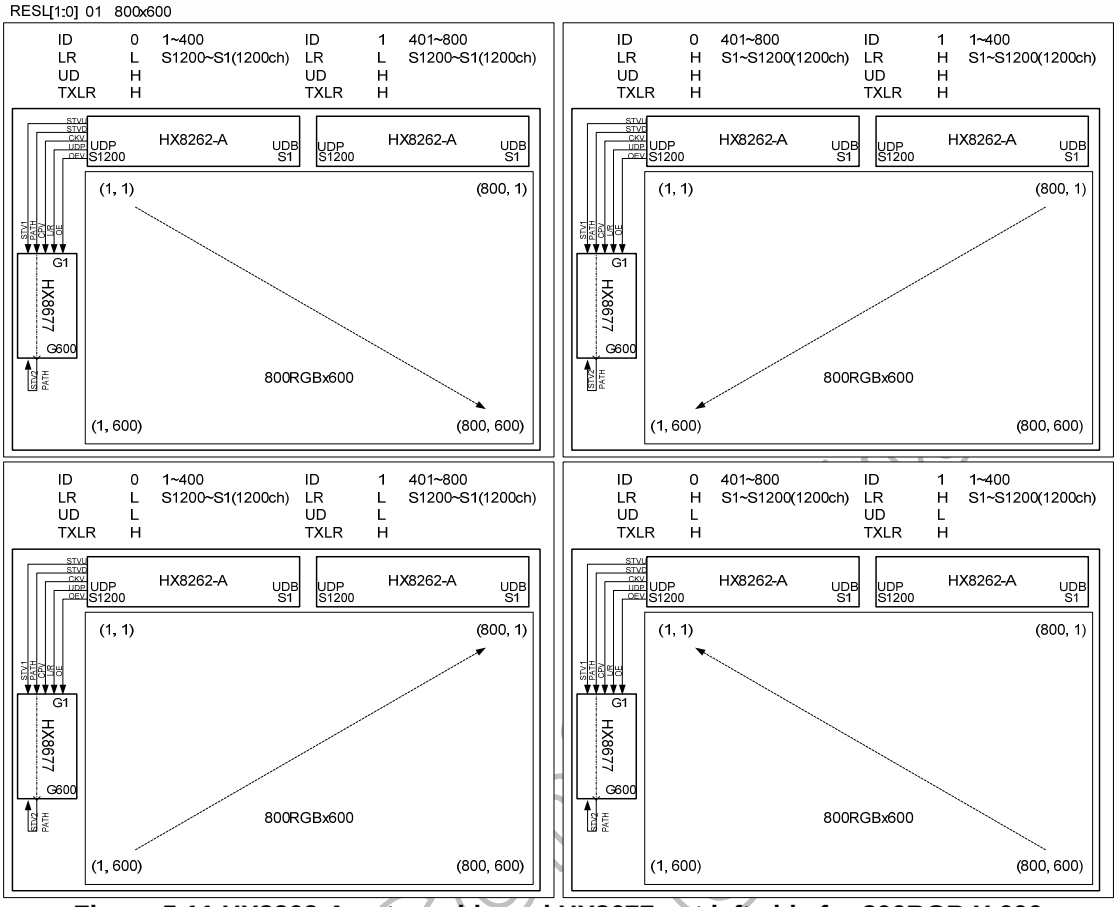


Figure 5.11 HX8262-A put up side and HX8677 put left side for 800RGB X 600

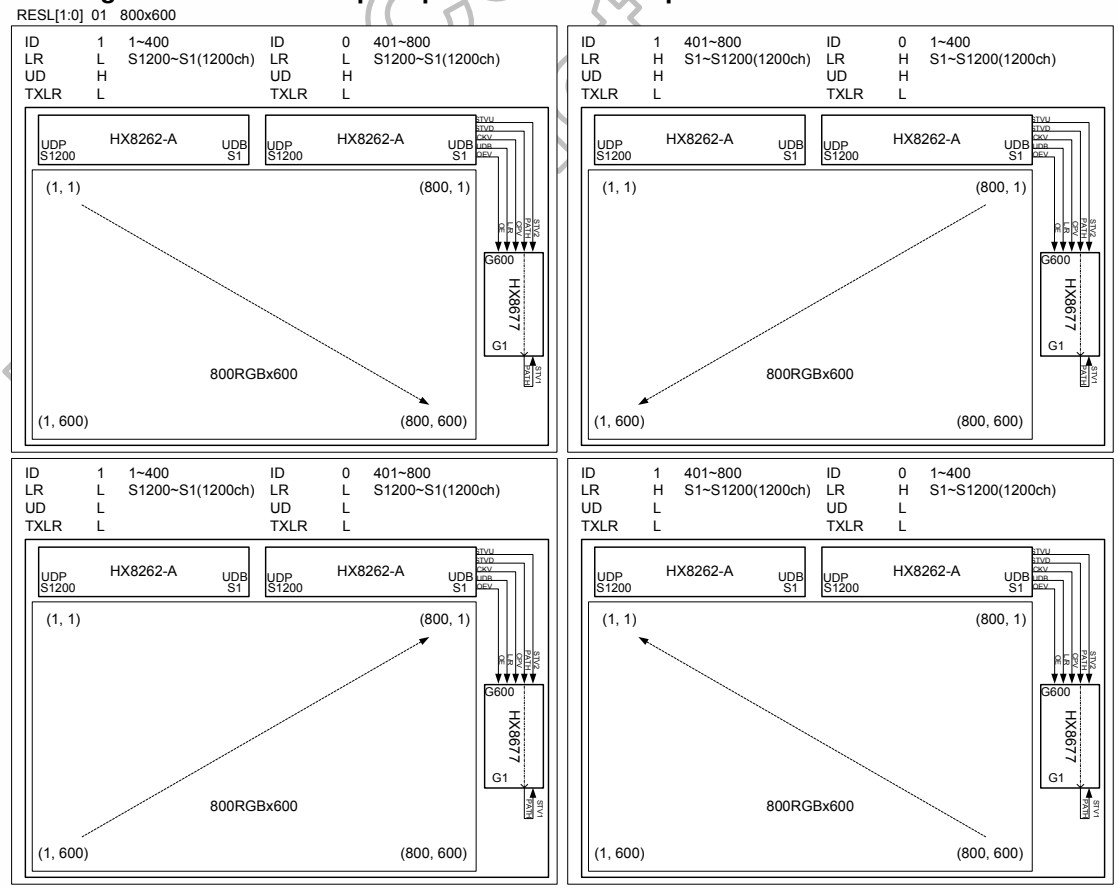


Figure 5.12 HX8262-A put up side and HX8677 put right side for 800RGB X 600

HX8262-A has several modes of timing control circuit, according to the setting ID and shift direction (LR) of the driver. These modes are decided by ID and LR settings as table 5.1 and 5.2. For example, when resolution is 800RGBx480, LR=H and HX8262-A ID is set as the 0, it latches the display data from the 1st to the 400th clock in DE active regions. When HX8262-A ID is set as the 1, it starts latching data from the 401th to the 800th clock in DE active region.

TXLR=L					
RESL[1:0]		ID	Sample cycle		Channel Number
			LR = H	LR = L	
0	0	0	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
0	0	1	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
0	1	0	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
0	1	1	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
1	0	0	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	0	1	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	1	0	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	1	1	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)

Table 5.1 Several modes of timing control

TXLR=H					
RESL[1:0]		ID	Sample cycle		Channel Number
			LR = H	LR = L	
0	0	0	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
0	0	1	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
0	1	0	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
0	1	1	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
1	0	0	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	0	1	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	1	0	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
1	1	1	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)

Table 5.2 Several modes of timing control

5.3 Internal Data Latch Sequence

In HX8262-A, 24-bit data are transferred into HX8262-A each cycle when DE is activated. Meanwhile, if LR="H" (right shift), D07 to D00 is displayed for output channel S3n-2, D17 to D10 are displayed for channel S3n-1, and D27 to D20 are displayed for channel S3n, where n=1, 2, … to 400 sequentially. The relationship between display data and source output is shown in the following figure.

If LR="L" (left shift), D07 to D00, D17 to D10, and D27 to D20 are still displayed for channel S3n-2, S3n-1, and S3n, respectively, but n=400 to 1 sequentially.

Driver latch data according to LR pin setting.

Input data format :	24-bit RGB, 3 dots (sub-pixels) per clock
Input data width :	24 bits with Dx7 is MSB and Dx0 is LSB, x=0,1,2

The following diagram shows the relationship of input data and output source channel for HX8262-A in different configurations (800 RGB resolution).

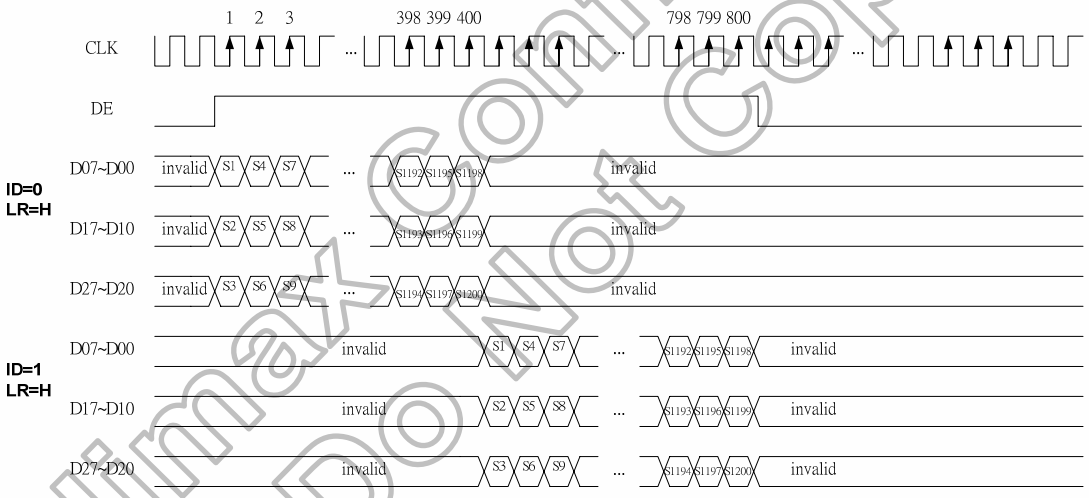


Figure 5.13 Input output relationship

5.4 Connect circuits for cascade mode

HX8262-A supports 800x480 and 800x600 resolutions by cascade 2 chips. In cascade mode, user need to set ID pins to define chip's ID, detail connect circuits are shown in Figure 5.14 and 5.15. The connect circuits depend on amount of chips and TXLR

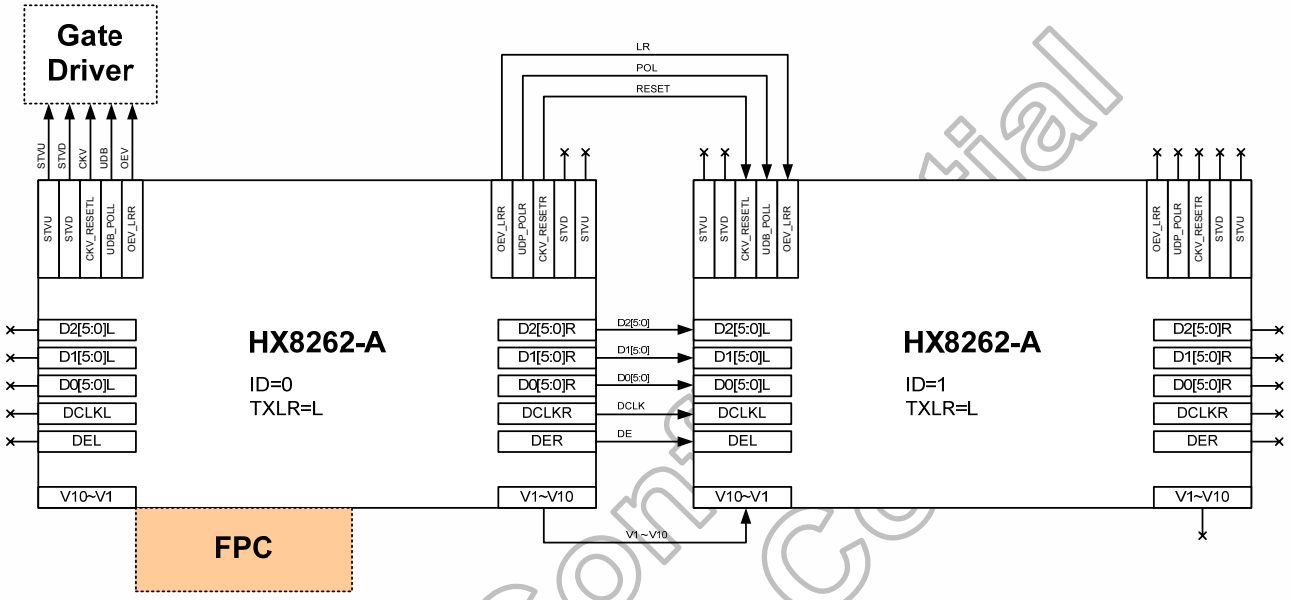


Figure 5.14 the connect circuit for cascading two HX8262-A chips when TXLR=L

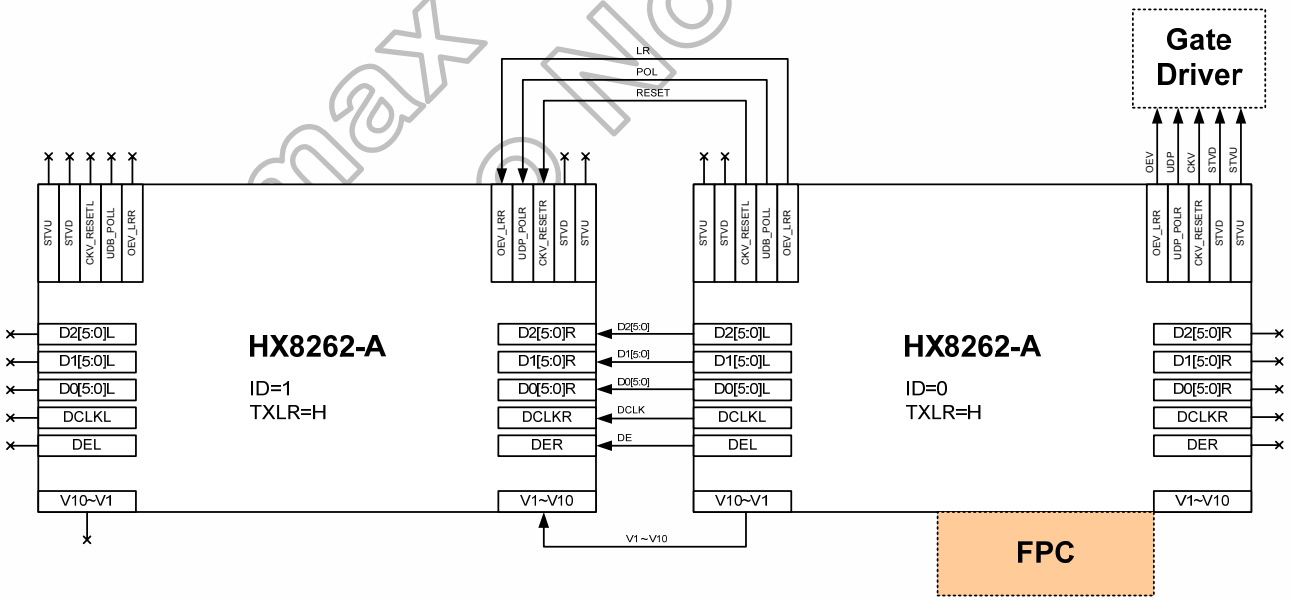


Figure 5.15 the connect circuit for cascading two HX8262-A chips when TXLR=H

TXLR	H	L	H	L
	ID=0		ID=1	
CKV_RESETR	CKV output	RESET output	RESET input	RESET output
CKV_RESETL	RESET output	CKV output	RESET output	RESET input
UDP_POLR	UDP output	POL output	POL input	POL output
UDB_POLL	POL output	UDB output	POL output	POL input
OEV_LRR	OEV output	LR output	LR input	LR output
OEV_LRL	LR output	OEV output	LR output	LR input
DCLKR	Hi-Z	DCLKR Output	DCLKL Input	Hi-Z
DCLKL	DCLKL Output	Hi-Z	Hi-Z	DCLKR Input
Dx[5:0]R, x=2,1,0	Hi-Z	Dx[5:0]R Output	Dx[5:0]L Input	Hi-Z
Dx[5:0]L, x=2,1,0	Dx[5:0]L Output	Hi-Z	Hi-Z	Dx[5:0]R Input
DER	Hi-Z	DER Output	DEL Input	Hi-Z
DEL	DEL Output	Hi-Z	Hi-Z	DER Input

Table 5.3a

ID=0				
TXLR	H	L	H	L
	UD=0		UD=1	
STVUL	Hi-Z	Hi-Z	Hi-Z	STVU Output
STVDL	Hi-Z	STVD Output	Hi-Z	Hi-Z
STVUR	Hi-Z	Hi-Z	STVU	Hi-Z
STVDR	STVD	Hi-Z	Hi-Z	Hi-Z

Table 5.3b

ID=1				
TXLR	H	L	H	L
	UD=0		UD=1	
STVUL	Hi-Z	Hi-Z	Hi-Z	Hi-Z
STVDL	Hi-Z	Hi-Z	Hi-Z	Hi-Z
STVUR	Hi-Z	Hi-Z	Hi-Z	Hi-Z
STVDR	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Table 5.3c

6. Gamma Adjustment Function

The HX8262-A incorporates gamma adjustment function for the 262K-color display. Gamma adjustment is implemented by deciding the 5-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

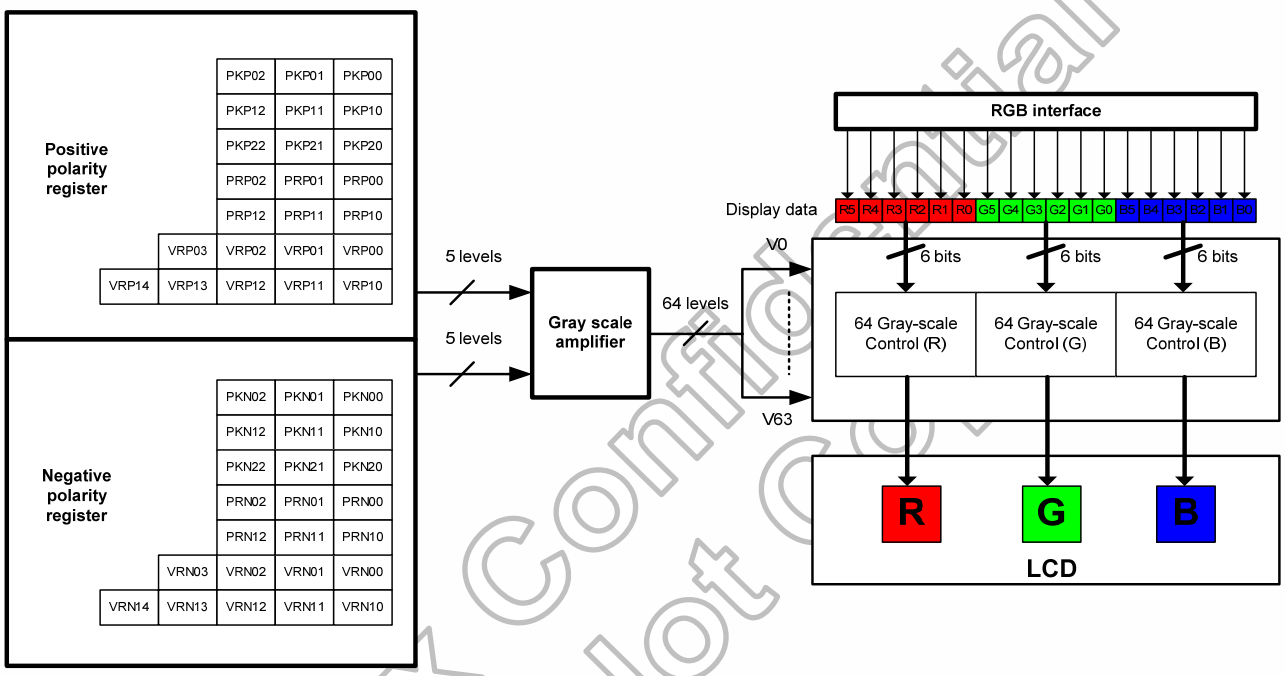


Figure 6. 1 Grayscale Control Block

6.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 10 levels (VIN1-VIN10) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

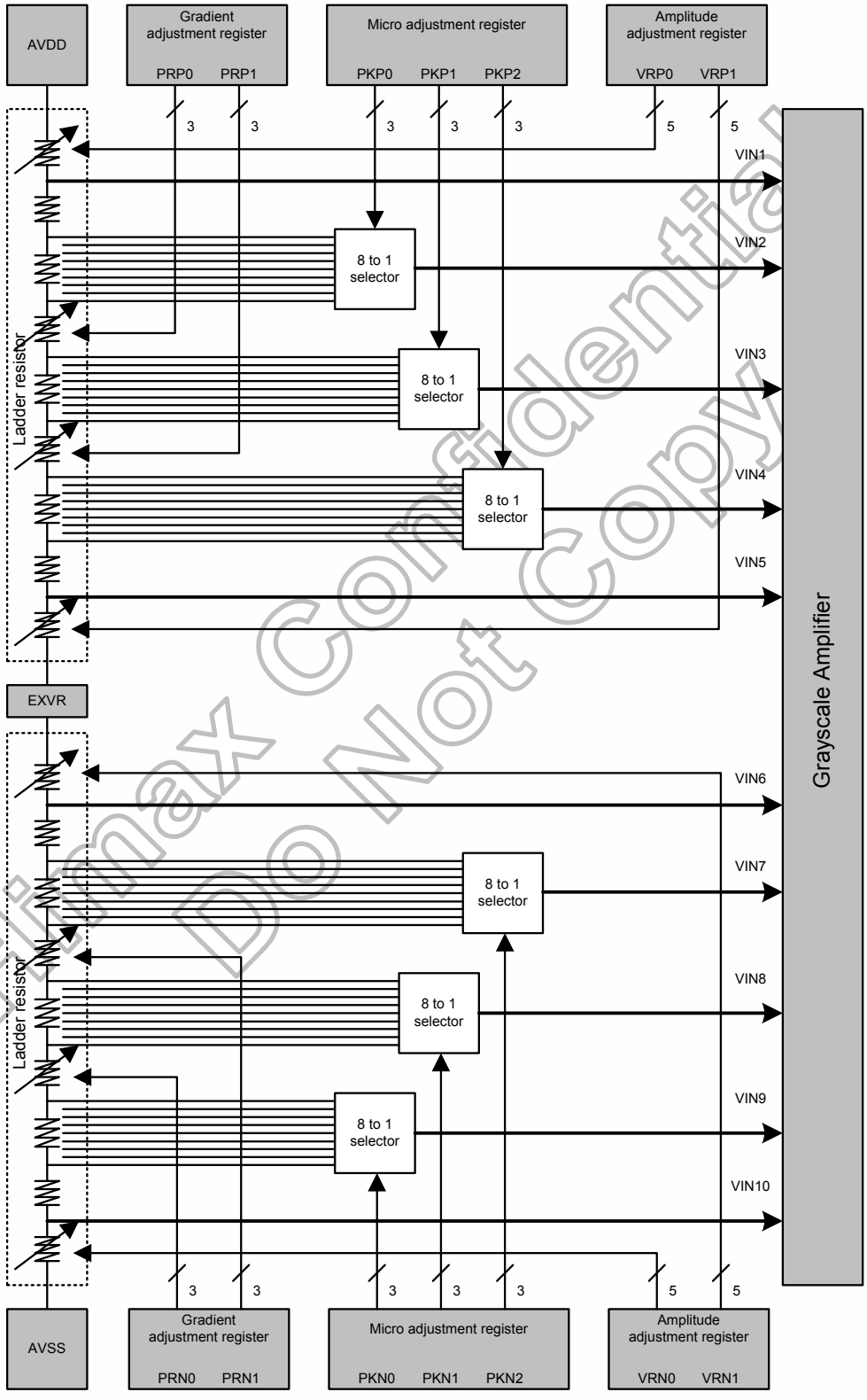


Figure 6. 2 Grayscale Amplifier

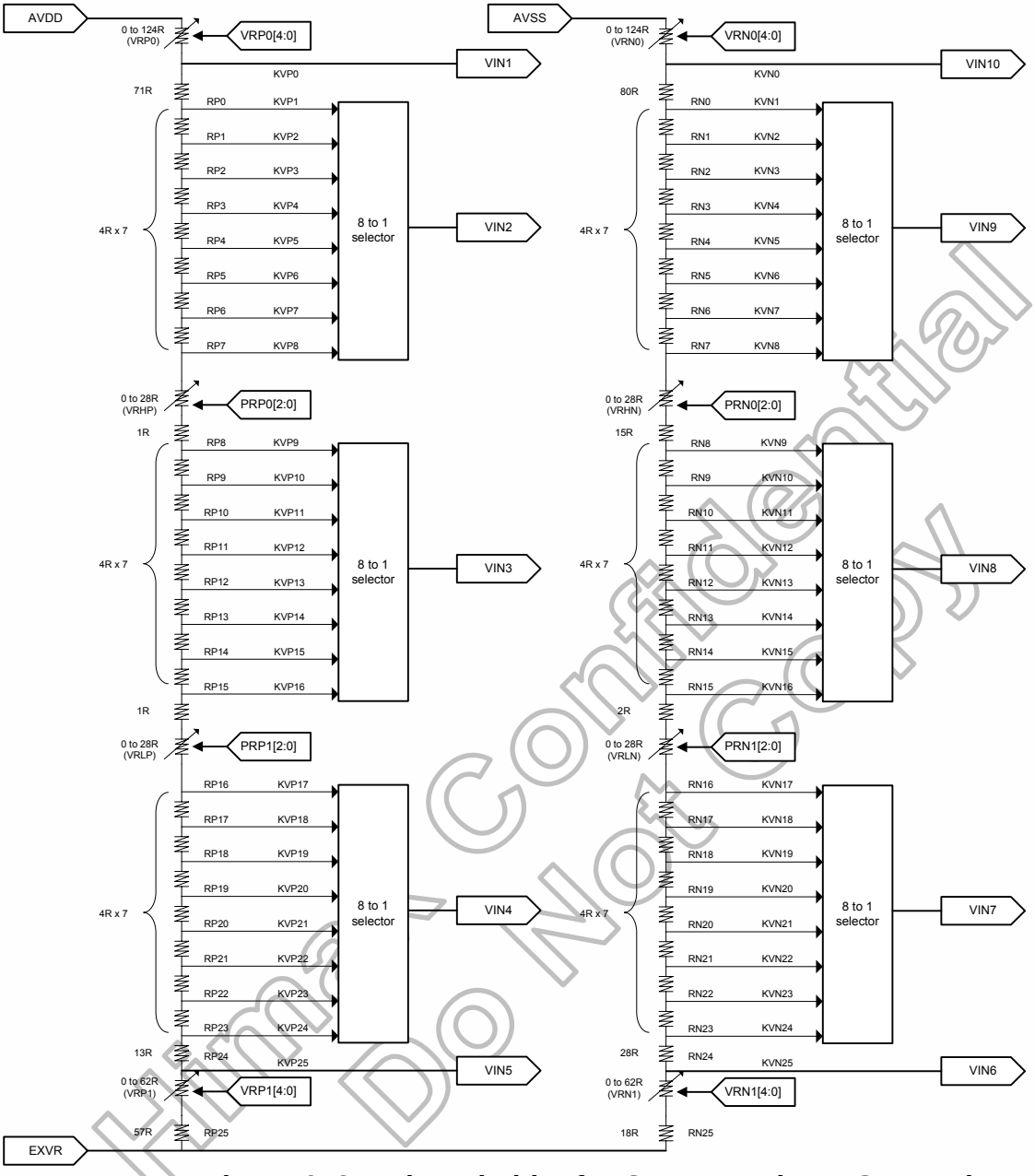


Figure 6. 3Resistor ladder for Gamma Voltage Generation

6.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

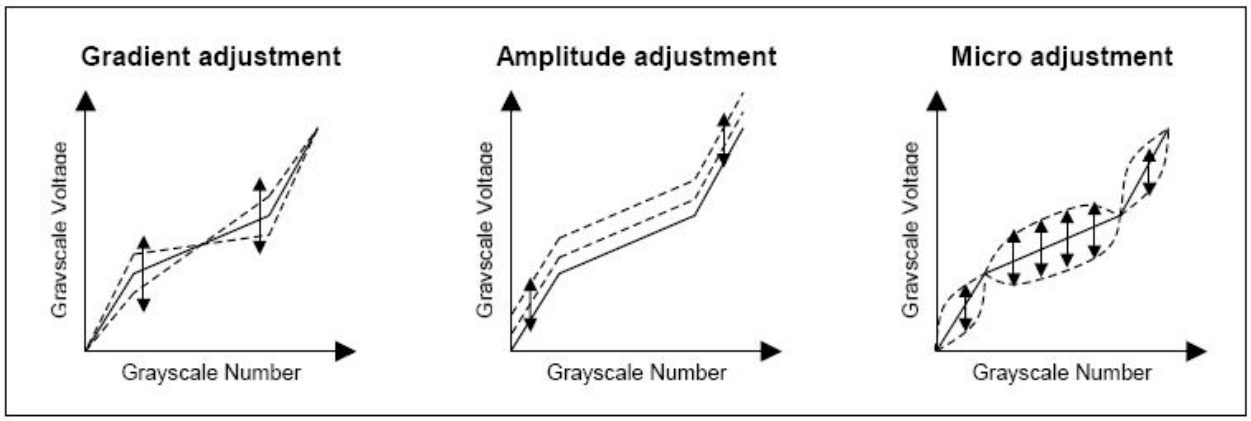


Figure 6. 3 Gamma Adjustment Function

6.2.1 Gradient Adjusting Register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP (N) 0 / PRP (N) 1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

6.2.2 Amplitude Adjusting Register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP (N) 0 / VRP (N) 1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

6.2.3 Micro Adjusting Register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

6.3 Ladder Resistor / 8 to 1 Selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSSA or an external variable resistor for compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP (N) 0 / PRP (N) 1) and (VRP (N) 0 / VRP (N) 1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 6. 1 PRP (N)

VRP(N)0	Resistance
00000	0R
00001	8R
00010	16R
: Step = 4R :	
11110	120R
11111	124R

Table 6. 2 VRP (N) 0

VRP(N)1	Resistance
00000	0R
00001	2R
00010	4R
: Step = 2R :	
11110	60R
11111	62R

Table 6. 3 VRP (N) 1

8 to 1 Selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are ten types of reference voltage (VIN1 to VIN10) and totally 24 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Positive polarity				Negative polarity			
Register PKP[2:0]	Selected voltage			Register PKN[2:0]	Selected voltage		
	VIN2	VIN3	VIN4		VIN7	VIN8	VIN9
000	KVP1	KVP9	KVP17	000	KVN1	KVN9	KVN17
001	KVP2	KVP10	KVP18	001	KVN2	KVN10	KVN18
010	KVP3	KVP11	KVP19	010	KVN3	KVN11	KVN19
011	KVP4	KVP12	KVP20	011	KVN4	KVN12	KVN20
100	KVP5	KVP13	KVP21	100	KVN5	KVN13	KVN21
101	KVP6	KVP14	KVP22	101	KVN6	KVN14	KVN22
110	KVP7	KVP15	KVP23	110	KVN7	KVN15	KVN23
111	KVP8	KVP16	KVP24	111	KVN8	KVN16	KVN24

Table 6. 4 PKP and PKN

Reference	Formula	Micro-adjusting register	Reference voltage
KVP0	VDDA - ΔV x VRP0 / SUMRP	-	VIN1
KVP1	VDDA - ΔV x (VRP0 + 71R) / SUMRP	PKP0[2:0] = ”000”	VIN2
KVP2	VDDA - ΔV x (VRP0 + 75R) / SUMRP	PKP0[2:0] = ”001”	
KVP3	VDDA - ΔV x (VRP0 + 79R) / SUMRP	PKP0[2:0] = ”010”	
KVP4	VDDA - ΔV x (VRP0 + 83R) / SUMRP	PKP0[2:0] = ”011”	
KVP5	VDDA - ΔV x (VRP0 + 87R) / SUMRP	PKP0[2:0] = ”100”	
KVP6	VDDA - ΔV x (VRP0 + 91R) / SUMRP	PKP0[2:0] = ”101”	
KVP7	VDDA - ΔV x (VRP0 + 95R) / SUMRP	PKP0[2:0] = ”110”	
KVP8	VDDA - ΔV x (VRP0 + 99R) / SUMRP	PKP0[2:0] = ”111”	
KVP9	VDDA - ΔV x (VRP0 + 100R + VRHP) / SUMRP	PKP1[2:0] = ”000”	VIN3
KVP10	VDDA - ΔV x (VRP0 + 104R + VRHP) / SUMRP	PKP1[2:0] = ”001”	
KVP11	VDDA - ΔV x (VRP0 + 108R + VRHP) / SUMRP	PKP1[2:0] = ”010”	
KVP12	VDDA - ΔV x (VRP0 + 112R + VRHP) / SUMRP	PKP1[2:0] = ”011”	
KVP13	VDDA - ΔV x (VRP0 + 116R + VRHP) / SUMRP	PKP1[2:0] = ”100”	
KVP14	VDDA - ΔV x (VRP0 + 120R + VRHP) / SUMRP	PKP1[2:0] = ”101”	
KVP15	VDDA - ΔV x (VRP0 + 124R + VRHP) / SUMRP	PKP1[2:0] = ”110”	
KVP16	VDDA - ΔV x (VRP0 + 128R + VRHP) / SUMRP	PKP1[2:0] = ”111”	
KVP17	VDDA - ΔV x (VRP0 + 129R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”000”	VIN4
KVP18	VDDA - ΔV x (VRP0 + 133R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”001”	
KVP19	VDDA - ΔV x (VRP0 + 137R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”010”	
KVP20	VDDA - ΔV x (VRP0 + 141R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”011”	
KVP21	VDDA - ΔV x (VRP0 + 145R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”100”	
KVP22	VDDA - ΔV x (VRP0 + 149R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”101”	
KVP23	VDDA - ΔV x (VRP0 + 153R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”110”	
KVP24	VDDA - ΔV x (VRP0 + 157R + VRHP + VRLP) / SUMRP	PKP2[2:0] = ”111”	
KVP25	VDDA - ΔV x (VRP0 + 170R + VRHP + VRLP) / SUMRP	-	VIN5

Table 6. 5 Reference Voltages of Positive Polarity

SUMRP: Total of the positive polarity ladder resistance = 227R + VRHP + VRLP + VRP0 + VRP1
ΔV: Voltage difference between VDDA and EXVR.

Reference	Formula	Micro-adjusting register	Reference voltage
KVN0	VSSA + ΔV x VRN0 / SUMRN	-	VIN10
KVN1	VSSA + ΔV x (VRN0 + 80R) / SUMRN	PKN0[2:0] = ”000”	VIN9
KVN2	VSSA + ΔV x (VRN0 + 84R) / SUMRN	PKN0[2:0] = ”001”	
KVN3	VSSA + ΔV x (VRN0 + 88R) / SUMRN	PKN0[2:0] = ”010”	
KVN4	VSSA + ΔV x (VRN0 + 92R) / SUMRN	PKN0[2:0] = ”011”	
KVN5	VSSA + ΔV x (VRN0 + 96R) / SUMRN	PKN0[2:0] = ”100”	
KVN6	VSSA + ΔV x (VRN0 + 100R) / SUMRN	PKN0[2:0] = ”101”	
KVN7	VSSA + ΔV x (VRN0 + 104R) / SUMRN	PKN0[2:0] = ”110”	
KVN8	VSSA + ΔV x (VRN0 + 108R) / SUMRN	PKN0[2:0] = ”111”	
KVN9	VSSA + ΔV x (VRN0 + 123R + VRHN) / SUMRN	PKN1[2:0] = ”000”	VIN8
KVN10	VSSA + ΔV x (VRN0 + 127R + VRHN) / SUMRN	PKN1[2:0] = ”001”	
KVN11	VSSA + ΔV x (VRN0 + 131R + VRHN) / SUMRN	PKN1[2:0] = ”010”	
KVN12	VSSA + ΔV x (VRN0 + 135R + VRHN) / SUMRN	PKN1[2:0] = ”011”	
KVN13	VSSA + ΔV x (VRN0 + 139R + VRHN) / SUMRN	PKN1[2:0] = ”100”	
KVN14	VSSA + ΔV x (VRN0 + 143R + VRHN) / SUMRN	PKN1[2:0] = ”101”	
KVN15	VSSA + ΔV x (VRN0 + 147R + VRHN) / SUMRN	PKN1[2:0] = ”110”	
KVN16	VSSA + ΔV x (VRN0 + 151R + VRHN) / SUMRN	PKN1[2:0] = ”111”	
KVN17	VSSA + ΔV x (VRN0 + 153R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”000”	VIN7
KVN18	VSSA + ΔV x (VRN0 + 157R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”001”	
KVN19	VSSA + ΔV x (VRN0 + 161R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”010”	
KVN20	VSSA + ΔV x (VRN0 + 165R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”011”	
KVN21	VSSA + ΔV x (VRN0 + 169R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”100”	
KVN22	VSSA + ΔV x (VRN0 + 173R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”101”	
KVN23	VSSA + ΔV x (VRN0 + 177R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”110”	
KVN24	VSSA + ΔV x (VRN0 + 181R + VRHN + VRLN) / SUMRN	PKN2[2:0] = ”111”	
KVN25	VSSA + ΔV x (VRN0 + 209R + VRHN + VRLN) / SUMRN	-	VIN6

Table 6. 6 Reference Voltages of Negative Polarity

SUMRN: Total of the negative polarity ladder resistance = 227R + VRHN + VRLN + VRN0 + VRN1
ΔV: Voltage difference between EXVR and VSSA.

6.4 Relationship between gamma correction and output voltage

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V10 gamma correction reference voltage inputs.

Gamma correction characteristic curve:

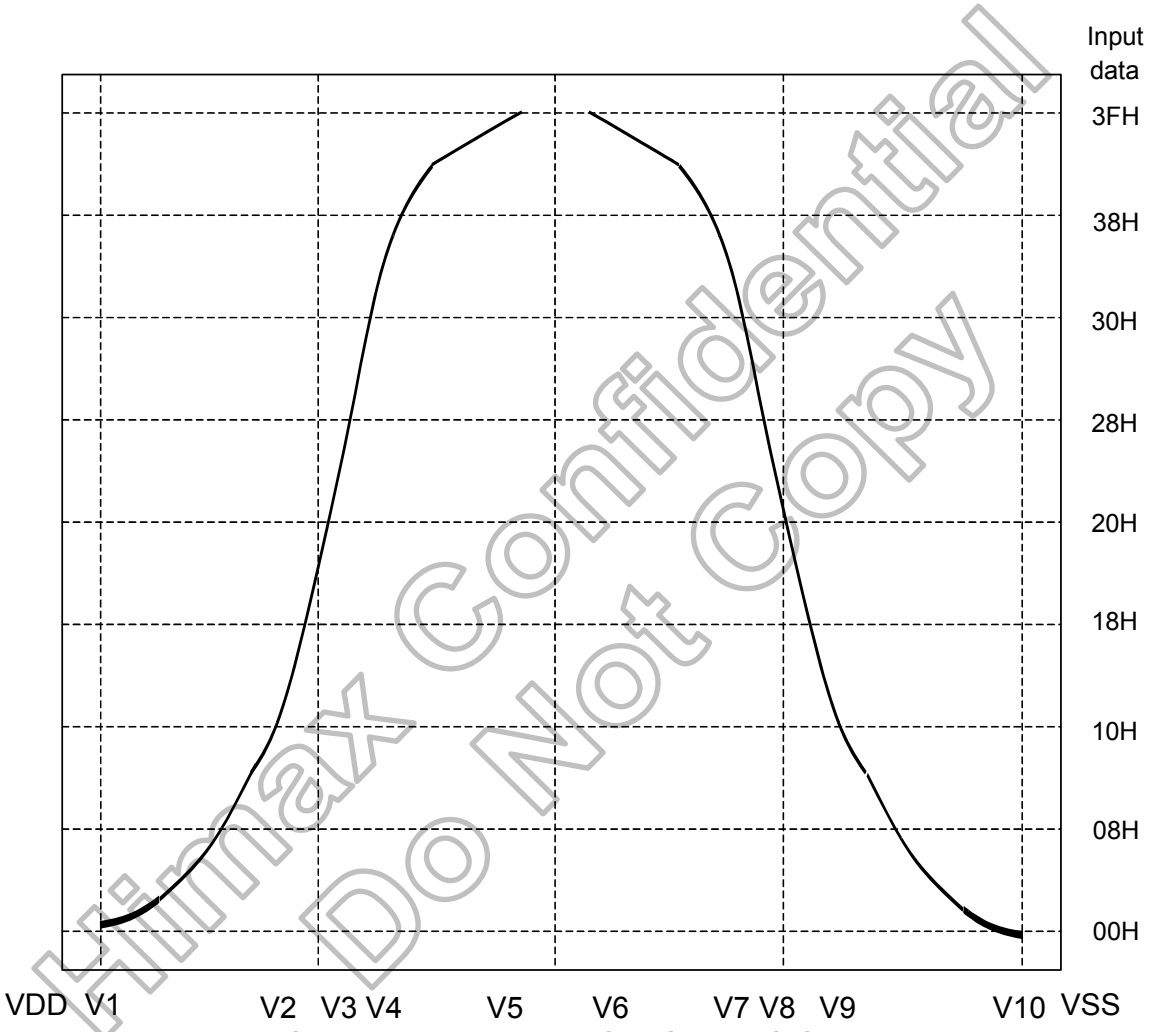


Figure 6.5 Gamma correction characteristic curve

Gamma correction resistor ratio: (1 unit = 125ohm)

V1, V10 →

Name	Resistor	Name	Resistor
R0	6.4	R32	0.8
R1	6	R33	0.8
R2	5.6	R34	0.8
R3	5.2	R35	0.8
R4	4.8	R36	0.8
R5	4.4	R37	0.8
R6	4.4	R38	0.8
R7	4	R39	0.8
R8	4	R40	0.8
R9	3.2	R41	0.8
R10	3.2	R42	0.8
R11	2.8	R43	0.8
R12	2.8	R44	0.8
R13	2.8	R45	0.8
R14	2.4	R46	0.8
R15	2.4	R47	0.8
R16	2.4	R48	0.8
R17	2	R49	0.8
R18	2	R50	0.8
R19	2	R51	0.8
R20	1.6	R52	0.8
R21	1.6	R53	1.2
R22	1.6	R54	1.2
R23	1.2	R55	1.2
R24	1.2	R56	1.6
R25	1.2	R57	1.6
R26	1.2	R58	2
R27	0.8	R59	2
R28	0.8	R60	2.4
R29	0.8	R61	4
R30	0.8	R62	6.4
R31	0.8		

V2, V9 →

← V4, V7

← V5, V6

V3, V8 →

Output Voltages vs. Source Input Data when VSET=H:
Please input V1~V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V2 + (V1 – V2)X 58 / 64.4	V10 + (V9 – V10)X 6.4 / 64.4
02H	V2 + (V1 – V2)X 52 / 64.4	V10 + (V9 – V10)X 12.4 / 64.4
03H	V2 + (V1 – V2)X 46.4 / 64.4	V10 + (V9 – V10)X 18 / 64.4
04H	V2 + (V1 – V2)X 41.2 / 64.4	V10 + (V9 – V10)X 23.2 / 64.4
05H	V2 + (V1 – V2)X 36.4 / 64.4	V10 + (V9 – V10)X 28 / 64.4
06H	V2 + (V1 – V2)X 32 / 64.4	V10 + (V9 – V10)X 32.4 / 64.4
07H	V2 + (V1 – V2)X 27.6 / 64.4	V10 + (V9 – V10)X 36.8 / 64.4
08H	V2 + (V1 – V2)X 23.6 / 64.4	V10 + (V9 – V10)X 40.8 / 64.4
09H	V2 + (V1 – V2)X 19.6 / 64.4	V10 + (V9 – V10)X 44.8 / 64.4
0AH	V2 + (V1 – V2)X 16.4 / 64.4	V10 + (V9 – V10)X 48 / 64.4
0BH	V2 + (V1 – V2)X 13.2 / 64.4	V10 + (V9 – V10)X 51.2 / 64.4
0CH	V2 + (V1 – V2)X 10.4 / 64.4	V10 + (V9 – V10)X 54 / 64.4
0DH	V2 + (V1 – V2)X 7.6 / 64.4	V10 + (V9 – V10)X 56.8 / 64.4
0EH	V2 + (V1 – V2)X 4.8 / 64.4	V10 + (V9 – V10)X 59.6 / 64.4
0FH	V2 + (V1 – V2)X 2.4 / 64.4	V10 + (V9 – V10)X 62 / 64.4
10H	V2	V9
11H	V3 + (V2 – V3) X 19.6 / 22	V9 + (V8 – V9)X 2.4 / 22
12H	V3 + (V2 – V3) X 17.6 / 22	V9 + (V8 – V9)X 4.4 / 22
13H	V3 + (V2 – V3) X 15.6 / 22	V9 + (V8 – V9)X 6.4 / 22
14H	V3 + (V2 – V3) X 13.6 / 22	V9 + (V8 – V9)X 8.4 / 22
15H	V3 + (V2 – V3) X 12 / 22	V9 + (V8 – V9)X 10 / 22
16H	V3 + (V2 – V3) X 10.4 / 22	V9 + (V8 – V9)X 11.6 / 22
17H	V3 + (V2 – V3) X 8.8 / 22	V9 + (V8 – V9)X 13.2 / 22
18H	V3 + (V2 – V3) X 7.6 / 22	V9 + (V8 – V9)X 14.4 / 22
19H	V3 + (V2 – V3) X 6.4 / 22	V9 + (V8 – V9)X 15.6 / 22
1AH	V3 + (V2 – V3) X 5.2 / 22	V9 + (V8 – V9)X 16.8 / 22
1BH	V3 + (V2 – V3) X 4 / 22	V9 + (V8 – V9)X 18 / 22
1CH	V3 + (V2 – V3) X 3.2 / 22	V9 + (V8 – V9)X 18.8 / 22
1DH	V3 + (V2 – V3) X 2.4 / 22	V9 + (V8 – V9)X 19.6 / 22
1EH	V3 + (V2 – V3) X 1.6 / 22	V9 + (V8 – V9)X 20.4 / 22
1FH	V3 + (V2 – V3) X 0.8 / 22	V9 + (V8 – V9)X 21.2 / 22

Output Voltages vs. Source Input Data when VSET=H (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V3	V8
21H	V4 + (V3 – V4) X 12 / 12.8	V8 + (V7 – V8) X 0.8 / 12.8
22H	V4 + (V3 – V4) X 11.2 / 12.8	V8 + (V7 – V8) X 1.6 / 12.8
23H	V4 + (V3 – V4) X 10.4 / 12.8	V8 + (V7 – V8) X 2.4 / 12.8
24H	V4 + (V3 – V4) X 9.6 / 12.8	V8 + (V7 – V8) X 3.2 / 12.8
25H	V4 + (V3 – V4) X 8.8 / 12.8	V8 + (V7 – V8) X 4 / 12.8
26H	V4 + (V3 – V4) X 8 / 12.8	V8 + (V7 – V8) X 4.8 / 12.8
27H	V4 + (V3 – V4) X 7.2 / 12.8	V8 + (V7 – V8) X 5.6 / 12.8
28H	V4 + (V3 – V4) X 6.4 / 12.8	V8 + (V7 – V8) X 6.4 / 12.8
29H	V4 + (V3 – V4) X 5.6 / 12.8	V8 + (V7 – V8) X 7.2 / 12.8
2AH	V4 + (V3 – V4) X 4.8 / 12.8	V8 + (V7 – V8) X 8 / 12.8
2BH	V4 + (V3 – V4) X 4 / 12.8	V8 + (V7 – V8) X 8.8 / 12.8
2CH	V4 + (V3 – V4) X 3.2 / 12.8	V8 + (V7 – V8) X 9.6 / 12.8
2DH	V4 + (V3 – V4) X 2.4 / 12.8	V8 + (V7 – V8) X 10.4 / 12.8
2EH	V4 + (V3 – V4) X 1.6 / 12.8	V8 + (V7 – V8) X 11.2 / 12.8
2FH	V4 + (V3 – V4) X 0.8 / 12.8	V8 + (V7 – V8) X 12 / 12.8
30H	V4	V7
31H	V5 + (V4 – V5) X 26.8 / 27.6	V7 + (V6 – V7) X 0.8 / 27.6
32H	V5 + (V4 – V5) X 26 / 27.6	V7 + (V6 – V7) X 1.6 / 27.6
33H	V5 + (V4 – V5) X 25.2 / 27.6	V7 + (V6 – V7) X 2.4 / 27.6
34H	V5 + (V4 – V5) X 24.4 / 27.6	V7 + (V6 – V7) X 3.2 / 27.6
35H	V5 + (V4 – V5) X 23.6 / 27.6	V7 + (V6 – V7) X 4 / 27.6
36H	V5 + (V4 – V5) X 22.4 / 27.6	V7 + (V6 – V7) X 5.2 / 27.6
37H	V5 + (V4 – V5) X 21.2 / 27.6	V7 + (V6 – V7) X 6.4 / 27.6
38H	V5 + (V4 – V5) X 20 / 27.6	V7 + (V6 – V7) X 7.6 / 27.6
39H	V5 + (V4 – V5) X 18.4 / 27.6	V7 + (V6 – V7) X 9.2 / 27.6
3AH	V5 + (V4 – V5) X 16.8 / 27.6	V7 + (V6 – V7) X 10.8 / 27.6
3BH	V5 + (V4 – V5) X 14.8 / 27.6	V7 + (V6 – V7) X 12.8 / 27.6
3CH	V5 + (V4 – V5) X 12.8 / 27.6	V7 + (V6 – V7) X 14.8 / 27.6
3DH	V5 + (V4 – V5) X 10.4 / 27.6	V7 + (V6 – V7) X 17.2 / 27.6
3EH	V5 + (V4 – V5) X 6.4 / 27.6	V7 + (V6 – V7) X 21.2 / 27.6
3FH	V5	V6

Output Voltages vs. Source Input Data when VSET=L:
Please input V1, V5 and V6, V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V5 + (V1 – V5)X 120.4 / 126.8	V10 + (V6 – V10)X 6.4 / 126.8
02H	V5 + (V1 – V5)X 114.4 / 126.8	V10 + (V6 – V10)X 12.4 / 126.8
03H	V5 + (V1 – V5)X 108.8 / 126.8	V10 + (V6 – V10)X 18 / 126.8
04H	V5 + (V1 – V5)X 103.6 / 126.8	V10 + (V6 – V10)X 23.2 / 126.8
05H	V5 + (V1 – V5)X 98.8 / 126.8	V10 + (V6 – V10)X 28 / 126.8
06H	V5 + (V1 – V5)X 94.4 / 126.8	V10 + (V6 – V10)X 32.4 / 126.8
07H	V5 + (V1 – V5)X 90 / 126.8	V10 + (V6 – V10)X 36.8 / 126.8
08H	V5 + (V1 – V5)X 86 / 126.8	V10 + (V6 – V10)X 40.8 / 126.8
09H	V5 + (V1 – V5)X 82 / 126.8	V10 + (V6 – V10)X 44.8 / 126.8
0AH	V5 + (V1 – V5)X 78.8 / 126.8	V10 + (V6 – V10)X 48 / 126.8
0BH	V5 + (V1 – V5)X 75.6 / 126.8	V10 + (V6 – V10)X 51.2 / 126.8
0CH	V5 + (V1 – V5)X 72.8 / 126.8	V10 + (V6 – V10)X 54 / 126.8
0DH	V5 + (V1 – V5)X 70 / 126.8	V10 + (V6 – V10)X 56.8 / 126.8
0EH	V5 + (V1 – V5)X 67.2 / 126.8	V10 + (V6 – V10)X 59.6 / 126.8
0FH	V5 + (V1 – V5)X 64.8 / 126.8	V10 + (V6 – V10)X 62 / 126.8
10H	V5 + (V1 – V5)X 62.4 / 126.8	V10 + (V6 – V10)X 64.4 / 126.8
11H	V5 + (V1 – V5)X 60 / 126.8	V10 + (V6 – V10)X 66.8 / 126.8
12H	V5 + (V1 – V5)X 58 / 126.8	V10 + (V6 – V10)X 68.8 / 126.8
13H	V5 + (V1 – V5)X 56 / 126.8	V10 + (V6 – V10)X 70.8 / 126.8
14H	V5 + (V1 – V5)X 54 / 126.8	V10 + (V6 – V10)X 72.8 / 126.8
15H	V5 + (V1 – V5)X 52.4 / 126.8	V10 + (V6 – V10)X 74.4 / 126.8
16H	V5 + (V1 – V5)X 50.8 / 126.8	V10 + (V6 – V10)X 76 / 126.8
17H	V5 + (V1 – V5)X 49.2 / 126.8	V10 + (V6 – V10)X 77.6 / 126.8
18H	V5 + (V1 – V5)X 48 / 126.8	V10 + (V6 – V10)X 78.8 / 126.8
19H	V5 + (V1 – V5)X 46.8 / 126.8	V10 + (V6 – V10)X 80 / 126.8
1AH	V5 + (V1 – V5)X 45.6 / 126.8	V10 + (V6 – V10)X 81.2 / 126.8
1BH	V5 + (V1 – V5)X 44.4 / 126.8	V10 + (V6 – V10)X 82.4 / 126.8
1CH	V5 + (V1 – V5)X 43.6 / 126.8	V10 + (V6 – V10)X 83.2 / 126.8
1DH	V5 + (V1 – V5)X 42.8 / 126.8	V10 + (V6 – V10)X 84 / 126.8
1EH	V5 + (V1 – V5)X 42 / 126.8	V10 + (V6 – V10)X 84.8 / 126.8
1FH	V5 + (V1 – V5)X 41.2 / 126.8	V10 + (V6 – V10)X 85.6 / 126.8

Output Voltages vs. Source Input Data when VSET=L (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V5 + (V1 – V5)X 40.4 / 126.8	V10 + (V6 – V10)X 86.4 / 126.8
21H	V5 + (V1 – V5)X 39.6 / 126.8	V10 + (V6 – V10)X 87.2 / 126.8
22H	V5 + (V1 – V5)X 38.8 / 126.8	V10 + (V6 – V10)X 88 / 126.8
23H	V5 + (V1 – V5)X 38 / 126.8	V10 + (V6 – V10)X 88.8 / 126.8
24H	V5 + (V1 – V5)X 37.2 / 126.8	V10 + (V6 – V10)X 89.6 / 126.8
25H	V5 + (V1 – V5)X 36.4 / 126.8	V10 + (V6 – V10)X 90.4 / 126.8
26H	V5 + (V1 – V5)X 35.6 / 126.8	V10 + (V6 – V10)X 91.2 / 126.8
27H	V5 + (V1 – V5)X 34.8 / 126.8	V10 + (V6 – V10)X 92 / 126.8
28H	V5 + (V1 – V5)X 34 / 126.8	V10 + (V6 – V10)X 92.8 / 126.8
29H	V5 + (V1 – V5)X 33.2 / 126.8	V10 + (V6 – V10)X 93.6 / 126.8
2AH	V5 + (V1 – V5)X 32.4 / 126.8	V10 + (V6 – V10)X 94.4 / 126.8
2BH	V5 + (V1 – V5)X 31.6 / 126.8	V10 + (V6 – V10)X 95.2 / 126.8
2CH	V5 + (V1 – V5)X 30.8 / 126.8	V10 + (V6 – V10)X 96 / 126.8
2DH	V5 + (V1 – V5)X 30 / 126.8	V10 + (V6 – V10)X 96.8 / 126.8
2EH	V5 + (V1 – V5)X 29.2 / 126.8	V10 + (V6 – V10)X 97.6 / 126.8
2FH	V5 + (V1 – V5)X 28.4/ 126.8	V10 + (V6 – V10)X 98.4 / 126.8
30H	V5 + (V1 – V5)X 27.6 / 126.8	V10 + (V6 – V10)X 99.2 / 126.8
31H	V5 + (V1 – V5)X 26.8 / 126.8	V10 + (V6 – V10)X 100 / 126.8
32H	V5 + (V1 – V5)X 26 / 126.8	V10 + (V6 – V10)X 100.8 / 126.8
33H	V5 + (V1 – V5)X 25.2 / 126.8	V10 + (V6 – V10)X 101.6 / 126.8
34H	V5 + (V1 – V5)X 24.4 / 126.8	V10 + (V6 – V10)X 102.4 / 126.8
35H	V5 + (V1 – V5)X 23.6 / 126.8	V10 + (V6 – V10)X 103.2 / 126.8
36H	V5 + (V1 – V5)X 22.4 / 126.8	V10 + (V6 – V10)X 104.4 / 126.8
37H	V5 + (V1 – V5)X 21.2 / 126.8	V10 + (V6 – V10)X 105.6 / 126.8
38H	V5 + (V1 – V5)X 20 / 126.8	V10 + (V6 – V10)X 106.8 / 126.8
39H	V5 + (V1 – V5)X 18.4 / 126.8	V10 + (V6 – V10)X 108.4 / 126.8
3AH	V5 + (V1 – V5)X 16.8 / 126.8	V10 + (V6 – V10)X 110 / 126.8
3BH	V5 + (V1 – V5)X 14.8 / 126.8	V10 + (V6 – V10)X 112 / 126.8
3CH	V5 + (V1 – V5)X 12.8 / 126.8	V10 + (V6 – V10)X 114 / 126.8
3DH	V5 + (V1 – V5)X 10.4 / 126.8	V10 + (V6 – V10)X 116.4 / 126.8
3EH	V5 + (V1 – V5)X 6.4 / 126.8	V10 + (V6 – V10)X 120.4 / 126.8
3FH	V5	V6

7. SPI Register Setting

7.1 SPI Register Description

Register name	Test	Address					Data							
	RW	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0							PSC	RESETB
													0	1
R1	0	0	0	0	0	1				PGEN	GOTP	RESL2	RESL1	RESL0
										0	0	0	0	0
R2	0	0	0	0	1	0	STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
							1	0	0	0	0	0	0	0
R3	0	0	0	0	1	1		STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0
								0	0	1	1	0	1	1
R4	0	0	0	1	0	0		EDGSL	LR	UD	CS	FRC	VS_POL	HS_POL
								0	1	0	1	1	0	0
R5	0	0	0	1	0	1							A_TIME1	A_TIME0
													0	0
R6	0	0	0	1	1	1	PWMA	FBA2	FBA1	FBA0	PWMB	FBB2	FBB1	FBB0
							0	0	1	0	0	0	1	0
R7	0	0	1	0	0	0			PKP02	PKP01	PKP00	PKP12	PKP11	PKP10
									1	1	0	1	0	0
R8	0	0	1	0	0	1			PKP22	PKP21	PKP20	PRP02	PRP01	PRP00
									0	0	1	0	0	0
R9	0	0	1	0	1	0	PRP12	PRP11	PRP10	VRP04	VRP03	VRP02	VRP01	VRP00
							0	0	0	1	0	0	1	1
R10	0	0	1	0	1	1				VRP14	VRP13	VRP12	VRP11	VRP10
										0	1	0	1	0
R11	0	0	1	1	0	0			PKN02	PKN01	PKN00	PKN12	PKN11	PKN10
									1	0	1	0	1	1
R12	0	0	1	1	0	1			PKN22	PKN21	PKN20	PRN02	PRN01	PRN00
									0	0	1	0	0	0
R13	0	0	1	1	1	0	PRN12	PRN11	PRN10	VRN04	VRN03	VRN02	VRN01	VRN00
							0	0	0	1	0	0	0	1
R14	0	0	1	1	1	0				VRN14	VRN13	VRN12	VRN11	VRN10
										1	0	0	0	0
R15	0	1	0	0	0	0		CEL	PPR	VPS	PA1	PA0	PWE	POR
								0	0	0	0	0	0	0
R16	0	1	0	0	0	1	CELL1-31	CELL1-30	CELL1-29	CELL1-28	CELL1-27	CELL1-26	CELL1-25	CELL1-24
R17	0	1	0	0	1	0	CELL1-23	CELL1-22	CELL1-21	CELL1-20	CELL1-19	CELL1-18	CELL1-17	CELL1-16
										0				
R18	0	1	0	0	1	1	CELL1-15	CELL1-14	CELL1-13	CELL1-12	CELL1-11	CELL1-10	CELL1-9	CELL1-8
										0				
R19	0	1	0	1	0	0	CELL1-7	CELL1-6	CELL1-5	CELL1-4	CELL1-3	CELL1-2	CELL1-1	CELL1-0
										0				
R20	0	1	0	1	0	1	CELL2-31	CELL2-30	CELL2-29	CELL2-28	CELL2-27	CELL2-26	CELL2-25	CELL2-24
										0				
R21	0	1	0	1	1	0	CELL2-23	CELL2-22	CELL2-21	CELL2-20	CELL2-19	CELL2-18	CELL2-17	CELL2-16
										0				
R22	0	1	0	1	1	1	CELL2-15	CELL2-14	CELL2-13	CELL2-12	CELL2-11	CELL2-10	CELL2-9	CELL2-8
										0				
R23	0	1	1	0	0	0	CELL2-7	CELL2-6	CELL2-5	CELL2-4	CELL2-3	CELL2-2	CELL2-1	CELL2-0
										0				

Table 7.1 Register list

- **Register R00**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	reserved	PSC	RESETB
Default	-	-	-	-	-	-	0	1

Table 7. 2 Register R0 setting

PSC: Operating mode setting by input pin or SPI register.
PSC=L, set CS ,RESL[1:0], EDGSL, LR, UD by input pin.
PSC=H, set CS ,RESL[1:0], EDGSL, LR, UD by SPI register.

RESETB: Global reset.
RESETB=L, Reset the whole chip.
RESETB=H, Normal operation.

- **Register R01**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	PGEN	GOTP	reserved	RESL1	RESL0
Default	–	–	–	0	0	–	0	0

Table 7. 3 Register R1 setting

PGEN: Select V1 ~ V10 from internal programmable gamma curve or external
PGEN=L, disable internal programmable gamma, input V1 ~ V10 as gamma voltage.
PGEN=H, internal programmable gamma enable

GOTP : Control all gamma setting is effective from OTP or SPI register
GOTP=L, OTP effective
GOTP=H, SPI register effective

RESL [1:0]: Display resolution selection.

RESL1	RESL0	Resolution
0	0	800x480
0	1	800x600
1	x	400x240

Table 7. 4 Display resolution selection.

Register R02

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	1	0	0	0	0	0	0	0

Table 7. 5 Register R2 setting

STHD [7:0]: adjust first dot data position,

STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position adjust	Unit
0	0	0	0	0	0	0	0	0	T_{CPH}
0	0	0	0	0	0	0	1	1	T_{CPH}
0	0	0	0	0	0	1	0	2	T_{CPH}
0	0	0	0	0	0	1	1	3	T_{CPH}
0	0	0	0	0	1	0	0	4	T_{CPH}
0	0	0	0	0	1	0	1	5	T_{CPH}
0	0	0	0	0	1	1	0	6	T_{CPH}
0	0	0	0	0	1	1	1	7	T_{CPH}
0	1	0	1	1	0	0	0	88	T_{CPH}
0	1	0	1	1	0	0	1	89	T_{CPH}
0	1	0	1	1	0	1	0	90	T_{CPH}
0	1	1	1	1	1	1	0	126	T_{CPH}
0	1	1	1	1	1	1	1	127	T_{CPH}
1	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***128***	T_{CPH}
1	1	1	1	1	0	0	0	248	T_{CPH}
1	1	1	1	1	0	0	1	249	T_{CPH}
1	1	1	1	1	0	1	0	250	T_{CPH}
1	1	1	1	1	0	1	1	251	T_{CPH}
1	1	1	1	1	1	0	0	252	T_{CPH}
1	1	1	1	1	1	0	1	253	T_{CPH}
1	1	1	1	1	1	1	0	254	T_{CPH}
1	1	1	1	1	1	1	1	255	T_{CPH}

T_{HS}= STHD [7:0]+ N (N depend on resolution).

Table 7. 6 Adjust start pulse position by dot

- **Register R03**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0
Default	–	0	0	1	1	0	1	1

Table 7. 7 Register R3 setting

STVD [6:0]: adjust first line position,

STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0	STV position adjust	Unit
0	0	0	0	0	0	0	0	T_H
0	0	0	0	0	0	1	1	T_H
0	0	0	0	0	1	0	2	T_H
0	0	0	0	0	1	1	3	T_H
0	0	0	0	1	0	0	4	T_H
0	0	0	0	1	0	1	5	T_H
0	0	0	0	1	1	0	6	T_H
0	0	0	0	1	1	1	7	T_H
				⋮				
0	0	1	1	0	0	0	24	T_H
0	0	1	1	0	0	1	25	T_H
0	0	1	1	0	1	0	26	T_H
0	***0***	***1***	***1***	***0***	***1***	***1***	***27***	***T_H***
0	0	1	1	1	0	0	28	T_H
0	0	1	1	1	0	1	29	T_H
0	0	1	1	1	1	0	30	T_H
0	0	1	1	1	1	1	31	T_H
				⋮				
1	1	1	1	0	0	0	120	T_H
1	1	1	1	0	0	1	121	T_H
1	1	1	1	0	1	0	122	T_H
1	1	1	1	0	1	1	123	T_H
1	1	1	1	1	0	0	124	T_H
1	1	1	1	1	0	1	125	T_H
1	1	1	1	1	1	0	126	T_H
1	1	1	1	1	1	1	127	T_H

T_{VS}= STVD [6:0] + N (N depend on resolution).

Table 7. 8 Adjust first line position by line

- **Register R04**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	EDGSL	LR	UD	CS	FRC	VS_POL	HS_POL
Default	–	0	1	0	1	1	0	0

Table 7. 9 Register R4 setting

EDGSL: Define input clock polarity.
EDGSL=L, CLK polarity is not inverted, latch data at CLK rising edge.
EDGSL=H, CLK polarity is inverted, latch data at CLK falling edge.

LR: Shift direction control.
LR=H: DIO1->SO1->• • • • • •->SO1200->DIO2
LR=L: DIO2->SO1200->• • • • • •->SO1->DIO1

UD: Gate Driver Up/down scan setting.
UD=H, reverse scan.
UD=L, normal scan.

CS: Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function.

FRC: Dithering ON/OFF control.
FRC=L, Dithering function disable.
FRC=H, Dithering function enable

VS_POL: VS polarity setting.
VS_POL=L, negative polarity.
VS_POL=H, positive polarity.

HS_POL: HS polarity setting.
HS_POL=L, negative polarity.
HS_POL=H, positive polarity.

- **Register R05**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	reserved	A_TIME1	A_TIME0
Default	–	–	–	–	–	–	0	0

Table 7. 10 Register R5 setting

A_TIME [1:0]: The blanking image display time is decided by A_TIME

00: blanking image display time is 4 VS time.

01: blanking image display time is 8 VS time.

10: blanking image display time is 16 VS time.

11: blanking image display time is 32 VS time.

- **Register R06**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWMA	FBA2	FBA1	FBA0	PWMB	FBB2	FBB1	FBB0
Default	0	0	1	0	0	0	1	0

Table 7. 11 Register R7 setting

FBA[2:0] : Adjust the feedback voltage of 1st PWM circuit.

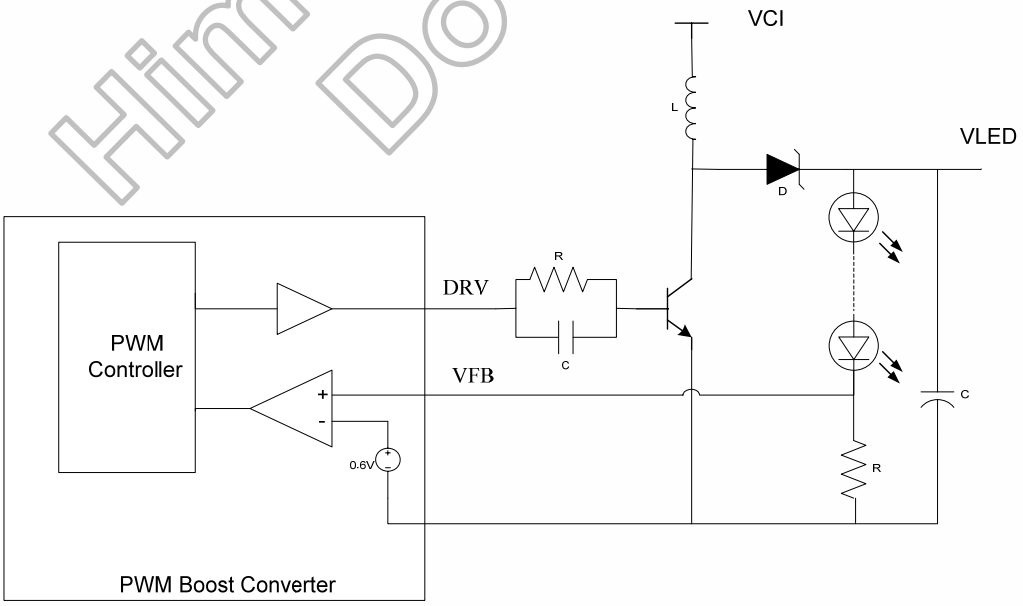
FBB[2:0] : Adjust the feedback voltage of 2nd PWM circuit.

FBA[2:0]	Voltage	FBB[2:0]	Voltage
000	0.4V	000	0.4V
001	0.45V	001	0.45V
010	0.5V	010	0.5V
011	0.55V	011	0.55V
100	0.6V	100	0.6V
101	0.65V	101	0.65V
110	0.7V	110	0.7V
111	0.75V	111	0.75V

PWMA : When PWMA=0, 1st PWM function is disabled.
When PWMA=1, 1st PWM function is enabled.

PWMB : When PWMB=0, 2nd PWM function is disabled.
When PWMB=1, 2nd PWM function is enabled.

PWM Boost Converter



- **Gamma Control1 Register R07**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	PKP02	PKP01	PKP00	PKP12	PKP11	PKP10
Default	–	–	1	1	0	1	0	0

- **Gamma Control2 Register R08**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	PKP22	PKP21	PKP20	PRP02	PRP01	PRP00
Default	–	–	0	0	1	0	0	0

- **Gamma Control3 Register R9**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PRP12	PRP11	PRP10	VRP04	VRP03	VRP02	VRP01	VRP00
Default	0	0	0	1	0	0	1	1

- **Gamma Control4 Register R10**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	Reserved	VRP14	VRP13	VRP12	VRP11	VRP10
Default	–	–	–	0	1	0	1	0

- **Gamma Control5 Register R11**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	PKN02	PKN01	PKN00	PKN12	PKN11	PKN10
Default	–	–	1	0	1	0	1	1

- **Gamma Control6 Register R12**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	PKN22	PKN21	PKN20	PRN02	PRN01	PRN00
Default	–	–	0	0	1	0	0	0

- **Gamma Control7 Register R13**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PRN12	PRN11	PRN10	VRN04	VRN03	VRN02	VRN01	VRN00
Default	0	0	0	1	0	0	0	1

- **Gamma Control8 Register R14**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	Reserved	VRN14	VRN13	VRN12	VRN11	VRN10
Default	–	–	–	1	0	0	0	0

- **Register R15**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	CEL	PPR	VPS	PA1	PA0	PWE	POR
Default	–	0	0	0	0	0	0	0

CEL: OTP cell selection
CEL=L, CELL1
CEL=H, CELL2

PPR: Control PPROG signal
PPR=L, PPROG signal disable
PPR=H, PPROG signal enable

VPS: Control VPP power internal switch
VPS=L, VPP connect to VCC(3.3V)
VPS=H, VPP connect to AVDD(6.5V)

PA[1:0]: Address signal for OTP cell
PA=00, OTP address 0~7 are selected
PA=01, OTP address 8~15 are selected
PA=10, OTP address 16~23 are selected
PA=11, OTP address 24~31 are selected

OTP Address Table:

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cell 1	PKP02	PKP01	PKP00	PKP12	PKP11	PKP10	PKP22	PKP21	PKP20		PRP02	PRP01	PRP00	PRP12	PRP11	PRP10
Cell 2	PKN02	PKN01	PKN00	PKN12	PKN11	PKN10	PKN22	PKN21	PKN20		PRN02	PRN01	PRN00	PRN12	PRN11	PRN10
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cell 1	VRP04	VRP03	VRP02	VRP01	VRP00	VRP14	VRP13	VRP12	VRP11	VRP10						
Cell 2	VRN04	VRN03	VRN02	VRN01	VRN00	VRN14	VRN13	VRN12	VRN11	VRN10						

PWE: Control PWE signal for OTP cell
PWE=L, PWE signal disable
PWE=H, PWE signal enable

POR: Control POR signal for OTP cell
POR=L, POR signal disable
POR=H, POR signal enable

- **OTP Read Out Value0 Register R16**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL1-31	CELL1-30	CELL1-29	CELL1-28	CELL1-27	CELL1-26	CELL1-25	CELL1-24
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value1 Register R17**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL1-23	CELL1-22	CELL1-21	CELL1-20	CELL1-19	CELL1-18	CELL1-17	CELL1-16
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value2 Register R18**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL1-15	CELL1-14	CELL1-13	CELL1-12	CELL1-11	CELL1-10	CELL1-9	CELL1-8
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value3 Register R19**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL1-7	CELL1-6	CELL1-5	CELL1-4	CELL1-3	CELL1-2	CELL1-1	CELL1-0
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value4 Register R20**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL2-31	CELL2-30	CELL2-29	CELL2-28	CELL2-27	CELL2-26	CELL2-25	CELL2-24
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value5 Register R21**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL2-23	CELL2-22	CELL2-21	CELL2-20	CELL2-19	CELL2-18	CELL2-17	CELL2-16
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value6 Register R22**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL2-15	CELL2-14	CELL2-13	CELL2-12	CELL2-11	CELL2-10	CELL2-9	CELL2-8
Default	–	–	–	–	–	–	–	–

- **OTP Read Out Value7 Register R23**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CELL2-7	CELL2-6	CELL2-5	CELL2-4	CELL2-3	CELL2-2	CELL2-1	CELL2-0
Default	–	–	–	–	–	–	–	–

8. Power ON/OFF sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: (VCC, GND) → (VDDA, VSSA) → (V1 to V10)
Power OFF: (V1 to V10) → (VDDA, VSSA) → (VCC, GND)

8.1 Power ON Control

HX8262-A has a power ON sequence control function. When power is ON, blanking data is output for 4-frames (default value) first, from the falling edge of the following VS signal. It can be defined in register R5 A_TIME[1:0].The blanking data would be gray level 255 for normally white panel.

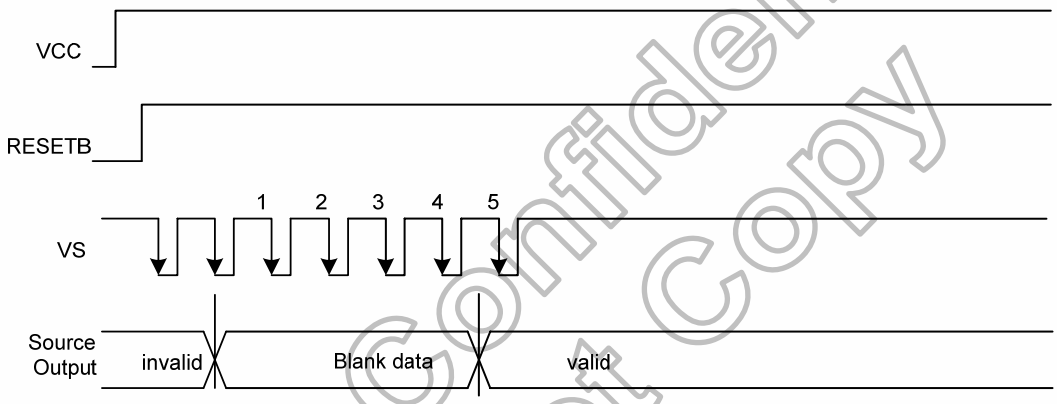


Figure 8.1 Power on control for Auto Mode

8.2 Reset when power on

HX8262-A is internally initialized by the global reset signal, RESETB. The reset input must be held low for at least 1ms after power is stable.

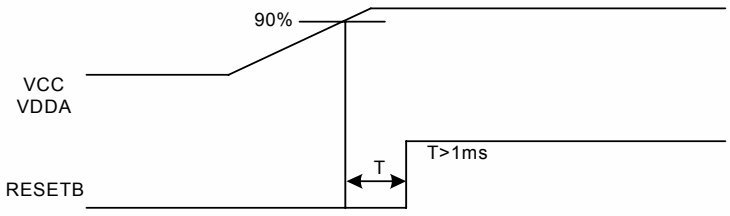


Figure 8.2 RESETB control after power stable

9. DC Characteristics

9.1 Absolute Maximum Rating (GND=VSSA=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VCC	-0.3	-	+7.0	V
Power supply voltage 2	VDDA	-0.3	-	+13.5	V
Logic Output Voltage	V_{OUT}	-0.3	-	+7.0	V
Input voltage	Vin	-0.3	-	VDDA+0.3	V
Operation temperature	T_{OPR}	-40	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: (1)All of the voltages listed above are with respective to GND=VSSA=0V.
(2)Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

9.2 DC Electrical Characteristics (GND=VSSA=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	2.7	3.3	3.6	V	-
Power supply voltage	VDDA	6.5	8.4	13.5	V	-
Low level input voltage	V_{IL}	0	-	0.3VCC	V	-
High level input voltage	V_{IH}	0.7VCC	-	VCC	V	-
Output low voltage	V_{OL}	0	-	0.2VCC	V	I_{OL}=400μA
Output high voltage	V_{OH}	0.8VCC	-	VCC	V	I_{OH}=-400μA
Input leakage current	I_{IN}	-1	-	+1	μA	No pull up or pull down.
Output voltage deviation	V_{VD}	-	±20	-	mV	SO1~SO1200
DC offset	V_{OS}	-	-	±20	mV	SO1~SO1200, V_{IN}=0.1~13.4V,
Output leakage current	I_O	-1	-	+1	μA	SO1~SO1200 at high impedance
Pull high resistance	R_H	600	900	1200	kΩ	RESETB,TXLR, CS, SPCK, SPEN, SDI, LR, VSET, VS, HS
Pull low resistance	R_L	600	900	1200	kΩ	Dx[7:0] (x=2,1,0), DEN,RESL[1:0], EDGSL, UD, TEST[1:0], TESTG[1:0], CLK
Output current	I_{OH}	40	60	-	μA	SO1~SO1200, V_O =9.9V vs. 9V, VDDA=10V
Output current	I_{OL}	40	60	-	μA	SO1~SO1200, Vo=0.1V vs. 1.0V, VDDA=10V
Analog operating current	I_{DD}	-	TBD	-	mA	F_{cph}=33MHz, f_{HS}=40.1KHz, black pattern, VDDA=8.4V, RL=2K, CL=60pF
Digital operating current	I_{CC}	-	TBD	-	mA	F_{cph}=33MHz, f_{HS}=40.1KHz, black pattern, VCC=3.3V
Analog standby current	I_{VDDA}	-	-	TBD	μA	All LCD outputs are High-Z.
Digital standby current	I_{VCC}	-	-	TBD	μA	All inputs are stopped and outputs are High-Z.

10. AC Characteristics

10.1 Input signal characteristics

10.1.1 AC Electrical Characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
HS setup time	T_{hst}	6	-	-	ns
HS hold time	T_{hhd}	6	-	-	ns
VS setup time	T_{vst}	6	-	-	ns
VS hold time	T_{vhd}	6	-	-	ns
Data setup time	T_{dsu}	6	-	-	ns
Data hold time	T_{dhd}	6	-	-	ns
DE setup time	T_{esu}	6	-	-	ns
Source output settling time	T_{ST}	-	-	15	µs
Source output loading R	R_{SL}	-	2	-	K ohm
Source output loading C	C_{SL}	-	60	-	pF
POL output delay time	T_{DP}	-	-	40	ns

10.1.2 Resolution：800x480

- **sync mode**

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	33.26	-	MHz
CLK period	T_{CPH}	-	30.06	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1056	-	T_{CPH}
HS pulse width	T_{WH}	1	128	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+88(i)			T_{CPH}
HS Active Time	T_{HA}	-	800	-	T_{CPH}
VS period	T_V	-	525	-	T_H
VS pulse width	T_{WV}	1	2	-	T_H
VS-DE time	T_{VS}	STVD[6:0]+8			T_H
VS Active Time	T_{VA}	-	480	-	T_H

- **DE mode**

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	33.26	-	MHz
CLK period	T_{CPH}	-	30.06	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1000	1056	1200	T_{CPH}
DE pulse width	T_{DH}	-	800	-	T_{CPH}
DE frame blanking	T_{HS}	10	45	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{EP}	-	480	-	$T_{DEH}+T_{DEL}$

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	150	-	T_{CPH}
CKV pulse width	T_{CKV}	-	133	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	40	-	T_{CPH}
DE(internal)-OEV time	T_3	-	23	-	T_{CPH}
DE(internal)-POL time	T_4	-	157	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

(i). $T_{HS}+T_{HA}<T_H$

10.1.3 Resolution：800x600

- **sync mode**

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	39.79	-	MHz
CLK period	T_{CPH}	-	25.13	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1056	-	T_{CPH}
HS pulse width	T_{WH}	1	128	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+88(i)			T_{CPH}
HS Active Time	T_{HA}	-	800	-	T_{CPH}
VS period	T_V	-	628	-	T_H
VS pulse width	T_{WV}	1	4	-	T_H
VS-DE time	T_{VS}	STVD[6:0]+0			T_H
VS Active Time	T_{VA}	-	600	-	T_H

- **DE mode**

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	39.79	-	MHz
CLK period	T_{CPH}	-	25.13	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1000	1056	1200	T_{CPH}
DE pulse width	T_{DH}	-	800	-	T_{CPH}
DE frame blanking	T_{HS}	10	28	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{EP}	-	600	-	$T_{DEH}+T_{DEL}$

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	150	-	T_{CPH}
CKV pulse width	T_{CKV}	-	133	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	40	-	T_{CPH}
DE(internal)-OEV time	T_3	-	23	-	T_{CPH}
DE(internal)-POL time	T_4	-	157	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

(i). $T_{HS}+T_{HA}<T_H$

10.1.4 Resolution：400x240

- **Sync mode**

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	8.3	-	MHz
CLK period	T_{CPH}	-	120.47	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	528	-	T_{CPH}
HS pulse width	T_{WH}	1	46	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]-26(i) (ii)			T_{CPH}
HS Active Time	T_{HA}	-	400	-	T_{CPH}
VS period	T_V	-	262	-	T_H
VS pulse width	T_{WV}	1	2	-	T_H
VS-DE time	T_{VS}	STVD[6:0]-9(iii)			T_H
VS Active Time	T_{VA}	-	240	-	T_H

- **DE mode**

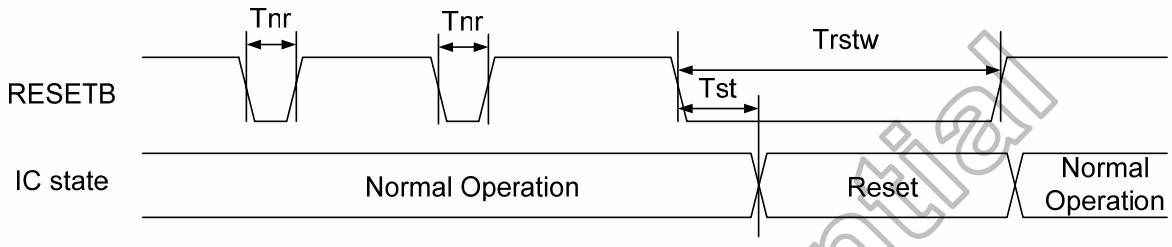
PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	8.3	-	MHz
CLK period	T_{CPH}	-	120.47	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	500	528	600	T_{CPH}
DE pulse width	T_{DH}	-	400	-	T_{CPH}
DE frame blanking	T_{HS}	10	22	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{EP}	-	240	-	$T_{DEH}+T_{DEL}$

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	43	-	T_{CPH}
CKV pulse width	T_{CKV}	-	39	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	14	-	T_{CPH}
DE(internal)-OEV time	T_3	-	10	-	T_{CPH}
DE(internal)-POL time	T_4	-	45	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

(i). $T_{HS}+T_{HA}<T_H$
(ii). T_{HS} must be greater than 8 → STHD[7:0] must be greater than 34
(iii). T_{VS} must be greater than 0 → STVD[6:0] must be greater than 9

10.1.5 Hardware reset timing

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
RESETB low pulse width	T_{rstw}	10	-	-	µs
Negative noise pulse width	T_{nr}		-	2	µs
Reset start time	T_{st}	2	-		µs



11. Waveform

11.1 Timing Controller Timing Chart

11.1.1 Clock and Data input waveforms

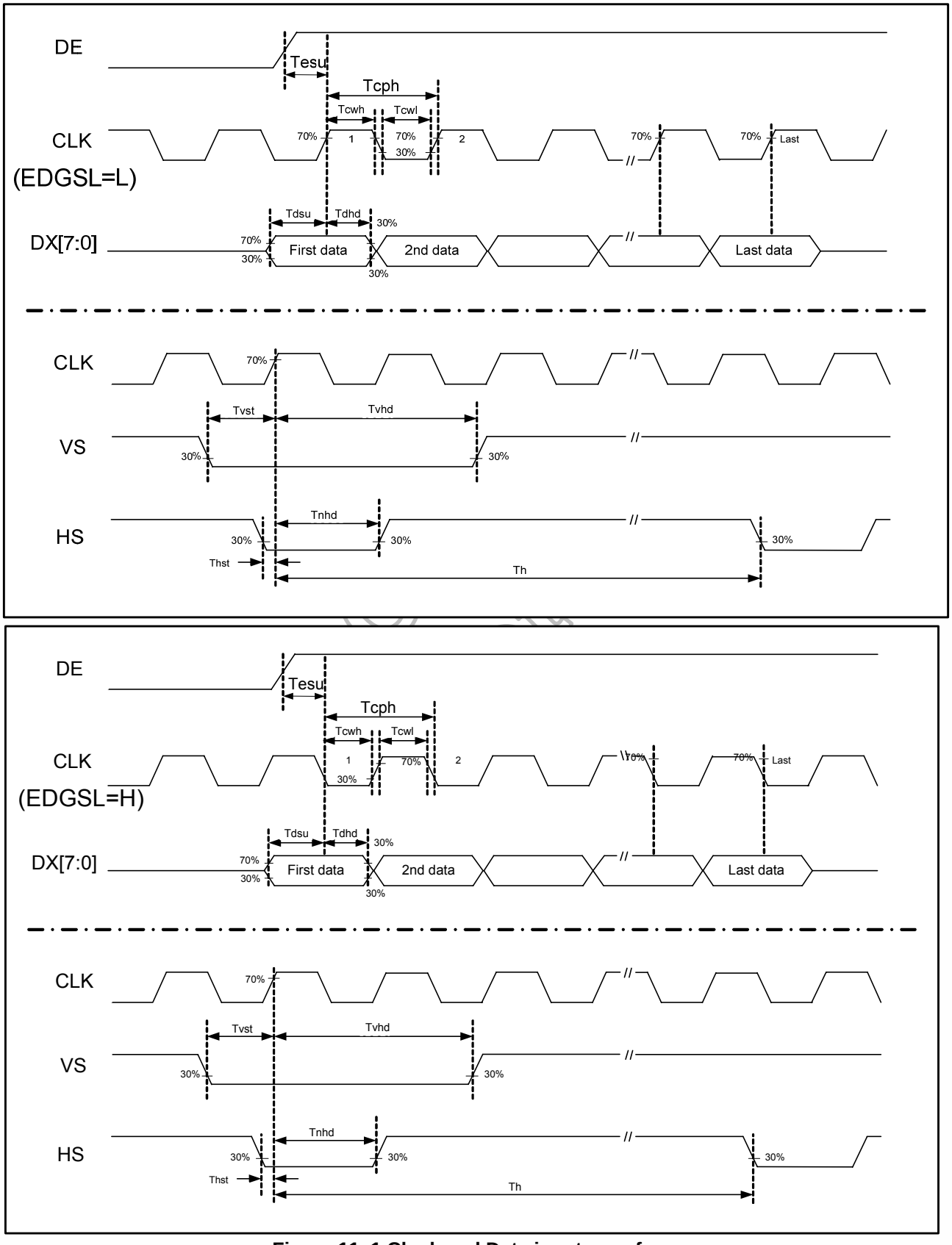


Figure 11. 1 Clock and Data input waveforms.

11.1.2 Data input format

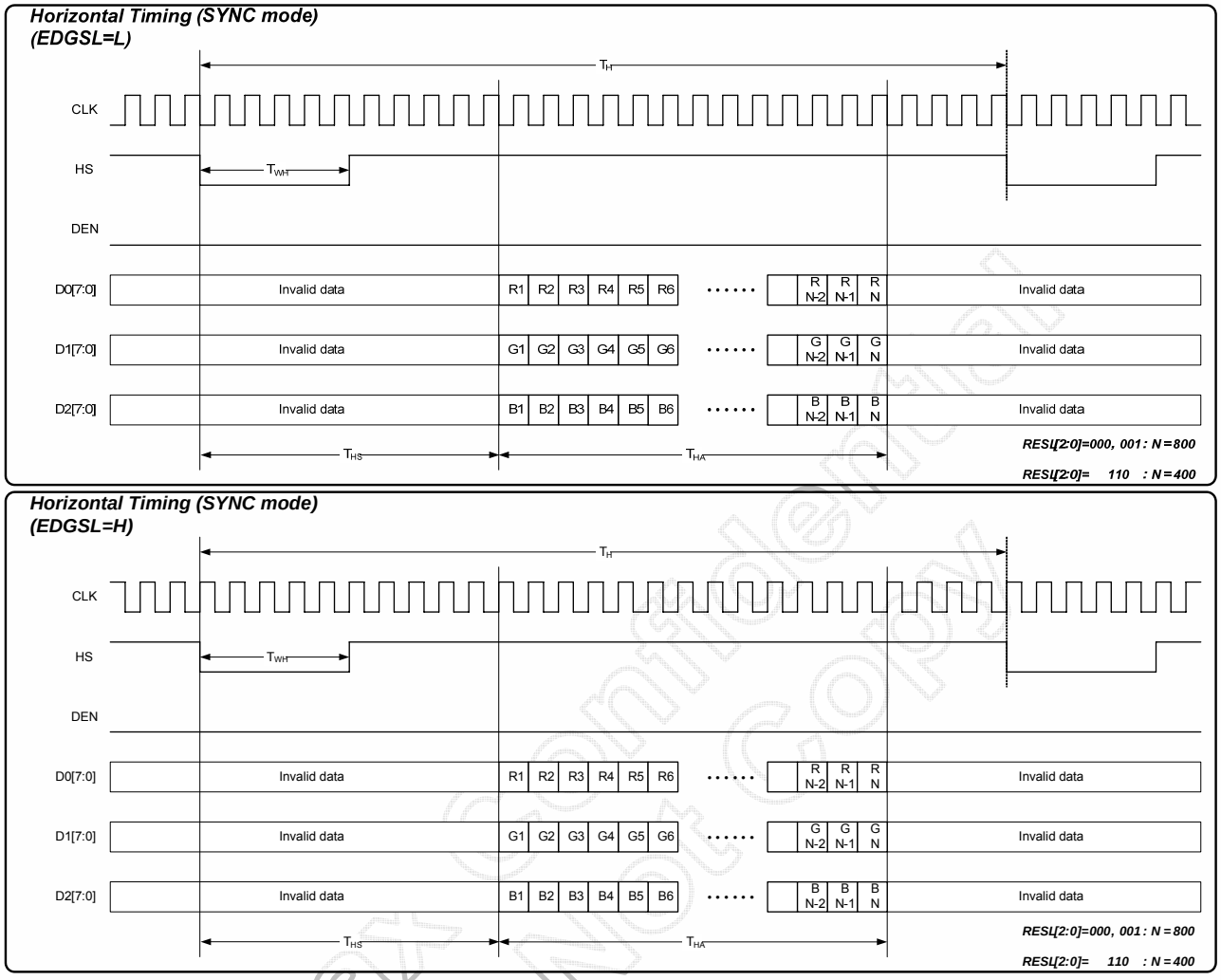


Figure 11. 2 SYNC Mode Horizontal Data Format

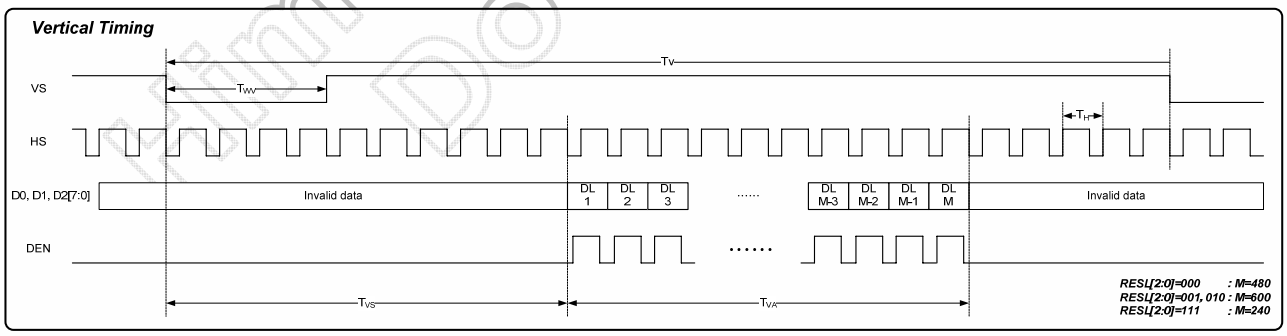


Figure 11. 3 SYNC Mode Vertical Data Format

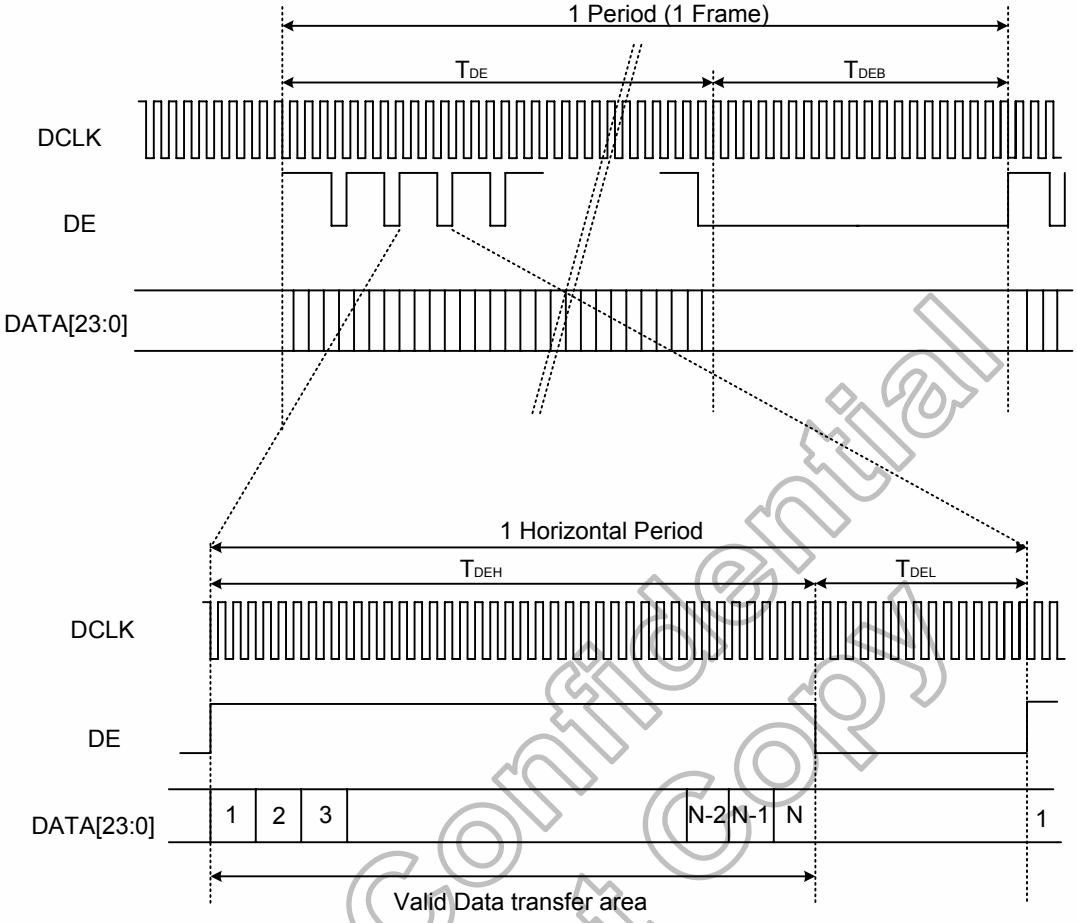


Figure 11. 4 DE Mode Data Format

11.1.3 Digital Output timing waveforms

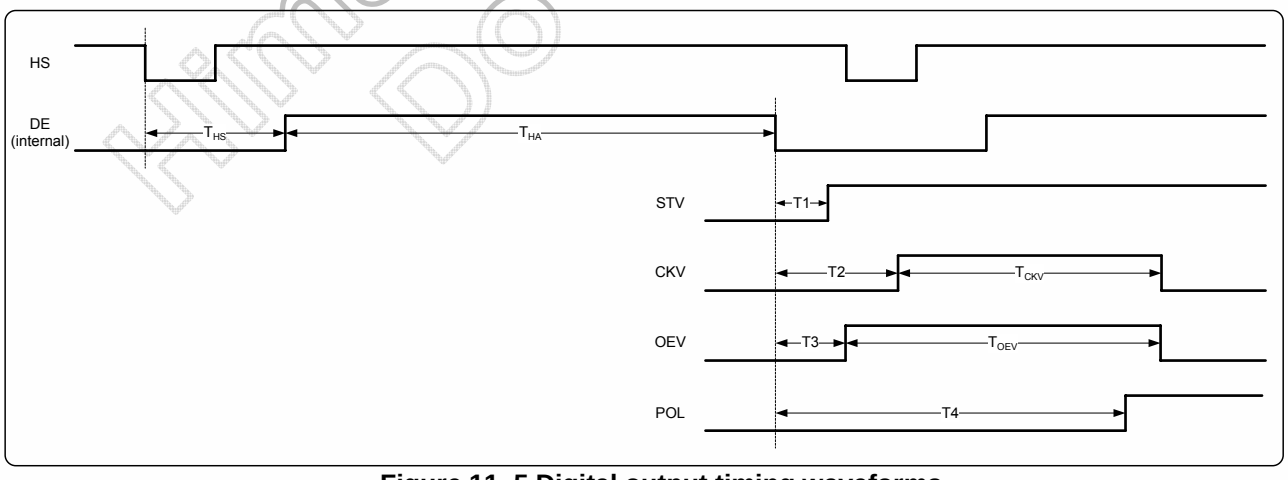


Figure 11. 5 Digital output timing waveforms

11.3 Output Timing Chart

11.3.1 Source Driver output timing waveforms

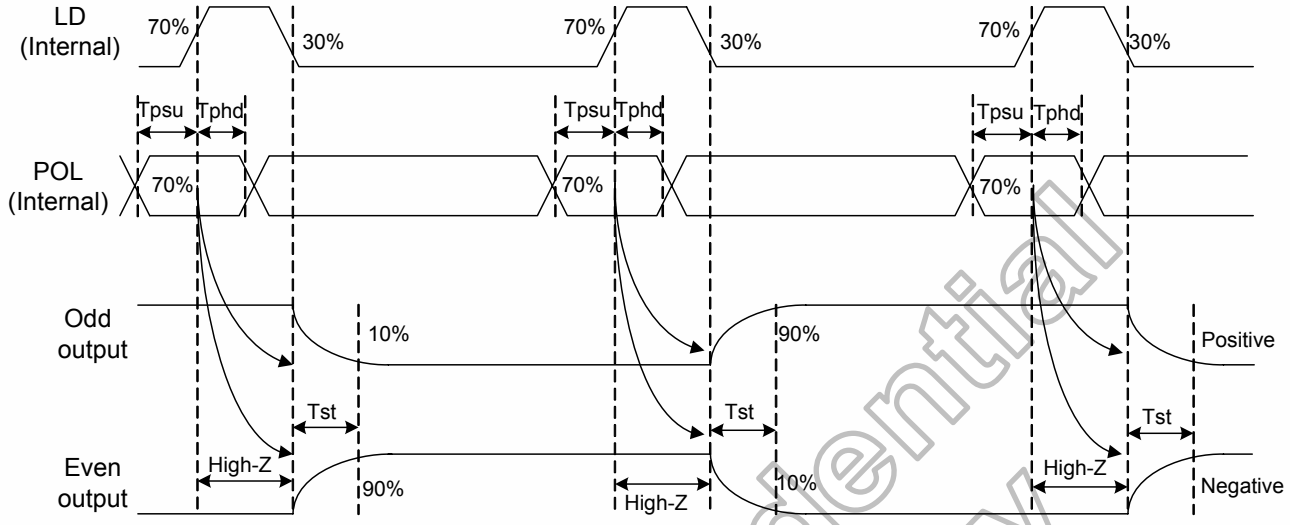
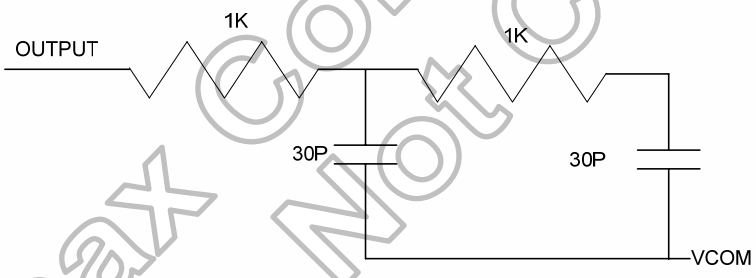


Figure 11. 10 LD and Source Data Output timing waveforms

Source Output load condition:



12. SPI timing characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	200	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

- **SPI timing**

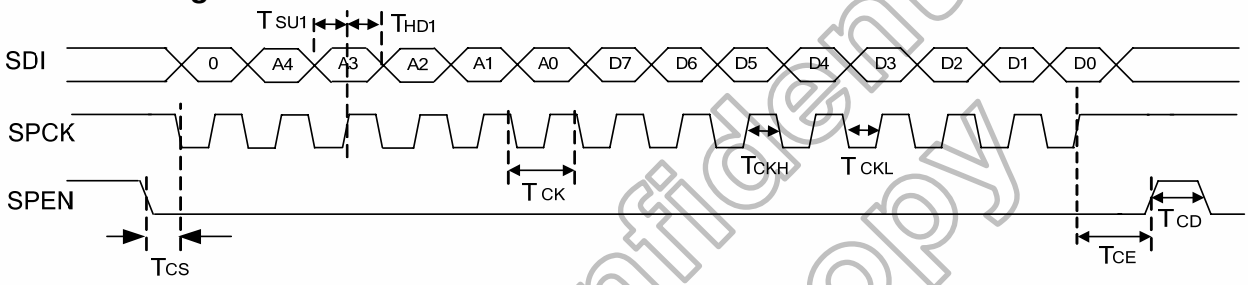
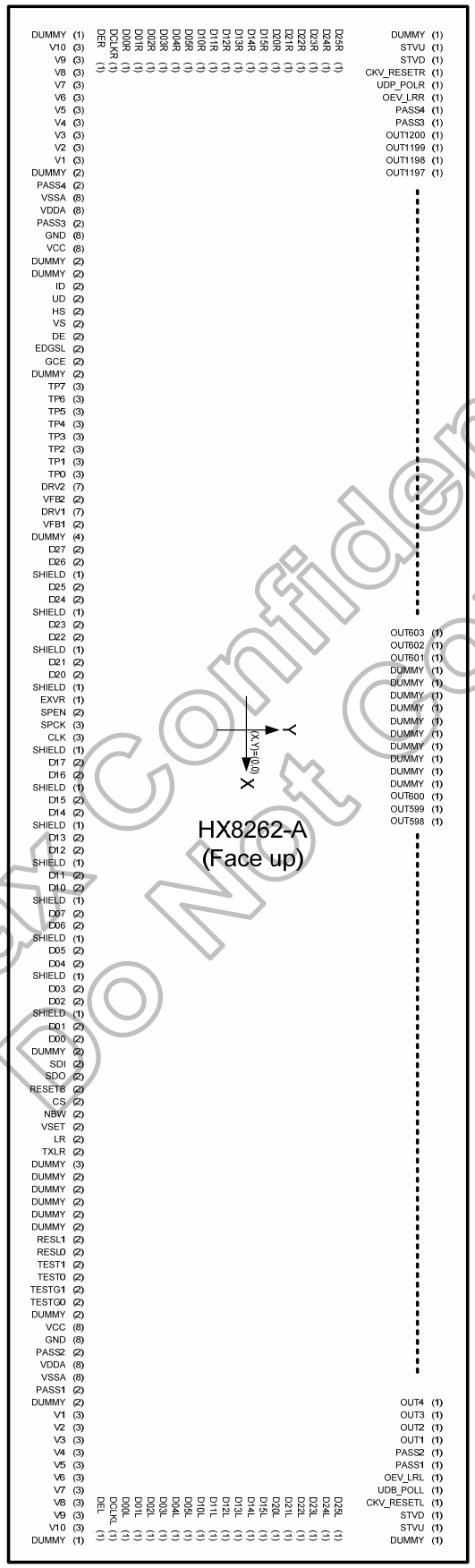


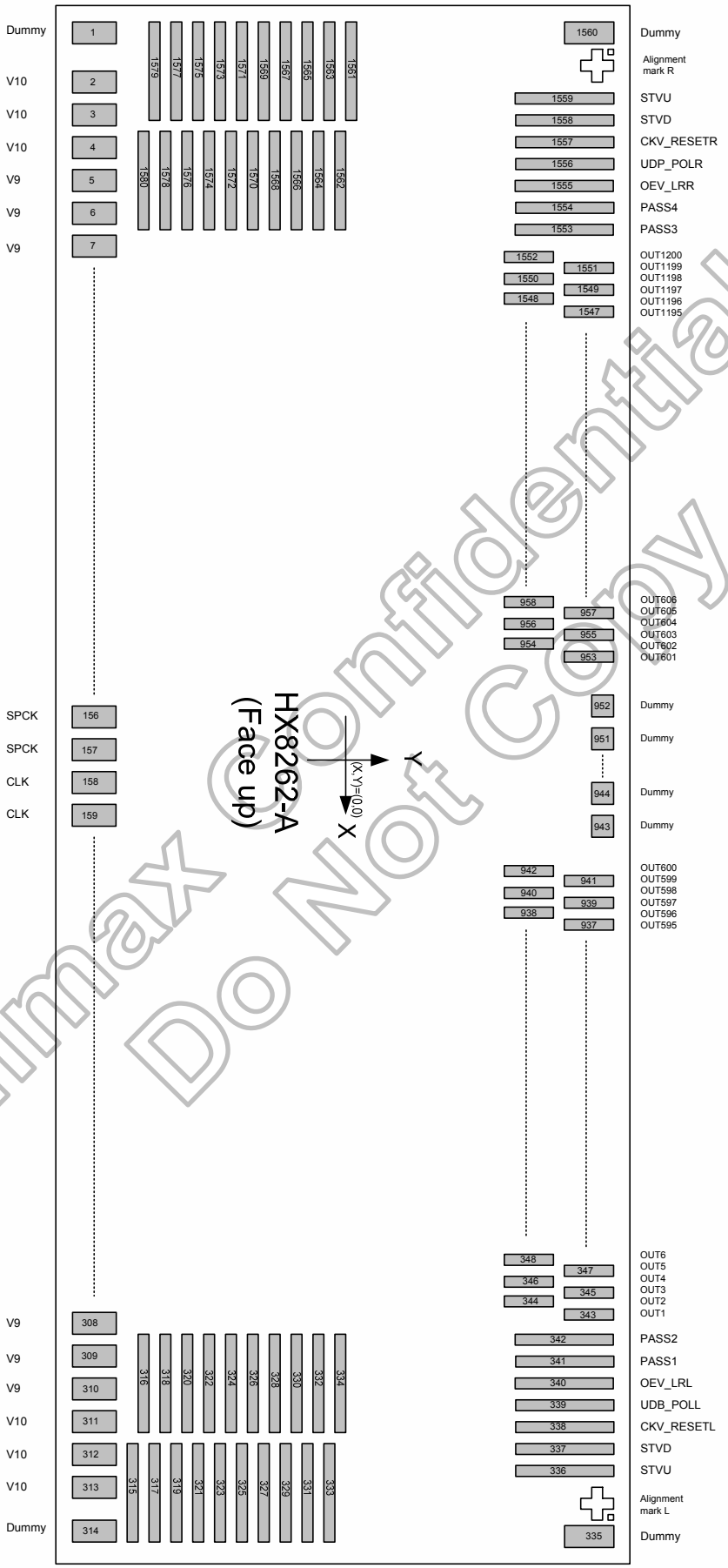
Figure 12. 4 SPI timing (write data)

- SPEN must keep low more than 13 clock after SDI starting to write data.
- Write SPI commend must after RESET rising more than 10 us.

13. Pin Assignment (IC face view)



14. Package Outline



14.1 Pad Coordinate

No.	Name	X	Y
1	DUMMY	-11050	-470
2	V10	-10885	-470
3	V10	-10815	-470
4	V10	-10745	-470
5	V9	-10675	-470
6	V9	-10605	-470
7	V9	-10535	-470
8	V8	-10465	-470
9	V8	-10395	-470
10	V8	-10325	-470
11	V7	-10255	-470
12	V7	-10185	-470
13	V7	-10115	-470
14	V6	-10045	-470
15	V6	-9975	-470
16	V6	-9905	-470
17	V5	-9835	-470
18	V5	-9765	-470
19	V5	-9695	-470
20	V4	-9625	-470
21	V4	-9555	-470
22	V4	-9485	-470
23	V3	-9415	-470
24	V3	-9345	-470
25	V3	-9275	-470
26	V2	-9205	-470
27	V2	-9135	-470
28	V2	-9065	-470
29	V1	-8995	-470
30	V1	-8925	-470
31	V1	-8855	-470
32	DUMMY	-8785	-470
33	DUMMY	-8715	-470
34	PASS4	-8645	-470
35	PASS4	-8575	-470
36	VSSA	-8505	-470
37	VSSA	-8435	-470
38	VSSA	-8365	-470
39	VSSA	-8295	-470
40	VSSA	-8225	-470
41	VSSA	-8155	-470
42	VSSA	-8085	-470
43	VSSA	-8015	-470
44	VDDA	-7945	-470
45	VDDA	-7875	-470
46	VDDA	-7805	-470
47	VDDA	-7735	-470
48	VDDA	-7665	-470
49	VDDA	-7595	-470
50	VDDA	-7525	-470

No.	Name	X	Y
51	VDDA	-7455	-470
52	PASS3	-7385	-470
53	PASS3	-7315	-470
54	VCC	-7245	-470
55	VCC	-7175	-470
56	VCC	-7105	-470
57	VCC	-7035	-470
58	VCC	-6965	-470
59	VCC	-6895	-470
60	VCC	-6825	-470
61	VCC	-6755	-470
62	GND	-6685	-470
63	GND	-6615	-470
64	GND	-6545	-470
65	GND	-6475	-470
66	GND	-6405	-470
67	GND	-6335	-470
68	GND	-6265	-470
69	GND	-6195	-470
70	DUMMY	-6125	-470
71	DUMMY	-6055	-470
72	DUMMY	-5985	-470
73	DUMMY	-5915	-470
74	ID0	-5845	-470
75	ID0	-5775	-470
76	UD	-5705	-470
77	UD	-5635	-470
78	HS	-5565	-470
79	HS	-5495	-470
80	VS	-5425	-470
81	VS	-5355	-470
82	DEN	-5285	-470
83	DEN	-5215	-470
84	EDGSL	-5145	-470
85	EDGSL	-5075	-470
86	GCE	-5005	-470
87	GCE	-4935	-470
88	TP7	-4865	-470
89	TP7	-4795	-470
90	TP7	-4725	-470
91	TP6	-4655	-470
92	TP6	-4585	-470
93	TP6	-4515	-470
94	TP5	-4445	-470
95	TP5	-4375	-470
96	TP5	-4305	-470
97	TP4	-4235	-470
98	TP4	-4165	-470
99	TP4	-4095	-470
100	TP3	-4025	-470

No.	Name	X	Y
101	TP3	-3955	-470
102	TP3	-3885	-470
103	TP2	-3815	-470
104	TP2	-3745	-470
105	TP2	-3675	-470
106	TP1	-3605	-470
107	TP1	-3535	-470
108	TP1	-3465	-470
109	TP0	-3395	-470
110	TP0	-3325	-470
111	TP0	-3255	-470
112	DRV2	-3185	-470
113	DRV2	-3115	-470
114	DRV2	-3045	-470
115	DRV2	-2975	-470
116	DRV2	-2905	-470
117	DRV2	-2835	-470
118	DRV2	-2765	-470
119	VFB2	-2695	-470
120	VFB2	-2625	-470
121	DRV1	-2555	-470
122	DRV1	-2485	-470
123	DRV1	-2415	-470
124	DRV1	-2345	-470
125	DRV1	-2275	-470
126	DRV1	-2205	-470
127	DRV1	-2135	-470
128	VFB1	-2065	-470
129	VFB1	-1995	-470
130	DUMMY	-1925	-470
131	DUMMY	-1855	-470
132	D27	-1785	-470
133	D27	-1715	-470
134	D26	-1645	-470
135	D26	-1575	-470
136	SHIELD	-1505	-470
137	D25	-1435	-470
138	D25	-1365	-470
139	D24	-1295	-470
140	D24	-1225	-470
141	SHIELD	-1155	-470
142	D23	-1085	-470
143	D23	-1015	-470
144	D22	-945	-470
145	D22	-875	-470
146	SHIELD	-805	-470
147	D21	-735	-470
148	D21	-665	-470
149	D20	-595	-470
150	D20	-525	-470

No.	Name	X	Y
151	SHIELD	-455	-470
152	EXVR	-385	-470
153	SPEN	-315	-470
154	SPEN	-245	-470
155	SPCK	-175	-470
156	SPCK	-105	-470
157	SPCK	-35	-470
158	CLK	35	-470
159	CLK	105	-470
160	CLK	175	-470
161	SHIELD	245	-470
162	D17	315	-470
163	D17	385	-470
164	D16	455	-470
165	D16	525	-470
166	SHIELD	595	-470
167	D15	665	-470
168	D15	735	-470
169	D14	805	-470
170	D14	875	-470
171	SHIELD	945	-470
172	D13	1015	-470
173	D13	1085	-470
174	D12	1155	-470
175	D12	1225	-470
176	SHIELD	1295	-470
177	D11	1365	-470
178	D11	1435	-470
179	D10	1505	-470
180	D10	1575	-470
181	SHIELD	1645	-470
182	D07	1715	-470
183	D07	1785	-470
184	D06	1855	-470
185	D06	1925	-470
186	SHIELD	1995	-470
187	D05	2065	-470
188	D05	2135	-470
189	D04	2205	-470
190	D04	2275	-470
191	SHIELD	2345	-470
192	D03	2415	-470
193	D03	2485	-470
194	D02	2555	-470
195	D02	2625	-470
196	SHIELD	2695	-470
197	D01	2765	-470
198	D01	2835	-470
199	D00	2905	-470
200	D00	2975	-470

No.	Name	X	Y
201	DUMMY	3045	-470
202	DUMMY	3115	-470
203	SDI	3185	-470
204	SDI	3255	-470
205	SDO	3325	-470
206	SDO	3395	-470
207	RESETB	3465	-470
208	RESETB	3535	-470
209	CS	3605	-470
210	CS	3675	-470
211	NBW	3745	-470
212	NBW	3815	-470
213	VSET	3885	-470
214	VSET	3955	-470
215	LR	4025	-470
216	LR	4095	-470
217	TXLR	4165	-470
218	TXLR	4235	-470
219	DUMMY	4305	-470
220	DUMMY	4375	-470
221	DUMMY	4445	-470
222	DUMMY	4515	-470
223	DUMMY	4585	-470
224	DUMMY	4655	-470
225	DUMMY	4725	-470
226	DUMMY	4795	-470
227	DUMMY	4865	-470
228	DUMMY	4935	-470
229	DUMMY	5005	-470
230	DUMMY	5075	-470
231	DUMMY	5145	-470
232	RESL1	5215	-470
233	RESL1	5285	-470
234	RESL0	5355	-470
235	RESL0	5425	-470
236	TEST1	5495	-470
237	TEST1	5565	-470
238	TEST0	5635	-470
239	TEST0	5705	-470
240	TESTG1	5775	-470
241	TESTG1	5845	-470
242	TESTG0	5915	-470
243	TESTG0	5985	-470
244	DUMMY	6055	-470
245	DUMMY	6125	-470
246	GND	6195	-470
247	GND	6265	-470
248	GND	6335	-470
249	GND	6405	-470
250	GND	6475	-470

No.	Name	X	Y
251	GND	6545	-470
252	GND	6615	-470
253	GND	6685	-470
254	VCC	6755	-470
255	VCC	6825	-470
256	VCC	6895	-470
257	VCC	6965	-470
258	VCC	7035	-470
259	VCC	7105	-470
260	VCC	7175	-470
261	VCC	7245	-470
262	PASS2	7315	-470
263	PASS2	7385	-470
264	VDDA	7455	-470
265	VDDA	7525	-470
266	VDDA	7595	-470
267	VDDA	7665	-470
268	VDDA	7735	-470
269	VDDA	7805	-470
270	VDDA	7875	-470
271	VDDA	7945	-470
272	VSSA	8015	-470
273	VSSA	8085	-470
274	VSSA	8155	-470
275	VSSA	8225	-470
276	VSSA	8295	-470
277	VSSA	8365	-470
278	VSSA	8435	-470
279	VSSA	8505	-470
280	PASS1	8575	-470
281	PASS1	8645	-470
282	DUMMY	8715	-470
283	DUMMY	8785	-470
284	V1	8855	-470
285	V1	8925	-470
286	V1	8995	-470
287	V2	9065	-470
288	V2	9135	-470
289	V2	9205	-470
290	V3	9275	-470
291	V3	9345	-470
292	V3	9415	-470
293	V4	9485	-470
294	V4	9555	-470
295	V4	9625	-470
296	V5	9695	-470
297	V5	9765	-470
298	V5	9835	-470
299	V6	9905	-470
300	V6	9975	-470

No.	Name	X	Y
301	V6	10045	-470
302	V7	10115	-470
303	V7	10185	-470
304	V7	10255	-470
305	V8	10325	-470
306	V8	10395	-470
307	V8	10465	-470
308	V9	10535	-470
309	V9	10605	-470
310	V9	10675	-470
311	V10	10745	-470
312	V10	10815	-470
313	V10	10885	-470
314	DUMMY	11050	-470
315	DEL	10975	-395
316	DCLKL	10755	-375
317	D00L	10975	-355
318	D01L	10755	-335
319	D02L	10975	-315
320	D03L	10755	-295
321	D04L	10975	-275
322	D05L	10755	-255
323	D10L	10975	-235
324	D11L	10755	-215
325	D12L	10975	-195
326	D13L	10755	-175
327	D14L	10975	-155
328	D15L	10755	-135
329	D20L	10975	-115
330	D21L	10755	-95
331	D22L	10975	-75
332	D23L	10755	-55
333	D24L	10975	-35
334	D25L	10755	-15
335	DUMMY	11050	465
336	STVU	10870	415
337	STVD	10830	415
338	CKV_RESETL	10790	415
339	UDB_POLL	10750	415
340	OEV_LRL	10710	415
341	PASS1	10670	415
342	PASS2	10630	415
343	OUT1	10567	465
344	OUT2	10551.5	345
345	OUT3	10536	465
346	OUT4	10520.5	345
347	OUT5	10505	465
348	OUT6	10489.5	345
349	OUT7	10474	465
350	OUT8	10458.5	345

No.	Name	X	Y
351	OUT9	10443	465
352	OUT10	10427.5	345
353	OUT11	10412	465
354	OUT12	10396.5	345
355	OUT13	10381	465
356	OUT14	10365.5	345
357	OUT15	10350	465
358	OUT16	10334.5	345
359	OUT17	10319	465
360	OUT18	10303.5	345
361	OUT19	10288	465
362	OUT20	10272.5	345
363	OUT21	10257	465
364	OUT22	10241.5	345
365	OUT23	10226	465
366	OUT24	10210.5	345
367	OUT25	10195	465
368	OUT26	10179.5	345
369	OUT27	10164	465
370	OUT28	10148.5	345
371	OUT29	10133	465
372	OUT30	10117.5	345
373	OUT31	10102	465
374	OUT32	10086.5	345
375	OUT33	10071	465
376	OUT34	10055.5	345
377	OUT35	10040	465
378	OUT36	10024.5	345
379	OUT37	10009	465
380	OUT38	9993.5	345
381	OUT39	9978	465
382	OUT40	9962.5	345
383	OUT41	9947	465
384	OUT42	9931.5	345
385	OUT43	9916	465
386	OUT44	9900.5	345
387	OUT45	9885	465
388	OUT46	9869.5	345
389	OUT47	9854	465
390	OUT48	9838.5	345
391	OUT49	9823	465
392	OUT50	9807.5	345
393	OUT51	9792	465
394	OUT52	9776.5	345
395	OUT53	9761	465
396	OUT54	9745.5	345
397	OUT55	9730	465
398	OUT56	9714.5	345
399	OUT57	9699	465
400	OUT58	9683.5	345

No.	Name	X	Y
401	OUT59	9668	465
402	OUT60	9652.5	345
403	OUT61	9637	465
404	OUT62	9621.5	345
405	OUT63	9606	465
406	OUT64	9590.5	345
407	OUT65	9575	465
408	OUT66	9559.5	345
409	OUT67	9544	465
410	OUT68	9528.5	345
411	OUT69	9513	465
412	OUT70	9497.5	345
413	OUT71	9482	465
414	OUT72	9466.5	345
415	OUT73	9451	465
416	OUT74	9435.5	345
417	OUT75	9420	465
418	OUT76	9404.5	345
419	OUT77	9389	465
420	OUT78	9373.5	345
421	OUT79	9358	465
422	OUT80	9342.5	345
423	OUT81	9327	465
424	OUT82	9311.5	345
425	OUT83	9296	465
426	OUT84	9280.5	345
427	OUT85	9265	465
428	OUT86	9249.5	345
429	OUT87	9234	465
430	OUT88	9218.5	345
431	OUT89	9203	465
432	OUT90	9187.5	345
433	OUT91	9172	465
434	OUT92	9156.5	345
435	OUT93	9141	465
436	OUT94	9125.5	345
437	OUT95	9110	465
438	OUT96	9094.5	345
439	OUT97	9079	465
440	OUT98	9063.5	345
441	OUT99	9048	465
442	OUT100	9032.5	345
443	OUT101	9017	465
444	OUT102	9001.5	345
445	OUT103	8986	465
446	OUT104	8970.5	345
447	OUT105	8955	465
448	OUT106	8939.5	345
449	OUT107	8924	465
450	OUT108	8908.5	345

No.	Name	X	Y
451	OUT109	8893	465
452	OUT110	8877.5	345
453	OUT111	8862	465
454	OUT112	8846.5	345
455	OUT113	8831	465
456	OUT114	8815.5	345
457	OUT115	8800	465
458	OUT116	8784.5	345
459	OUT117	8769	465
460	OUT118	8753.5	345
461	OUT119	8738	465
462	OUT120	8722.5	345
463	OUT121	8707	465
464	OUT122	8691.5	345
465	OUT123	8676	465
466	OUT124	8660.5	345
467	OUT125	8645	465
468	OUT126	8629.5	345
469	OUT127	8614	465
470	OUT128	8598.5	345
471	OUT129	8583	465
472	OUT130	8567.5	345
473	OUT131	8552	465
474	OUT132	8536.5	345
475	OUT133	8521	465
476	OUT134	8505.5	345
477	OUT135	8490	465
478	OUT136	8474.5	345
479	OUT137	8459	465
480	OUT138	8443.5	345
481	OUT139	8428	465
482	OUT140	8412.5	345
483	OUT141	8397	465
484	OUT142	8381.5	345
485	OUT143	8366	465
486	OUT144	8350.5	345
487	OUT145	8335	465
488	OUT146	8319.5	345
489	OUT147	8304	465
490	OUT148	8288.5	345
491	OUT149	8273	465
492	OUT150	8257.5	345
493	OUT151	8242	465
494	OUT152	8226.5	345
495	OUT153	8211	465
496	OUT154	8195.5	345
497	OUT155	8180	465
498	OUT156	8164.5	345
499	OUT157	8149	465
500	OUT158	8133.5	345

No.	Name	X	Y
501	OUT159	8118	465
502	OUT160	8102.5	345
503	OUT161	8087	465
504	OUT162	8071.5	345
505	OUT163	8056	465
506	OUT164	8040.5	345
507	OUT165	8025	465
508	OUT166	8009.5	345
509	OUT167	7994	465
510	OUT168	7978.5	345
511	OUT169	7963	465
512	OUT170	7947.5	345
513	OUT171	7932	465
514	OUT172	7916.5	345
515	OUT173	7901	465
516	OUT174	7885.5	345
517	OUT175	7870	465
518	OUT176	7854.5	345
519	OUT177	7839	465
520	OUT178	7823.5	345
521	OUT179	7808	465
522	OUT180	7792.5	345
523	OUT181	7777	465
524	OUT182	7761.5	345
525	OUT183	7746	465
526	OUT184	7730.5	345
527	OUT185	7715	465
528	OUT186	7699.5	345
529	OUT187	7684	465
530	OUT188	7668.5	345
531	OUT189	7653	465
532	OUT190	7637.5	345
533	OUT191	7622	465
534	OUT192	7606.5	345
535	OUT193	7591	465
536	OUT194	7575.5	345
537	OUT195	7560	465
538	OUT196	7544.5	345
539	OUT197	7529	465
540	OUT198	7513.5	345
541	OUT199	7498	465
542	OUT200	7482.5	345
543	OUT201	7467	465
544	OUT202	7451.5	345
545	OUT203	7436	465
546	OUT204	7420.5	345
547	OUT205	7405	465
548	OUT206	7389.5	345
549	OUT207	7374	465
550	OUT208	7358.5	345

No.	Name	X	Y
551	OUT209	7343	465
552	OUT210	7327.5	345
553	OUT211	7312	465
554	OUT212	7296.5	345
555	OUT213	7281	465
556	OUT214	7265.5	345
557	OUT215	7250	465
558	OUT216	7234.5	345
559	OUT217	7219	465
560	OUT218	7203.5	345
561	OUT219	7188	465
562	OUT220	7172.5	345
563	OUT221	7157	465
564	OUT222	7141.5	345
565	OUT223	7126	465
566	OUT224	7110.5	345
567	OUT225	7095	465
568	OUT226	7079.5	345
569	OUT227	7064	465
570	OUT228	7048.5	345
571	OUT229	7033	465
572	OUT230	7017.5	345
573	OUT231	7002	465
574	OUT232	6986.5	345
575	OUT233	6971	465
576	OUT234	6955.5	345
577	OUT235	6940	465
578	OUT236	6924.5	345
579	OUT237	6909	465
580	OUT238	6893.5	345
581	OUT239	6878	465
582	OUT240	6862.5	345
583	OUT241	6847	465
584	OUT242	6831.5	345
585	OUT243	6816	465
586	OUT244	6800.5	345
587	OUT245	6785	465
588	OUT246	6769.5	345
589	OUT247	6754	465
590	OUT248	6738.5	345
591	OUT249	6723	465
592	OUT250	6707.5	345
593	OUT251	6692	465
594	OUT252	6676.5	345
595	OUT253	6661	465
596	OUT254	6645.5	345
597	OUT255	6630	465
598	OUT256	6614.5	345
599	OUT257	6599	465
600	OUT258	6583.5	345

No.	Name	X	Y
601	OUT259	6568	465
602	OUT260	6552.5	345
603	OUT261	6537	465
604	OUT262	6521.5	345
605	OUT263	6506	465
606	OUT264	6490.5	345
607	OUT265	6475	465
608	OUT266	6459.5	345
609	OUT267	6444	465
610	OUT268	6428.5	345
611	OUT269	6413	465
612	OUT270	6397.5	345
613	OUT271	6382	465
614	OUT272	6366.5	345
615	OUT273	6351	465
616	OUT274	6335.5	345
617	OUT275	6320	465
618	OUT276	6304.5	345
619	OUT277	6289	465
620	OUT278	6273.5	345
621	OUT279	6258	465
622	OUT280	6242.5	345
623	OUT281	6227	465
624	OUT282	6211.5	345
625	OUT283	6196	465
626	OUT284	6180.5	345
627	OUT285	6165	465
628	OUT286	6149.5	345
629	OUT287	6134	465
630	OUT288	6118.5	345
631	OUT289	6103	465
632	OUT290	6087.5	345
633	OUT291	6072	465
634	OUT292	6056.5	345
635	OUT293	6041	465
636	OUT294	6025.5	345
637	OUT295	6010	465
638	OUT296	5994.5	345
639	OUT297	5979	465
640	OUT298	5963.5	345
641	OUT299	5948	465
642	OUT300	5932.5	345
643	OUT301	5917	465
644	OUT302	5901.5	345
645	OUT303	5886	465
646	OUT304	5870.5	345
647	OUT305	5855	465
648	OUT306	5839.5	345
649	OUT307	5824	465
650	OUT308	5808.5	345

No.	Name	X	Y
651	OUT309	5793	465
652	OUT310	5777.5	345
653	OUT311	5762	465
654	OUT312	5746.5	345
655	OUT313	5731	465
656	OUT314	5715.5	345
657	OUT315	5700	465
658	OUT316	5684.5	345
659	OUT317	5669	465
660	OUT318	5653.5	345
661	OUT319	5638	465
662	OUT320	5622.5	345
663	OUT321	5607	465
664	OUT322	5591.5	345
665	OUT323	5576	465
666	OUT324	5560.5	345
667	OUT325	5545	465
668	OUT326	5529.5	345
669	OUT327	5514	465
670	OUT328	5498.5	345
671	OUT329	5483	465
672	OUT330	5467.5	345
673	OUT331	5452	465
674	OUT332	5436.5	345
675	OUT333	5421	465
676	OUT334	5405.5	345
677	OUT335	5390	465
678	OUT336	5374.5	345
679	OUT337	5359	465
680	OUT338	5343.5	345
681	OUT339	5328	465
682	OUT340	5312.5	345
683	OUT341	5297	465
684	OUT342	5281.5	345
685	OUT343	5266	465
686	OUT344	5250.5	345
687	OUT345	5235	465
688	OUT346	5219.5	345
689	OUT347	5204	465
690	OUT348	5188.5	345
691	OUT349	5173	465
692	OUT350	5157.5	345
693	OUT351	5142	465
694	OUT352	5126.5	345
695	OUT353	5111	465
696	OUT354	5095.5	345
697	OUT355	5080	465
698	OUT356	5064.5	345
699	OUT357	5049	465
700	OUT358	5033.5	345

No.	Name	X	Y
701	OUT359	5018	465
702	OUT360	5002.5	345
703	OUT361	4987	465
704	OUT362	4971.5	345
705	OUT363	4956	465
706	OUT364	4940.5	345
707	OUT365	4925	465
708	OUT366	4909.5	345
709	OUT367	4894	465
710	OUT368	4878.5	345
711	OUT369	4863	465
712	OUT370	4847.5	345
713	OUT371	4832	465
714	OUT372	4816.5	345
715	OUT373	4801	465
716	OUT374	4785.5	345
717	OUT375	4770	465
718	OUT376	4754.5	345
719	OUT377	4739	465
720	OUT378	4723.5	345
721	OUT379	4708	465
722	OUT380	4692.5	345
723	OUT381	4677	465
724	OUT382	4661.5	345
725	OUT383	4646	465
726	OUT384	4630.5	345
727	OUT385	4615	465
728	OUT386	4599.5	345
729	OUT387	4584	465
730	OUT388	4568.5	345
731	OUT389	4553	465
732	OUT390	4537.5	345
733	OUT391	4522	465
734	OUT392	4506.5	345
735	OUT393	4491	465
736	OUT394	4475.5	345
737	OUT395	4460	465
738	OUT396	4444.5	345
739	OUT397	4429	465
740	OUT398	4413.5	345
741	OUT399	4398	465
742	OUT400	4382.5	345
743	OUT401	4367	465
744	OUT402	4351.5	345
745	OUT403	4336	465
746	OUT404	4320.5	345
747	OUT405	4305	465
748	OUT406	4289.5	345
749	OUT407	4274	465
750	OUT408	4258.5	345

No.	Name	X	Y
751	OUT409	4243	465
752	OUT410	4227.5	345
753	OUT411	4212	465
754	OUT412	4196.5	345
755	OUT413	4181	465
756	OUT414	4165.5	345
757	OUT415	4150	465
758	OUT416	4134.5	345
759	OUT417	4119	465
760	OUT418	4103.5	345
761	OUT419	4088	465
762	OUT420	4072.5	345
763	OUT421	4057	465
764	OUT422	4041.5	345
765	OUT423	4026	465
766	OUT424	4010.5	345
767	OUT425	3995	465
768	OUT426	3979.5	345
769	OUT427	3964	465
770	OUT428	3948.5	345
771	OUT429	3933	465
772	OUT430	3917.5	345
773	OUT431	3902	465
774	OUT432	3886.5	345
775	OUT433	3871	465
776	OUT434	3855.5	345
777	OUT435	3840	465
778	OUT436	3824.5	345
779	OUT437	3809	465
780	OUT438	3793.5	345
781	OUT439	3778	465
782	OUT440	3762.5	345
783	OUT441	3747	465
784	OUT442	3731.5	345
785	OUT443	3716	465
786	OUT444	3700.5	345
787	OUT445	3685	465
788	OUT446	3669.5	345
789	OUT447	3654	465
790	OUT448	3638.5	345
791	OUT449	3623	465
792	OUT450	3607.5	345
793	OUT451	3592	465
794	OUT452	3576.5	345
795	OUT453	3561	465
796	OUT454	3545.5	345
797	OUT455	3530	465
798	OUT456	3514.5	345
799	OUT457	3499	465
800	OUT458	3483.5	345

No.	Name	X	Y
801	OUT459	3468	465
802	OUT460	3452.5	345
803	OUT461	3437	465
804	OUT462	3421.5	345
805	OUT463	3406	465
806	OUT464	3390.5	345
807	OUT465	3375	465
808	OUT466	3359.5	345
809	OUT467	3344	465
810	OUT468	3328.5	345
811	OUT469	3313	465
812	OUT470	3297.5	345
813	OUT471	3282	465
814	OUT472	3266.5	345
815	OUT473	3251	465
816	OUT474	3235.5	345
817	OUT475	3220	465
818	OUT476	3204.5	345
819	OUT477	3189	465
820	OUT478	3173.5	345
821	OUT479	3158	465
822	OUT480	3142.5	345
823	OUT481	3127	465
824	OUT482	3111.5	345
825	OUT483	3096	465
826	OUT484	3080.5	345
827	OUT485	3065	465
828	OUT486	3049.5	345
829	OUT487	3034	465
830	OUT488	3018.5	345
831	OUT489	3003	465
832	OUT490	2987.5	345
833	OUT491	2972	465
834	OUT492	2956.5	345
835	OUT493	2941	465
836	OUT494	2925.5	345
837	OUT495	2910	465
838	OUT496	2894.5	345
839	OUT497	2879	465
840	OUT498	2863.5	345
841	OUT499	2848	465
842	OUT500	2832.5	345
843	OUT501	2817	465
844	OUT502	2801.5	345
845	OUT503	2786	465
846	OUT504	2770.5	345
847	OUT505	2755	465
848	OUT506	2739.5	345
849	OUT507	2724	465
850	OUT508	2708.5	345

No.	Name	X	Y
851	OUT509	2693	465
852	OUT510	2677.5	345
853	OUT511	2662	465
854	OUT512	2646.5	345
855	OUT513	2631	465
856	OUT514	2615.5	345
857	OUT515	2600	465
858	OUT516	2584.5	345
859	OUT517	2569	465
860	OUT518	2553.5	345
861	OUT519	2538	465
862	OUT520	2522.5	345
863	OUT521	2507	465
864	OUT522	2491.5	345
865	OUT523	2476	465
866	OUT524	2460.5	345
867	OUT525	2445	465
868	OUT526	2429.5	345
869	OUT527	2414	465
870	OUT528	2398.5	345
871	OUT529	2383	465
872	OUT530	2367.5	345
873	OUT531	2352	465
874	OUT532	2336.5	345
875	OUT533	2321	465
876	OUT534	2305.5	345
877	OUT535	2290	465
878	OUT536	2274.5	345
879	OUT537	2259	465
880	OUT538	2243.5	345
881	OUT539	2228	465
882	OUT540	2212.5	345
883	OUT541	2197	465
884	OUT542	2181.5	345
885	OUT543	2166	465
886	OUT544	2150.5	345
887	OUT545	2135	465
888	OUT546	2119.5	345
889	OUT547	2104	465
890	OUT548	2088.5	345
891	OUT549	2073	465
892	OUT550	2057.5	345
893	OUT551	2042	465
894	OUT552	2026.5	345
895	OUT553	2011	465
896	OUT554	1995.5	345
897	OUT555	1980	465
898	OUT556	1964.5	345
899	OUT557	1949	465
900	OUT558	1933.5	345

No.	Name	X	Y
901	OUT559	1918	465
902	OUT560	1902.5	345
903	OUT561	1887	465
904	OUT562	1871.5	345
905	OUT563	1856	465
906	OUT564	1840.5	345
907	OUT565	1825	465
908	OUT566	1809.5	345
909	OUT567	1794	465
910	OUT568	1778.5	345
911	OUT569	1763	465
912	OUT570	1747.5	345
913	OUT571	1732	465
914	OUT572	1716.5	345
915	OUT573	1701	465
916	OUT574	1685.5	345
917	OUT575	1670	465
918	OUT576	1654.5	345
919	OUT577	1639	465
920	OUT578	1623.5	345
921	OUT579	1608	465
922	OUT580	1592.5	345
923	OUT581	1577	465
924	OUT582	1561.5	345
925	OUT583	1546	465
926	OUT584	1530.5	345
927	OUT585	1515	465
928	OUT586	1499.5	345
929	OUT587	1484	465
930	OUT588	1468.5	345
931	OUT589	1453	465
932	OUT590	1437.5	345
933	OUT591	1422	465
934	OUT592	1406.5	345
935	OUT593	1391	465
936	OUT594	1375.5	345
937	OUT595	1360	465
938	OUT596	1344.5	345
939	OUT597	1329	465
940	OUT598	1313.5	345
941	OUT599	1298	465
942	OUT600	1282.5	345
943	DUMMY	990	490
944	DUMMY	770	490
945	DUMMY	550	490
946	DUMMY	330	490
947	DUMMY	110	490
948	DUMMY	-110	490
949	DUMMY	-330	490
950	DUMMY	-550	490

No.	Name	X	Y
951	DUMMY	-770	490
952	DUMMY	-990	490
953	OUT601	-1282.5	465
954	OUT602	-1298	345
955	OUT603	-1313.5	465
956	OUT604	-1329	345
957	OUT605	-1344.5	465
958	OUT606	-1360	345
959	OUT607	-1375.5	465
960	OUT608	-1391	345
961	OUT609	-1406.5	465
962	OUT610	-1422	345
963	OUT611	-1437.5	465
964	OUT612	-1453	345
965	OUT613	-1468.5	465
966	OUT614	-1484	345
967	OUT615	-1499.5	465
968	OUT616	-1515	345
969	OUT617	-1530.5	465
970	OUT618	-1546	345
971	OUT619	-1561.5	465
972	OUT620	-1577	345
973	OUT621	-1592.5	465
974	OUT622	-1608	345
975	OUT623	-1623.5	465
976	OUT624	-1639	345
977	OUT625	-1654.5	465
978	OUT626	-1670	345
979	OUT627	-1685.5	465
980	OUT628	-1701	345
981	OUT629	-1716.5	465
982	OUT630	-1732	345
983	OUT631	-1747.5	465
984	OUT632	-1763	345
985	OUT633	-1778.5	465
986	OUT634	-1794	345
987	OUT635	-1809.5	465
988	OUT636	-1825	345
989	OUT637	-1840.5	465
990	OUT638	-1856	345
991	OUT639	-1871.5	465
992	OUT640	-1887	345
993	OUT641	-1902.5	465
994	OUT642	-1918	345
995	OUT643	-1933.5	465
996	OUT644	-1949	345
997	OUT645	-1964.5	465
998	OUT646	-1980	345
999	OUT647	-1995.5	465
1000	OUT648	-2011	345

No.	Name	X	Y
1001	OUT649	-2026.5	465
1002	OUT650	-2042	345
1003	OUT651	-2057.5	465
1004	OUT652	-2073	345
1005	OUT653	-2088.5	465
1006	OUT654	-2104	345
1007	OUT655	-2119.5	465
1008	OUT656	-2135	345
1009	OUT657	-2150.5	465
1010	OUT658	-2166	345
1011	OUT659	-2181.5	465
1012	OUT660	-2197	345
1013	OUT661	-2212.5	465
1014	OUT662	-2228	345
1015	OUT663	-2243.5	465
1016	OUT664	-2259	345
1017	OUT665	-2274.5	465
1018	OUT666	-2290	345
1019	OUT667	-2305.5	465
1020	OUT668	-2321	345
1021	OUT669	-2336.5	465
1022	OUT670	-2352	345
1023	OUT671	-2367.5	465
1024	OUT672	-2383	345
1025	OUT673	-2398.5	465
1026	OUT674	-2414	345
1027	OUT675	-2429.5	465
1028	OUT676	-2445	345
1029	OUT677	-2460.5	465
1030	OUT678	-2476	345
1031	OUT679	-2491.5	465
1032	OUT680	-2507	345
1033	OUT681	-2522.5	465
1034	OUT682	-2538	345
1035	OUT683	-2553.5	465
1036	OUT684	-2569	345
1037	OUT685	-2584.5	465
1038	OUT686	-2600	345
1039	OUT687	-2615.5	465
1040	OUT688	-2631	345
1041	OUT689	-2646.5	465
1042	OUT690	-2662	345
1043	OUT691	-2677.5	465
1044	OUT692	-2693	345
1045	OUT693	-2708.5	465
1046	OUT694	-2724	345
1047	OUT695	-2739.5	465
1048	OUT696	-2755	345
1049	OUT697	-2770.5	465
1050	OUT698	-2786	345

No.	Name	X	Y
1051	OUT699	-2801.5	465
1052	OUT700	-2817	345
1053	OUT701	-2832.5	465
1054	OUT702	-2848	345
1055	OUT703	-2863.5	465
1056	OUT704	-2879	345
1057	OUT705	-2894.5	465
1058	OUT706	-2910	345
1059	OUT707	-2925.5	465
1060	OUT708	-2941	345
1061	OUT709	-2956.5	465
1062	OUT710	-2972	345
1063	OUT711	-2987.5	465
1064	OUT712	-3003	345
1065	OUT713	-3018.5	465
1066	OUT714	-3034	345
1067	OUT715	-3049.5	465
1068	OUT716	-3065	345
1069	OUT717	-3080.5	465
1070	OUT718	-3096	345
1071	OUT719	-3111.5	465
1072	OUT720	-3127	345
1073	OUT721	-3142.5	465
1074	OUT722	-3158	345
1075	OUT723	-3173.5	465
1076	OUT724	-3189	345
1077	OUT725	-3204.5	465
1078	OUT726	-3220	345
1079	OUT727	-3235.5	465
1080	OUT728	-3251	345
1081	OUT729	-3266.5	465
1082	OUT730	-3282	345
1083	OUT731	-3297.5	465
1084	OUT732	-3313	345
1085	OUT733	-3328.5	465
1086	OUT734	-3344	345
1087	OUT735	-3359.5	465
1088	OUT736	-3375	345
1089	OUT737	-3390.5	465
1090	OUT738	-3406	345
1091	OUT739	-3421.5	465
1092	OUT740	-3437	345
1093	OUT741	-3452.5	465
1094	OUT742	-3468	345
1095	OUT743	-3483.5	465
1096	OUT744	-3499	345
1097	OUT745	-3514.5	465
1098	OUT746	-3530	345
1099	OUT747	-3545.5	465
1100	OUT748	-3561	345

No.	Name	X	Y
1101	OUT749	-3576.5	465
1102	OUT750	-3592	345
1103	OUT751	-3607.5	465
1104	OUT752	-3623	345
1105	OUT753	-3638.5	465
1106	OUT754	-3654	345
1107	OUT755	-3669.5	465
1108	OUT756	-3685	345
1109	OUT757	-3700.5	465
1110	OUT758	-3716	345
1111	OUT759	-3731.5	465
1112	OUT760	-3747	345
1113	OUT761	-3762.5	465
1114	OUT762	-3778	345
1115	OUT763	-3793.5	465
1116	OUT764	-3809	345
1117	OUT765	-3824.5	465
1118	OUT766	-3840	345
1119	OUT767	-3855.5	465
1120	OUT768	-3871	345
1121	OUT769	-3886.5	465
1122	OUT770	-3902	345
1123	OUT771	-3917.5	465
1124	OUT772	-3933	345
1125	OUT773	-3948.5	465
1126	OUT774	-3964	345
1127	OUT775	-3979.5	465
1128	OUT776	-3995	345
1129	OUT777	-4010.5	465
1130	OUT778	-4026	345
1131	OUT779	-4041.5	465
1132	OUT780	-4057	345
1133	OUT781	-4072.5	465
1134	OUT782	-4088	345
1135	OUT783	-4103.5	465
1136	OUT784	-4119	345
1137	OUT785	-4134.5	465
1138	OUT786	-4150	345
1139	OUT787	-4165.5	465
1140	OUT788	-4181	345
1141	OUT789	-4196.5	465
1142	OUT790	-4212	345
1143	OUT791	-4227.5	465
1144	OUT792	-4243	345
1145	OUT793	-4258.5	465
1146	OUT794	-4274	345
1147	OUT795	-4289.5	465
1148	OUT796	-4305	345
1149	OUT797	-4320.5	465
1150	OUT798	-4336	345

No.	Name	X	Y
1151	OUT799	-4351.5	465
1152	OUT800	-4367	345
1153	OUT801	-4382.5	465
1154	OUT802	-4398	345
1155	OUT803	-4413.5	465
1156	OUT804	-4429	345
1157	OUT805	-4444.5	465
1158	OUT806	-4460	345
1159	OUT807	-4475.5	465
1160	OUT808	-4491	345
1161	OUT809	-4506.5	465
1162	OUT810	-4522	345
1163	OUT811	-4537.5	465
1164	OUT812	-4553	345
1165	OUT813	-4568.5	465
1166	OUT814	-4584	345
1167	OUT815	-4599.5	465
1168	OUT816	-4615	345
1169	OUT817	-4630.5	465
1170	OUT818	-4646	345
1171	OUT819	-4661.5	465
1172	OUT820	-4677	345
1173	OUT821	-4692.5	465
1174	OUT822	-4708	345
1175	OUT823	-4723.5	465
1176	OUT824	-4739	345
1177	OUT825	-4754.5	465
1178	OUT826	-4770	345
1179	OUT827	-4785.5	465
1180	OUT828	-4801	345
1181	OUT829	-4816.5	465
1182	OUT830	-4832	345
1183	OUT831	-4847.5	465
1184	OUT832	-4863	345
1185	OUT833	-4878.5	465
1186	OUT834	-4894	345
1187	OUT835	-4909.5	465
1188	OUT836	-4925	345
1189	OUT837	-4940.5	465
1190	OUT838	-4956	345
1191	OUT839	-4971.5	465
1192	OUT840	-4987	345
1193	OUT841	-5002.5	465
1194	OUT842	-5018	345
1195	OUT843	-5033.5	465
1196	OUT844	-5049	345
1197	OUT845	-5064.5	465
1198	OUT846	-5080	345
1199	OUT847	-5095.5	465
1200	OUT848	-5111	345

No.	Name	X	Y
1201	OUT849	-5126.5	465
1202	OUT850	-5142	345
1203	OUT851	-5157.5	465
1204	OUT852	-5173	345
1205	OUT853	-5188.5	465
1206	OUT854	-5204	345
1207	OUT855	-5219.5	465
1208	OUT856	-5235	345
1209	OUT857	-5250.5	465
1210	OUT858	-5266	345
1211	OUT859	-5281.5	465
1212	OUT860	-5297	345
1213	OUT861	-5312.5	465
1214	OUT862	-5328	345
1215	OUT863	-5343.5	465
1216	OUT864	-5359	345
1217	OUT865	-5374.5	465
1218	OUT866	-5390	345
1219	OUT867	-5405.5	465
1220	OUT868	-5421	345
1221	OUT869	-5436.5	465
1222	OUT870	-5452	345
1223	OUT871	-5467.5	465
1224	OUT872	-5483	345
1225	OUT873	-5498.5	465
1226	OUT874	-5514	345
1227	OUT875	-5529.5	465
1228	OUT876	-5545	345
1229	OUT877	-5560.5	465
1230	OUT878	-5576	345
1231	OUT879	-5591.5	465
1232	OUT880	-5607	345
1233	OUT881	-5622.5	465
1234	OUT882	-5638	345
1235	OUT883	-5653.5	465
1236	OUT884	-5669	345
1237	OUT885	-5684.5	465
1238	OUT886	-5700	345
1239	OUT887	-5715.5	465
1240	OUT888	-5731	345
1241	OUT889	-5746.5	465
1242	OUT890	-5762	345
1243	OUT891	-5777.5	465
1244	OUT892	-5793	345
1245	OUT893	-5808.5	465
1246	OUT894	-5824	345
1247	OUT895	-5839.5	465
1248	OUT896	-5855	345
1249	OUT897	-5870.5	465
1250	OUT898	-5886	345

No.	Name	X	Y
1251	OUT899	-5901.5	465
1252	OUT900	-5917	345
1253	OUT901	-5932.5	465
1254	OUT902	-5948	345
1255	OUT903	-5963.5	465
1256	OUT904	-5979	345
1257	OUT905	-5994.5	465
1258	OUT906	-6010	345
1259	OUT907	-6025.5	465
1260	OUT908	-6041	345
1261	OUT909	-6056.5	465
1262	OUT910	-6072	345
1263	OUT911	-6087.5	465
1264	OUT912	-6103	345
1265	OUT913	-6118.5	465
1266	OUT914	-6134	345
1267	OUT915	-6149.5	465
1268	OUT916	-6165	345
1269	OUT917	-6180.5	465
1270	OUT918	-6196	345
1271	OUT919	-6211.5	465
1272	OUT920	-6227	345
1273	OUT921	-6242.5	465
1274	OUT922	-6258	345
1275	OUT923	-6273.5	465
1276	OUT924	-6289	345
1277	OUT925	-6304.5	465
1278	OUT926	-6320	345
1279	OUT927	-6335.5	465
1280	OUT928	-6351	345
1281	OUT929	-6366.5	465
1282	OUT930	-6382	345
1283	OUT931	-6397.5	465
1284	OUT932	-6413	345
1285	OUT933	-6428.5	465
1286	OUT934	-6444	345
1287	OUT935	-6459.5	465
1288	OUT936	-6475	345
1289	OUT937	-6490.5	465
1290	OUT938	-6506	345
1291	OUT939	-6521.5	465
1292	OUT940	-6537	345
1293	OUT941	-6552.5	465
1294	OUT942	-6568	345
1295	OUT943	-6583.5	465
1296	OUT944	-6599	345
1297	OUT945	-6614.5	465
1298	OUT946	-6630	345
1299	OUT947	-6645.5	465
1300	OUT948	-6661	345

No.	Name	X	Y
1301	OUT949	-6676.5	465
1302	OUT950	-6692	345
1303	OUT951	-6707.5	465
1304	OUT952	-6723	345
1305	OUT953	-6738.5	465
1306	OUT954	-6754	345
1307	OUT955	-6769.5	465
1308	OUT956	-6785	345
1309	OUT957	-6800.5	465
1310	OUT958	-6816	345
1311	OUT959	-6831.5	465
1312	OUT960	-6847	345
1313	OUT961	-6862.5	465
1314	OUT962	-6878	345
1315	OUT963	-6893.5	465
1316	OUT964	-6909	345
1317	OUT965	-6924.5	465
1318	OUT966	-6940	345
1319	OUT967	-6955.5	465
1320	OUT968	-6971	345
1321	OUT969	-6986.5	465
1322	OUT970	-7002	345
1323	OUT971	-7017.5	465
1324	OUT972	-7033	345
1325	OUT973	-7048.5	465
1326	OUT974	-7064	345
1327	OUT975	-7079.5	465
1328	OUT976	-7095	345
1329	OUT977	-7110.5	465
1330	OUT978	-7126	345
1331	OUT979	-7141.5	465
1332	OUT980	-7157	345
1333	OUT981	-7172.5	465
1334	OUT982	-7188	345
1335	OUT983	-7203.5	465
1336	OUT984	-7219	345
1337	OUT985	-7234.5	465
1338	OUT986	-7250	345
1339	OUT987	-7265.5	465
1340	OUT988	-7281	345
1341	OUT989	-7296.5	465
1342	OUT990	-7312	345
1343	OUT991	-7327.5	465
1344	OUT992	-7343	345
1345	OUT993	-7358.5	465
1346	OUT994	-7374	345
1347	OUT995	-7389.5	465
1348	OUT996	-7405	345
1349	OUT997	-7420.5	465
1350	OUT998	-7436	345

No.	Name	X	Y
1351	OUT999	-7451.5	465
1352	OUT1000	-7467	345
1353	OUT1001	-7482.5	465
1354	OUT1002	-7498	345
1355	OUT1003	-7513.5	465
1356	OUT1004	-7529	345
1357	OUT1005	-7544.5	465
1358	OUT1006	-7560	345
1359	OUT1007	-7575.5	465
1360	OUT1008	-7591	345
1361	OUT1009	-7606.5	465
1362	OUT1010	-7622	345
1363	OUT1011	-7637.5	465
1364	OUT1012	-7653	345
1365	OUT1013	-7668.5	465
1366	OUT1014	-7684	345
1367	OUT1015	-7699.5	465
1368	OUT1016	-7715	345
1369	OUT1017	-7730.5	465
1370	OUT1018	-7746	345
1371	OUT1019	-7761.5	465
1372	OUT1020	-7777	345
1373	OUT1021	-7792.5	465
1374	OUT1022	-7808	345
1375	OUT1023	-7823.5	465
1376	OUT1024	-7839	345
1377	OUT1025	-7854.5	465
1378	OUT1026	-7870	345
1379	OUT1027	-7885.5	465
1380	OUT1028	-7901	345
1381	OUT1029	-7916.5	465
1382	OUT1030	-7932	345
1383	OUT1031	-7947.5	465
1384	OUT1032	-7963	345
1385	OUT1033	-7978.5	465
1386	OUT1034	-7994	345
1387	OUT1035	-8009.5	465
1388	OUT1036	-8025	345
1389	OUT1037	-8040.5	465
1390	OUT1038	-8056	345
1391	OUT1039	-8071.5	465
1392	OUT1040	-8087	345
1393	OUT1041	-8102.5	465
1394	OUT1042	-8118	345
1395	OUT1043	-8133.5	465
1396	OUT1044	-8149	345
1397	OUT1045	-8164.5	465
1398	OUT1046	-8180	345
1399	OUT1047	-8195.5	465
1400	OUT1048	-8211	345

No.	Name	X	Y
1401	OUT1049	-8226.5	465
1402	OUT1050	-8242	345
1403	OUT1051	-8257.5	465
1404	OUT1052	-8273	345
1405	OUT1053	-8288.5	465
1406	OUT1054	-8304	345
1407	OUT1055	-8319.5	465
1408	OUT1056	-8335	345
1409	OUT1057	-8350.5	465
1410	OUT1058	-8366	345
1411	OUT1059	-8381.5	465
1412	OUT1060	-8397	345
1413	OUT1061	-8412.5	465
1414	OUT1062	-8428	345
1415	OUT1063	-8443.5	465
1416	OUT1064	-8459	345
1417	OUT1065	-8474.5	465
1418	OUT1066	-8490	345
1419	OUT1067	-8505.5	465
1420	OUT1068	-8521	345
1421	OUT1069	-8536.5	465
1422	OUT1070	-8552	345
1423	OUT1071	-8567.5	465
1424	OUT1072	-8583	345
1425	OUT1073	-8598.5	465
1426	OUT1074	-8614	345
1427	OUT1075	-8629.5	465
1428	OUT1076	-8645	345
1429	OUT1077	-8660.5	465
1430	OUT1078	-8676	345
1431	OUT1079	-8691.5	465
1432	OUT1080	-8707	345
1433	OUT1081	-8722.5	465
1434	OUT1082	-8738	345
1435	OUT1083	-8753.5	465
1436	OUT1084	-8769	345
1437	OUT1085	-8784.5	465
1438	OUT1086	-8800	345
1439	OUT1087	-8815.5	465
1440	OUT1088	-8831	345
1441	OUT1089	-8846.5	465
1442	OUT1090	-8862	345
1443	OUT1091	-8877.5	465
1444	OUT1092	-8893	345
1445	OUT1093	-8908.5	465
1446	OUT1094	-8924	345
1447	OUT1095	-8939.5	465
1448	OUT1096	-8955	345
1449	OUT1097	-8970.5	465
1450	OUT1098	-8986	345

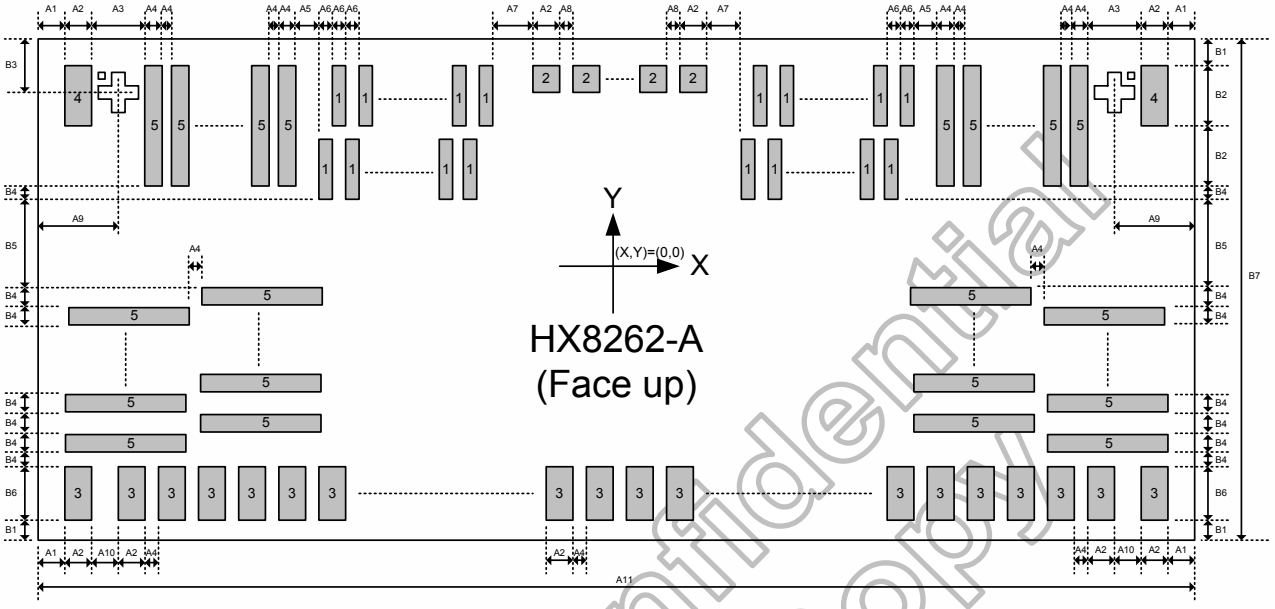
No.	Name	X	Y
1451	OUT1099	-9001.5	465
1452	OUT1100	-9017	345
1453	OUT1101	-9032.5	465
1454	OUT1102	-9048	345
1455	OUT1103	-9063.5	465
1456	OUT1104	-9079	345
1457	OUT1105	-9094.5	465
1458	OUT1106	-9110	345
1459	OUT1107	-9125.5	465
1460	OUT1108	-9141	345
1461	OUT1109	-9156.5	465
1462	OUT1110	-9172	345
1463	OUT1111	-9187.5	465
1464	OUT1112	-9203	345
1465	OUT1113	-9218.5	465
1466	OUT1114	-9234	345
1467	OUT1115	-9249.5	465
1468	OUT1116	-9265	345
1469	OUT1117	-9280.5	465
1470	OUT1118	-9296	345
1471	OUT1119	-9311.5	465
1472	OUT1120	-9327	345
1473	OUT1121	-9342.5	465
1474	OUT1122	-9358	345
1475	OUT1123	-9373.5	465
1476	OUT1124	-9389	345
1477	OUT1125	-9404.5	465
1478	OUT1126	-9420	345
1479	OUT1127	-9435.5	465
1480	OUT1128	-9451	345
1481	OUT1129	-9466.5	465
1482	OUT1130	-9482	345
1483	OUT1131	-9497.5	465
1484	OUT1132	-9513	345
1485	OUT1133	-9528.5	465
1486	OUT1134	-9544	345
1487	OUT1135	-9559.5	465
1488	OUT1136	-9575	345
1489	OUT1137	-9590.5	465
1490	OUT1138	-9606	345
1491	OUT1139	-9621.5	465
1492	OUT1140	-9637	345
1493	OUT1141	-9652.5	465
1494	OUT1142	-9668	345
1495	OUT1143	-9683.5	465
1496	OUT1144	-9699	345
1497	OUT1145	-9714.5	465
1498	OUT1146	-9730	345
1499	OUT1147	-9745.5	465
1500	OUT1148	-9761	345

No.	Name	X	Y
1501	OUT1149	-9776.5	465
1502	OUT1150	-9792	345
1503	OUT1151	-9807.5	465
1504	OUT1152	-9823	345
1505	OUT1153	-9838.5	465
1506	OUT1154	-9854	345
1507	OUT1155	-9869.5	465
1508	OUT1156	-9885	345
1509	OUT1157	-9900.5	465
1510	OUT1158	-9916	345
1511	OUT1159	-9931.5	465
1512	OUT1160	-9947	345
1513	OUT1161	-9962.5	465
1514	OUT1162	-9978	345
1515	OUT1163	-9993.5	465
1516	OUT1164	-10009	345
1517	OUT1165	-10024.5	465
1518	OUT1166	-10040	345
1519	OUT1167	-10055.5	465
1520	OUT1168	-10071	345
1521	OUT1169	-10086.5	465
1522	OUT1170	-10102	345
1523	OUT1171	-10117.5	465
1524	OUT1172	-10133	345
1525	OUT1173	-10148.5	465
1526	OUT1174	-10164	345
1527	OUT1175	-10179.5	465
1528	OUT1176	-10195	345
1529	OUT1177	-10210.5	465
1530	OUT1178	-10226	345
1531	OUT1179	-10241.5	465
1532	OUT1180	-10257	345
1533	OUT1181	-10272.5	465
1534	OUT1182	-10288	345
1535	OUT1183	-10303.5	465
1536	OUT1184	-10319	345
1537	OUT1185	-10334.5	465
1538	OUT1186	-10350	345
1539	OUT1187	-10365.5	465
1540	OUT1188	-10381	345
1541	OUT1189	-10396.5	465
1542	OUT1190	-10412	345
1543	OUT1191	-10427.5	465
1544	OUT1192	-10443	345
1545	OUT1193	-10458.5	465
1546	OUT1194	-10474	345
1547	OUT1195	-10489.5	465
1548	OUT1196	-10505	345
1549	OUT1197	-10520.5	465
1550	OUT1198	-10536	345

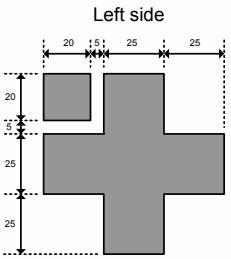
No.	Name	X	Y
1551	OUT1199	-10551.5	465
1552	OUT1200	-10567	345
1553	PASS3	-10630	415
1554	PASS4	-10670	415
1555	OEV_LRR	-10710	415
1556	UDP_POLR	-10750	415
1557	CKV_RESETR	-10790	415
1558	STVD	-10830	415
1559	STVU	-10870	415
1560	DUMMY	-11050	465
1561	D25R	-10975	-15
1562	D24R	-10755	-35
1563	D23R	-10975	-55
1564	D22R	-10755	-75
1565	D21R	-10975	-95
1566	D20R	-10755	-115
1567	D15R	-10975	-135
1568	D14R	-10755	-155
1569	D13R	-10975	-175
1570	D12R	-10755	-195
1571	D11R	-10975	-215
1572	D10R	-10755	-235
1573	D05R	-10975	-255
1574	D04R	-10755	-275
1575	D03R	-10975	-295
1576	D02R	-10755	-315
1577	D01R	-10975	-335
1578	D00R	-10755	-355
1579	DCLKR	-10975	-375
1580	DER	-10755	-395
	Alignment mark R	-10952.5	452.5
	Alignment mark L	10952.5	452.5

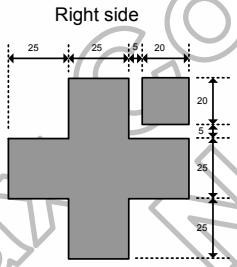
14. Bump Mask information

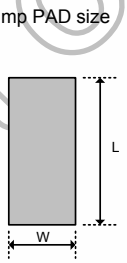
- Chip size : 22280 um x 1160 um (include scribe line)
- Bump height : 15 um ± 3 um
- Bump hardness : 60 Hv ± 15 Hv

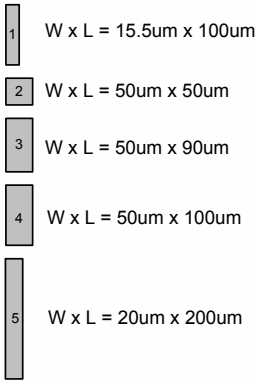


Alignment mark
(unit : um)









Symbol	Dimension (um)
A1	65
A2	50
A3	145
A4	20
A5	45.25
A6	15.5
A7	259.75
A8	170
A9	187.5
A10	115
A11	22280

Symbol	Dimension (um)
B1	65
B2	100
B3	127.5
B4	20
B5	300
B6	90
B7	1160

15. Ordering Information

PART NO.	PACKAGE TYPE
HX8262-A000PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400μm)

16. Revision History

Ver. No	Date	Section	Description