APPLICATION NOTE

SKY77344-21 Power Amplifier Module — Evaluation Information

Applicability: SKY77344 Version -21

Introduction

This Application Note describes the functionality, board layout and applications instructions of the SKY77344-21 Power Amplifier Module.

The SKY77344-21 Power Amplifier Module (PAM) is designed for quad-band cellular handsets comprising GSM850/900, DCS1800/ PCS1900, and supports Class 12 General Packet Radio Service (GPRS) multi-slot operation, and Enhanced Data GSM Environment (EDGE) (8PSK) linear modulation. A single analog control voltage is used at the VRAMP port for both GMSK and EDGE modes. The active logic level at the MODE terminal determines the function of the VRAMP signal.

The EDGE mode is supported with a linear open loop configuration where amplifier gain is held constant with VRAMP and output power is determined by input power. GMSK mode is supported by operating the SKY77344-21 as a variable gain amplifier where VRAMP controls gain and resultant output power.

The SKY77344-21 PAM consists of an Indium Gallium Phosphide (InGaP) PA block, a BiCMOS multi-function controller (MFC) block, and impedance-matching circuitry. The new BiCMOS collector voltage amplitude controller (COVAC) provides envelope amplitude control and bias optimization for each mode of operation, thus reducing sensitivity to input drive, temperature, power supply, and process variations. Embedded within a single Gallium Arsenide (GaAs) die using InGaP technology, one Heterojunction Bipolar Transistor (HBT) PA lineup supports the GSM850/900 bands and another supports the DCS1800 and PCS1900 bands.

The module also contains band select switching circuitry to select GSM (logic 0) and DCS/PCS (logic 1) as determined from the Band Select (BS) signal. As determined by the MODE control, VRAMP controls the level of output power for GMSK modulation or optimizes the performance for EDGE modulation. The Enable input signal allows initial turn-on of the PAC circuitry to minimize battery drain.

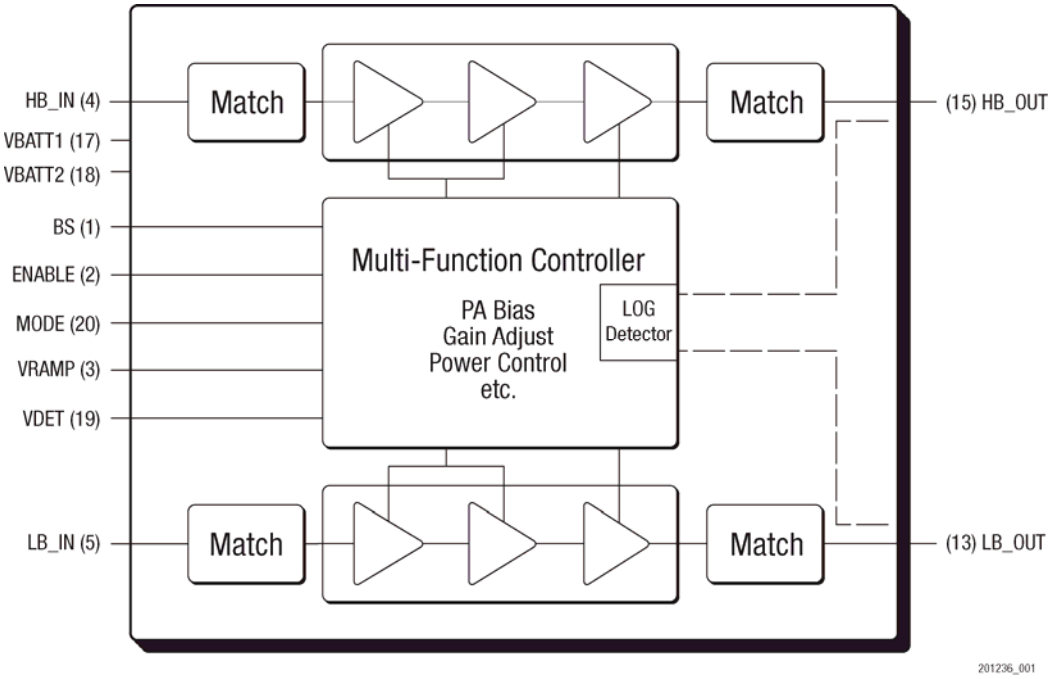


Figure 1. SKY77344-21 Functional Block Diagram

OPERATIONAL CONSIDERATIONS

The SKY77344-21 is intended for multi-modulation GSM/GPRS/EDGE handset applications. The next two sections will describe how the module should be configured for use with GSM/GPRS and the EDGE waveforms.

GSM/GPRS OPERATION

For GMSK operation, set EN input high and MODE low (< 0.5 V). Select the desired TX band by setting the BS low (CEL/EGSM) or high (DCS/PCS). VRAMP is a pulsed ramp input that controls the module output power in a manner similar to a traditional "VAPC" or "VPC" input control signal. The pulsed ramp profile is optimized with the baseband DAC control software to be compliant with PVT and ORFS due to switching system specifications.

VRAMP Filter

It is advisable to use a first order RC network on VRAMP line to filter noise introduced by the baseband DAC. The filter should be designed so as to not slow down the power mask timing requirements.

Recommended RC network values are: R = 110 Ω, C = 10 nF, (F_{POLE} = 145 kHz).

Depending upon the baseband DAC operating characteristics, the RC network can be redesigned or eliminated. The values selected for the RC network are critical for correct saturation detection / correction operation. A limit of R < 1 kΩ is recommended.

Power Control Scheme

An integrated power control scheme is used to control the PA output power for GMSK operation. The COVAC configuration combined with a coupler / log detector provides a closed loop feedback mechanism. The COVAC scheme is based on limiting power at the collector by limiting collector voltage while the feedback path monitors output power. During saturated GMSK operation, the RF input drive is held constant while saturation characteristics of the amplifier are used to control output power. Reduction of the collector voltage of the amplifier driver stages forces saturation, effectively limiting the large signal gain and reducing the drive level to the final stage amplifier. Coincident reduction of the quiescent current in the amplifier provides reduction of the small signal gain along with reduced current drain. Significant reduction of the final stage bias point below the base-emitter voltage is required to meet aggressive low power performance as well.

Table 2 is a simplified schematic of PA control scheme which senses the detected output power, compares it to the external VRAMP signal and sets the required bias voltage at the PA collector.

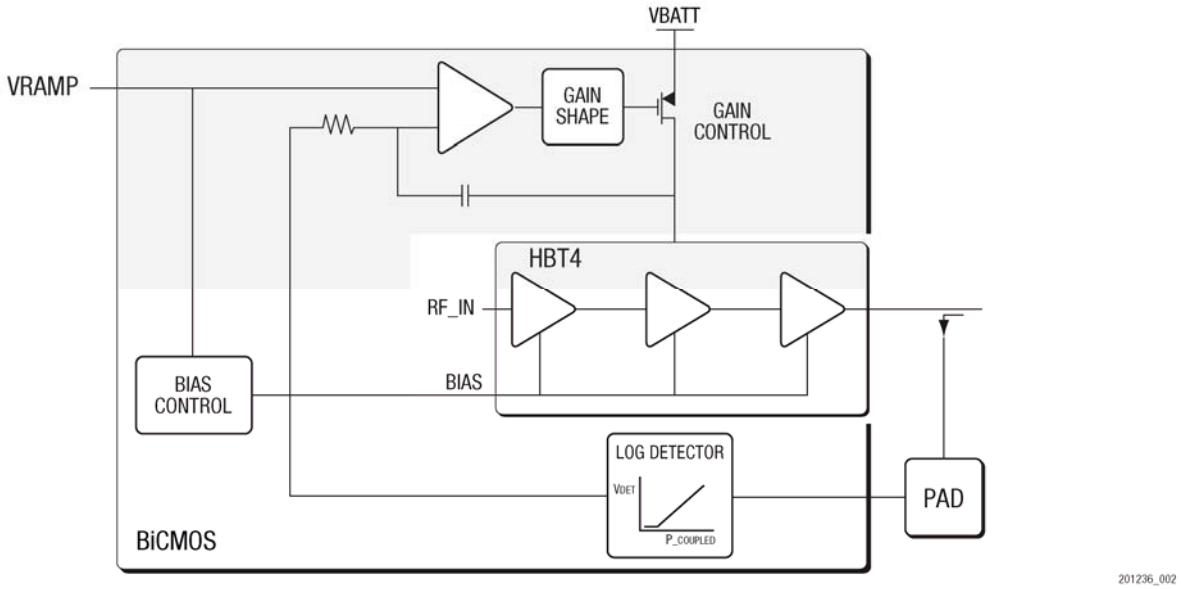


Figure 2. SKY77344-21 Power Control Scheme – GMSK Mode

Saturation Detection/Correction Operation Description and External V_{RAMP} Filter Guideline

When the SKY77344-21 PAM saturates under conditions of low battery and/or VSWR, a decrease in the internal power control loop gain-bandwidth occurs, producing high level switching transients on the falling edge of the burst. To prevent this condition, the SKY77344-21 includes an autonomous saturation detection / correction function. When saturation is detected, output power is reduced by approximately 0.5 dB which is sufficient to increase the loop gain-bandwidth to a level that restores switching transients to specification compliance (with additional production margin).

Under some environmental conditions, the PA may enter soft saturation, which is the transition region between no saturation and hard saturation. To ensure compliant switching transients in this region, the PA is "tested" for soft saturation by pushing the PA into hard saturation. This is achieved by reducing the output power approximately 0.5 dB about 100 µs after the start of every burst. This "correct every burst" feature occurs for all V_{RAMP} levels greater than 1.0 V. Saturation is detected during the first 100 µs or "high" part of the carrier power envelope followed by the required power reduction. Whether the PA is saturated or non-saturated, a ~0.5 dB power correction will be observed for all V_{RAMP} levels greater than 1.0 V. Nominally, this power correction will occur ~100 µs after the start of the burst.

However, as V_{RAMP} exceeds the voltage required for nominal rated output power (~1.85 V), the correction duty cycle will increase from 100 µs / 577 µs (17%) to 100%. As the applied V_{RAMP} is increased beyond that required for nominal rated power, the internal V_{RAMP}, which references the internal PA control loop, must be further decreased to pull the control loop out of saturation. Since the internal pullback time constant is fixed, this action requires additional time and results in increasing the correction duty cycle. For V_{RAMP} greater than ~2.2 V, which is beyond the normal operating region of the device, the duty cycle is ~100% and the saturation detection/correction circuitry is no longer active.

Under conditions of low battery and/or VSWR PA load, where the saturated PA output power (P_{SAT}) has decreased, the correction duty cycle will also increase beyond the nominal 17%. The internal V_{RAMP} must be decreased below the lower V_{RAMP} @P_{SAT} value to pull the control loop out of saturation. Since the internal pullback time constant is fixed, this action requires additional time or longer correction duty cycle. To ensure part-to-part constancy, the correction factor (~0.5 dB for Low Band, ~0.4 dB for High Band) is screened at production test.

Figure 3 illustrates a block diagram of the saturation detection/correction technique used in the SKY77344-21. Depicted are the power amplifier, detector, collector voltage power control loop, and the saturation detection/correction functions, V_{RAMP} comparator, timer, correction offset ramp generator, I_{OFFSET} current source, and saturation detector.

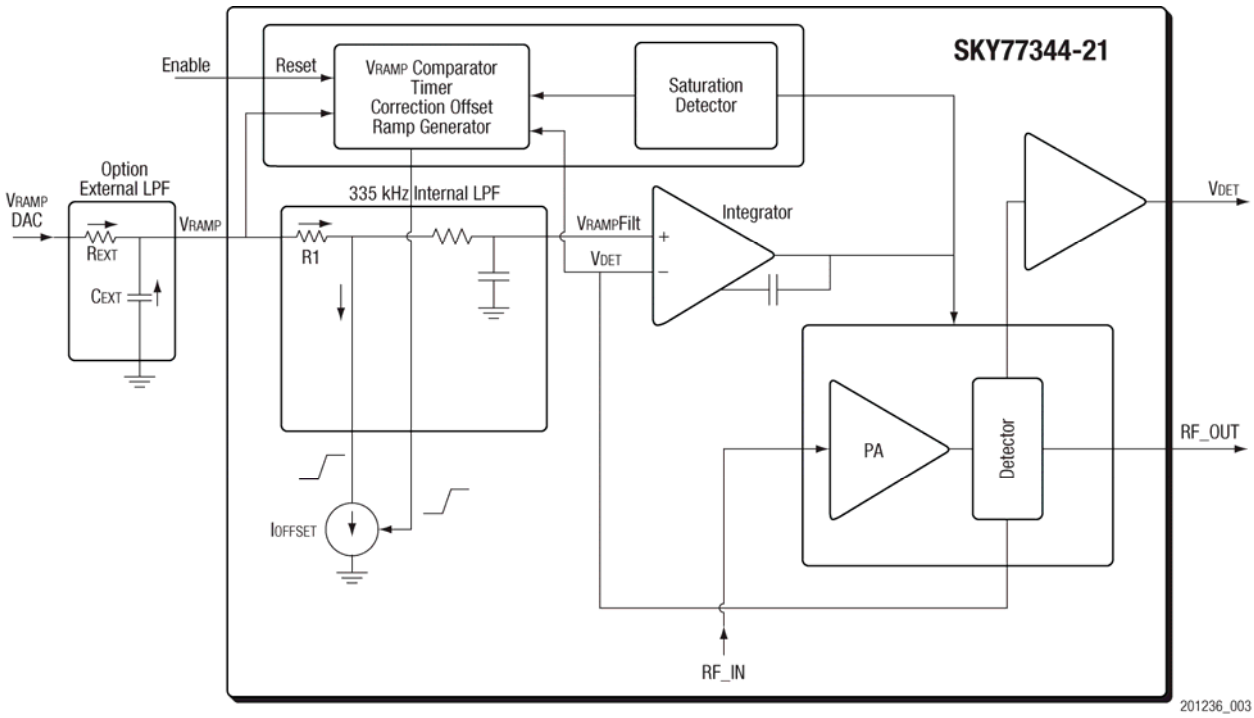


Figure 3. SKY77344-21 Block Diagram of Saturation Detection / Correction Technique

Also shown in Figure 3 are two V_{RAMP} RC LP filters. The internal LP filter has a ~335 kHz 3 dB cutoff frequency which is adequate for suppressing DAC quarter-bit step transition transients. If courser DAC step sizes are used, an external V_{RAMP} filter may be added for additional transient suppression. However, the values selected for R_{EXT} and C_{EXT} are critical for correct saturation detection / correction operation. Selection guidelines for the R_{EXT} and C_{EXT} values are addressed in the last section.

When V_{RAMP} exceeds ~1.0 V, an internal 100 µs timer is initiated. After the timer expires, saturation is checked followed by the power correction. The internal reference voltage applied to the power control loop integrator input ($V_{RAMPFILT}$) is reduced by subtracting a linearly increasing voltage offset from the applied V_{RAMP} control level. This voltage offset is created by sinking a linearly increasing offset current (I_{OFFSET} < 100 µA) across the internal and external V_{RAMP} LP filter resistors. The $V_{RAMPFILT}$ power control reference voltage decreases with time until the ~0.5 dB power reduction target is met, at which point I_{OFFSET} is held constant until V_{RAMP} decreases below 0.9 V or a PA enable high-to-low transition occurs. For multi-slot GMSK-to-GMSK operation, transitioning V_{RAMP} below ~0.9 V between slots is required to reset the saturation detection/correct function for correct operation in the following slot.

$V_{OFFSET} = (R_{EXT} + R1) * I_{OFFSET} * \text{Delta T}$

Where:

R_{EXT} = external V_{RAMP} filter resistor

R1 = internal V_{RAMP} filter resistor segment (approximately 3 kΩ).

I_{OFFSET} = linearly increasing current ramp (1.1 A per second).

Delta T = V_{OFFSET} ramp duration: Time between saturation detection and P_{OUT} reduction completion.

The V_{OFFSET} ramp slope was optimized with the internal closed loop time constants to achieve correct saturation detection / correction operation. If R_{EXT} is non-zero, the V_{OFFSET} ramp slope [(R_{EXT} + R1)* I_{OFFSET}] is faster than the loop time constants causing P_{OUT} to reduce beyond the ~0.5 dB design point.

To maintain the P_{OUT} reduction within a ~0.4 dB for HB to ~0.5 dB for LB window, limiting R_{EXT} to < 1 kΩ is recommended. For a desired filter pole, the external shunt capacitor (C_{EXT}) should be increased using the following relation.

$C_{EXT} = 1/(2\pi * F_{POLE} * R_{EXT})$.

EDGE (8PSK) OPERATION

The module operates in a linear open loop configuration with P_{OUT} controlled by the input power (P_{IN}). Output power is defined as:

$P_{OUT} = P_{IN} + \text{Gain}$

To operate the SKY77344-21 in EDGE (8PSK) mode, set both EN input and MODE high. Select the desired TX band by setting BS low for CEL/EGSM or high for DCS/PCS. The analog input, VRAMP, adjusts the quiescent current and is set to obtain the desired ACPR and EVM margin for the appropriate band. VRAMP is intended to remain fixed throughout the transmit slot.

Using bias control, VRAMP, allows gain control and optimization of the current at lower output power; however, the bias control greatly affects the linearity of the module. Achieving the desired power while simultaneously meeting the linearity requirements necessitates careful setting of VRAMP.

During the linear EDGE mode, the amplifier quiescent current must be maintained constant, independent of temperature, to maintain constant intercept performance. The disadvantage of constant bias is that the small signal gain decreases with increasing temperature. Voltage headroom on each amplifier stage must also be maintained to prevent compression and degradation of the linearity. At reduced output power levels, the quiescent bias can be reduced to minimize current drain. Analog control of the bias points is provided through the VRAMP control signal. Output power is detected and translated to DC voltage linearly relative to the output power in dB.

Closed loop power control for EDGE mode is made possible with the RF power detector voltage at the VDET terminal. When the PA is disabled (EN < 0.5 V), the VDET terminal is tri-state (high impedance), allowing other 3G PAs to share a common VDET connection. A power control circuit external to the MFC can use this signal to achieve closed loop EDGE operation. Saturation Detection / Correction is disabled in EDGE operation.

LOGIC and INPUT SETTINGS

Table 1. Control Logic

Operational State	EN	BS	MODE	VRAMP
Standby/PA off	0	X	X	X
Low band GMSK[2]	1	0	0	Active [2]
Low band EDGE[3]	1	0	1	Active [3]
High band GMSK[2]	1	1	0	Active [2]
High band EDGE[3]	1	1	1	Active [3]

[1] X = don't care

[2] VRAMP controls output power

[3] VRAMP sets PA bias

Table 2. Maximum Bias Voltages to Achieve Rated POUT – EDGE and GMSK

Band and Modulation	Input	
	VRAMP	Mode
CEL/EGSM_TX EDGE	2.0 V	High
DCS/PCS_TX EDGE	2.0 V	High
CEL/EGSM_TX GMSK	2.0 V	Low
DCS/PCS_TX GMSK	2.0 V	Low

SKY77344-21 Test Fixture

The SKY77344-21 test fixture assembly is shown in Figure 3 and the schematic of the test fixture is shown in Figure 4. Artwork of the four layers of the test fixture assembly is shown in Figure 5 through Figure 8.

Not all components shown are installed on the test fixture. R1 is installed to connect VRAMP from P1. Alternately, R2 and J1 may be installed to allow application of VRAMP via the SMA coaxial connector. C3, C6, and C7 are not normally installed but provide mounting locations for additional capacitance to VBATT to insure good low frequency bypassing, depending on the quality of the bench power supply used. A VBATT_SENSE line (Figure 3, connector P1.5) provides feedback to a sensing power supply to help maintain proper voltage under transient conditions.

A single analog control voltage is used at the VRAMP port for both the GMSK and EDGE modes. The active signal is ultimately determined by the MODE control logic level applied. Figure 11 through Figure 15 provide recommended control timing and VRAMP profiles for proper operation in GMSK mode, EDGE mode, and multimode slot-to-slot operation. Table 1 shows the proper control logic combinations for GMSK and EDGE modes of operation for low band and high band.

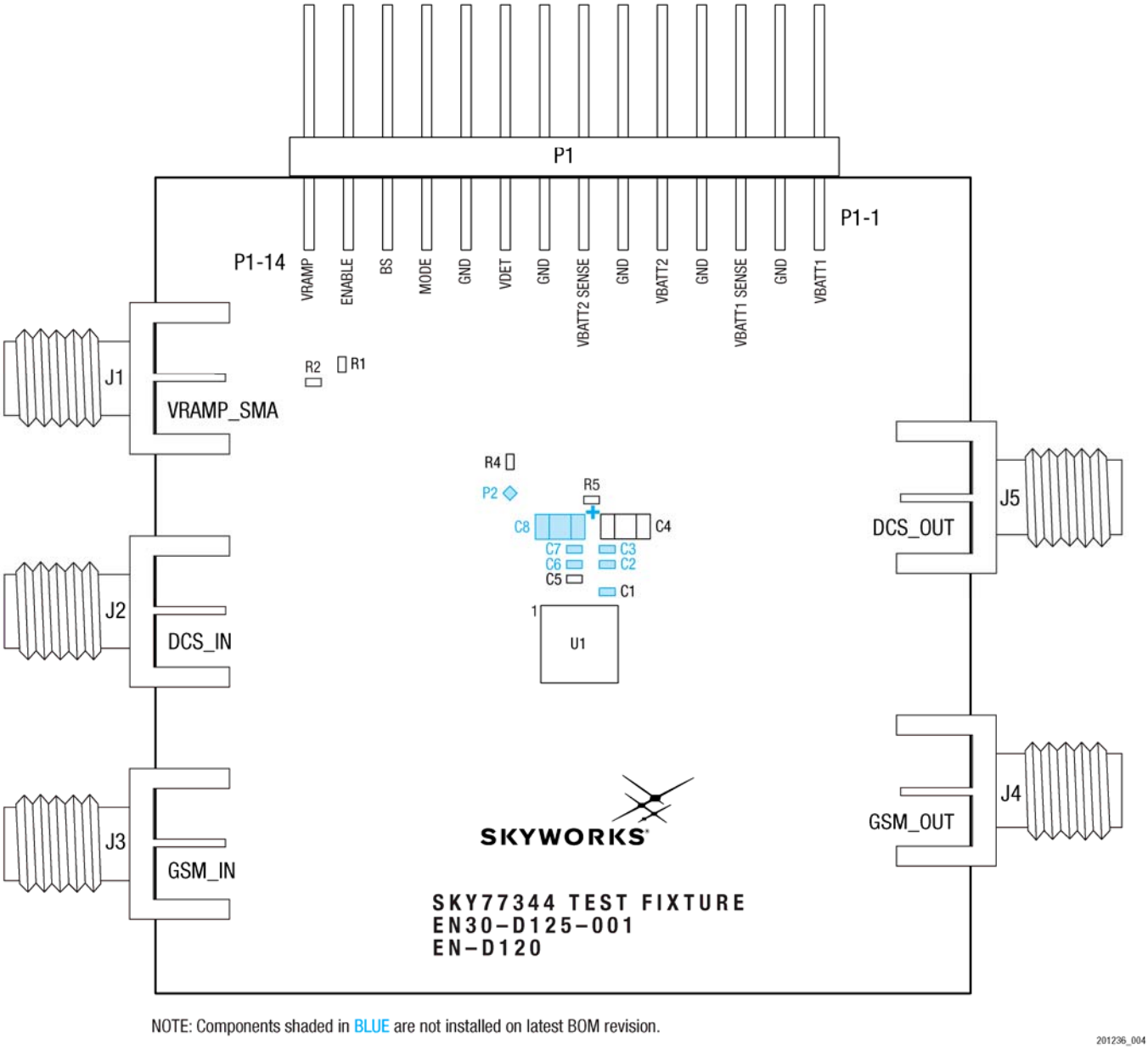
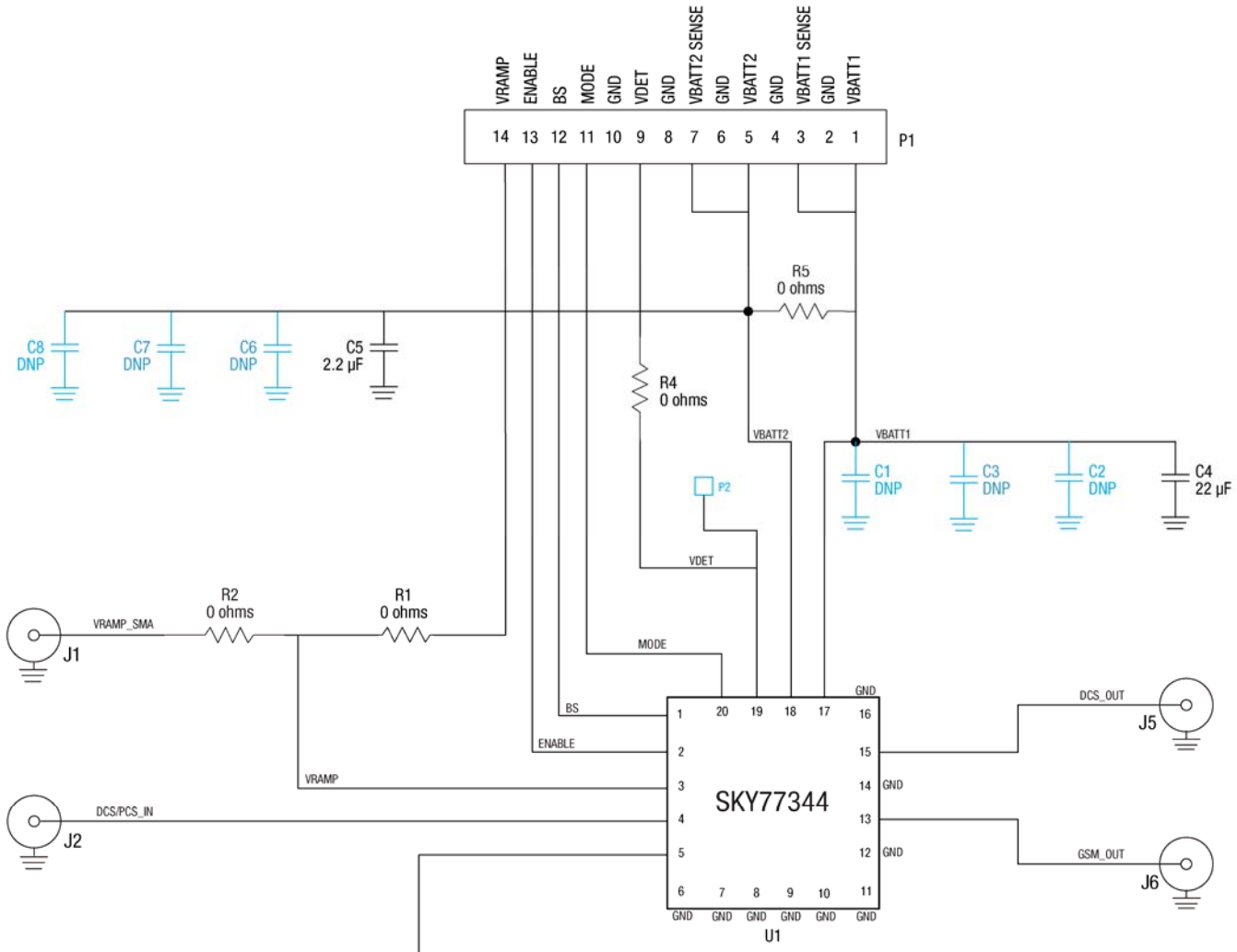


Figure 4. SKY77344-21 Power Amplifier Text Fixture



COMPONENTS TABLE		
REF	VALUE	DESCRIPTION
C1	do not place	
C2	do not place	
C3	do not place	
C4	22 µF	TANTALUM 0603
C5	2.2 µF	±10%, 0402
C6	do not place	
C7	do not place	
C8	do not place	
P2	do not place	
R1, R2	0 Ω	0402, FIXED, SMT, 50 V
R4, R5	0 Ω	0402, FIXED, SMT, 50 V

NOTES: UNLESS OTHERWISE SPECIFIED
1. Components shaded in BLUE are not installed on latest BOM revision.
2. For component values see Bill of Materials referenced in Assembly Drawing EN30-D120.
3. Test fixture schematic differs from Figure 9 (Application Circuit Diagram) due to specific testing requirements.

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Figure 5. Power Amplifier Test Fixture Schematic Diagram – SKY77344-21

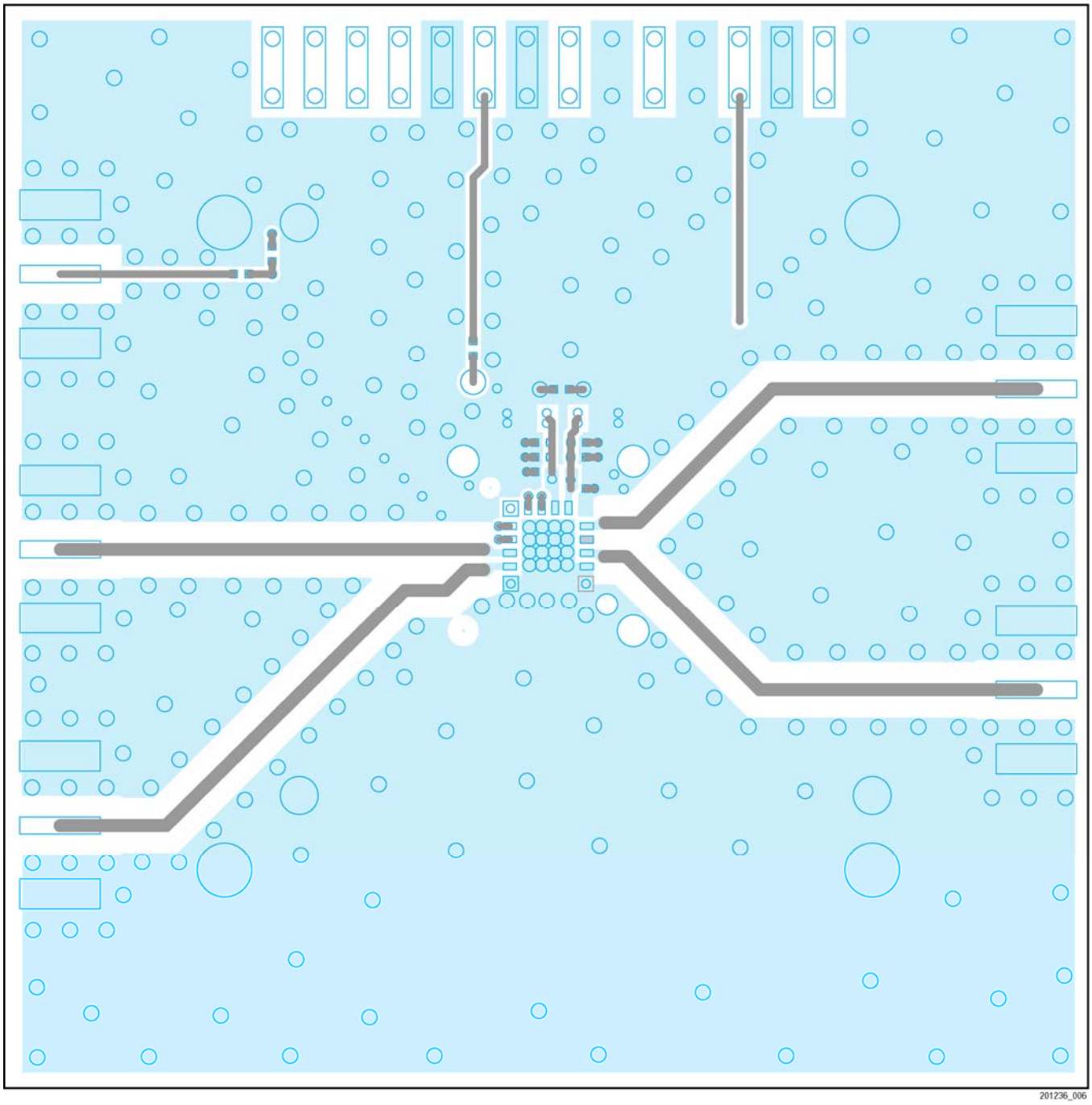

Figure 6. SKY77344-21 Power Amplifier Test Fixture PCB Layer 1

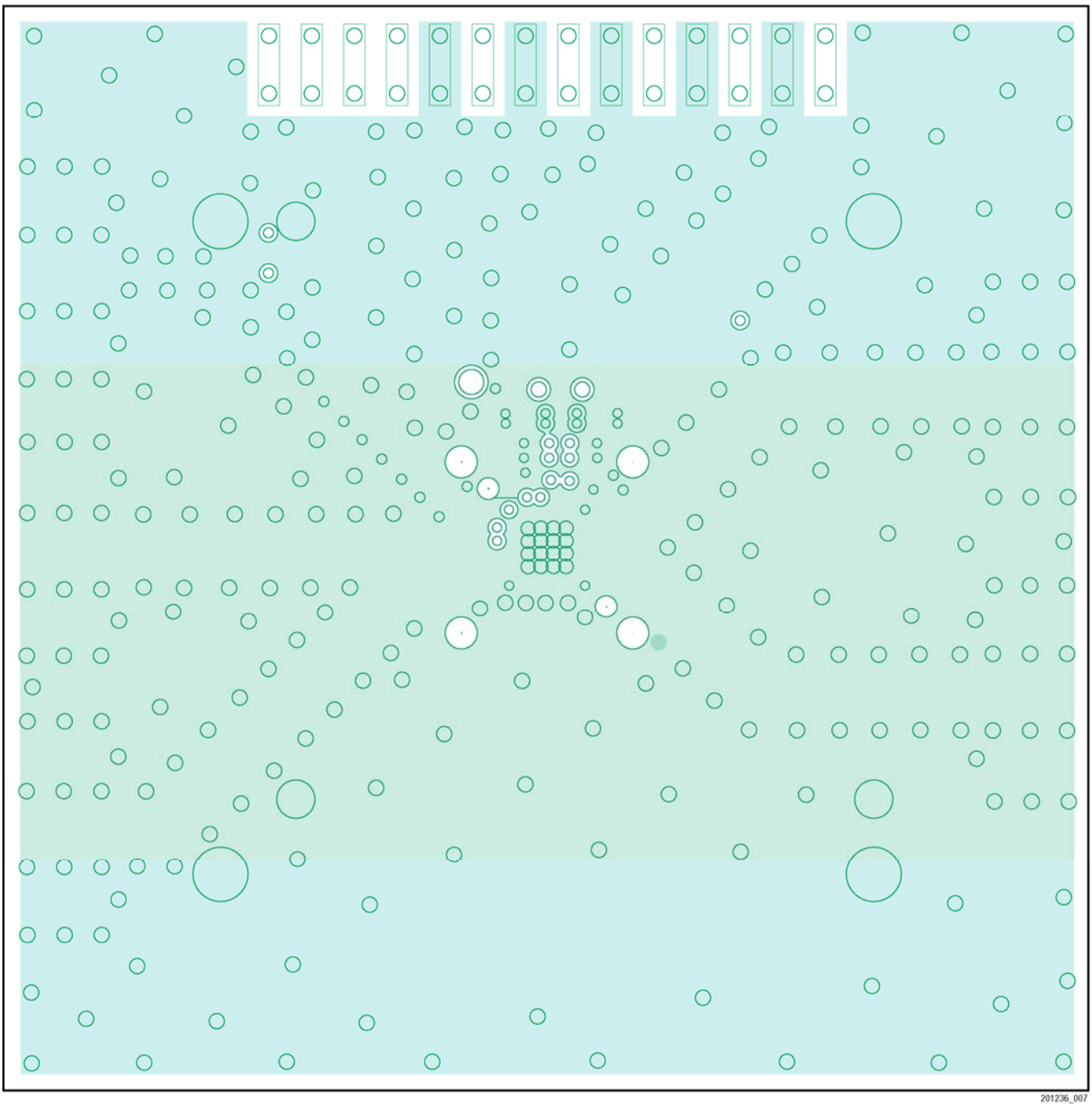

Figure 7. SKY77344-21 Power Amplifier Test Fixture PCB Layer 2

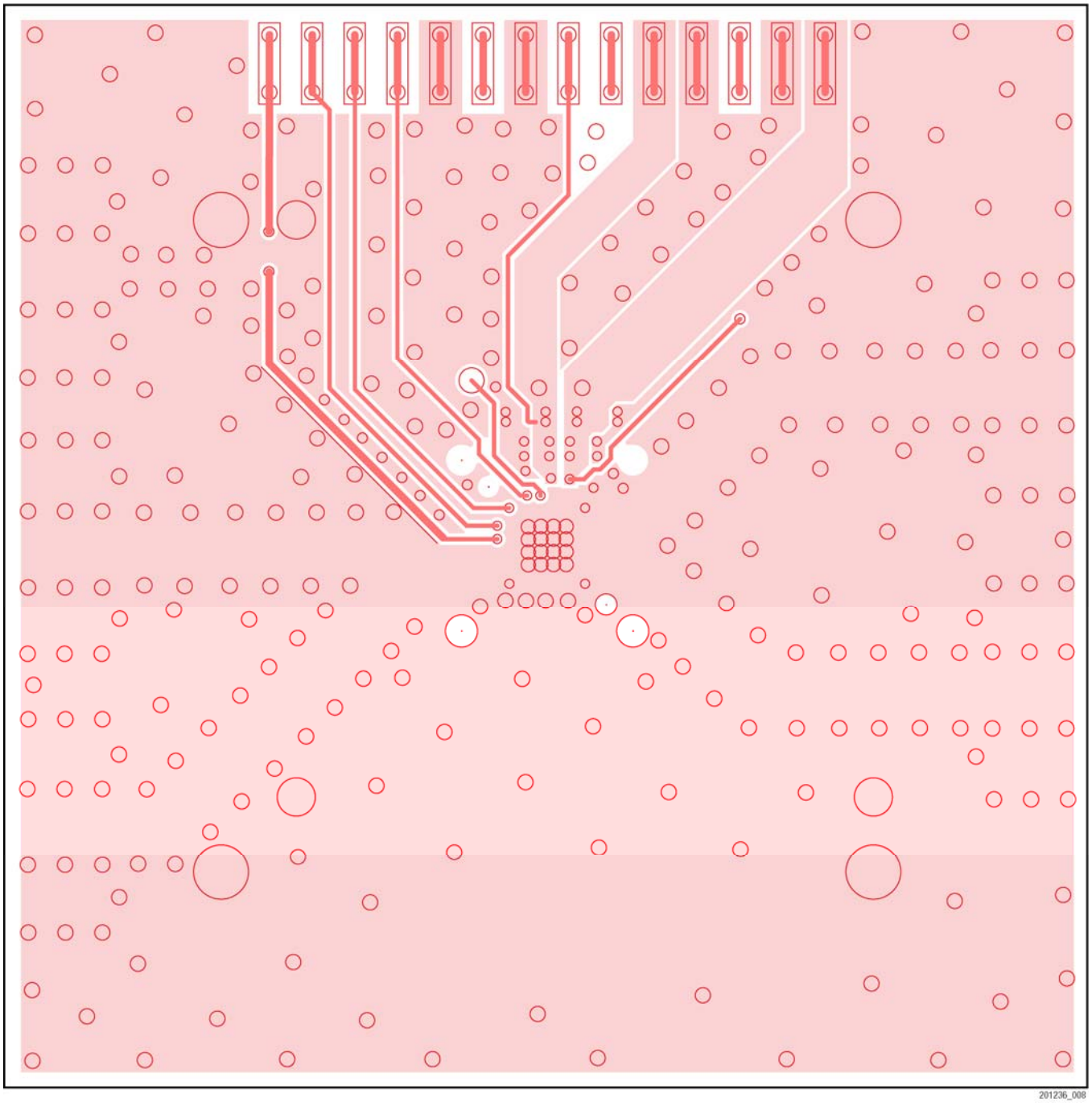

Figure 8. SKY77344-21 Power Amplifier Test Fixture PCB Layer 3

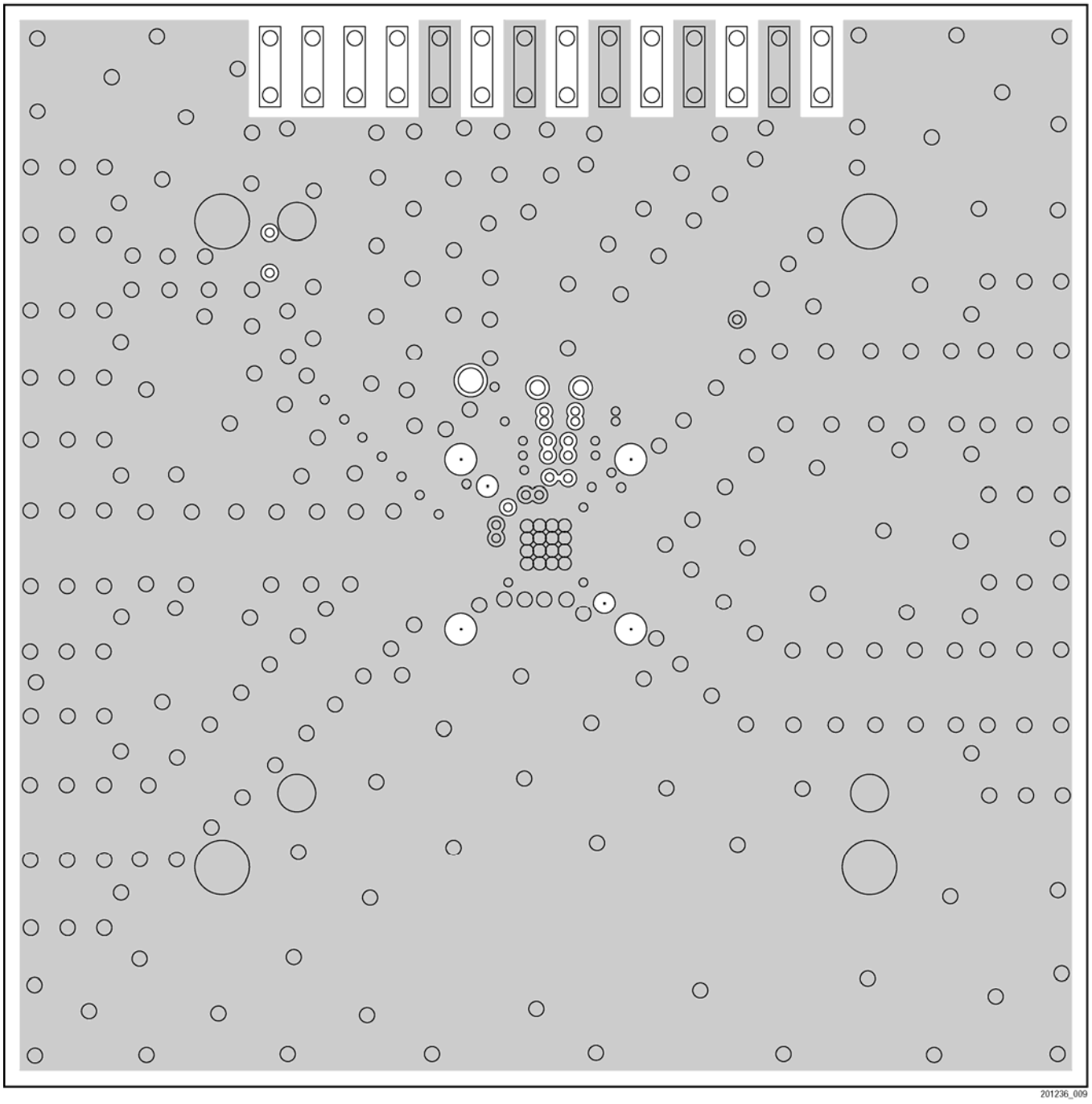

Figure 9. SKY77344-21 Power Amplifier Test Fixture PCB Layer 4

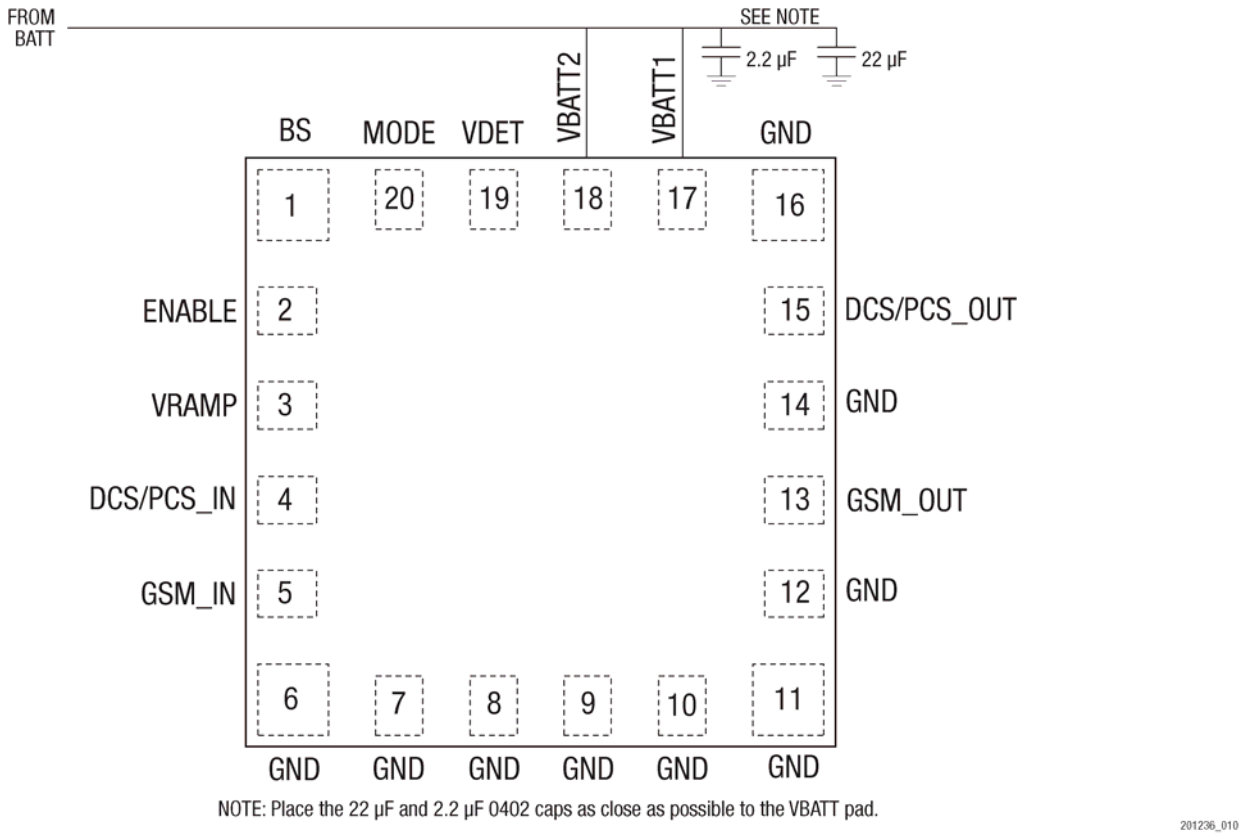

Figure 10. Application Circuit Diagram for SKY77344-21 Power Amplifier

Battery Bypassing

VBATT line of the PA module requires low frequency bypassing capacitance. In modern communication systems, a GSM PA draws rapid pulses of current that can cause a significant transient during the transmission. This might affect the output power mask at high power levels. Most lab supplies are not suited for digital communications and do not emulate the phone board battery condition. Hence, in some cases a higher value capacitor of 68 µF may be required.

In the phone board, battery ESR will reduce the transient voltage pulse and should not require more than a 22µF bypass capacitor. The bypass capacitor should be a good quality ceramic or tantalum capacitor.

INPUT / OUTPUT PAD DESCRIPTION

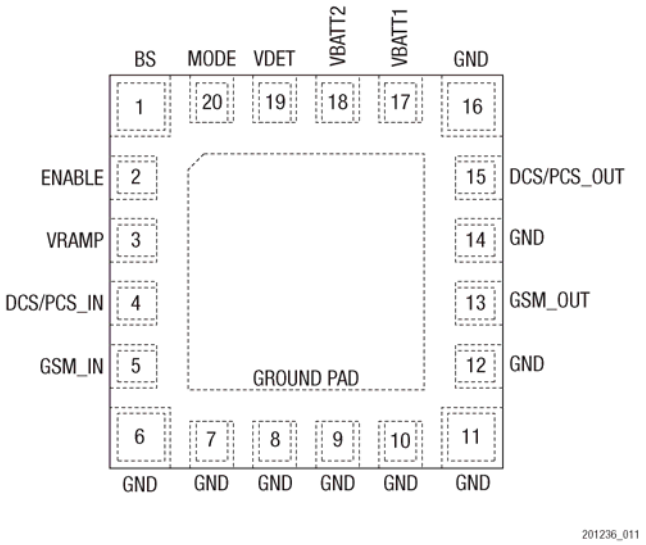

Figure 11. SKY77344-21 Pad Names and Configuration (Top View)

Table 3. SKY77344-21 Pad Descriptions

Pad [1]	Name	Description
1	BS	Band Select: Low = GSM850/900 TX; High = DCS1800 / PCS1900
2	ENABLE	Transmit Enable / Disable: High = Enable, Low = Disable
3	VRAMP	GMSK Power Control / EDGE Mode Bias Control
4	DCS/PCS_IN	DCS1800 / PCS1900 RF Input
5	GSM_IN	GSM850/900 RF Input
13	GSM_OUT	GSM850/900 RF Output
15	DCS/PCS_OUT	DCS1800 / PCS1900 RF Output
17	VBATT1	DC (Battery) Supply
18	VBATT2	DC (Battery) Supply
19	VDET	RF Log Detector Output
20	MODE	GMSK/EDGE Power Control Mode: Low = GMSK, High = EDGE
GROUND	GROUND PAD	Ground pad is device underside.

1. Pad numbers 6-12, 14, 16 are GROUND pads

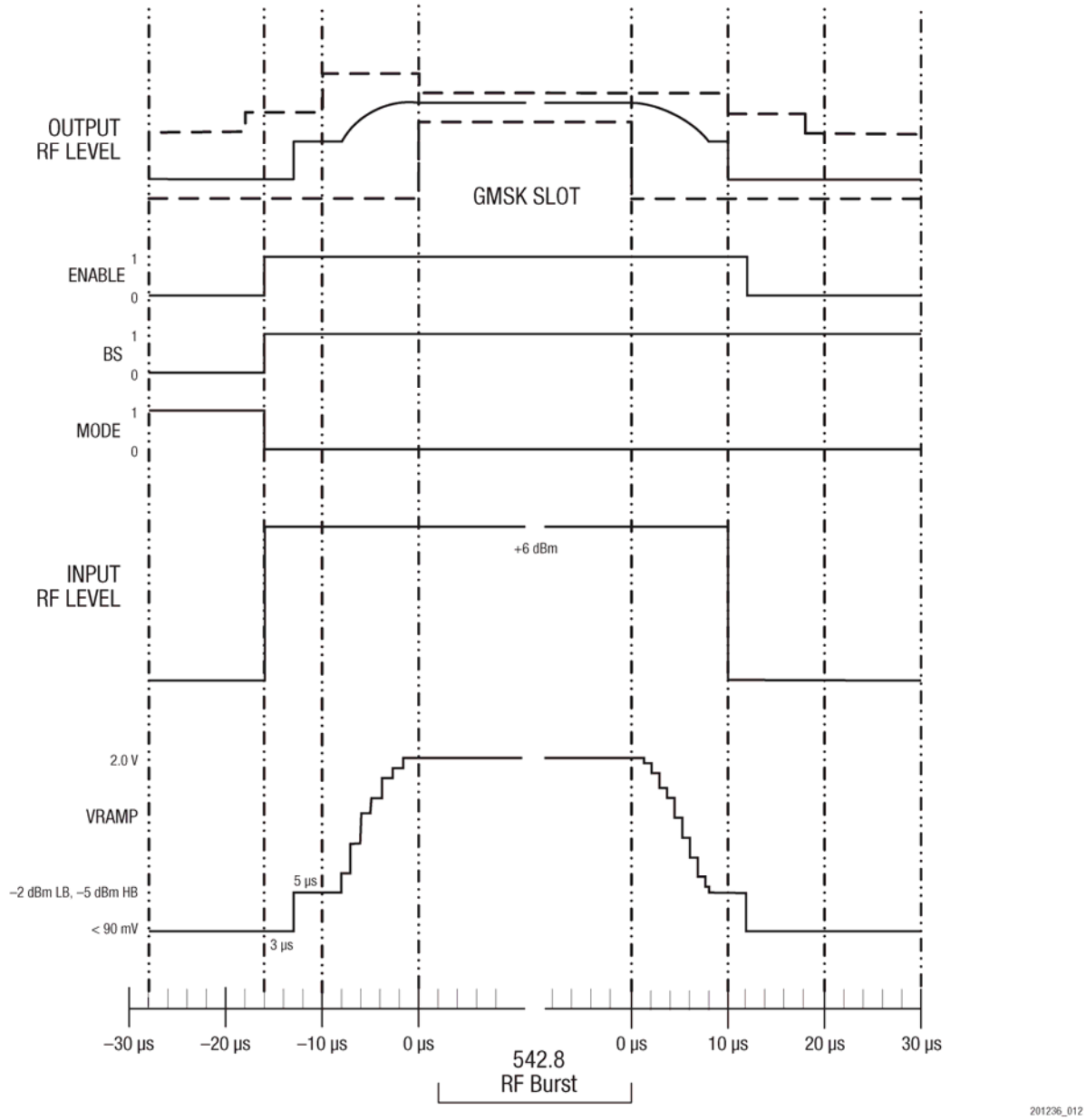

Figure 12. Transmit Timing Diagram for Single-Slot GMSK Operation

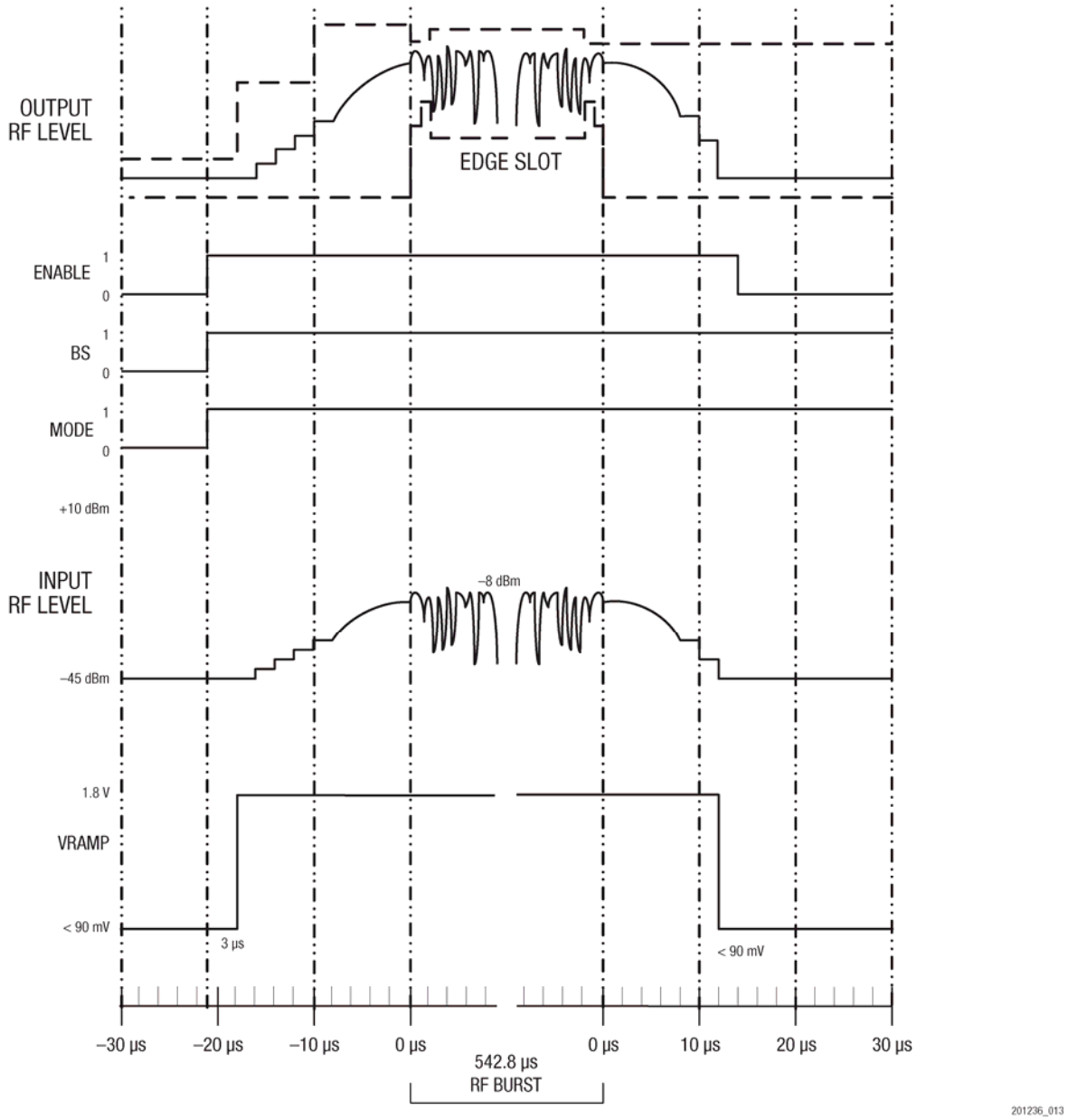

Figure 13. Transmit Timing Diagram for Single-Slot EDGE Timing

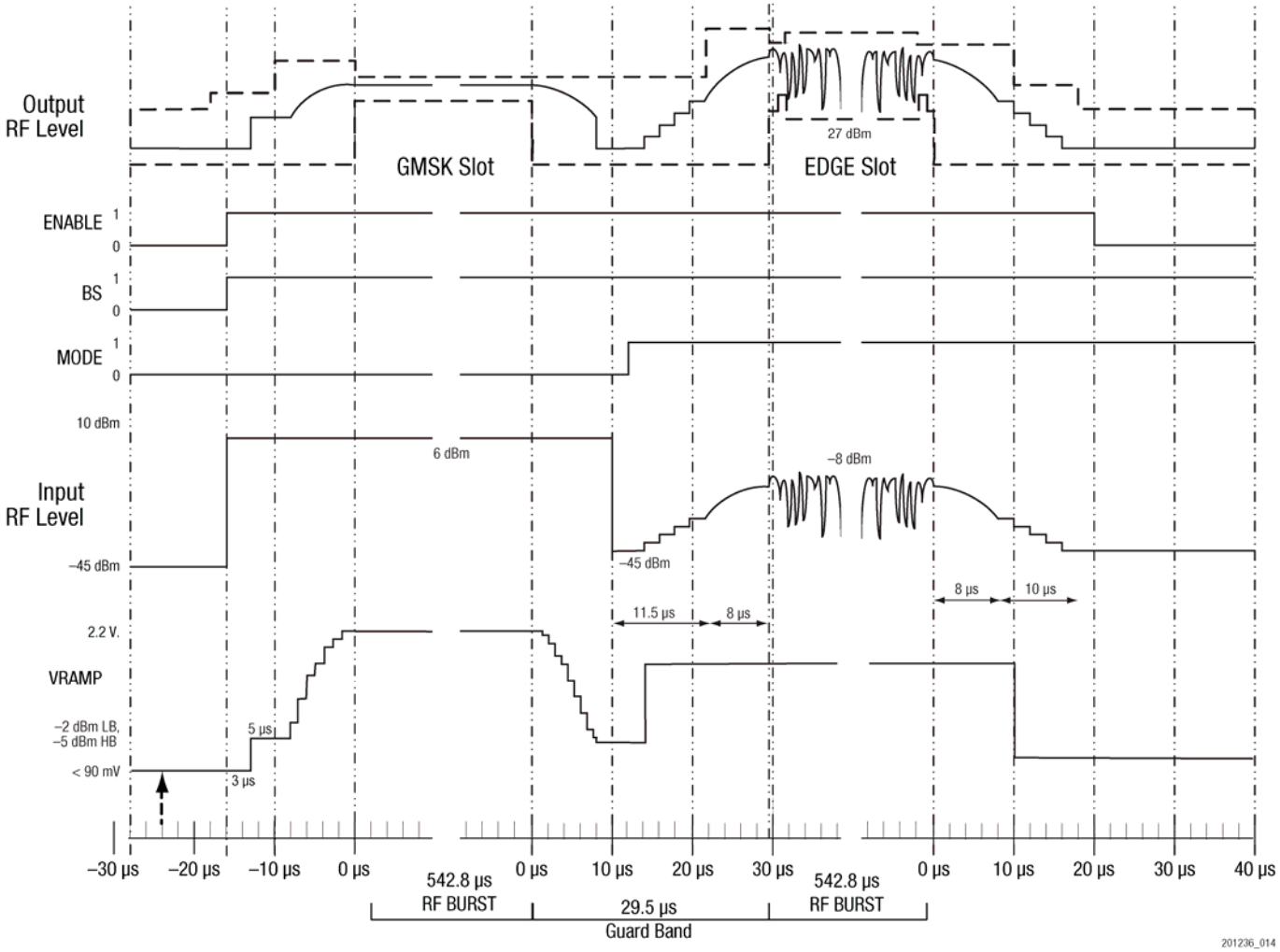

Figure 14. Transmit Timing Diagram for Multi-slot GMSK to EDGE Slot Operation

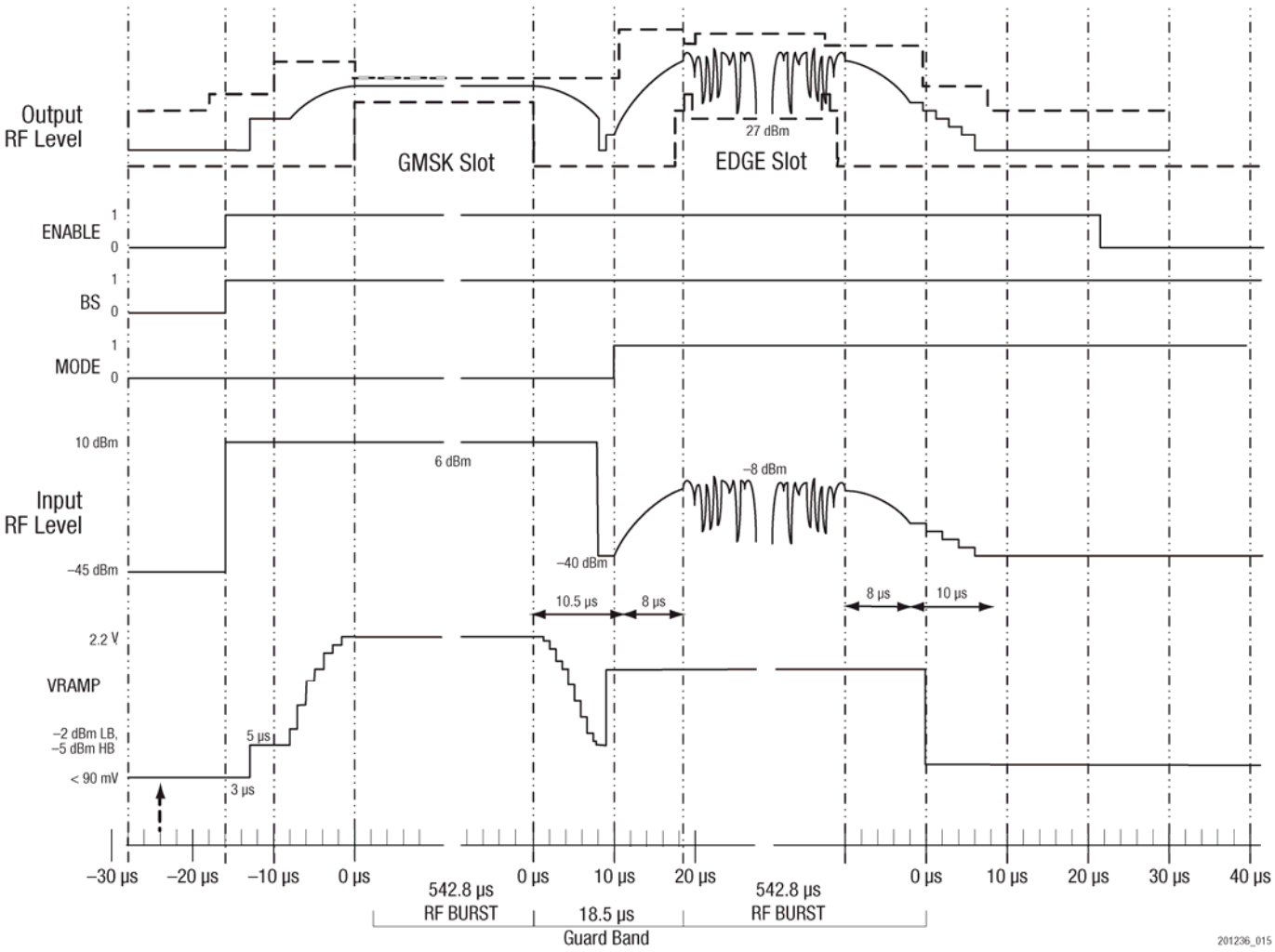

Figure 15. Transmit Timing Diagram for Multi-slot GMSK to EDGE Operation – Maximum Timing Advance

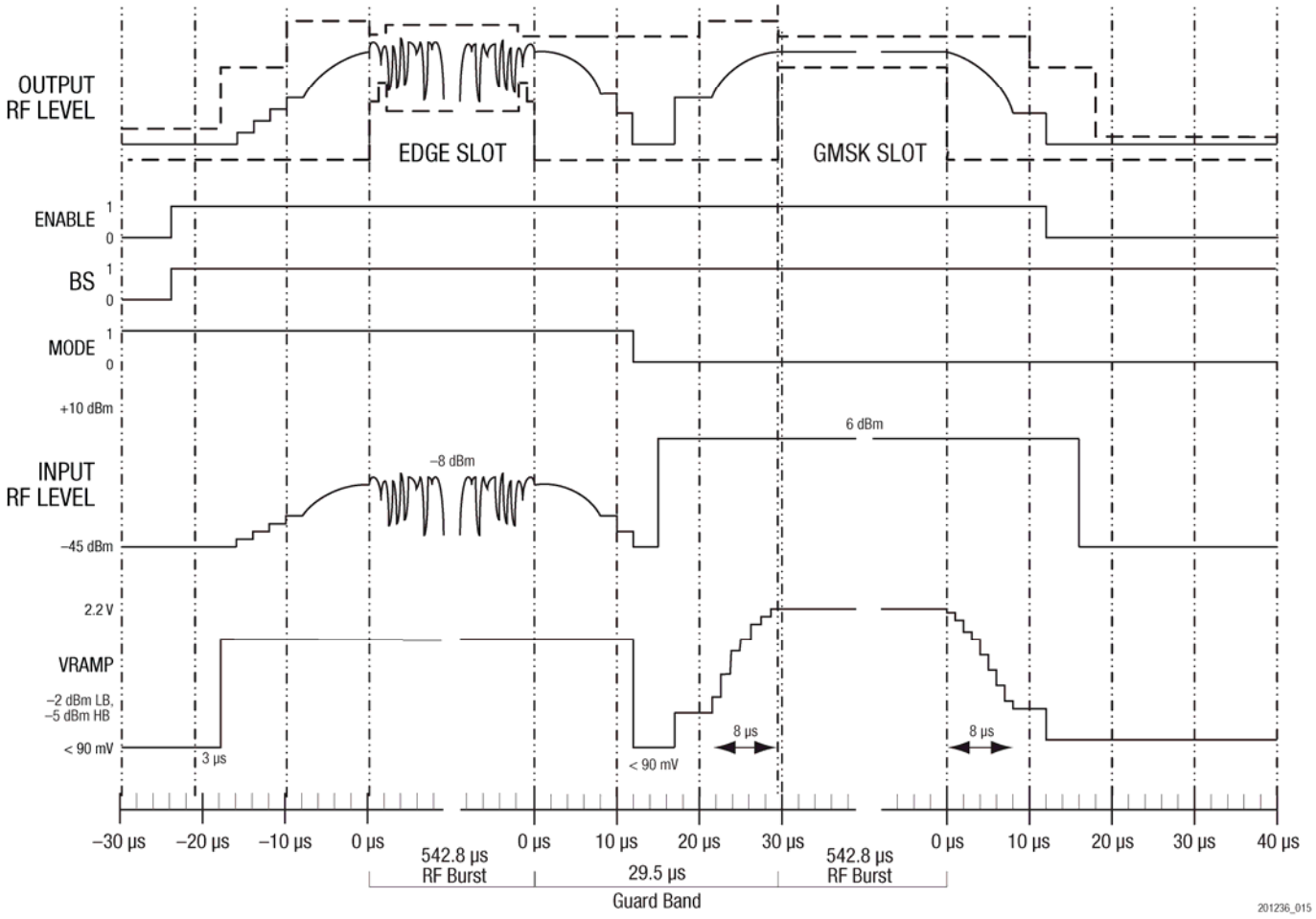

Figure 16. Transmit Timing Diagram for Multi-slot EDGE to GMSK Operation

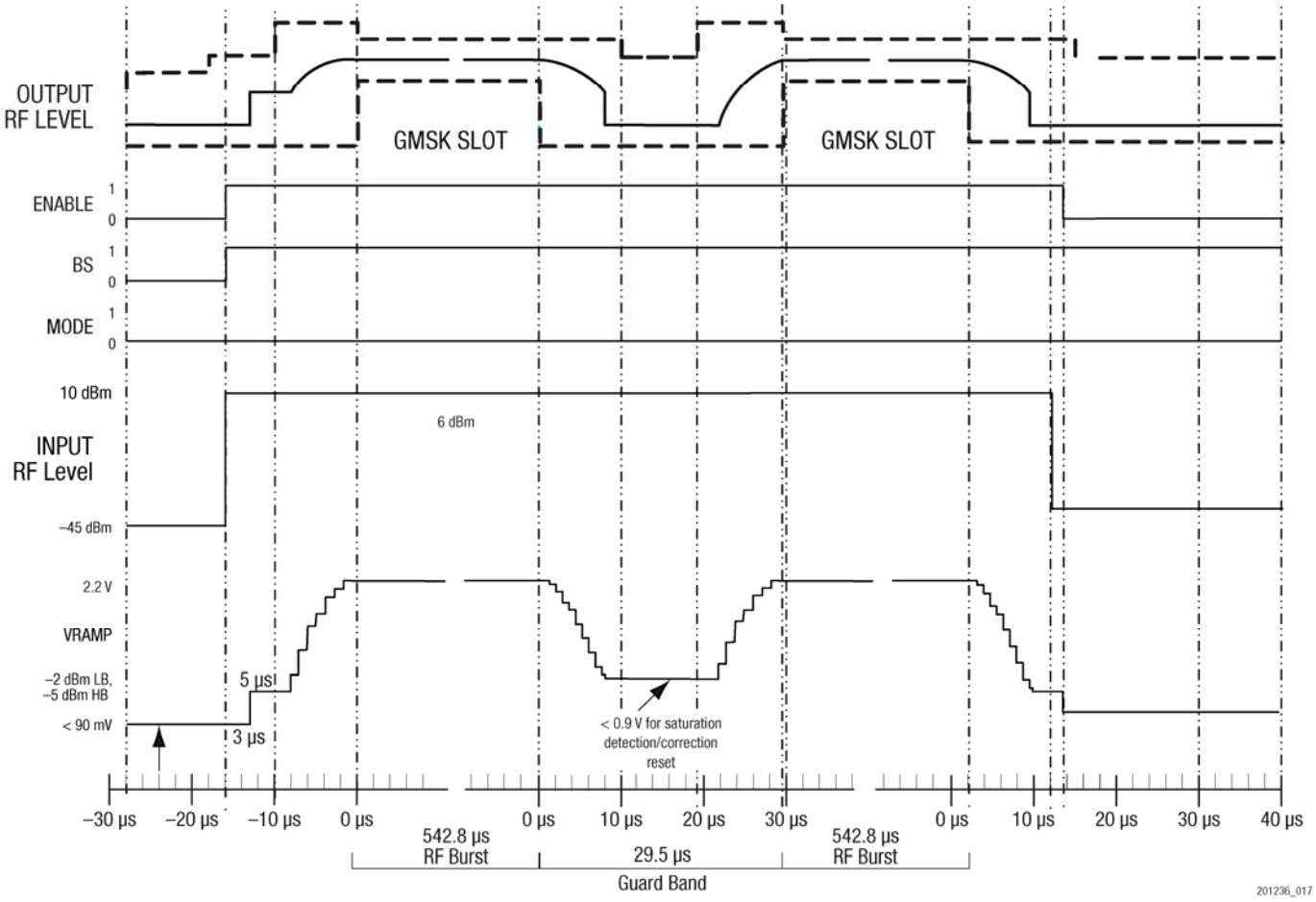

Figure 17. Transmit Timing Diagram for Multi-slot GMSK to GMSK Operation

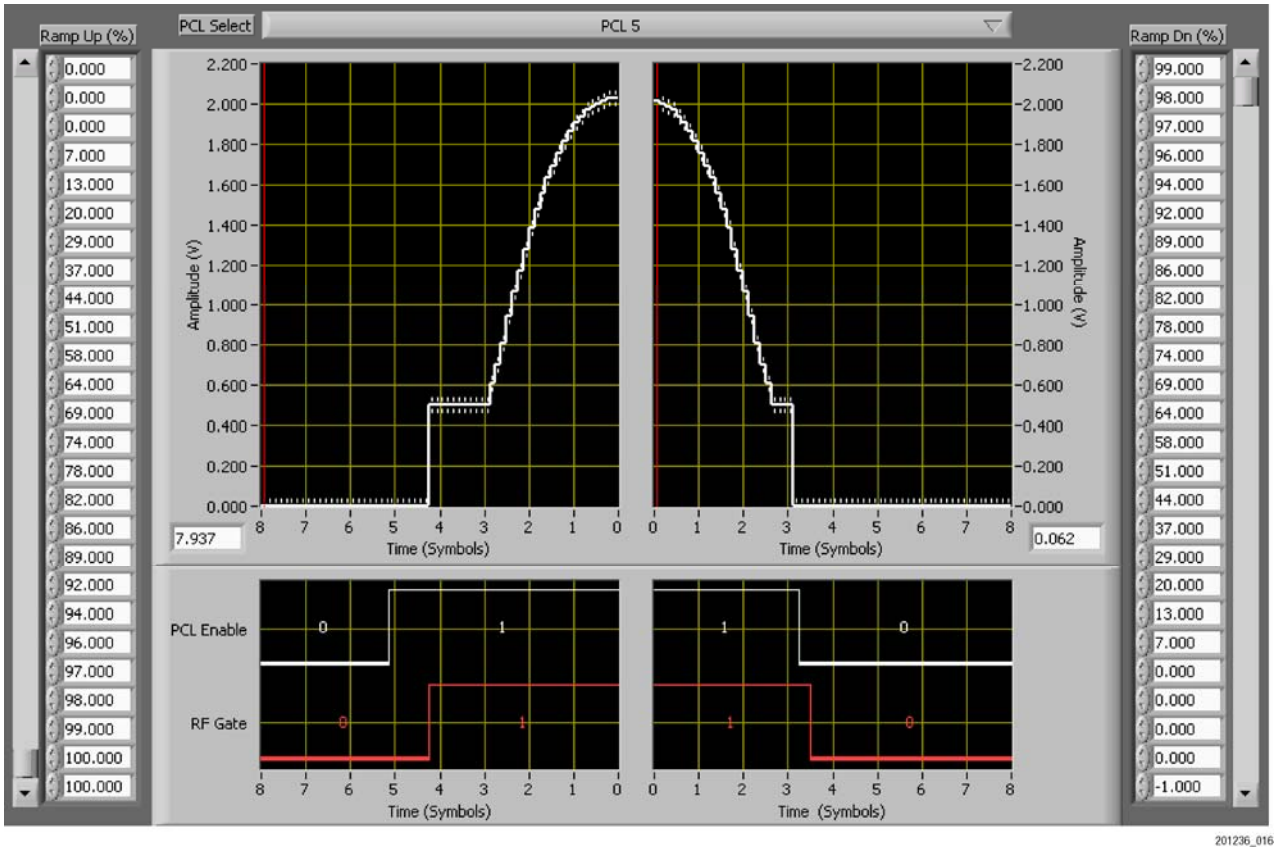

Figure 18. Recommended RAMP Profile

GMSK Ramp Profile Recommendations

- 3 µs from ENABLE edge to VRAMP pedestal set (precharge)
- 5 µs VRAMP pedestal set at –2 dBm (LB), –5 dBm (HB)
- TX_ANT_SW_EN set at end of pedestal
- 10 µs log ramp-up profile
- 10 µs log ramp-down profile
- 1.5 µs dwell at 500 mV ramp level
- VRAMP transitioned low
- ENABLE, TX_ANT_SW_EN set low

Revision History

Revision	Date	Description
A	February 16, 2010	Initial Release

References

Data Sheet: SKY77344-21 PA Module for Quad-Band GSM / EDGE, Document No. 201086