1.3 HX8369-A DSI CMD / Video mode initial code for LGD 4.0 inch panel

DSI Video mode setting:
VSYNC_Width= 8 Hsync
VSYNC_BP= 16 Hsync
VSYNC_FP= 8 Hsync
HSYNC_Width= 5 PCLK
HSYNC_BP= 5 PCLK
HSYNC_FP= 5 PCLK

//Please send initial code in LP mode.**//**
PacketHeader[39 04 00 2C], // Set Password
Payload[B9 FF 83 69],
CheckSum[XX XX]

PacketHeader[39 14 00 0A] // Set Power
Payload[B1 01 00 34 07 00 0F 0F 21 28 3F 3F 07 23 01 E6 E6 E6 E6 E6]
CheckSum[XX XX]

PacketHeader[39 10 00 29] // Set Display
Payload[B2 00 20 0A 0A 70 00 FF 00 00 00 00 03 03 00 01] //DSI CMD mode
Payload[B2 00 23 0A 0A 70 00 FF 00 00 00 00 03 03 00 01] //DSI Video mode
CheckSum[XX XX]

PacketHeader[39 06 00 30] // Set CYC
Payload[B4 00 0C 84 0C 01]
CheckSum[XX XX]

PacketHeader[39 03 00 09] // Set VCOM
Payload[B6 2C 2C]
CheckSum[XX XX]

PacketHeader[39 1B 00 0A] // Set GIP
Payload[D5 00 05 03 00 01 09 10 80 37 37 20 31 46 8A 57 9B 20 31 46 8A 57 9B 07 0F 07 00]
CheckSum[XX XX]

PacketHeader[39 23 00 20] // SetGamma
Payload[E0 00 06 06 29 2D 3F 13 32 08 0C 0D 11 14 11 14 0E 15 00 06 06 29 2D 3F 13 32 08 0C 0D 11 14 11 14 0E 15]
CheckSum[XX XX]

PacketHeader[15 3A 77 1F] // Set Pixel Format

PacketHeader[39 0E 00 15] // Set MIPI
Payload[BA 00 A0 C6 00 0A 00 10 30 6C 02 10 18 40] //1 Lane mode
Payload[BA 00 A0 C6 00 0A 00 10 30 6C 02 11 18 40] //2 Lane mode
CheckSum[XX XX]

PacketHeader[05 11 00 36] // Sleep Out
Delay 120ms

PacketHeader[05 29 00 1C] // Display On
Delay 10ms

Video Stream for DSI CMD mode：

(1) Write memory start
PacketHeader[39 WC0 WC1 ECC]
Payload[2C, pixel data……..]
CheckSum[XX XX]

(2) Write memory continue
PacketHeader[39 WC0 WC1 ECC]
Payload[3C, pixel data……..]
CheckSum[XX XX]

Note: WC0 is Word Count low byte, WC1 is Word Count high byte. The Word Count is equal to Payload length including one byte CMD(2C or 3C) and pixels length.
HX8369-A does not support sub-pixel write function, so pixel length in these packets must be multiple of 3(RGB888 format).