

## =Short Datasheet=

## AK8975/AK8975B

## **3-axis Electronic Compass**

## 1. Features

A 3-axis electronic compass IC with high sensitive Hall sensor technology. Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

#### Functions:

- 3-axis magnetometer device suitable for compass application
- Built-in A to D Converter for magnetometer data out
- 13 bit data out for each 3 axis magnetic components
  - Sensitivity: 0.3µT/LSB typ.
- Serial interface
  - I<sup>2</sup>C bus interface.

Standard mode and Fast mode compliant with Philips I2C specification Ver.2.1

- 4-wire SPI
- Operation mode:

Power-down mode, Single Measurement mode, Continuous Measurement mode, External trigger mode, Self test mode and Fuse access mode.

- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Built-in oscillator for internal clock source
- Power on Reset circuit
- Self test function with built-in internal magnetic field generator

#### Operating temperatures:

• -30°C to +85°C

Operating supply voltage:

• Analog power supply +2.4V to +3.6V

• Digital Interface supply +1.65V to analog power supply voltage.

Current consumption:

• Power-down: 10µA max.

• Measurement:

- Average power consumption at Continuous Measurement mode (@8Hz): 1.0 mA max.

#### Package:

AK8975 16-pin QFN package : 4.0mm×4.0mm×0.75mm AK8975B 14-pin WL-CSP (BGA) : 2.0mm×2.0mm×0.65mm

## 2. Overview

AK8975/B is 3-axis electronic compass IC with high sensitive Hall sensor technology.

Small package of AK8975/B incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

#### AK8975/B has the following features:

- (1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.
- (2) Enhanced architecture of signal processor realizes wide dynamic measurement range and high resolution with lower current consumption.

Output data resolution: 13 bit (0.3µT/LSB).

Measurement range:  $\pm 1200 \mu T$ 

- (3) Digital serial interface
  - I<sup>2</sup>C bus interface to control AK8975/B functions and to read out the measured data by external CPU. A dedicated power supply for I<sup>2</sup>C bus interface can work in low-voltage apply as low as 1.65V.
  - 4-wire SPI (Serial port interface) is also supported. A dedicated power supply for SPI interface can work in low-voltage apply as low as 1.65V.
- (4) DRDY pin and register inform to system that measurement is end and set of data in registers are ready to be read
- (5) Device is worked by on-chip oscillator so no external clock source is necessary.
- (6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

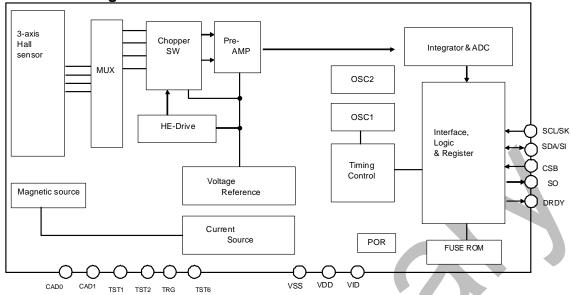


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## 4. Circuit Configuration

## 4.1. Block Diagram



### 4.2. Block Function

Function
Monolithic Hall sensor element.
Multiplexer for selecting driving and signal detecting path from Hall sensor
elements.
Performs chopping.
Magnetic sensor drive circuit for constant-current driving of sensor
Variable-gain differential amplifier used to amplify the magnetic sensor signal.
Integrates and amplifies pre-AMP output and performs analog-to-digital
conversion.
Generates an operating clock for sensor measurement.
6.144MHz(typ)
Generates a clock for measurement frequency of 8Hz.
128kHz(typ)
Power On Reset circuit. Generates reset signal on rising edge of VDD.
Exchanges data with an external CPU.
DRDY pin indicates sensor measurement end and data is ready to be read.
I <sup>2</sup> C bus interface using two pins, namely, SCL and SDA. Standard mode and Fast
mode are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin.
4-wire SPI is also supported by SK, SI, SO and CSB pins.
4-wire SPI works in VID pin voltage down to 1.65V, too.
Generates a timing signal required for internal operation from a clock generated
by the OSC1.
Generates magnetic field for self test of magnetic sensor.
Generates current for generating magnetic field.
Fuse for adjustment

## 4.3. Pin Function

SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain  SI I SI I SPA VID CMOS  SI I SPA SO O VID CMOS  SI I Serial data input pin  When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII When the 4-wire SPI is selected (SSB pin is connected to VII Informs measurement ended and data is ready to be read.  7 C4 VID Power Digital interface positive power supply pin.  16 B1 VDD Power Analog Power supply pin.  17 C4DO I/O VDD CMOS Ground pin.  When the 1°C bus interface is selected (CSB pin is connected to VII GADo: Slave address 0 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADo: Slave address 1 input pin When the 4-wire serial interface is selected (Connect to VSS.  When the 1°C bus interface is selected (CSB pin is connected to VII CADo: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADo: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADo: Slave address 1 input pin When the 4-wire serial interface is selected Connect to VSS.  8 - NC1 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  12 - NC2 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  External trigger mode is not in use, keep this pin electrically nonconnected.  Batternal trigger mode is not in use, keep this pin electrically nonconnected.  Hi-Z output. Keep this pin electrically nonconnected.	<u>4.3.</u>	1 1111	runcti	OH			
2 A2 CSB I VID CMOS  Chip select pin for 4-wire SPI.  "L" active. Connect to VID when selecting I°C bus interface.  When the I°C bus interface is selected (CSB pin is connected to VID)  SCL: Control data clock input pin Input: Schmidt trigger  When the 4-wire SPI is selected  SK: Serial clock input pin Input: Schmidt trigger  When the 4-wire SPI is selected (CSB pin is connected to VID)  SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain  When the 4-wire SPI is selected (CSB pin is connected to VID)  SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain  When the 4-wire SPI is selected SI: Serial data input pin When the 4-wire SPI is selected (CSB pin is connected to VID)  When the 4-wire SPI is selected (CSB pin is connected to VID)  When the 4-wire SPI is selected (CSB pin is connected to VID)  When the 4-wire SPI is selected SI: Serial data input pin When the 1°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  When the 4-wire SPI is selected Connected to VID (CMOS)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface is selected (CSB pin is connected to VID)  The the I°C bus interface positive				I/O	supply	Туре	Function
A3   SCL	2	A2	CSB	I		CMOS	•
SK Sc. Serial clock input pin  SK SDA I/O  SDA I/O  VID  SDA: Control data input/output pin input: Schmidt trigger. Output: Open drain  When the I*C bus interface is selected (CSB pin is connected to VII input: Schmidt trigger. Output: Open drain  When the 4-wire SPI is selected  SI: Serial data input pin  When the 1*C bus interface is selected (CSB pin is connected to VII Hi-Z output. Connect to VSS or VID.  When the 4-wire SPI is selected  Serial data output pin.  Data ready signal output pin. Active "H". Informs measurement ended and data is ready to be read.  To C4 VID Power Digital interface positive power supply pin.  16 B1 VDD Power Analog Power supply pin.  15 C1 VSS Power Ground pin.  When the 1*C bus interface is selected (CSB pin is connected to VII CADO: Slave address 0 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial interface is selected (CADO: Slave address 1 input pin When the 4-wire serial int	4	A3	SCL	ı	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID)  SCL: Control data clock input pin
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Hi-Z output. Connect to VSS or VID.   When the 4-wire SPI is selected   Serial data output pin.   Active "H"   Informs measurement ended and data is ready to be read.			SI	ı			
Data ready signal output pin. Active "H". Informs measurement ended and data is ready to be read.	6	B4	so	0	VID	CMOS	When the 4-wire SPI is selected
16 B1 VDD Power Analog Power supply pin.  15 C1 VSS Power Ground pin.  When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VII CAD0: Slave address 0 input pin When the 4-wire serial interface is selected (CSB pin is connected to VII CAD1: Slave address 1 input pin When the 4-wire serial interface is selected Connect to VSS.  When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VII CAD1: Slave address 1 input pin When the 4-wire serial interface is selected Connect to VSS.  8 - NC1 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  12 - NC2 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ resister. When External trigger mode is not in use, keep this pin electrically nonconnected or connect to VSS.  1 A1 TST1 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.  9 D4 TST6 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	10	С3	DRDY	0	VID	CMOS	Data ready signal output pin. Active "H".
15 C1 VSS Power Ground pin.  13 D1 CADO I/O VDD CMOS  The connected to VIII CADO: Slave address 0 input pin When the 4-wire serial interface is selected (CSB pin is connected to VIII CADO: Slave address 0 input pin When the 4-wire serial interface is selected Connect to VSS.  When the 1°C bus interface is selected (CSB pin is connected to VIII CAD1: Slave address 1 input pin When the 4-wire serial interface is selected Connect to VSS.  8 - NC1 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  12 - NC2 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  External trigger pulse input pin.  Enabled only in External trigger mode. Pulled down by 100kΩ resister. When External trigger mode is not in use, keep this pin electrically nonconnected or connect to VSS.  1 A1 TST1 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.  9 D4 TST6 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	7	C4	VID	-	-	Power	Digital interface positive power supply pin.
D1	16	B1	VDD	-	-	Power	Analog Power supply pin.
D1 CAD0 I/O VDD CMOS CAD0: Slave address 0 input pin When the 4-wire serial interface is selected Connect to VSS.  When the I²C bus interface is selected (CSB pin is connected to VIII CAD1: Slave address 1 input pin When the 4-wire serial interface is selected (CSB pin is connected to VIII CAD1: Slave address 1 input pin When the 4-wire serial interface is selected Connect to VSS.  NC1 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.  TRG I VID CMOS External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ resister. When External trigger mode is not in use, keep this pin electrically nonconnected or connect to VSS.  A1 TST1 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	15	C1	VSS	-	-	Power	Ground pin.
D2	13	D1	CAD0	I/O	VDD	CMOS	When the 4-wire serial interface is selected
12 - NC2 I/O VID ANALOG Hi-Z output. Keep this pin electrically nonconnected.    3	11	D2	CAD1	I/O	VDD	CMOS	When the 4-wire serial interface is selected
3 A4 TRG I VID CMOS External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ resister. When External trigger mode is not in use, keep this pin electrically nonconnected or connect to VSS.  1 A1 TST1 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.  9 D4 TST6 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	8	-	NC1	I/O	VID	ANALOG	Hi-Z output. Keep this pin electrically nonconnected.
3 A4 TRG I VID CMOS Enabled only in External trigger mode. Pulled down by 100kΩ resister. When External trigger mode is not in use, keep this pin electrically nonconnected or connect to VSS.  1 A1 TST1 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.  9 D4 TST6 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	12	-	NC2	I/O	VID	ANALOG	Hi-Z output. Keep this pin electrically nonconnected.
9 D4 TST6 I/O VDD ANALOG Hi-Z output. Keep this pin electrically nonconnected.	3	A4	TRG	I	VID	CMOS	Enabled only in External trigger mode. Pulled down by $100k\Omega$ resister. When External trigger mode is not in use, keep this pin
	1	A1	TST1	I/O	VDD	ANALOG	Hi-Z output. Keep this pin electrically nonconnected.
14 C2 TST2 I/O VDD ANALOG Hi-7 output Keen this pin electrically ponconnected	9	D4	TST6	I/O	VDD	ANALOG	Hi-Z output. Keep this pin electrically nonconnected.
14 62 1612 1/6 VBB /11/2 64-pair. Neep tills pill disollicating file installication.	14	C2	TST2	I/O	VDD	ANALOG	Hi-Z output. Keep this pin electrically nonconnected.

## 5. Overall Characteristics

### 5.1. Absolute Maximum Ratings

VSS=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (VDD, VID)	V+	-0.3	+6.5	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-	<u>±</u> 10	mA
Storage temperature	TST	-40	+125	°C

<sup>(</sup>Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

### 5.2. Recommended Operating Conditions

VSS=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	°C
Power supply voltage	VDD pin voltage	VDD	2.4	3.0	3.6	V
	VID pin voltage	VID	1.65		VDD	V

#### 5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:

VDD=2.4V to 3.6V, VID=1.65V to VDD, Temperature range=-30°C to 85°C

#### 5.3.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Тур.	Max.	Unit
High level input voltage 1	VIH1	CSB TRG		70%VID			V
Low level input voltage 1	VIL1	SK SI				30%VID	V
High level input voltage 2	VIH2	SCL		70%VID		VID+0.5	V
Low level input voltage 2	VIL2	SDA		-0.5		30%VID	V
High level input voltage 3	VIH3	CAD0		70%VDD			V
Low level input voltage 3	VIL3	CAD1				30%VDD	V
Input current	IIN	SCL SK SDA SI CSB	Vin=VSS or VID	-10		+10	μА
Hysteresis input voltage	VHS	SCL	VID≥2V	5%VID			V
(Note 2)		SDA TRG	VID<2V	10%VID			V
High level output voltage 1	VOH1	SO	IOH≥-100µA (Note 5)	80%VID			V
Low level output voltage 1	VOL1	DRDY	IOL≤+100µA (Note 5)			20%VID	V
Low level output voltage 2	VOL2	SDA	IOL≤3mA VID≥2V			0.4	V
(Note 3)(Note 4)			IOL≤3mA VID<2V			20%VID	V
Current consumption	IDD1	VDD VID	Power-down mode VDD=VID=2.5V		TBD	10	μΑ
	IDD2		When magnetic sensor is driven VDD=VID=2.5V		TBD	TBD	mA
	IDD3		Average in Continuous measurement mode VDD=VID=2.5V		TBD	1	mA

(Note 2) Schmitt trigger input (reference value for design)

(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the I<sup>2</sup>C bus interface)

(Note 4) Output is open-drain. Connect a pull-up resistor externally.

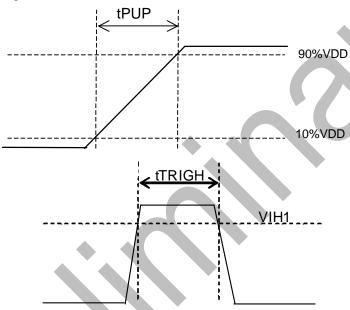
(Note 5) Load capacitance: 20pF

### 5.3.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Тур.	Max.	Unit
Power supply rise time effective for POR circuit (Note 6)	tPUP	VDD	Period of time from 10%VDD to 90%VDD (Note 7)			200	μs
Power-down mode transit time (Note 6)		VDD	Period of time from 90%VDD at power-on to Power-down mode			TBD	μs
Effective pulse width for trigger input	tTRIGH	TRG		200			ns
Effective frequency for trigger input (Note 6)		TRG				TBD	Hz
Wait time before mode setting	Twat			100			μs

(Note 6) Reference value for design

(Note 7) Only when VDD meets this condition, POR circuit starts and generates the reset pulse. This pulse initializes all registers and AK8975/B transits to Power-down mode.



5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Measurement data output bit	DBIT			13		bit
Output data rate	ODR	Continuous measurement mode		8		Hz
Time for measurement	TSM	Single measurement mode		7.30		ms
Magnetic sensor sensitivity	BSE	Tc=25°C (Note 8)	TBD	0.3	TBD	μT/LSB
Magnetic sensor measurement range (Note 9)	BRG	Tc=25°C (Note 8)	±1167	±1229	±1290	μТ
Magnetic sensor initial offset (Note 10)		Tc=25°C	-1000		+1000	LSB

(Note 8) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM.

(Note 9) Reference value for design

(Note 10) Value of measurement data register on shipment without applying artificial magnetic field.

### 5.3.4. 4-wire SPI Interface

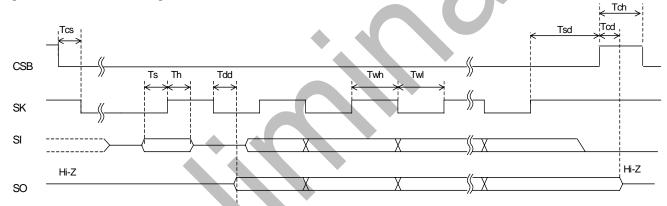
4-wire SPI interface is compliant with mode 3

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
CSB setup time	Tcs		50			ns
Data setup time	Ts		50			ns
Data hold time	Th		50			ns
SK high time	Twh	VID≥2.5V	100			ns
		2.5V>VID≥1.65V	150			ns
SK low time	Twl	VID≥2.5V	100			ns
		2.5V>VID≥1.65V	150			ns
SK setup time	Tsd		50			ns
SK to SO delay time	Tdd				50	ns
CSB to SO delay time	Tcd				50	ns
SK rise time (Note 12)	Tr				100	ns
SK fall time (Note 12)	Tf				100	ns
CSB high time	Tch		150			ns

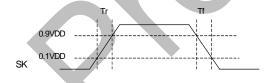
(Note 11) SO load capacitance: 20pF

(Note 12) These parameter values are sample values; not all values are measured.

### [Four-wire serial interface]



[Rise time and fall time]



### 5.3.5. I<sup>2</sup>C Bus Interface

CSB pin = "H"

I<sup>2</sup>C bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

#### (1) Standard mode

 $fSCL{\le}100kHz$ 

1.65V≤VID≤VDD

Symbol	Parameter	Min.	Тур.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			μS
tLOW	SCL clock "Low" time	4.7			μS
tR	SDA and SCL rise time			1.0	μS
tF	SDA and SCL fall time			0.3	μS
tHD:STA	Start Condition hold time	4.0			μS
tSU:STA	Start Condition setup time	4.7			μS
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

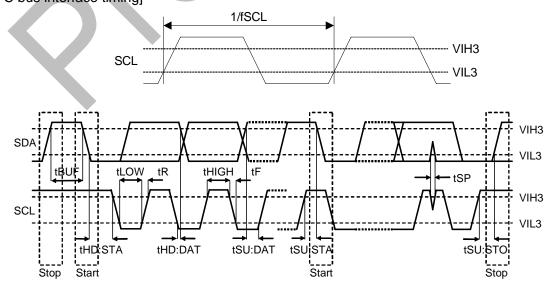
#### (2) Fast mode

 $100kHz < fSCL \le 400kHz$ 

1.65V≤VID≤VDD

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			μs
tLOW	SCL clock "Low" time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μS
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μS
tSP	Noise suppression pulse width			50	ns

## [I<sup>2</sup>C bus interface timing]



## 6. Functional Explanation

#### 6.1. Power state

When VDD and VID is turned on from VDD=0V and VID=0V, all registers in AK8975/B are initialized by POR circuit and AK8975/B transits to Power-down mode.

VDD	VID	Power state
0V	0V	OFF
0V	1.65V to 3.6V	OFF. It doesn't affect external interface.
2.4V to 3.6V	0V	OFF. It consumes current same as Power-down
		mode.
2.4V to 3.6V	1.65V to VDD	ON

Table 6.1

#### 6.2. Reset functions

AK8975/B has two types of reset;

- (1) Power on reset (POR)
  - POR works when VDD is turned on from 0V, until VDD reaches specified level (about 2V: reference value for design). When POR is released, AK8975/B is reset.
- (2) VID monitor
  - When VID is turned off, AK8975/B is reset.

When AK8975/B is reset, all registers are initialized and AK8975/B transits to Power-down mode.



#### 6.3. Operation Modes

AK8975/B has following six operation modes:

- (1) Power-down mode
- (2) Continuous measurement mode
- (3) Single measurement mode
- (4) External trigger measurement mode
- (5) Self-test mode
- (6) Fuse ROM access mode

By setting CNTL register MODE[3:0] bits, the operation set for each mode is started. A transition from one mode to another is shown below.

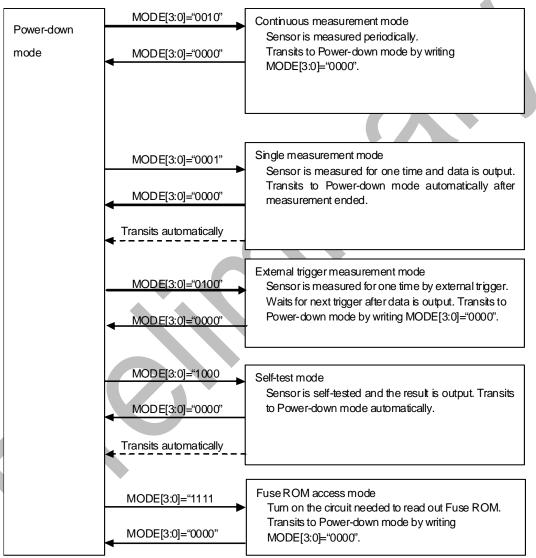


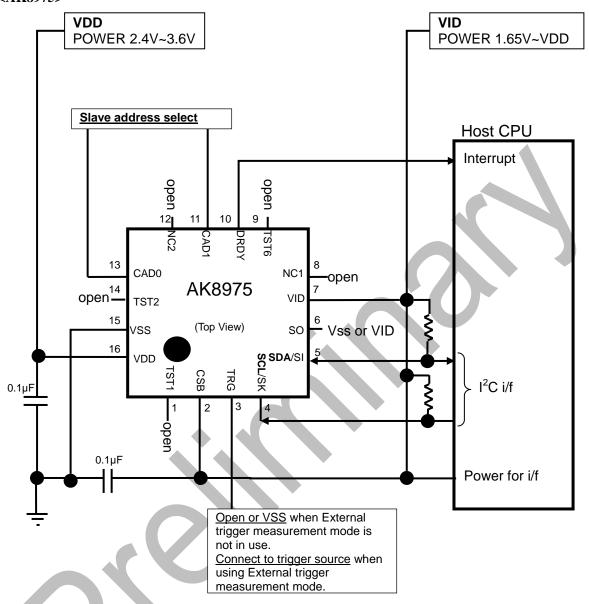
Figure 6.1 Operation modes

When power is turned ON, AK8975/B is in power-down mode. When MODE[3:0] is set, AK8975/B transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 100µs(Twat) is needed before setting another mode.

## 7. Example of Recommended External Connection

### 7.1. I<sup>2</sup>C Bus Interface

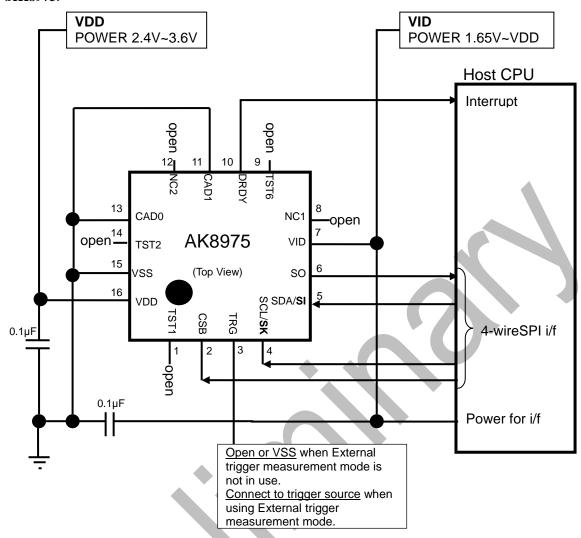
<AK8975>



<**AK8975B**>
Same as AK8975

### 7.2. 4-wire SPI Interface

#### <AK8975>



**<AK8975B>** Same as AK8975

## 8. Package

## 8.1. Marking

#### <AK8975>

Company logo: AKMProduct name: 8975

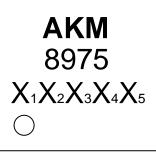
• Date code:  $X_1X_2X_3X_4X_5$ 

 $X_1 = ID$ 

 $X_2$  = Year code

 $X_3X_4$  = Week code

 $X_5 = Lot$ 



<Top view>

#### <AK8975B>

• Product name: 8975

• Date code:  $X_1X_2X_3X_4X_5$ 

 $X_1 = ID$ 

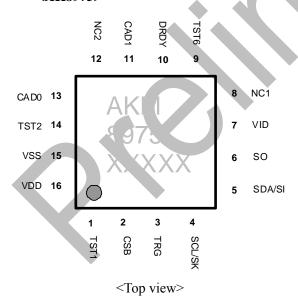
 $X_2$  = Year code

 $X_3X_4$  = Week code

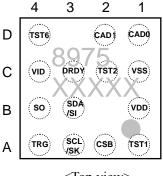
 $X_5 = Lot$ 



# 8.2. Pin Assignment <AK8975>



### <AK8975B>



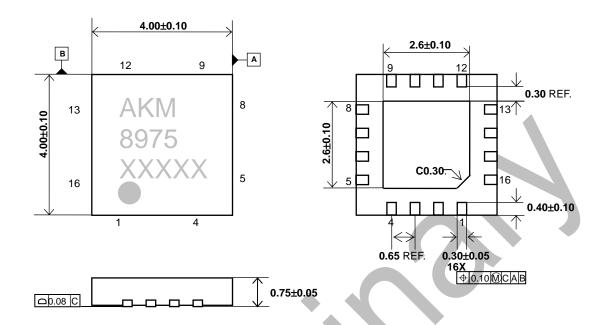
<Top view>

### 8.3. Outline Dimensions

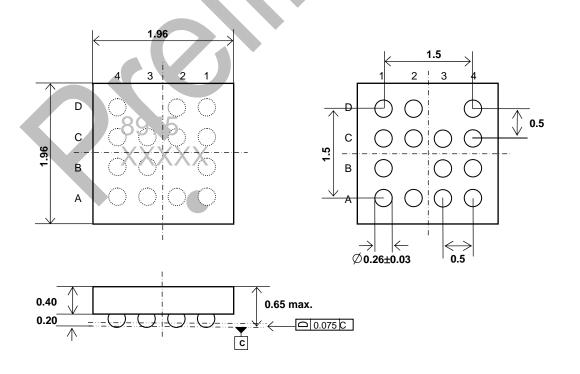
### <AK8975>

[mm]

[mm]



<AK8975B>



## 8.4. Recommended Foot Print Pattern

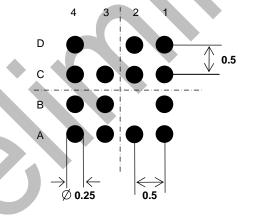
<AK8975>

4.6±0.1 3.0±0.1 0.80±0.10 9.65×3=1.95±0.05 1.0±9.1 1.0±9.7 1.0±9.7

<AK8975B>

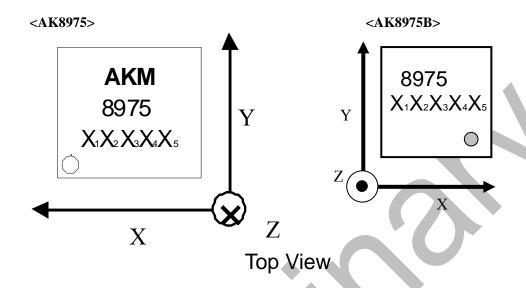
[mm]

[mm]



## 9. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions. On the Z-axis, data increases as the magnetic flux density in the direction from the back of the package to the front face increases.



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