TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

TENTATIVE

Low Power SDRAM and Nand E^{2}PROM Mixed Multi-Chip Package

DESCRIPTION

The TY9A0A111171KC40 is a mixed multi-chip package containing a 536,870,912-bit DDR Low Power Synchronous DRAM and a 1,107,296,256-bit Nand E²PROM. The TY9A0A111171KC40 is available in a 107-pin BGA package making it suitable for a variety of applications.

MCP Features

- Power supply voltage
  - Low power SDRAM : 1.7 to 1.9 V
  - Nand E²PROM : 1.70 to 1.95 V
- Operating temperature of –30° to 85°C
- Package
  - P-TFBGA107-0912-0.80CZ (Weight: 0.23 g)

DDR Low Power SDRAM Features

- Organization : 8M × 16 bits × 4 banks
- Power dissipation
  - Operating : 50 mA maximum
  - Burst operating: 90 mA maximum
  - Refresh : 100 mA maximum
  - Self refresh : 500 μA maximum
- Clock frequency: 166MHz (max.)
- 2KB page size
- Row address : A0 to A12
- Column address : A0 to A9
- Data Strobe
  - LDQS and UDQS
  - Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DQS
- Data Mask
  - LDM and UDM
  - DM masks write data-in at the both rising and falling edges of the data strobe
- PASR (Partial Array Self-Refresh)
- Auto TCSR (Temperature Compensated Self-Refresh)
- DS (Driver Strength)
- Differential clock inputs (CLK and $\overline{\text{CLK}}$)
- $\overline{\text{CAS}}$ Latency (CL): 3
- Burst Length
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- Precharge:
  - auto precharge option for each burst access
- Auto Refresh and Self Refresh mode
- Clock Stop mode
- Clock stop mode is a feature supported

Nand E^{2}PROM Features

- Organization
  - Memory cell array : 1056 × 64K × 16 bits
  - Register : 1056 × 16 bits
  - Page size : 1056 words
  - Block size : (64K + 2K) words
- Power dissipation
  - Read operating : 30 mA maximum
  - Program / Erase operating : 30 mA maximum
  - Standby : 50 μA maximum
- Access time :
  - Cell array register : 30 μs
  - Serial read cycle : 50 ns @CL=30pF
- Modes :
  - Read , Reset , Auto page program
  - Auto block erase , Status read
- Mode control
  - Serial input / output , Command control

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A		NC							DNU	DNU
B	DNU	NC	DQ0	V_{CCd}	V_{SS}	V_{CCn}	NC	A3	NC	DNU
C		V_{SS}	DQ2	DQ1	CLE	$\overline{CE}$	A0	A1	A2	
D		V_{CCQd}	DQ4	DQ3	ALE	$\overline{WEn}$	BA0	BA1	A10	
E		V_{SS}	DQ6	DQ5	$\overline{RE}$	RY/$\overline{BY}$	$\overline{RAS}$	NC	$\overline{CS}$	
F		V_{CCd}	LDQS	DQ7	$\overline{WP}$	NC	$\overline{CAS}$	$\overline{WEd}$	V_{SS}	
G		V_{SS}	LDM	$\overline{CLK}$	NC	NC	A12	CKE	V_{CCd}	
H		V_{CCd}	UDM	CLK	NC	NC	A8	A9	A11	
J		V_{SS}	UDQS	DQ8	I/O1	I/O3	I/O5	I/O7	A7	
K		V_{CCQd}	DQ9	DQ10	I/O9	I/O11	I/O13	I/O15	A6	
L		V_{SS}	DQ11	DQ12	I/O2	I/O4	I/O6	I/O8	A5	
M		V_{CCd}	DQ13	DQ14	I/O10	I/O12	I/O14	I/O16	A4	
N	DNU	NC	DQ15	V_{SS}	V_{SS}	V_{CCn}	V_{CCn}	V_{SS}	NC	DNU
P	DNU	DNU							DNU	DNU

PIN NAMES

A0 to A12	Address inputs for DDR Low Power SDRAM
BA0,BA1	Bank Select for DDR Low Power SDRAM
DQ0 to DQ15	Data inputs / outputs for DDR Low Power SDRAM
CLK, $\overline{CLK}$	Clock inputs for DDR Low Power SDRAM
CKE	Clock enable for DDR Low Power SDRAM
$\overline{CS}$	Chip select for DDR Low Power SDRAM
$\overline{RAS}$	Row address strobe for DDR Low Power SDRAM
$\overline{CAS}$	Column address strobe for DDR Low Power SDRAM
$\overline{WEd}$	Write enable for DDR Low Power SDRAM
UDM	Upper data mask enable for DDR Low Power SDRAM
LDM	Lower data mask enable for DDR Low Power SDRAM
UDQS	Upper data strobe for DDR Low Power SDRAM
LDQS	Upper data strobe for DDR Low Power SDRAM
I/O1 to I/O16	I/O port Nand E^2PROM
$\overline{CE}$	Chip enable for Nand E^2PROM
$\overline{RE}$	Read enable for Nand E^2PROM
$\overline{WEn}$	Write enable for Nand E^2PROM
CLE	Command latch enable for Nand E^2PROM
ALE	Address latch enable for Nand E^2PROM
$\overline{WP}$	Write protect for Nand E^2PROM
RY/$\overline{BY}$	Ready/Busy for Nand E^2PROM
V_{CCd}	Main power supply for Low Power SDRAM
V_{CCQd}	DQ power supply for Low Power SDRAM
V_{CCn}	Power supply for Nand E^2PROM
V_{SS}	Ground
NC	Not connected

PIN NAME CONVERSION TABLE

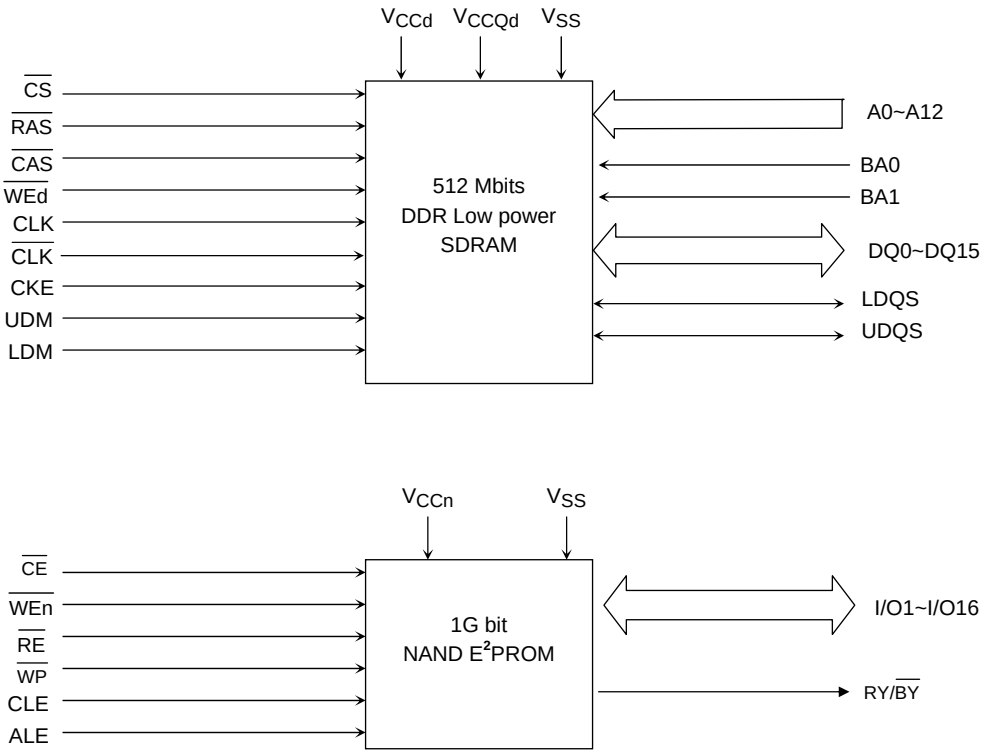
MCP Pin		512M	1G
Location	Name	LPSD	Nand
A1	–	–	–
A2	DNU	–	–
A3	–	–	–
A4	–	–	–
A5	–	–	–
A6	–	–	–
A7	–	–	–
A8	–	–	–
A9	DNU	–	–
A10	DNU	–	–
B1	DNU	–	–
B2	NC	–	–
B3	DQ0	DQ0	–
B4	VCCd	VDD	–
B5	VSS	VSS*	VSS
B6	VCCn	–	VCC
B7	NC	–	–
B8	A3	A3	–
B9	NC	–	–
B10	DNU	–	–
C1	–	–	–
C2	VSS	VSS*	VSS
C3	DQ2	DQ2	–
C4	DQ1	DQ1	–
C5	CLE	–	CLE
C6	$\overline{CE}$	–	$\overline{CE}$
C7	A0	A0	–
C8	A1	A1	–
C9	A2	A2	–
C10	–	–	–
D1	–	–	–
D2	VCCQd	VDDQ	–
D3	DQ4	DQ4	–
D4	DQ3	DQ3	–
D5	ALE	–	ALE
D6	$\overline{WEn}$	–	$\overline{WE}$
D7	BA0	BA0	–
D8	BA1	BA1	–
D9	A10	A10	–
D10	–	–	–
E1	–	–	–
E2	VSS	VSS*	VSS
E3	DQ6	DQ6	–
E4	DQ5	DQ5	–
E5	$\overline{RE}$	–	$\overline{RE}$
E6	$\overline{RY/BY}$	–	$\overline{RY/BY}$
E7	$\overline{RAS}$	$\overline{RAS}$	–
E8	NC	–	–
E9	$\overline{CS}$	$\overline{CS}$	–
E10	–	–	–

MCP Pin		512M	1G
Location	Name	LPSD	Nand
F1	–	–	–
F2	VCCQd	VDDQ	–
F3	LDQS	LDQS	–
F4	DQ7	DQ7	–
F5	$\overline{WP}$	–	$\overline{WP}$
F6	NC	–	–
F7	$\overline{CAS}$	$\overline{CAS}$	–
F8	$\overline{WEd}$	$\overline{WE}$	–
F9	VSS	VSS*	VSS
F10	–	–	–
G1	–	–	–
G2	VSS	VSS*	VSS
G3	LDM	LDM	–
G4	$\overline{CLK}$	$\overline{CK}$	–
G5	NC	–	–
G6	NC	–	–
G7	A12	A12	–
G8	CKE	CKE	–
G9	VCCd	VDD	–
G10	–	–	–
H1	–	–	–
H2	VCCd	VDD	–
H3	UDM	UDM	–
H4	CLK	CK	–
H5	NC	–	–
H6	NC	–	–
H7	A8	A8	–
H8	A9	A9	–
H9	A11	A11	–
H10	–	–	–
J1	–	–	–
J2	VSS	VSS*	VSS
J3	UDQS	UDQS	–
J4	DQ8	DQ8	–
J5	I/O1	–	I/O1
J6	I/O3	–	I/O3
J7	I/O5	–	I/O5
J8	I/O7	–	I/O7
J9	A7	A7	–
J10	–	–	–
K1	–	–	–
K2	VCCQd	VDDQ	–
K3	DQ9	DQ9	–
K4	DQ10	DQ10	–
K5	I/O9	–	I/O9
K6	I/O11	–	I/O11
K7	I/O13	–	I/O13
K8	I/O15	–	I/O15
K9	A6	A6	–
K10	–	–	–

MCP Pin		512M	1G
Location	Name	LPSD	Nand
L1	–	–	–
L2	VSS	VSS*	VSS
L3	DQ11	DQ11	–
L4	DQ12	DQ12	–
L5	I/O2	–	I/O2
L6	I/O4	–	I/O4
L7	I/O6	–	I/O6
L8	I/O8	–	I/O8
L9	A5	A5	–
L10	–	–	–
M1	–	–	–
M2	VCCd	VDD	–
M3	DQ13	DQ13	–
M4	DQ14	DQ14	–
M5	I/O10	–	I/O10
M6	I/O12	–	I/O12
M7	I/O14	–	I/O14
M8	I/O16	–	I/O16
M9	A4	A4	–
M10	–	–	–
N1	DNU	–	–
N2	NC	–	–
N3	DQ15	DQ15	–
N4	VSS	VSS*	VSS
N5	VSS	VSS*	VSS
N6	VCCn	–	VCC
N7	VCCn	–	VCC
N8	VSS	VSS*	VSS
N9	NC	–	–
N10	DNU	–	–
P1	DNU	–	–
P2	DNU	–	–
P3	–	–	–
P4	–	–	–
P5	–	–	–
P6	–	–	–
P7	–	–	–
P8	–	–	–
P9	DNU	–	–
P10	DNU	–	–

VSS* : VSS / VSSQ

BLOCK DIAGRAM



Electrical Specifications (LPSDRAM)

All voltages are referenced to V_{SS} (GND).
After power up, wait more than 200 μs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RANGE	UNIT
V_{CCd}	LPSDRAM V_{CCd} Supply Voltage		−0.5~2.3	V
V_{CCQd}	LPSDRAM V_{CCQd} Supply Voltage (DQ)		−0.5~2.3	V
V_{CCn}	Nand E^2PROM V_{CCn} Supply Voltage		−0.5~2.5	V
V_{IN}	Input Voltage	LPSDRAM	−0.5~2.3	V
		Nand E^2PROM	−0.5~2.5	V
V_{DQ}	Input/Output Voltage	LPSDRAM	−0.5~ 2.3	V
		Nand E^2PROM	−0.5~V_{CCn} + 0.3 (≤ 2.5)	V
T_{opr}	Operating Temperature		−30~85	°C
P_D	Power Dissipation		1	W
T_{solder}	Soldering Temperature		260	°C
I_{OSHORT}	Output Short Circuit Current(1)		50	mA
T_{stg}	Storage Temperature		−55~125	°C

Note : (1) Output shorted for no more than one second. No more than one output shorted at a time

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Ta = –30°~85°C) see note 4

SYMBOL		PARAMETER		MIN	TYP.	MAX	UNIT
V_{CCd} (1)		LPSDRAM V_{CCd} Supply Voltage		1.7	1.8	1.9	V
V_{CCQd} (1)		LPSDRAM V_{CCQd} Supply Voltage (DQ)		1.7	1.8	1.9	
V_{CCn}		Nand E^2PROM V_{CCn} Supply Voltage		1.7	1.8	1.95	
LPSDRAM	V_{IH}	Input High Level Voltage		0.8 × V_{CCQd}	—	V_{CCQd} + 0.3	
	V_{IL}	Input Low Level Voltage		–0.3	—	0.2 × V_{CCQd}	
	$V_{IN(DC)}$	$\frac{CLK}{\overline{CLK}}$	DC Input Voltage Level	–0.3	—	V_{CCQd} + 0.3	
	V_{IX} (3)		AC Input Differential cross point Voltage	0.4 × V_{CCQd}	0.5 × V_{CCQd}	0.6 × V_{CCQd}	
	$V_{ID(DC)}$ (2)		DC Input Differential Voltage	0.4 × V_{CCQd}	—	V_{CCQd} + 0.6	
	$V_{ID(AC)}$ (2)		AC Input Differential Voltage	0.6 × V_{CCQd}	—	V_{CCQd} + 0.6	
	$V_{IHD(DC)}$	DQ DQM DQS	DC Input High Voltage	0.7 × V_{CCQd}	—	V_{CCQd} + 0.3	
	$V_{ILD(DC)}$		DC Input Low Voltage	–0.3	—	0.3 × V_{CCQd}	
	$V_{IHD(AC)}$		AC Input High Voltage	0.8 × V_{CCQd}	—	V_{CCQd} + 0.3	
	$V_{ILD(AC)}$		AC Input Low Voltage	–0.3	—	0.2 × V_{CCQd}	
Nand E^2PROM	V_{IH}	Input High Level Voltage		0.78 × V_{CCn}	—	V_{CCn} + 0.3	
	V_{IL}	Input Low Level Voltage		–0.3 (5)	—	0.22 × V_{CCn}	

Note: (1) V_{CCQd} must be equal to V_{CCd}.

(2) $V_{ID(DC)}$ and $V_{ID(AC)}$ are the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.

(3) The value of VIX is expected to be 0.5 × V_{CCQd} and must track variations in the DC level of the same.

(4) All voltage referred to VSS must be same potential.

(5) –2.0 V for pulse width ≤ 20 ns

CAPACITANCE (LPSDRAM / Nand E^2PROM) (Ta = 25°C)

SYMBOL	PARAMETER		CONDITION	MIN	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	LPSDRAM	f = 100 MHz, V_{OUT} = V_{CCQd}/2, ΔV_{OUT} = 0.2 V	—	—	5.5	pF
		Nand E^2PROM	f = 1 MHz , V_{IN} = 0 V	—	—	10	pF
C_{OUT}	Output Capacitance	LPSDRAM	f = 100 MHz, V_{OUT} = V_{CCQd}/2, ΔV_{OUT} = 0.2 V DOUT circuit disabled	—	—	6.5	pF
		Nand E^2PROM	f = 1 MHz, V_{OUT} = GND	—	—	10	pF

Note: These parameters are sampled periodically and are not tested for every device.

DC CHARACTERISTICS - 1

(Ta = –30°~85°C, V_{CCd}/V_{CCQd} = 1.70V~1.90V, V_{CCn} = 1.70V~1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CC1sd}	DDR LPSDRAM Operating current(1)	Burst length=2 , tRC ≥ tRC min, I_{OUT} = 0 mA , One bank active	—	50	mA
I_{CC2Psd}	DDR LPSDRAM Standby current in power down	CKE ≤ V_{IL} max, tCK = tCK min	—	0.3	mA
$I_{CC2PSsd}$	DDR LPSDRAM Standby current in power down (Input signal stable)	CKE ≤ V_{IL} max, tCK = ∞	—	0.3	mA
I_{CC2Nsd}	DDR LPSDRAM Standby current in non power down	CKE ≥ V_{IH} min, tCK = tCK min, $\overline{CS}$ ≥ V_{IH} min Input signals are changed one time during 2tCK.	—	12	mA
$I_{CC2NSsd}$	DDR LPSDRAM Standby current in non power down (Input signal stable)	CKE ≥ V_{IH} min, tCK = ∞ , Input signals are stable	—	8	mA
I_{CC3Psd}	DDR LPSDRAM Active standby Current in power down	CKE ≤ V_{IL} max, tCK = tCK min	—	5	mA
$I_{CC3PSsd}$	DDR LPSDRAM Active standby Current in power down (Input signal stable)	CKE ≤ V_{IL} max, tCK = ∞	—	3	mA
I_{CC3Nsd}	DDR LPSDRAM Active standby Current in non power down	CKE ≥ V_{IH} min , tCK = tCK min, $\overline{CS}$ ≥ V_{IH} min Input signals are changed one time during 2tCK.	—	15	mA
$I_{CC3NSsd}$	DDR LPSDRAM Active standby Current in non power down (Input signal stable)	CKE ≥ V_{IH} min , tCK = ∞ , Input signals are stable	—	10	mA
I_{CC4sd}	DDR LPSDRAM Burst operating current (1)	Burst length=4, tCK ≥ tCK min, I_{OUT} = 0 mA All banks active	—	90	mA
I_{CC5sd}	DDR LPSDRAM Refresh current	tRFC ≥ tRFC min	—	100	mA
I_{CC7sd}	DDR LPSDRAM Standby current in deep power down mode (Reserved)	CKE ≤ 0.2V	—	10	μA

SYMBOL	PARAMETER	CONDITION		TYP	MAX	UNIT
I_{CC6sd}	DDR LPSDRAM Self refresh current (4)	CKE ≤ 0.2V	PASR="000" (Full)	—	500	μA
			PASR="001" (2BK)	—	400	
			PASR="010" (1BK)	—	300	
		Ta ≤ +40°C CKE ≤ 0.2V	PASR="000" (Full)	—	250	
			PASR="001" (2BK)	—	220	
			PASR="010" (1BK)	—	200	

DC CHARACTERISTICS - 2

(Ta = −30°~85°C, V_{CCd} / V_{CCQd} = 1.70V~1.90V, V_{CCn} = 1.70V~1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CCO1n}	Nand E^{2}PROM Serial Read current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA , t_{cycle} = 50 ns	—	30	mA
I_{CCO2n}	Nand E^{2}PROM Programming current	—	—	30	mA
I_{CCO3n}	Nand E^{2}PROM Erasing current	—	—	30	mA
I_{CCS1n}	Nand E^{2}PROM Standby current	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0 V or V_{CCn}	—	1	mA
I_{CCS2n}	Nand E^{2}PROM Standby current	$\overline{CE}$ = V_{CCn} − 0.2 V, $\overline{WP}$ = 0 V or V_{CCn}	—	50	μA
I_{IL}	Input leakage current	V_{IN} = 0 V~V_{CCn} (V_{CCQd})	—	±10	μA
I_{OHsd}	LPSDRAM Output high current	V_{OH} = V_{CCQd} − 0.2 V	−0.1	—	mA
I_{OLsd}	LPSDRAM Output low current	V_{OL} = 0.2 V	0.1	—	mA
I_{OHn}	Nand E^{2}PROM Output high current	V_{OH} = V_{CCn} − 0.2 V	−0.1	—	mA
I_{OLn}	Nand E^{2}PROM Output low current	V_{OL} = 0.2 V	0.1	—	mA
I_{OLn} ($\overline{RY/BY}$)	Nand E^{2}PROM Output Current of $\overline{RY/BY}$ pin	V_{OL} = 0.2 V	4(5)	—	mA
I_{LO}	Output leakage current	V_{OUT} = 0 V~ V_{CCn}(V_{CCQd}), I/O disable	—	±10	μA

Note :

(1) I_{CC} specifications are tested after the device is properly initialized

(2) Input slew rate is 1V/ns

(3) Definitions for I_{CC} :

LOW is defined as VIN ≤ 0.1 x V_{CCQd}

HIGH is defined as VIN ≥ 0.9 x V_{CCQd}

STABLE is defined as inputs stable at a HIGH or LOW level

SWITCHING is defined as

- address and command: inputs changing between HIGH and LOW once per two clock cycles
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle

DM and DQS are STABLE

(4) With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.

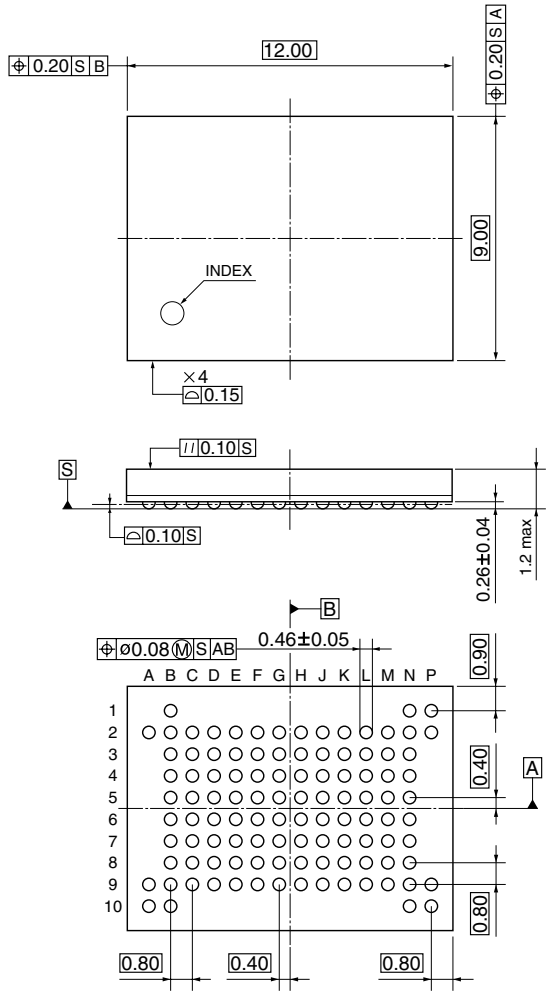
(5) Typical

See page DDRH-1 to page DDRH-47 for the specification of DDR Low Power SDRAM.

See page N-1 to page N-32 for the specification of Nand E^{2}PROM.

PACKAGE DIMENSION

P-TFBGA107-0912-0.80CZ Unit: mm



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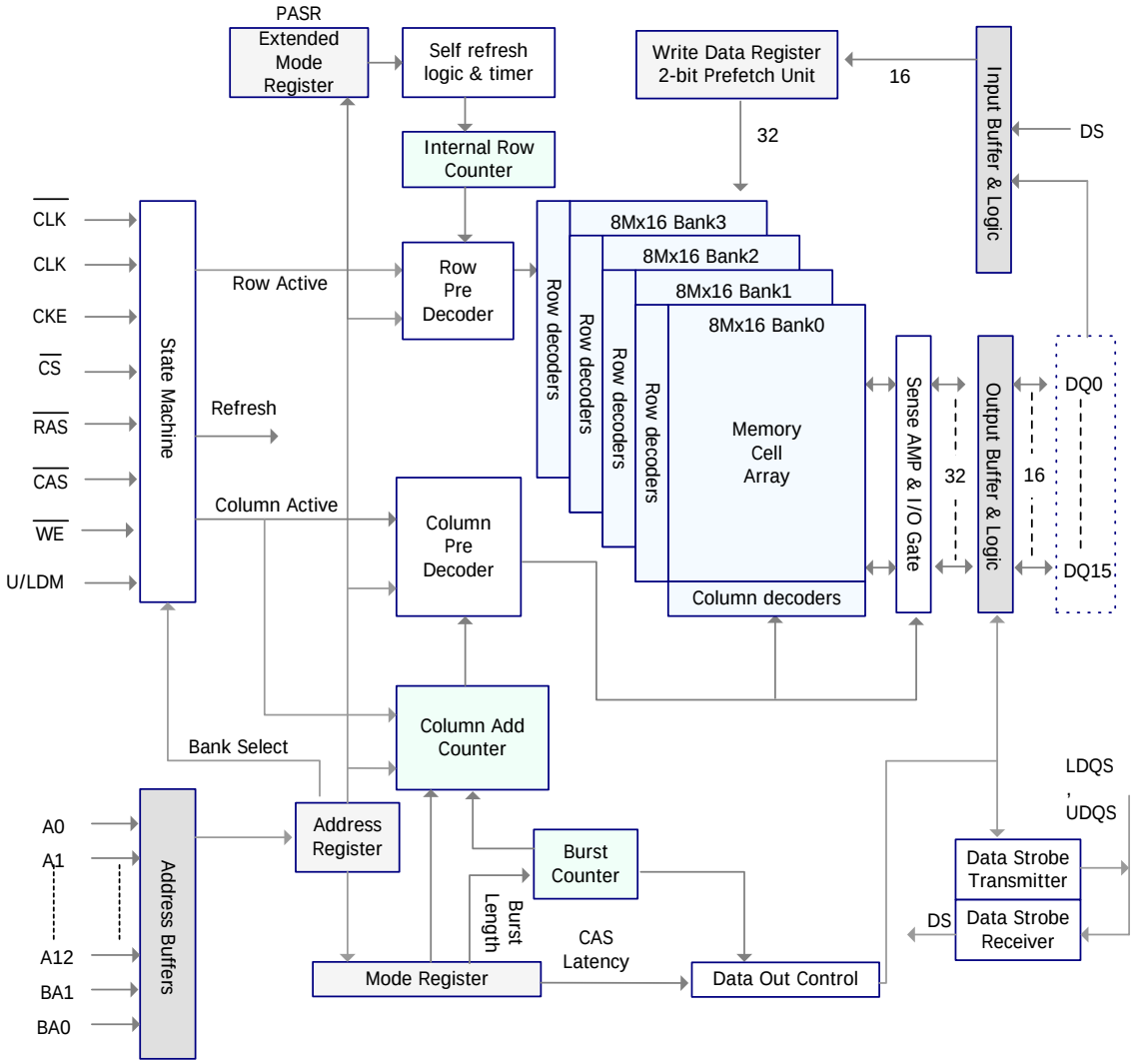
512 Mbits DDR LPSDRAM 166MHz

Organization : 8M words × 16 bits × 4 banks

Functional Block Diagram



Register Definition 1

Mode Register Set(MRS)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Length		

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

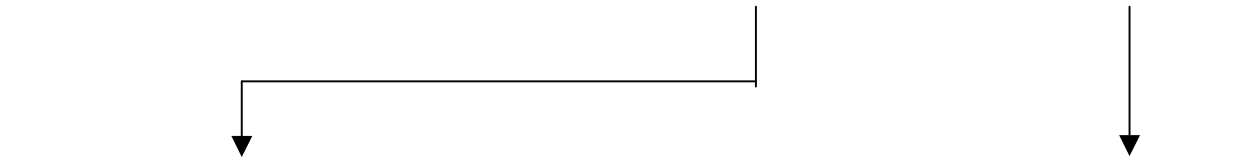
Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Register Definition 2

Extended Mode Register Set(EMRS)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS		0	0	PASR		



DS (Driver Strength)

A6	A5	Driver Strength
0	0	Full
0	1	Half (Default)
1	0	Quarter
1	1	Octant

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks (Default)
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One Eighth of Total Bank (BA1=BA0= Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1=BA0= Row Address 2 MSBs=0)
1	1	1	Reserved

Command Truth Table

Function	/CS	/RAS	/CAS	/WE	BA	A10/AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Autoprecharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Autoprecharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN (Reserved)	L	H	H	L	X	X	X	4,5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all Banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op Code		10

DM Truth Table

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:

1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with auto precharge disabled. This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among MRS, EMRS and SRR.
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH.

CKE Truth Table

CKE*n-1*	CKE*n*	Current State	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down (Reserved)	X	Maintain Deep Power Down (Reserved)	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,10
L	H	Deep Power Down (Reserved)	NOP or DESELECT	Exit Deep Power Down (Reserved)	5,8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down (Reserved)	
H	H	See the other Truth Tables			

Note:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LP DDR immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least one time during the t_{XP} period.
10. The clock must toggle at least once during the t_{XSR} time.

Current State BANK*n* Truth Table (COMMAND to BANK *n*)

Current State	Command					Action	Note
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start write burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto recharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
   Precharging: Starts with the registration of a PRECHARGE command and ends when t_{RP} is met.
   Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met.
   Once t_{RCD} is met, the bank will be in the "row active" state.
   Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met.
   Once t_{RFC} is met, the LP DDR will be in an "all banks idle" state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
   Once t_{MRD} is met, the LP DDR will be in an "all banks idle" state.
   Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when t_{RP} is met.
   Once t_{RP} is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

Current State BANK*n* Truth Table (COMMAND to BANK *m*)

Current State	Command					Action	Note
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Pre-charging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

AC Characteristics 1 (AC operating conditions unless otherwise noted)

Parameter		Symbol	min.	max.	Unit	Note
DQ Output Access Time from (CK,/CK)		tAC	2.0	6.0	ns	
DQS Output Access Time from (CK,/CK)		tDQSCK	2.0	6.0	ns	
Clock High-level Width		tCH	0.45	0.55	tCK	
Clock Low-level Width		tCL	0.45	0.55	tCK	
Clock Half Period		tHP	tCL, tCH (Min)	—	ns	1,2
System Clock Cycle Time	CL=3	tCK3	6.0	—	ns	3
	CL=2	tCK2	12	—	ns	
DQ and DM Input Setup Time		tDS	0.6	—	ns	4,5,6
DQ and DM Input Hold Time		tDH	0.6	—	ns	4,5,6
DQ and DM Input Pulse Width		tDIPW	1.6	—	ns	7
Address and Control Input Setup Time		tIS	1.1	—	ns	6,8,9
Address and Control Input Hold Time		tIH	1.1	—	ns	6,8,9
Address and Control Input Pulse Width		tIPW	2.2	—	ns	7
DQ & DQS Low-impedance time from CK,/CK		tLZ	1.0	—	ns	10
DQ & DQS High-impedance time from CK,/CK		tHZ	—	5.0	ns	10
DQS - DQ Skew		tDQSQ	—	0.5	ns	11
DQ / DQS output hold time from DQS		tQH	tHP - tQHS	—	ns	2
Data Hold Skew Factor		tQHS	—	0.65	ns	2
Write Command to 1st DQS Latching Transition		tDQSS	0.75	1.25	tCK	
DQS Input High-Level Width		tDQSH	0.4	—	tCK	
DQS Input Low-Level Width		tDQSL	0.4	—	tCK	
DQS Falling Edge of CK Setup Time		tDSS	0.2	—	tCK	
DQS Falling Edge Hold Time from CK		tDSH	0.2	—	tCK	
MODE REGISTER SET Command Period		tMRD	2	—	tCK	
MRS to Read Command Period		tSRR	2	—	tCK	
Minimum Time between Status Register Read to Next Valid Command		tSRC	CL+1	—	tCK	
Write Preamble Setup Time		tWPRES	1.0	—	ns	12
Write Postamble		tWPST	0.4	0.6	tCK	13
Write Preamble		tWPRE	0.25	—	tCK	
Read Preamble	CL=3	tRPRE	0.9	1.1	tCK	14
	CL=2	tRPRE	0.5	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	tCK	
ACTIVE to PRECHARGE Command Period		tRAS	42	70,000	ns	
ACTIVE to ACTIVE Command Period		tRC	60	—	ns	
AUTO REFRESH to ACTIVE/AUTO REFRESH Command Period		tRFC	72	—	ns	
ACTIVE to READ or WRITE Delay		tRCD	18	—	ns	15
PRECHARGE Command Period		tRP	18	—	ns	15
ACTIVE Bank A to ACTIVE Bank B Delay		tRRD	12	—	ns	
WRITE Recovery Time		tWR	15	—	ns	
Auto Precharge Write Recovery + Precharge Time		tDAL	(tWR/tCK) + (tRP/tCK)			15
Internal Write to Read Command Delay		tWTR	1	—	tCK	

AC Characteristics 2 (AC operating conditions unless otherwise noted)

Parameter	Symbol	min.	max.	Unit	Note
Self Refresh Exit to next valid Command Delay	tXSR	120	—	ns	
Exit Power Down to next valid Command Delay	tXP	tIS + 1CLK	—	ns	
CKE min. Pulse Width (High and Low)	tCKE	1	—	tCK	
Average Periodic Refresh Interval	tREFI	7.8	—	µs	
Refresh Period	tREF	—	64	ms	

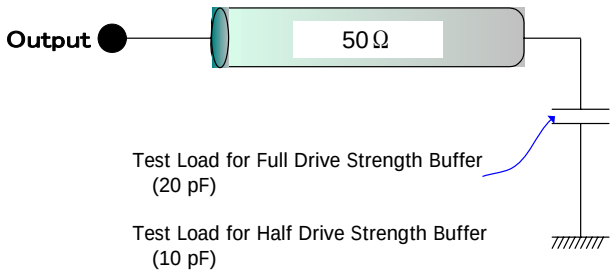
Note:

1. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)
2. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for
   1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
4. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.
5. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
6. Input slew rate ≥ 1.0 V/ns.
7. These parameters guarantee device timing but they are not necessarily tested on each device.
8. The transition time for address and command inputs is measured between VIH and VIL.
9. A CK/CK differential slew rate of 2.0 V/ns is assumed for this parameter.
10. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
11. tDQSQ consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
15. Speed bin (CL-tRCD-tRP) = 3-3-3
16. tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms above, if not already an integer, round to the next higher integer.
17. A maximum of eight Refresh commands can be posted to any given Low Power DDR SDRAM (DDR LPSDRAM), meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*tREFI.
18. All AC parameters are guaranteed by full range of operating voltage and temperature.
    VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30°C ~ +85°C.

AC Operating Test Conditions

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.8*VDDQ/0.2*VDDQ	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note: 1. The circuit shown on the right represents the timing load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design and characterization. Use of IBIS or other simulation tools for system design validation is suggested.



DDR LPSDRAM Output Slew rate Characteristics

Parameter	Min.	Max.	Unit	Note
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1,2
Output Slew Rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

Note:

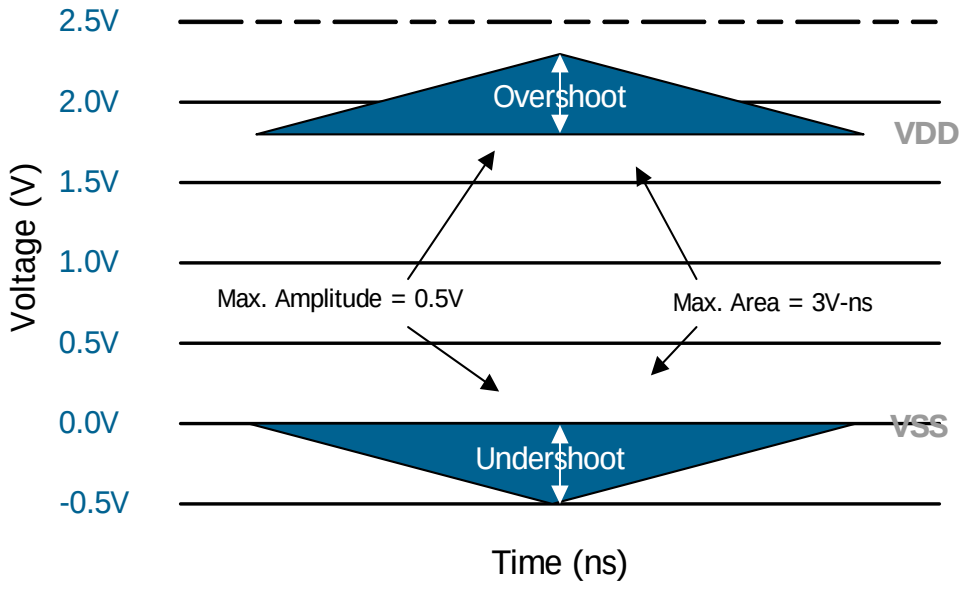
1. Measured with a test load of 20pF connected to VSSQ
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC)
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

DDR LPSDRAM AC OVERSHOOT / UNDERSHOOT SPECIFICATION

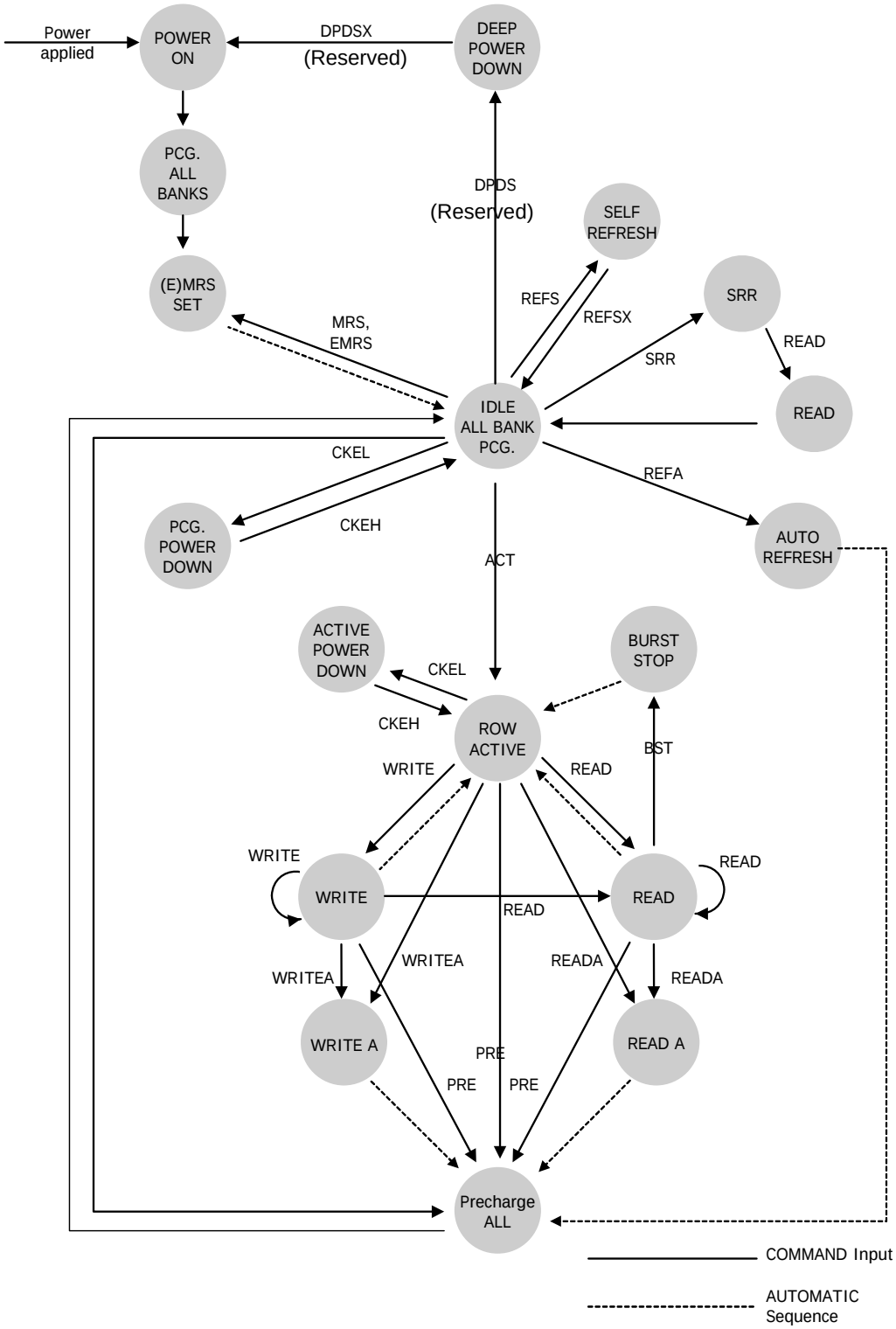
Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.5 V
Maximum peak amplitude allowed for undershoot	0.5 V
The area between overshoot signal and VDD must be less than or equal to	3V -ns
The area between undershoot signal and GND must be less than or equal to	3V -ns

Note:

1. This specification is intended for devices with no clamp protection and is guaranteed by design.



State Diagram



ACT :
Active

BST :
Burst

CKEL :
Enter Power-Down

CKEH :
Exit Power-Down

DPDS :
Enter Deep Power-Down (Reserved)

DPDSX :
Exit Deep Power-Down (Reserved)

EMRS :
Ext. Mode Reg. set

MRS :
Mode Register set

PRE :
Precharge

PREALL :
Precharge All Banks

REFA :
Auto Refresh

REFS :
Enter Self Refresh

REFSX :
Exit Self Refresh

READ :
READ w/o Auto Precharge

READA :
READ with Auto Precharge

WRITE :
WRITE w/o Auto Precharge

WRITEA :
WRITE with Auto Precharge

SRR :
Status Register Read

DESELECT

The DESELECT function (CS = High) prevents new commands from being executed by the DDR LPSDRAM. The DDR LPSDRAM is effectively deselected. Operations already in progress are not affected.

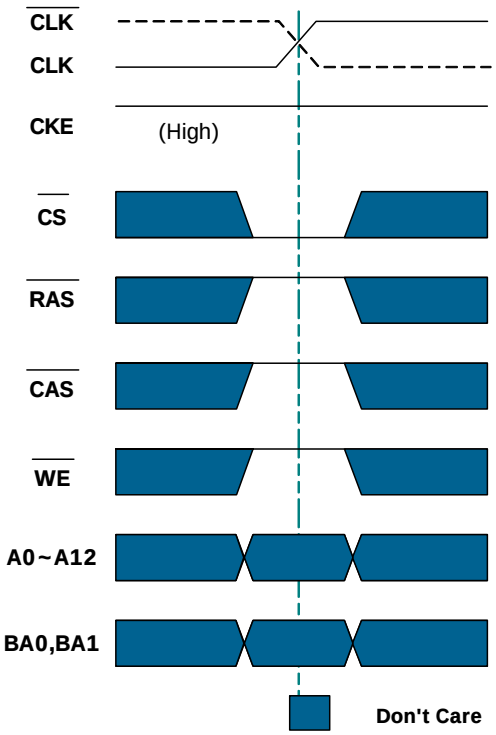
NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a DDR LPSDRAM that is selected (CS = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

ACTIVE

The Active command is used to activate a row in a particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A12 (or the highest address bit) selects the row. (see to next figure)

Before any READ or WRITE commands can be issued to a bank within the DDR LPSDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.
The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.
A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.

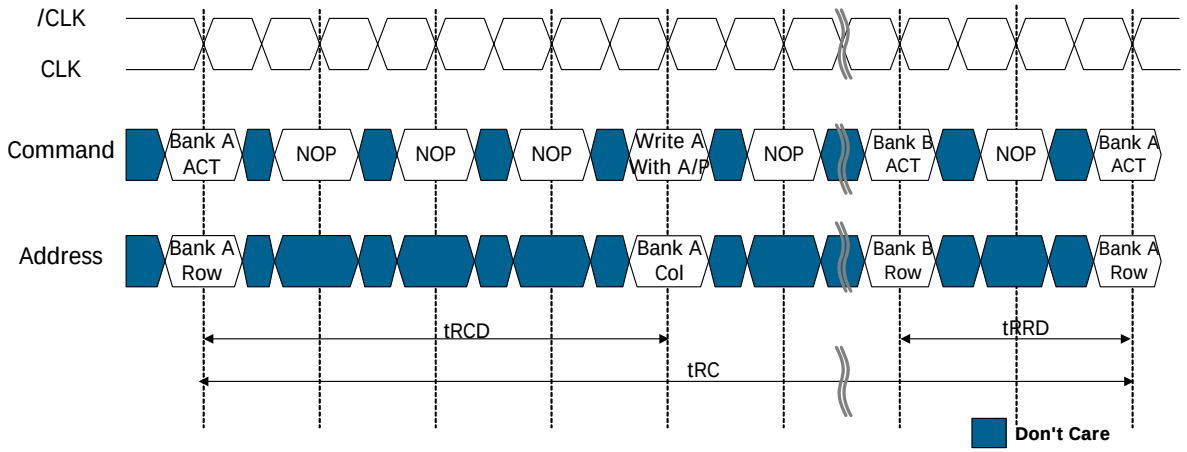


NOP Command

ACTIVE Command

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

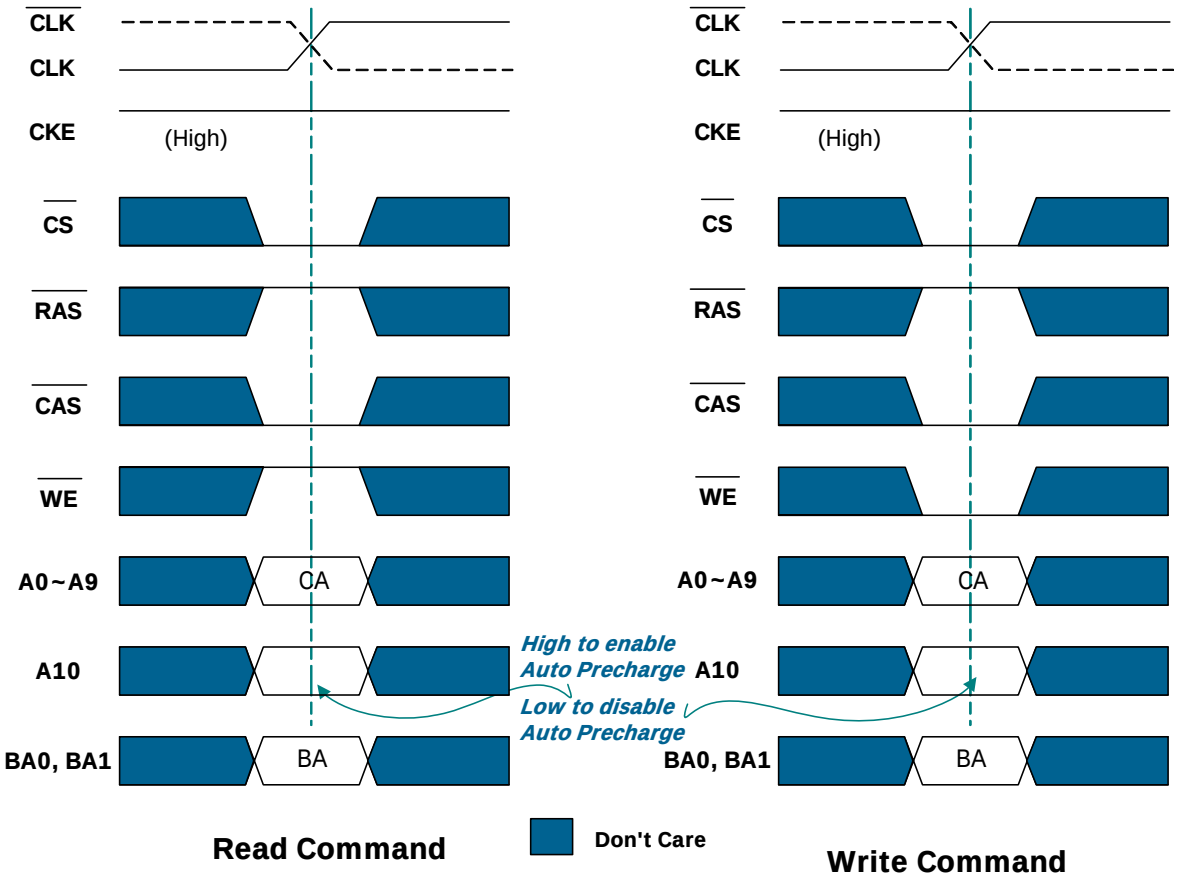
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.



READ / WRITE COMMAND

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued.
The DDR LPSDRAM drives the DQS during read operations. The initial low state of the DQS is known as the read preamble and the last data-out element is coincident with the read postamble. DQS is edge-aligned with read data. Upon completion of a burst, assuming no new READ commands have been initiated, the I/O's will go high-Z.

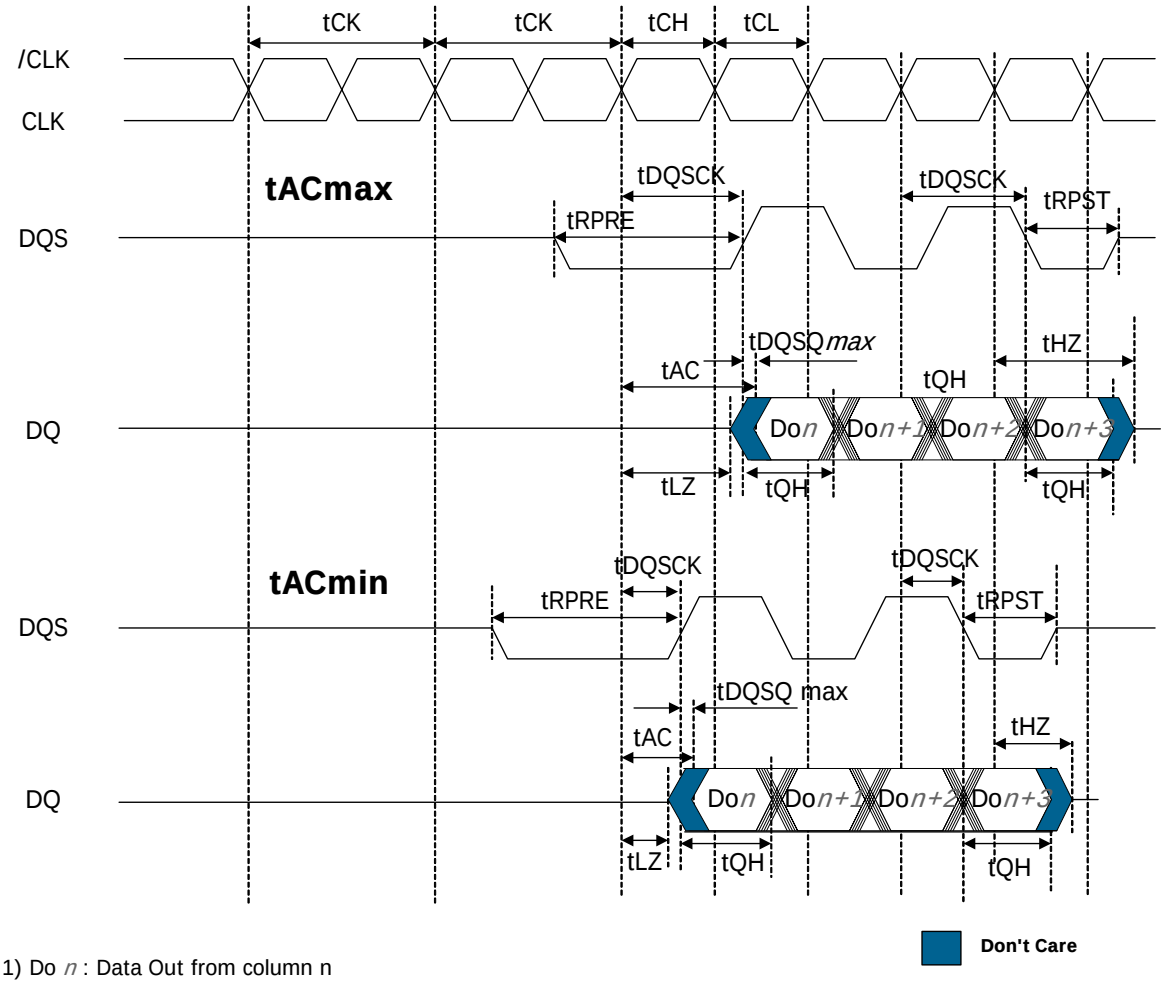
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used.If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access. Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to the memory; if the DM signal is registered high, the corresponding data-inputs will be ignored, and a write will not be executed to that byte/column location. The memory controller drives the DQS during write operations. The initial low state of the DQS is known as the write preamble and the low state following the last data-in element is write postamble. Upon completion of a burst, assuming no new commands have been initiated, the I/O's will stay high-Z and any additional input data will be ignored.



READ / WRITE COMMAND

READ

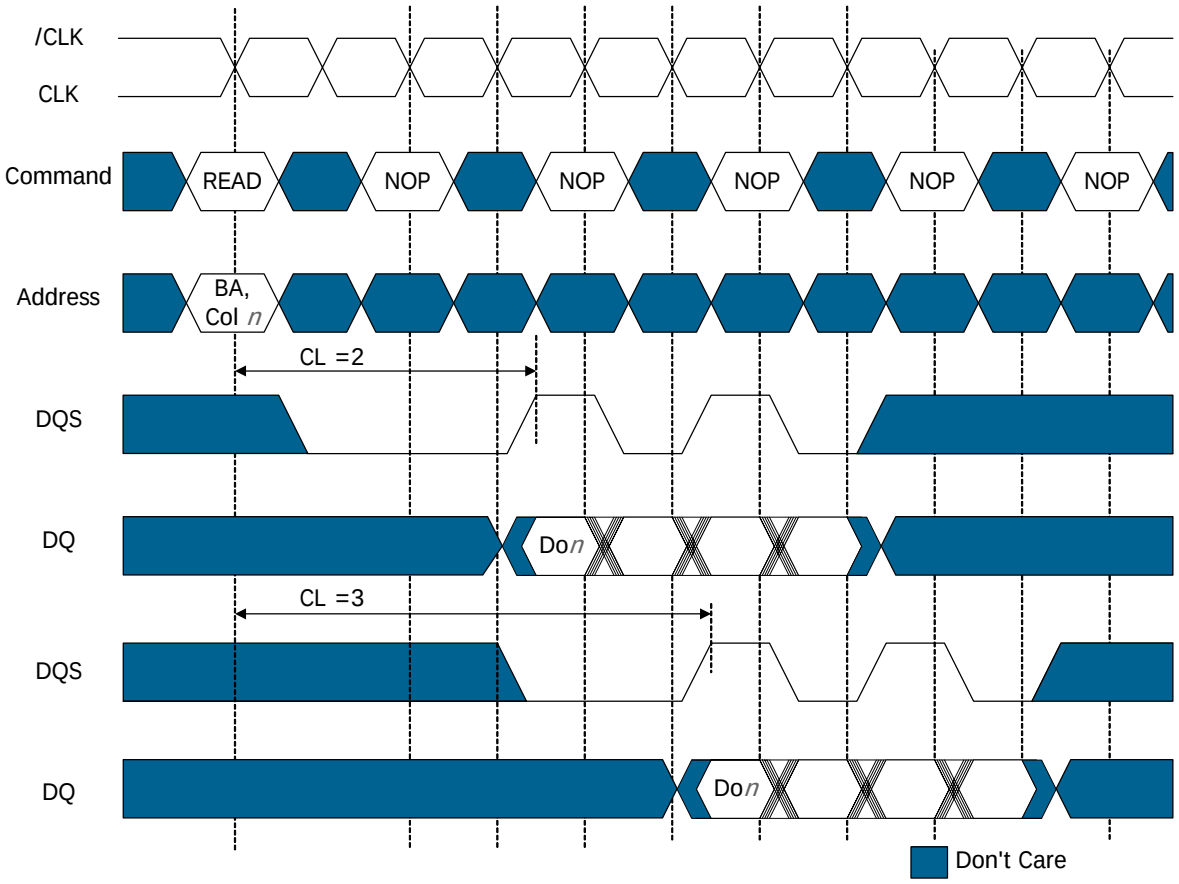
The basic Read timing parameters for DQ are shown next figure (Basic Read Timing Parameters). They apply to all Read operations. During Read bursts, DQS is driven by the DDR LPSDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble.



1) Do *n* : Data Out from column n
2) All DQ are vaild tAC after the CK edge
   All DQ are vaild tDQSQ after the DQS edge, regardless of tAC

Basic Read Timing Parameters

The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in next figure with a CAS latency of 2 and 3. Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

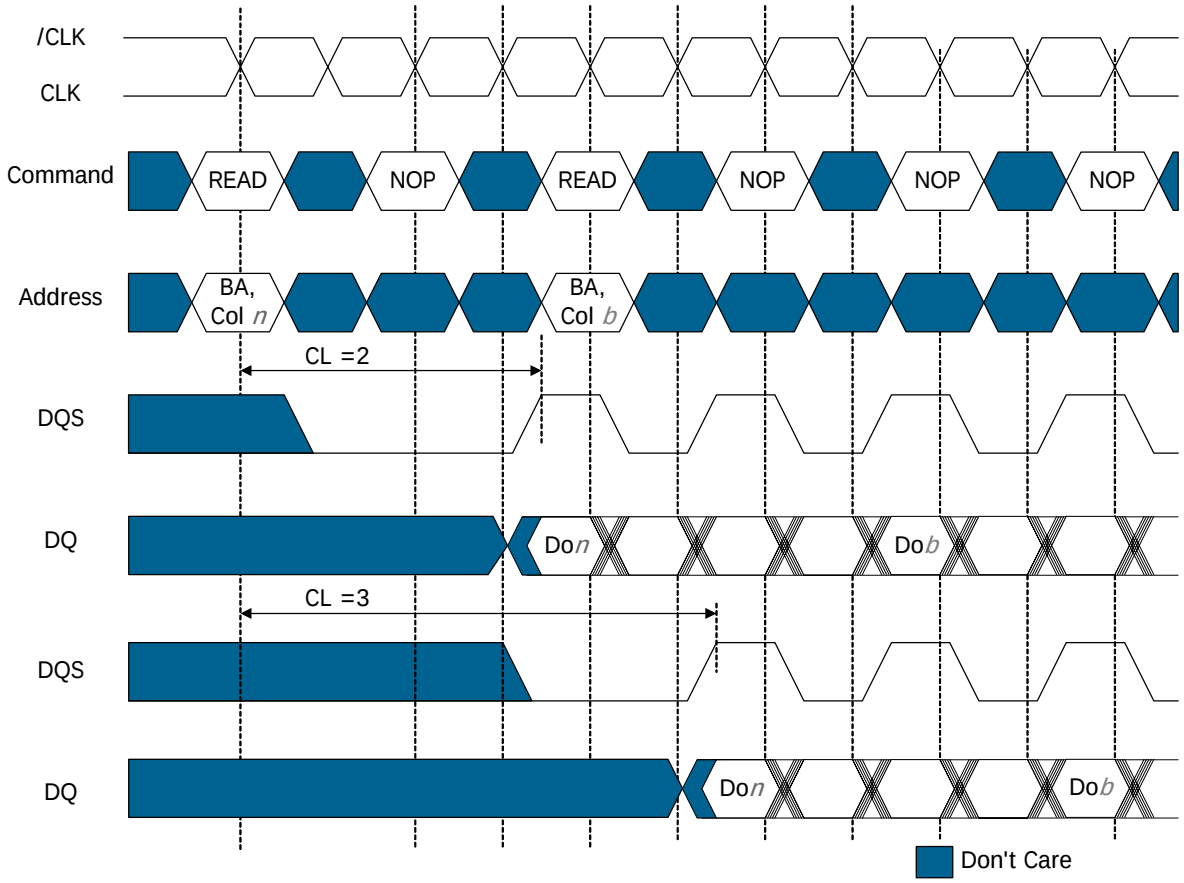


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 4; 3 subseqnent elements of Data Out appear in the programmed order following Do *n*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Read Burst Showing CAS Latency

READ to READ

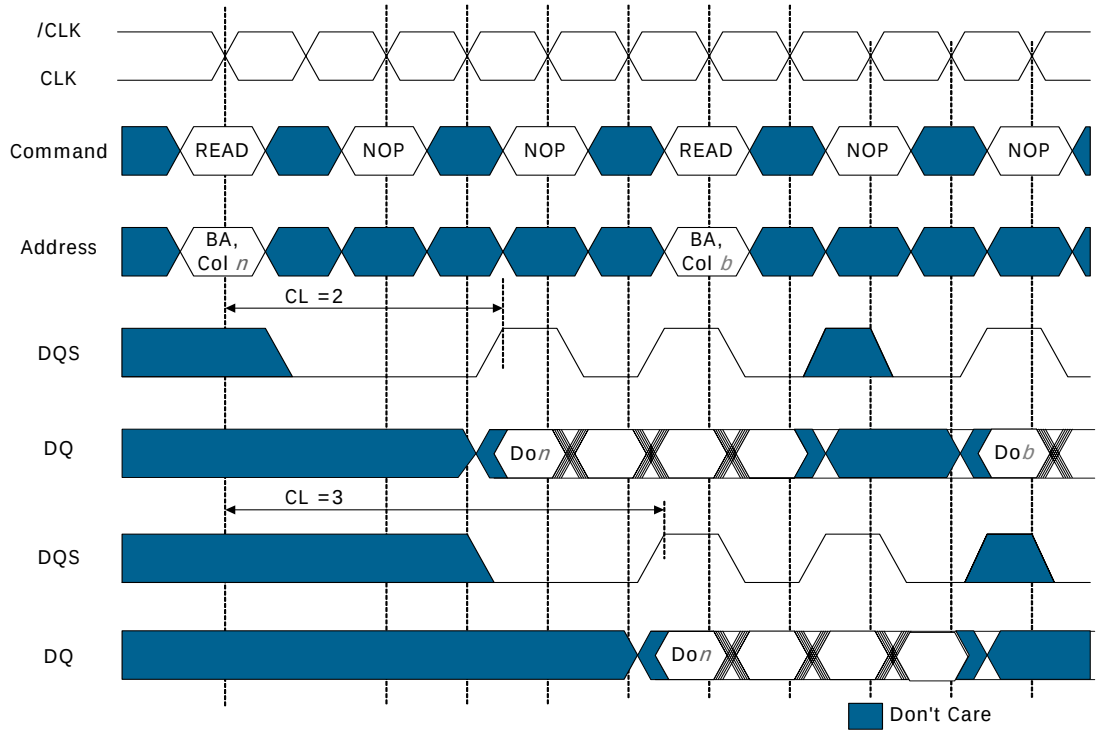
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
4) Read bursts are to an active row in any bank
5) Shown with nominal tAC, tDQSCK and tDQSQ

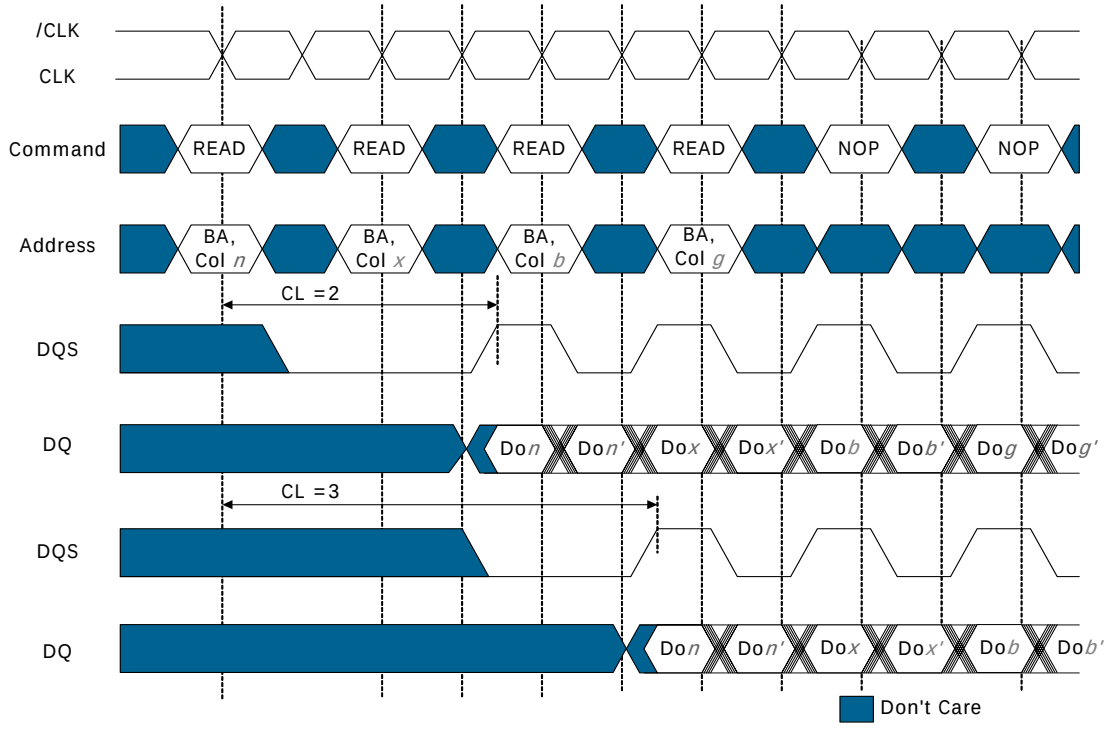
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command.
Non-consecutive Reads are shown in the first figure of next page. Random read accesses within a page or pages can be performed as shown in second figure of next page.



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following Do *n (b)*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Non-Consecutive Read Bursts

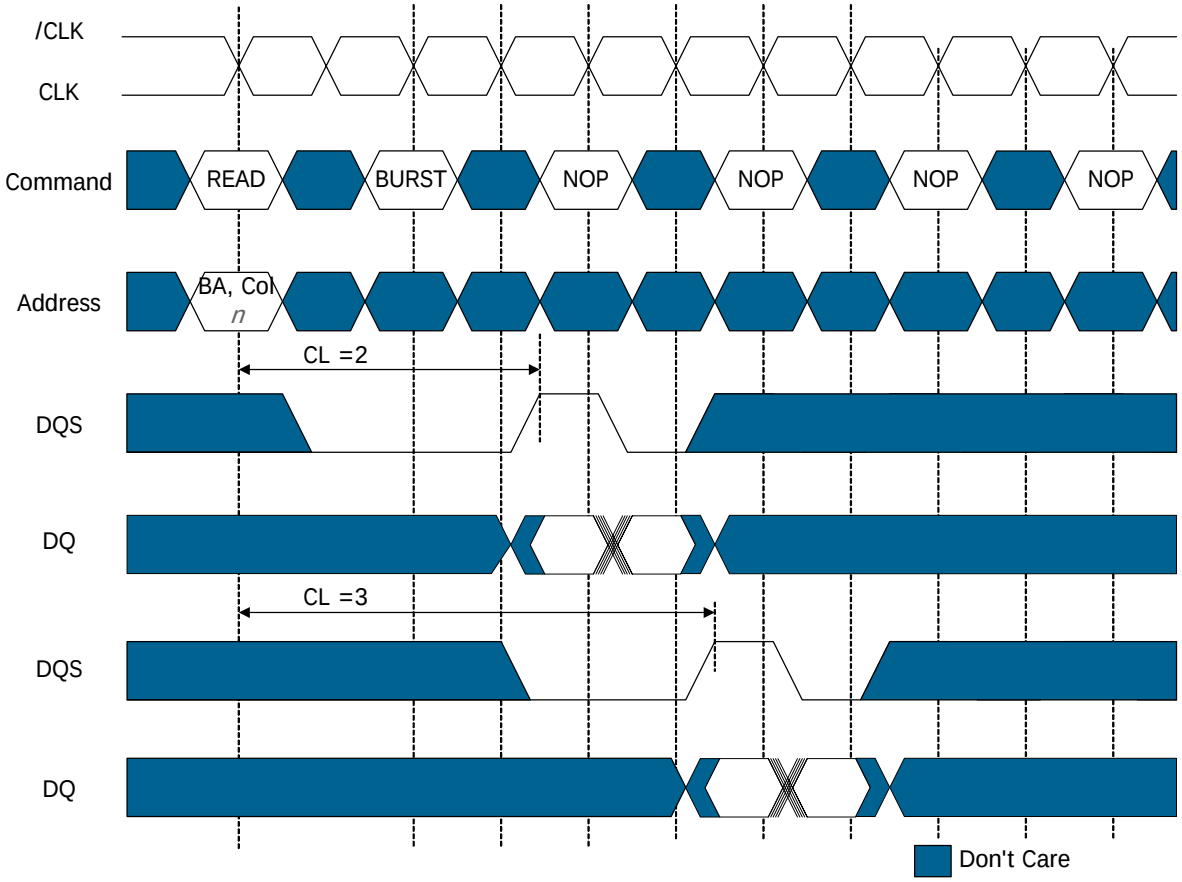


1) Do*n,* etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 2, 4 or 8 in cases shown (if burst of 4 or 8, the burst is interrupted)
4) Read are to active rows in any banks

Random Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

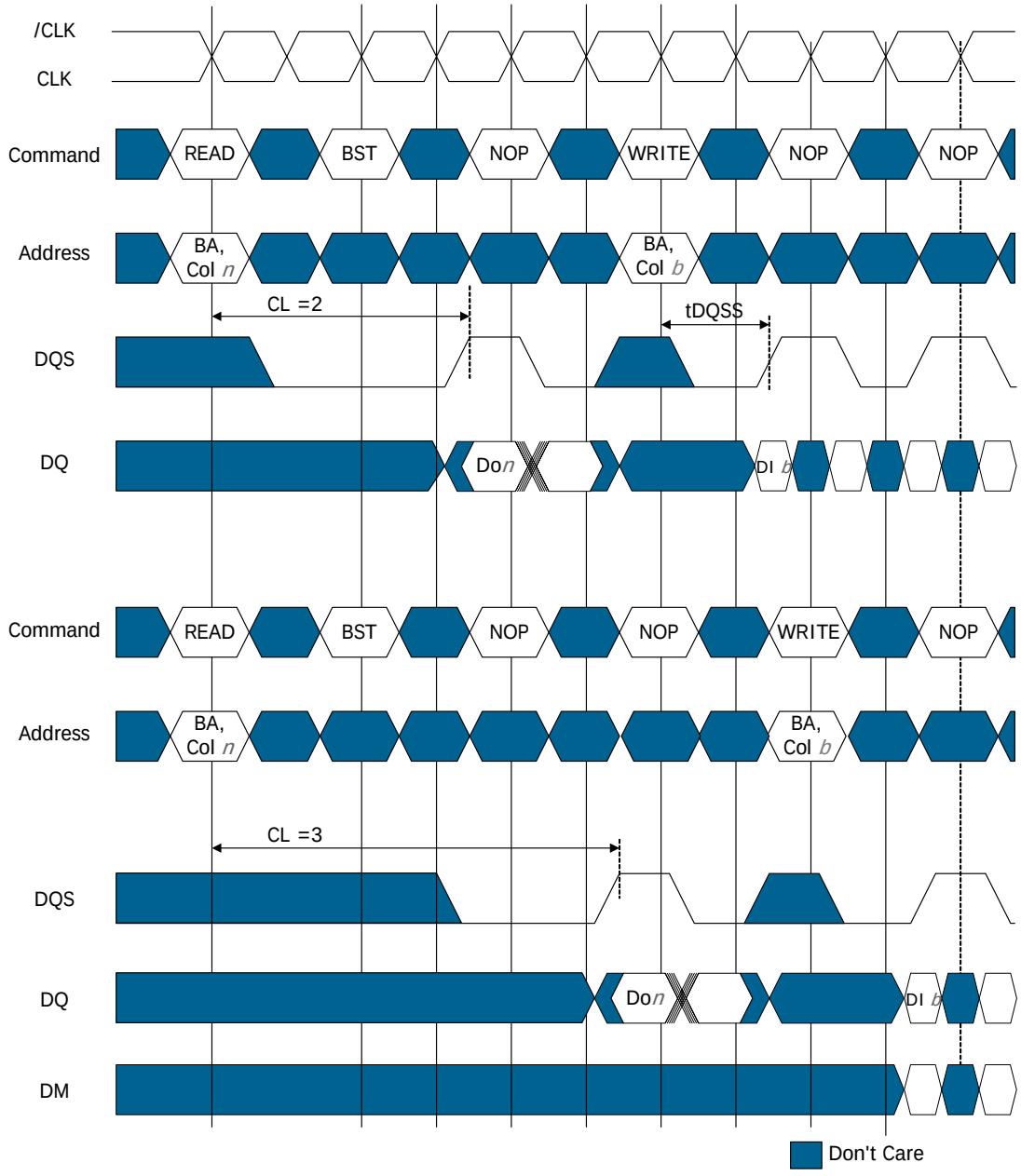


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Cases shown are bursts of 4 or 8 terminated after 2 data elements
4) Shown with nominal tAC, tDQSCK and tDQSQ

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig. for the case of nominal tDQSS.

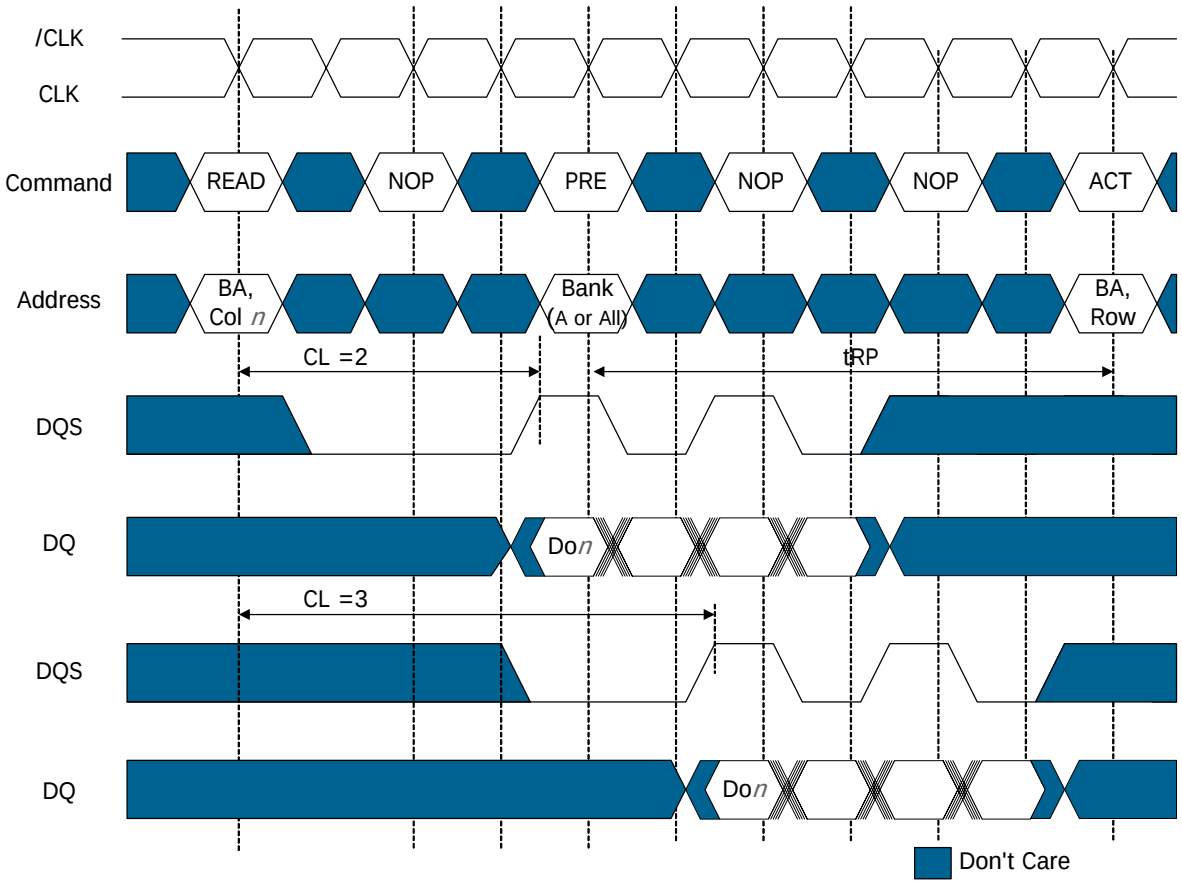


1) DO *n* = Data Out from column n; DI b = Data In to column b
2) Burst length = 4 or 8 in the cases shown; if the burst length is 2, the BST command can be ommitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

Read to Write

READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.
Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled.
The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

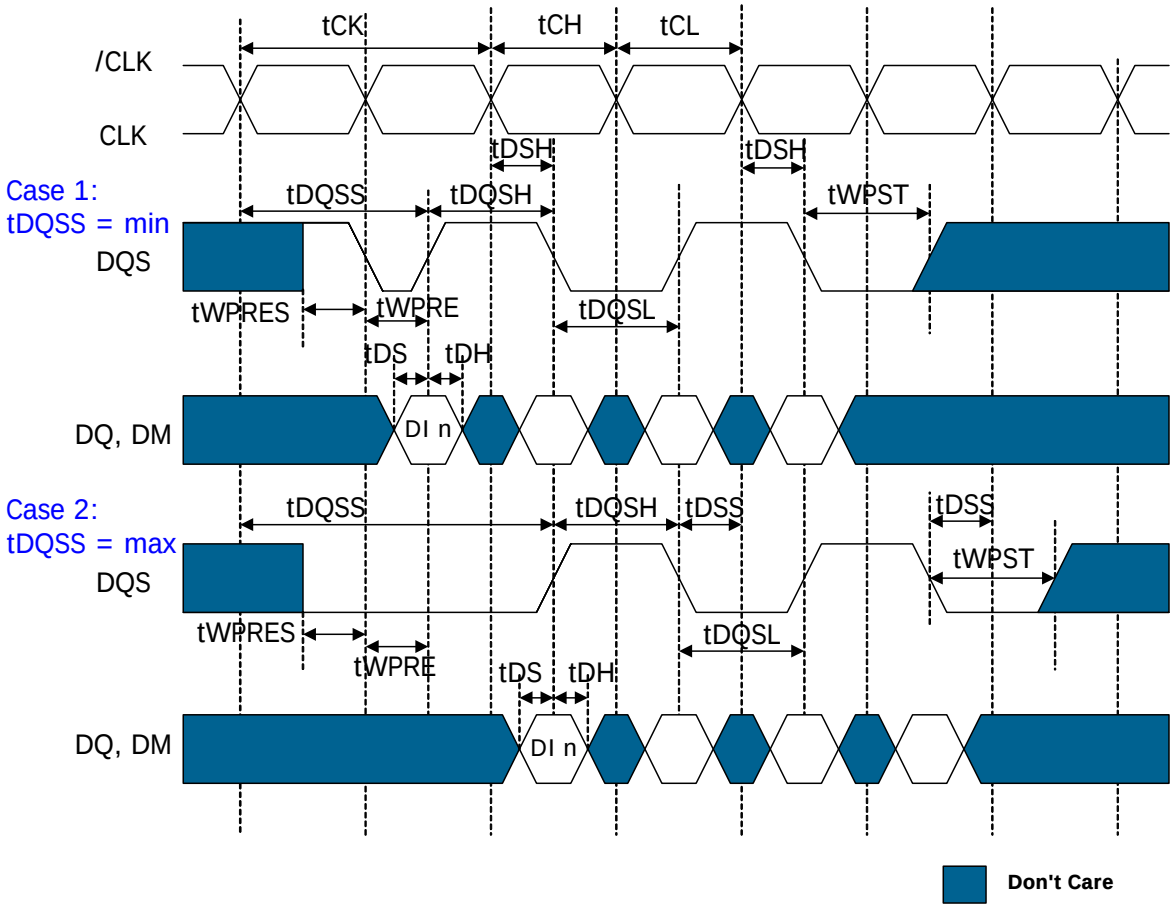


1) DO *n* = Data Out from column n
2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8
3) Shown with nominal tAC, tDQSCK and tDQSQ
4) Precharge may be applied at (BL / 2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

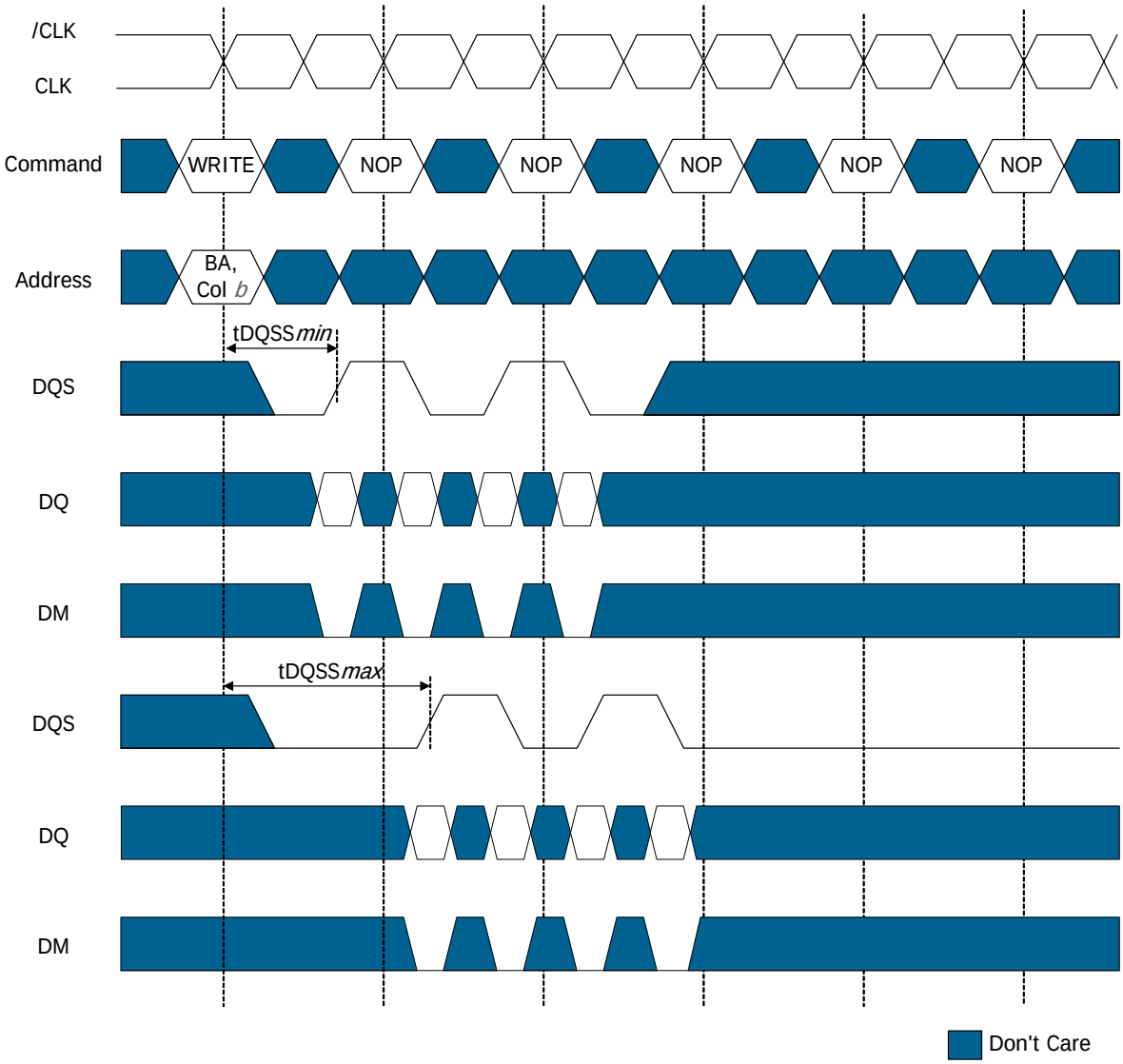
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
Basic Write timing parameters for DQ are shown in Figure; they apply to all Write operations.



1) DI n: Data in for column n
2) 3 subsequent elements of Data in are applied in the programmed order following DI n
3) tDQSS : each rising edge of DQS must fall within the +/-25 (percentage) window of the corresponding positive clock edge

Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.
The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Next fig. shows the two extremes of tDQSS for a burst of 4.
Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain high-Z and any additional input data will be ignored.

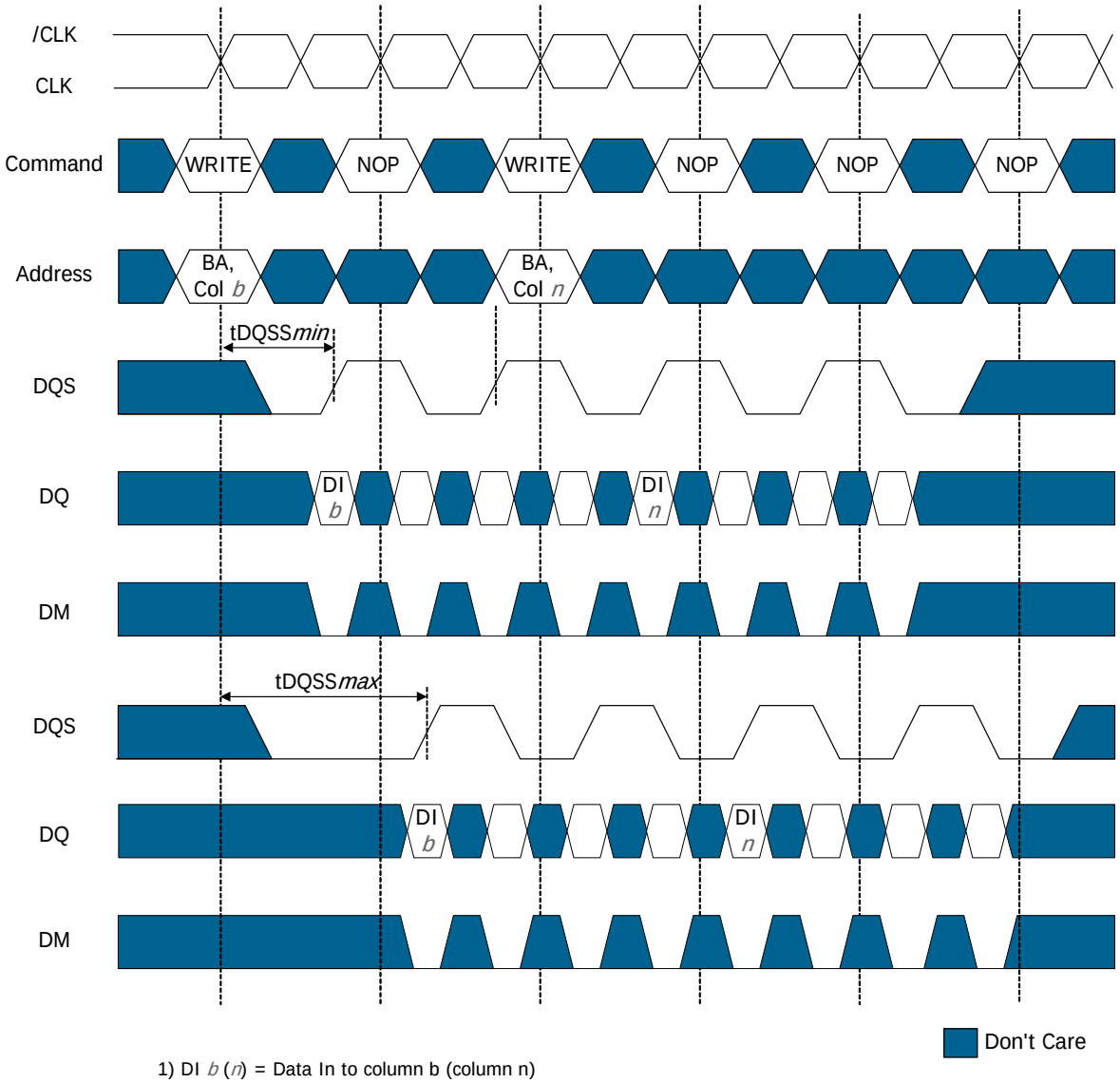


1) DI b = Data In to column b
2) 3 subsequent elements of Data In are applied in the programmed order following DI b
3) A non-interrupted burst of 4 is shown
4) A10 is low with the WRITE command (Auto Precharge is disabled)

Write Burst (min. and max. tDQSS)

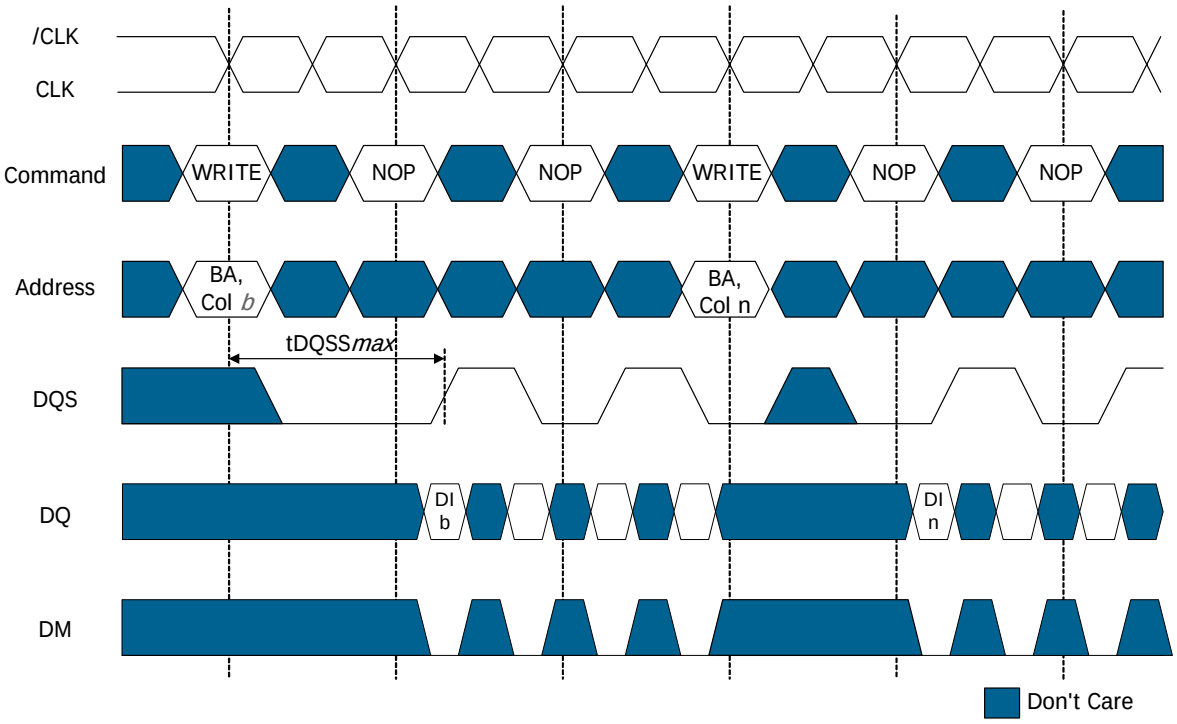
WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command. The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.



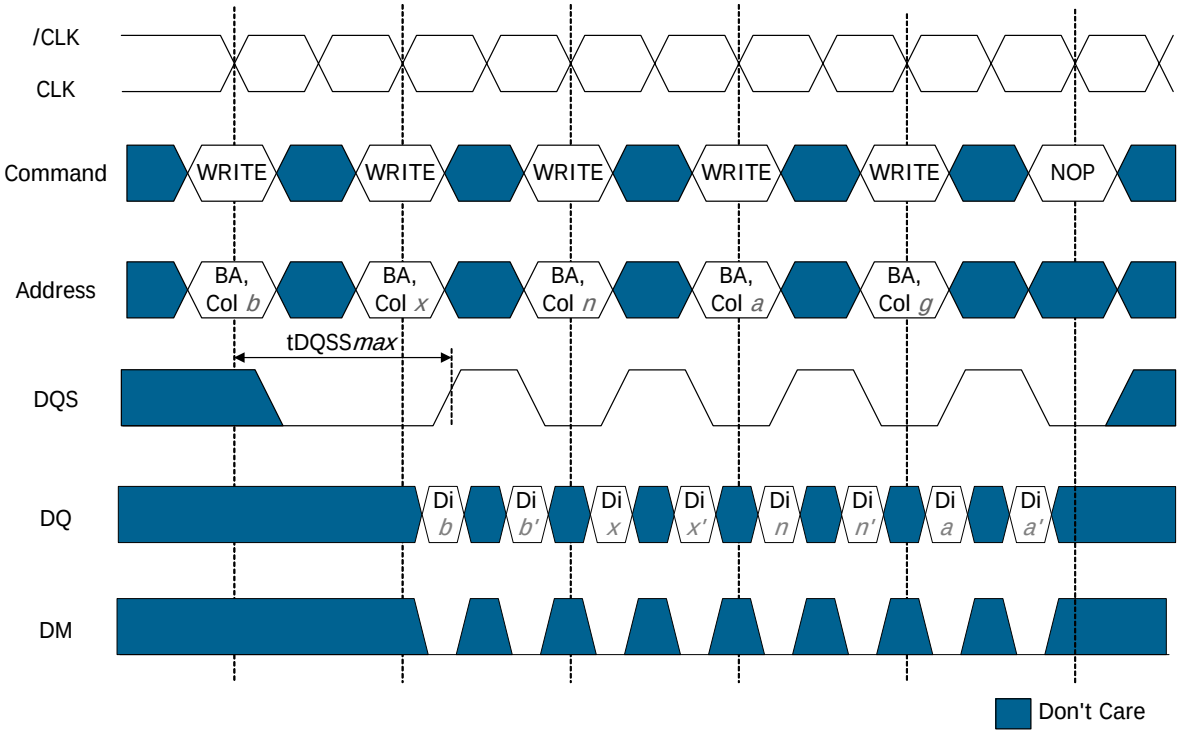
1) DI *b* (*n*) = Data In to column b (column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
   3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

Concatenated Write Bursts



1) DI *b* (*n*) = Data In to column b (or column n).
2) 3 subsequent elements of Data In are applied in the programmed order following DI *b*.
   3 subsequent elements of Data In are applied in the programmed order following DI *n*.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

Non-Concatenated Write Bursts

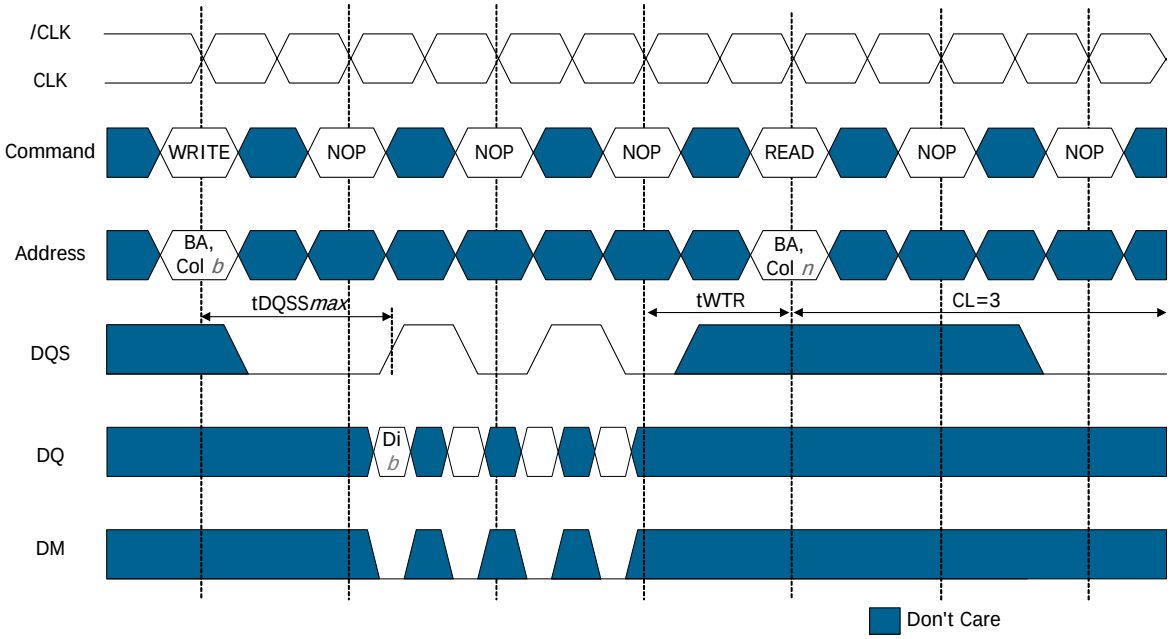


1) DI b etc. = Data In to column b, etc.
   ; b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4 or 8 in cases shown. If burst of 4 or 8, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

Random Write Cycles

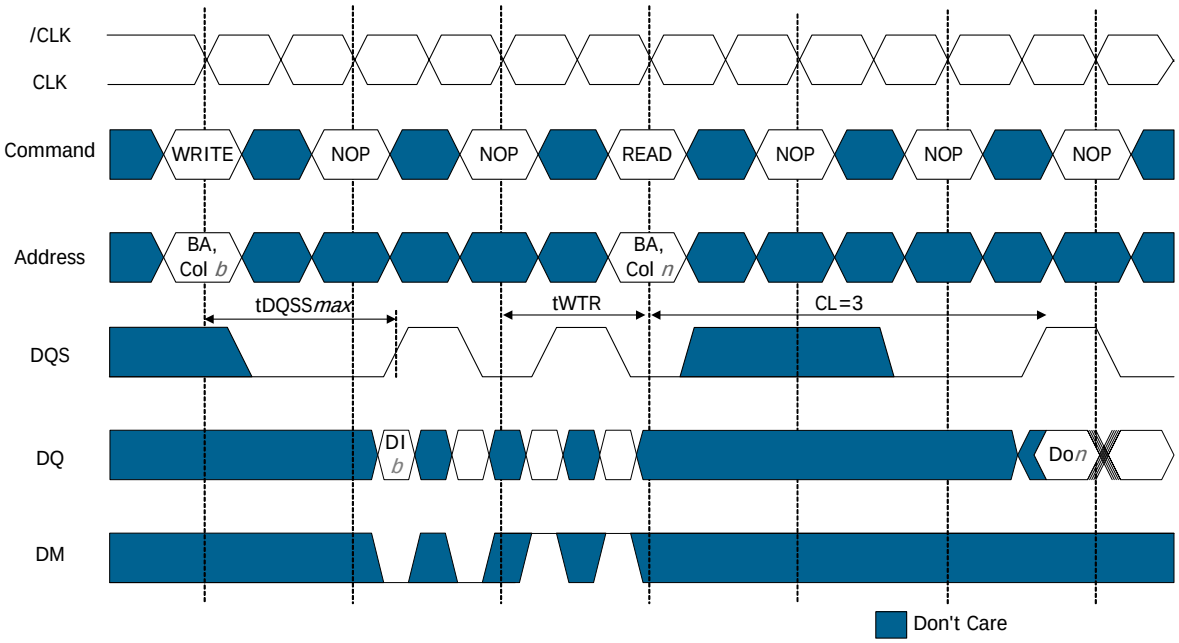
WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Figure.



1) DI *b* = Data In to column b . 3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

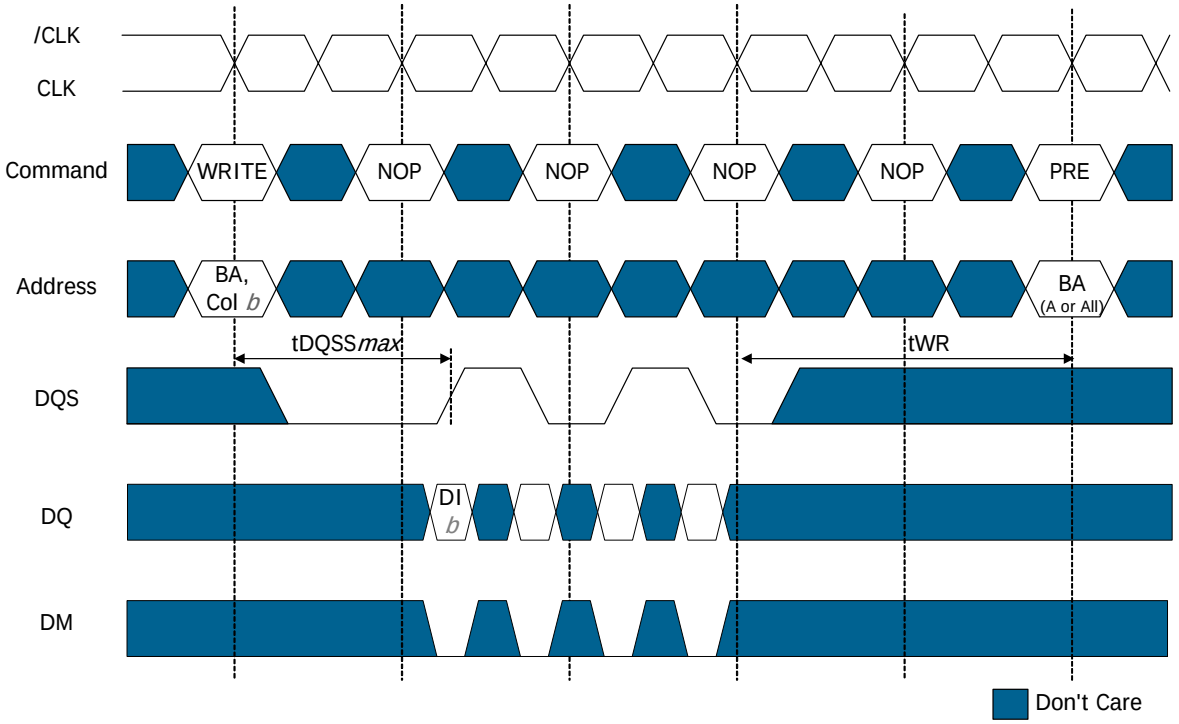


1) DI *b* = Data In to column b. DO *n* = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Interrupting Write to Read

WRITE to PRECHARGE

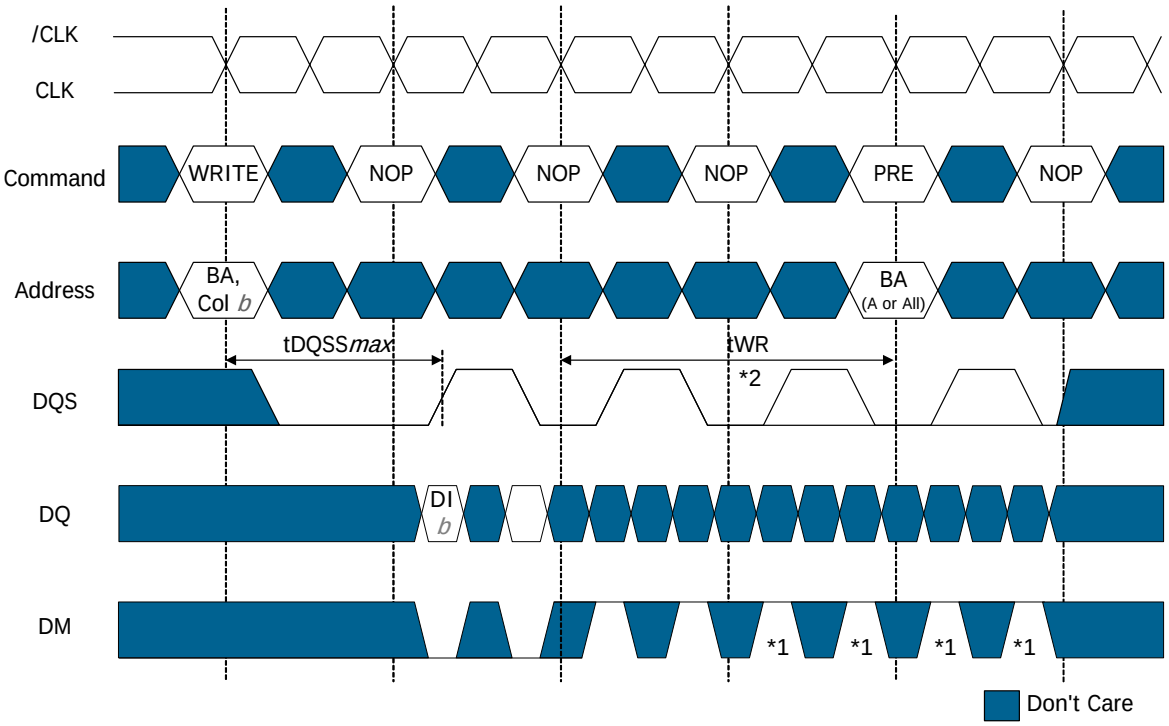
Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in Fig.



1) DI b (n) = Data In to column b (column n)
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted bursts of 4 are shown.
3) tWR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Non-Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

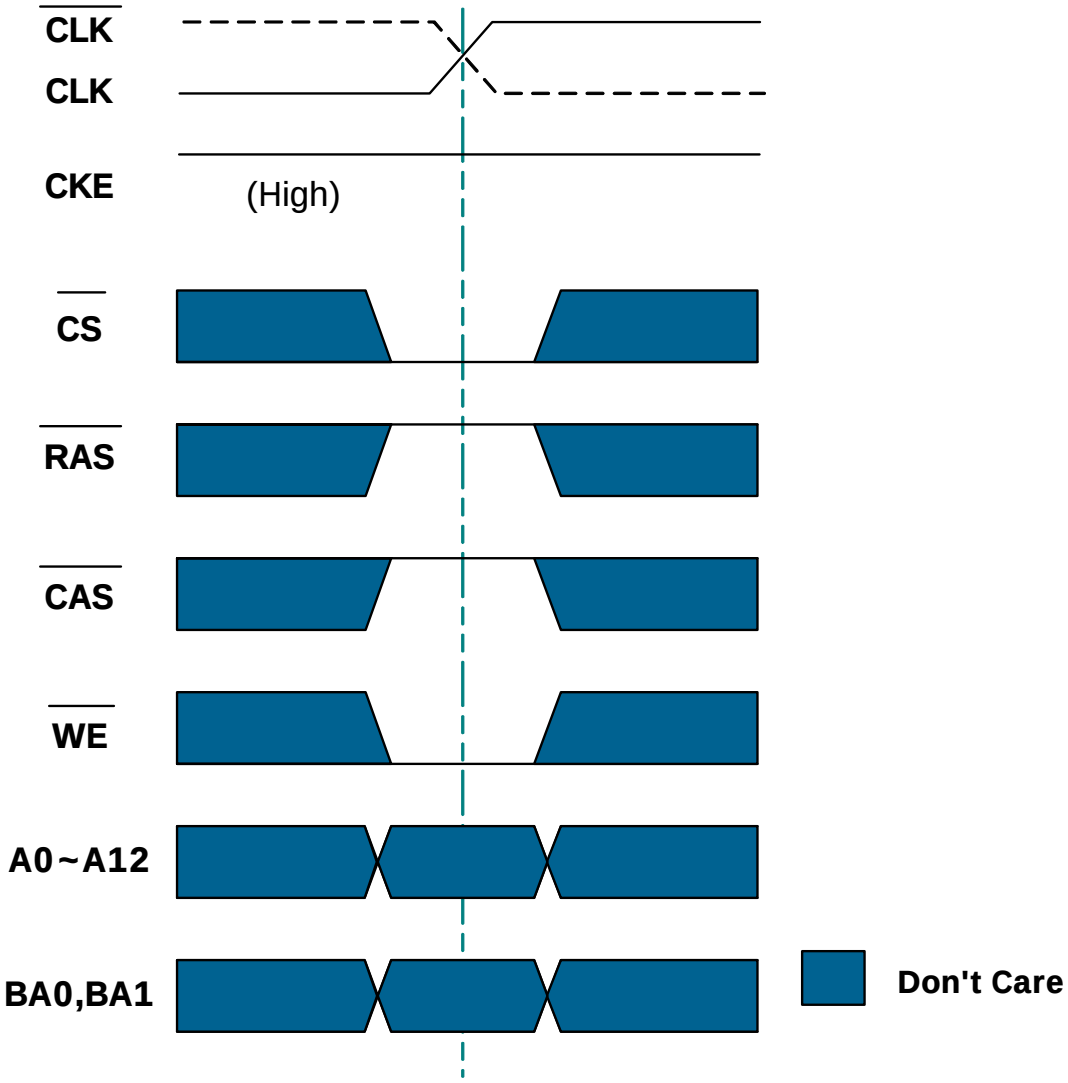


1) DI b = Data In to column b .
2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
3) tWR is referenced from the positive clock edge after the last desired Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) *1 = can be Don't Care for programmed burst length of 4
6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Interrupting Write to Precharge

BURST TERMINATE

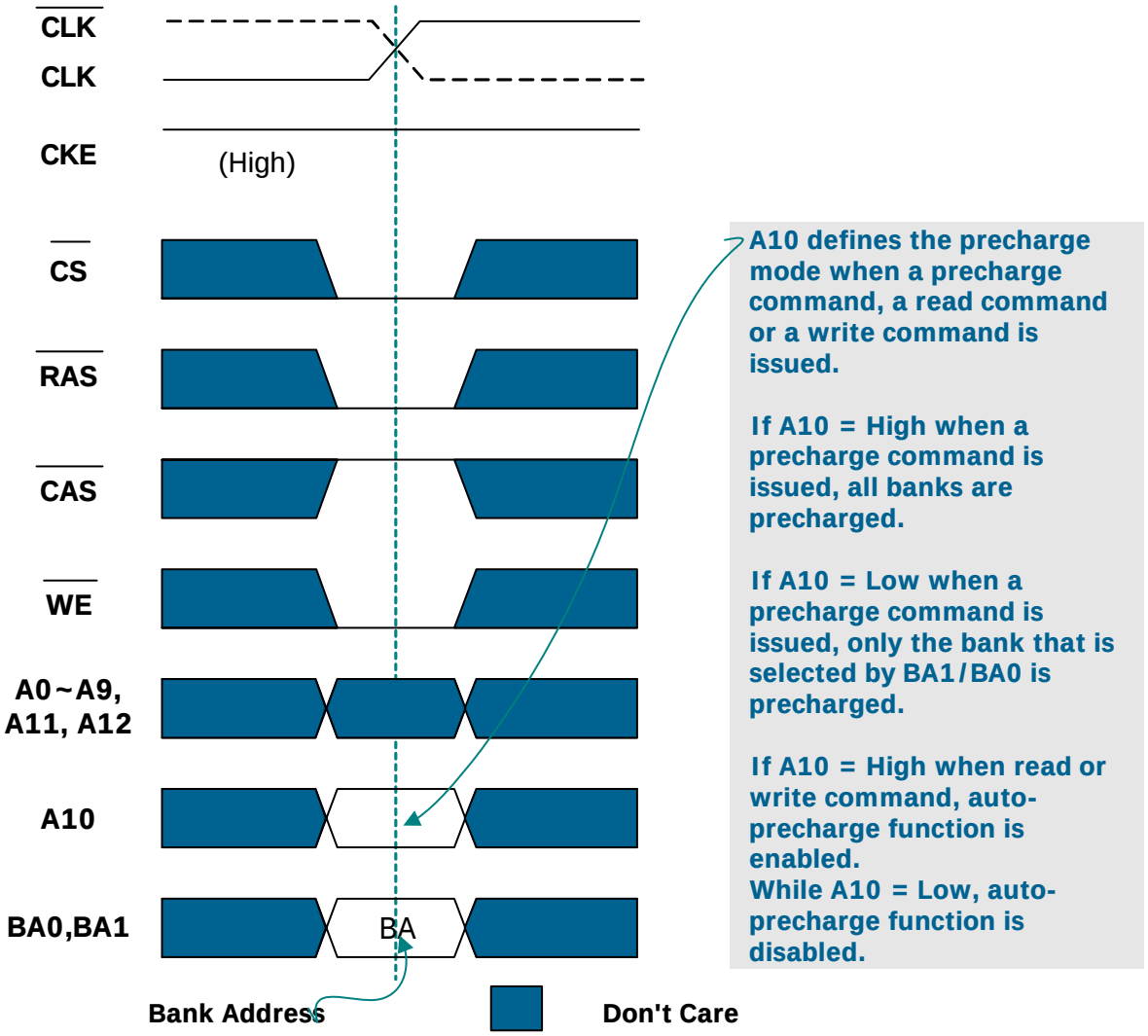
The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.



BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.
If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.
This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.
Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.
The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

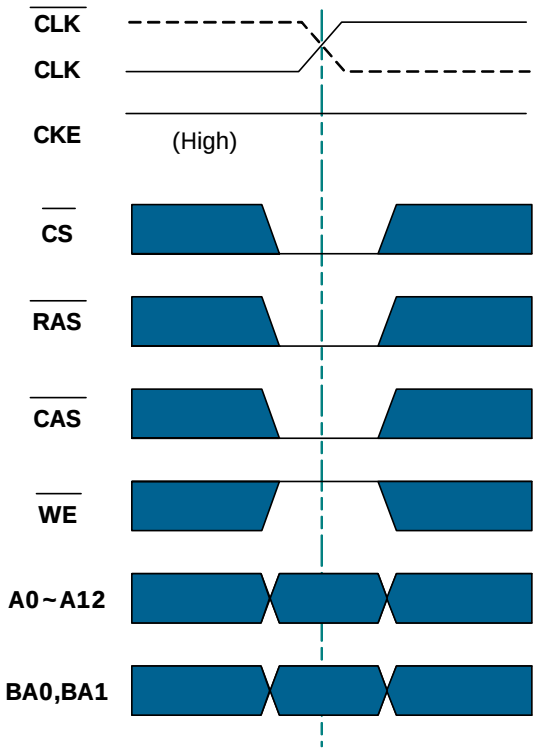
DDR LPSDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

- AUTO REFRESH.

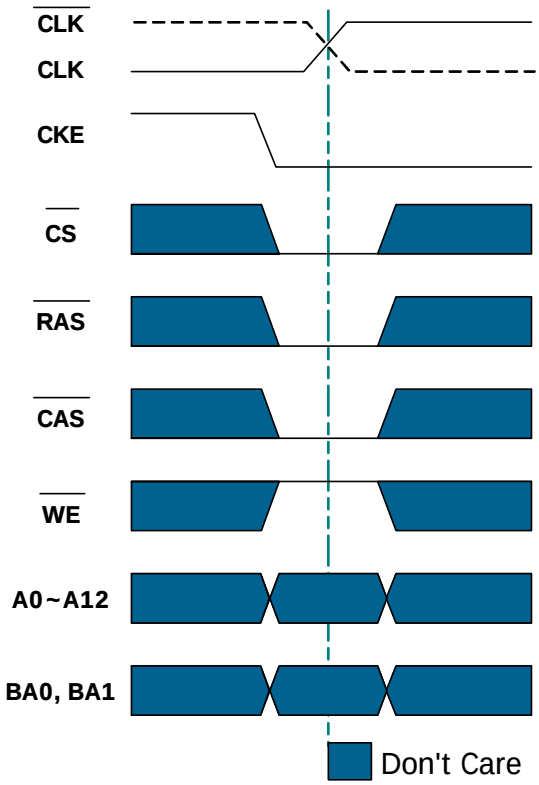
This command is used during normal operation of the DDR LPSDRAM. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The DDR LPSDRAM requires AUTO REFRESH commands at an average periodic interval of tREFI.
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR LPSDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

-SELF REFRESH.

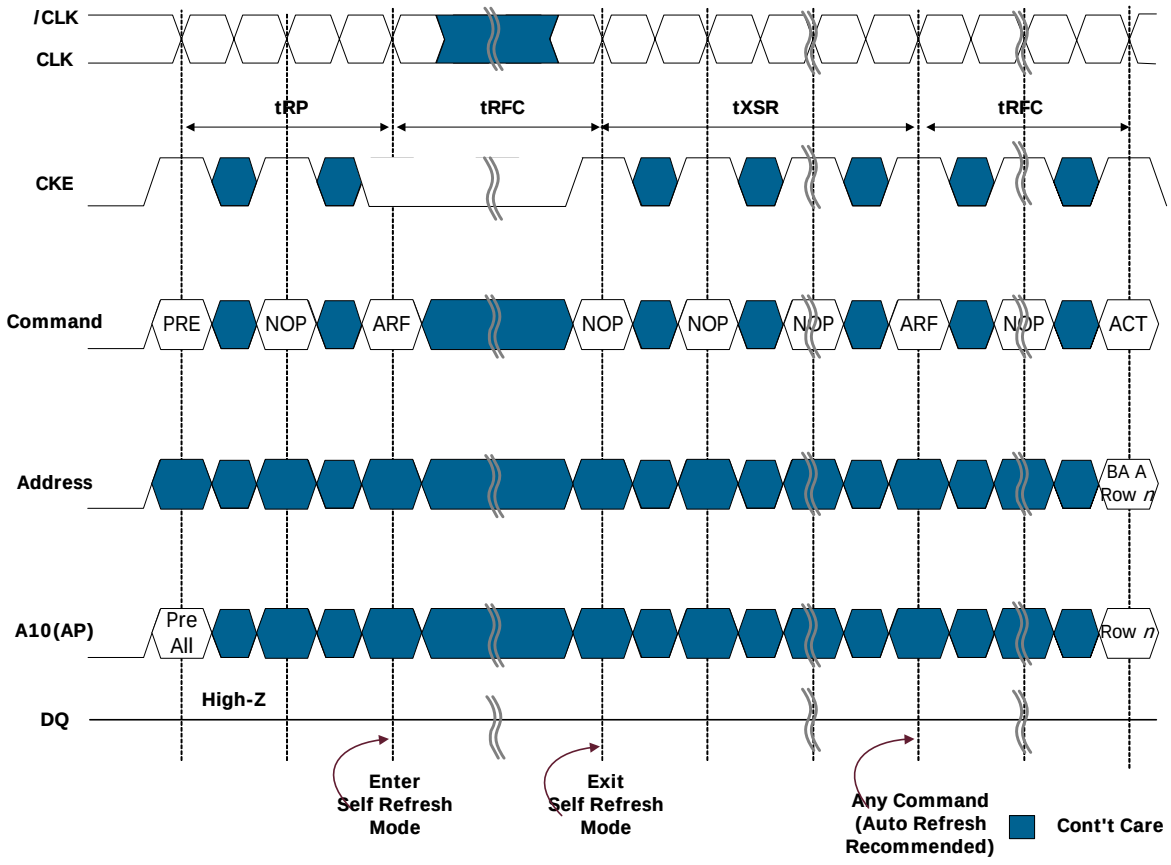
This state retains data in the DDR LPSDRAM, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the DDR LPSDRAM and may vary and may not meet tREFI time.
''Don't Care'' except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high.
NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress.
The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.
The Self Refresh command is used to retain cell data in the LPSDRAM. In the Self Refresh mode, the LP SDRAM operates refresh cycle asynchronously.
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). The DDR LPSDRAM can accomplish an special Self Refresh operation by the specific modes (PASR) programmed in extended mode registers. The DDR LPSDRAM can control the refresh rate automatically by the temperature value of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR (Partial Array Self Refresh). The DDR LPSDRAM can reduce the self refresh current(IDD6) by using these two modes.



Auto Refresh Command



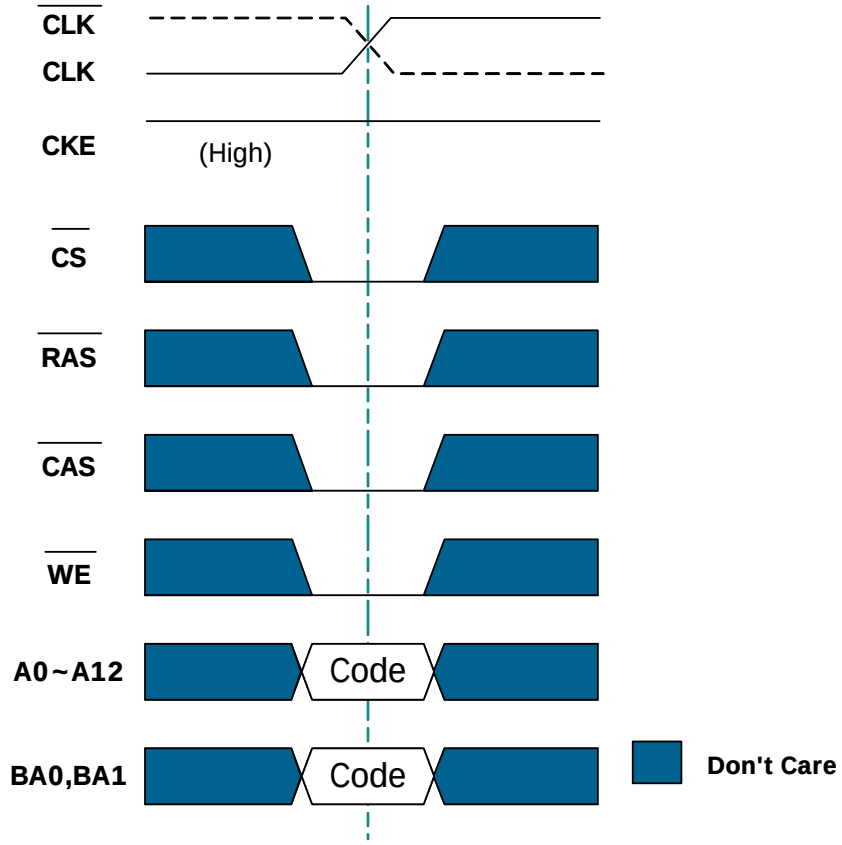
Self Refresh Command



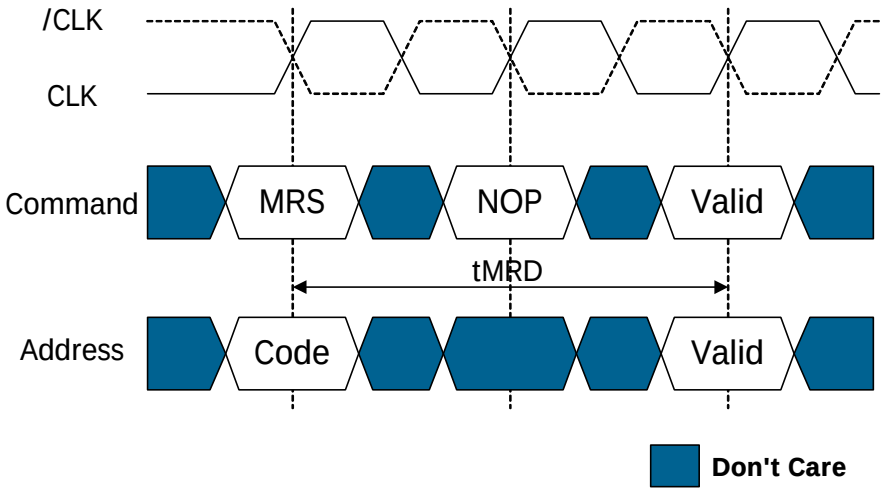
SELF REFRESH ENTRY AND EXIT

MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address bits. BA0 and BA1 are used to select among the Mode Register, the Extended Mode Register and Status Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.



MODE REGISTER SET COMMAND

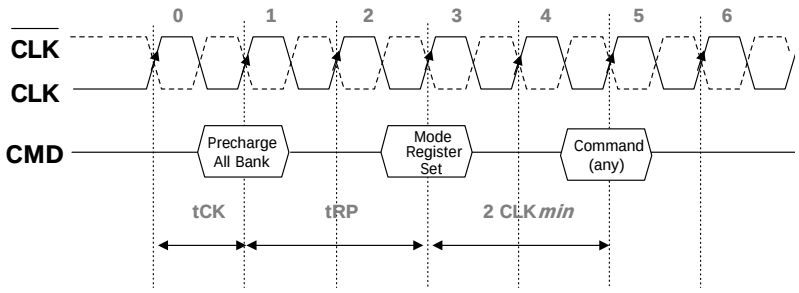


Code = Mode Register / Extended Mode Register selection (BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

Mode Register

The mode register contains the specific mode of operation of the DDR LPSDRAM. This register includes the selection of a burst length(2, 4 or 8), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.



Mode Register Set

BURST LENGTH

Read and write accesses to the DDR LPSDRAM are burst oriented, with the burst length being programmable, as shown in Page10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved.

CAS LATENCY

The CAS latency is the delay between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

Extended Mode Register

The Extended Mode Register contains the specific features of self refresh operation of the DDR LPSDRAM.
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power-Down mode, or the device loses power. The Extended Mode Register should be loaded when all Banks are idle and no bursts are in progress, and subsequent operation should only be initiated after tMRD. Violating these requirements will result in unspecified operation.
The Extended Mode Register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA0. The state of address pins A0 ~ A12 and BA1 in the same cycle as /CS, /RAS, /CAS and /WE going low are written in the extended mode register. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.
This register includes the selection of partial array to be refreshed (full array, half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

PARTIAL ARRAY SELF REFRESH (PASR)

With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, 1/4 array, 1/8 array or 1/16 array could be selected.

DRIVE STRENGTH (DS)

The drive strength could be set to full or half via address bits A5 and A6. The half drive strength is intended for lighter loads or point-to-point environments.

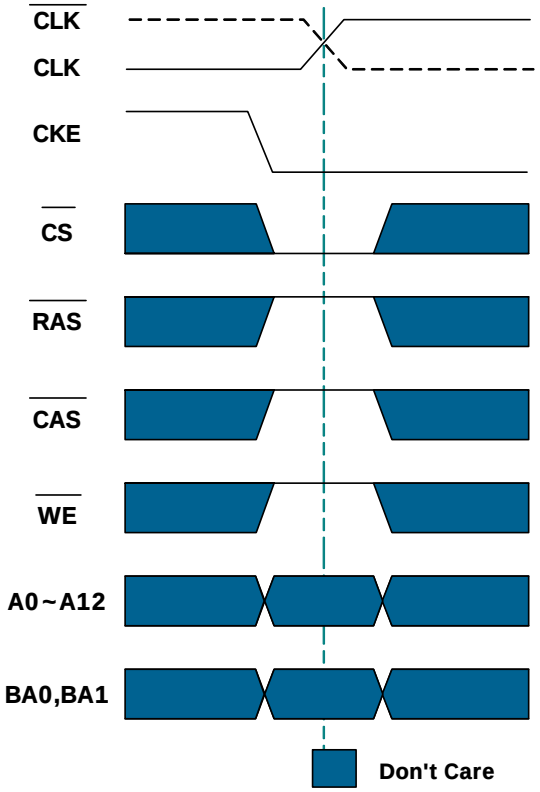
POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
A valid command can be issued after tXP. For Clock stop during power down mode, please refer to the Clock Stop subsection in Operation section of this datasheet.

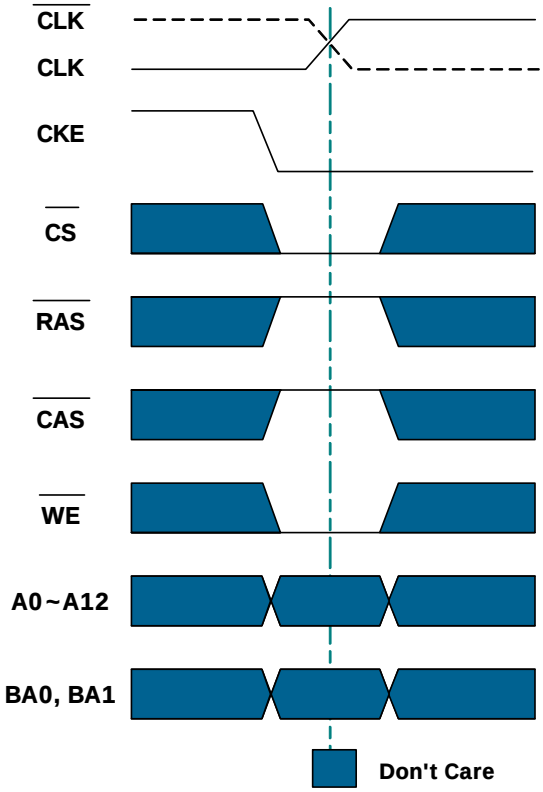
NOTE: This case shows CKE low coincident with NO OPERATION.
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.

DEEP POWER DOWN (Reserved)

The Deep Power Down (DPD) mode enables very low standby currents. All internal voltage generators inside the DDR LPSDRAM are stopped and all memory data is lost in this mode.
All the information in the Mode Register and the Extended Mode Register is lost. Next Figure, DEEP POWER DOWN COMMAND shows the DEEP POWER DOWN command All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this state, CKE must be held in a constant low state.
To exit the DPD mode, CKE is taken high after the clock is stable and NOP command must be maintained for at least 200 us. After 200 us a complete re-initialization routing is required following steps 4 through 11 as defined in POWER-UP and INITIALIZATION SEQUENCES.



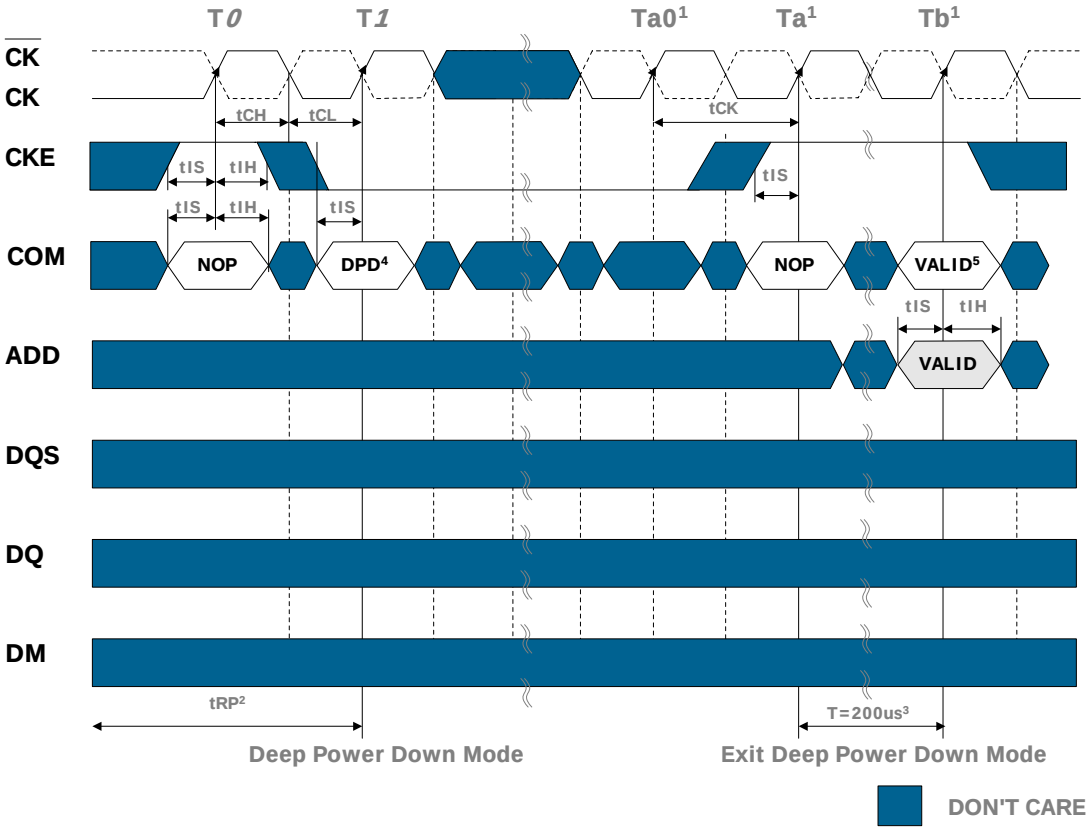
POWER-DOWN ENTRY COMMAND



DEEP POWER DOWN ENTRY COMMAND
(Reserved)

Deep Power Down Entry and Exit (Reserved)

Before entering deep power down the DRAM must be in an all banks idle state with no activity on the data bus. Upon entering deep power down all data will be lost. While in deep power down CKE must be held in a constant low state. Upon exiting deep power down NOP command must be maintained for 200us. After 200us a complete initialization routine is required following steps 4 through 11 as defined in POWER-UP and INITIALIZATION SEQUENCES.



Deep Power-Down Entry and Exit
(Reserved)

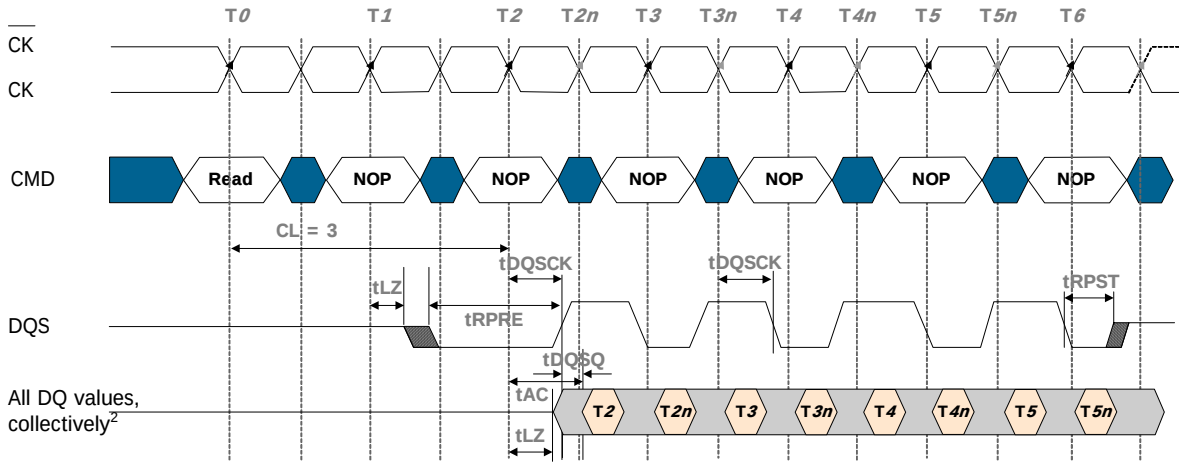
Note:

1. Clock must be stable before exiting deep power down mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering Deep Power Down mode.
3. 200us is required before any command can be applied upon exiting DPD.
4. DPD = Deep Power Down command.
5. Upon exiting Deep Power Down a precharge all command must be issued followed by two auto refresh commands and a load mode register sequence.

CAS LATENCY DEFINITION

CAS latency definition of DDR LPSDRAM must be must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation.

CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (See Figure 2)



CAS LATENCY DEFINITION

NOTE

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CK, and is the long term component of DQ skew.

Clock Stop Mode

Clock stop mode is a feature supported by DDR LPSDRAM devices. It reduces clock-related power consumption during idle periods of the device.

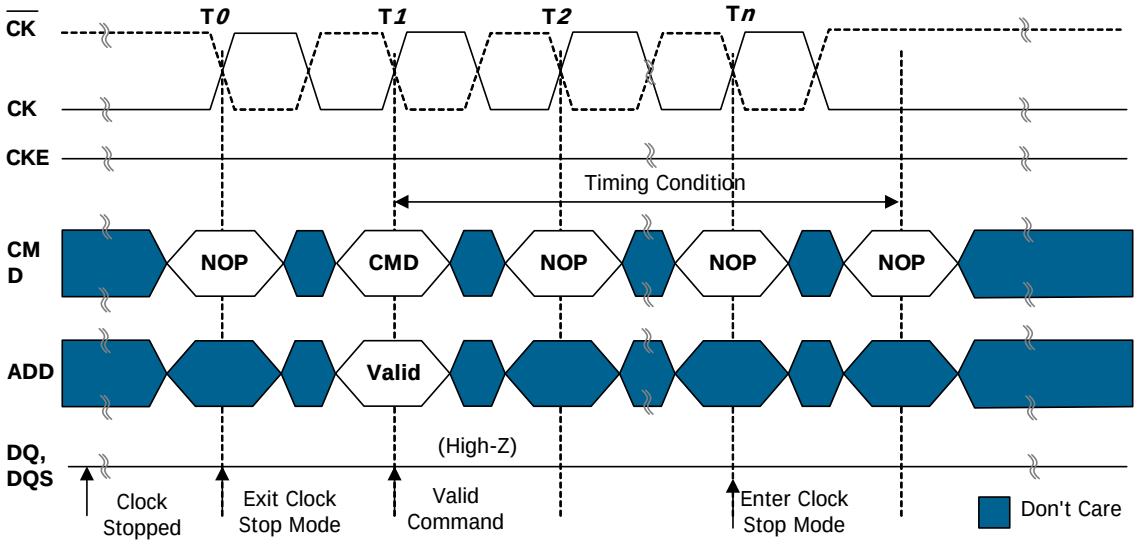
Conditions: the DDR LPSDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and CK held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure1 illustrates the clock stop mode:

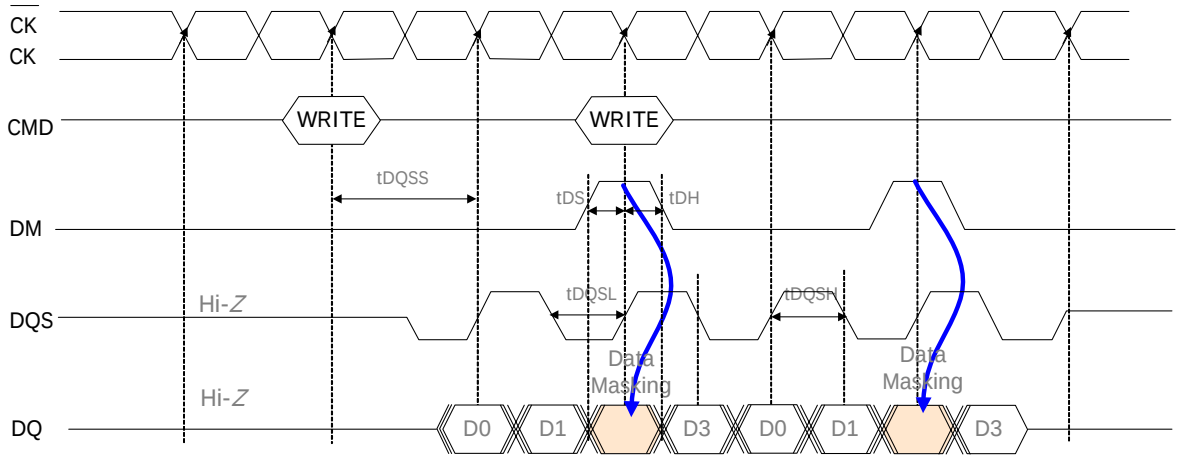
- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- Tn is the last clock pulse required by the access command latched with T1.
- The timing condition of this access command is met with the completion of Tn; therefore Tn is the last clock pulse required by this command and the clock is then stopped.



Clock Stop Mode

Data mask

DDR LPSDRAM uses a DQ write mask enable signal (DM) which masks write data.
Data masking is only available in the write cycle for DDR LPSDRAM. Data masking is available during write, but data masking during read is not available.
DM command masks burst write data with reference to data strobe signal and it is not related with read data.
DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero.
For x16 data I/O, DDR LPSDRAM is equipped with LDM and UDM which control DQ0~DQ7 and DQ8~DQ15 respectively.



POWER-UP AND INITIALIZATION SEQUENCES

DDR LPSDRAM must be powered up and initialized in a predefined manner. Operations procedures other thank those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

Step1: Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold CLOCK ENABLE (CKE) to a LVCMOS logic high level.

Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

Step 3: There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.

Step 4: Issue a PRECHARGE ALL command.

Step 5: Provide NOPs or DESELECT commands for at least tRP time.

Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time.
Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.

Step 7: Using the MRS command, load the base mode register. Set the desired operating modes.

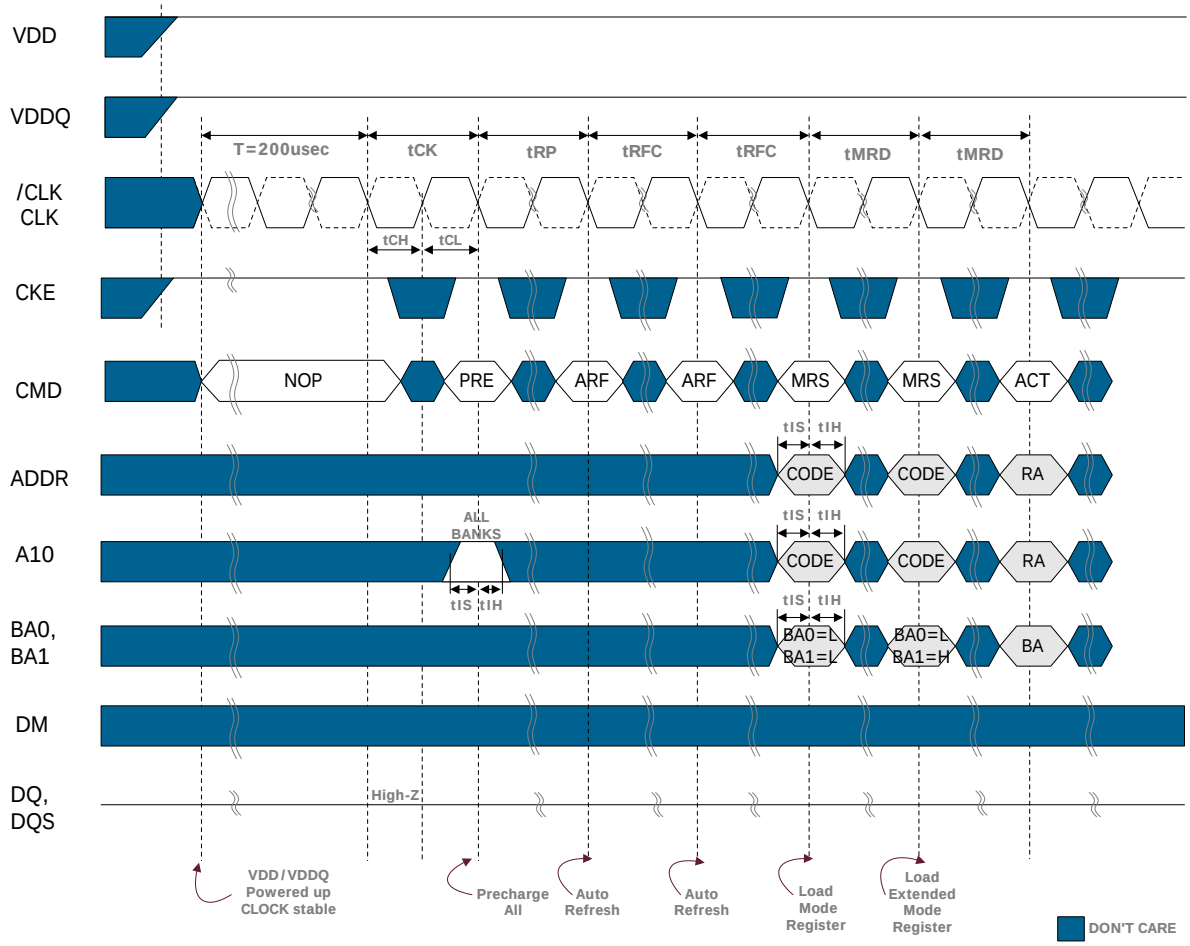
Step 8: Provide NOPs or DESELECT commands for at least tMRD time.

Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

Step 10: Provide NOP or DESELCT commands for at least tMRD time.

Step 11: The DRAM has been properly initialized and is ready for any valid command.

The Initialization flow sequence is below.



Initialization Waveform Sequence

1 Gbit NAND E2PROM

Memory cell 1056 × 64K × 16

Register 1056 × 16

Page size 1056 words

Block size (64K + 2K) words

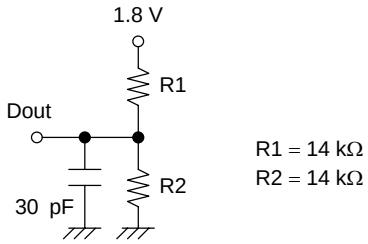
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = –30° to 85°C, V_{CC} = 1.70 V to 1.95 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	6	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	10	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	6	—	ns	
t_{WP}	Write Pulse Width	15	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	6	—	ns	
t_{DS}	Data Setup Time	12	—	ns	
t_{DH}	Data Hold Time	6	—	ns	
t_{WC}	Write Cycle Time	30	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	25	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time	—	25	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low	10	—	ns	
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns	
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	45	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	100	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	30	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	6/6/10/500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION
Vcc	1.70V to 1.95V
Input level	V_{CC} – 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	See below Figure



Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS

(Ta = –30° to 85°C, V_{CC} = 1.70 V to 1.95 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	300	700	μs	
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	2.5	10	ms	

(1): Refer to Application Note (12) toward the end of this document.

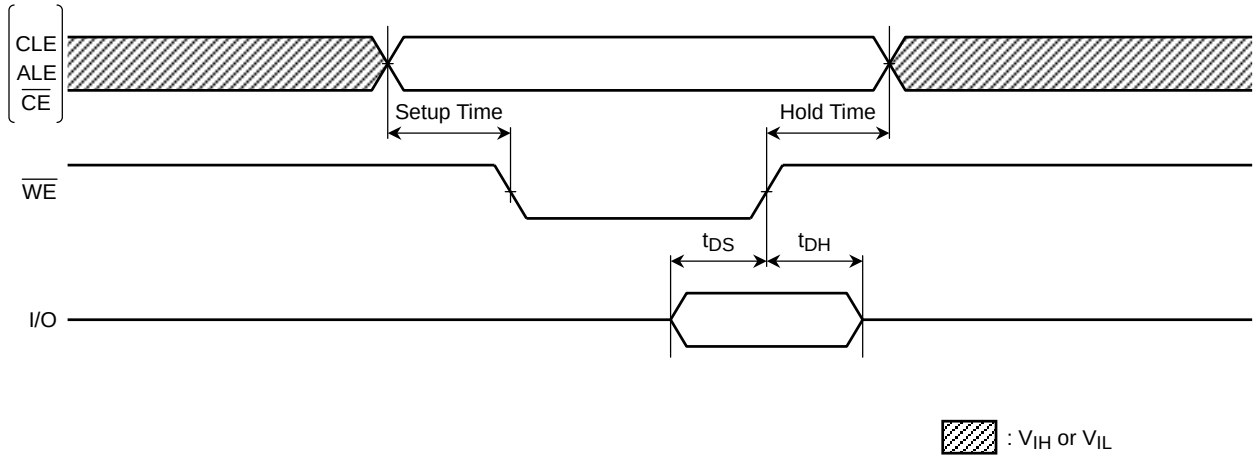
VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

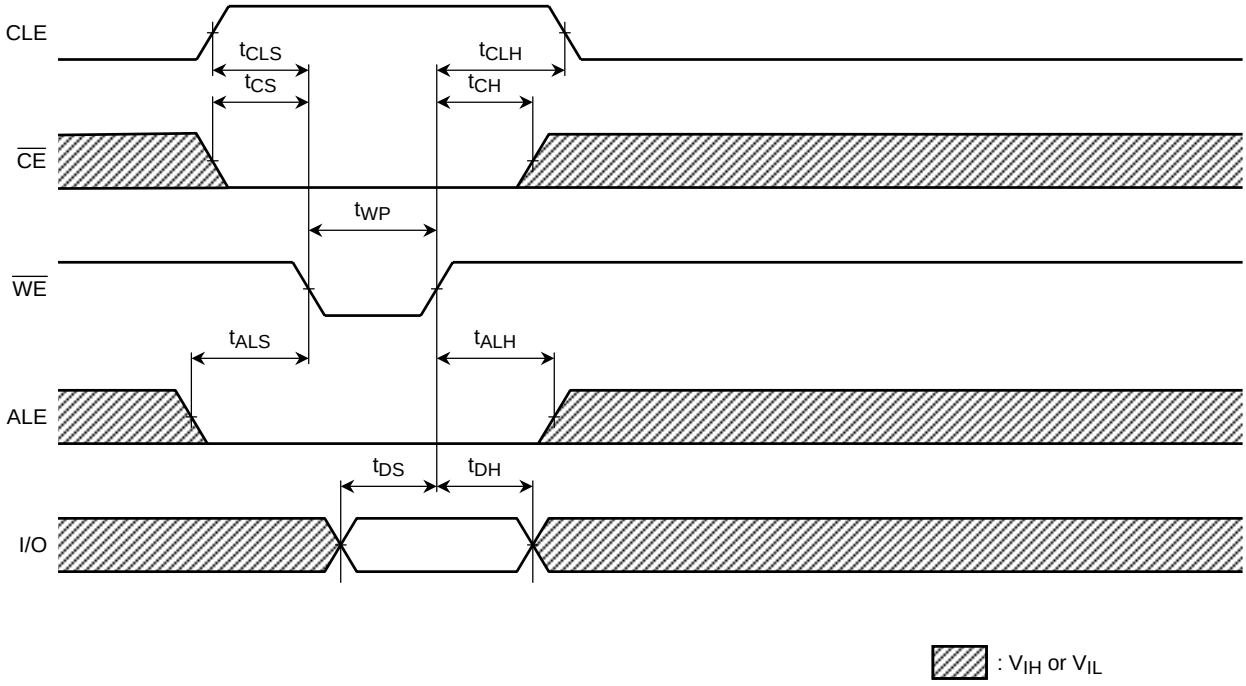
NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime..

TIMING DIAGRAMS

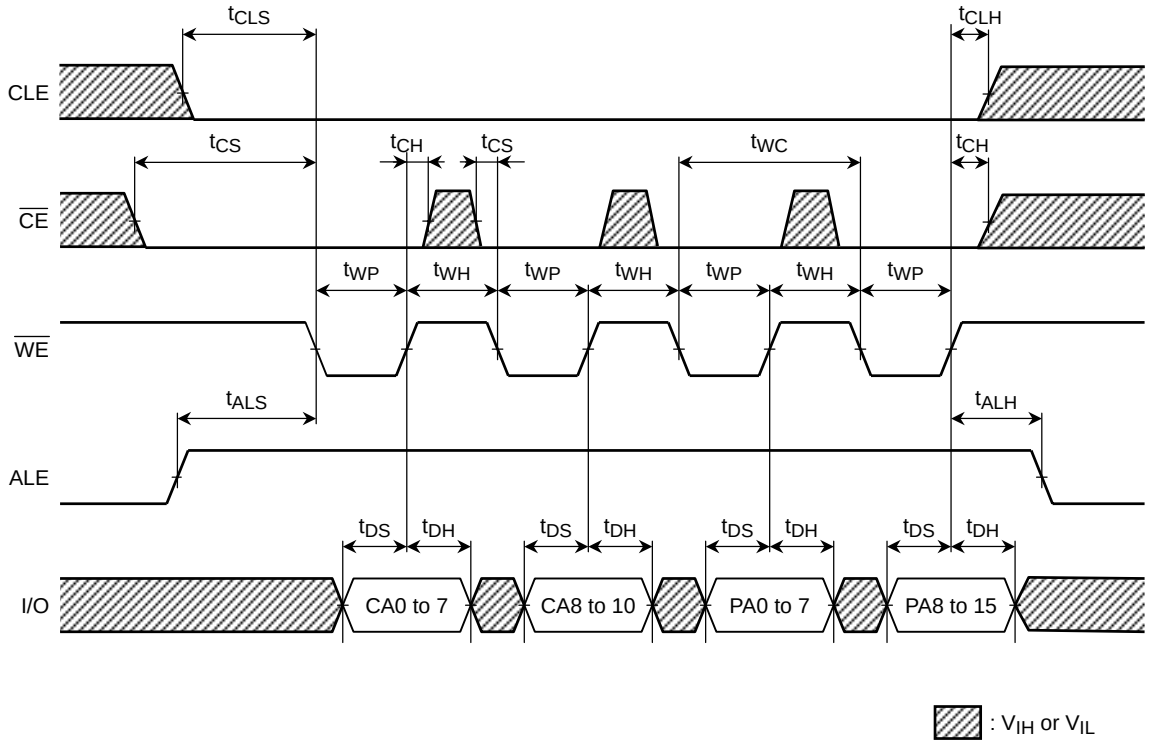
Latch Timing Diagram for Command/Address/Data



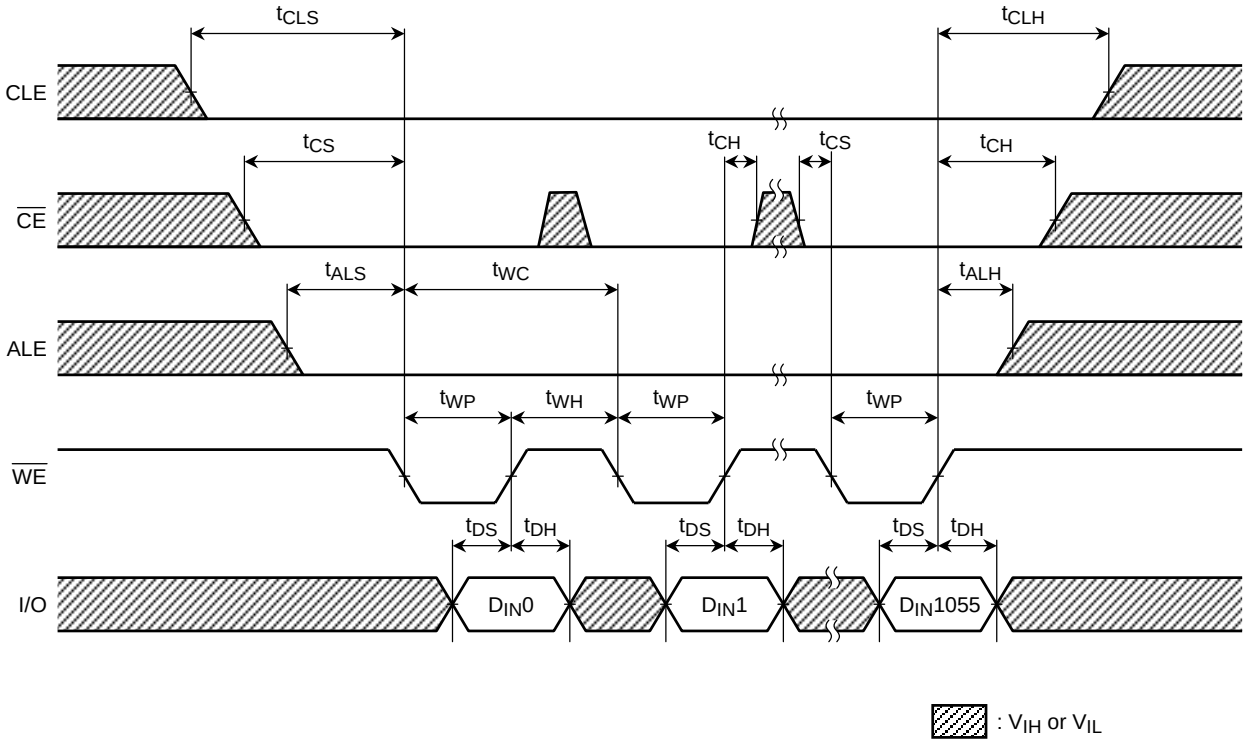
Command Input Cycle Timing Diagram



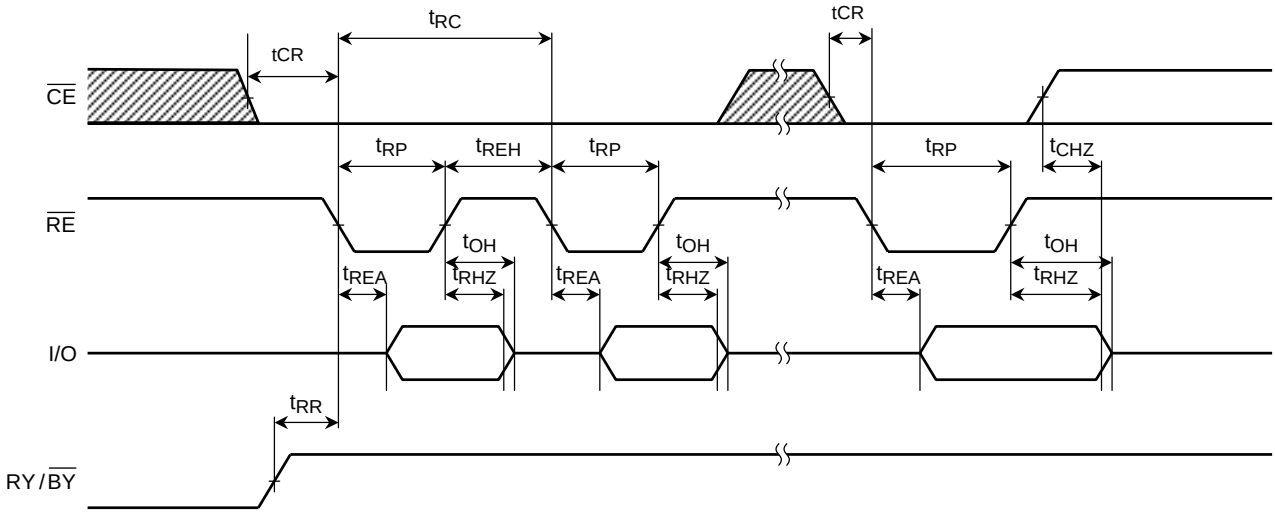
Address Input Cycle Timing Diagram



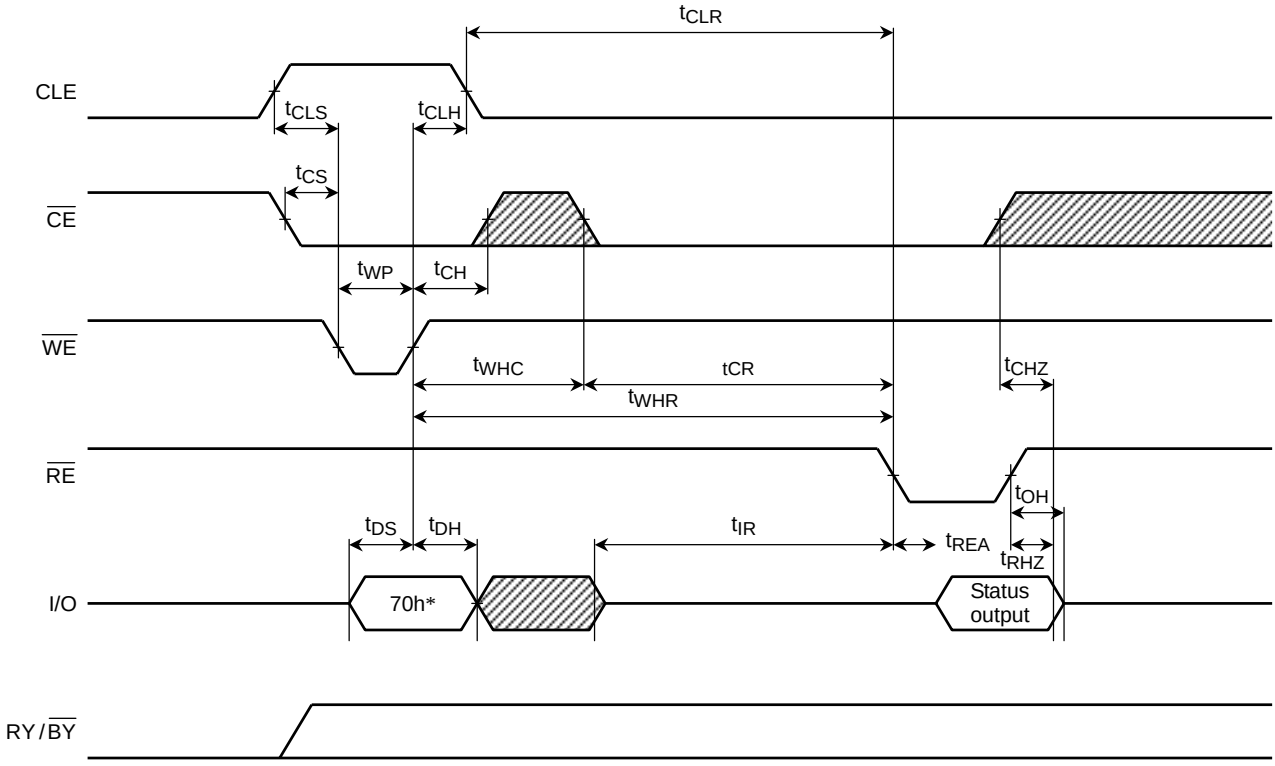
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



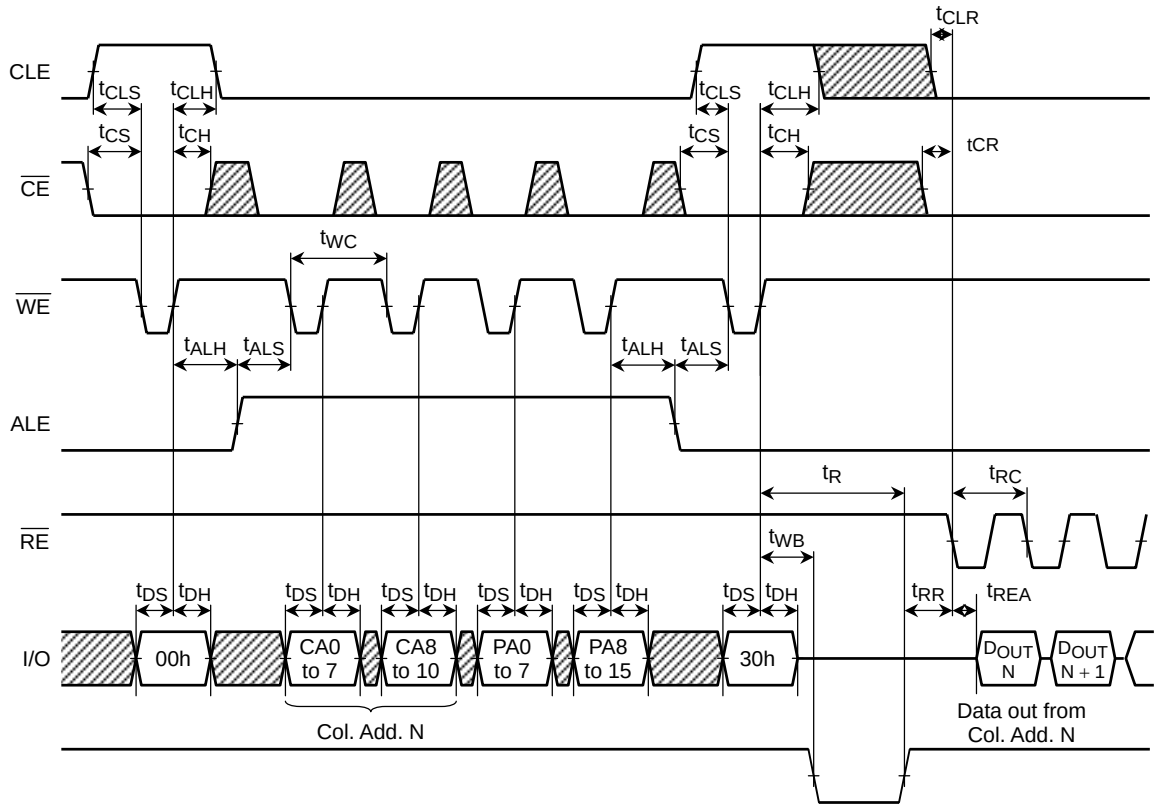
Status Read Cycle Timing Diagram



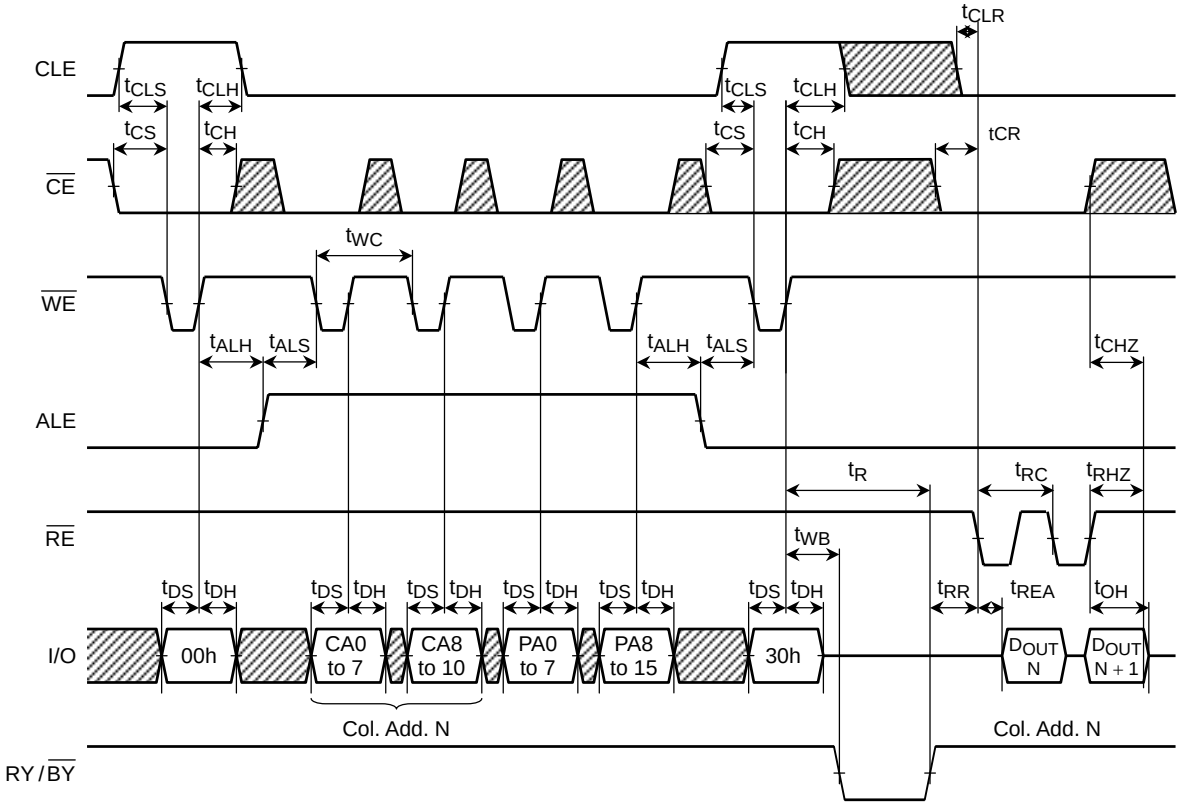
*: 70h represents the hexadecimal number

: V_{IH} or V_{IL}

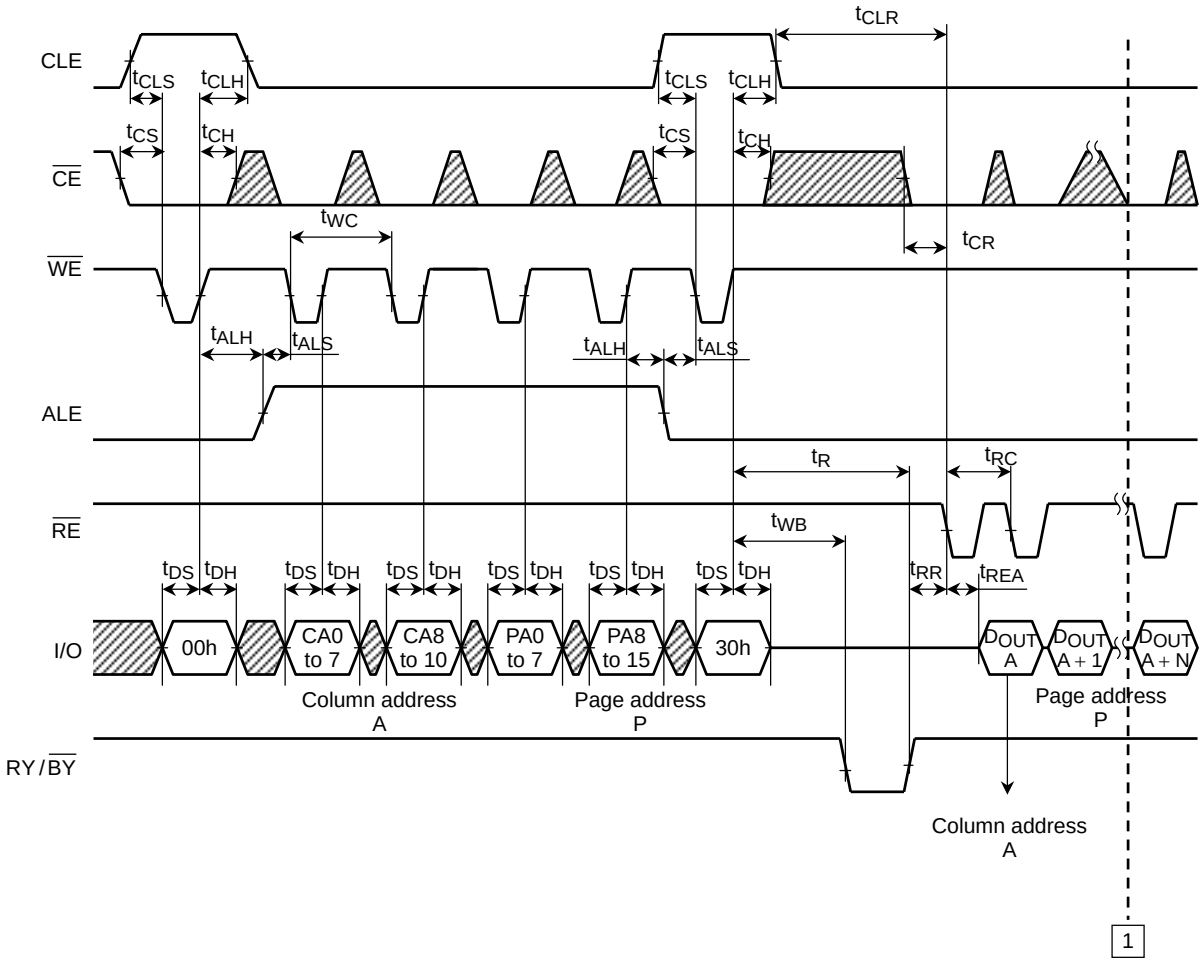
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

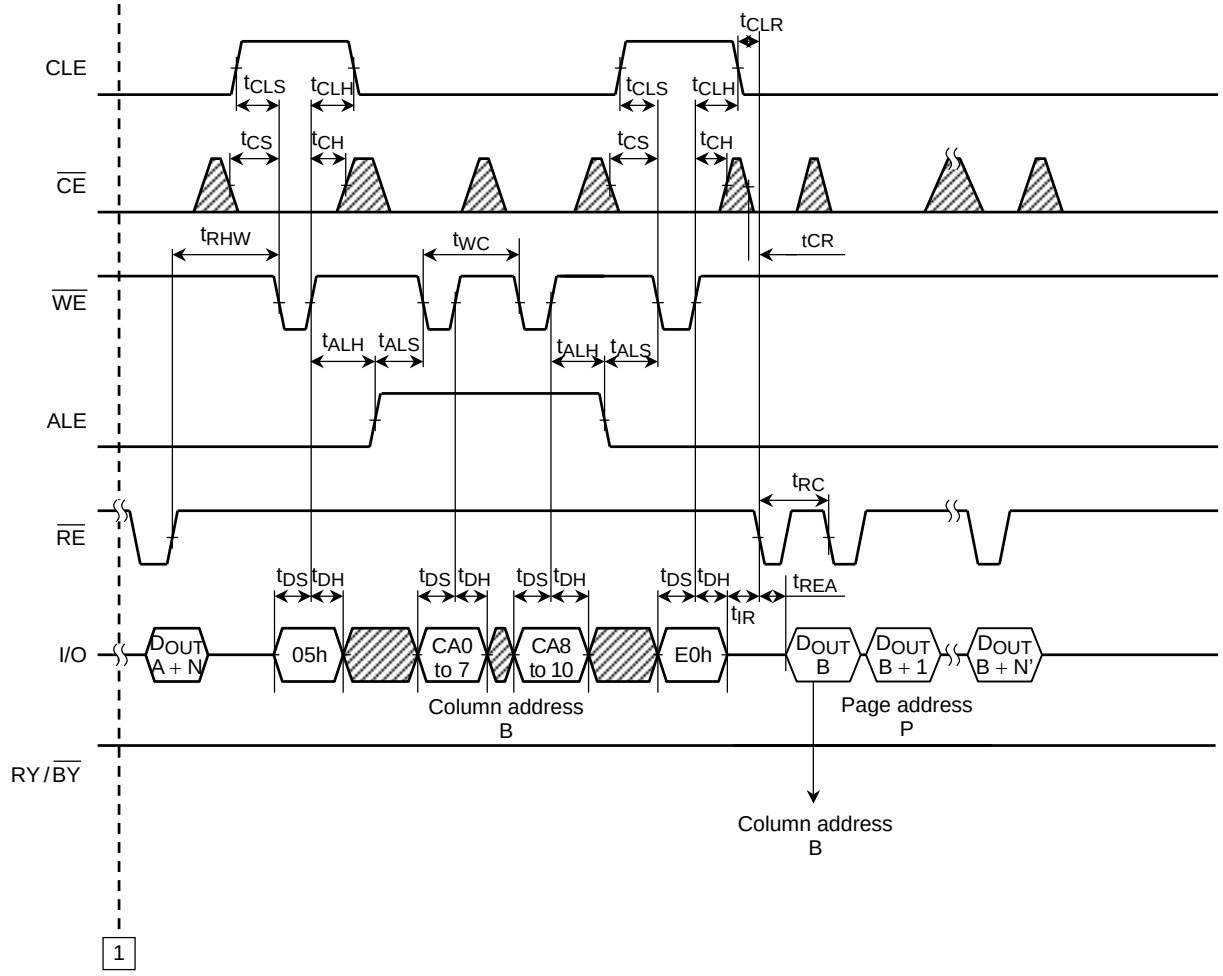


Column Address Change in Read Cycle Timing Diagram (1/2)



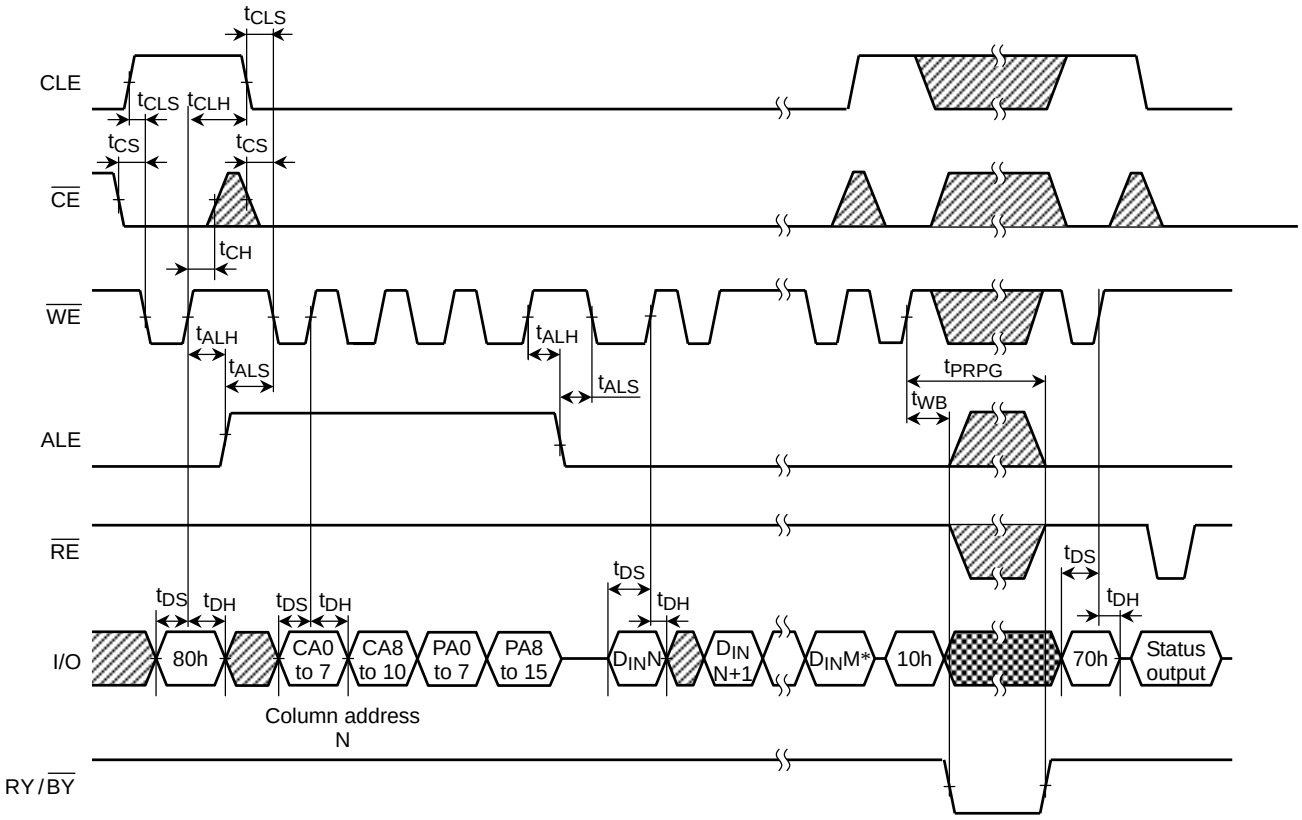
Continues from 1 of next page

Column Address Change in Read Cycle Timing Diagram (2/2)



Continues from 1 of last page

Auto-Program Operation Timing Diagram

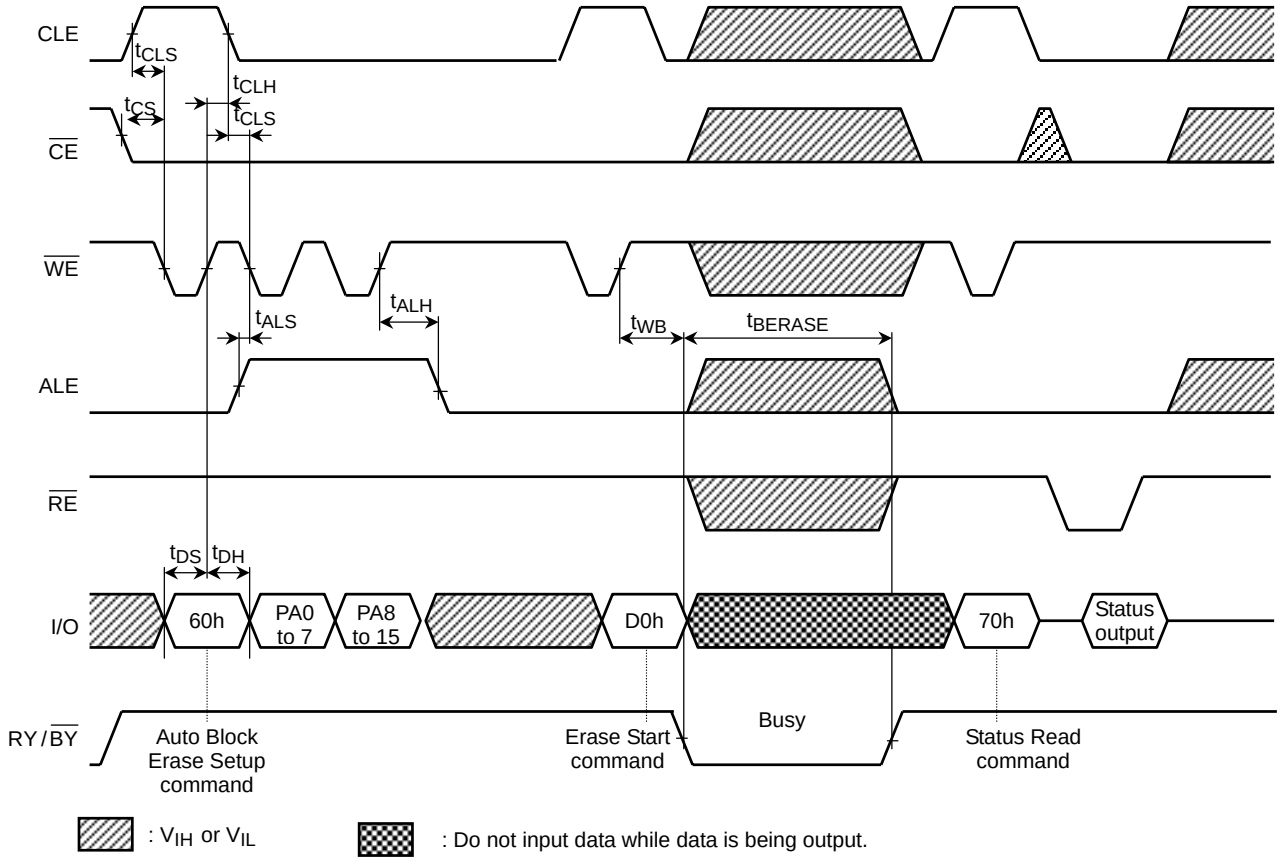


: Do not input data while data is being output.

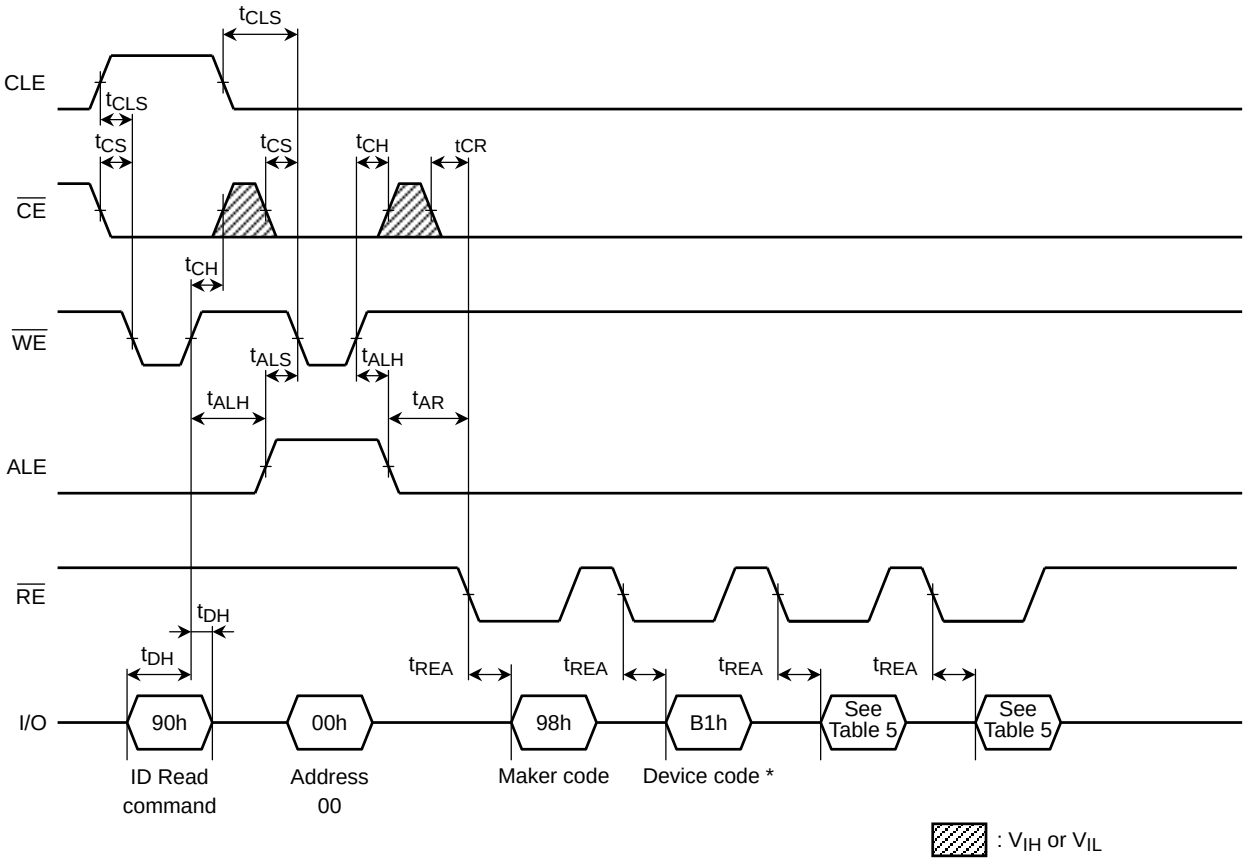
: V_{IH} or V_{IL}

*) M: up to 1056

Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + l) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

I/O Port: I/O9 to 16

The I/O9 to 16 pins are used as a port for transferring input/output data to and from the device. I/O9 to 16 pins must be low level (V_{IL})when address and command are input.

Write Protect: $\overline{WP}$

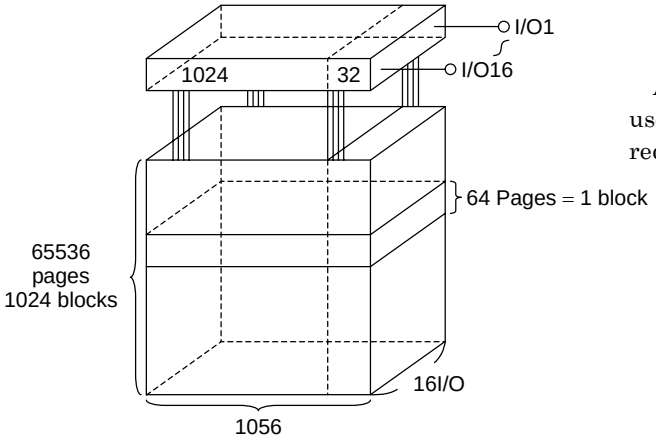
The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to V_{CC} with an appropriate resister.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 1056 words in which 1024 words are used for main memory storage and 32 words are for redundancy or for other uses.

1 page = 1056 words
1 block = 1056 words × 64 pages = (64K + 2K) words
Capacity = 1056 bytes × 64pages × 1024 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	L	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA10: Column address
PA0 to PA15 Page address

PA6 to PA15 Block address
PA0 to PA5: NAND address in block

Note) I/O9 – 16 must be held low when address is input.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L		H	*
Data Input	L	L	L		H	H
Address input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
Reset	FF	—	○

HEX data bit assignment

(Example)

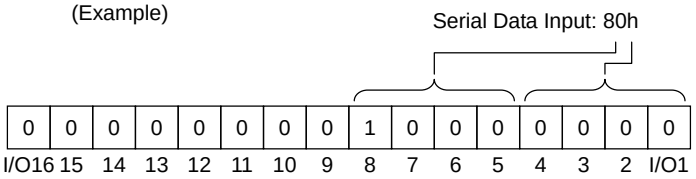


Table 4. Read mode operation states

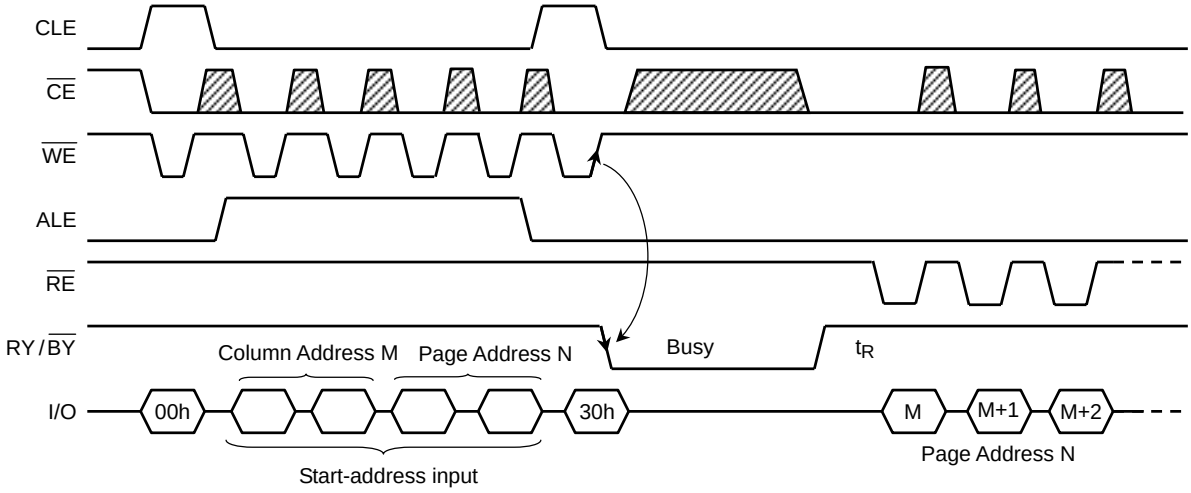
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O16	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

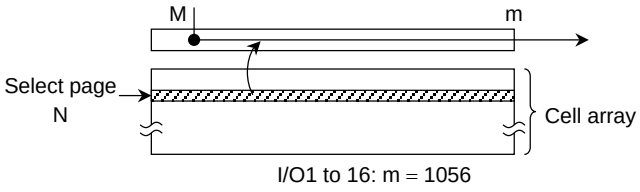
H: V_{IH}, L: V_{IL},

DEVICE OPERATION

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).

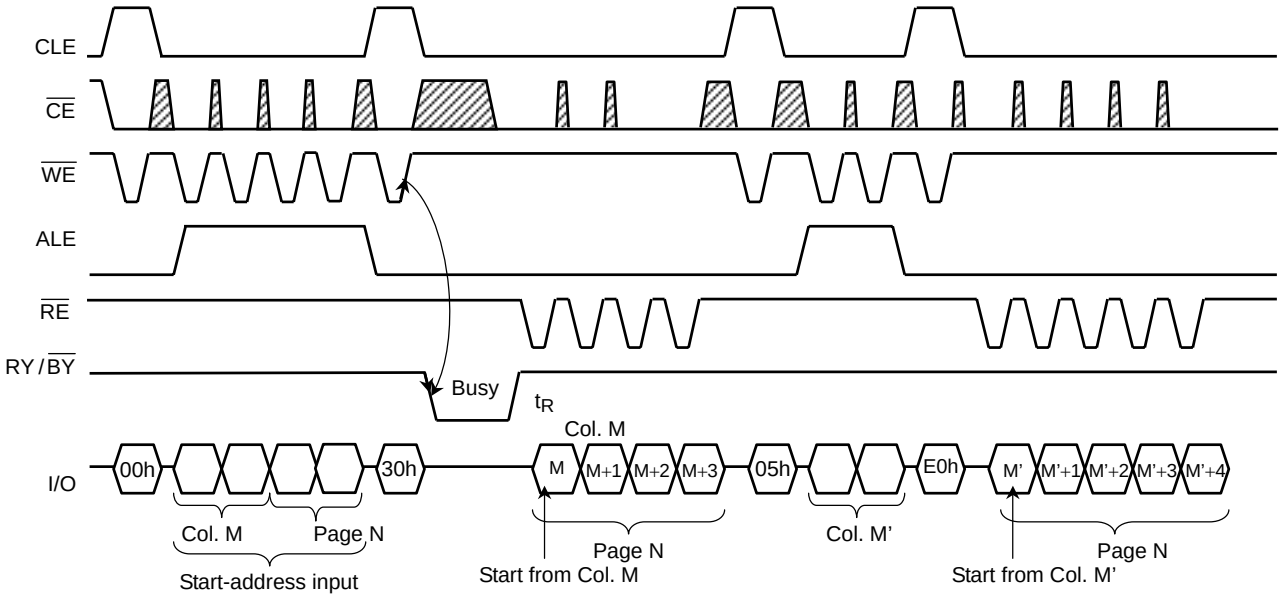


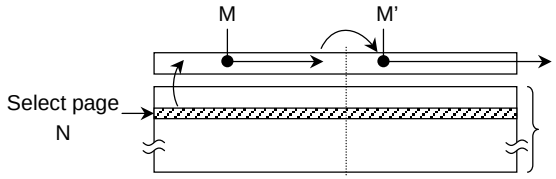


A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle..

Random Column Address Change in Read Cycle

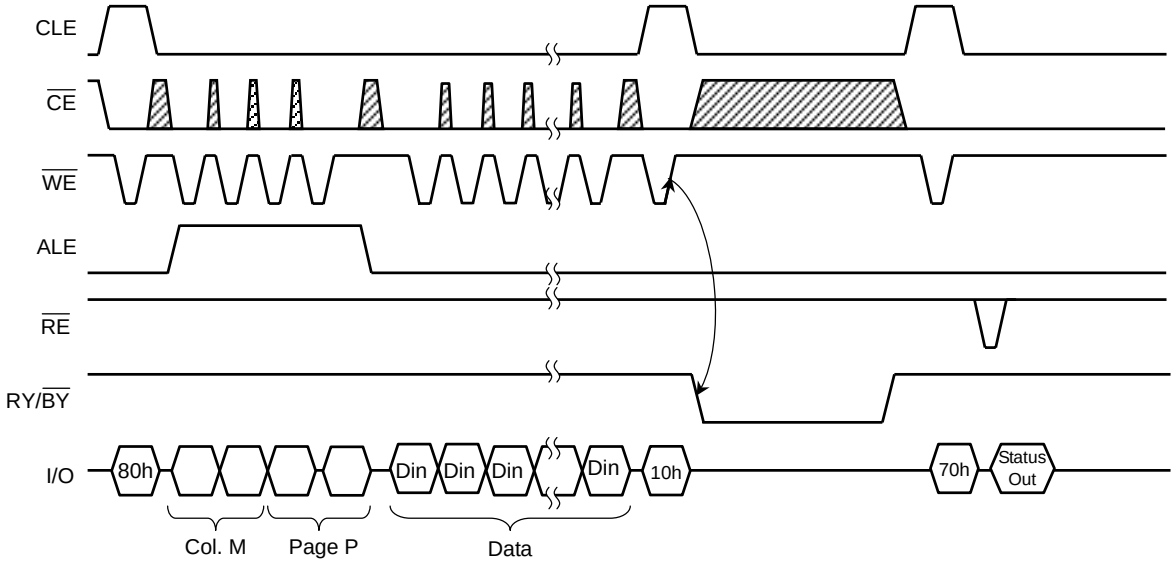


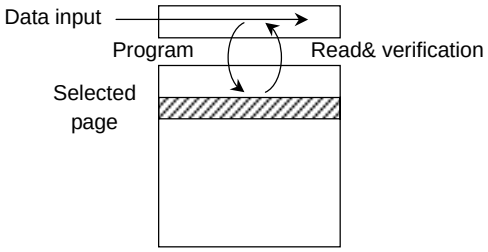


During the serial data output from the register, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



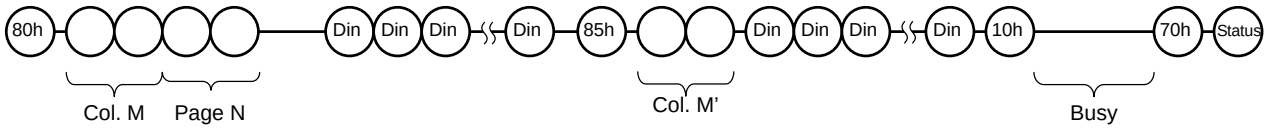


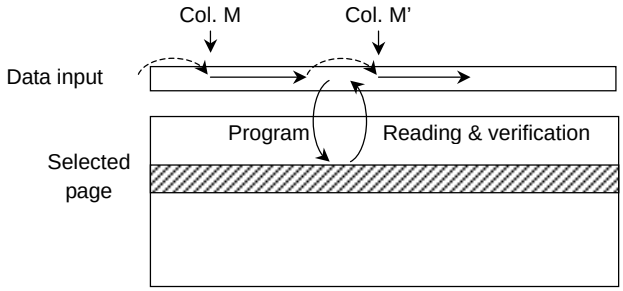
The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the "10h" command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

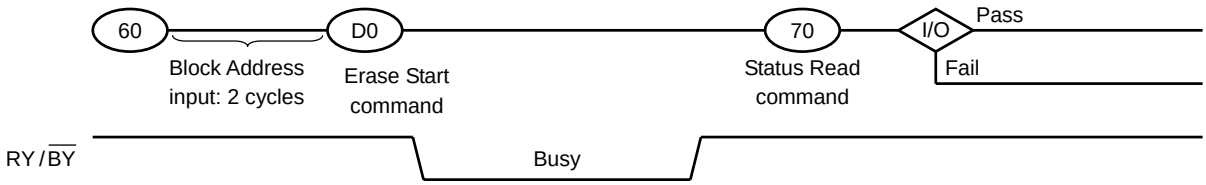
Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.





Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

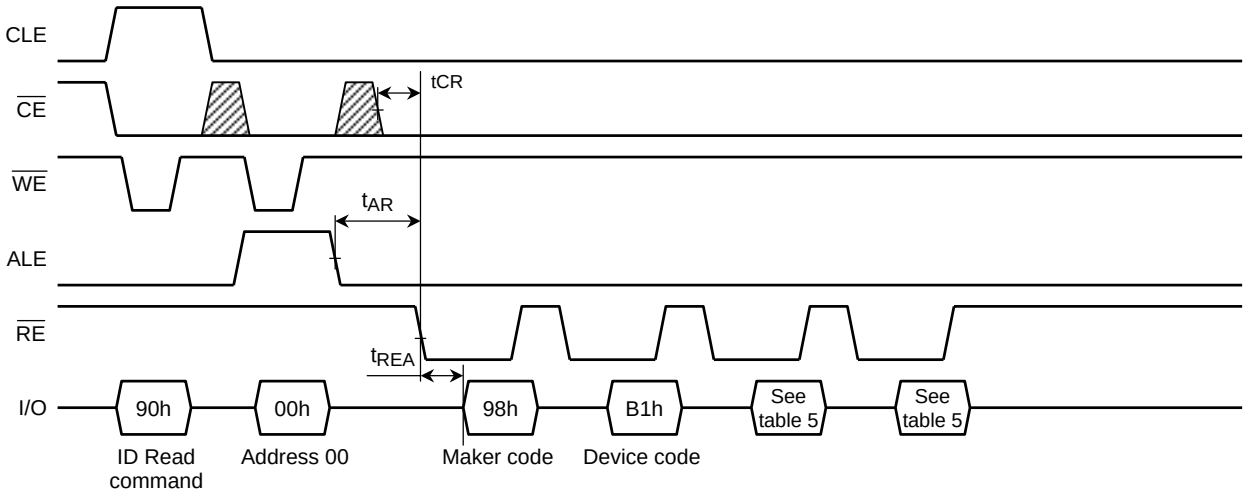


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	0	1	1	0	0	0	1	B1h
3rd Data	Chip Number, Cell Type	—	—	—	—	—	—	—	—	See table
4th Data	Page Size, Block Size, Redundant Size, Organization	—	—	—	—	—	—	—	—	See table

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		
Reserved		0 or 1	0	0 or 1	0 or 1				

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB 2 KB 4 KB 8 KB							0 0 1 1	0 1 0 1
Block Size (without redundant area)	64 KB 128 KB 256 KB 512 KB			0 0 1 1	0 1 0 1				
Redundant area size (byte/512byte)	8 16 Reserved Reserved					0 0 1 1	0 1 0 1		
Organization	×8 ×16		0 1						
Reserved		0 or 1							

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a "70h" command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

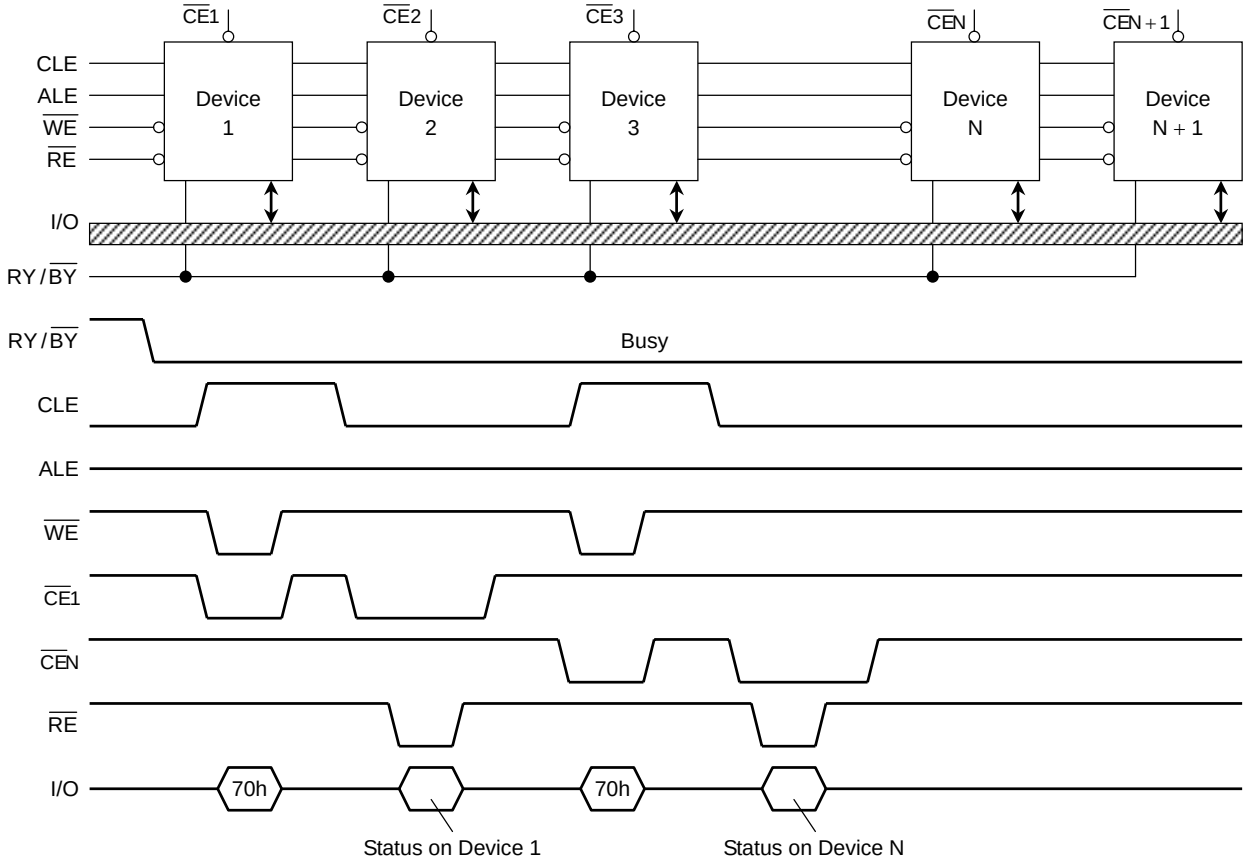
The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Read
I/O1	Chip Status Pass: 0 Fail: 1	Pass/Fail	Invalid
I/O2	Not Used	Invalid	Invalid
I/O3	Not Used	0	0
I/O4	Not Used	0	0
I/O5	Not Used	0	0
I/O6	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy
I/O7	Not Used	Invalid	Invalid
I/O8	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect
I/O9-16	Not Used	Not Used	Not Used

The Pass/Fail status on I/O1 and I/O2 is only valid during a Program/Erase operation when the device is in the Ready state.

An application example with multiple devices is shown in the figure below.



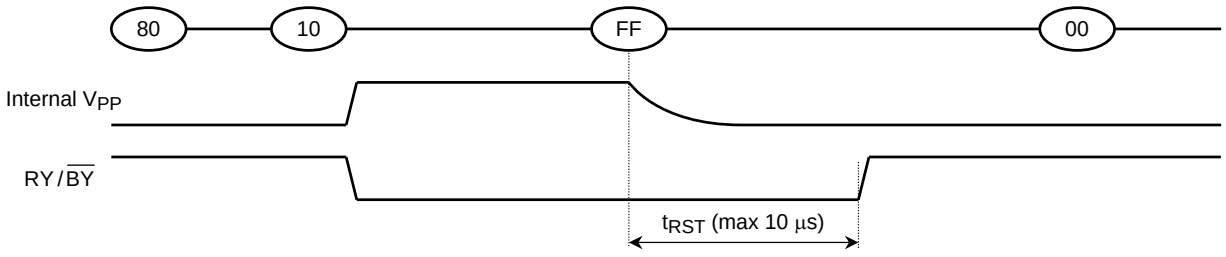
System Design Note: If the RY / $\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Reset

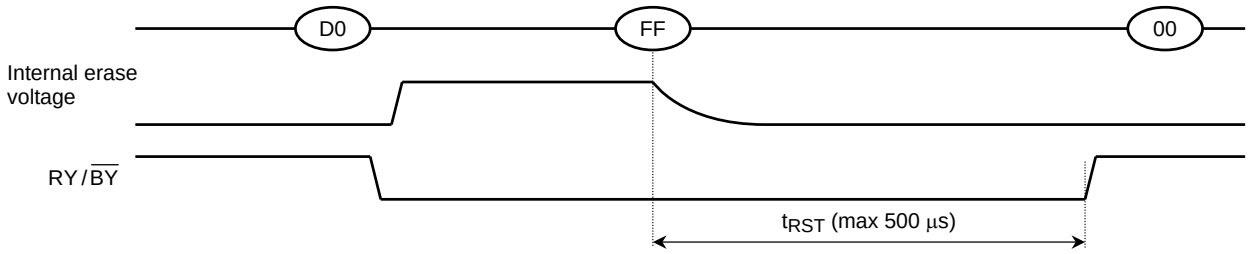
The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

The response to a "FFh" Reset command input during the various device operations is as follows:

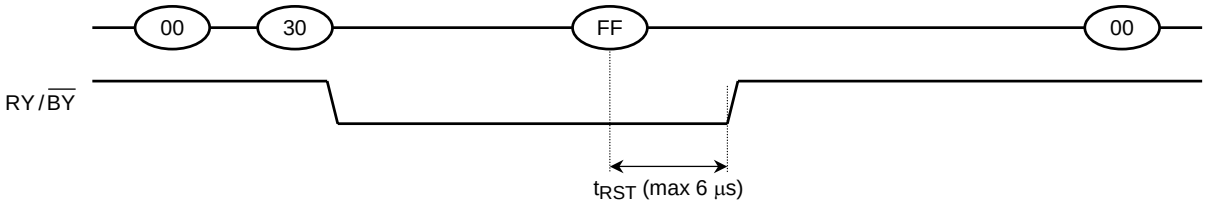
When a Reset (FFh) command is input during programming



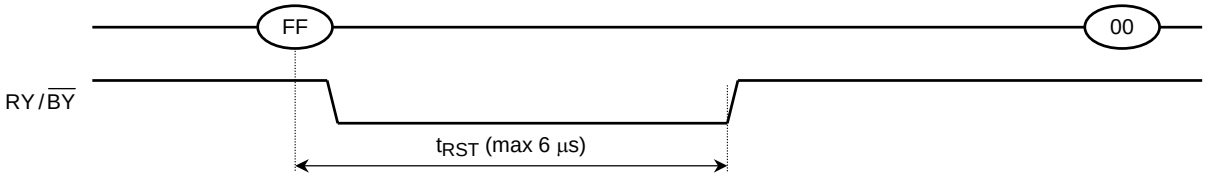
When a Reset (FFh) command is input during erasing



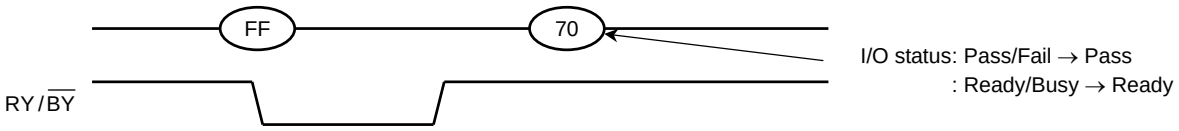
When a Reset (FFh) command is input during Read operation



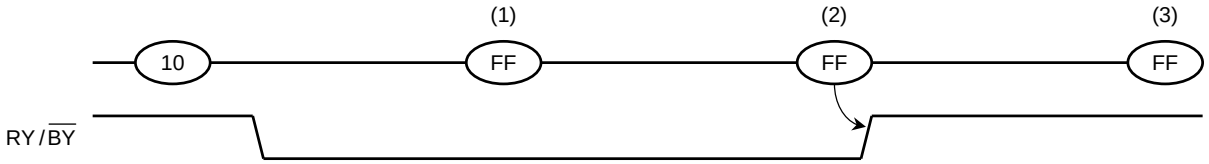
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



The second (FF) command is invalid, but the third (FF) command is valid.

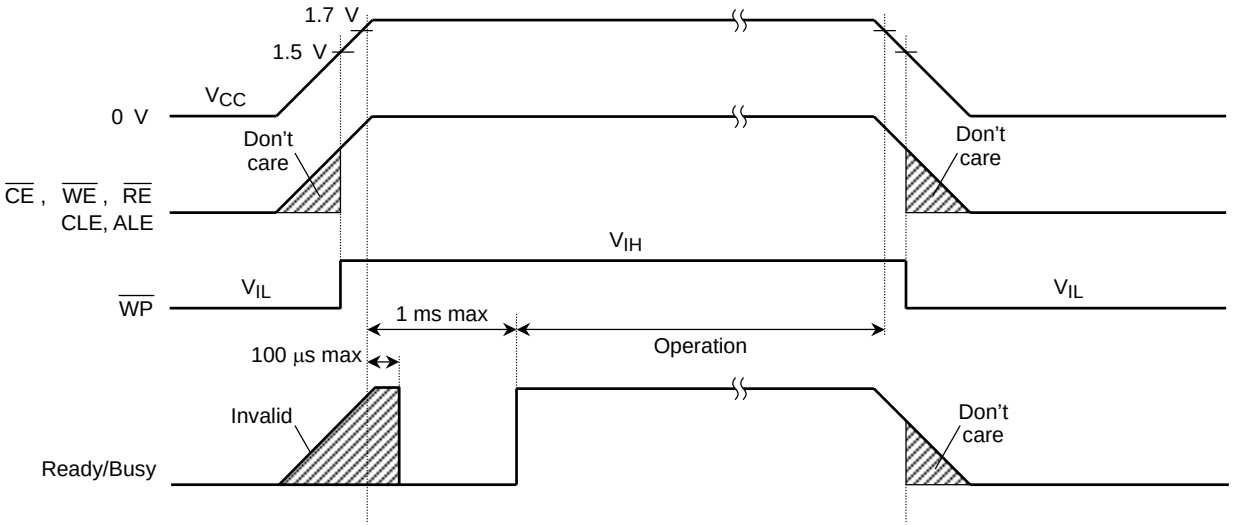
APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

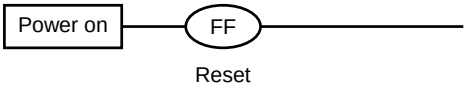
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

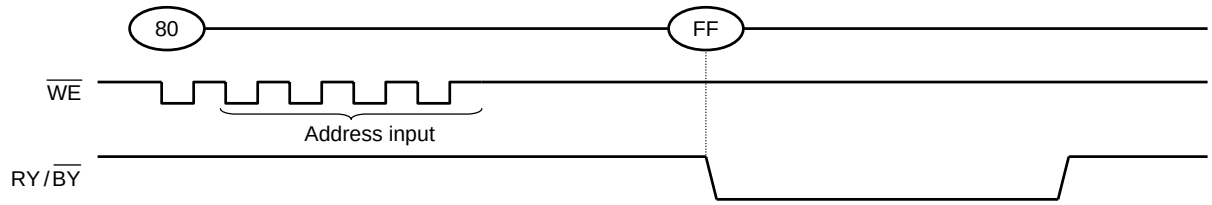
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

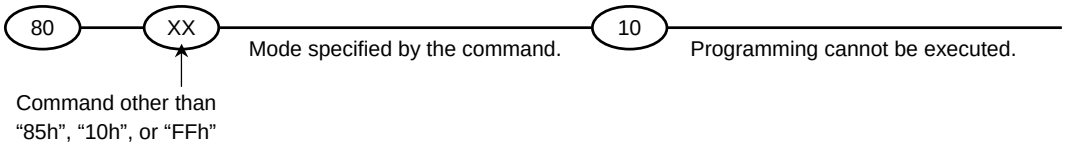
During the Busy state, do not input any command except 70h and FFh.

(5) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Column Address Change in Serial Data Input command "85h", Auto Program command "10h" or the Reset command "FFh".

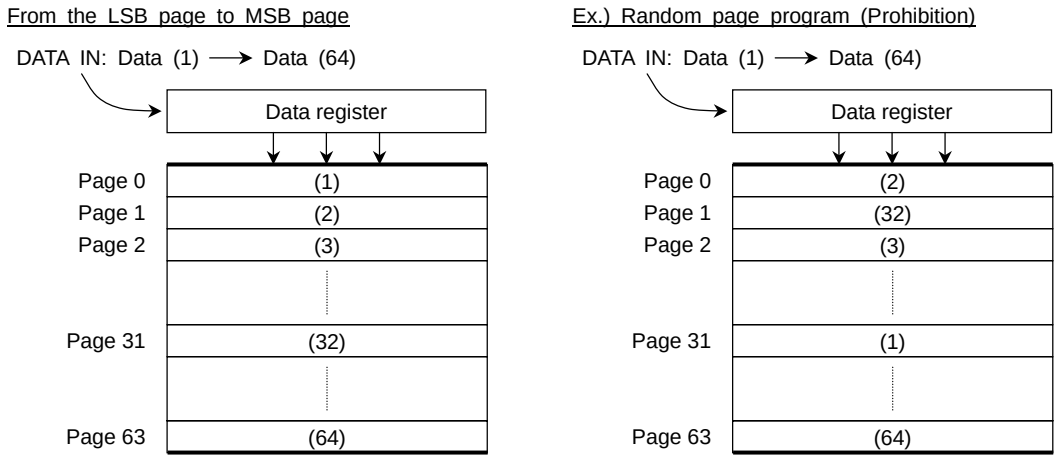


If a command other than "85h", "10h" or "FFh" is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

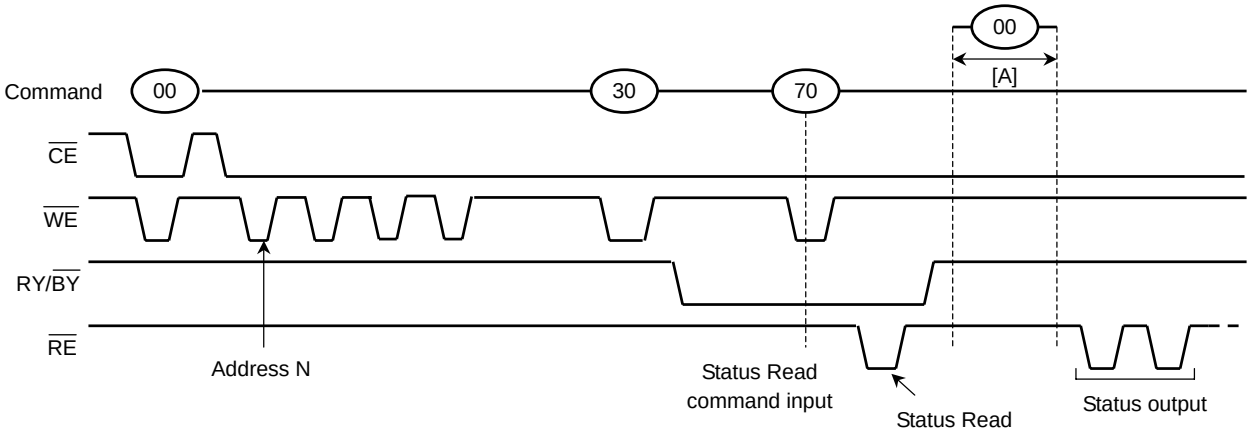


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

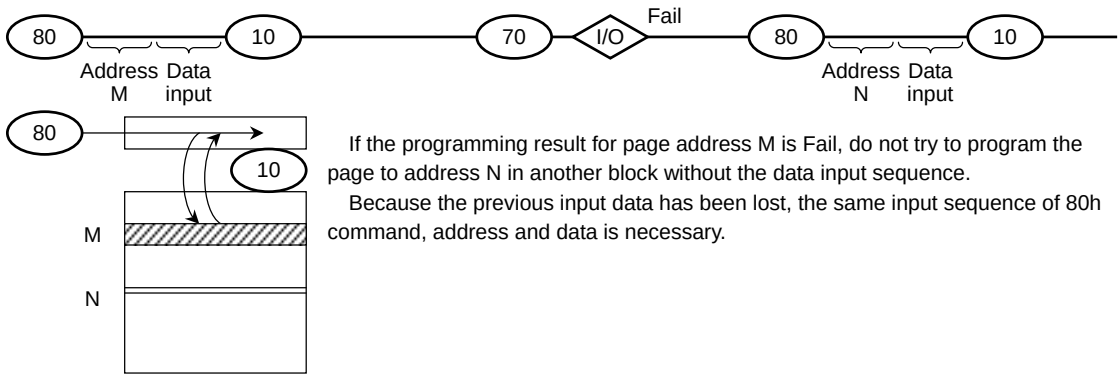


(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command "70h" in Read mode. Once the device has been set to Status Read mode by a "70h" command, the device will not return to Read mode unless the Read command "00h" is input during [A]. In this case, data output starts automatically from address N and address input is unnecessary.

(8) Auto programming failure

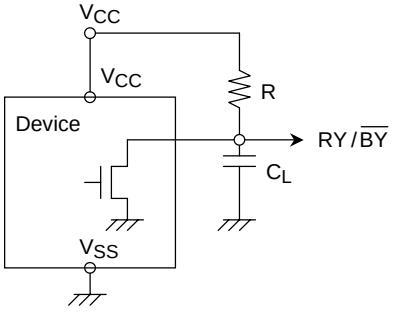


If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

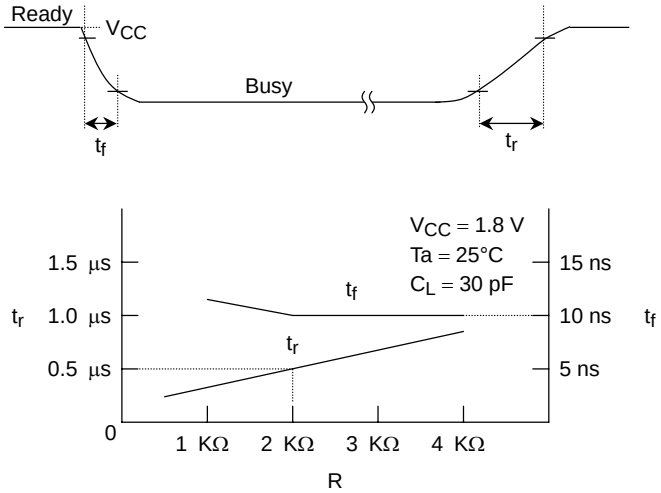
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.



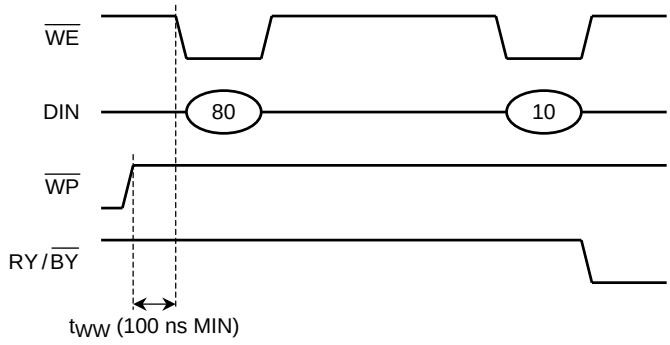
This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.



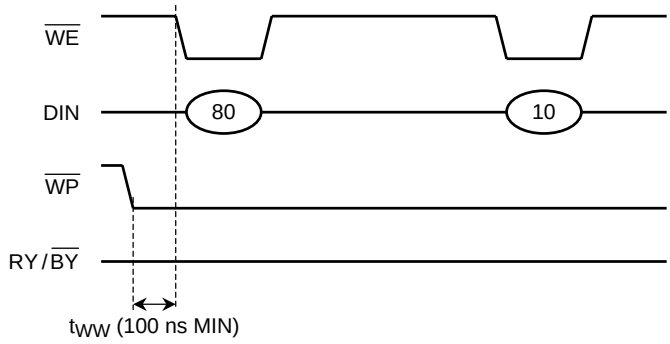
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

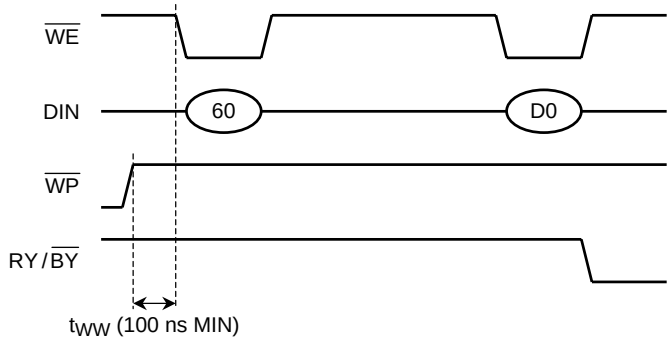
Enable Programming



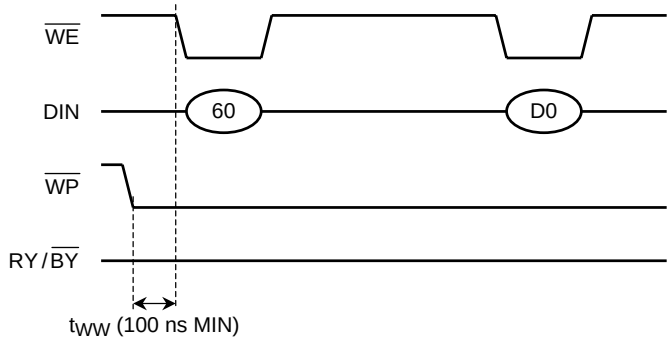
Disable Programming



Enable Erasing



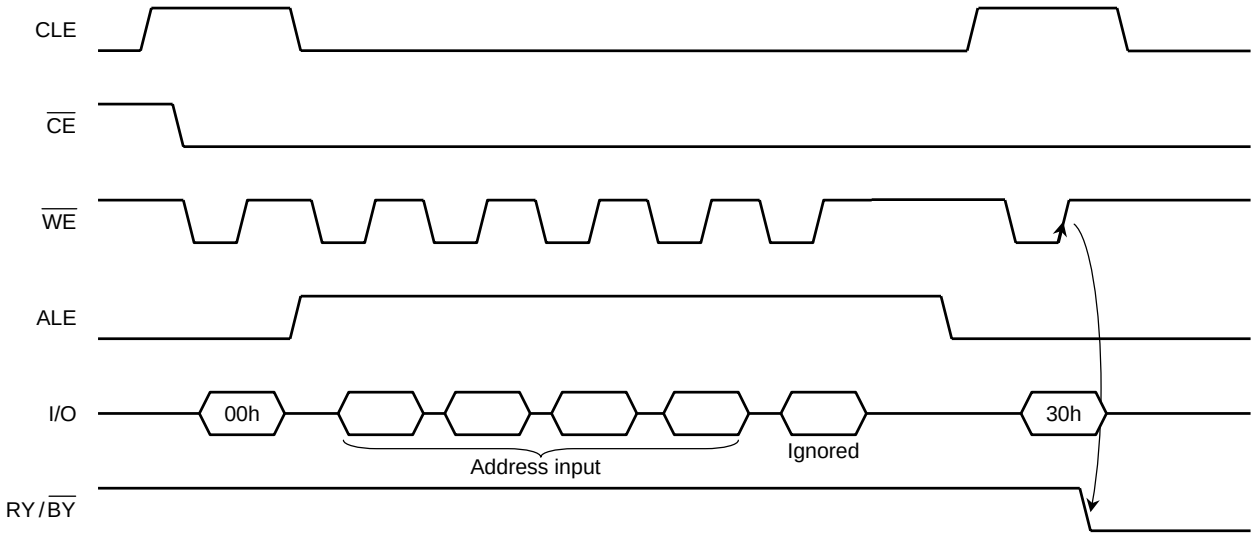
Disable Erasing



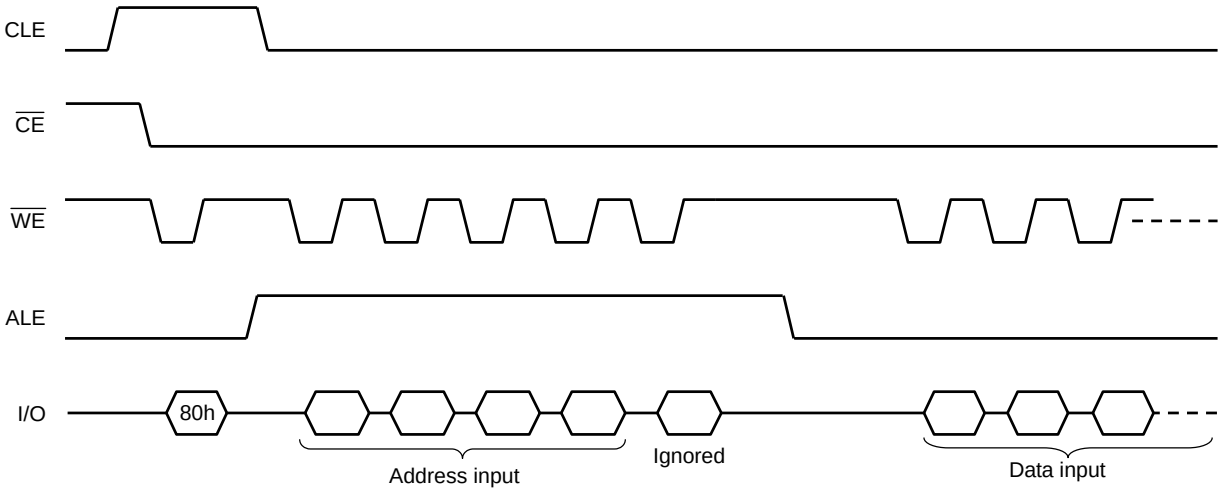
(11) When five address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

Read operation

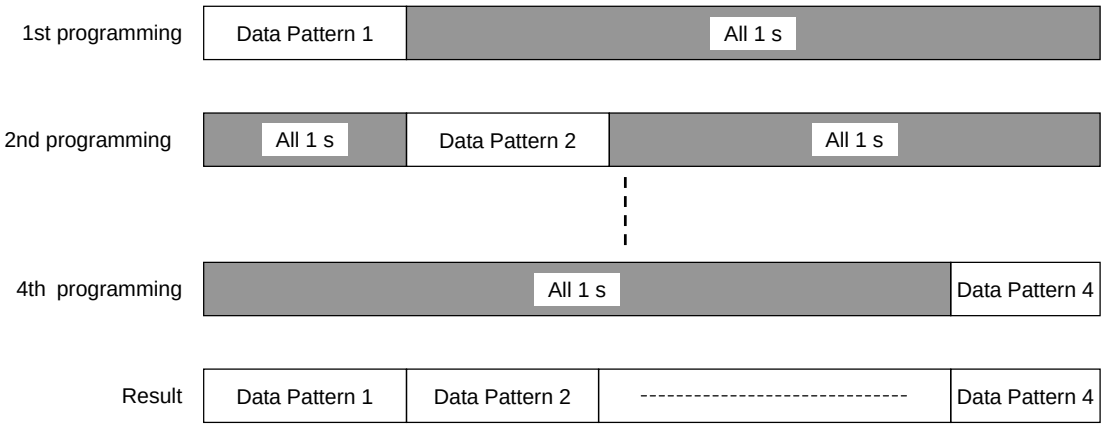


Program operation



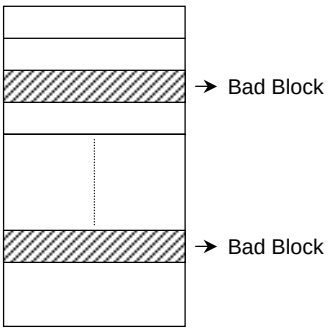
(12) Several programming cycles on the same page (Partial Page Program)

Each segment can be programmed individually as follows:



(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

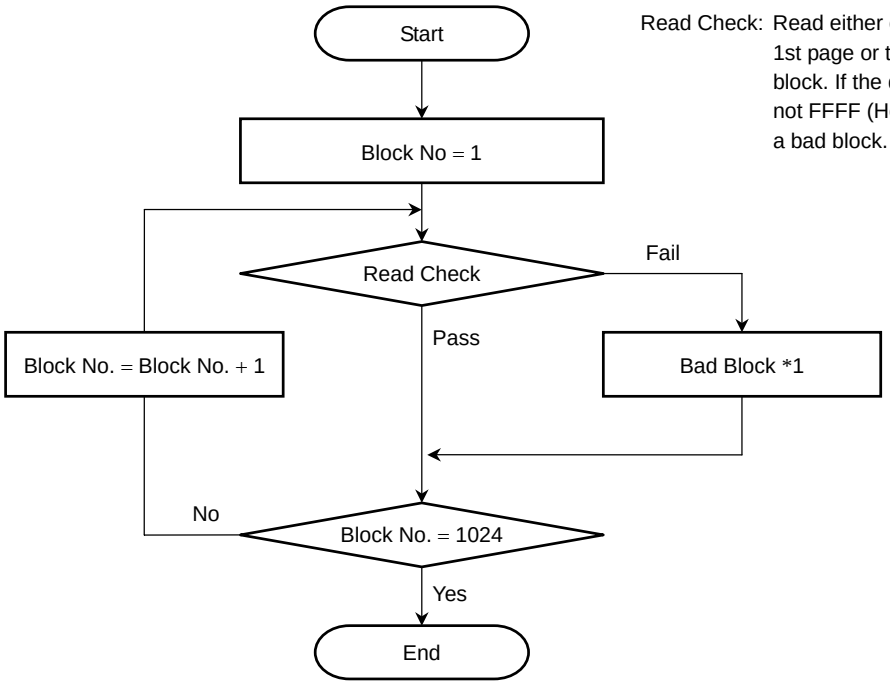
Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Block

Bad Block Test Flow



Read Check: Read either column 0 or 1024 of the 1st page or the 2nd page of each block. If the data of the column is not FFFF (Hex), define the block as a bad block.

*1: No erase operation is allowed to detected bad blocks

(14) Failure phenomena for Program and Erase operations

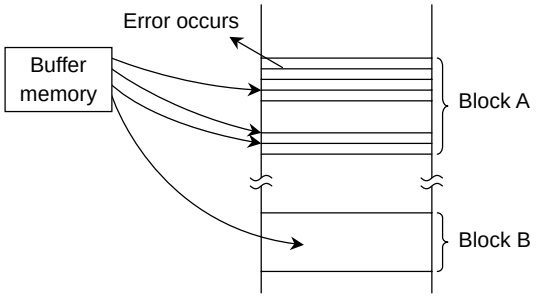
The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure “1 to 0”	ECC

- ECC: Error Correction Code. 2 bits per page is necessary.
  In case the 2 Kbytes page is divided into segments of 512 bytes, 1 bit correction per segment is necessary.

- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.