

Список литературы

- [1] Baldi, M, Corno, F, Rebaudengo, M, Reorda, M. S, & Squillero, G. (2000), eds. Corne, D, Smith, G, & Oates, M. J. (Wiley).
- [2] Corno, F, Reorda, M. S, & Squillero, G. (2000) Rt-level itc 99 benchmarks and first atpg results. pp. 44–53.
- [3] Corno, F, Prinetto, P, Rebaudengo, M, Reorda, M. S, & Squillero, G. (2002) Initializability analysis of synchronous sequential circuits.
- [4] Corno, F, Prinetto, P, Rebaudengo, M, Reorda, M. S, & Squillero, G. (1997) *A New Approach for Initialization Sequences Computation for Synchronous Sequential Circuits*. pp. 381–386.
- [5] Corno, F, Prinetto, P, Rebaudengo, M, Reorda, M. S, & Squillero, G. (1997) *A Genetic Algorithm for the Computation of Initialization Sequences for Synchronous Sequential Circuits*. pp. 56–61.
- [6] Baldi, M, Corno, F, Rebaudengo, M, Prinetto, P, Reorda, M. S, & Squillero, G. (1997) *Simulation-Based Verification of Network Protocols Performance*. pp. 236–251.
- [7] Baldi, M, Corno, F, Rebaudengo, M, & Squillero, G. (1997) *GA-based Performance Analysis of Network Protocols*. pp. 118–124.
- [8] Corno, F, Reorda, M. S, & Squillero, G. (1998) *The Selfish Gene Algorithm: a New Evolutionary Optimization Strategy*. pp. 349–355.
- [9] Corno, F, Reorda, M. S, & Squillero, G. (1998) *A New Evolutionary Algorithm Inspired by the Selfish Gene Theory*. pp. 575–580.
- [10] Corno, F, Reorda, M. S, & Squillero, G. (1998) *VEGA: A Verification Tool Based on Genetic Algorithms*. pp. 321–326.
- [11] Corno, F, Reorda, M. S, & Squillero, G. (1999) *Approximate Equivalence Verification of Sequential Circuits via Genetic Algorithms*.
- [12] Corno, F, Reorda, M. S, & Squillero, G. (1999) *Approximate Equivalence Verification for Protocol Interface Implementation via Genetic Algorithms*. pp. 182–192.
- [13] Corno, F, Reorda, M. S, & Squillero, G. (1999) *Optimizing Deceptive Functions with the SG-Clans Algorithm*. pp. 2190–2195.
- [14] Corno, F, Reorda, M. S, & Squillero, G. (1999) *Verifying the Equivalence of Sequential Circuits with Genetic Algorithms*. pp. 1293–1297.
- [15] Corno, F, Reorda, M. S, & Squillero, G. (1999) *Simulation-Based Sequential Equivalence Checking of RTL VHDL*. pp. 351–354.
- [16] Corno, F, Reorda, M. S, & Squillero, G. (1999) *High Quality Test Pattern Generation for RT-level VHDL Descriptions*.
- [17] Corno, F, Manzone, A, Pincetti, A, Reorda, M. S, & Squillero, G. (2000) *Automatic Test Bench Generation for Validation of RT-level Descriptions: an Industrial Experience*. pp. 385–389.
- [18] Corno, F, Reorda, M. S, & Squillero, G. (2000) *Automatic Validation of Protocol Interfaces Described in VHDL*. pp. 205–213.
- [19] Corno, F, Rebaudengo, M, Reorda, M. S, Squillero, G, & Violante, M. (2000) *Prediction of Power Requirements for High-Speed Circuits*. pp. 247–254.
- [20] Corno, F, Reorda, M. S, & Squillero, G. (2000) *Evolving Cellular Automata for Self-Testing Hardware*. pp. 31–39.
- [21] Corno, F, Reorda, M. S, & Squillero, G. (2000) *High-Level Observability for Effective High-Level ATPG*. pp. 411–416.

- [22] Corno, F, Rebaudengo, M, Reorda, M. S, Squillero, G, & Violante, M. (2000) *Low Power BIST via Hybrid Cellular Automata*. pp. 29–34.
- [23] Corno, F, Reorda, M. S, Squillero, G, & Violante, M. (2000) *CA-CSTP: A new BIST Architecture for Sequential Circuits*. pp. 167–172.
- [24] Corno, F, Reorda, M. S, & Squillero, G. (2000) *An Improved Cellular Automata-Based BIST Architecture for Sequential Circuits*. pp. 76–79.
- [25] Corno, F, Reorda, M. S, & Squillero, G. (2000) *Exploiting the Selfish Gene Algorithm for Evolving Hardware Cellular Automata*. pp. 1401–1406.
- [26] Corno, F, Reorda, M. S, & Squillero, G. (2000) *Exploiting the Selfish Gene Algorithm for Evolving Cellular Automata*.
- [27] Corno, F, Reorda, M. S, Squillero, G, & Violante, M. (2000) *A Genetic Algorithm-based System for Generating Test Programs for Microprocessor IP Cores*.
- [28] Corno, F, Reorda, M. S, & Squillero, G. (2001) *Evolving Effective CA/CSTP BIST Architectures for Sequential Circuits*.
- [29] Corno, F, Reorda, M. S, Squillero, G, & Violante, M. (2001) *On the Test of Microprocessor IP Cores*. pp. 209–213.
- [30] Corno, F, Cumani, G, Reorda, M. S, & Squillero, G. (2001) *ARPIA: a High-Level Evolutionary Test Signal Generator*.
- [31] Corno, F, Cumani, G, Reorda, M. S, & Squillero, G. (2001) *Effective Techniques for High-Level ATPG*.
- [32] Corno, F, Cumani, G, Reorda, M. S, & Squillero, G. (2001) *Devising an RT-Level ATPG for uProcessor Cores*.
- [33] Corno, F, Reorda, M. S, & Squillero, G. (2002) *An Evolutionary Algorithm for Reducing Integrated-Circuit Test Application Time*. pp. 608–611.
- [34] Corno, F, Cumani, G, Reorda, M. S, & Squillero, G. (2002) *Automatic Test Program Generation from RT-level microprocessor descriptions*.
- [35] Corno, F, Reorda, M. S, & Squillero, G. (2002) *Evolutionary Techniques for Minimizing Test Signals Application Time*.
- [36] Corno, F, Cumani, G, Reorda, M. S, & Squillero, G. (2002) *Efficient Machine-Code Test-Program Induction*.