Список литературы

- [1] KOZA, J. R. et al., Use of conditional developmental operators and free variables in automatically synthesizing generalized circuits using genetic programming, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 5–16, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [2] LEVI, D., Hereboy: A fast evolutionary algorithm, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 17–24, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [3] SEOK, H. et al., Genetic programming of process decomposition strategies for evolvable hardware, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 25–34, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [4] POLLACK, J. et al., The golem project: Evolving hardware bodies and brains, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 37–42, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [5] Bennett III, F. H. et al., Design of decentralized controllers for self-reconfigurable modular robots using genetic programming, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 43–52, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [6] VASSILEV, V. et al., Scalability problems of digital circuit evolution: Evolvability and efficient designs, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 55–64, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [7] KALGANOVA, T., Bidirectional incremental evolution in extrinsic evolvable hardware, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 65–74, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [8] IMAMURA, K. et al., Bidirectional incremental evolution in extrinsic evolvable hardware, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 75–80, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [9] MASNER, J. et al., Size versus robustness in evolved sorting networks: Is bigger better?, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 81–87, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [10] ZEBULUM, R. et al., A reconfigurable platform for the automatic synthesis of analog circuits, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 91–98, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [11] STOICA, A. et al., Evolution of analog circuits on field programmable transistor arrays, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 99–108, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [12] THOMPSON, A. et al., Evolutionary design of single electron systems, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 109–116, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.

- [13] FLOCKTON, S. et al., Behavior of a building block for intrinsic evolution of analogue signal shaping and filtering circuits, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 117–124, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [14] MARSTON, N. et al., An evolutionary approach to ghz digital systems, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 125–131, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [15] JONATHAN, M. et al., Multiobjective optimization techniques: A study of the energy minimization method and its application to the synthesis of ota amplifiers, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 133–140, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [16] TUFTE, G. et al., Evolving an adaptive digital filter, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 143–150, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [17] COELLO, C. et al., Evolutionary multiobjective design of combinational logic circuits, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 161–170, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [18] KORKIN, M. et al., Evolving hardware on a large scale, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 173–182, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [19] LEE, C. et al., Self-repairable eplds: Design, self-repair, and evaluation methodology, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 183–194, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [20] HOLLINGWORTH, G. et al., Safe intrinsic evolution of virtex devices, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 195–202, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [21] MANGE, D. et al., Toward self-repairing and self-replicating hardware: The embryonics approach, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 205– 214, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [22] BRADLEY, D. et al., Embryonics + immunotronics: A bio-inspired approach to fault tolerance, in The Second NASA/DoD workshop on Evolvable Hardware, edited by LOHN, J. et al., pages 205– 224, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [23] de Garis, H. et al., Building multimodule systems with unlimited evolvable capacities from modules with limited evolvable capacities (mecs), in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 225–234, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [24] LEVY, R. et al., Slate of the art: An evolving fpga-based board for handwritten-digit recognition, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 237–244, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [25] TORRESEN, J., Scalable evolvable hardware applied to road image recognition, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 245–252, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.

- [26] YASUNAGA, M. et al., Kernel-based pattern recognition hardware: Its design methodology using evolved truth tables, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 253–262, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [27] MILANO, M. et al., A clustering genetic algorithm for actuator optimization in flow control, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by LOHN, J. et al., pages 263–270, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.