

Список литературы

- [1] Koza, J. R., Yu, J., Keane, M. A., and Mydlowec, W., Use of conditional developmental operators and free variables in automatically synthesizing generalized circuits using genetic programming, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 5–16, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [2] Levi, D., Herebooy: A fast evolutionary algorithm, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 17–24, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [3] Seok, H., Lee, K., Zhang, B., Lee, D., and Sim, K., Genetic programming of process decomposition strategies for evolvable hardware, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 25–34, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [4] Pollack, J. and Lipson, H., The golem project: Evolving hardware bodies and brains, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 37–42, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [5] Bennett III, F. H. and Rieffel, E., Design of decentralized controllers for self-reconfigurable modular robots using genetic programming, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 43–52, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [6] Vassilev, V. and Miller, J., Scalability problems of digital circuit evolution: Evolvability and efficient designs, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 55–64, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [7] Kalganova, T., Bidirectional incremental evolution in extrinsic evolvable hardware, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 65–74, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [8] Imamura, K., Foster, J., and Krings, A., Bidirectional incremental evolution in extrinsic evolvable hardware, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 75–80, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [9] Masner, J., Cavalieri, J., Frenzel, J., and Foster, J., Size versus robustness in evolved sorting networks: Is bigger better?, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 81–87, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [10] Zebulum, R. et al., A reconfigurable platform for the automatic synthesis of analog circuits, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 91–98, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [11] Stoica, A. et al., Evolution of analog circuits on field programmable transistor arrays, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 99–108, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [12] Thompson, A. and Wasshuber, C., Evolutionary design of single electron systems, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 109–116, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.

- [13] Flockton, S. and Sheehan, K., Behavior of a building block for intrinsic evolution of analogue signal shaping and filtering circuits, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 117–124, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [14] Marston, N. et al., An evolutionary approach to ghz digital systems, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 125–131, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [15] Jonathan, M., Zebulum, R., Pacheco, M., and Vellasco, M., Multiobjective optimization techniques: A study of the energy minimization method and its application to the synthesis of ota amplifiers, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 133–140, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [16] Tufte, G. and Haddow, P., Evolving an adaptive digital filter, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 143–150, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [17] Coello, C., Aguirre, A., and Buckles, B., Evolutionary multiobjective design of combinational logic circuits, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 161–170, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [18] Korkin, M., Fehr, G., and Jeffery, G., Evolving hardware on a large scale, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 173–182, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [19] Lee, C., Hall, D., Perkowski, M., and Jun, D., Self-repairable eplds: Design, self-repair, and evaluation methodology, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 183–194, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [20] Hollingworth, G., Smith, S., and Tyrrell, A., Safe intrinsic evolution of virtex devices, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 195–202, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [21] Mange, D., Sipper, M., Stauffer, A., and Tempesti, G., Toward self-repairing and self-replicating hardware: The embryonics approach, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 205–214, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [22] Bradley, D., Ortega-Sanchez, C., and Tyrrell, A., Embryonics + immunotronics: A bio-inspired approach to fault tolerance, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 205–224, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [23] de Garis, H. et al., Building multimodule systems with unlimited evolvable capacities from modules with limited evolvable capacities (mecs), in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 225–234, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [24] Levy, R., Lepri, S., Sanchez, E., Ritter, G., and Sipper, M., Slate of the art: An evolving fpga-based board for handwritten-digit recognition, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 237–244, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.

- [25] Torresen, J., Scalable evolvable hardware applied to road image recognition, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 245–252, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [26] Yasunaga, M., Nakamura, T., Yoshihara, I., and Kim, J., Kernel-based pattern recognition hardware: Its design methodology using evolved truth tables, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 253–262, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.
- [27] Milano, M. and Koumoutsakos, P., A clustering genetic algorithm for actuator optimization in flow control, in *The Second NASA/DoD workshop on Evolvable Hardware*, edited by Lohn, J., Stoica, A., and Keymeulen, D., pages 263–270, Palo Alto, California, 2000, Jet Propulsion Laboratory, California Institute of Technology, IEEE Computer Society.