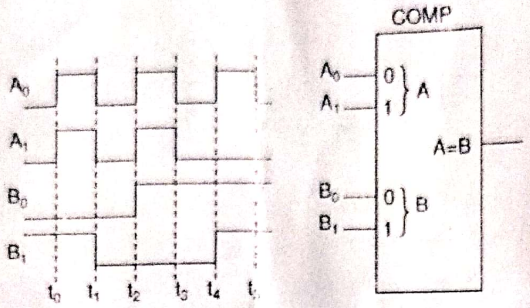
(End Semester Exam - Mon... Maximum Marks: 40

Duration: 3 Hours

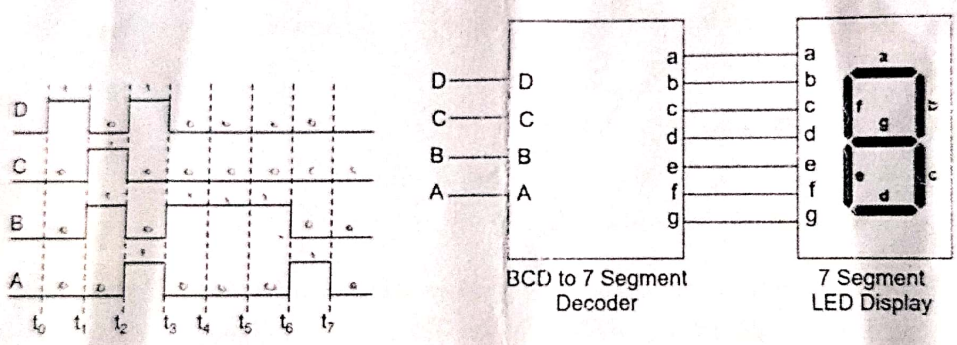
Instructions: • Answer all questions
• Assume missing data suitably, by clearly stating the assumption

1. In a digital system a 4-bit BCD adder is needed. Design a 4-bit BCD adder using 4-bit binary adders and other necessary gates (3 marks)

2. A 2-bit comparator which compares two input $A(= A_1A_0)$ and $B(= B_1B_0)$ is shown in the figure. The waveforms applied to the comparator are as given. Determine the output $(A = B)$ waveform for the time duration t_0 to t_5. (2 marks)



3. A 7-segment decoder with $ABCD$ as the BCD input (A as MSB and D as LSB) drives the display in the figure. If the waveforms are applied as indicated, determine the sequence of digits that appears on the display for $t_0 < t \leq t_7$. (2 marks)



4. Find the Boolean expressions to convert the binary number $B_2B_1B_0$ to gray code. Realize the code converter with exclusive- OR gates. (3 marks)

5. (a) Design a decimal to BCD encoder with active high output.

(b) For the decimal to BCD encoder, if the input 9 and input 2 become HIGH simultaneously what will be output code? Is it a valid BCD code? (2+1=3 marks)

6. Realize the following Boolean functions using 8:1 MUX and NOT gate

(a) $F(A, B, C, D) = \sum(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$

(b) $F = ABC + BCD + CDA + DAB$ ($2 \times 2 = 4$ marks)

7. Implement a positive edge triggered master-slave D flip flop using D latches. Suggest a method to convert it into a negative edge triggered master-slave D flip flop (3 marks)

[P.T.O.]

8. (a) Express the characteristic tables of flip-flops AB and XY given below as characteristic equations.

i)

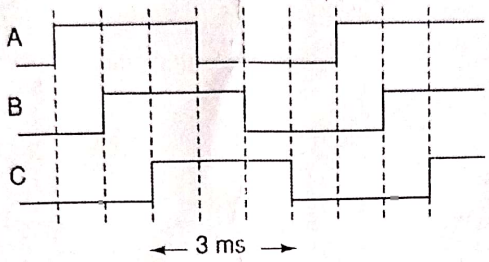
A	B	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'

ii)

X	Y	Q^+
0	0	Q
0	1	1
1	0	Q'
1	1	0

(b) Realize the flip flops AB and XY (mentioned in 8(a)) using D flip flops (1+2=3 marks)

9. Generate the waveforms A, B and C using three D Flip Flops only. You are given a clock signal of 1 kHz. (2 marks)



10. The decimal equivalent of the largest number a binary ripple counter can count is 4095. What should be the clock frequency at the input to the counter if it is necessary to obtain a frequency of 550 Hz at the output of the most significant stage ? Neglect propagation delays. (2 marks)

11. Design a controlled synchronous counter using JK flip flops such that when control signal M=0, it will act a mod-5 counter producing the sequence....0,1,2,3,4,0,1,2.....and when the control signal M=1 it will act a mod-7 counter producing the sequence ....0,1,2,3,4,5,6,0,1,2.... (6 marks)

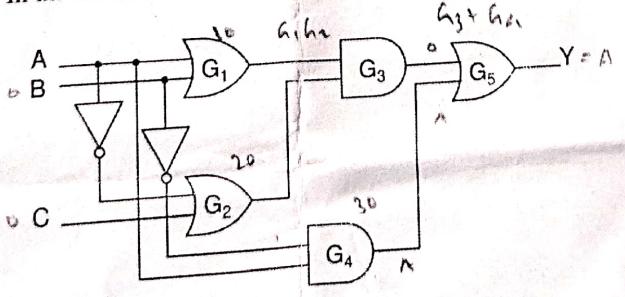
12. A Mealy state machine checks an input bit sequence X and produces an output Z which will be high when a overlapping sequence 1010 is detected.

(a) Obtain the state diagram of the state machine.

(b) Using normal binary encoding of states, obtain the state table.

(c) Find the output Z for the input sequence 00010101001110. (2+1+1=4 marks)

13. In the following circuit gates G_1, G_2 and G_4 has a propagation delays of 10 ns, 20ns and 30ns respectively. The other gates have no delay. In the circuit $B = C = 0$ (always) and A changes from 0 to 1 at time t=10ns.



(a) Obtain the timing wavefroms of the outputs of G_1, G_2, G_3, G_4 and G_5 for $0 < t \leq 60$ns

(b) Does the output Y suffer from a hazard. If so mention the type of hazard and mention the reason for such a hazard. (2+1=3 marks)