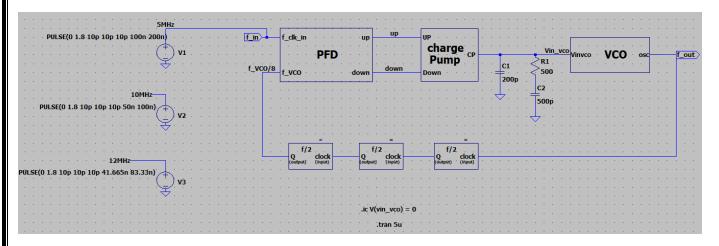


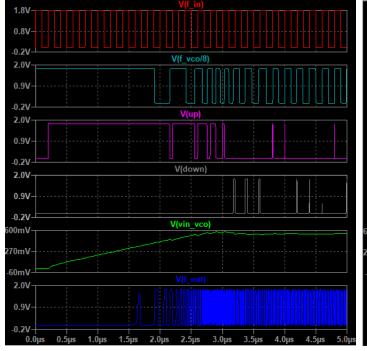
Final Report

Submitted by – Paras Sanjay Gidd

Block Diagram:



For Input frequency(f_in) = 5MHz



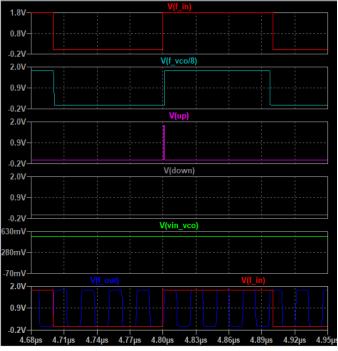


Fig: waveforms at each nodes of PLL

Fig: waveforms at each nodes of PLL (magnified)

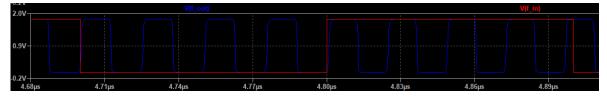
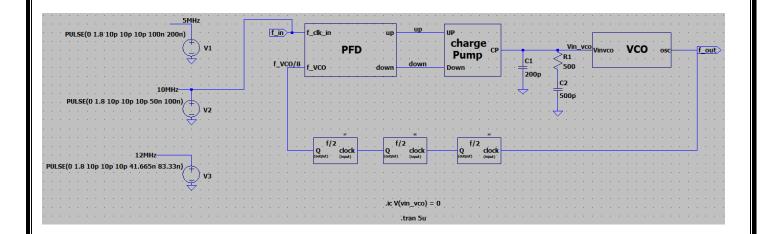


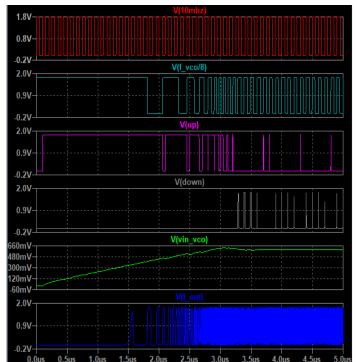
Fig: waveform showing Input output comparison

Result:

	<mark>MHz</mark>
Output Frequency (f_out) 39	<mark>9.73MHz</mark>

2. For Input frequency(f_in) = 10MHz





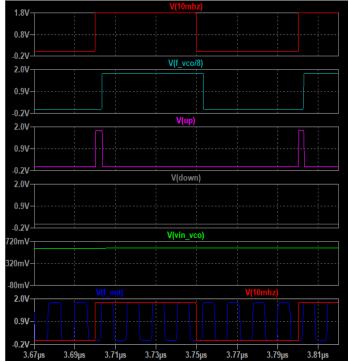


Fig: waveforms at each nodes of PLL

Fig: waveforms at each nodes of PLL (magnified)

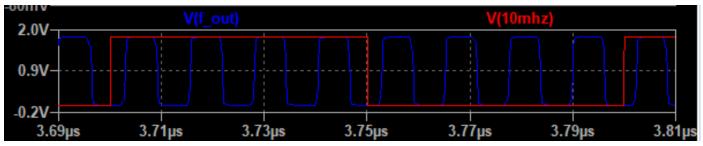
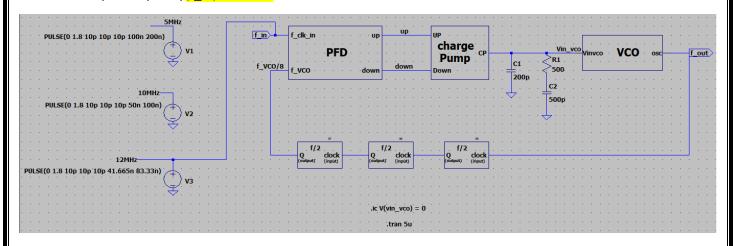


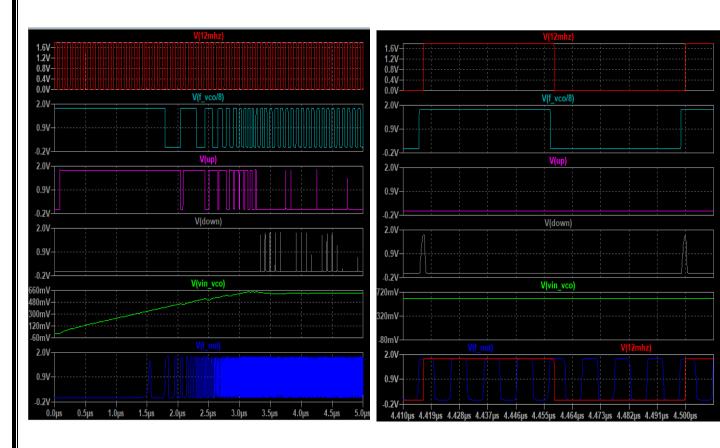
Fig: waveform showing Input output comparison

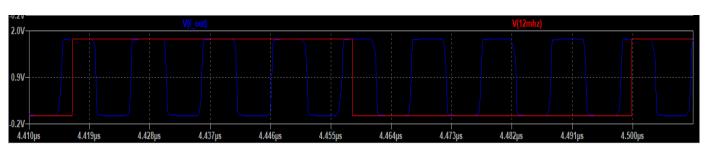
Result:

Input frequency <mark>(f_in)</mark>	10MHz
Output Frequency <mark>(f_out)</mark>	80.91MHz

3. For Input frequency(f_in) = 12MHz







Result:

Input frequency <mark>(f_in)</mark>	12MHz
Output Frequency <mark>(f_out)</mark>	96.1 MHz