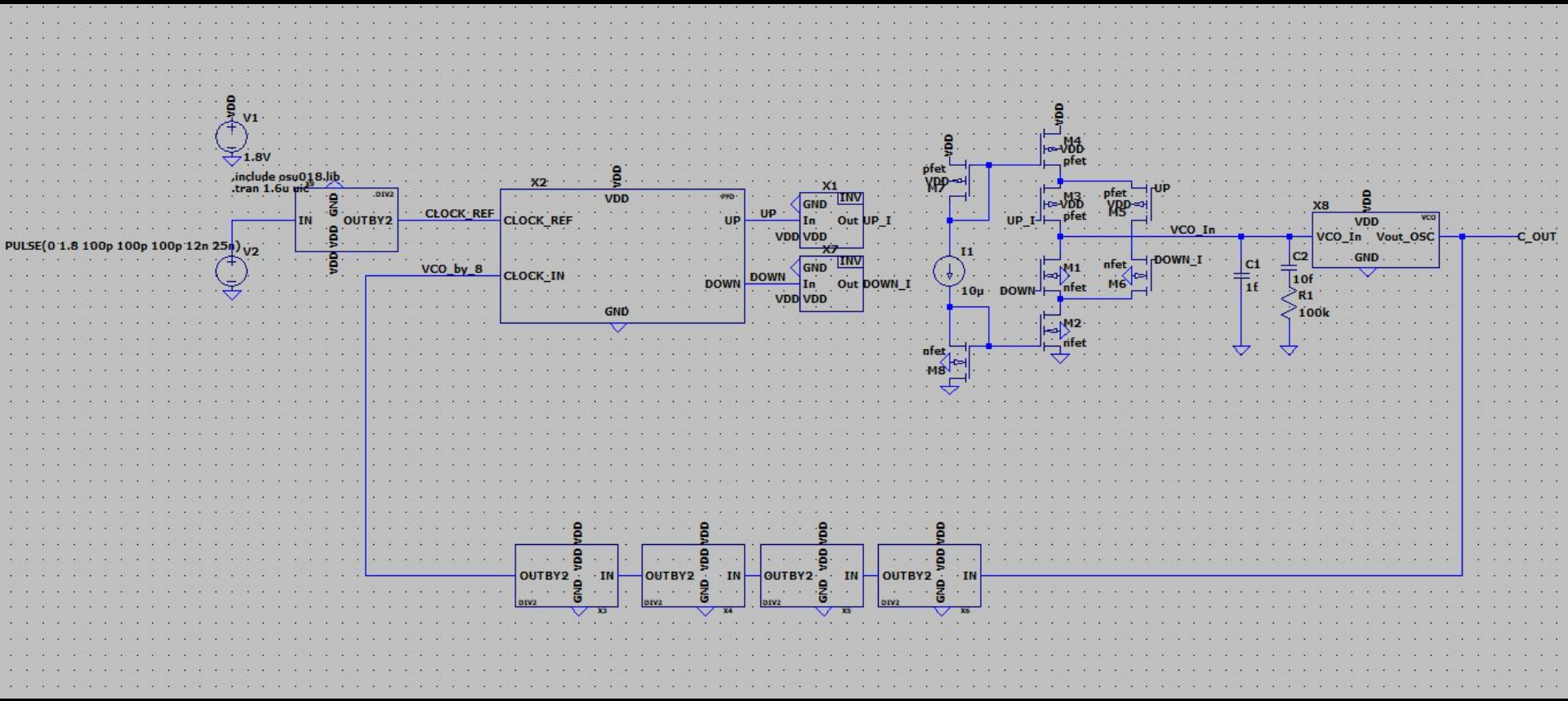
STAGE 2 REPORT
On chip PLL

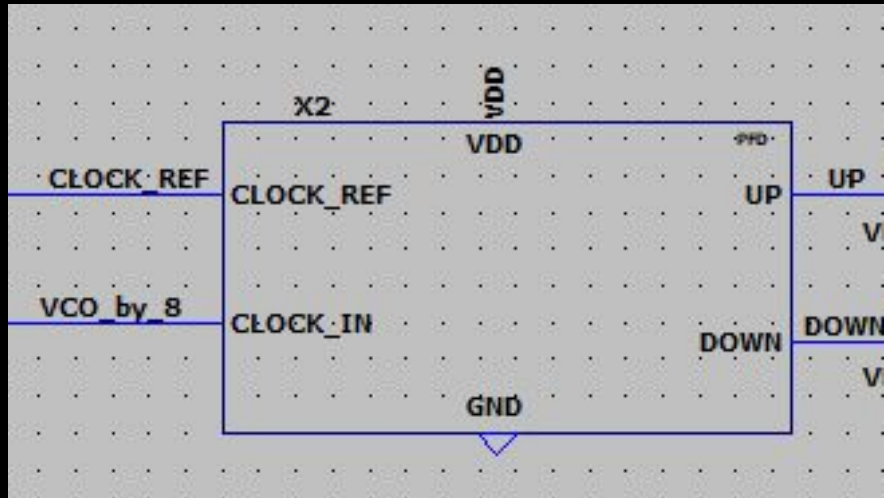
For clock generation


V1
1.8V
.include osu018.lib
.tran 1.6u uic
PULSE(0 1.8 100p 100p 100p 12n 25n)
V2
IN
OUTBY2
CLOCK_REF
VCO_by_8
X2
CLOCK_REF
CLOCK_IN
UP
DOWN
X1
X7
INV
UP_I
DOWN_I
I1
10µ
M1
M2
M3
M4
M5
M6
M7
M8
pfet
nfet
VCO_In
C1
1f
C2
10f
R1
100k
X8
Vout_OSC
C_OUT
X3
X4
X5
X6

PFD

Detects the difference in phase and frequency difference between the external clock and generated clock.

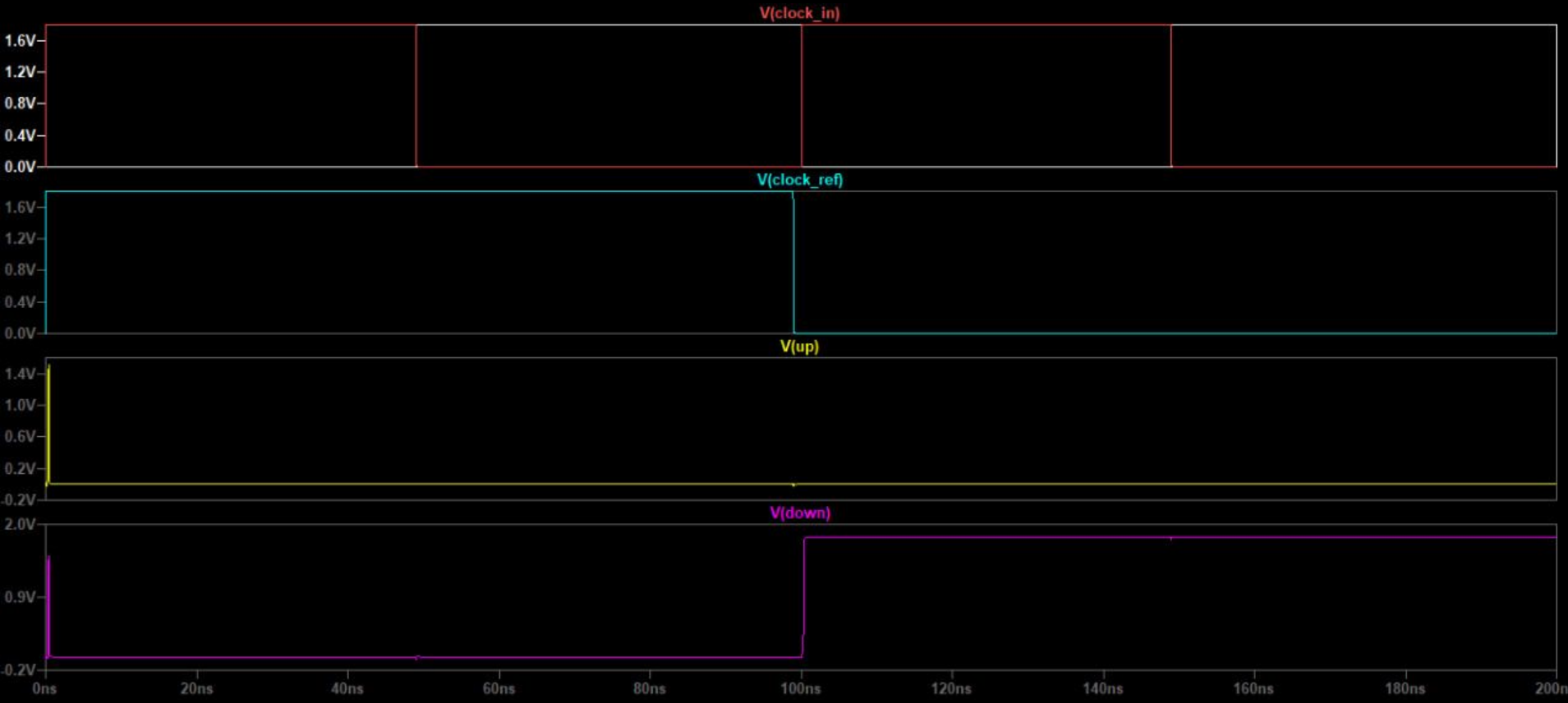
When there is negligible phase difference and the frequency is identical, the PLL is in the locked state.



Fin < Fref


V(clock_in)
1.6V
1.2V
0.8V
0.4V
0.0V
V(clock_ref)
1.6V
1.2V
0.8V
0.4V
0.0V
V(up)
2.0V
0.9V
-0.2V
V(down)
1.4V
1.0V
0.6V
0.2V
-0.2V
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns

Fin > Fref


V(clock_in)
1.6V
1.2V
0.8V
0.4V
0.0V
V(clock_ref)
1.6V
1.2V
0.8V
0.4V
0.0V
V(up)
1.4V
1.0V
0.6V
0.2V
-0.2V
V(down)
2.0V
0.9V
-0.2V
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns

Fin = Fref

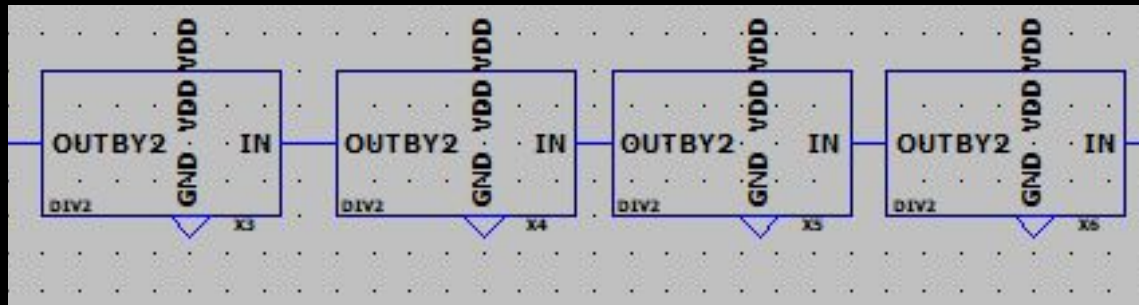

V(clock_in)
1.6V
1.2V
0.8V
0.4V
0.0V
V(clock_ref)
1.6V
1.2V
0.8V
0.4V
0.0V
V(up)
1.4V
1.0V
0.6V
0.2V
-0.2V
V(down)
1.4V
1.0V
0.6V
0.2V
-0.2V
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns

Divide By 2 and 16

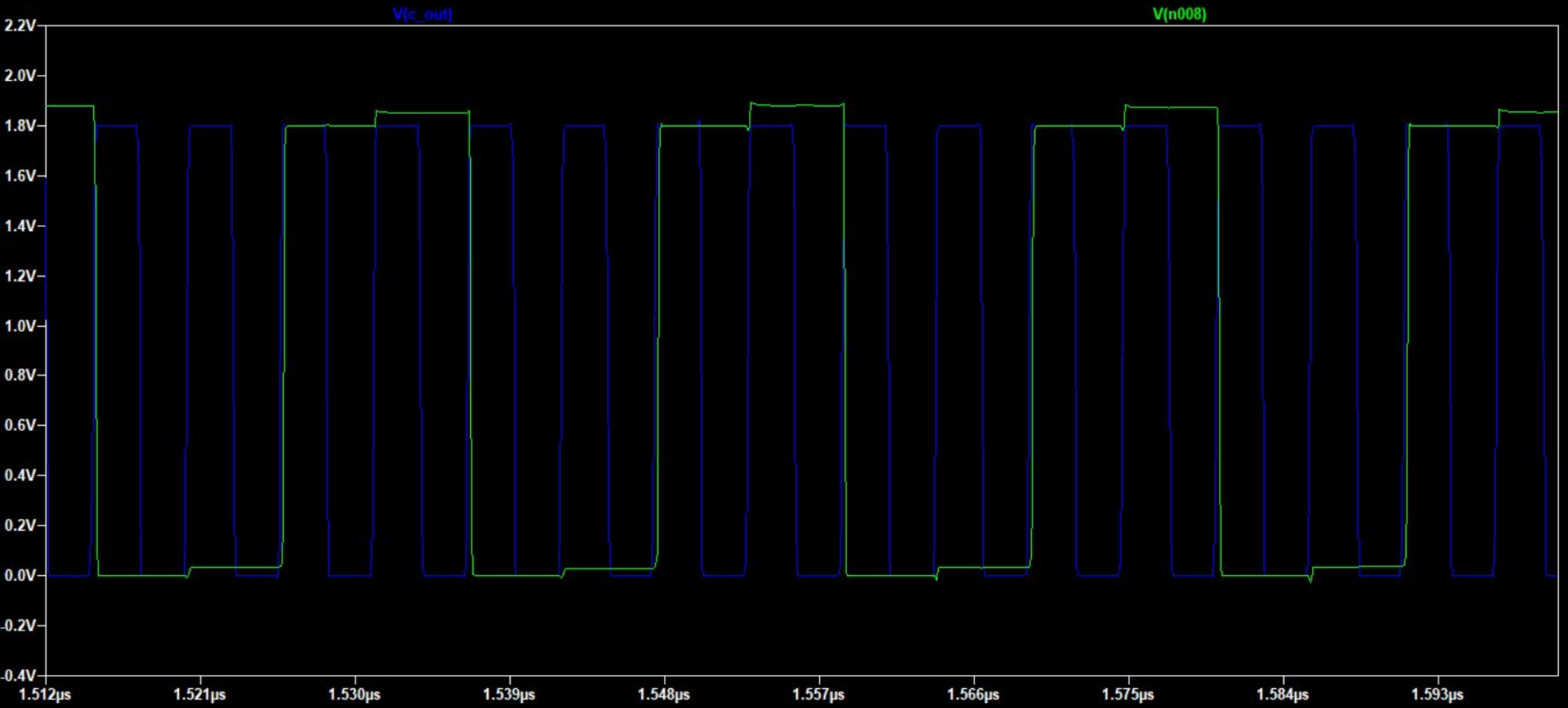
-> DFF divides the frequency by 2 or multiplies the time period by 2.

-> The output of the VCO is divided by 2 for 4 times.

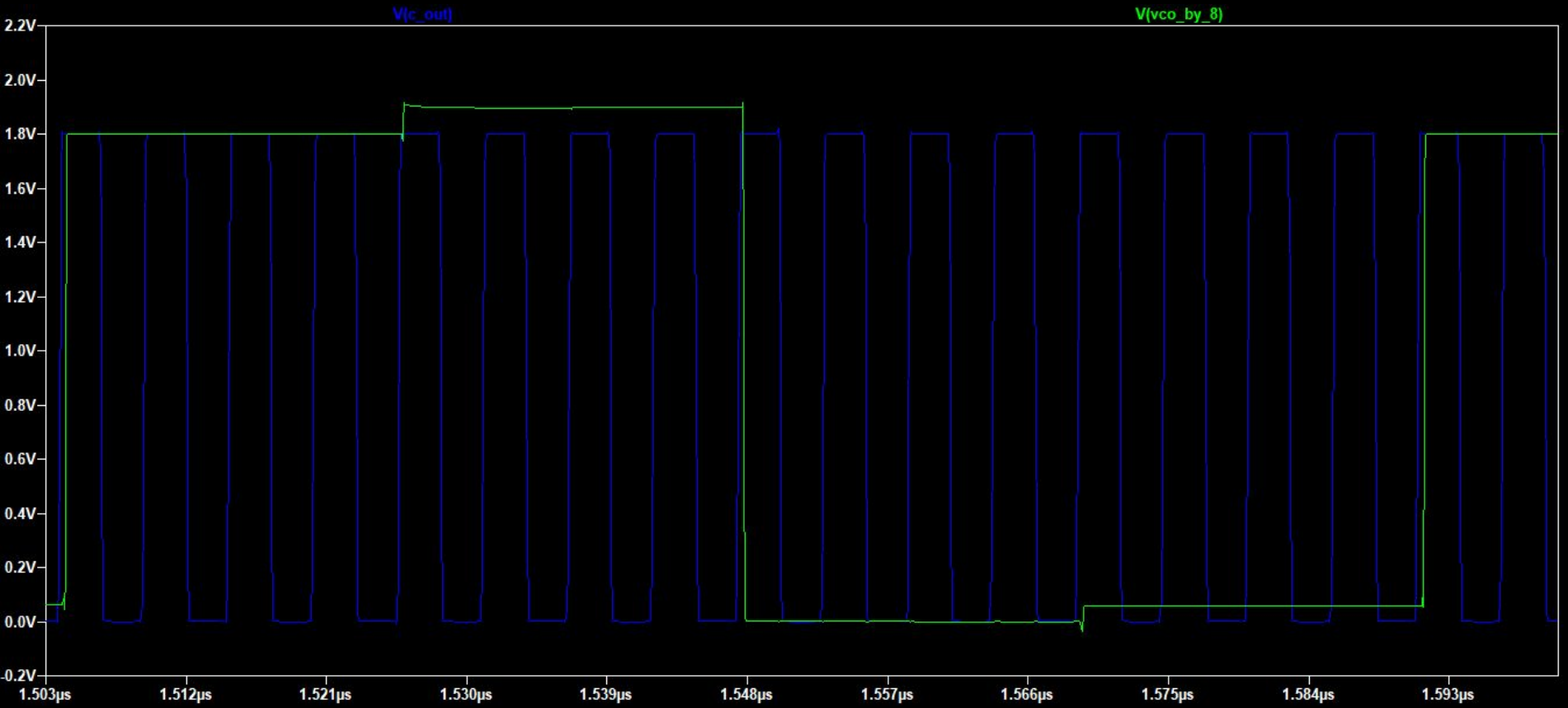
-> Resulting in a constant×8 multiplication of the PLL clock output.



Div2


V(c_out)
V(n008)
2.2V
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
1.512µs
1.521µs
1.530µs
1.539µs
1.548µs
1.557µs
1.566µs
1.575µs
1.584µs
1.593µs

Div16


V(c_out)
V(vco_by_8)
2.2V
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
1.503µs
1.512µs
1.521µs
1.530µs
1.539µs
1.548µs
1.557µs
1.566µs
1.575µs
1.584µs
1.593µs

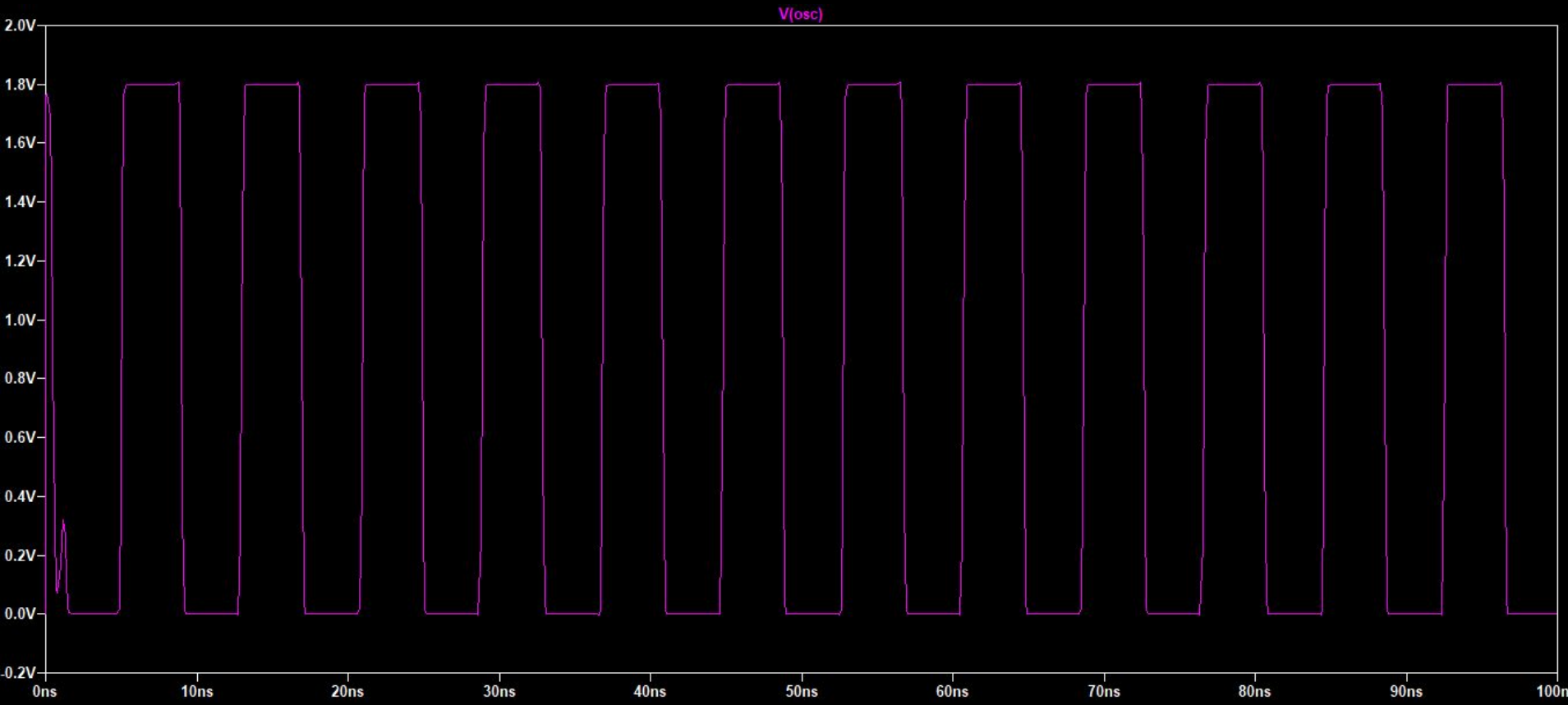
VCO

-> Generates an output frequency proportional to the input voltage.

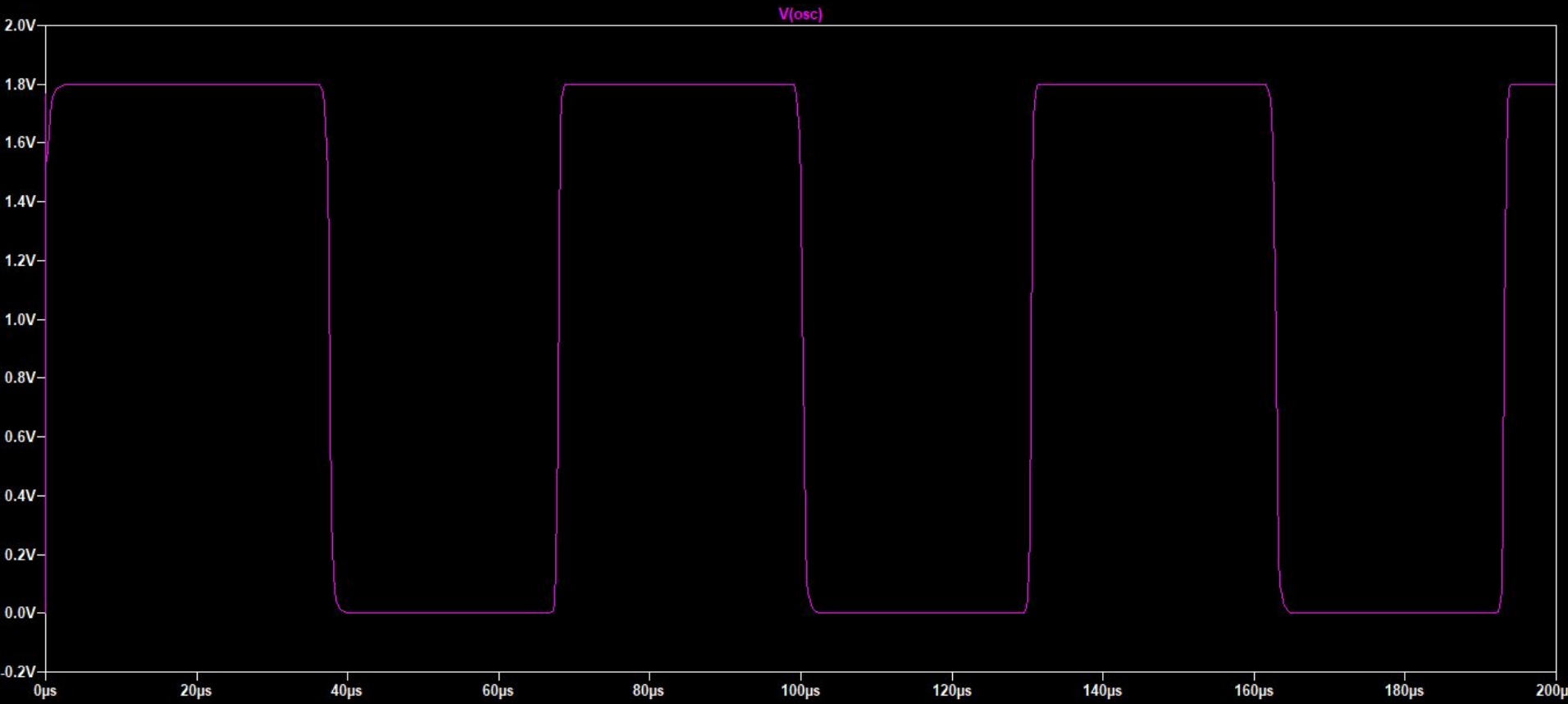
-> In PLL this is the error voltage generated by the PD.

-> Ring oscillator

100 Mhz - VCO at 1.2V



16KHz - VCO at 0.2V

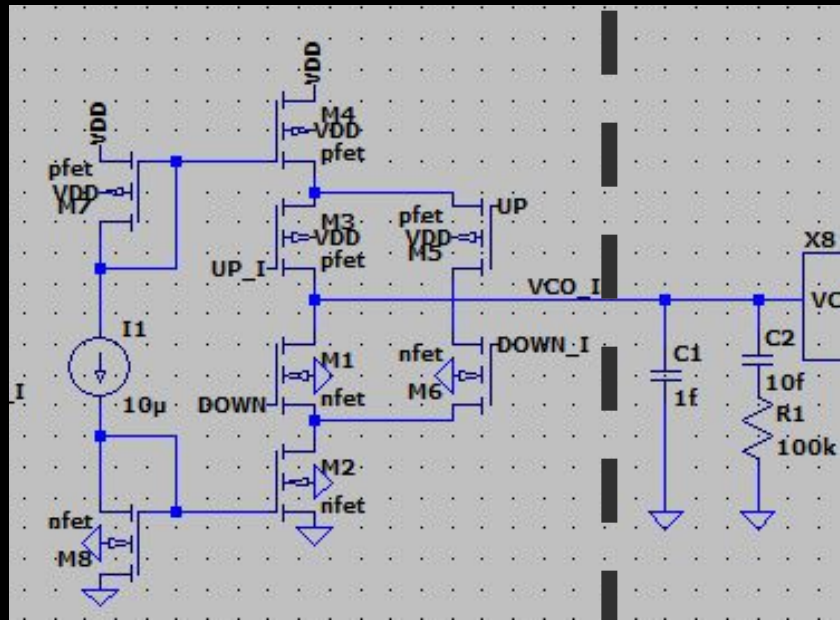


Loop Filter & Charge Pump

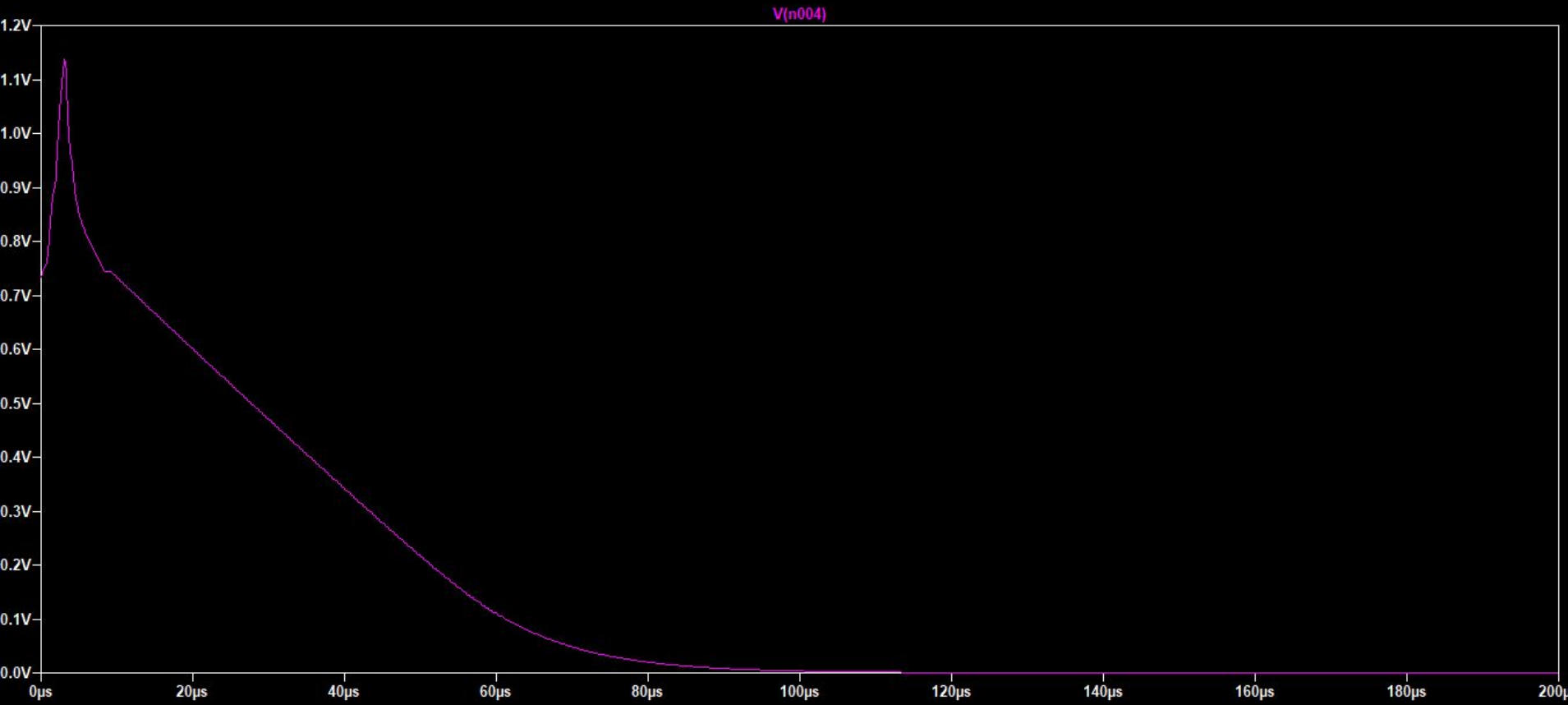
-> Charge pump generates voltage greater than VDD (less than GND).

-> Loop filter integrates the charge supplied by the charge pump.

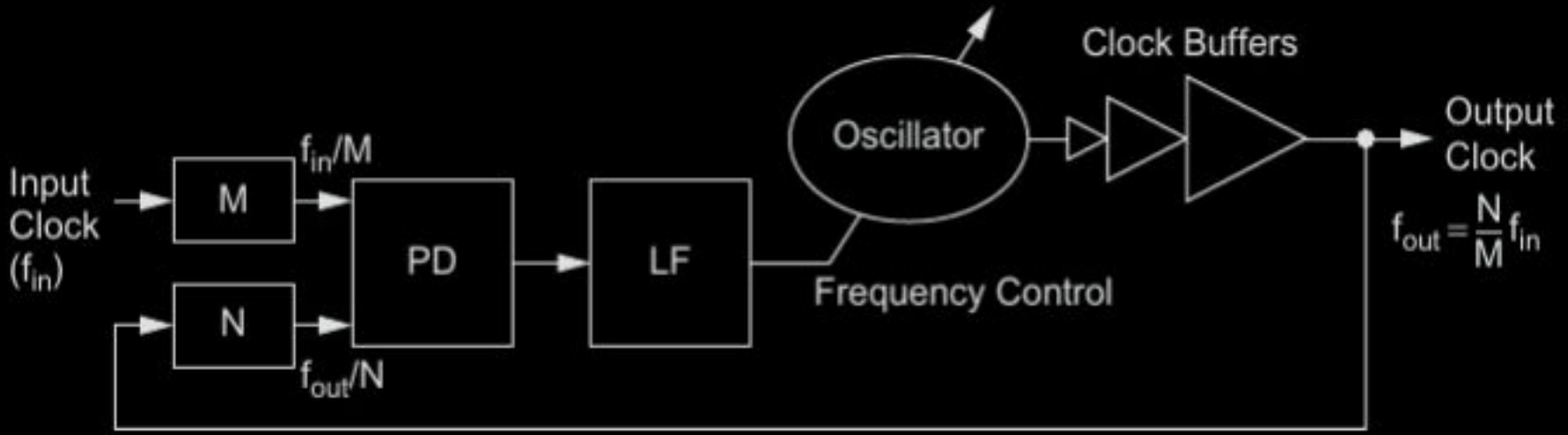
-> Loop filter helps in achieving phase lock.



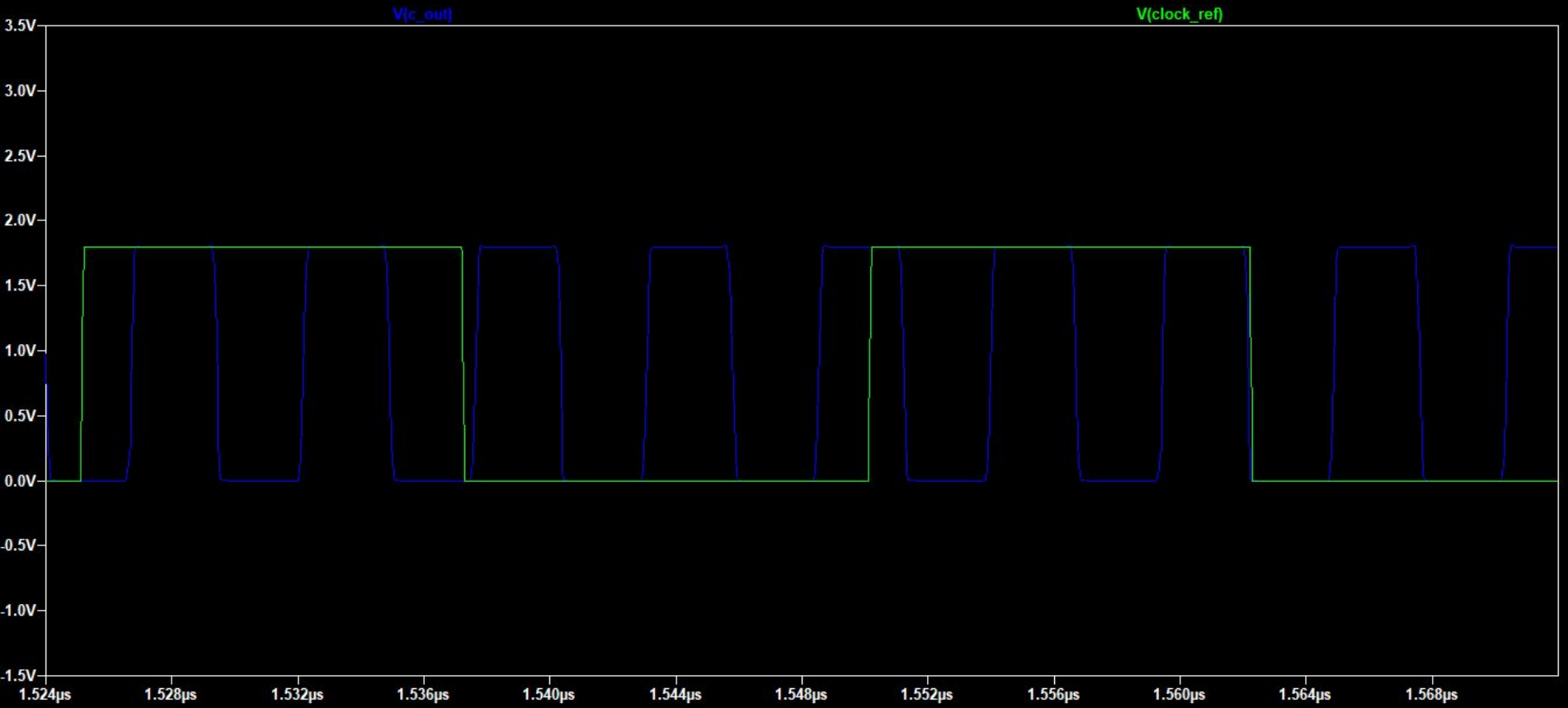
Vpump for same input



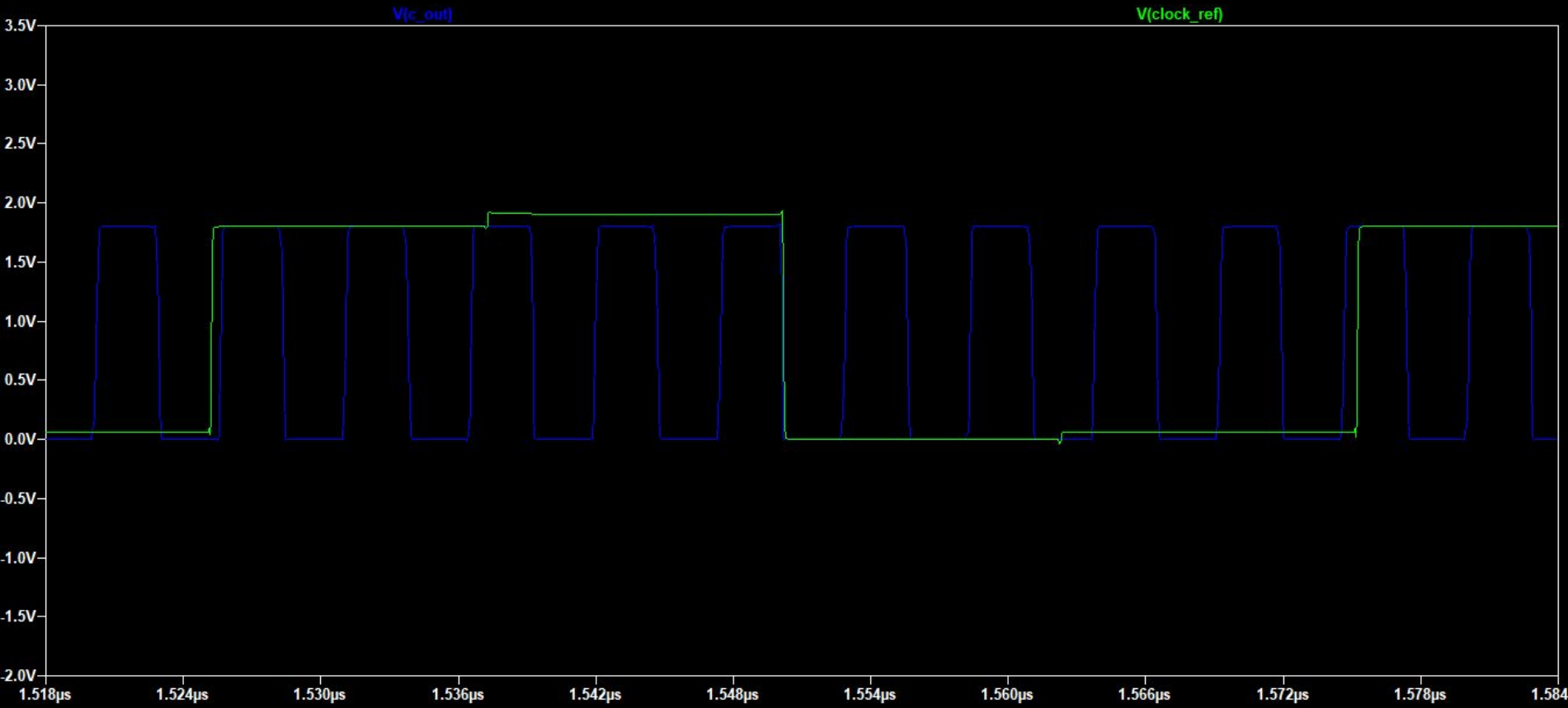
50% duty cycle and phase match



Input not divided by 2



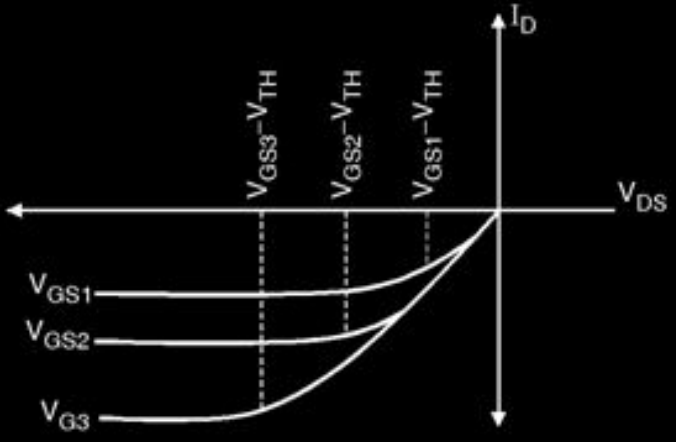
Input divided by 2



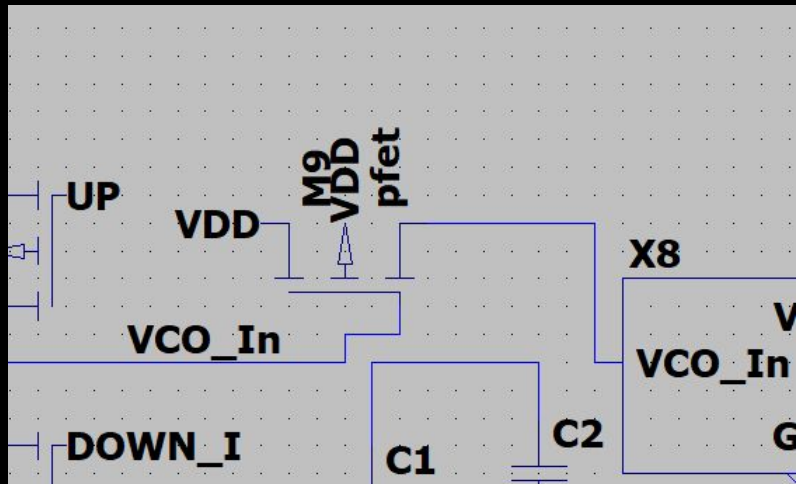
Leaky Bucket Theory

-> Loop filter prevents voltage jumps on the input of the VCO and thus frequency jumps in the PLL output.

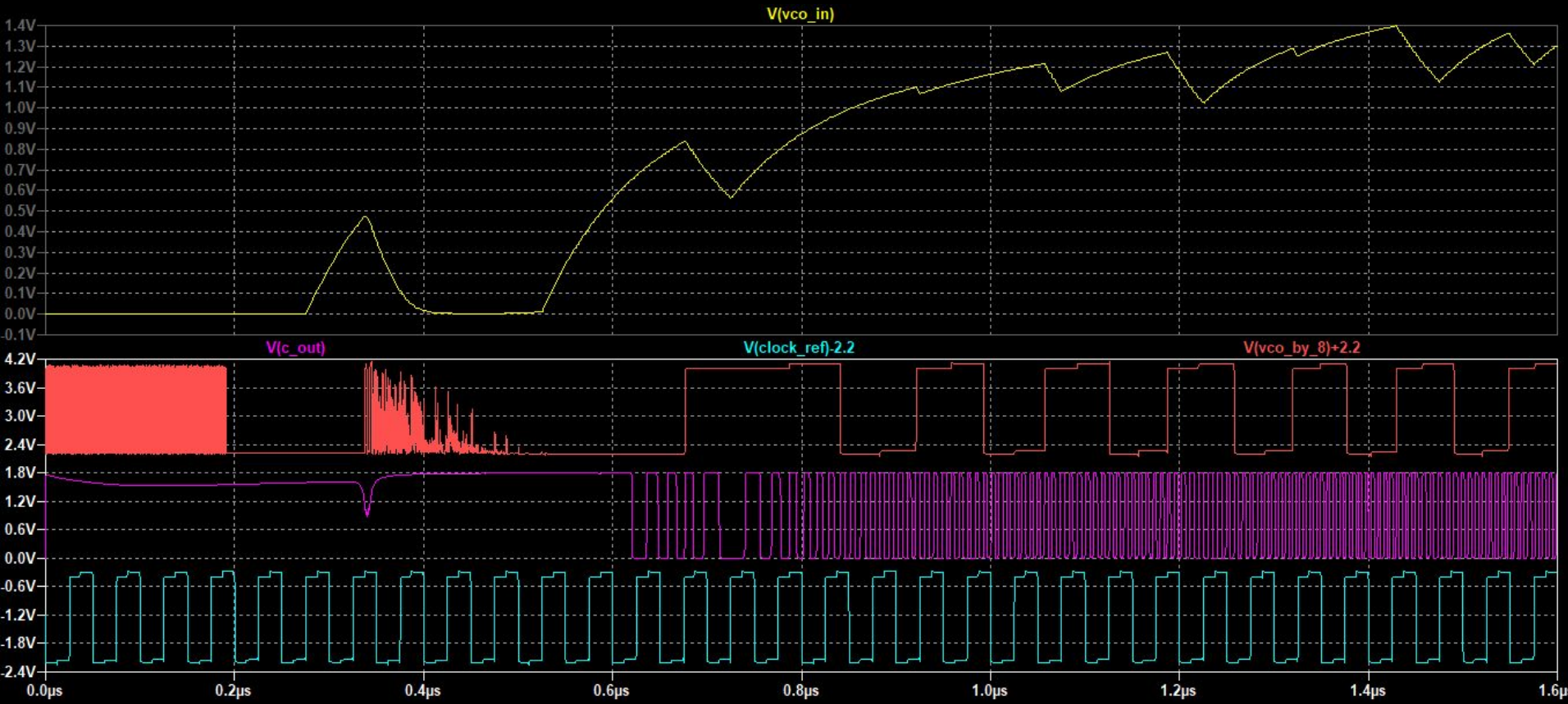
-> Acts like a “Leaky Bucket”.



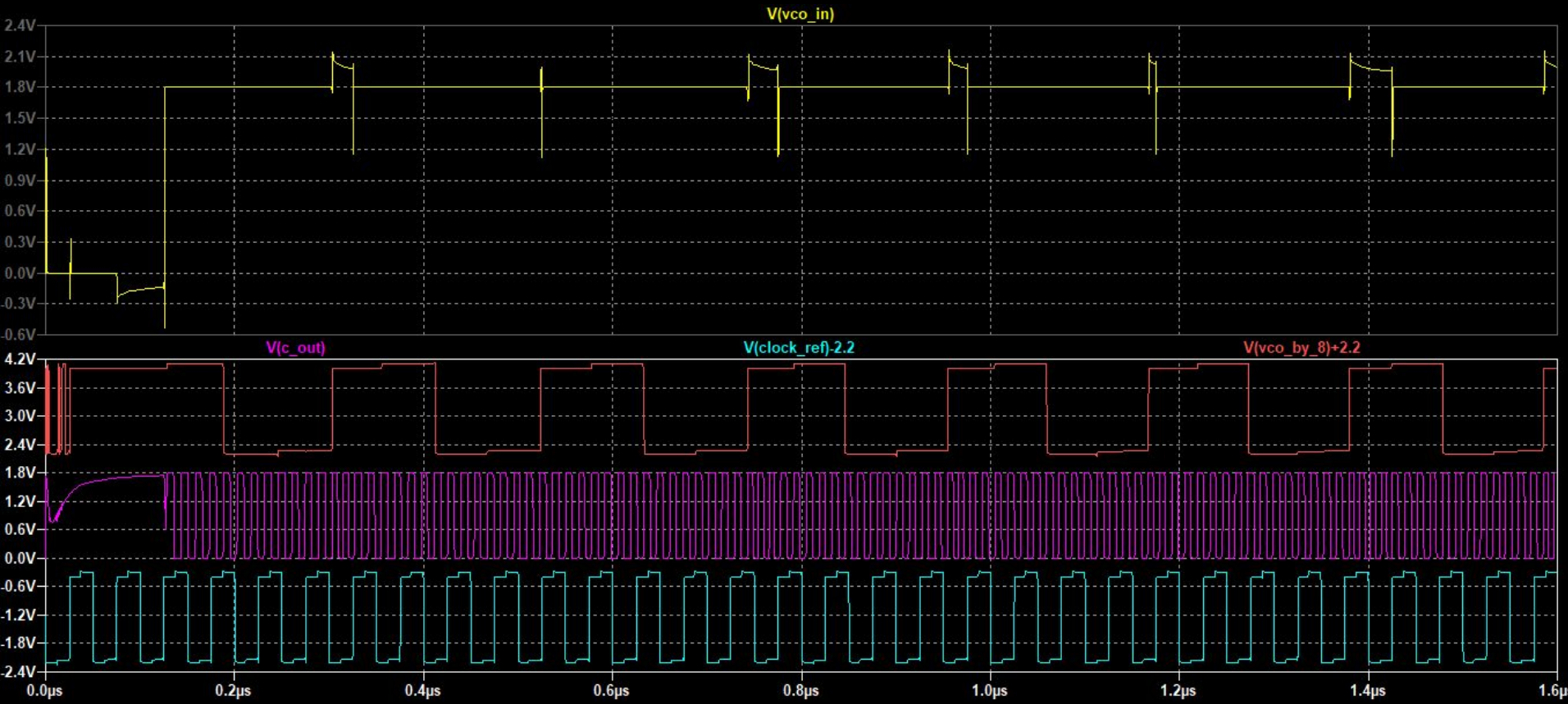
I-V characteristics of PMOS transistor



With loop filter



Without loop filter



-> VCO mode is not working as desired.

-> Biasing not used in VCO.

-> Loop filter can be improved/replaced.

-> Transistor count can be reduced with better modules but may affect performance. (285 Transistors and ~76% area utilisation)