A 100MHz-1.8V On Chip Clock Multiplier using PLL

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***Abstract*—This paper discusses the preliminary investigation carried in designing the specified analog IP as part of the VSD internship program and provides an overview of the concept of PLL. An on chip PLL is a critical component in the design of integrated circuits which is used as a frequency multiplier for generating a clock which is a multiple of the base clock.**

***Index Terms*—phase locked loop, clock generation, divide by n, voltage controlled oscillator, frequency multiplier**

I. Introduction

THE phase locked loop (PLL) is a crucial building block of linear systems. The high cost of realising PLL with discrete components limited its use in electronics. With the advancement in integrated circuit technologies, PLLs are available in inexpensive monolithic ICs. PLLs are used in applications such as frequency multiplication/division, frequency translation, AM detection, FM demodulation.[1]

In a microprocessor, PLL is used as a frequency multiplier to generate a high speed internal clock for the microprocessor from a low cost, low frequency, yet stable oscillator like quartz crystals. This allows the processor to function at a high internal clock frequency that is derived from a low frequency clock input.[2]

II. PLL Elements

A. Phase Detector

The Phase Detector (PD) detects the difference in phase between the external clock and generated clock. When there is negligible phase difference and the frequency is identical, the PLL is in the locked state.[1]

B. Voltage Controlled Oscillator

The function of the VCO is to generate an output frequency that is directly proportional to the input voltage, in a PLL this is the error voltage generated by the PD.[1]

C. Feedback Divider

PLL has a divider between the reference clock and the reference input to the phase detector. This allows to control the output clock frequency.[1]

III. Clock Generation

Fig.1 represents the typical clock system. The clock generation unit receives an external clock signal which is then frequency or phase adjusted by a PLL or delayed-lock loop (DLL). DLL is a variant of PLL that uses a voltage controlled delay line but is not capable of frequency multiplication. The global clock is then distributed throughout the chip. The PLL receives a reference clock and a feedback clock and produces

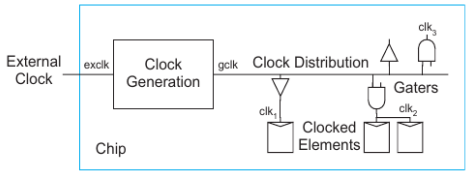

Fig. 1. Clock system in integrated circuits

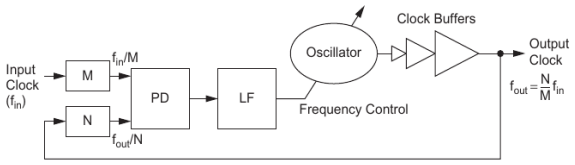

Fig. 2. PLL as frequency multiplier

an output clock. The phase and frequency of the output clock is adjusted until it is aligned with the reference clock.[3]

IV. PLL as Frequency Multiplier

The PLL may be used as a frequency multiplier as shown in Fig.2. The divider in the feedback path divides by N and the reference input divider divides by M, it allows the PLL to multiply the reference frequency by N/M. [3]

V. Conclusion

The low frequency input clock reduces the electromagnetic interference created by a system. It also reduces cost by eliminating the requirement of additional oscillators to a system. PLL may be designed to generate a clock at twice the microprocessor clock frequency which is then divided by two for achieving an accurate 50% duty cycle.[4] The major contributor of noise at the output jitter is the power supply switching noise, so the power supply noise rejection of the design needs to be maximized.[2]

The task ahead is to design a PLL with the required multiplication factor along with low power consumption, low supply voltage and limited output jitter.

References

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