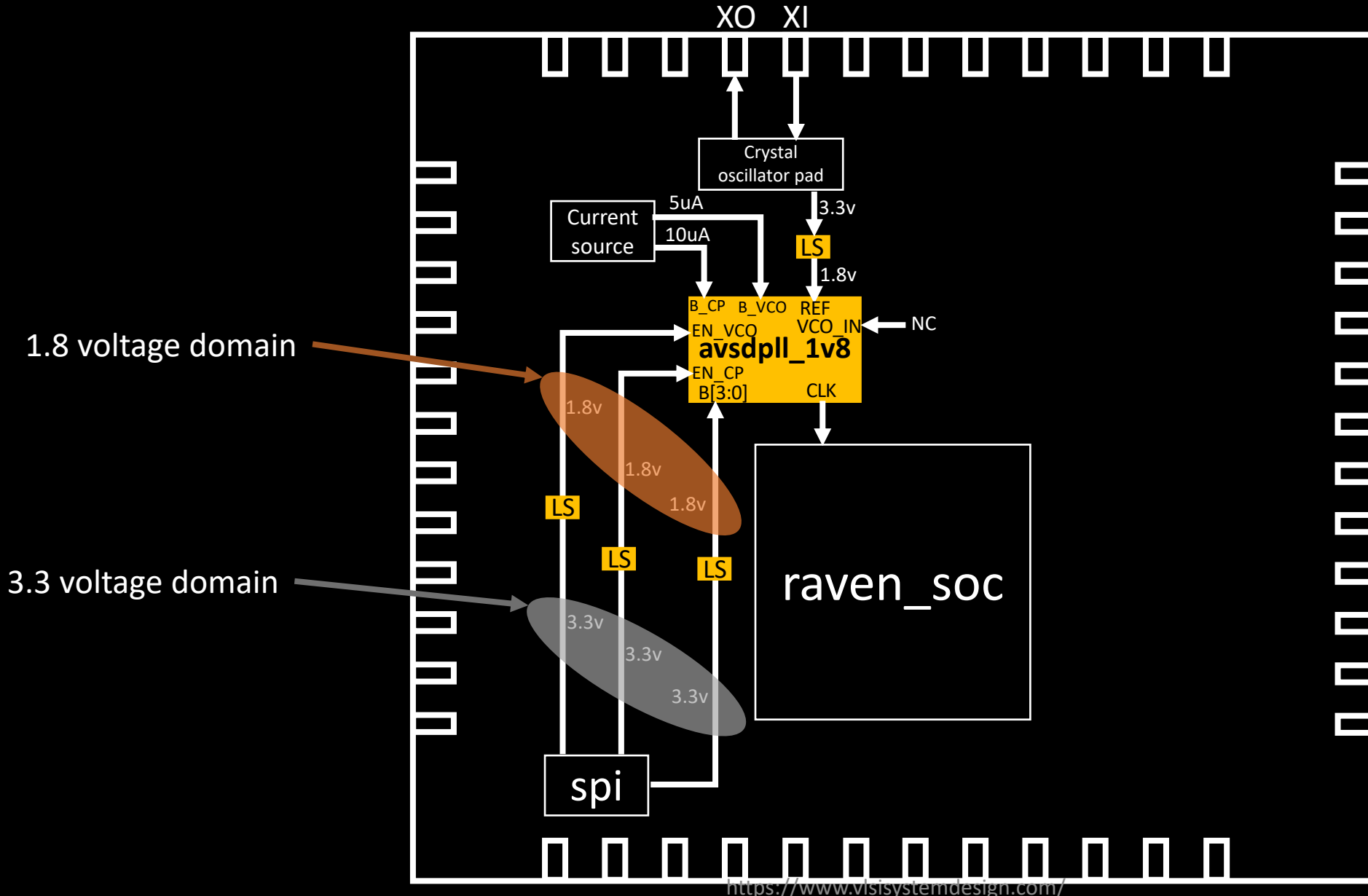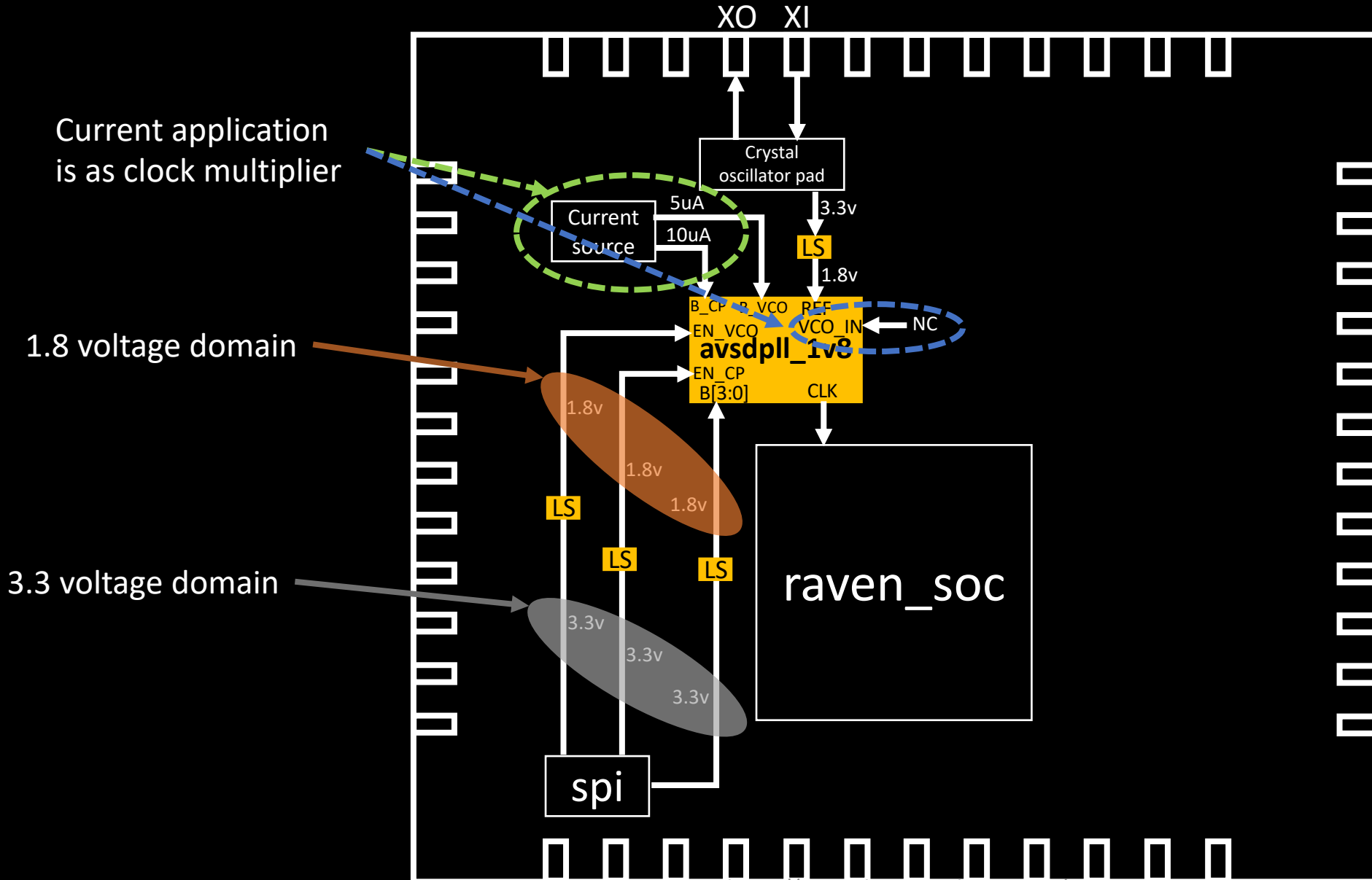# On-chip PLL (avsdpll_3v3) spec sheet for 180nm tech node

- **Specs released under APACHE LICENSE 2.0**

- **Please contact Kunal at kunalpghosh@gmail.com in case of any doubts**

Application Note for On-chip PLL(avsdpll_1v8)

Application Note for On-chip PLL(avsdpll_1v8)

XO XI

Current application is as clock multiplier

Crystal oscillator pad

Current source
5uA
10uA
3.3v
LS
1.8v

B_CP B_VCO REF
EN_VCO   VCO_IN ← NC
avsdpll_1v8
EN_CP
B[3:0]   CLK

1.8 voltage domain

1.8v
1.8v
1.8v

LS
LS
LS

3.3 voltage domain

3.3v
3.3v
3.3v

raven_soc

spi

avsdpll_1v8 preferred dimensions, pin locations and metal layers

270.78 um

155.24 um

B_CP
m2
m1

B_VCO
m2
m1

REF
m2
m1

VCO_IN
m1

EN_VCO
m2

avsdpll_1v8

m1

EN_CP
m2

m2
B[3:0]

m2
CLK

m1
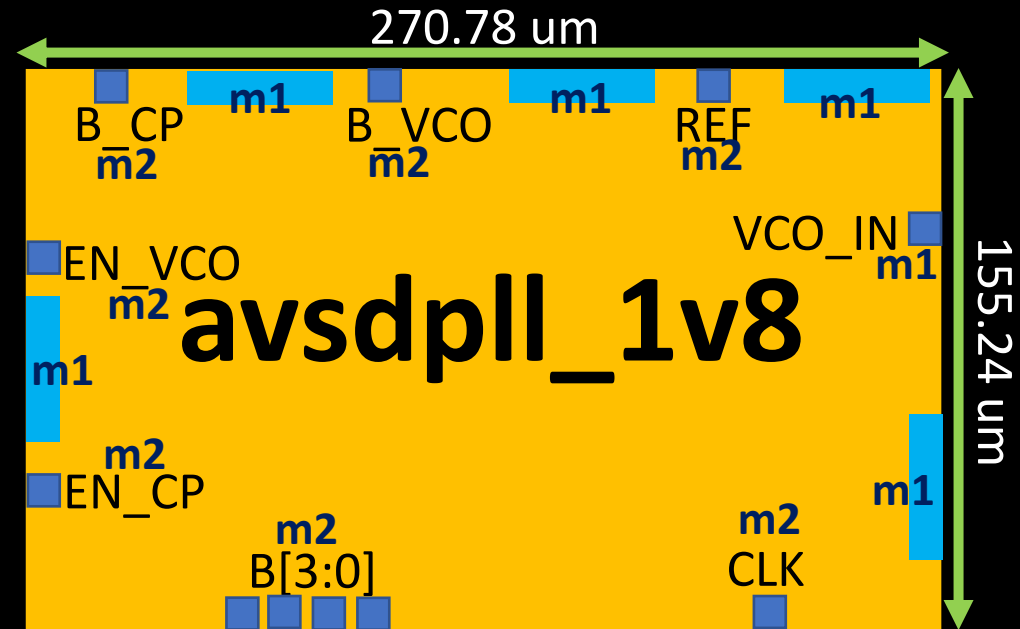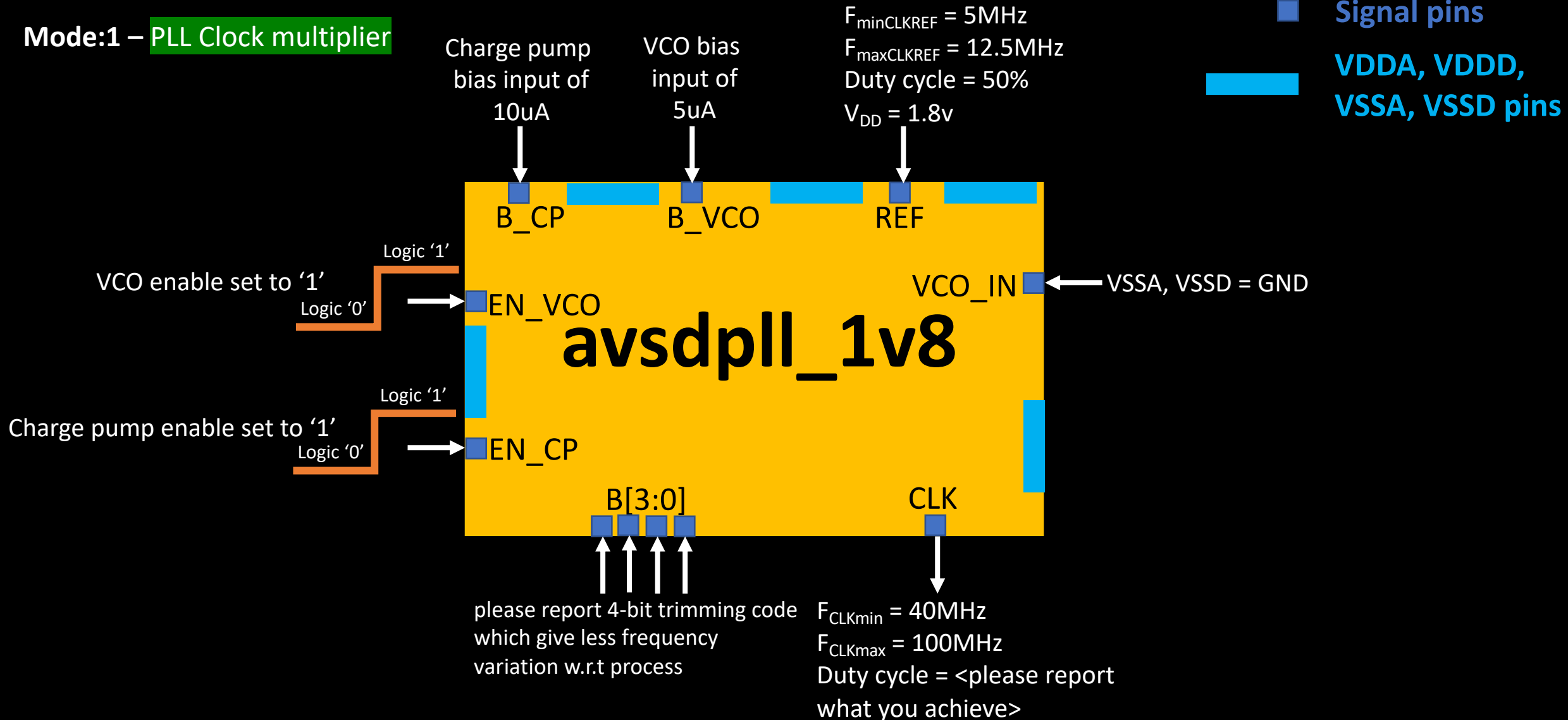
■ Signal pins – 0.34um x 0.34um

VDDA, VDDD, VSSA, VSSD pins
3um x 0.34um

avsdpll_1v8 operating modes

Mode:1 – PLL Clock multiplier

Charge pump bias input of 10uA

VCO bias input of 5uA

$F_{minCLKREF}$ = 5MHz
$F_{maxCLKREF}$ = 12.5MHz
Duty cycle = 50%
V_{DD} = 1.8v

Signal pins

VDDA, VDDD, VSSA, VSSD pins

B_CP

B_VCO

REF

VCO enable set to '1'

Logic '1'

Logic '0'

EN_VCO

VCO_IN

VSSA, VSSD = GND

Charge pump enable set to '1'

Logic '1'

Logic '0'

EN_CP

avsdpll_1v8

B[3:0]

CLK

please report 4-bit trimming code which give less frequency variation w.r.t process

F_{CLKmin} = 40MHz
F_{CLKmax} = 100MHz
Duty cycle = <please report what you achieve>

avsdpll_1v8 operating modes

Signal pins

VDDA, VDDD, VSSA, VSSD pins

Mode:2 – VCO only

VCO bias input of 5uA

VSSA,VSSD = GND

VSSA,VSSD = GND

B_CP

B_VCO

REF

VCO enable set to '1'

Logic '1'

Logic '0'

EN_VCO

avsdpll_1v8

VCO_IN

V_{MIN} = 0.2v
V_{MAX} = 1.2v

Logic '1'

Charge pump enable set to '0'

Logic '0'

EN_CP

B[3:0]

CLK

please report 4-bit trimming code which give less frequency variation w.r.t process

F_{CLKmin} = 20MHz
F_{CLKmax} = 120MHz
Duty cycle = <please report what you achieve>

avsdpll_1v8 plots and values needed

1) Jitter(RMS) at input F_{REFCLK} of 10MHz in PLL mode (expected = 30ps) – Post tape-out

2) F_{CLK} vs VCO at T=-40C, +27C, +150C with VDD = 1.8v and recommended trimming bit code B[3:0]

3) F_{CLK} vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111

4) F_{CLK} vs VDD at T=-40C, +27C, +150C with VCO = 0.2v and recommended trimming bit code B[3:0]

avsdpll_1v8 plots and values needed

5) F_{CLK} vs T (-40C to 160C) at VDD = 1.6v, 1.8v, 1.98v with VCO = 0.2v and recommended trimming bit code B[3:0]

6) IDDA vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111 (VCO mode)

7) IDDD vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111 (VCO mode)

8) Duty cycle vs VDDR[1.6V to 2V] at F_{CLKREF} = 10MHz and recommended trimming bit code B[3:0] (PLL mode)