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WELCOME TO ELECTROMANIA!

DAY - 3

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01
ADDERS

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HALF-ADDER

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value.

It has two inputs, called A and B, and two outputs S (sum) and C (carry). The common representation uses a XOR logic gate and an AND logic gate.

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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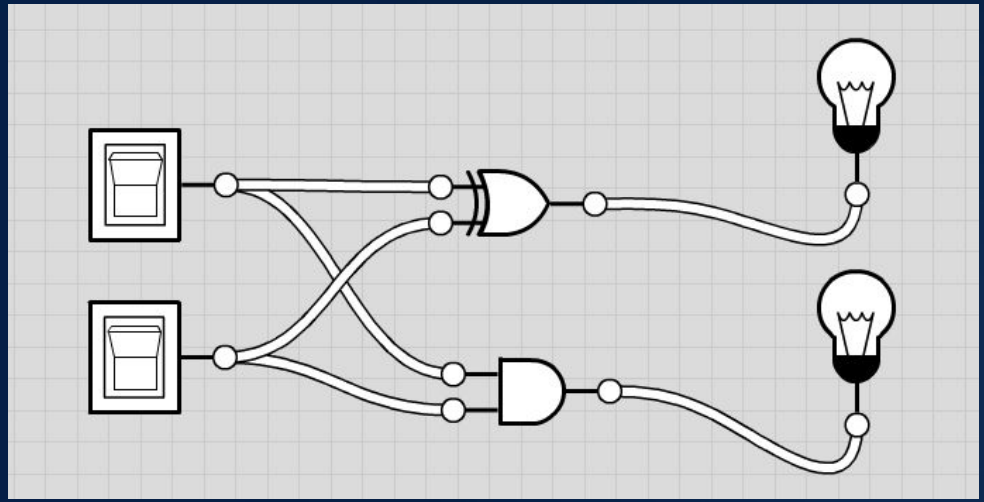
SUM, S = A XOR B
CARRY, C = A AND B



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FULL ADDER

A full adder is a digital circuit that performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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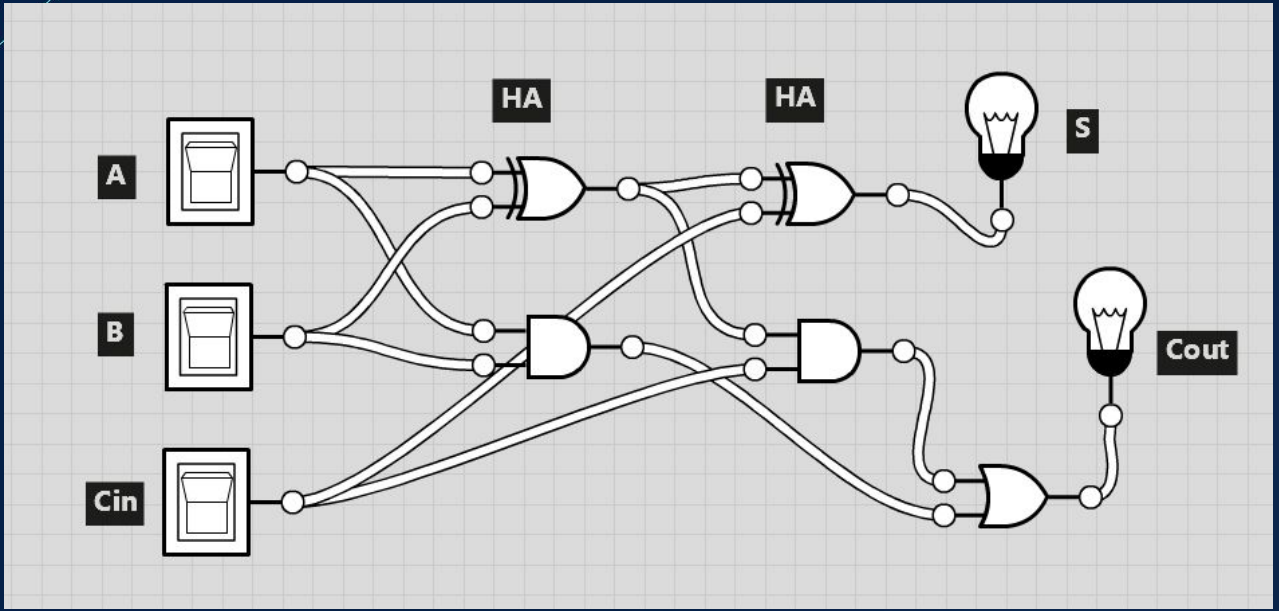
S = A XOR B XOR C

C = (A & B) | (C & (A ^ B))



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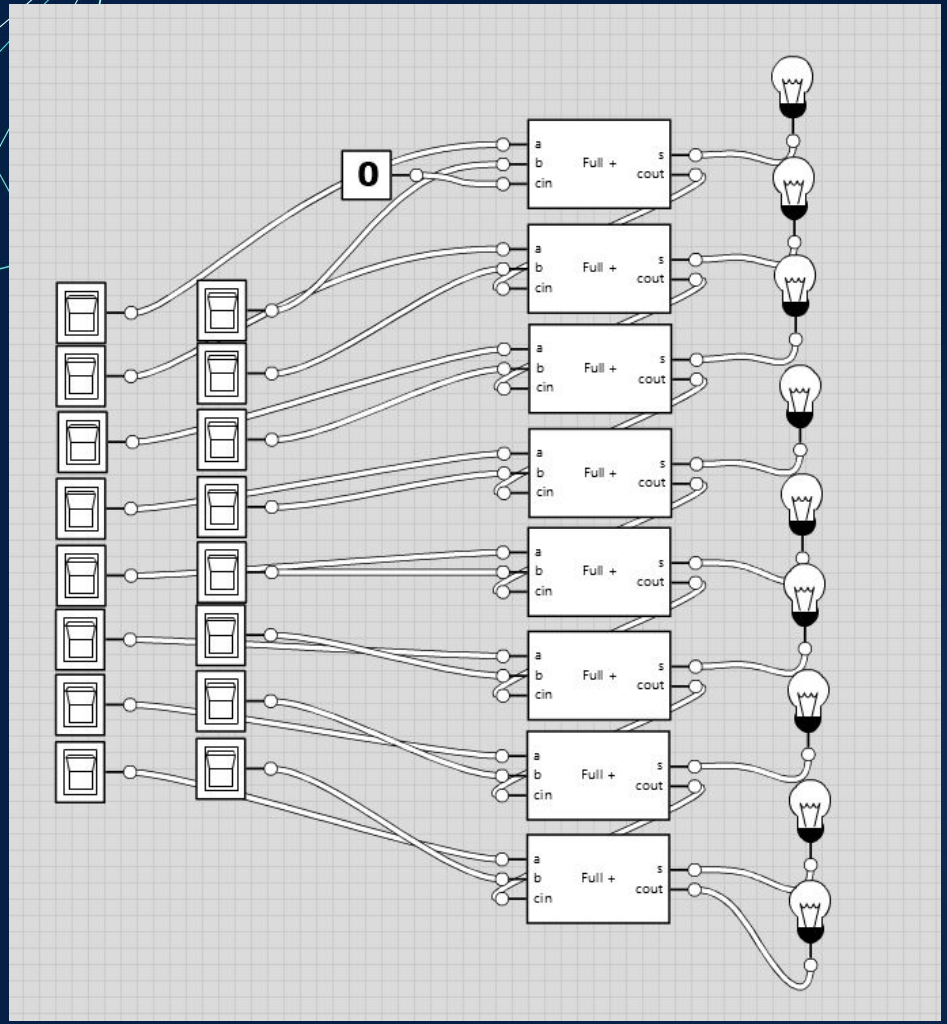

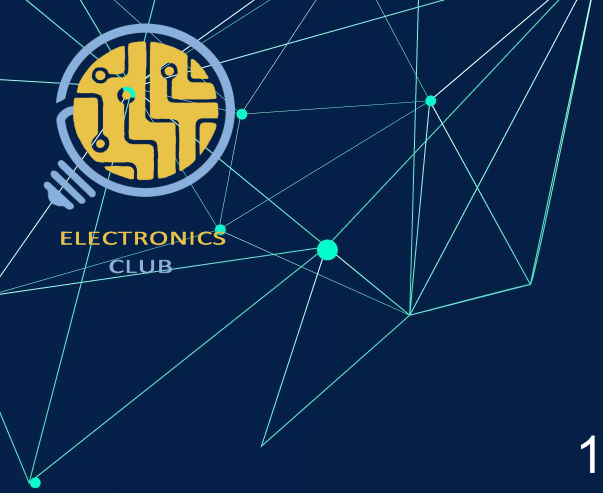

Different Coding Styles In Verilog

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1. Behavioral or Algorithmic level
2. Dataflow level
3. Gate level or Structural level
4. Switch level

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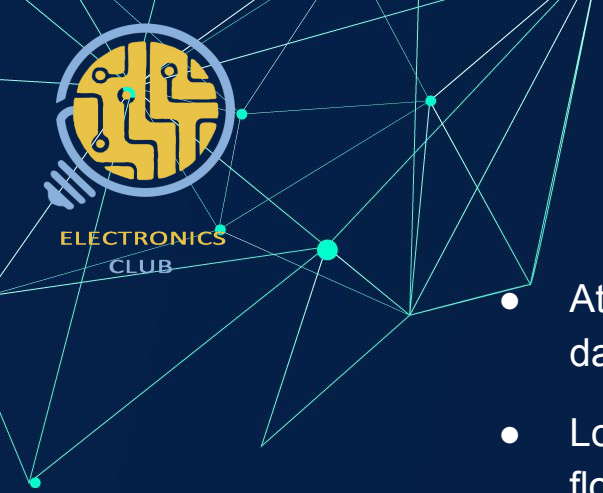
Behavioural or Algorithmic

- This is the highest level of abstraction provided by Verilog HDL.
- A module can be implemented in terms of the desired design algorithm without concern for the hardware implementation details.
- It specifies the circuit in terms of its expected behavior.
- It is the closest to a natural language description of the circuit functionality, but also the most difficult to synthesize.



DataFlow level

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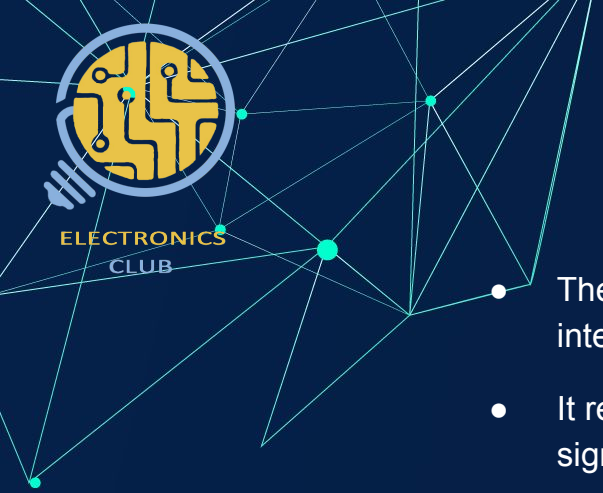
- At this level, the module is designed by specifying the data flow.
- Looking towards this design, one can realize how data flows between hardware registers and how the data is processed in the design.
- This style is similar to logical equations. The specification is comprised of expressions made up of input signals and assigned to outputs.
- In most cases, such an approach can be quite easily translated into a structure and then implemented



Gate level

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- The module is implemented in terms of logic gates and interconnections between these gates.
- It resembles a schematic drawing with components connected with signals.
- A change in the value of any input signal of a component activates the component. If two or more components are activated concurrently, they will perform their actions concurrently as well.
- A structural system representation is closer to the physical implementation than behavioral one but it is more involved because of large number of details. Since logic gate is most popular component, Verilog has a predefined set of logic gates known as ***primitives***. Any digital circuit can be built from these primitives.

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02

SUBTRACTORS

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HALF-SUBTRACTOR

The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend **X** and subtrahend **Y** and two outputs the difference **D** and borrow out **B**. The borrow out signal is set when the subtractor needs to borrow from the next digit in a multi-digit subtraction.

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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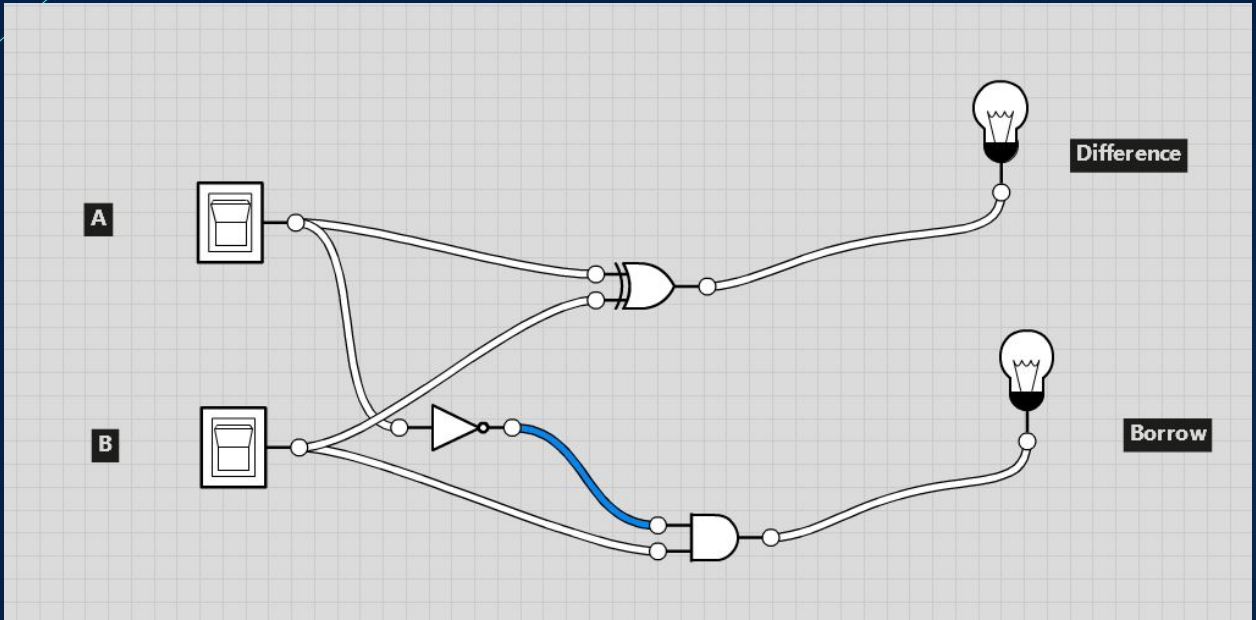
Diff = A XOR B
Borrow = A' AND B



FULL SUBTRACTOR

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The full subtractor is a combinational circuit which is used to perform subtraction of three input bits: the minuend **X**, subtrahend **Y**, and borrow in **B**. The full subtractor generates two output bits: the difference **D** and borrow out **B**. **B** is set when the previous digit is borrowed from **X**. Thus, **B** is also subtracted from **X** as well as the subtrahend **Y**.

INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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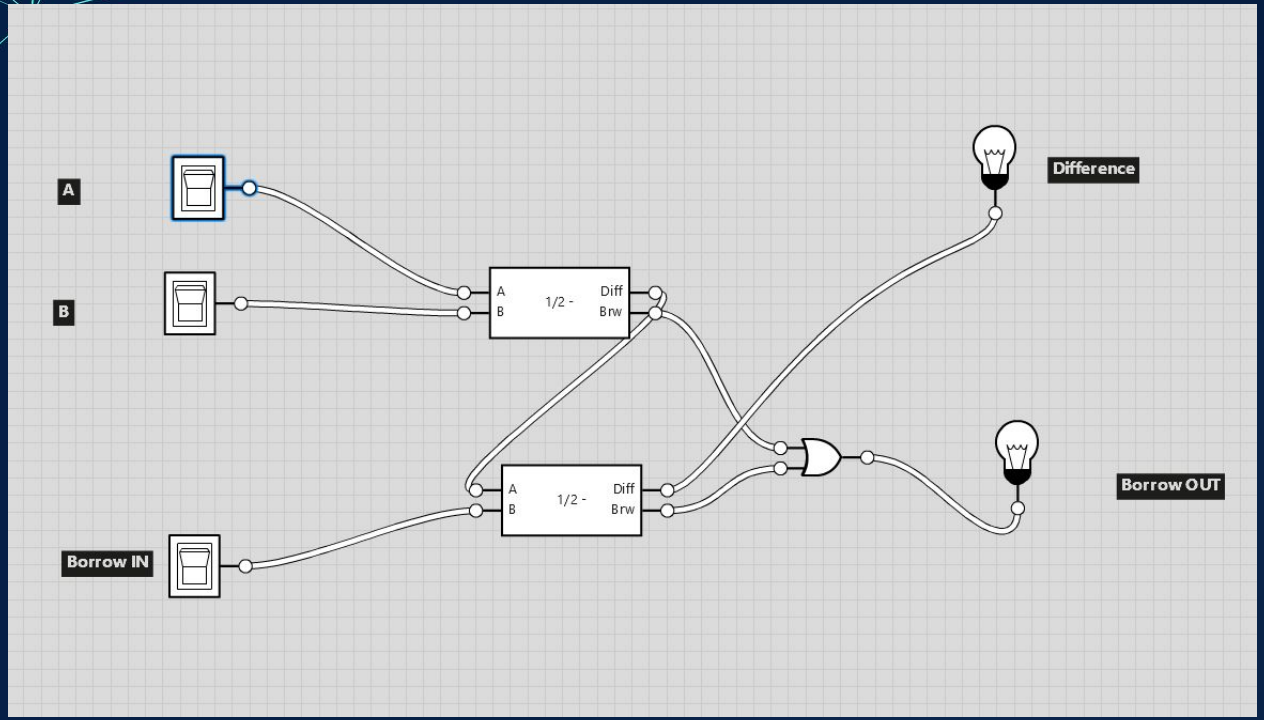
Diff = D2
Borrow Out= Brw1 OR Brw2



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03

MULTIPLIER

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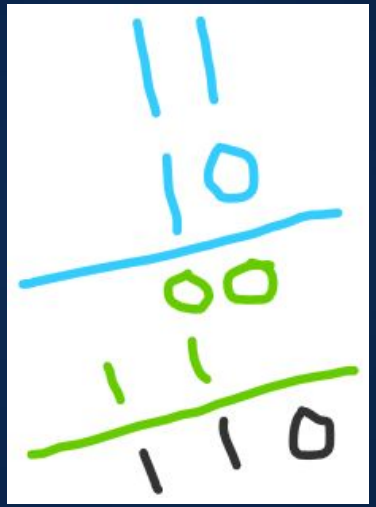
		b1	b0
		a1	a0
		a0b1	a0b0
	a1b1	a1b0	
c3	c2	c1	c0

An array multiplier is a digital combinational circuit used for multiplying two binary numbers by employing an array of full adders and half adders. This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the Adder array.



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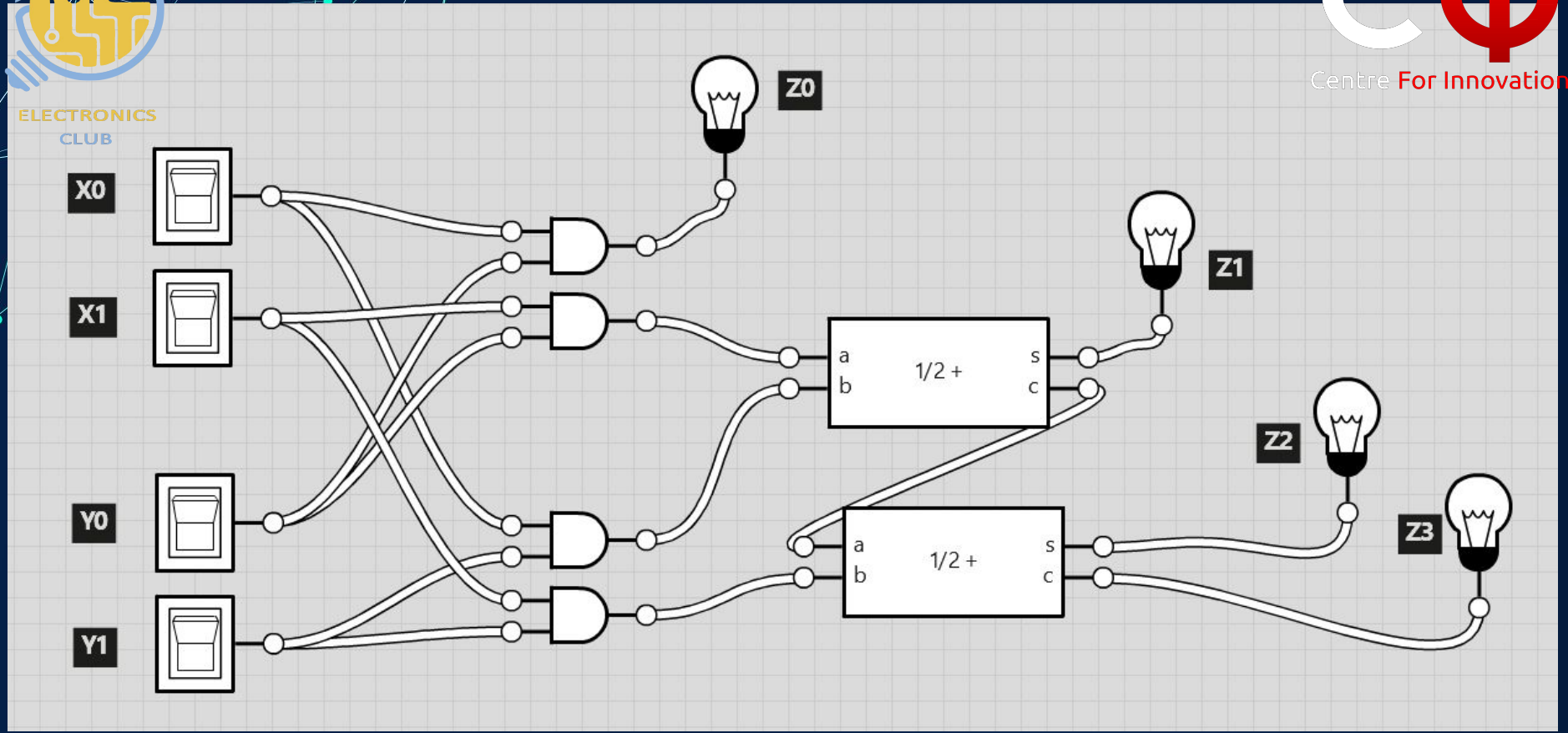

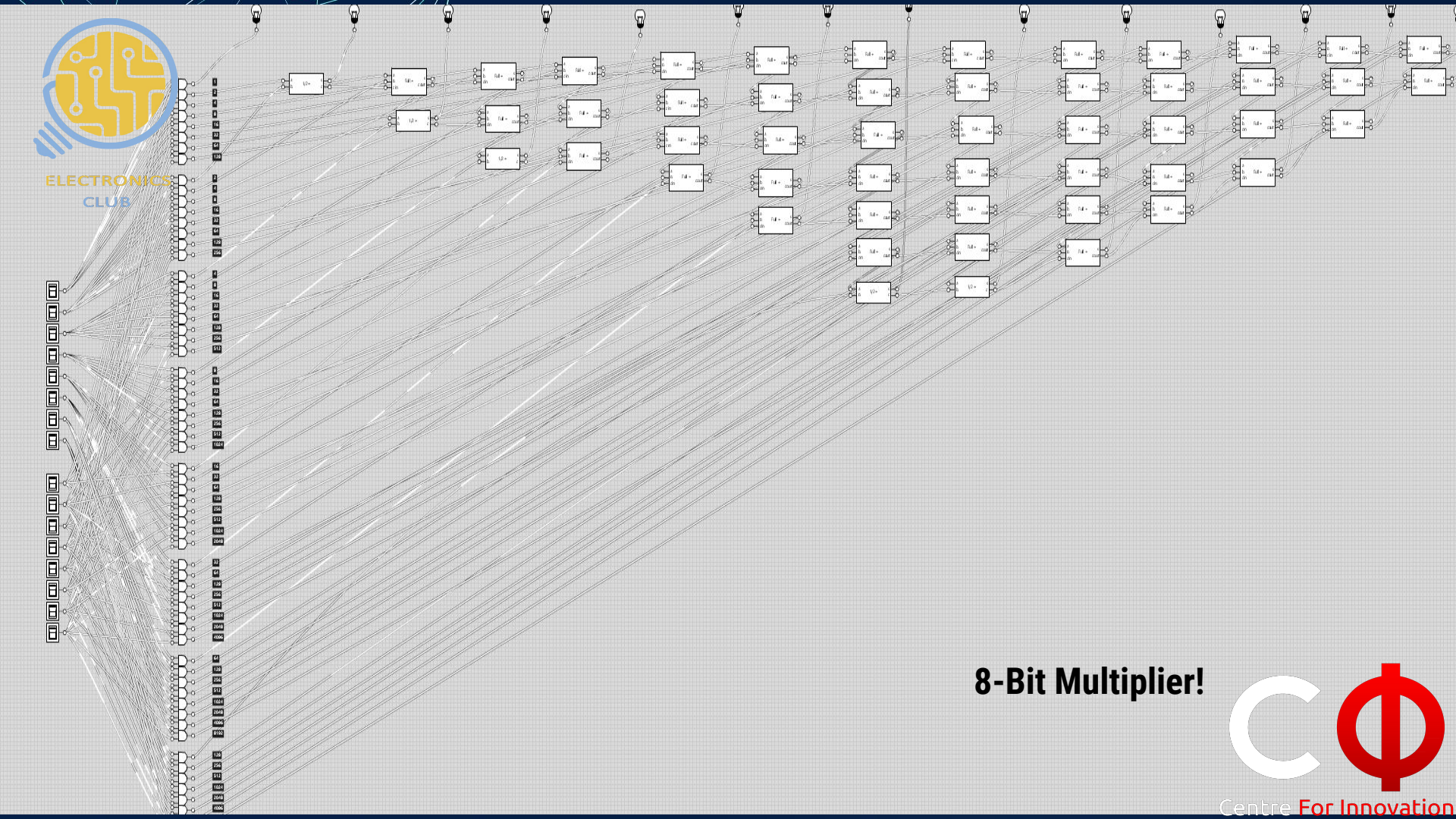
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8-Bit Multiplier!
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THANKS

Do you have any questions?

https://forms.gle/X6ry7PcFWmkF9RGA8

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