Prabalakshmi Arumugam

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Education

Boise State University **Jan 2025 – Dec 2026**
Master of Engineering in Electrical and Computer Engineering; GPA: 3.9/4.0 Boise, ID
Coursework: CMOS Analog IC Design, Memory-Centric Architecture, Advanced Device Design and Simulation, Digital Hardware Design, Computer Architecture, Digital Integrated Circuit Design

Anna University **Aug 2018 – Jun 2022**
Bachelor of Engineering in Electronics and Communication Engineering; GPA: 3.6/4.0 Tamil Nadu, India

Technical Skills

Hardware Description and Verification: Verilog, SystemVerilog, UVM
Programming Languages: Python, C++, MATLAB
Simulation and EDA Tools: Cadence Virtuoso, Spectre, ModelSim, Synopsys Design Compiler, Quartus, Xilinx Vivado, COMSOL
AI/ML and Software Development: PyTorch, TensorFlow, Scikit-learn, NumPy, Pandas, Matplotlib, Seaborn, Plotly, Git, Linux

Work Experience

Dish Network Technologies **Aug 2022 – Dec 2024**
Software Engineer Bengaluru, India

- Developed and optimized backend services for Sling streaming platform using **Python**, **Django** and MSSQL, implementing advanced **SQL tuning** to reduce server response time by **25%**.
- Designed **RESTful APIs** and **GraphQL** endpoints, cutting API latency by **20%** and validating performance with **Postman**.
- Streamlined deployment processes and ensured consistent environments across stages by implementing **CI/CD** with **Jenkins** and **GitLab**, and managing containerization with **Docker** and **Kubernetes**.

Delta Electronics **Feb 2022 – Jul 2022**
Physical Failure Analysis Intern Hosur, India

- Performed **root cause analysis** on failed **Variable Frequency drive** (VFD) **PCBs** using **advanced microscopy** and **electrical probing**, identifying defects such as solder joint fractures, trace burns, and component failures.
- Prepared detailed **failure reports** linking defect characteristics to potential process or material issues, enabling targeted corrective actions by manufacturing quality teams.
- Identified previously undetected **defects** missed by **Automatic Optical Inspection (AOI)** and collaborated with the team to integrate them into the AOI **detection library** for improved defect tracking.

Projects

Low-Noise Neural Amplifier Design | ***Cadence Virtuoso*** **Spring 2025**

- Designed a folded **Cascode neural amplifier** (less than 1 microWatt power, microvolt-level signal amplification) using gm/ID methodology; achieved 47 V/V gain and 7 kHz bandwidth.
- Executed **TT/SS/FF corner**, **Monte Carlo**, and **noise simulations** to assess PVT robustness, mismatch effects, and minimize **input-referred noise** with thick oxide devices.
- Validated performance via **AC**, **transient**, and **noise analyses** in Spectre; documented gain, phase margin, and integrated noise for final design sign-off.

DRAM-Based In-Memory ALU Accelerator | ***Verilog, Yosys*** **Spring 2025**

- Engineered a custom **8-bit ALU** (addition and multiplication) in **Verilog**, synthesized with **Yosys**, and integrated at the **DRAM column decoder** for near-data processing.
- Enabled **64-way parallelism** (8 banks × 8 subarrays), achieving 546 GigaOps per second throughput with only **0.4%** area overhead at 130nm, and benchmarked timing (**tRCD**, **tCAS**), power (**12.5 microW per ALU**), and energy (**125–250 fJ/op**), demonstrating scalability for embedded AI.

AXI-Based PWM Module Design and Verification | ***Verilog, SystemVerilog, ModelSim, Yosys*** **Summer 2025**

- Designed an **AXI4-Lite register-mapped PWM** peripheral in **SystemVerilog**, supporting programmable period, duty cycle, and enable/disable control, and integrated for **SoC-level readiness**.
- Developed a **self-checking UVM/SystemVerilog testbench** with assertions, functional coverage, and protocol checks for AXI handshakes; validated functionality via GTKWave waveform analysis and protocol compliance.
- Synthesized the design with **Yosys** using FPGA flow, generated **area/utilization reports** (LUTs, FFs).

Research Publications

1. A Comparative Study on Plant Classification Performance Using Deep Learning Optimizers. [**Link**]
2. Identification of Indian Medicinal Plants from Leaves using Transfer Learning Approach. [**Link**]
3. A Novel Convolutional Neural Network Architecture to Diagnose COVID-19. [**Link**]