Prabalakshmi Arumugam

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Education

Boise State University **Jan 2025 – Dec 2026**
Master of Engineering in Electrical and Computer Engineering; GPA: 3.9/4.0 Boise, ID
Coursework: CMOS Analog IC Design, Memory-Centric Architecture, Advanced Device Design and Simulation, Digital Hardware Design, Computer Architecture, Digital Integrated Circuit Design

Anna University **Aug 2018 – Jun 2022**
Bachelor of Engineering in Electronics and Communication Engineering; GPA: 3.6/4.0 Tamil Nadu, India

Technical Skills

Failure Analysis: Optical microscopy, electrical probing, PCB inspection, defect localization, continuity and leakage testing, RCA.
Lab Equipment: Multimeter, power supply, oscilloscope, logic analyzer, soldering and rework tools, curve tracer (familiarity).
Hardware Description and Verification: Verilog, SystemVerilog, UVM
Programming and Software: Python, C++, MATLAB, Git, Linux
Simulation and EDA Tools: Cadence Virtuoso, Xilinx Vivado, Spectre, ModelSim, Synopsys DC, GTKWave, Quartus, COMSOL

Work Experience

Dish Network Technologies **Aug 2022 – Dec 2024**
Software Engineer Bengaluru, India

- Performed **root cause analysis** on production failures by analyzing **logs**, and **traffic patterns** to identify **fault origins**.
- Optimized backend services (**Python**, **Django**, **MSSQL**) by identifying performance-limiting components and validating improvements through repeatable test cases.
- Maintained stable deployments using **CI/CD automation** (**Jenkins**, **GitLab**) and **containerized environments** to ensure controlled, reproducible software releases.

Delta Electronics **Feb 2022 – Jul 2022**
Physical Failure Analysis Intern Hosur, India

- Executed **electrical fault isolation** and physical root cause analysis on variable-frequency drive (VFD) PCBs, characterizing failure mechanisms including solder fatigue, **EOS (Electrical Overstress)**, and open/short circuits via **optical microscopy**.
- Generated comprehensive **failure analysis reports** correlating electrical signatures to physical defects, providing critical **feedback to process engineering teams** to resolve material deviations and **improve manufacturing yield**.
- Analyzed **Automatic Optical Inspection escape points** to identify non-standard defect signatures; updated the inspection library parameters, significantly **reducing false negatives** and enhancing **inline quality control**.

Projects

Low-Noise Neural Amplifier Design and Reliability Analysis | ***Cadence Virtuoso*** **Spring 2025**

- Designed a folded **Cascode neural amplifier** (less than 1 microwatt power, microvolt-level signal amplification) using gm/ID methodology; achieved 47 V/V gain and 7 kHz bandwidth.
- Executed **TT/SS/FF corner**, **Monte Carlo**, **noise simulations** and **fault injection simulation** (resistive shorts/opens) to assess PVT robustness, **analyze physical defect impacts**, and minimize **input-referred noise**.
- Validated performance via **AC**, **transient**, and **noise analyses** in Spectre; documented gain, phase margin, **electrical failure signatures** and integrated noise for final design sign-off.

DRAM-Based In-Memory ALU Accelerator | ***Verilog, Xilinx Vivado*** **Spring 2025**

- Engineered a custom **8-bit ALU** (addition and multiplication) in **Verilog**, synthesized with **Xilinx Vivado**, and integrated at the **DRAM column decoder** for near-data processing.
- Enabled **64-way parallelism** (8 banks × 8 subarrays), achieving 546 GigaOps per second throughput with only **0.4%** area overhead at 130nm, and benchmarked timing (**tRCD**, **tCAS**), power (**12.5 microW per ALU**), and energy (**125–250 fJ/op**), demonstrating scalability for embedded AI.

RTL Design and FPGA Implementation of a Soda Vending Machine | ***Verilog, Xilinx Vivado*** **Fall 2025**

- Designed a soda vending machine in **Verilog** using a Finite State Machine (FSM) controller and a custom datapath (adders, comparators) for logic operations.
- Managed the complete **RTL-to-bitstream** flow in **Xilinx Vivado**, including synthesis, implementation, and writing .XDC constraint files for the Zybo board, and verified with a **command-driven testbench**.
- Analyzed synthesis reports to compare FSM encoding styles for **resource usage (LUTs vs. FFs)** and implemented on Zybo.

Research Publications

1. A Comparative Study on Plant Classification Performance Using Deep Learning Optimizers. [**Link**]
2. Identification of Indian Medicinal Plants from Leaves using Transfer Learning Approach. [**Link**]