Sairam INSTITUTIONS

Sri SAI RAM ENGINEERING COLLEGE

INSTITUTE OF TECHNOLOGY

West Tambaram, Chennai - 44

YEAR	SEM
II	III

CS8351

DIGITAL PRINCIPLES AND SYSTEM DESIGN (COMMON TO CSE&IT)

UNIT No. 3

3.2 STORAGE ELEMENTS :LATCHES,FLIP-LOPS

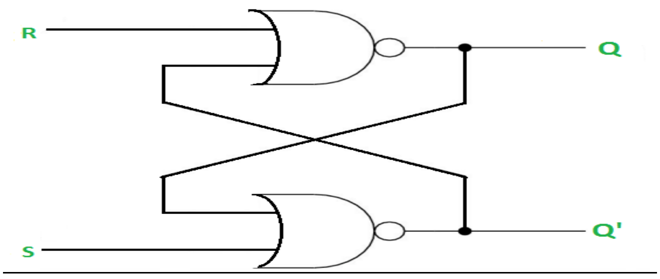
Latches and flip flops are the basic elements and these are used to store information. One flip flop and latch can store one bit of data. The main difference between the latches and flip flops is that, a latch checks input continuously and changes the output whenever there is a change in input. But, flip flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock.

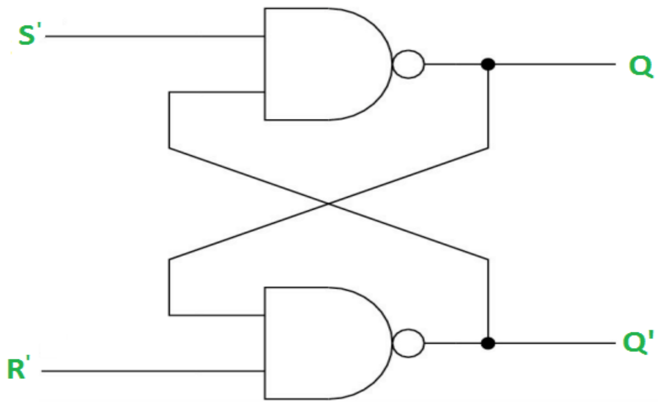
- Flip flop is a data storage device
- Stored data can be changed by varying input data
- Flip flops and latches are the fundamental building blocks of digital electronic system
- Basic difference between latch and flip flop is a gating or clocking mechanism

- There are four types of flip flops
- 1. SR flip flop
- 2. JK flip flop
- 3. D flip flop
- 4. T flip flop

LATCHES	FLIP FLOPS
Latches can be build from logic gates	Flip flops can be build from latches
Based on enable function input	Based on clock pulses
Latches continuously checks its input and change its output correspondingly	Continuously checks its input and changes its output only at times determined by clocking pulse

SR latch using NOR and NAND gates





Two inputs SET and RESET
Two output's Q and Q'

Case-1:S'=R'=1(S=R=0)

If Q = 1, Q and R' inputs for 2nd NAND gate are both 1.
If Q = 0, Q and R' inputs for 2nd NAND gate are 0 and 1 respectively.

Case-2: S'=0, R'=1 (S=1, R=0)

As S'=0, the output of 1st NAND gate, Q = 1(**SET state**). In 2nd NAND gate, as Q and R' inputs are 1, Q'=0.

Case-3: S'= 1, R'= 0 (S=0, R=1) –

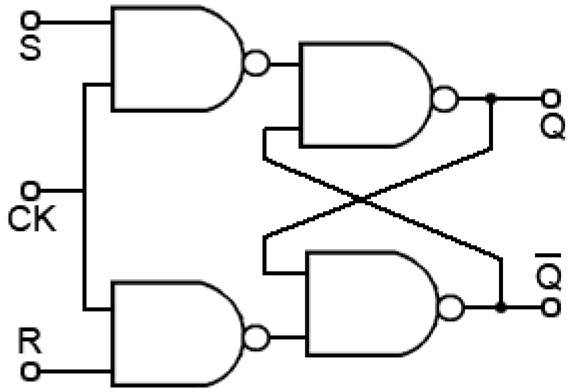
As R'=0, the output of 2nd NAND gate, Q' = 1. In 1st NAND gate, as Q and S' inputs are 1, Q=0(**RESET state**).

Case-4: S'= R'= 0 (S=R=1) –

When S=R=1, both Q and Q' becomes 1 which is not allowed. So, the input condition is prohibited.

S	**R**	**Q**	**Q'**
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	indefinite	indefinite

SR flip flop using NAND gate



Truth Table

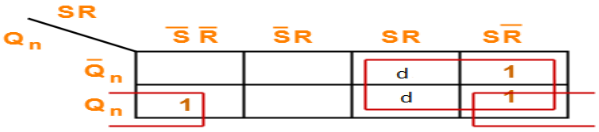
Clk	S	R	Q	Q’
↑	0	0	Q	Q’
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	indefinite	indefinite

Characteristics Table

Q(present state)	S	R	Q_{n+1}(next state)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

Excitation Table

Q	$\bar{Q}$	S	R
0	0	0	d
0	1	1	0
1	0	0	1
1	1	d	0

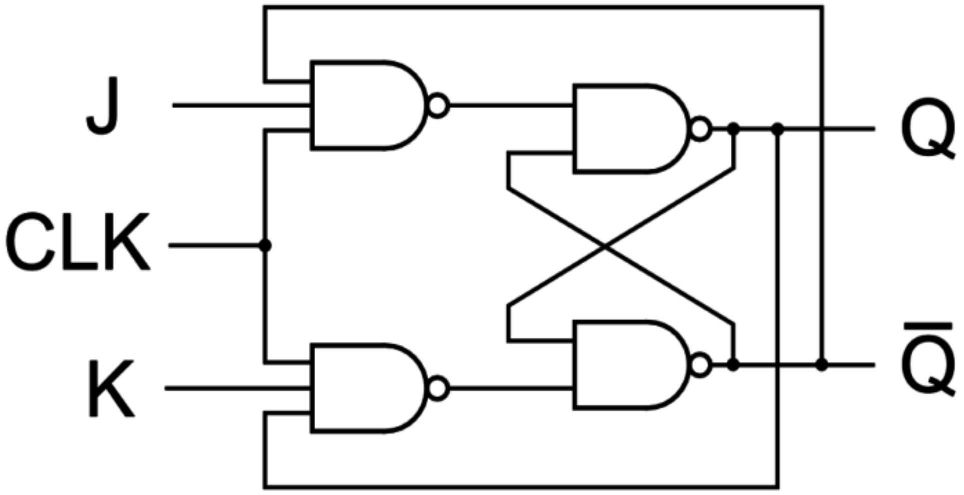


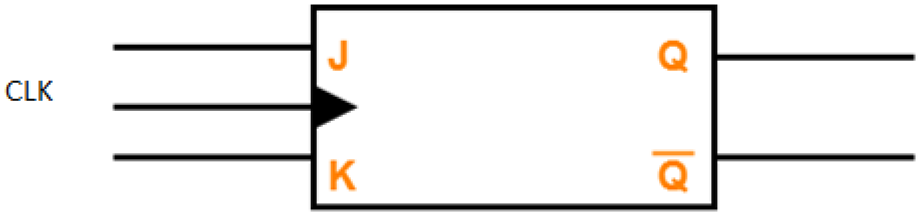
Q_n \ SR	$\bar{S}\bar{R}$	$\bar{S}R$	SR	$S\bar{R}$
$\bar{Q}_n$			d	1
Q_n	1		d	1

K Map

Characteristic equation Q_{n+1}=S+Q_nR

JK FLIP FLOP





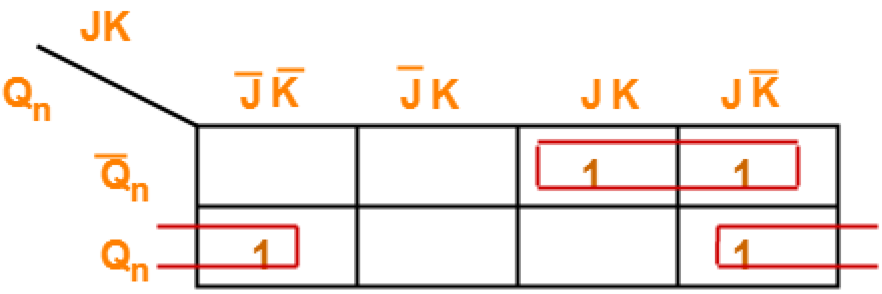
Logic Symbol

Truth Table

Clk	**J**	**K**	**Q**	**Q’**
↑	0	0	Q	Q’
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Q’	Q

Characteristics Table

Clk	**Q**	**J**	**K**	**Q_{n+1}**
↑	0	0	0	0
↑	0	0	1	0
↑	0	1	0	1
↑	0	1	1	1
↑	1	0	0	1
↑	1	0	1	0
↑	1	1	0	1
↑	1	1	1	0



K Map

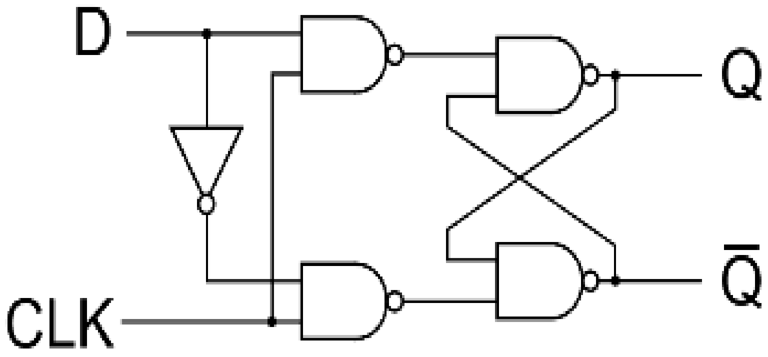
$$Q_{n+1} = Q'_nJ + Q_nK'$$

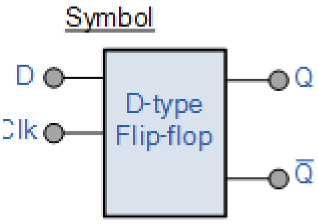
Excitation Table

Qn	Q_{n+1}	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

D FLIP FLOP

The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time.





Characteristic Table

Q(present state)	D	Q_{n+1}(next state)
0	0	0
0	1	1
1	0	0
1	1	1

Truth Table

Clk	D	Q_{n+1}
↑	0	0
↑	1	1

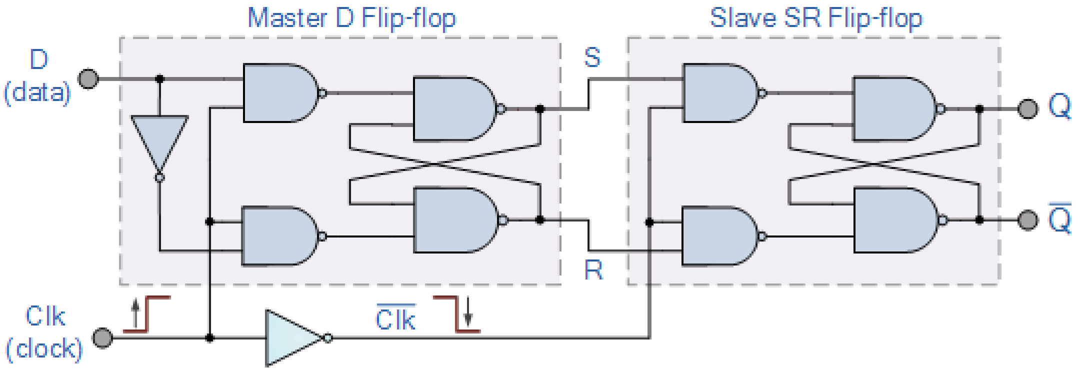
Excitation Table

Q(present state)	Q_{n+1}(next state)	D
0	0	0
0	1	1
1	0	0
1	1	1

Characteristics Equation

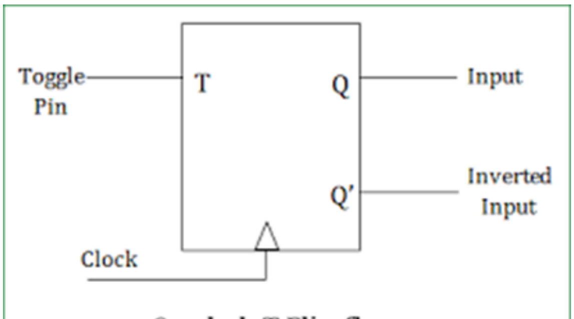
$Q_{n+1} = D$

The master Slave D flip flop circuit

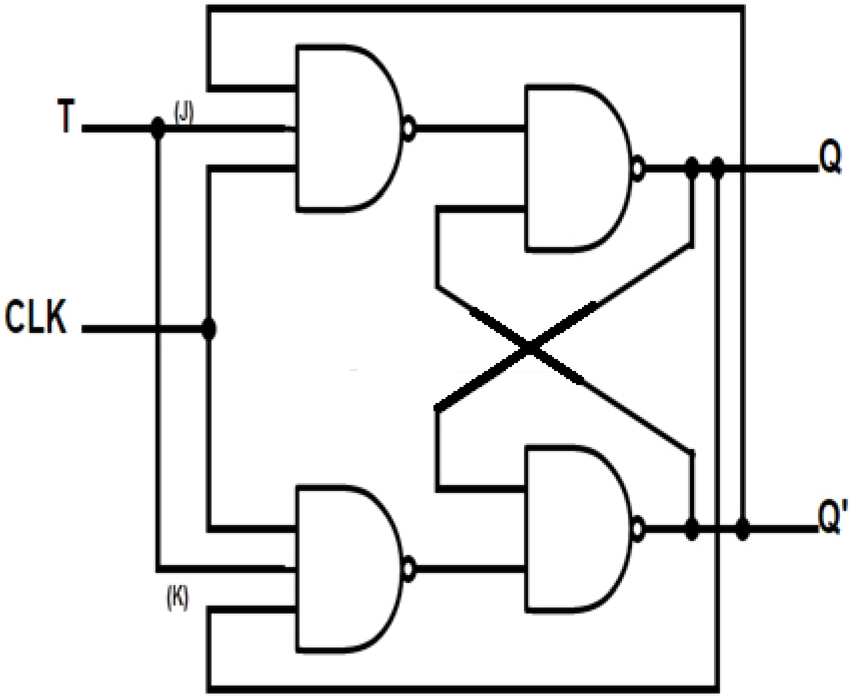


We can see from above that on the leading edge of the clock pulse the master flip-flop will be loading data from the data D input, therefore the master is "ON". With the trailing edge of the clock pulse the slave flip-flop is loading data, i.e. the slave is "ON". Then there will always be one flip-flop "ON" and the other "OFF" but never both the master and slave "ON" at the same time. Therefore, the output Q acquires the value of D, only when one complete pulse, ie, 0-1-0 is applied to the clock input.

T flip flop



Symbol: T Flip-flop



Characteristic Table

Q	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table

Clk	**T**	**Q_{n+1}**
↑	0	Q
↑	1	Q'

Excitation Table

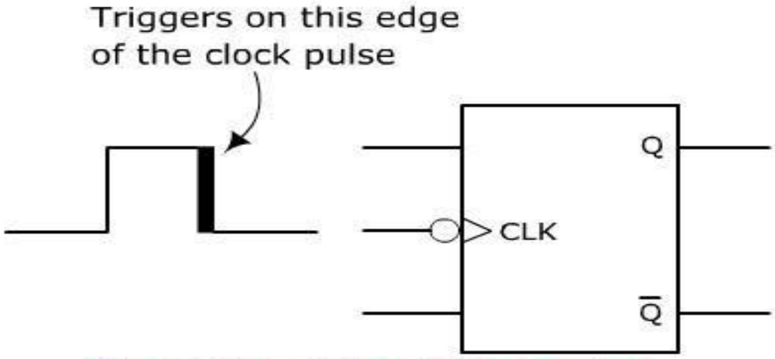
Qn	**Q_{n+1}**	**T**
0	0	0
0	1	1
1	0	1
1	1	0

Charcteristic Equation Q_{n+1}= T'Q_n+Q_n'T

Edge triggering and level triggering

Negative Edge Triggering

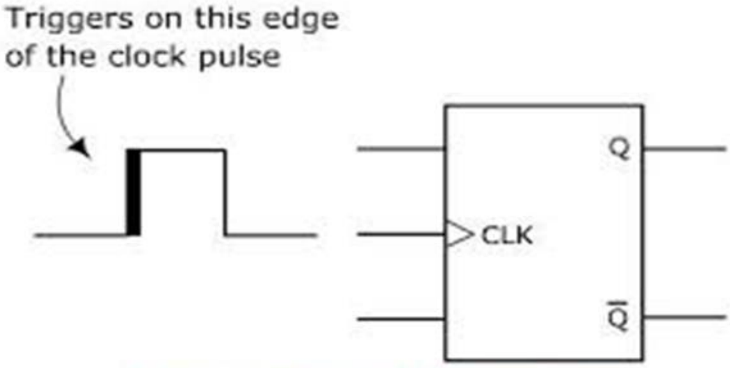
When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used.. It is mainly identified from the clock input lead along with a low-state indicator and a triangle. Take a look at the symbolic representation shown below.



Negative Edge Triggering

Positive Edge Triggering

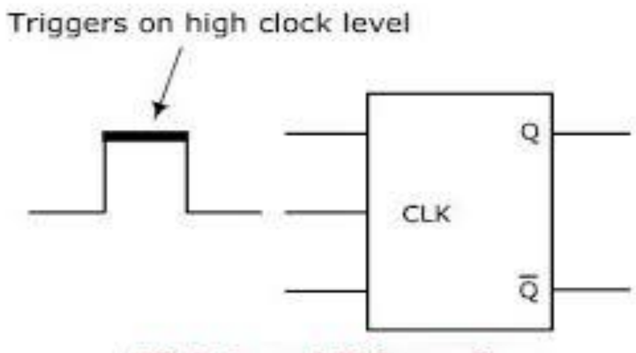
When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used. It is mainly identified from the clock input lead along with a triangle. Take a look at the symbolic representation shown below.



Positive Edge Triggering

High Level Triggering

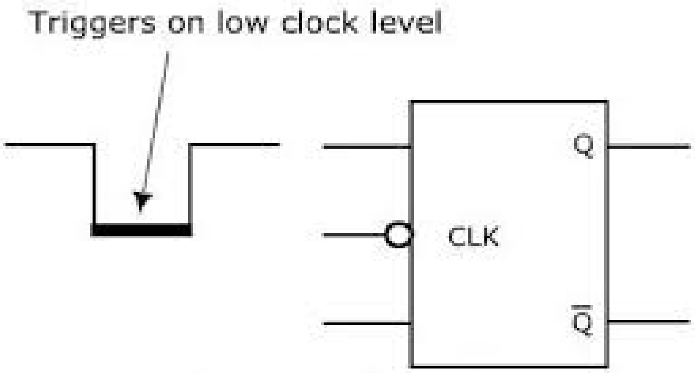
When a flip flop is required to respond at its HIGH state, a HIGH level triggering method is used. It is mainly identified from the straight lead from the clock input. Take a look at the symbolic representation shown below.



High Level Triggering

Low Level Triggering

When a flip flop is required to respond at its LOW state, a LOW level triggering method is used.. It is mainly identified from the clock input lead along with a low state indicator bubble. Take a look at the symbolic representation shown below.



Low Level Triggering

Conversion of one flip flop to another

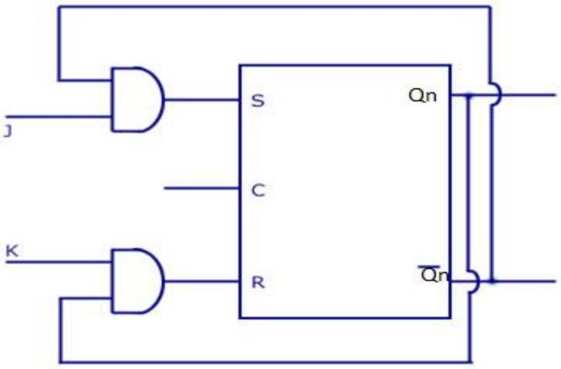
SR to JK flip flop

S-R Flip Flop to J-K Flip Flop

Conversion Table

J-K Inputs		Outputs		S-R Inputs	
J	K	Qn	Qn+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Logic Diagram



J \ KQn	00	01	11	10
0	0 ^{0}	X ^{1}	0 ^{3}	0 ^{2}
1	1 ^{4}	X ^{5}	0 ^{7}	1 ^{6}

$S = \overline{J}Qn$

J \ KQn	00	01	11	10
0	X ^{0}	0 ^{1}	1 ^{3}	X ^{2}
1	0 ^{4}	0 ^{5}	1 ^{7}	0 ^{6}

R = KQn

K-Map

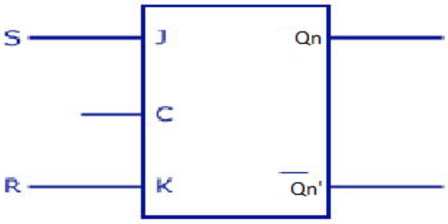
JK to SR flip flop

J-K Flip Flop to S-R Flip Flop

Conversion Table

S-R Inputs		Outputs		J-K Inputs	
S	R	Qn	Qn+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

Logic Diagram



S \ RQn	00	01	11	10
0	0 ^{0}	X ^{1}	X ^{3}	0 ^{2}
1	1 ^{4}	X ^{5}	X ^{7}	X ^{6}

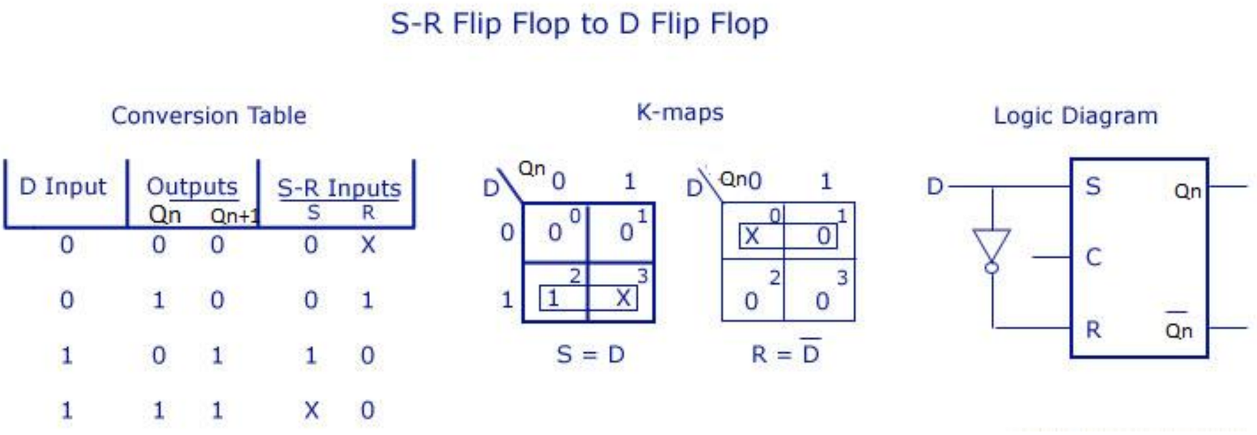
J=S

S \ R	00	01	11	10
0	X ^{0}	0 ^{1}	1 ^{3}	X ^{2}
1	X ^{4}	0 ^{5}	X ^{7}	X ^{6}

K-maps

K=R

SR to D flip flop



S-R Flip Flop to D Flip Flop

Conversion Table

D Input	Outputs		S-R Inputs	
	Qn	Qn+1	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

K-maps

D \ Qn	0	1
0	0	0
1	1	X

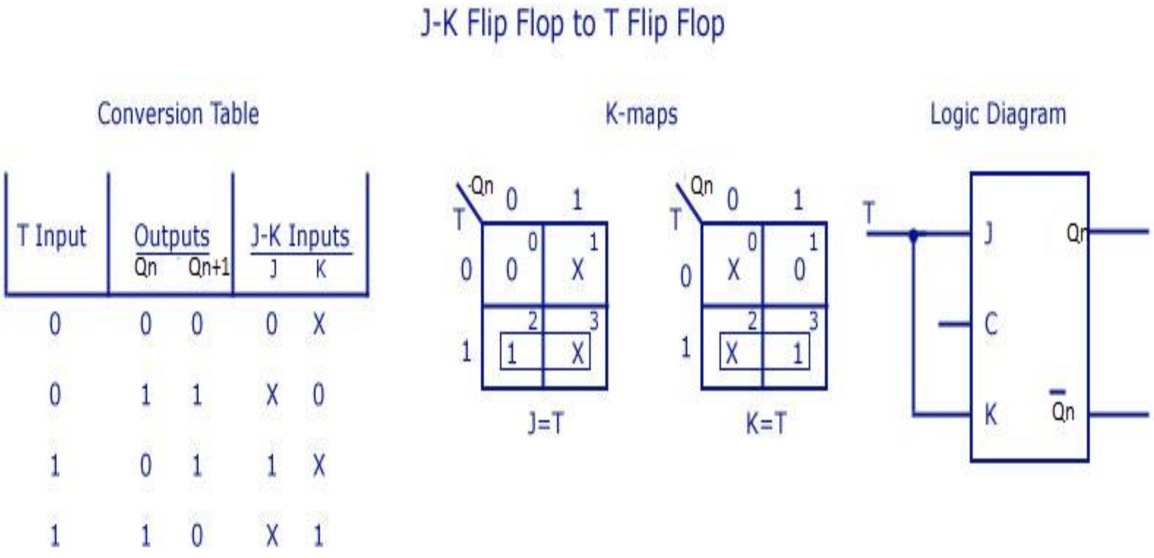
S = D

D \ Qn	0	1
0	X	0
1	0	0

$R = \overline{D}$

Logic Diagram

JK to T flip flop



J-K Flip Flop to T Flip Flop

Conversion Table

T Input	Outputs		J-K Inputs	
	Qn	Qn+1	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-maps

T \ Qn	0	1
0	0	X
1	1	X

J=T

T \ Qn	0	1
0	X	0
1	X	1

K=T

Logic Diagram