Sairam INSTITUTIONS

Sri SAI RAM ENGINEERING COLLEGE
INSTITUTE OF TECHNOLOGY
West Tambaram, Chennai - 44

YEAR	SEM
II	III

CS 8351

DIGITALPRINCIPLES AND SYSTEMDESIGN
(Common to CSE & IT)

UNIT NO. 5-MEMORY AND PROGRAMMABLE LOGIC

5.7 SEQUENTIAL PROGRAMMABLE DEVICE

Version 1.0

4 QUALITY EDUCATION

NBA NATIONAL BOARD OF ACCREDITATION

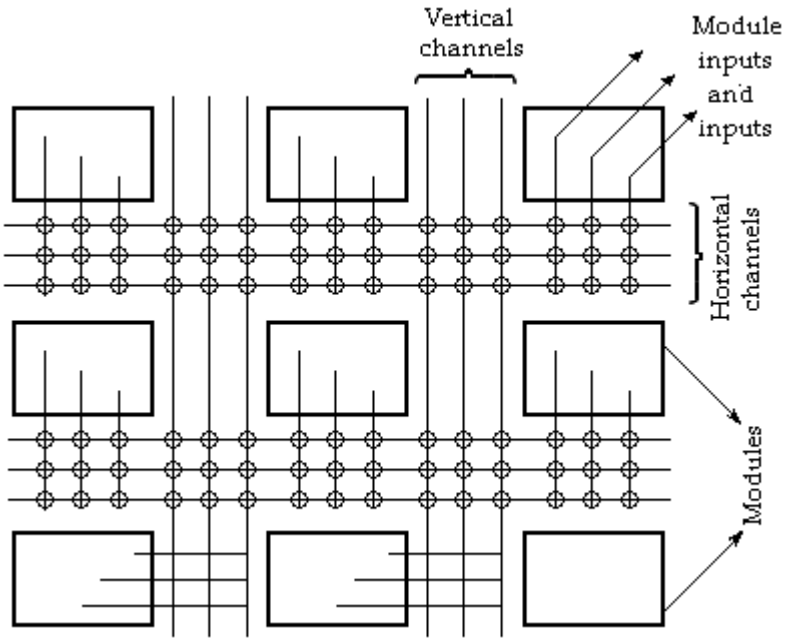
NAAC A+

nirf NATIONAL INSTITUTIONAL RANKING FRAMEWORK

BUREAU VERITAS Certification

FIELD PROGRAMMABLE GATE ARRAY: (FPGA)

Field Programmable Gate Array (FPGA) is a flexible architecture programmable logic device. The word field refers to the ability of the gate arrays to be programmed for specific function by the user. It is a Very Large Scale Integrated (VLSI) circuit constructed on a single piece of silicon. It consists of identical individually programmable rectangular modules as shown in figure below.



Architecture of FPGA

The modules are separated in both horizontal and vertical metallic conductors called *channels*. Each module has vertical and horizontal conductors at its input and output that cross one or more of the channels. Each intersection between the horizontal and vertical conductors marked as a Å in the figure, is a programmable link. These programmable links are used to interconnect the modules and also to program the individual modules.

The content of the modules depends on the type of FPGA. For easy use, the modules need to be programmable into the gates and sequential elements. A module may have both combinational and sequential components.

The logic circuit design procedure using FPGA involves the following steps:

1. Capture the logic circuit to be implemented with a suitable software package, using a library of logic elements which are various configurations of basic modules available in the FPGA. In addition, many FPGA libraries also contain predesigned circuits for multiplexers, encoders, adders and so on. Predesigned circuits make design much easier.
2. ***Functional simulation***: It simulates the circuits to determine whether it is functioning properly.
3. Configure and interconnect the modules of the FPGA to produce the desired logic circuit. This may be done automatically by routing software called **router**. Once the routing is over, it is now possible to determine the actual circuit delays which can now be introduced into the simulation model. Now,an accurate simulation of the circuit can be available.
4. ***Programming***: It is a completely automated step in which FPGA interconnections are done. The routing of the devices determined in the previous step is now made into a fuse map. Then, this fuse map is used in conjunction with a device programmer to make the internal device connections.
5. ***Testing***: After programming, it must be tested. If the designed function is not fulfilled, it must be reprogrammed. With careful simulation, reprogramming can be minimized.