Sairam INSTITUTIONS

Sri SAI RAM ENGINEERING COLLEGE
INSTITUTE OF TECHNOLOGY
West Tambaram, Chennai - 44

YEAR	SEM
II	III

CS 8351

DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to CSE & IT)

UNIT NO. 2

2.2 DESIGN PROCEDURE

Version: 1.0

4 QUALITY EDUCATION

NBA NATIONAL BOARD OF ACCREDITATION

NAAC NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL A+

nirf NATIONAL INSTITUTIONAL RANKING FRAMEWORK

ISO 9001 : 2015 BUREAU VERITAS Certification

Designing Combinational Circuits

The design procedure for combinational circuits is in many ways the reverse of the analysis procedure. It starts at the problem specification and comprises the following steps:

Determine required number of inputs and outputs from the specifications

Derive the truth table for each of the outputs based on their relationships to the input

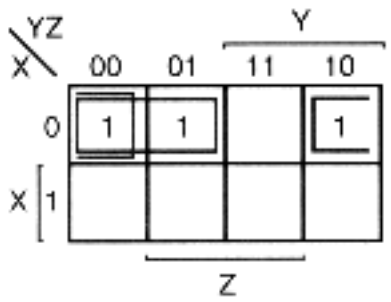
Simplify the Boolean functions for each output as a function of its inputs

Draw a logic diagram that represents the implementation of the design

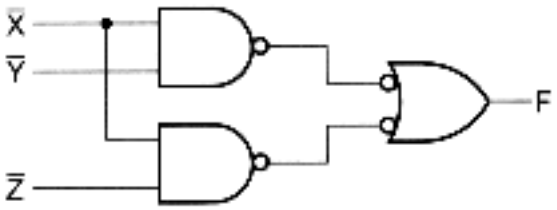
The verification of the design is by analysis of its implementation.

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(a) Truth table



(b) Map $F = \bar{X}\bar{Y} + \bar{X}\bar{Z}$



(c) Logic diagram

BCD to excess-3 code converter

Decimal	BCD input				excess-3 output			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

We start with the truth table for the code converter.

From the K-maps, we can reduce the expressions for each of the outputs to minimal sum of products.

$W = A + B\,C + B\,D \qquad = A + B(C + D)$

$X = B\,\overline{C} + B\,\overline{D} + B\,\overline{C}\,\overline{D} \qquad = B(C + D) + B\,C\,D$

$Y = \overline{C}\,\overline{D} + C\,D \qquad = C \text{ XOR } D$

$Z = \overline{D}$

Unlike in the case of minimisation for a single output, the alternative form of the expressions with further factorisation of the term (C + D) allow for the sharing of the circuits in this case. The penalty however is increased delay because there are more gates in series between the inputs and outputs.