

Reg. No.

Question Paper Code

21030


Sri SAI RAM INSTITUTE OF TECHNOLOGY
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Sai Leo Nagar, West Tambaram, Chennai - 600 044. www.sairamit.edu.in

B.E / B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2021

Fourth Semester

Common to CSE & IT

CS8491 – COMPUTER ARCHITECTURE

(Regulations 2017)

Duration: 3 Hours

Max. Marks: 100

Answer ALL Questions

PART-A (10 x 2 = 20 Marks)

1.	State Moore's law.	K1	CO1
2.	A favorite program runs in 10 seconds on computer A which has a 2GHZ clock. We have to design a computer B such that it can run the same program in 6 seconds. Determine the clock rate for computer B. Also assume that computer B requires 1.2 times as many clock cycles as computer A.	K3	CO2
3.	Multiply the given signed 2's complement numbers using bit pair recoding Multiplier= 011011 (+27) Multiplicand = 110101 (-11)	K3	CO3
4.	What is the need for carry look ahead adder?	K2	CO3
5.	Create a data path diagram for fetching the instruction from memory and incrementing the program counter.	K5	CO4
6.	Differentiate between data hazard and control hazard.	K4	CO4
7.	State Amdahl's law.	K1	CO5
8.	What is meant by hardware multithreading?	K1	CO5
9.	How will you evaluate or measure the performance of cache memory?	K6	CO6
10.	What is meant by bus arbitration?	K1	CO6

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 - Create

PART – B (5 x 13 = 65 marks)

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|-----|----|---|----|----|-----|
| 11. | a) | Explain in detail about the functional units of a computer system. | 13 | K2 | CO1 |
| | | OR | | | |
| | b) | What are the metrics involved in measuring the performance of a computer? Give examples. | 13 | K4 | CO2 |
| 12. | a) | Explain the working of carry look ahead adder with a neat sketch. | 13 | K3 | CO3 |
| | | OR | | | |
| | b) | Divide $(12)_{10}$ by $(3)_{10}$ using Restoring and Non restoring division algorithm with step by step intermediate results and explain. | 13 | K5 | CO3 |
| 13. | a) | Draw and explain the data path for a branch instruction with necessary control lines | 13 | K6 | CO4 |
| | | OR | | | |
| | b) | Explain in detail about the types of hazards in pipelining? | 13 | K2 | CO5 |
| 14. | a) | Discuss about Flynn's classification in detail. | 13 | K2 | CO5 |
| | | OR | | | |
| | b) | Write notes on hardware multithreading. Compare and contrast Fine grained multithreading with Coarse grained multithreading. | 13 | K2 | CO5 |
| 15. | a) | Explain about bus arbitration schemes. | 13 | K1 | CO6 |
| | | OR | | | |
| | b) | What is virtual memory? How can you implement virtual memory in a computer? | 13 | K1 | CO6 |

PART C (1 X 15 = 15 Marks)

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|-----|----|---|----|----|-----|
| 16. | a) | Write notes on Graphics processing units and shared memory multiprocessors with relevant examples. Also explain a scenario of where the above technologies can be used. | 15 | K2 | CO5 |
| | | OR | | | |
| | b) | (i) A Block set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,834 blocks and each block contains 256 -8 bit words. How many bits are required for addressing the main memory and how many bits are required to represent the TAG, SET & WORD fields? | 8 | K1 | CO6 |
| | | (ii) Consider a direct mapped cache with 8 cache blocks(0-7).If the memory block requests are in the order 3,5,2,8,0,6,3,9,16,20,17,25,18,30,5,24.which of the following memory blocks will not be in the cache at the end of the sequence. | 7 | K1 | CO6 |