Sairam INSTITUTIONS

Sri SAI RAM ENGINEERING COLLEGE
INSTITUTE OF TECHNOLOGY
West Tambaram, Chennai - 44

YEAR	SEM
II	III

CS8351

Digital Principles and System Design
(Common to CSE and IT)

UNIT IV ASYNCHRONOUS SEQUENTIAL LOGIC

4.6 HAZARDS

HAZARDS

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

Hazards occur in combinational circuits, where they may cause a temporary false-output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state.

Hazards in Combinational Circuits:

A hazard is a condition where a single variable change produces a momentary output change when no output change should occur.

Types of Hazards:

Static hazard

Dynamic hazard

Static Hazard

In digital systems, there are only two possible outputs, a ‘0’ or a ‘1’. The hazard may produce a wrong ‘0’ or a wrong ‘1’. Based on these observations, there are three types,

Static- 0 hazard,

Static- 1 hazard,

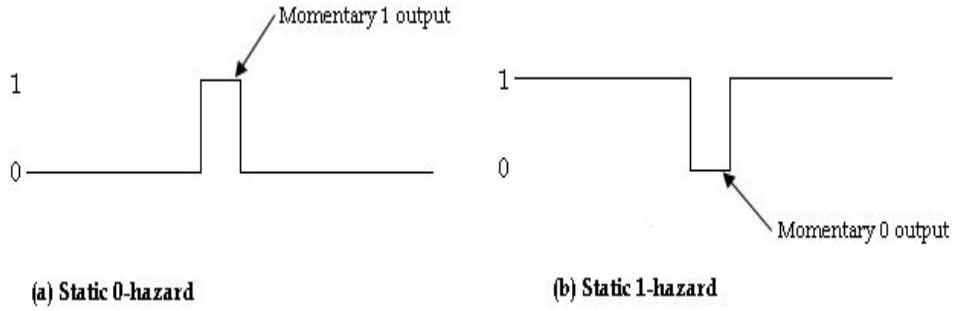
Static- 0 hazard:

When the output of the circuit is to remain at 0, and a momentary 1

output is possible during the transmission between the two inputs, then the hazard is called a static 0-hazard.

Static- 1 hazard:

When the output of the circuit is to remain at 1, and a momentary 0 output is possible during the transmission between the two inputs, then the hazard is called a static 1-hazard.

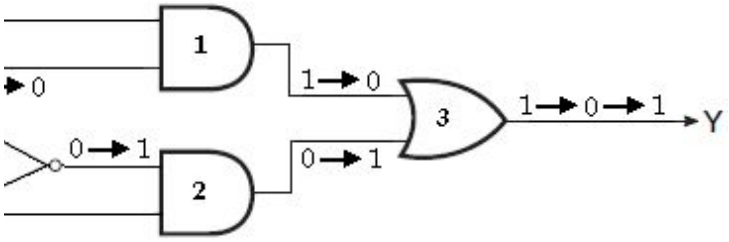


(a) Static 0-hazard (b) Static 1-hazard

The below circuit demonstrates the occurrence of a static 1-hazard. Assume that all three inputs are initially equal to 1 i.e., X1X2X3= 111. This causes the output of the gate 1 to be 1, that of gate 2 to be 0, and the output of the circuit to be equal to 1. Now consider a change of X2 from 1 to 0 i.e., X1X2X3= 101. The output of gate 1 changes to 0 and that of gate 2 changes to 1, leaving the output at 1. The output may momentarily go to 0 if the propagation delay through the inverter is taken into consideration.

The delay in the inverter may cause the output of gate 1 to change to 0 before the output of gate 2 changes to 1. In that case, both inputs of gate 3 are momentarily equal to 0, causing the output to go to 0 for the short interval of time that the input signal from X2 is delayed while it is propagating through the inverter circuit.

Thus, a static 1-hazard exists during the transition between the input states X1X2X3= 111 and X1X2X3= 101.

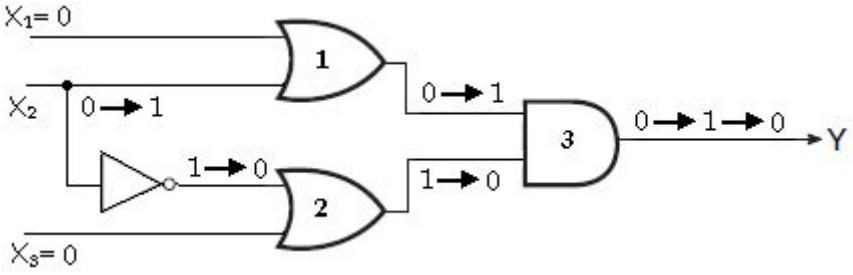


Circuit with static-1 hazard

Now consider the below network, and assume that the inverter has an appreciably greater propagation delay time than the other gates. In this case there is a static 0-hazard in the transition between the input states X1X2X3= 000 and X1X2X3= 010 since it is possible for a logic-1 signal to appear at both input terminals of the AND gate for a short duration.

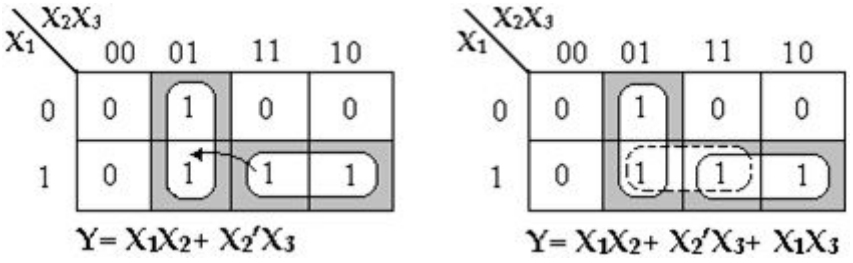
The delay in the inverter may cause the output of gate 1 to change to 1 before the output of gate 2 changes to 0. In that case, both inputs of gate 3 are momentarily equal to 0, causing the output to go to 1 for the short interval of time that the input signal from X2 is delayed while it is propagating through the inverter circuit.

Thus, a static 0-hazard exists during the transition between the input states X1X2X3= 000 and X1X2X3= 010.



Circuit with static-0 hazard

A hazard can be detected by inspection of the map of the particular circuit. To illustrate, consider the map in the circuit with static 0-hazard, which is a plot of the function implemented. The change in X2 from *1* to 0 moves the circuit from minterm 111 to minterm 101. The hazard exists because the change in input results in a different product term covering the two min terms.



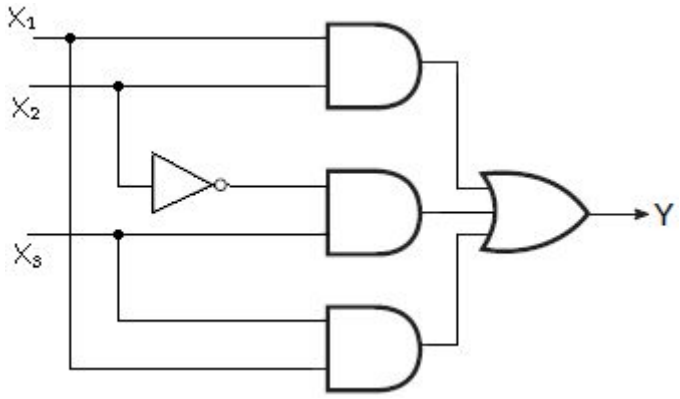
Maps demonstrating a Hazard and its Removal

The minterm 111 is covered by the product term implemented in gate 1 and minterm 101 is covered by the product term implemented in gate 2. Whenever the circuit must move from one product term to another, there is a possibility of a momentary interval when neither term is equal to 1, giving rise to an undesirable 0 output.

The remedy for eliminating a hazard is to enclose the two minterms in question with another product term that overlaps both groupings.

This situation is shown in the *map* above, where the two terms that causes the hazard are combined into one product term. The hazard- free circuit obtained by this combinational is shown below.

Hazard-free Circuit

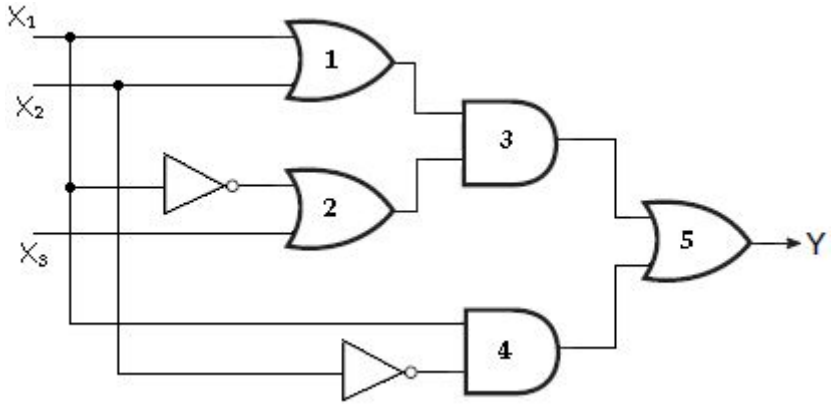


The extra gate in the circuit generates the product term X1X4. The hazards in combinational circuits can be removed by covering any two minterms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

Dynamic Hazard

A dynamic hazard is defined as a transient change occurring three or more times at an output terminal of a logic network when the output is supposed to change only once during a transition between two input states differing in the value of one variable.

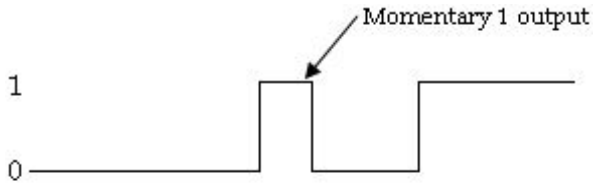
Now consider the input states X1X2X3= 000 and X1X2X3= 100. For the first input state, the steady state output is 0; while for the second input state, the steady state output is 1. To facilitate the discussion of the transient behavior of this network, assume there are no propagation delays through gates G3 and G5 and that the propagation delays of the other three gates are such that G1 can switch faster than G2 and G2 can switch faster than G4.



Circuit with Dynamic hazard

When X1 changes from 0 to 1, the change propagates through gate G1 before gate G2 with the net effect that the inputs to gate G3 are simultaneously 1 and the network output changes from 0 to 1. Then, when X1 change propagates through gate G2, the lower input to gate G3 becomes 0 and the network output changes back to 0.

Finally, when the X1= 1 signal propagates through gate G4, the lower input to gate G5 becomes 1 and the network output again changes to 1. It is therefore seen that during the change of X1 variable from 0 to 1 the output undergoes the sequence, 0 ->1 -> 0 -> 1, which results in three changes when it should have undergone only a single change.



Dynamic hazard

Essential Hazard

An essential hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause such a hazard. Essential hazards elimination:

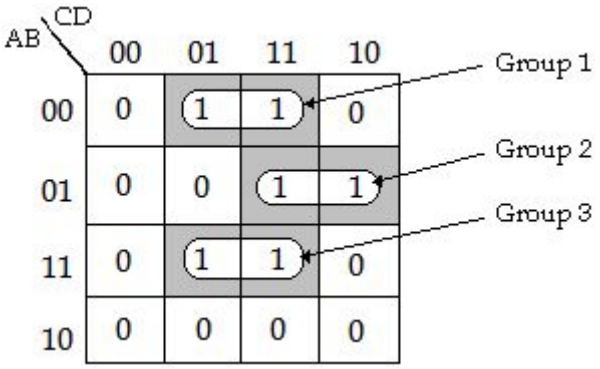
Essential hazards can be eliminated by adjusting the amount of delays in the affected path. To avoid essential hazards, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared with delays of other signals that originate from the input terminals.

Design Of Hazard Free Circuits

1. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (1, 3, 6, 7, 13, 15)

Soln:

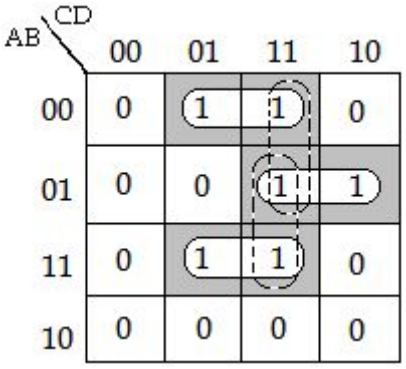
a) <u>K-map Implementation and grouping</u>



F=A'B'D+ A'BC+ ABD

b) Hazard- free realization

The first additional product term A'CD, overlapping two groups (group 1 & 2) and the second additional product term, BCD, overlapping the two groups (group 2 & 3).

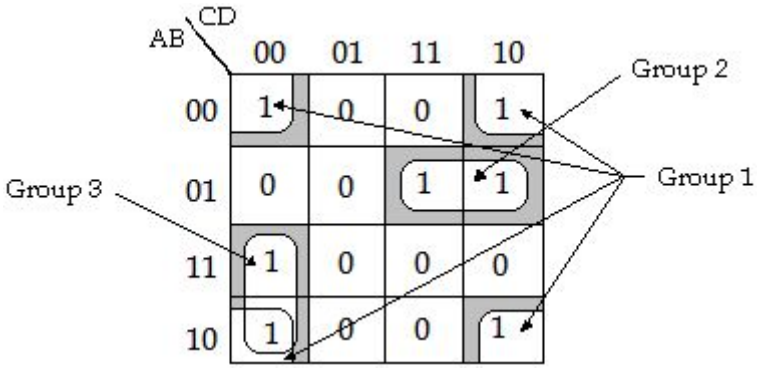


F=A'B'D+ A'BC+ ABD+ A'CD+ BCD

2. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 2, 6, 7, 8, 10, 12).

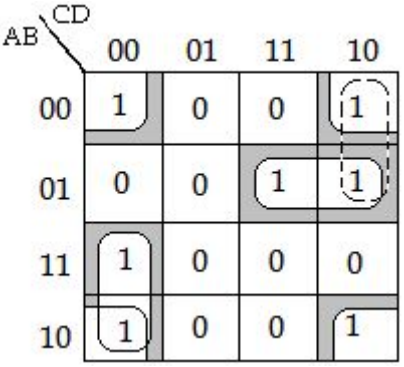
Soln:

a) K-map Implementation and grouping



a) Hazard- free realization

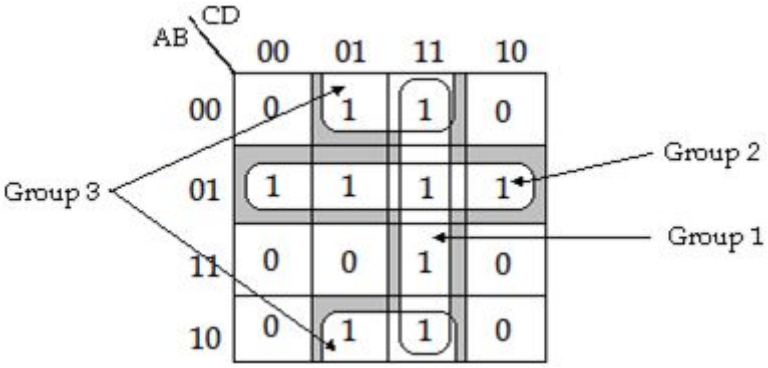
The additional product term, A'CD' overlapping two groups (group 1 & 2) for hazard free realization. Group 1 and 3 are already overlapped hence they do not require additional minterm for grouping.



F= B'D'+ A'BC+ AC'D'+ A'CD'

3. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (1, 3, 4, 5, 6, 7, 9, 11, 15).

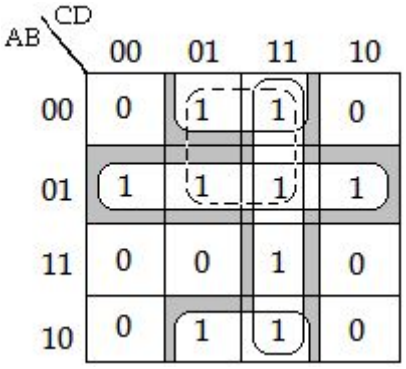
a) <u>K-map Implementation and grouping</u>



<u>F= CD+ A'B+ B'D</u>

b) Hazard- free realization

The additional product term, A'D overlapping two groups (group 2 & 3) for hazard free realization. Group 1 and 2 are already overlapped hence they do not require additional minterm for grouping.

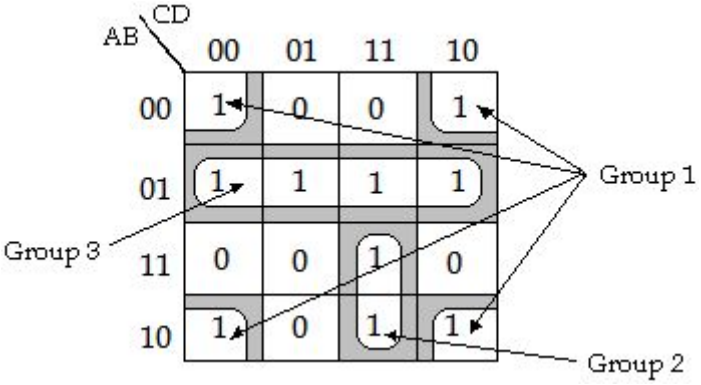


F= CD+ A'B+ B'D+ A'D

4. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 2, 4, 5, 6, 7, 8, 10, 11, 15).

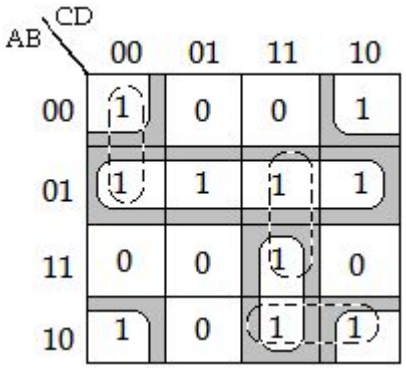
Soln:

a) <u>K-map Implementation and grouping</u>



<u>F= B'D'+ A'B+ ACD</u>

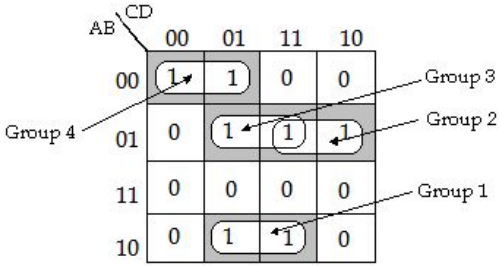
b) Hazard- free realization



F= B'D'+ A'B+ ACD+ A'C'D'+ BCD+ AB'C

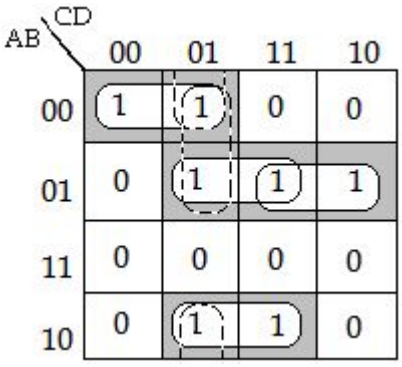
5. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 1, 5, 6, 7, 9, 11).

a) K-map Implementation and grouping



F= AB'D+ A'BC+ A'BD+ A'B'C'

b) Hazard- free realization:



F= AB'D+ A'BC+ A'BD+ A'B'C'+ A'C'D+ B'C'D