Sairam INSTITUTIONS

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YEAR II | SEM III

# CS 8351

## DIGITAL PRINCIPLES AND SYSTEM DESIGN
## (Common to CSE & IT)

## UNIT NO. V

## 5.1 RANDOM ACCESS MEMORY

Version: 1.0

# RANDOM ACCESS MEMORY

## Classification of Memories

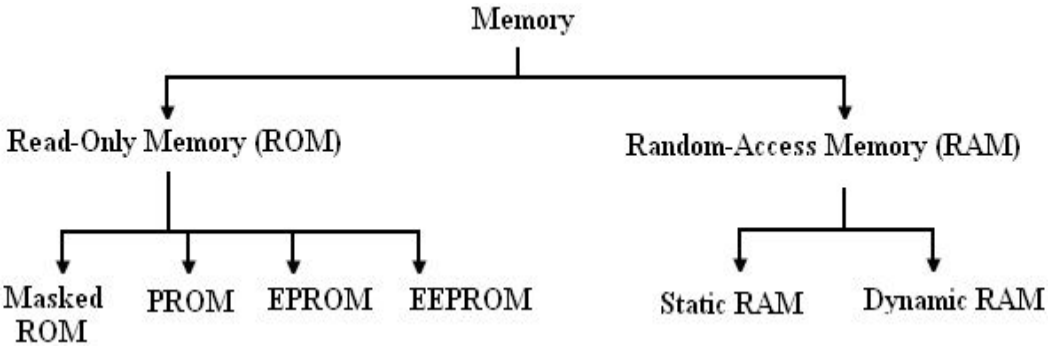
There are two types of memories that are used in digital systems:

1.Random-Access Memory

2.(RAM),Read-Only Memory (ROM).

**RAM** (random-access memory) is a type of memory in which all addresses are accessible in an equal amount of time and can be selected in any order for a read or write operation. All RAMs have both read and write capability. Because RAMs lose stored data when the power is turned off, they are ***volatile*** memories.

**ROM** (read-only memory) is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation as in the RAM. The ROM, like the RAM, is a random-access memory but the term RAM traditionally means a random-access read/write memory.Because ROMs retain stored data even if power is turned off, they are ***nonvolatile*** memories.




## RANDOM-ACCESS MEMORIES (RAMS)

RAMs are read/write memories in which data can be written into or read from any selected address in any sequence. When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new data unit. When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation. This nondestructive read operation can be viewed as copying the content of an address while leaving the content intact.

A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off.

The two categories of RAM are the ***static* RAM** (SRAM) and the ***dynamic* RAM** (DRAM). Static RAMs generally use flip-flops as storage elements and can therefore store data indefinitely *as long as dc power is applied*. Dynamic RAMs use

capacitors as storage elements and cannot retain data very long without the capacitors being recharged by a process called **refreshing**. Both SRAMs and DRAMs will lose stored data when dc power is removed and, therefore, are classified as ***volatile memories***.

Data can be read much faster from SRAMs than from DRAMs. However, DRAMs can store much more data than SRAMs for a given physical size and cost because the DRAM cell is much simpler, and more cells can be crammed into a given chip area than in the SRAM.

## Static RAM (SRAM)

### Storage Cell:

All static RAMs are characterized by flip-flop memory cells. As long as dc power is applied to a static memory cell, it can retain a 1 or 0 state indefinitely. If power is removed, the stored data bit is lost.

The cell is selected by an active level on the Select line and a data bit (I or 0) is written into the cell by placing it on the Data in line. A data bit is read by taking it off the Data out line.

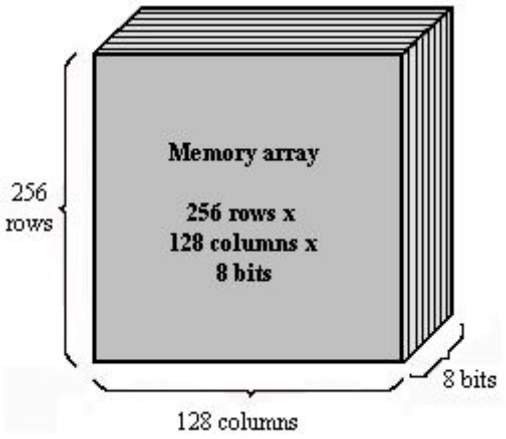
### Basic SRAM Organisation:

#### Basic Static Memory Cell Array

The memory cells in a SRAM are organized in rows and columns. All the cells in a row share the same Row Select line. Each set of Data in and Data out lines go to each cell in a given column and are

connected to a single data line that serves as both an input and output (Data I/O) through the data input and data output buffers.

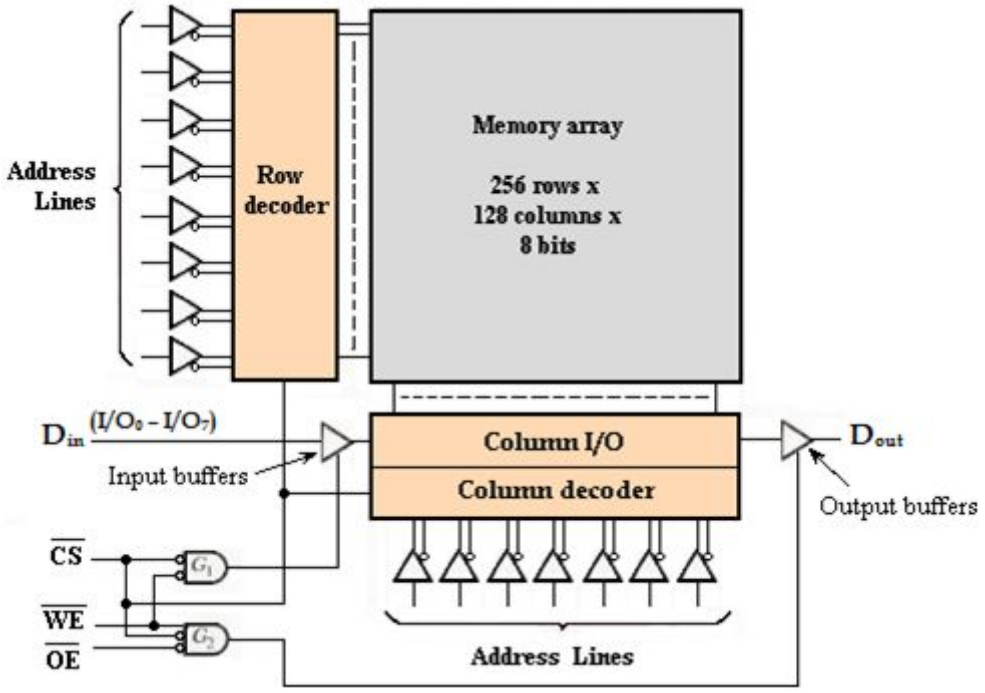
SRAM chips can be organized in single bits, nibbles (4 bits), bytes (8 bits), or multiple bytes (16, 24, 32 bits, etc.). The memory cell array is arranged in 256 rows and 128 columns, each with 8 bits as shown below. There are actually 215 = 32,768 addresses and each address contains 8 bits. The capacity of this example memory is 32,768 bytes (typically expressed as 32 kbytes).




**Operation:**

The SRAM works as follows. First, the chip select, CS, must be LOW for the memory to operate. Eight of the fifteen address lines are decoded by the row decoder to select one of the 256 rows. Seven of

the fifteen address lines are decoded by the column decoder to select one of the 128 8-bit columns.




Read:

In the READ mode, the write enable input, WE‘ is HIGH and the output enable, OE_ is LOW. The input tristate buffers are disabled by gate G1, and the column output tristate buffers are enabled by gate G2. Therefore, the eight data bits from the selected address are routed through the column I/O to the data lines (I/O1through I/O7), which are acting as data output lines.

**Write:**

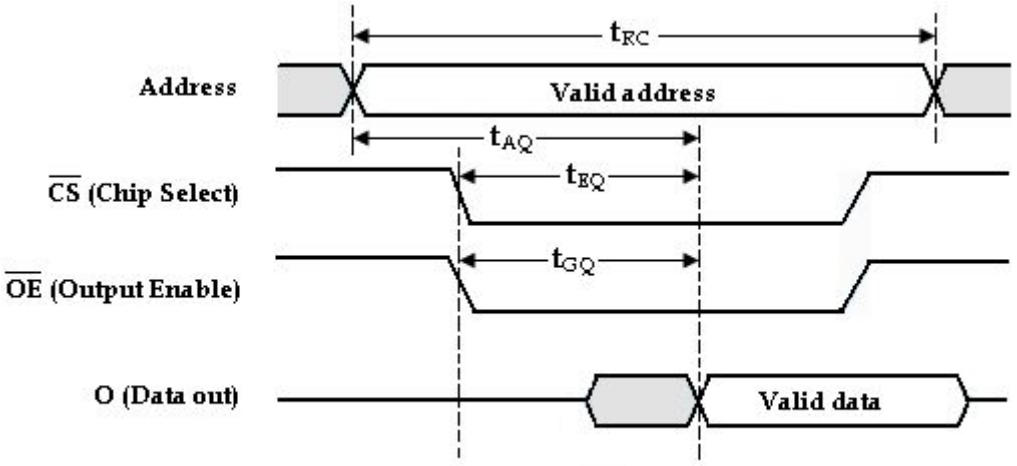
In the WRITE mode, WE‘ is LOW and OE‘ is HIGH. The input buffers are enabled by gate G1, and the output buffers are disabled by gate G2. Therefore the eight input data bits on the data lines are routed through the input data control and the column I/O to the selected address and stored.

**Read and Write Cycles:**

For the read cycle shown in part (a), a valid address code is applied to the address lines for a specified time interval called the ***read cycle time***, tWC. Next, the chip select (CS) and the output enable (DE) inputs go LOW. One time interval after

the DE input goes LOW; a valid data byte from the selected address appears on the data lines. This time interval is called the ***output enable access time***, tGQ. Two other access times for the read cycle are the ***address access time***, tAQ, measured from the beginning of a valid address to the appearance of valid data on the data lines and the **chip enable access time**, tEQ, measured from the HIGH-to-LOW transition of CS to the appearance of valid data on the data lines.

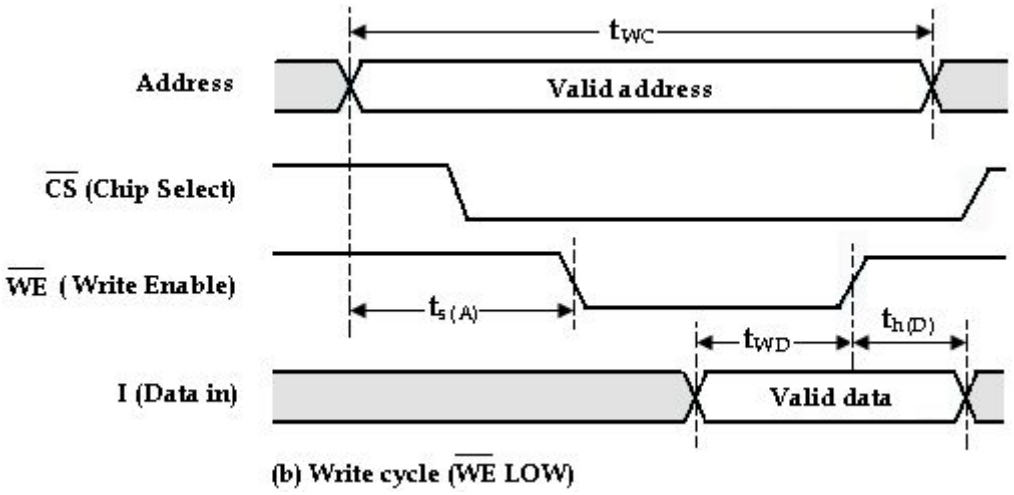
During each read cycle, one unit of data, a byte in this case is read from the memory.




(a) Read Cycle ($\overline{WE}$ HIGH)

For the write cycle shown in Figure (b), a valid address code is applied to the address lines for a specified time interval called the ***write cycle time***, tWE . Next, the chip select (CS) and the write enable (WE) in puts go LOW. The required time interval from the beginning of a valid address until the WE input goes LOW is called the ***address setup time***, t s(A). The time that the WE input must be LOW is the write pulse width. The time that the input WE must remain LOW after valid data are applied to the data inputs is designated t WD; the time that the valid input data must remain on the data lines after the WE input goes HIGH is the data hold time, t h(D).

During each write cycle, one unit of data is written into the memory.



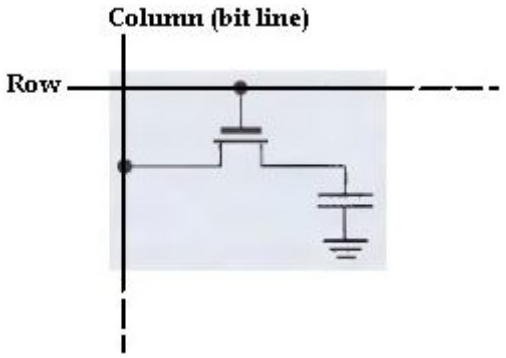
(b) Write cycle ($\overline{WE}$ LOW)

## Dynamic RAM (DRAM)

### Dynamic RAM Cell:

Dynamic memory cells store a data bit in the form of electric charges on capacitors. The basic storage device in DRAM is not a flip-flop but a simple MOSFET and a capacitor.

The advantage of this type of cell is that it is very simple, thus allowing very large memory arrays to be constructed on a chip at a lower cost per bit. The disadvantage is that the storage capacitor cannot hold its charge over an extended period of time and will lose the stored data bit unless its charge is refreshed periodically. To refresh requires additional memory circuitry and complicates the operation of the DRAM.




DRAM memory cell

In DRAM memory cell, a bit of data is stored as charge on storage capacitor, where the presence or absence of charge determines the value of the stored bit 1 or 0.

The DRAM cell includes a single MOS transistor (MOSFET) and a capacitor. When column line and row line go high, the MOSFET conducts and charges the capacitor. When the column and row lines go low, the MOSFET opens and the capacitor retains its charge. In this way it stores 1 bit.

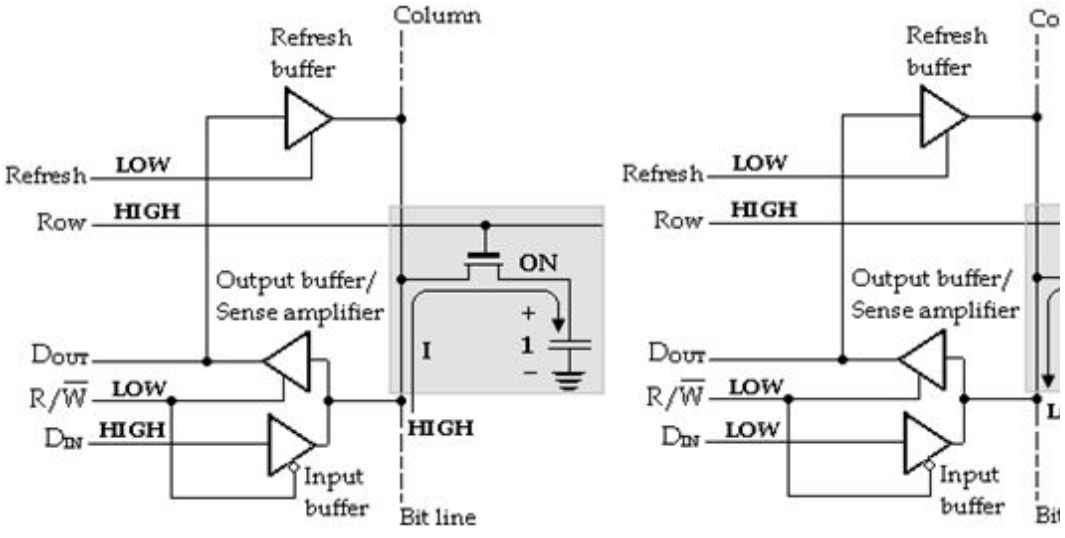
## Operation:

The DRAM cell consists of 3 tri-state buffers: Input buffer, Output buffer and refresh buffer. Input and output buffers are enabled and disabled by controlling R/W‘ line. When R/W‘= 0, input buffer is enabled and output buffer is disabled. When R/W‘= 1, input buffer is disabled and output buffer is enabled.

(i)Write:

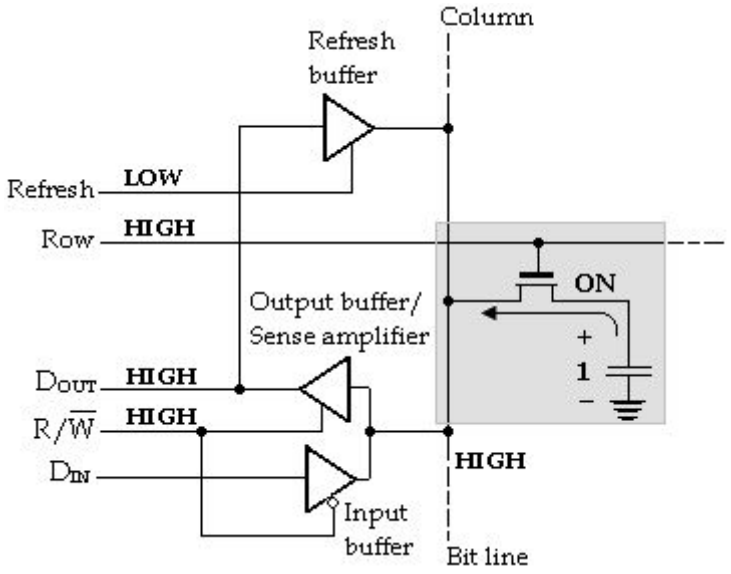
To enable write operation R/W‘ line is made low, which enables input buffer and disables output buffer. To write a 1 into the cell, the DIN line is high and MOSFET is turned ON by a high on the row line. This allows the capacitor to charge to a positive voltage. When 0 is to be stored, a low is applied to the DIN line. The capacitor remains unchanged or if it is storing a 1, it discharges.

When the row line is made low, the transistor turns OFF and disconnects the capacitor from the data line, thus storing the charge (1 or 0) on the capacitor.



**(ii) Read:**

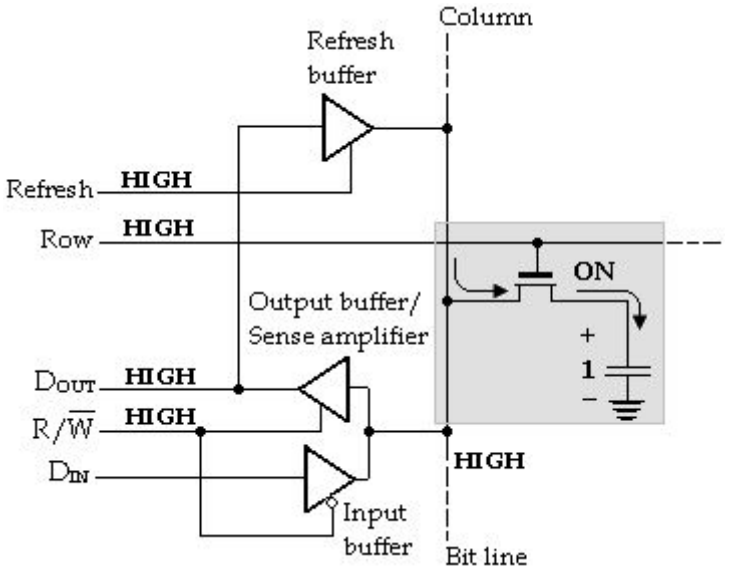
To read data from the cell, the R/W‘ line is made HIGH, which enables output buffer and disables input buffer. When the row line is made HIGH, the transistor turns ON and connects the capacitor to the DOUT line through output buffer.




Reading a 1 from the memory cell

### (iii) Refresh:

For refreshing the memory cell, the R/W line is HIGH, the row line is HIGH, and the refresh line is HIGH. The transistor turns on, connecting the capacitor to the bit line. The output buffer is enabled, and the stored data bit is applied to the input of the refresh buffer, which is enabled by the HIGH on the refresh input. This produces a voltage on the bit line corresponding to the stored bit thus refreshing the capacitor.




**Refreshing a stored 1**

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