



B.E./ B. Tech. Degree Examination

CONTINUOUS ASSESSMENT TEST-I [CSE/IT]

Subject Name: Digital Principles and System Design
Subject code: CS8351
Branch\year\sem: T\II\III

Digital Principles and System Design
Date: 10.00-11.30am
Date: 18.8.2020
Max. Marks: 50

$\underline{PART - A} \qquad (5*2=10)$

ANSWER ALL QUESTIONS

- 1. What is meant by weighted and non weighted coding?[R][CO1]
- 2. Convert 1101101110.100110 to hexadecimal equivalent.[A][CO1]
- 3. State DeMorgan 's theorem.[CO1]
- 4. State various laws of Boolean algebra.[U][CO1]
- 5. Prove A+AB=A.(A)[CO1]

<u>PART -B</u> (2*13=26 Marks)

6 a).i) Convert the expression in standards SOP form [U][CO1] (13)

i)
$$F(A,B,C) = A + BC$$
 [A] [CO1]

- ii)Convert (A+B)(B+C) (A+C) into standard POS form [U][CO1]
- iii) Convert the given expression in standard SOP form [U] (CO1)

$$F(A,B,C)=AB+BC+CA$$

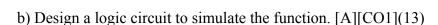
(OR)

- b) State and prove various properties and laws of boolean algebra also prove (13)

 Demorgans theorem [A][CO1]
- 7. a) Minimize the expression using K-Map[A][CO1]

$$F(A,B,C,D)=\sum m(0,2,4,5,6,8,10,15) + d(7,13,14)$$

$$F(A,B,C,D) = \prod M(0,2,3,8,9,12,13,15)$$



- (i) F= AB+ABC+A'BC+AB'+D using only NAND gates
- ii) Y= AC+BC+AB+D using only NOR gates

PART -C (1*14=14 Marks)

- 8. a) i) Design full adder using two half adders(AN)[CO2]
 - ii) Design a 4 bit parallel adder using full adders.(AN)[CO2]

СО	CS8351 DIGITAL PRINCIPLES AND SYSTEM DESIGN	DICITAL PRINCIPLES AND SYSTEM DESIGN	L	T	P	C
		4	0	0	4	
C202.1	Simplify Boolean functions using KMap.					
(CO1)						
C202.2	Design and Analyze Combinational and Sequential Circuits					
(CO2)						
C202.3	Implement designs using Programmable Logic Devices. Write HDL codes for combinational and					
(CO3)	sequential circuits.					
C202.4	Analyze a memory cell and apply for organizing larger memory.					
(CO4)						
C202.5	Understand and compare the concepts of programmable logic devices. Develop HDL programs for					
(CO5)	combinational and sequential circuits					