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B.E./ B. Tech. Degree Examination

Department of Computer Science and Engineering/ Information Technology

CONTINUOUS ASSESSMENT TEST III

Subject: Computer Architecture **Duration: 3 hours**

Subject Code: CS8491 **Date: 22.06.2021**

Branch: CSE & IT **Max. Marks: 100**

PART – A **(10 x 2 = 20 marks)**

1. State Amdahl's law. [K2] [CO1]
2. List R-type instructions? [K1] [CO1]
3. Define Throughput and Response Time. [K1] [CO2]
4. How overflow exception for addition and subtraction is handles in MIPS [K4] [CO3]
5. Interpret subword parallelism? [K2] [CO3]
6. Define a datapath in CPU. [K2] [CO4]
7. Name the control signals required to perform arithmetic operations. [K1] [CO4]
8. Define the terms Pipeline Bubble and Hazards. [K2] [CO5]
9. State the need for Instruction Level Parallelism. [K2] [CO5]
10. Define Cache hit and Cache Miss. [K1][CO6]

PART - B **(5 x 13 = 65 marks)**

11. a. Illustrate with suitable examples various addressing modes and MIPS addressing modes. [K2] [CO1] (13)

Or

b. Discuss various functional components of a computer system and the basic operational concepts. [K2] [CO1] (13)

12. a. Discuss the measures of the performance of the computer and derive the basic performance equation. [K2] [CO2] (13)

Or

b. i. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250ns and a CPI of 2.0 for some programs and computer B has a clock cycle time of 500ns and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much? [K3] [CO2] (5)

ii.If computer A runs a program in 10 seconds and computer B runs the same program in 15 seconds, how much faster is A than B? [K3] [CO2] (3)

iii. Our favorite program runs in 10 seconds on computer A, which has a 2 GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? [K3] [CO2] (5)

13. a. Explain the hardware implementation of floating point addition and subtraction. Also write the rules to perform addition and perform binary floating point addition between 0.5 10 and -0.4375 10. [K3] [CO3] (13)

Or

b. Explain restoring and non restoring algorithms with suitable examples. [K3] [CO3] (13)

14. a. Explain the operation of the data path for an R-type, Load Word, branch, jump instructions in detail. [K4] [CO4] (13)

Or

b. Draw and explain the functional block diagram with control signals for basic implementation of MIPS subset. [K2] [CO4] (13)

15.a. Explain in detail about various categories and hazards with example. [K2] [CO5] (13)

Or

b. Write short notes on multicore processors and Hardware Multithreading. [K2] [CO5] (13)

PART– C (**1x15=15)**

16.a Explain the DMA controller and illustrate how DMA controller is used for direct data transfer between memory and peripherals? [K1][CO6](15)

(OR)

b) i) What is virtual memory? Explain the steps involved in virtual memory address translation. [K1][CO6](10)

(ii) Differentiate Programmed I/O and Interrupt I/O. [K1][CO6](5)

Course Outcomes:

CO1: Understand the physical and logical aspects of Computer System. (K2)

CO2: Analyze the various parameters of the processor to improve system performance. (K4)

CO3: Evaluate the fixed and floating point arithmetic operations. (K5)

CO4: Design data path and control unit of computer system. (K6)

CO5: Understand parallel processing architectures with pipelining and avoidance of hazards (K2)

CO6: Define the various components of computer system hardware.(K1)