Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S, FE) / S2 (PT) (S) Examination January 2024 (2019 Scheme)

Course Code: CST 202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Explain how addressing modes contribute to the efficiency and flexibility of computer architecture.	(3)
2	What are the steps involved in the execution of an instruction in computer architecture? Provide a brief overview of these steps.	(3)
3	Differentiate between arithmetic and logic micro operations in the context of register transfer logic. Provide examples for each type of operation.	(3)
4	What is the role of the accumulator in a processor unit? How does it contribute to arithmetic and logic operations within the system?	(3)
5	Highlight the key steps involved in the restoring method for binary division.	(3)
6	Differentiate between instruction and arithmetic pipelines.	(3)
7	Give the key characteristics of PLA-based control organization and its advantages.	(3)
8	Enumerate the differences between hardwired control and microprogram control.	(3)
9	What is the role of interrupts in I/O organization? List the sequence of steps that follow an interrupt request.	(3)
10	List the key features of semiconductor RAMs. How do these features contribute to their widespread use in modern computer systems?	(3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	In a three-bus structure, give the control sequence for the instruction SUB R3, (R4). Explain each step and the role of control signals in the execution of this instruction.	(8)
	b)	Compare the execution of instructions during straight-line sequencing and	(6)

branching. Support your explanation with relevant examples, highlighting the impact on the instruction cycle.

12 a) Draw the block diagram of a single-bus organization and outline the control sequence for the instruction SUB (R2), R3 in this organizational structure. Provide an explanation of each step in the control sequence. (8)

b) In the context of addressing modes, elaborate on the concept of indirect addressing. Provide examples and explain how it contributes to the flexibility and versatility of instruction sequences in computer architecture. (6)

Module -2

13 a) Show the hardware implementation for executing the statement xT_1: A ← B. (7)

b) Design a 4-bit combinational logic shifter with two control variables, H1 and H0. Specify the operations for each control variable. (7)

14 a) Illustrate the design and functioning of a 4-bit arithmetic circuit within an ALU. Explain how this circuit performs addition and subtraction operations, providing a step-by-step breakdown of the processes involved. (7)

b) Explain the principles and applications of I/O mapped I/O and memory mapped I/O. Evaluate the advantages and disadvantages of each mapping technique (7)

Module -3

15 a) Draw the flow chart of Booth's multiplication algorithm. Multiply (+24) and (-21) using Booth's multiplication algorithm. (8)

b) Explain the principle of pipelining and discuss how it enhances the overall performance of a processor. Provide examples to support your explanation. (6)

16 a) Analyze the hazards associated with pipeline processors and propose solutions for overcoming data hazards in pipeline architecture. (8)

b) Design a 4x4 array multiplier and explain the steps involved in multiplying two binary numbers using this multiplier. (6)

Module -4

17 a) Design a hardwired control circuit for a processor unit that performs the addition and subtraction of two fixed-point numbers represented in sign-magnitude form. (10)

b) Differentiate between vertical and horizontal micro instructions. (4)

18 a) Design a microprogrammed CPU organization for a computer system capable of executing arithmetic, logic, and data transfer instructions. (7)

b) With the help of a block diagram and function table, illustrate the functioning of (7)

a microprogram sequencer in a control unit designed for a processor that supports both arithmetic and logical operations.

Module -5

19	a)	Explain the mechanisms involved in accessing I/O devices. Discuss the role of I/O organization and the steps taken by a processor to interact with different types of I/O devices.	(10)
	b)	Explain how DMA is employed in I/O organization to enhance data transfer between peripheral devices and memory.	(4)
20	a)	Discuss the role of mapping functions in cache memory and their impact on cache performance. Compare direct mapping, associative mapping, and set-associative mapping, providing examples for each.	(10)
	b)	Differentiate between cycle stealing DMA and burst mode DMA, highlighting the scenarios where each is most effective.	(4)

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