Module 2

Processor organisation

Processor unit :- part of digital computer that implements different operations in the system

Operations :- Arithmetic, logic, shift, transfer

CPU

Combination of processor unit and control unit

All operations are considered as micro operations

Data path :- set of functional units that carry out data processing operation. Data path with a control unit make up the CPU of the computer system

processor unit (data path) + CU → CPU

Data paths are controlled using gates.

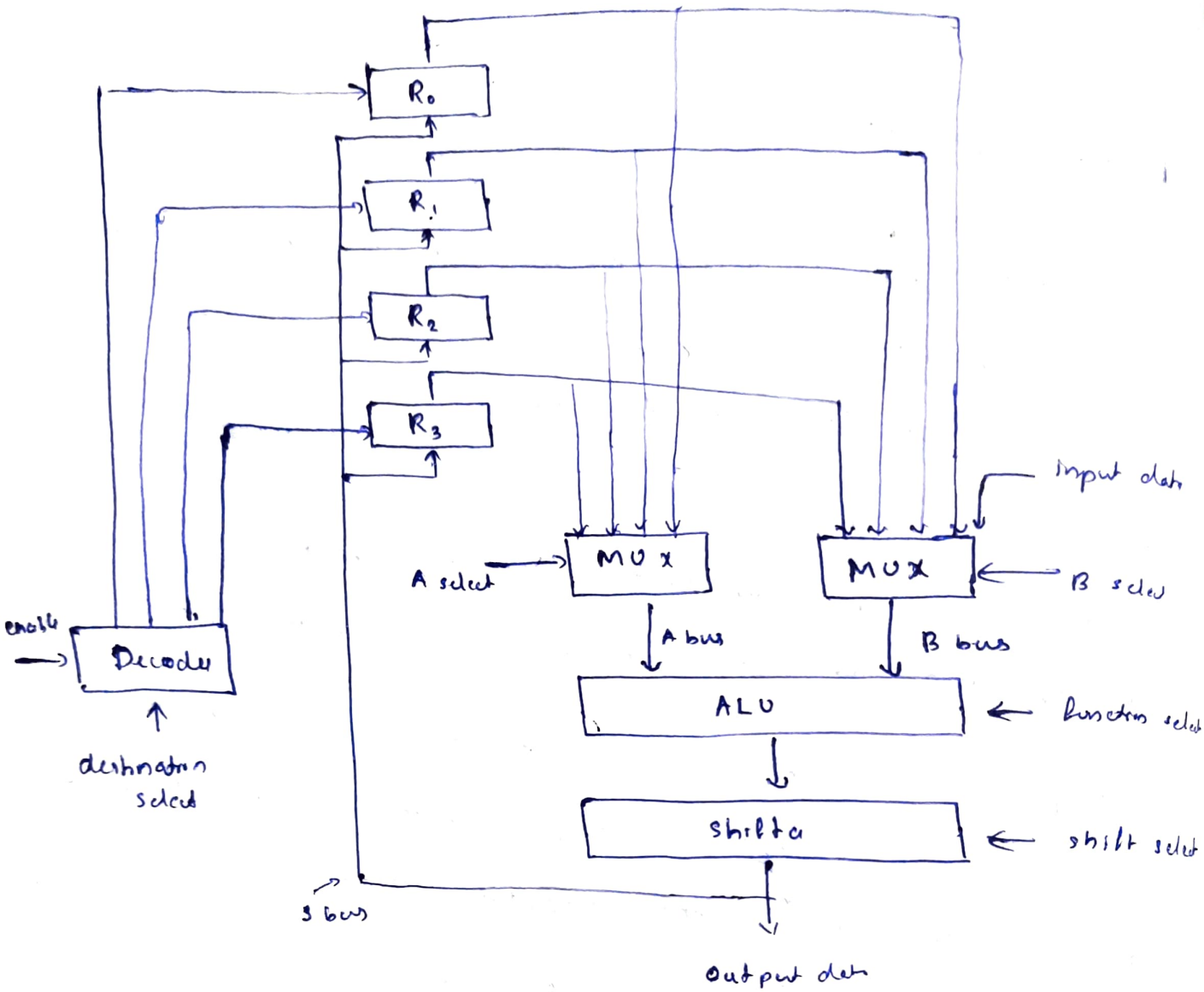
Methods of organizing processor

i) bus organization

ii) scratch pad memory

iii) Accumulators

i) Bus organisation



eg. $R_1 \leftarrow R_2 + R_3$

MUX A → place the contents of R_2 on BUS A

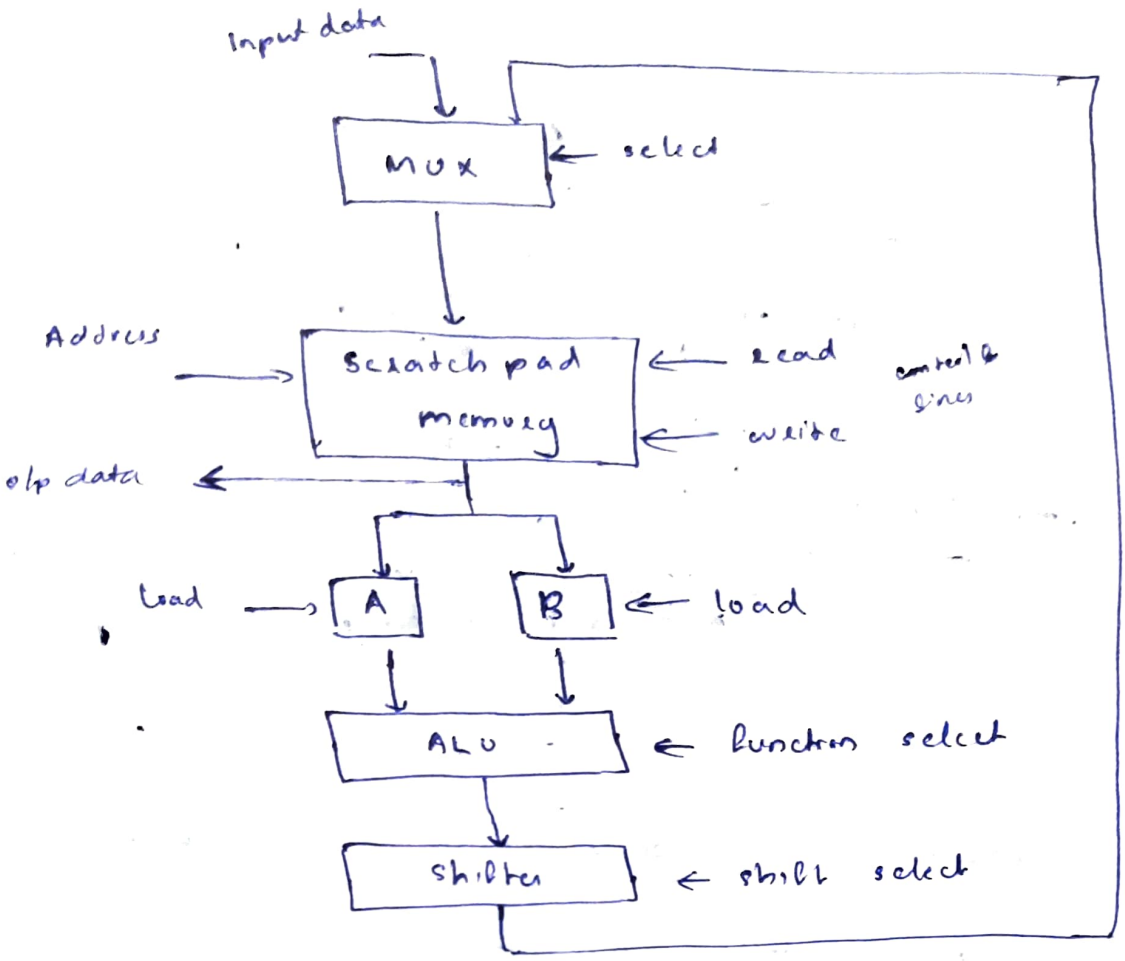
MUX B → R_3 on Bus B

ALU → based on the selection line, it perform $R_2 + R_3$ (A+B)

Shifter → transfer ALU content to S bus (O/P bus)

decoder → selection R_1 and transfer contents of S register to R_1

ii) scratchpad memory



Registers in processor unit can be enclosed within a small memory location unit called scratchpad memory.

A and B are temp registers

- In this memory access operation are more, so it reduces efficiency

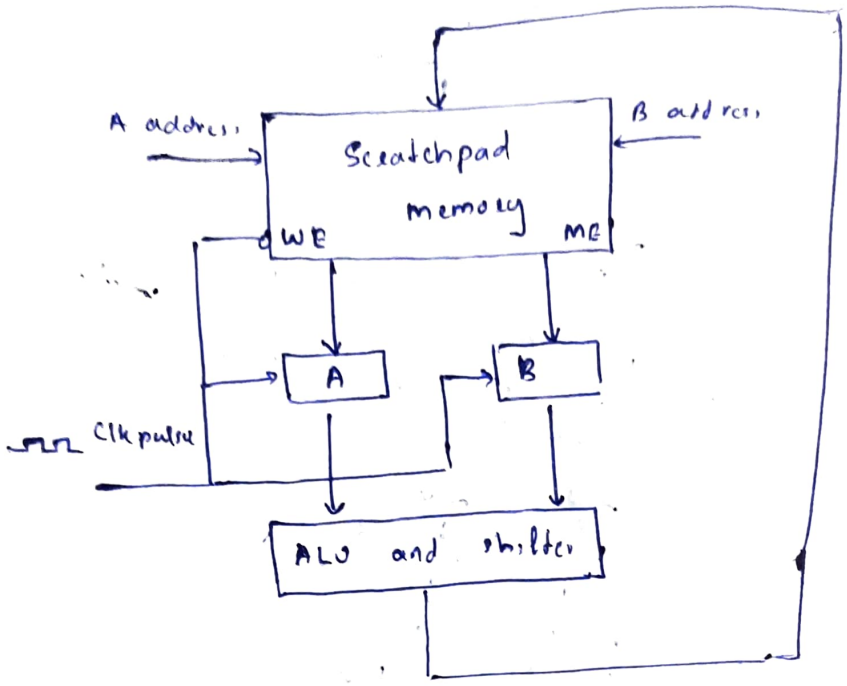
$R_1 \leftarrow R_2 + R_3$

$T_1 \rightarrow$ $A \leftarrow M[010]$ Read R_2 to bus A

$T_2 \rightarrow$ $B \leftarrow M[011]$ Read R_3 to Bus B

$T_3 \rightarrow$ $M(001)$ store result after performing A+B
(assuming it is destination)

Solution of this is two port memory (modification of scratch pad)



Here 2 operand address can be read in 1 clk cycle

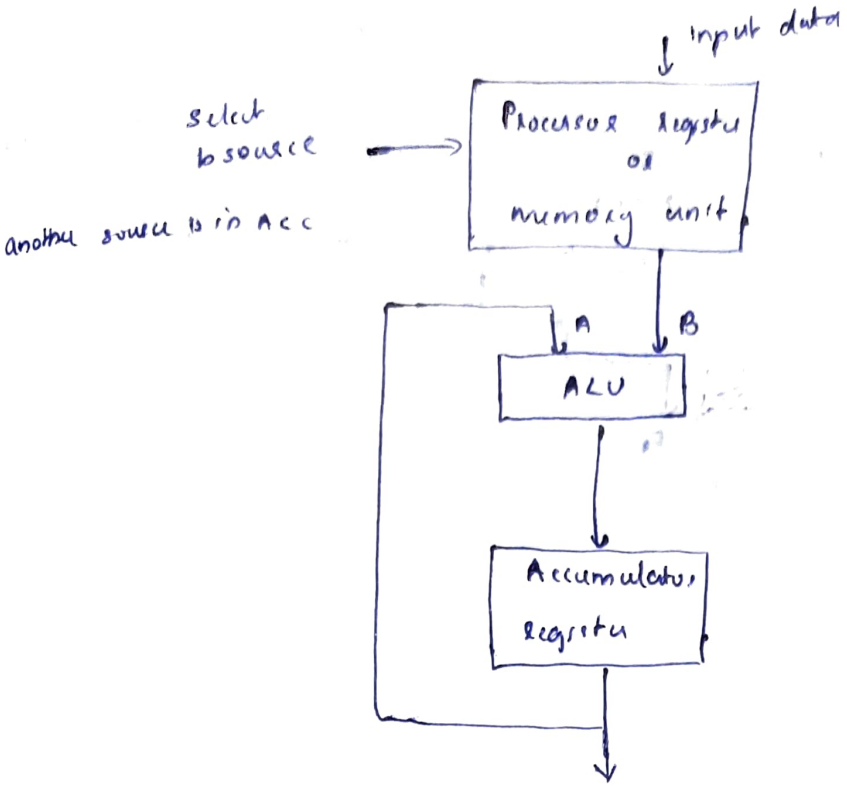
Using ME (Memory enable) we can choose B as destination register

based on value of clk we can choose Read / Write.

The clock pulse control the memory read and write operation through

the write enable input (WE)

iii) Accumulator



$R_3 \leftarrow R_1 + R_2$

T_1 $Acc \leftarrow 0$ clear accumulator

T_2 $Acc \leftarrow Acc + R_1$ transfer contents of R_1 to Acc

T_3 $Acc \leftarrow Acc + R_2$

ALU

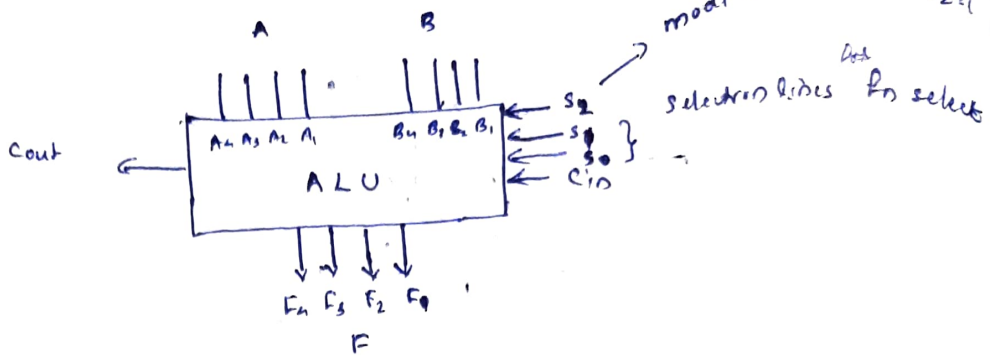
It is a digital circuit for performing arithmetic and logic operations

ALU has a no of selection lines to select a particular operation

selection lines are decoded within ALU so that k selection variable can specify upto 2^k operation

Block diagram of ALU

we need 2 operand, A and B which are of 4 bit



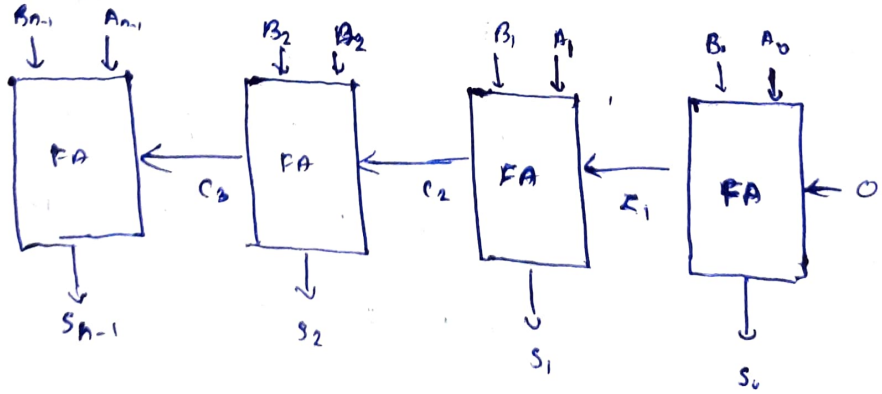
Design of arithmetic unit

Arithmetic operations

Addition, subtraction, increment, decrement, arithmetic shift

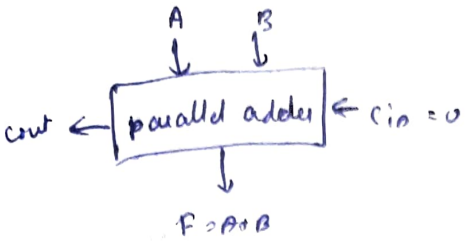
Parallel adder is used to perform these operations.

To perform n bit addition we require n full adder or n-1 full adder and 1 half adder (because initially there is no carry so we can perform addition using half adder)

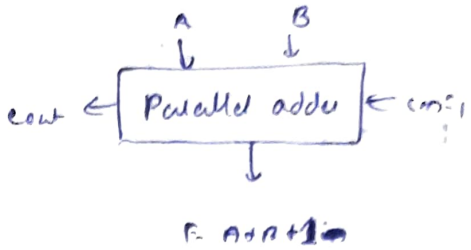


Using 4 parallel adder we can perform 8 operation (000 - 111)

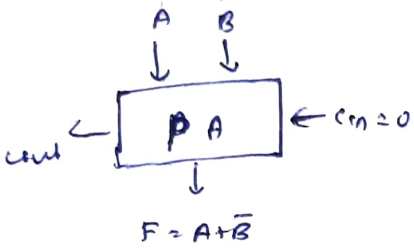
1) Addition



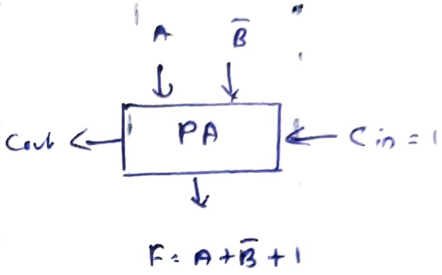
2) Addition with carry



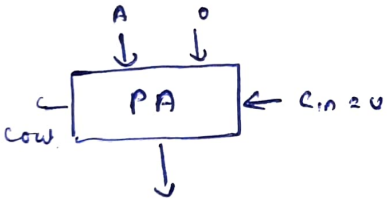
3) A plus 1's complement of B



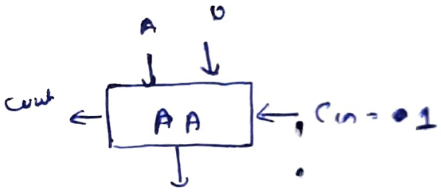
4. subtraction



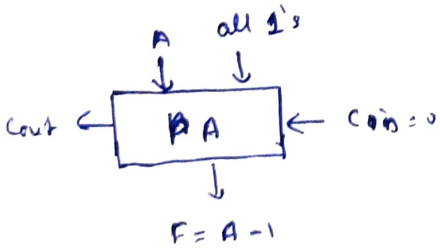
5. Transfer A



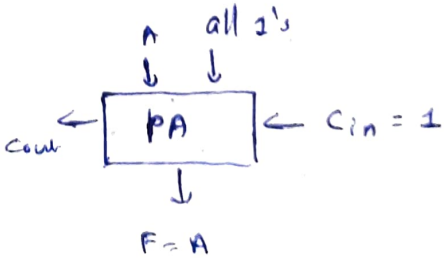
6. Increment A



7. Decrement A



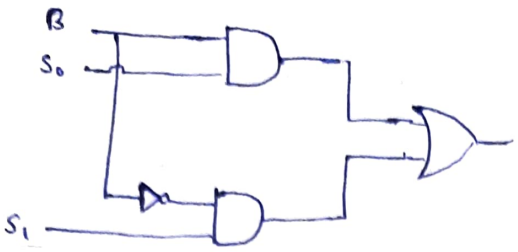
8. Transfer A



6 → 0110 +
1111
10101 ← 5

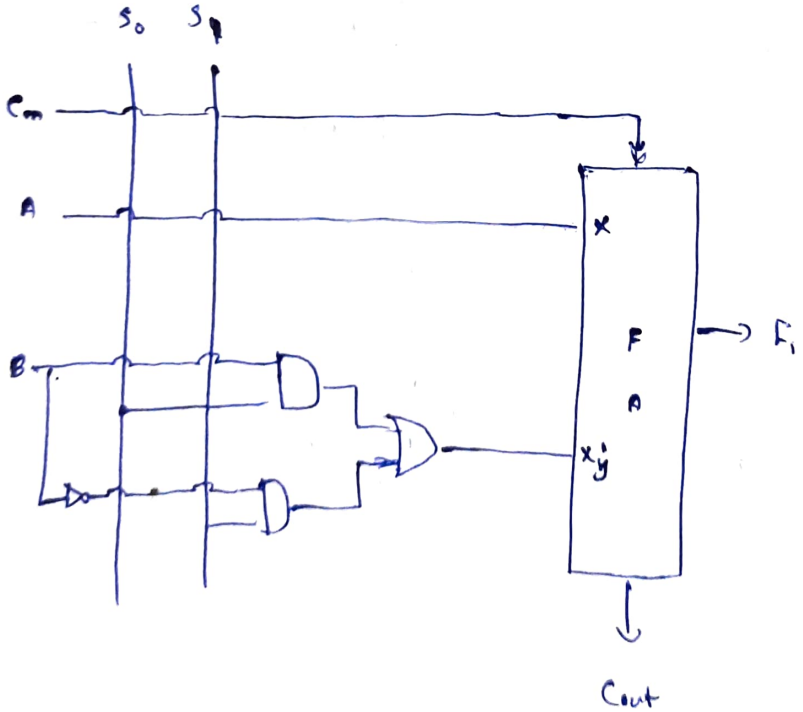
1'st operand is always A, 2nd operand values, 0, 1, B, B̄, so we have to create a circuit which produces these 4 to fed as I/p to FA

Circuit contains 2 AND, 1 OR and 1 NOT

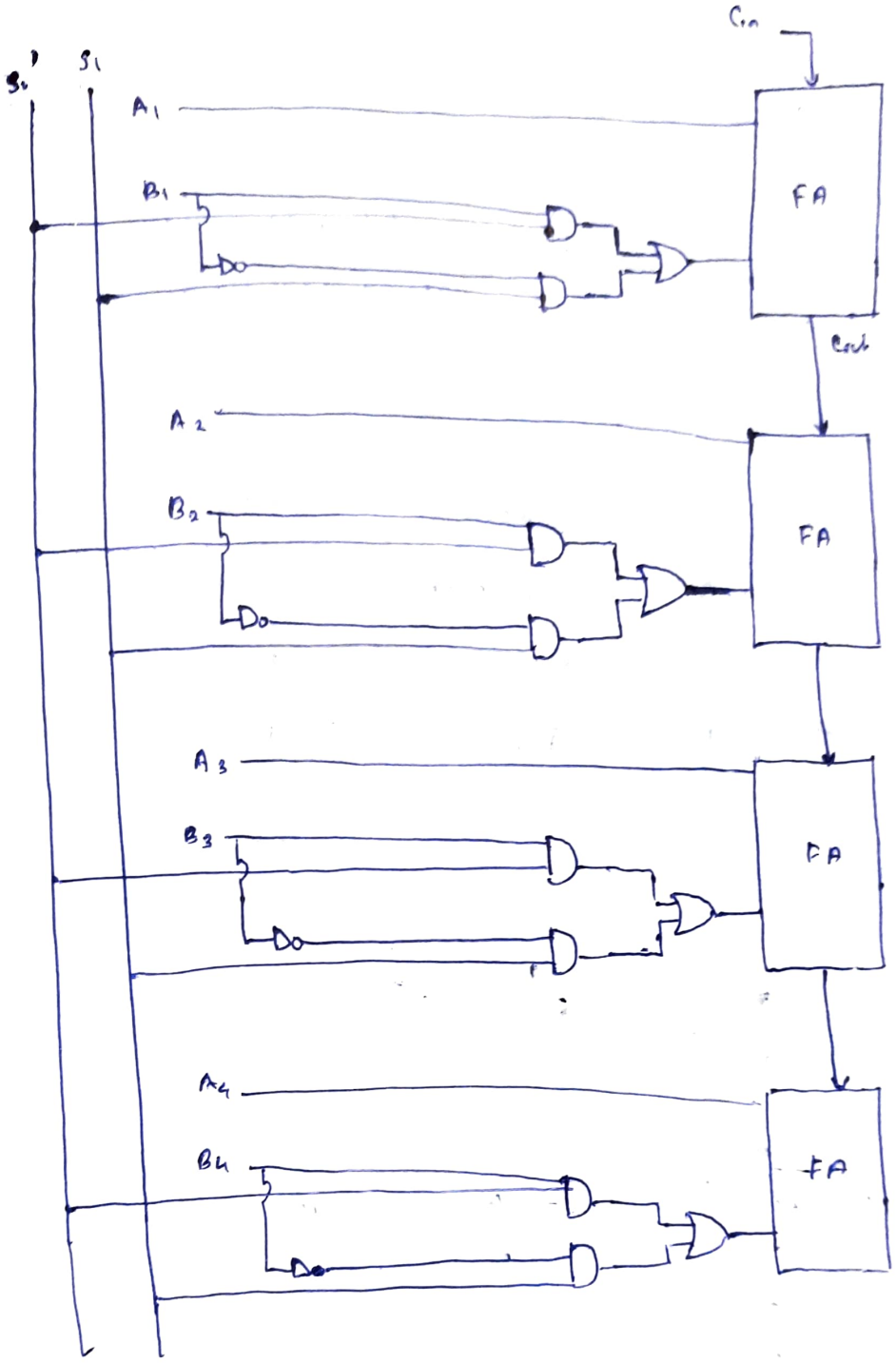


input						output
B	S_0	S_1	$\bar{B}$	BS_0	$\bar{B}S_1$	$BS_0 + \bar{B}S_1$
0	0	0	1	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	0	1	0	1

S_0	S_1	Y
0	0	0
0	1	$\bar{B}$
1	0	B
1	1	1



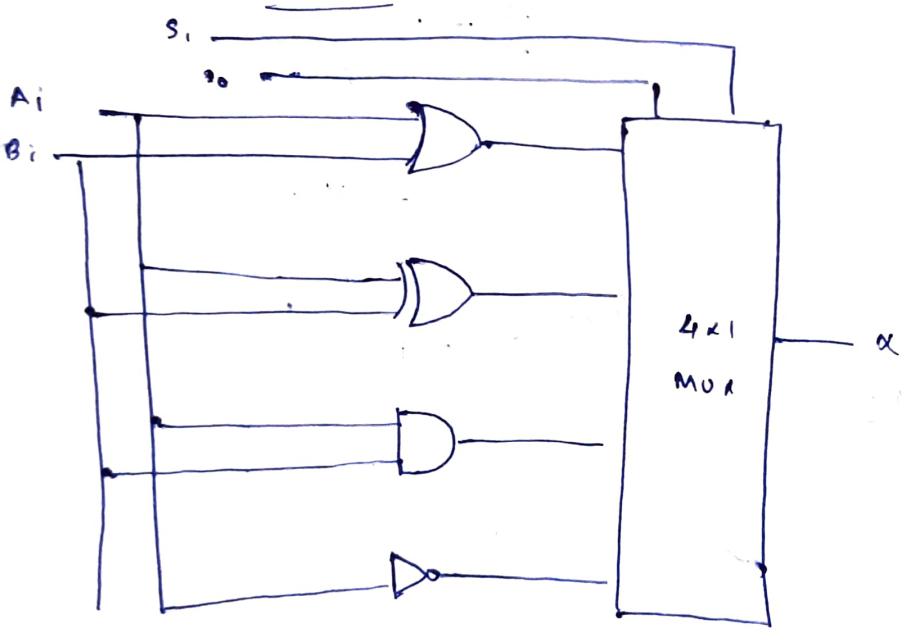
4 bit arithmetic circuit



Function table for arithmetic circuit

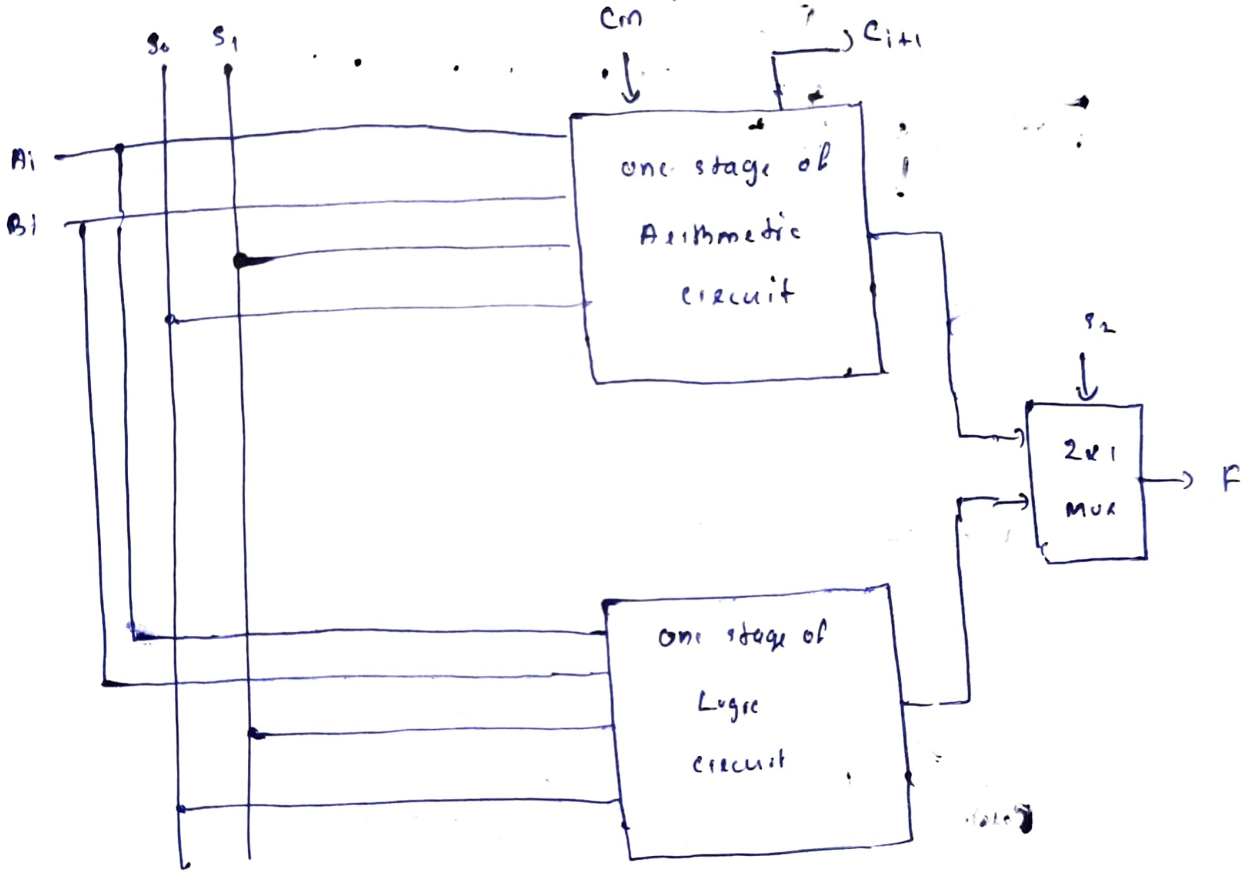
Selection			Input		operation	Function
S_1	S_0	C_{in}	A	B		
0	0	0	A	0	transfer	F = A
0	0	1	A	0	increment	F = A + 1
0	1	0	A	B	add	F = A + B
0	1	1	A	B	add with carry	F = A + B + 1
1	0	0	A	$\bar{B}$	1's subtraction	F = A + $\bar{B}$
1	0	1	A	$\bar{B}$	2's subtraction	F = A + $\bar{B}$ + 1
1	1	0	A	1	decrement	F = A - 1
1	1	1	A	1	Transfer	F = A

Design of logic circuit



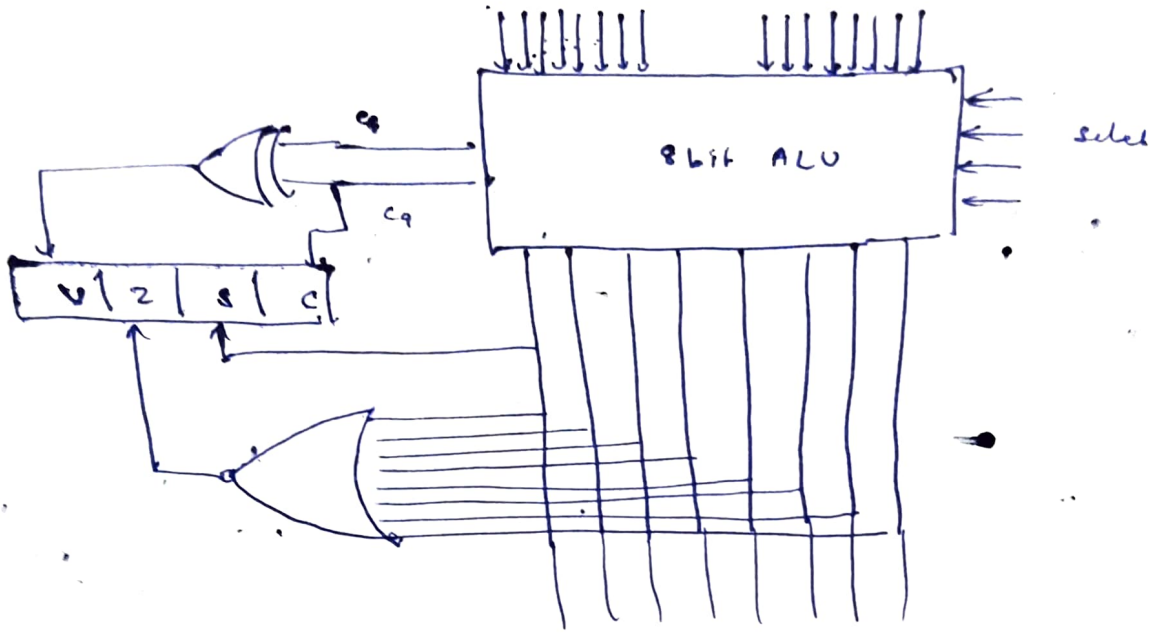
S_1	S_0	Input	Function
0	0	$A_i + B_i$	OR
0	1	$A_i \oplus B_i$	XOR
1	0	$A_i \cdot B_i$	AND
1	1	$(A_i)'$	NOT

Complete design of ALU



Status register

Status register is a 4 bit register. Four bits are C, Z, S and V. These bits are set or cleared as a result of an operation performed in the ALU.



For 8 bit
V is set if no of result > 127

Relation	Condition of status bit	Boolean function
A ≥ B	C = 1 and Z = 0	C Z'
A > B	C = 1	C
A < B	C = 0	C'
A ≤ B	C = 0 or Z = 1	C' + Z
A = B	Z = 1	Z
A ≠ B	Z = 0	Z'

Design of shifter

Shifter :

It transfer the output of ALU to the output bus, without a shift with right or left shift.

shifter can be implemented with bi-directional shift register

Difficulties in implementation of shifter using bidirectional

- clk pulse is needed for the transfer of information to the shifter
- another clk pulse is needed for shift operation
- another clk pulse is needed for moving information from the shift register to destination register

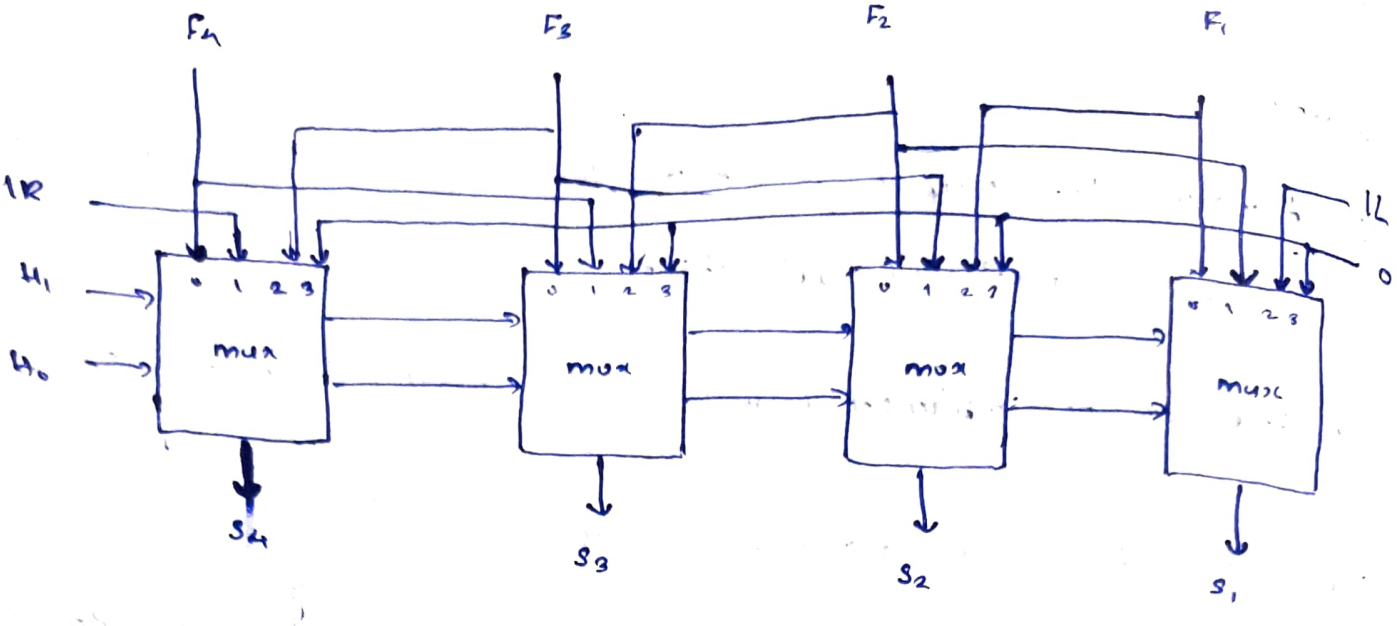
For a single shift operation 3 cycles are required

5

Implementation of shifter using combinational circuit

the signal from ALU to the output bus propagate through gates without need for a clk pulse. Only one clk pulse needed in the processor system for loading data from o/p bus to destination register

4 bit combinational logic shifter



Function table

H_1	H_0	Operation	Function
0	0	$S \leftarrow F$	Transfer F to S
0	1	$S \leftarrow shr\ F$	shift right F into S
1	0	$S \leftarrow shl\ F$	shift left F into S
1	1	$S \leftarrow 0$	Transfer 0's into S clear S

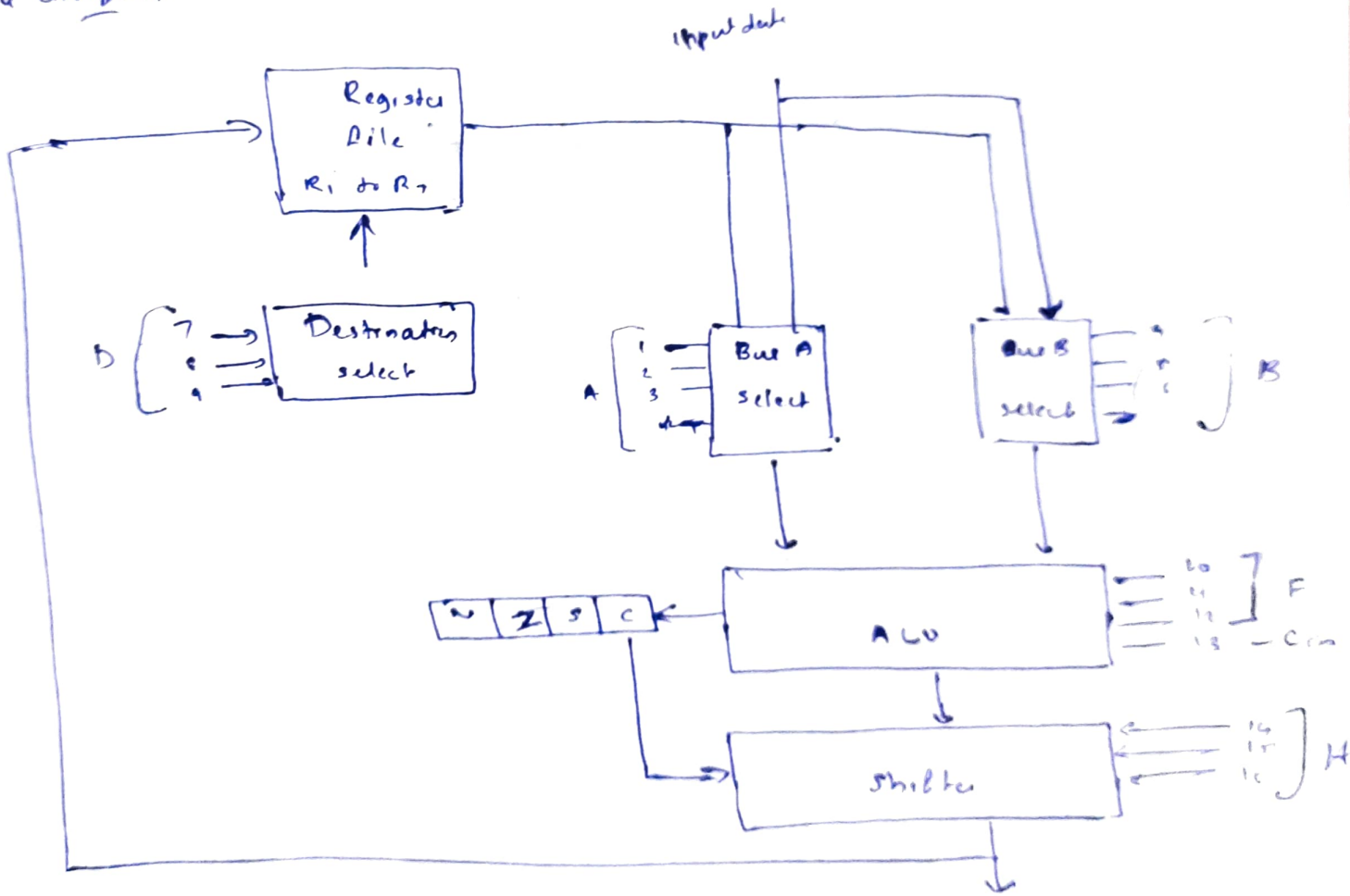
right shift

1001 → 0100

Processor unit

- selection variables in a processor unit control the micro-operation executed within processor during any clk pulse
- selection variable controls
  - bus
  - ALU
  - shifter
  - destination register

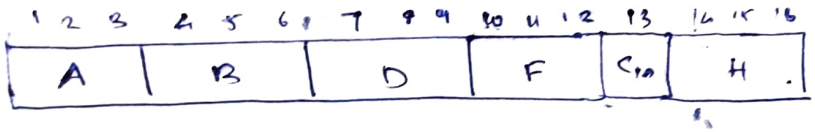
Block diagram



arithm selection dec Box circular shift

- It consists of 7 registers R1 to R7 and a status register
- The o/p go through 2 multiplexers to select the i/p to ALU
- I/p data from an external source are also selected by the same multiplexers. The output of ALU goes through a shifter and transferred to any one of the registers

- In this there are 16 selection variables in the unit and Fn is specified in control word



3 bits A → select a source register for the input to the left side of ALU

3 bits of B → selects a source register for the input to the right side of ALU

3 bits of D → select destination register

3 bits of F + 1 bit in Cin → select function for ALU

3 bits of H → select the type of shift in the shifter unit

Function of selection variables

Binary code	A	B	D	F with $C_{in}=0$	F with $C_{in}=1$	H
0 0 0	Input data	I/p data	None	A, C ← 0	A+1	No shift
0 0 1	R_1	R_1	R_1	A+B	A+B+1	shift right, $I_R=0$
0 1 0	R_2	R_2	R_2	A−B−1	A−B	shift left, $I_L=0$
0 1 1	R_3	R_3	R_3	A+1	A, C ← 1	0's in o/p bus
1 0 0	R_4	R_4	R_4	A∨B	–	—
1 0 1	R_5	R_5	R_5	A⊕B	–	Circulate right with C
1 1 0	R_6	R_6	R_6	A∧B	–	Circulate left with C
1 1 1	R_7	R_7	R_7	$\bar{A}$	–	—

1) A = B = 000 then mux selects input data (not value from register) and no destination is selected, D = 000

2) 2 bits in F field together with I/p carry Cin provide 12 micro operation of ALU

3) 3 bit 4 entries of one code in H field specify the shift operation of logic shifter.

$R_1 \leftarrow R_1 - R_2$

Find the control word

an

001	010	001	010	1	000
A	B	D	F	C_{in}	H

R_1 - left i/p of ALU

R_2 - right i/p of ALU

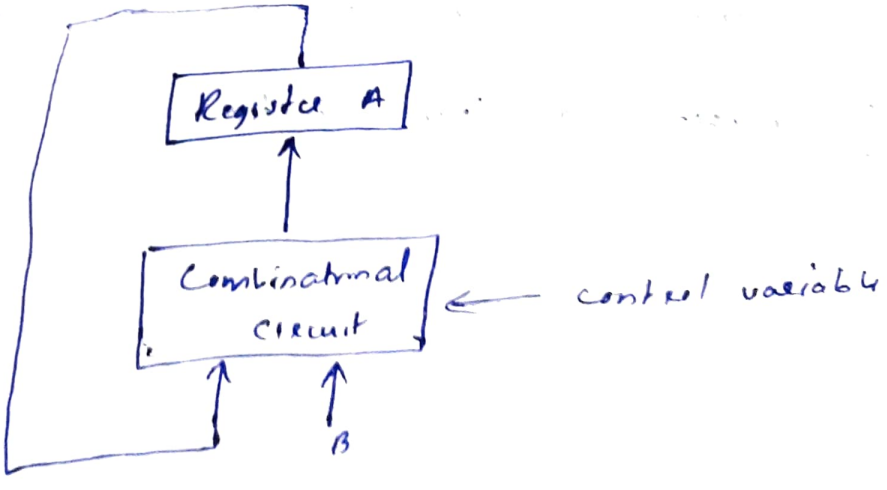
A-B is ALU operation

no shift required

R_1 destination register

Design of accumulator

Block diagram



The external inputs to accumulator are the data inputs from B and the control variables that determine the micro operations for the register. The next state of register A is a function of the present state of and the external inputs.

Accumulator can also perform data processing operations. Total of nine operations is considered here for the design of accumulator circuit.

Control variable	Microoperation	Name
P_1	$A \leftarrow A + B$	Add
P_2	$A \leftarrow 0$	clear
P_3	$A \leftarrow \bar{A}$	complement
P_4	$A \leftarrow A \wedge B$	AND
P_5	$A \leftarrow A \vee B$	OR
P_6	$A \leftarrow A \oplus B$	Ex-OR
P_7	$A \leftarrow shr\ A$	shift right
P_8	$A \leftarrow shl\ A$	left shift
P_9	$A \leftarrow A + 1$	increment
	If $(A = 0)$, then $(Z = 1)$	check for zero

4 bit accumulator