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Dept. of Computer Science & Engineering
IV Semester B.Tech Degree examination
I Series Test (MARCH 2024)

22CST402: Computer Organization and Architecture

Max. Marks: 50 **Time: 2 Hrs**

Qn No:	Part A Answer All Questions	Marks	BL	CO
1.	With a neat sketch, explain the connection between processor and main memory.	3	L1	CO1
2.	Distinguish big-endian and little-endian methods of memory representation with the help of suitable examples.	3	L2	CO1
3.	Write two address and zero address instruction for evaluating X = (A + B) * (C + D).	3	L2	CO2
4.	What are the performance benefits of employing a 2-port memory configuration in the scratchpad processor organization? Explain how this design choice enhances system efficiency.	3	L1	CO2
5.	Find the status of each flag register while performing the following operation. $65_{16} + DF_{16}$	3	L2	CO2
	Part B **Answer any Five questions.**			
6.	*Explain the following* *(i) Classification of computers based on computational ability.* *(ii) Memory hierarchy in computer system.*	7	L1	CO1
7.	*Illustrate the steps involved in execution of an instruction Z = X + Y written in high level language.*	7	L2	CO1
8.	Describe the process of fetching and executing an instruction within a computer system utilizing a single-bus organization. Explain with suitable figure.	7	L2	CO2
9.	Design an Arithmetic Unit to perform 4-bit arithmetic operations and logic functions with a given binary adder.	7	L2	CO2
10.	a) What are addressing modes in computer architecture, and how do they influence the execution of instructions?	3	L1	CO2
	b) The registers R1 and R2 of a computer contain decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instruction (i) Load 20(R1),R5 (ii) Move #3000,R5 (iii) Store R5, 30(R1,R2) (iv) Add –(R2),R5 (v) Subtract (R1)+,R5	4	L2	CO2

ax. Marks: 100

PART A

(Answer all questions; each question carries 3 marks)

Explain how the PC, IR, MAR and MDR registers are used during the instruction execution cycle.

What information is conveyed by the addressing mode used in an instruction? List any four addressing modes.

Explain shift microoperation with help of examples.

Illustrate the processor organisation using scratchpad memory with help of a diagram.

Illustrate divide overflow condition in restoring division with help of an example.

Differentiate between unifunction and multifunction pipelines.

Draw the block diagram for a control unit using PLA based organization.

What is the role of next address generator in microprogrammed control organization?

Does Direct Memory Access increase the efficiency of processor? Justify your answer.

Explain the need for using cache memory within the computer system.

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

a) What do you mean by byte addressable memory? Explain the two different types of byte assignment using diagrams.

b) Illustrate processor organisation using a single bus with help of a diagram. Explain how register transfers and ALU operations are carried out in the single bus organisation.

12 a) Describe the following addressing modes, giving an example for each: 7

i) Indirect Addressing mode

ii) Immediate Addressing mode

iii) Indexed Addressing mode

b) Discuss how instructions are classified based on number of operands or addresses they use. 7

Module -2

13 a) What is the role of status register within the processor? Draw the circuit diagram for a basic status register for an 8-bit ALU and explain how the carry and overflow status bits are set. 7

b) What is a control word? Explain, using an example, how a control word can be used to specify a complete instruction. 7

14 a) Draw the circuit diagram and function table for one stage of the logic unit for a 4-bit ALU with following logic operations – AND, OR, XOR and NOT. Explain the working. 7

b) Illustrate the use of accumulator register. Explain processor organization using accumulator register with help of a diagram. 7

Module -3

15 a) Explain the advantage of using an array multiplier. Design a 3x2 array multiplier. 7

b) Briefly describe the following with reference to pipelining: 7

i) Clock period

ii) Speedup

iii) Efficiency

iv) Throughput

16 a) Illustrate Booth's Multiplication algorithm with help of a flowchart and an example. 7

b) Summarize the different techniques used for pipeline hazard resolution. 7

Module -4

17 a) Are there any advantages in using PLA based or microprogrammed control organizations when compared to the hardwired organizations? Explain your answer. 7

b) Illustrate, with a diagram, how a microprogram sequencer helps to generate next address in a microprogrammed control organization. 7

Summarize, with help of an example, the steps involved in designing a hardwired control organization using one flip flop per state method. 14

Module -5

a) Explain the basic structure of a DRAM cell. Why does DRAMs need constant refreshing? 7

b) How does the processor react when an interrupt is raised by an I/O device? 7

a) What is a ROM? List and explain the different types of ROMs. 7

b) What are two modes in which Direct Memory Transfer can operate? Explain their differences. 7

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11.	Outline the differences in instruction execution during straight line sequencing and branching using suitable example.	7	L1	CO2
13.	Explain the following methods of organizing processor units (a) Bus Organization (b) Scratchpad Memory	7	L2	CO2