# UNIVERSITY OF ALBERTA

# DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

## CMPE 401 – Computer Interfacing

## Final Examination

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| Instructor: | B. F. Cockburn |
| Exam date: | December 17, 2010 |
| Exam duration: | 120 minutes |
| Aids permitted: | A hardcopy of the course lecture slides can be freely consulted.<br>Model solutions for the Fall 2010 assignments and midterm can be consulted.<br>No other model solutions are to be consulted.<br>One two-sided 8.5" x 11" formula sheet can be consulted.<br>Electronic calculators (all kinds) are permitted. |

Instructions:

1. Enter your printed name, signature and I.D. number on this cover page.
2. Verify that this booklet contains 10 pages (including this cover page).
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for extra space or rough work.

**Student name:** ____________________,________________
**Last name** **First name**

**Signature:** ______________________________________

**Student I.D.:** ______________________________________

| Question | Time | Worth | Mark | Subject |
|---|---|---|---|---|
| 1. | 15 | 12 |  | Fundamental Concepts |
| 2. | 20 | 17 |  | Multitasking Systems |
| 3. | 20 | 17 |  | The Fast Ethernet Controller |
| 4. | 15 | 12 |  | Message Queues in MicroC/OS |
| 5. | 20 | 17 |  | Flow Control in TCP/IP |
| 6. | 30 | 25 |  | Interfacing the MCF5234 bus to PCI |
| **Total** | **120 mins** | **100** |  | --- |

**Question #1 (Fundamental Concepts)**

In your own words briefly define each of the following concepts. Be sure to explain why each concept is important in Computer Interfacing.

(a) Instruction Operation Code

(b) Nonmaskable Interrupt

(c) Critical Section

**Question #2 (Multitasking Systems)**

(a) Partitioning a software system into interacting tasks has both possible advantages and disadvantages. Briefly comment on the suitability of a multitasking software architecture for each of the following: (i) the ability to enhance an existing system design with new external interfaces; (ii) the ability to protect critical system data stored in memory; (iii) the ability to ensure that the system responds in a timely and predictable way to externally-generated signals; (iv) the ability to debug and then correct problems.

**Question #2 (Multitasking Systems, cont'd)**

(b) In many process monitoring and control applications, it is convenient to adopt a multitasking architecture in which the tasks are expressed using a collection of interconnected states. Each task state is implemented as a (usually short and simple) segment of software. Once the present state of a task is executed, the task gives up the CPU. The next state of a task may be fixed for each possible current state, or may depend on the values of one or more status conditions. Discuss the likely advantages and disadvantages of such an architecture in the following two applications: (i) a controller must take measurements of many different process parameters, and the measurements might need to be performed at different frequencies for different parameters; (ii) a controller operates an Internet router, responding to the arrival of data packets, while also operating a user interface.

**Question #3 (The Fast Ethernet Controller)**

(a) The Fast Ethernet Controller (FEC) in the MCF5234 microcontroller is a subsystem that simplifies interfacing to 10-Mbps and 100-Mbps Ethernet LANs. The FEC includes shares a FIFO and a DMA controller for the receive and transmit directions. Briefly explain the reasons why both a FIFO and DMA controller are required in the FEC. What would happen if either the FIFO or the DMA controller were to be omitted?

**Question #3 (The Fast Ethernet Controller, cont'd)**

(b) There is a hard-coded controller inside the FEC that interprets the fields of the transmit and receiver buffer descriptors (BDs). The BDs are used to point to transmit (Tx) and receiver (Rx) buffers. The Tx buffers are variable in size, which the Rx buffers are all of the same size. What would be the main advantage(s) of expressing transmitted Ethernet frames as a series of variably-sized buffers? What would be the main advantage(s) of loading received Ethernet frames into a series of fixed-size buffers? Why should the Rx buffers be of some fixed size?

**Question #4 (Message Queues in MicroC/OS)**

The message queue in MicroC/OS is a flexible feature that allows messages to be passed in a controlled way between user tasks. Consider the following three code fragments, which appear in UserMain task, a first user task A, and a second user task B:

```
// Fragment in UserMain
OS_Q MyQueue;
void * MyQueueArray[ QSIZE ];
OSQInit( &MyQueue, MyQueueArray, QSIZE );

// Fragment in Task A
char * Pmsg;
Pmsg = "Hello World!";
OSQPost( &MyQueue, (void *) Pmsg );

// Fragment in Task B
char * Pmsg;
BYTE Err;
Pmsg = (char *) OSQPend( &MyQueue, 0, &Err );
```

(a) Briefly describe the difference between data structures MyQueue and MyQueueArray. Why are both data structures required? Why are the details of the OS_Q type kept private hidden inside MicroC/OS? What information must be maintained inside MyQueue?

(b) In the code fragment from Task B, briefly describe what happens when the third line of code (the call to OSQPend) is executed. Be sure to justify all parts of this particular line of code.

**Question #5 (Flow Control in TCP/IP)**

(a) The Transmission Control Protocol (TCP) uses a window-based flow control method, which simultaneously solves several challenges of operating a data connection over a potentially unreliable network. TCP provides a reliable bidirectional byte transportation service between a transmitting node and a receiving node. Briefly explain how TCP would handle the situation where the arrival order of two IP datagrams is reversed in the receiving node compared to the order in which the two datagrams were transmitted.

**Question #5 (Flow Control in TCP, cont'd)**

(b) Now explain how TCP would recover from the situation where exactly one byte is repeated twice (by mistake) in the payload of an IP datagram while it is passing through a network node somewhere along the route from a transmitting node to a receiving node.

### Question #6 (Interfacing the MCF5234 bus to PCI)

There are many similarities between the external MCF5234 system bus and the PCI bus. For example, both busses use active low byte enable signals. However, the two busses have many differences that would need to be overcome if they were to be interfaced together. Consider the problem of designing an interface circuit that would allow an MCF5234-based bus to operate in a PCI-based system. In particular, briefly describe in words how the PCI signals "IRDY", "TRDY", "FRAME", "DEVSEL" and "AD31-0" could be interfaced with the available MCF5234 bus signals (CS, R/W, TS, TIP, TA, TSIZ, etc.) Consider only the case where the ColdFire CPU in the MCF5234 on one PCI board needs to read a memory location (byte, word or long word) that is located in a second PCI board.