UNIVERSITY OF ALBERTA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CMPE 401 – Computer Interfacing

Final Examination

Instructor: B. F. Cockburn
Exam date: December 10, 2008
Exam duration: 120 minutes
Aids permitted: A hardcopy of the course overheads can be freely consulted.
Electronic calculators (all kinds) are permitted.
Model solutions for past assignments and exams are **not** permitted.

Instructions:
1. Enter your printed name, signature and I.D. number on this cover page.
2. Verify that this booklet contains 10 pages (including this cover page).
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for extra space or rough work.

Student name: _____,_____
Last name **First name**

Signature: _____

Student I.D.: _____

Question	Time	Worth	Mark	Subject
1.	12	10		Fundamental Concepts
2.	22	18		Real-time Multitasking
3.	18	15		UART and FEC Interrupts
4.	14	12		TCP/IP Stacks
5.	22	18		Layered Communications Interfaces
6.	18	15		Stepper Motor Control
7.	14	12		Direct Memory Access
Total	**120 mins**	**100**		---

Question #1 (Fundamental Concepts)

In your own words briefly define each of the following concepts. Be sure to explain why each concept is important in Computer Interfacing.

(a) Context switch

(b) Single-address DMA

(c) Determinism

Question #2 (Real-time Multitasking)

(a) Briefly explain what the major advantages and disadvantages of cooperative multitasking would be compared to pre-emptive multitasking. What requirements in the overall real-time problem would need to be considered when choosing between these two forms of multitasking? Comment on which of these two forms of multitasking would be more appropriate for (i) ensuring deterministic behaviour and (ii) making most efficient use of the available CPU clock cycles.

Question #2 (Real-time Multitasking, cont'd)

(b) Briefly explain how each of the following MicroC function calls can cause a context switch: (i) OSChangePrio(), (ii) OSTimeDly(), (iii) OSSemPost(), and (iv) OSSemPend(). Clearly indicate the conditions under which a context switch will occur in each case.

Question #3 (UART and FEC Interrupts)

(a) Both the Universal Asynchronous Receiver Transmitter (UART) and the Fast Ethernet Controller (FEC) modules in the MCF5234 microcontroller contain interrupt status registers (UISRn and EIRn) and interrupt mask registers (UIMRn and EIMRn). Briefly describe how the status and mask registers are used together to determine when interrupt signals are sent back to the MCF5234 Interrupt Controller Modules (and hence back to the ColdFire CPU).

(b) In the EIRn there are separate bits, RXF and RXB, for two different receiver interrupt conditions. Briefly describe how these two conditions are different. Why do you suppose that these interrupts were provided separately instead of providing a single receive interrupt? Give a simple example to illustrate your answer.

Question #4 (TCP/IP Stacks)

In the lectures we considered two different implementations of a TCP/IP stack for the MicroC multitasking kernel environment: a recent implementation from NetBurner and an older freeware stack called the Lightweight IP (lwIP). NetBurner's stack uses four separate tasks for the network hardware driver, the IP layer, the TCP layer, and the network application layer; by contrast, lwIP combines all four layers into one task and it uses its own complex buffer management system. Given that more recent microcomputers have much more available memory and run faster, give a reasonable justification for the stack configuration that was chosen by NetBurner. What are the major advantages of the stack architecture chosen by NetBurner?

Question #5 (Layered Communications Interfaces)

(a) In the lectures we discussed the advantages and disadvantages of layering in a communications interface with respect to the stack implementation in the communicating computers. But there is also impact on the efficiency (that is, the faction of communicated bits that are actually useful application data bits) with which the communication medium is used. What do you suppose would be some of the main disadvantages of layering a communications interface with respect to this measure of efficiency? Consider the following two cases: (i) data is being produced in fixed size blocks, and (ii) data is being produced as a continuous stream of bytes.

Question #5 (Layered Communications Interfaces, cont'd)

(b) The Internetworking Protocol (IP) is allowed to split up a TCP segment into smaller segments before creating IP datagrams. This might be a useful thing to do in order to ensure that the IP datagrams are small enough to be handled by the physical layer protocol. Consider the problem of splitting up a given TCP segment into two equal-length shorter segments. How would the IP software determine the values to use in the following header fields: (i) the source port, (ii) the destination port, (iii) the sequence number, (iv) the acknowledgement number, (v) the segment checksum, and (vi) the data field for the two new segments?

Question #6 (Stepper Motor Control)

(a) A stepper motor is conveniently controlled by purely digital signals, where the stator windings are either electro-magnetized in one of two possible directions, or are not magnetized at all. Stepper motors are in fact a type of synchronous motor. The ideal current waveform in a stepper motor would have the shape of a sinusoid (e.g. sine or cosine) over time. Using sinusoidal-shaped current waveforms would avoid the strong vibration experienced by stepper motors when they are operating. In the space below, draw the full-step current waveforms (with current on the vertical axis and time increasing along the horizontal axis) for a two-phase stepper motor. Forward current is to be shown with positive values, and reverse current is to be shown with negative values. Show how these waveforms are actually rough approximations to two sinusoidal waveforms that are 90 degrees out of phase.

(b) Now show that the half-step control waveforms are also rough approximations to two sinusoids that are 90 degrees out of phase. Indicate on your waveforms the current configurations that correspond to the new half-stepped positions. With the aid of your diagram, explain why the total rotor current varies with the position of the stepper motor rotor.

Question #7 (Direct Memory Access)

Consider the scenario where CPU-requested dual-address DMA is going to be performed using one of the three DMA controllers in an MCF5234 microcontroller. The source and destination devices are external memories, connected to different chip selects, that happen to have different data port widths. Specifically, the source device is 16 bits wide (connected to bits #31-16) and the destination device is 32 bits wide. Briefly explain the origin, the connecting path, and the destination of each of the following signals: (i) the source address; (ii) the destination address; (iii) the read/write signal; (iv) the chip select signals; and (v) the data signals.