ECE 315 Assignment 1

Arun Woosaree
XXXXXXX

March 18, 2020

1

The system will enter any of the low power modes below when a `STOP` instruction is executed. Depending on the `WCR[LPMD]` bits, the MCU will enter either wait, doze, or stop mode. For each of these modes, power is saved by idling the CPU with no active cycles, powering down the system, and stopping all internal clocks. The coldfire core is also disabled in each of the low-power modes.

A wake-up event will cause the MCU to exit any of these low power modes, and return to run mode. A wake-up event can be any type or reset, or any valid, enabled interrupt request. To exit from these low power modes with an interrupt, the interrupt request's priority should be higher than the value programmed in `WCR[LPMD]`, and higher than the value programmed in the interrupt priority mask (I) field of the core's status register. Additionally, the interrupt request should be from a source that is not masked in the interrupt controller's interrupt mask register, and it should have been enabled at the module of the interrupt's origin.

wait

Wait mode saves power by stopping the CPU and memory clocks until a wake-up event is detected. Peripherals can be programmed to continue operating, and can also generate interrupts which will cause the CPU to exit from wait mode. The wait mode is entered when the `STOP` instruction is executed, with the `WCR[LPMD]` bits having a value of `10`.

doze

Doze mode is similar to wait mode, in that it affects the processor in the same way as in wait mode, however, some peripherals define individual operational characteristics in doze mode. Peripherals continuing to run and having the capability of producing interrupts may cause the CPU to exit the doze mode and return to run mode. Stopped peripherals restart operation on exit from

doze mode, as defined for each peripheral The doze mode is entered when the `STOP` instruction is executed with the `WCR[LPMD]` bits having a value of `01`.

stop

Stop mode is also similar to wait and doze mode, in that it affects the processor the same way. However, all system clocks are stopped, and peripherals cease operation. The stop mode is entered when the `STOP` instruction is executed with the `WCR[LPMD]` bits having a value of `11`.

2

Similarities

1. both use harmonic intervals to move between different sections of code
2. each polled input or device is assigned to one loop or state
3. loops/states not giving up CPU until the code is done processing

Differences

1. separate blocks of code represented as a different loop vs. a different states
2. interupts for responding to external events, (Multiple nonpreemptive loops) provide fast and deterministic response to external events vs. giving up CPU to the kernel when the task is complete, meaning external events are only processed when the state associated with that peripheral is run (periodically state-driven)
3. advancing from state to state happens at predictable intervals, but with multiple nonpreemptive loops with interrupts, an interrupt can vary the time it takes to switch between tasks

3

Advantages

- All ethernet frames will fit in the buffer

When would it be more appropriate to choose a single threaded bare-metal architecture

- THe FEC would accept frames that are larger than the ethernet standard and are potentially garbage

4

The number of teeth a gear has determines how many steps there are in a full rotation. For example, a gear with four teeth will have 4 steps in a 360°rotation. Therefore, the step angle for the one gear would be $360°/4 = 25°$. The formula is 360°divided by the number of teeth. Now, in the stepper motor, there is a rotor and stator, and the rotor has more teeth than the stator. Because the rotor has more teeth than the stator, we can see both visually and mathematically that the individual step angle for the gear would be smaller than the stator. Because these gears rotate in opposite directions, the overall rotation would be the larger step angle of the stator, subtracted by the smaller step angle of the rotor. We subtract the step angle of the rotor, because it goes in the opposite direction of the stator. So, overall, we get

$$\frac{360°}{n_s} - \frac{360°}{n_r}$$

where n_s is the number of teeth of the stator, and n_r is the number of teeth of the rotor. This matches with the formula described in slide 10-10.

5

There are two different systems of priorities because tasks and hardware interrupts are meant to behave very differently from each other. Hardware interrupts usually are meant to interrupt tasks that are currently running, so that the system can react in real-time to external events, while tasks generally have lower priority. For example, waking up the system from a low-power state happens with a hardware interrupt, and stops the idle task from running. This is an example of the two different systems interacting. These two systems can also interact with each other when a task requires a hardware interrupt to continue execution. For example, waiting on a hardware timer, or an I/O request.

6

Calculating the error budget,

$$75\% \div 2 = 37.5\%$$

$$35\% \times 32 = 12$$

So, ± 12 periods is the error budget, except for that the clock and the received data stream are asynchronous and the falling edge of the start bit could occur just after a 32x clock rising edge, or just before one but without enough setup time to use it. So, the error budget is actually ± 11 periods.

The optimum sampling point for the stop bit is its bit-centre, which is

$$32 \times (1\ \textit{start bit} + 8\ \textit{data bits} + 0.5\ \textit{stop bit}) = 304$$

receive clocks after the original falling edge of the start bit.

So, the allowable error is

$$\frac{11}{304} \times 1000000 = 36184.21053 \; ppm$$

Calculation is based off of this tutorial: `http://www.eecs.umich.edu/courses/eecs373.w05/lecture/AN2141.pdf`

7

Manchester codes were widely used for magnetic recording on 600 bpi computer tapes, and was used for the early physical layer ethernet standards. Today, they are used in consumer IR protocols, RFID, and NFC communication.

It is a method of transmitting bits which allows the receiver to synchronize with the sender.[1]

4b/5b Encoding used for fast ethernet (100Mbps), and USB power delivery. It also allows for synchronization between the receiver and the sender.[2]

In terms of advantages over Manchester encoding, 4B/5B more efficiently utilizes the link. With Manchester encoding, the data rate is cut in half relative to the bandwidth of the data signal. In comparison, for 4B/5B, the signalling rate is 1.25 times the data rate. Additionally, 4B/5B encoding allows for better error detection, if a code received is not in the table.

8

A **duplex point-to-point link** is a point-to-point link that allows for simultaneous communication in both directions. (A point-to-point link is a dedicated connection between two communicating nodes, with one node at each end of the link.)

A **fully connected topology** is a network topology where every node has a dedicated link to every other node in the network, such that the number of connections required is $\frac{n(n-1)}{2}$, where n is the number of nodes in the network.

A **collision** occurs when two devices on the same network attempt to transmit data at the exact same time. As a result, the transmitted bits usually end up being mangled, and have to be retransmitted.

A **crossover cable** is an ethernet cable used to connect two computing devices of the same type together. One end is wired T-568A, while the other is wired T-568B.

A **daisy-chain configuration** is a scheme where devices are connected together in series. They can also be in a ring topology. It can be compared to

[1] `https://www.allaboutcircuits.com/technical-articles/manchester-encoding-what-is-it-and-why-use-it/`

[2] `https://topic.alibabacloud.com/a/4b-5b-coding-principle_8_8_31582667.html`

a string threaded through daisy flowers, where the daisies are devices, and the string forms the connections between them. Similarly, a ring can also be formed in this configuration.