UNIVERSITY OF ALBERTA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CMPE 401 – Computer Interfacing

Final Examination

Instructor: B. F. Cockburn
Exam date: December 11, 2009
Exam duration: 120 minutes
Aids permitted: A hardcopy of the course overheads can be freely consulted.
Model solutions for the Fall 2009 assignments and midterm can be consulted.
No other model solutions are to be consulted.
Electronic calculators (all kinds) are permitted.

Instructions:
1. Enter your printed name, signature and I.D. number on this cover page.
2. Verify that this booklet contains 10 pages (including this cover page).
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for extra space or rough work.

Student name: _____,_____
Last name **First name**

Signature: _____

Student I.D.: _____

Question	Time	Worth	Mark	Subject
1.	15	12		Fundamental Concepts
2.	30	25		Task Priorities
3.	15	12		Interfacing to Ethernet
4.	10	9		Client-Server Communication
5.	20	18		Buffering and Flow Control
6.	15	12		Improved Half-Stepping Waveforms
7.	15	12		Semisynchronous PCI Bus
Total	**120 mins**	**100**		---

Question #1 (Fundamental Concepts)

In your own words briefly define each of the following concepts. Be sure to explain why each concept is important in Computer Interfacing.

(a) Big Endian byte order

(b) Counting semaphore

(c) Two-address DMA

Question #2 (Task Priorities)

(a) In pre-emptive multitasking kernels, each task is assigned a priority. The task priorities are used by the kernel to decide which task should be allowed to run on the CPU at any given time. What would be some important considerations when assigning priorities to tasks? Which tasks should be assigned the higher priorities, and which tasks should be assigned the lower priorities? Justify your recommendation.

(b) In some pre-emptive multitasking kernels, the priority that is assigned to each task when the task is created is fixed; in other kernels, task priorities can be changed. Give at least two good reasons for having the ability to change the priority of a task. What are at least two disadvantages to allowing task priorities to be changed?

Question #2 (Task Priorities, cont'd)

(c) One of the potential drawbacks of priorities is that the high priority tasks might prevent the low priority tasks from having enough execution time on the CPU. Assume that the tasks in a given system have been split into two groups: high-priority tasks with priorities that lie within one range of priority values, and low-priority tasks with priorities that lie within a second range of priority values. Briefly outline a way in which a strictly pre-emptive kernel (like MicroC/OS) could be modified to use timer interrupts to ensure that low-priority tasks always get some minimum fraction of the available execution time compared to the high-priority tasks.

Question #3 (Interfacing to Ethernet)

(a) In the context of an Ethernet interface on a microcomputer, what is the PHY and what is the MAC? Why are these two subsystems often implemented as separate devices?

(b) Ethernet local area networks (LANs) use a physical layer addressing scheme where each device on a LAN has a 6-byte (48-bit) address. However, when an Ethernet LAN is connected to the Internet, 4-byte (32-bit) IP addresses must be assigned to each node. Why do you suppose both of these addressing schemes are being used? Hint: What is the primary purpose of Ethernet physical addresses and Internet IP addresses?

Question #4 (Client-Server Communication)

(a) What is meant by "client-server" communication over the Internet?

(b) Briefly describe how could the client-server model together with HTTP be used for organizing a system that monitors the status and controls a distributed network of data loggers?

Question #5 (Buffering and Flow Control)

(a) The flow of data in a computer system is typically managed using both data buffering (for example, FIFO queues or circular buffers) and flow control. Briefly explain the major purposes of data buffering and flow control. Be sure to explain the differences between these two mechanisms. Why are both mechanisms often required to handle the flow of data from a data source/producer to a data sink/consumer?

Question #5 (Buffering and Flow Control, cont'd)

(b) What is the "window size" in window-based flow control? What would be some reasonable factors to consider when choosing the window size in a particular situation?

(c) One of the challenges of implementing the ENQ/ACK flow control method is to design a method of recovering from lost "enq" and "ack" characters. Propose a strategy that could be used to recover from this error situation.

Question #6 (Improved Half-Stepping Waveforms)

Assume that you are given a new kind of bridge circuit that receives three digital inputs (E, D & M) to control each of two stepper motor windings, identified as "a" and "b". Inputs "Ea" and "Eb" enable (for input 1) or disable (for input 0) the current flow in windings "a" and "b", respectively. Inputs "Da" and "Db" give the current direction, either forward (0) or reverse (1), for the two windings. Finally, inputs "Ma" and "Mb" give the magnitude, either 0.707 times full strength (0) or 1.0 times full strength (1), for the two windings. Construct a table that illustrates an "improved" half-step drive waveform sequence. Your table should have seven columns (labeled angle, Ea, Da, Ma, Eb, Db, Mb) and eight rows of data. In what ways would this new half-stepping drive waveform be improved over standard half-stepping?

Question #7 (Semisynchronous PCI Bus)

(a) The Peripheral Communications Interconnection (PCI) Bus uses a semisynchronous bus, which includes a clock signal, and two active-low handshake signals: IRDY and TRDY. Briefly explain how these IRDY and TRDY signal are used to accommodate different peripheral response times in a read operation to a memory-mapped peripheral register.

(b) The PCI Bus uses "Incident Wave Switching", where the bus drivers produce half-height signals, and reflections at the end of the bus are used to double up the amplitude of the signals. What would be some of the major advantages and disadvantages of using this kind of scheme on a microcomputer bus?