Arush Karingala

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Education

Degree	Institute	Branch / Department	CGPA/Percentage	Year
M.Tech	National Institute of Technology, Warangal	ECE, Advanced Communication Systems.	7.63	2024
B.Tech	GRIET, Hyderabad	Electronics and Communication Engg.	8.5	2022
XII	Sri Chaitanya Junior College, Hyderabad	Maths, Phy and Chem.	95.8%	2018
X	Kendriya Vidyalaya AFS Begumpet	-	9.2	2016

Work Experience

1. Intel Corporation Pvt Ltd, Bengaluru (May 2023 - May 2024)

Role: Graduate Technical Intern

Responsibilities: Modelling, simulation and testing of client and discrete platform.

As part of Simulation team, responsible for delivering behavioral and functional models for Intel's Graphics products.

- Leading Pre-Si effort to shift left Post-Si/Power-on verification tests.
- Delivering full platform simulation products for Intel's Client and Discrete products.

Projects

1. Analysis of CMOS Inverter Characteristics using SkyWater SKY130 PDK and Ngspice SPICE simulator.

Analysis of VTC, MOS characteristics, noise analysis, power simulation of CMOS inverter.

2. Vending machine in Verilog.

Implemented Vending machine using verilog HDL in Xilinx Vivado.

3. Fall detector using IoT.

Detect's a fall and report's it via Google Firebase to mobile app developed using Kodular rapid mobile app development utility.

4. Machine Learning Techniques to Predict the risk of Heart Attack.

Served as a team leader at Advanced Academic Centre (AAC) to build an ML model using logistic regression statistical model to predict the risk of a heart attack by taking various attributes like resting blood sugar, maximum heart rate and many more.

Publications

• IEEE publication: Segmentation Of Biological Cells In Microscopic Images | 2022 Third International Conference on Intelligent Computing Instrumentation and Control Technologies (ICICICT)

Relevant Courses and Certifications

- o NPTEL: Digital IC Design, IIT Madras , Introduction to Embedded System Design, IIT Madras.
- o OpenEDG Python Institute: Programming Essentials in Python.
- Coursera: Hardware Description Languages for FPGA Design(Verilog).
- o Bharat Acharya: Computer Organization and Architecture.
- Youtube: Static Timing Analysis.
- Maven Silicon: VLSI System On Chip Design(ASIC design flow RTL to GDS covering front end and back end).

Technical Skills

- o Tools: Xilinx Vivado, MATLAB, LabVIEW, LateX, Microsoft Office, word, Excel.
- o Operating System: Windows, Linux.
- o Programming and scripting Language: C, Python.
- o Hardware Description Language: Verilog.

Achievements/Awards and Hobbies

- o 2nd position in essay writing competition on the topic History behind the Indian constitution, conducted by NITW.
- Secured 1st position in Quiz Bee conducted by IEEE.
- o Achieved National Cadet Corps (NCC) A certificate.

o Hobbies: Playing Cricket and Badminton.

Soft Skills

o Excellent analytical and logical skills.

- o Ability to think innovative ideas and optimum solution.
- o Effective performer as an individual or in a team.