With developing technology, reducing power consumption is an important goal.If the power consumption is more , a certain amount of heat is generated by the device which may affect the product life.Circuits operating in subthreshold region of the transistors is the solution to the problem.Adder are important part of microprocessor and system on chip design.Thus, designing a adder with reduced consumption can help a lot of designs in the future.

The Carry look ahead adder is basically a fast ripple carry adder. It improves the speed of the system by efficiently determining the carry bits signal well in advance.Carry look ahead adder is a fast adder architecture and it is used to design arithmetic circuits.The carry look ahead adder should be able to perform unsigned addition of two 4-bit numbers in parallel.This approach reduces the power consumption.A bottom-up design approach is adopted. The key components are first designed and tested such as propagate-generate sum generator and carry generator.Secondly, all the components are put together. Finally, the design layout and simulations are created and checked. The propagation delay is calculated by predicting the carry signal well in advance. Carry look ahead adder usually predicts the carry signal within 4 clock cycle. Carry look ahead adder reduces the number of gates through which a carry signal must propagate.

The adder is generated in 3 stages - propagate-generate block, sum generator and carry generator.The logic used for propagate block

* Gi = Ai.Bi
* Pi = Ai ⊕ Bi

As both the signals depend on input bits; they will be valid for just one gate delay

* Si = Pi ⊕ Ci

The equation on which the 4- bit Carry look ahead is defined is

* C1 =G0 + P0C0
* C2 = G1+ P1C1

= G1 + P1 (G0+P0C0)

* C3 = G2 + P2C2

= G2 + P2G1 + P2P1G0 + P2P1P0C0

* C4 = G3 + P3C3

= G3+P3 G2 +P3 P2G1 + P3P2P1G0 +P3 P2P1P0C0

The Carry look ahead adder is made of XOR, AND and inverter logic gates. The carry look ahead adder consists of propagate generator block, carry generator block, sum block. The basic block of carry look ahead is given 5 inputs which goes to propagate- generator block and the output of this block goes to the input of the carry generator or look ahead block. The carry bits are given to XOR gate with respective propagation bits to give final sum of the carry look ahead adder. The final carry would be generated.

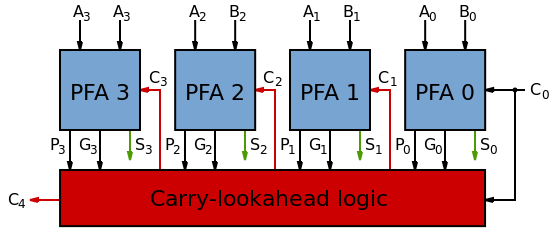


Fig 1. 4- bit Carry look ahead block diagram

Personal and Teammate's contribution to the project

I and my project partner worked on different modules on the project and finally merged respective work.

My team-mate Ankit Taskar worked on building the schematics and layouts for the XOR and Propagation and Generate Block, while I worked on the schematic and layout of the Carry look ahead adder.

CMOS Design

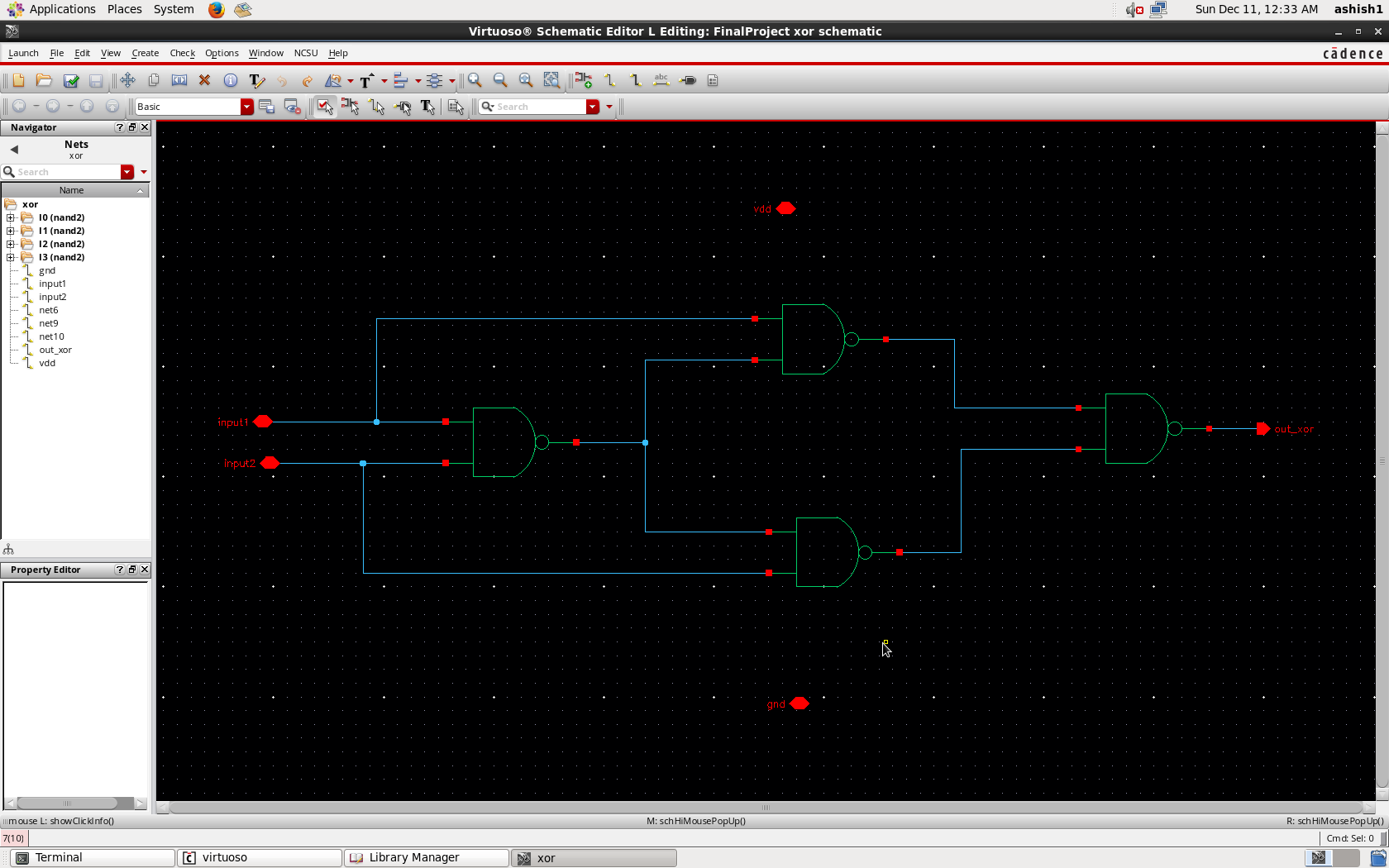


Fig 2. XOR SCHEMATIC



Fig 3. XOR Analysis

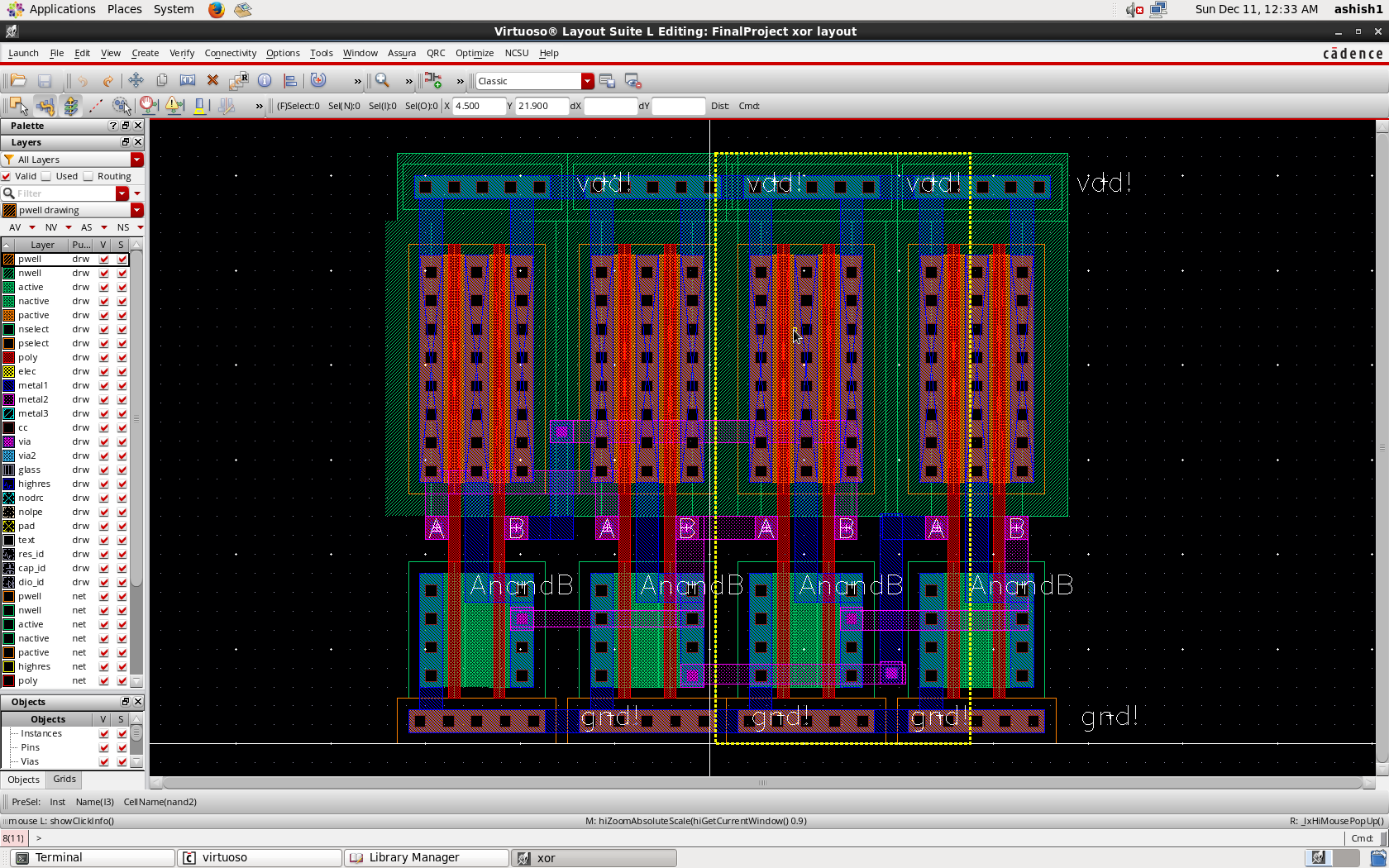


Fig 4. XOR Layout

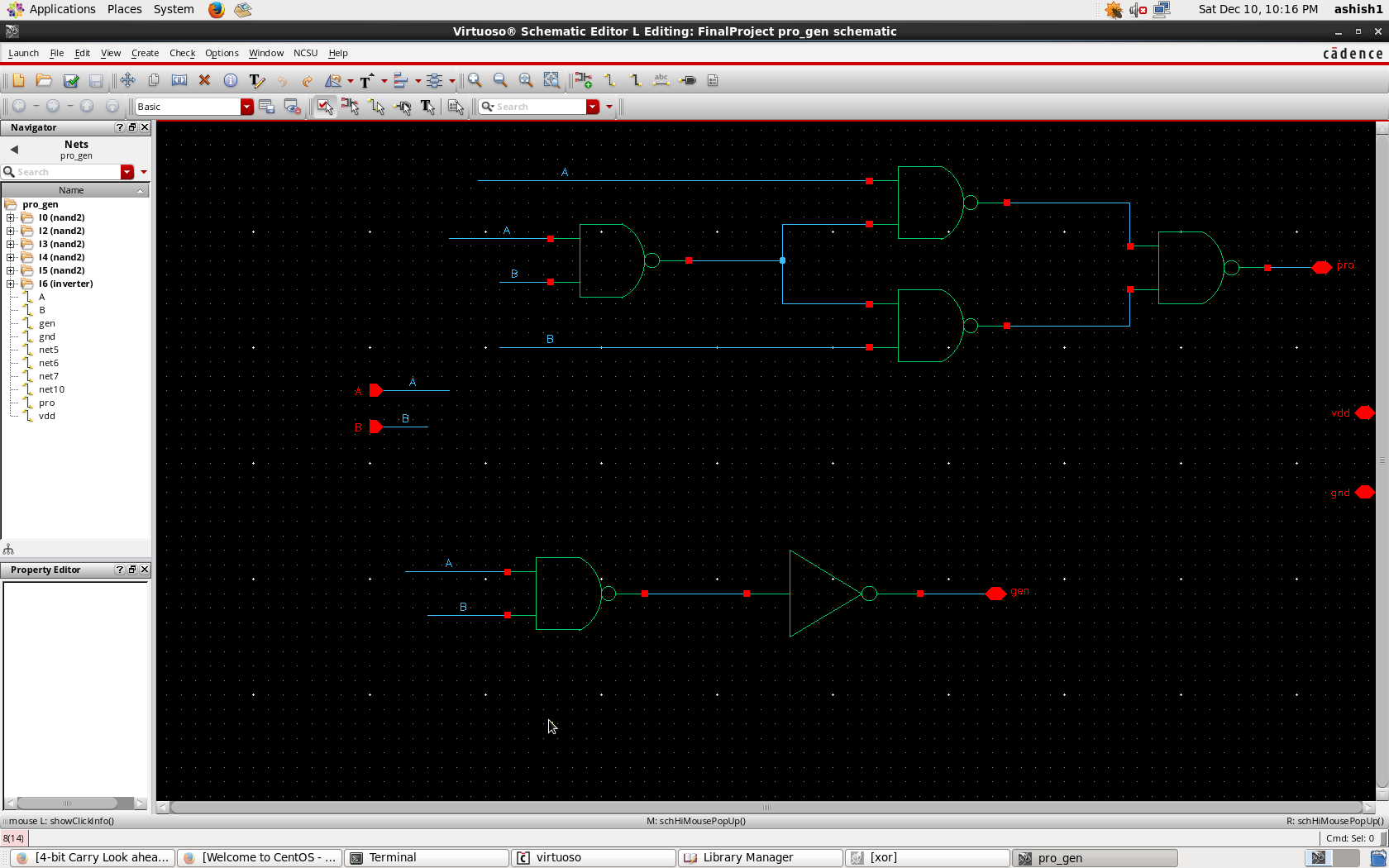


Fig 5. Schematic for Propagate and Generate Block

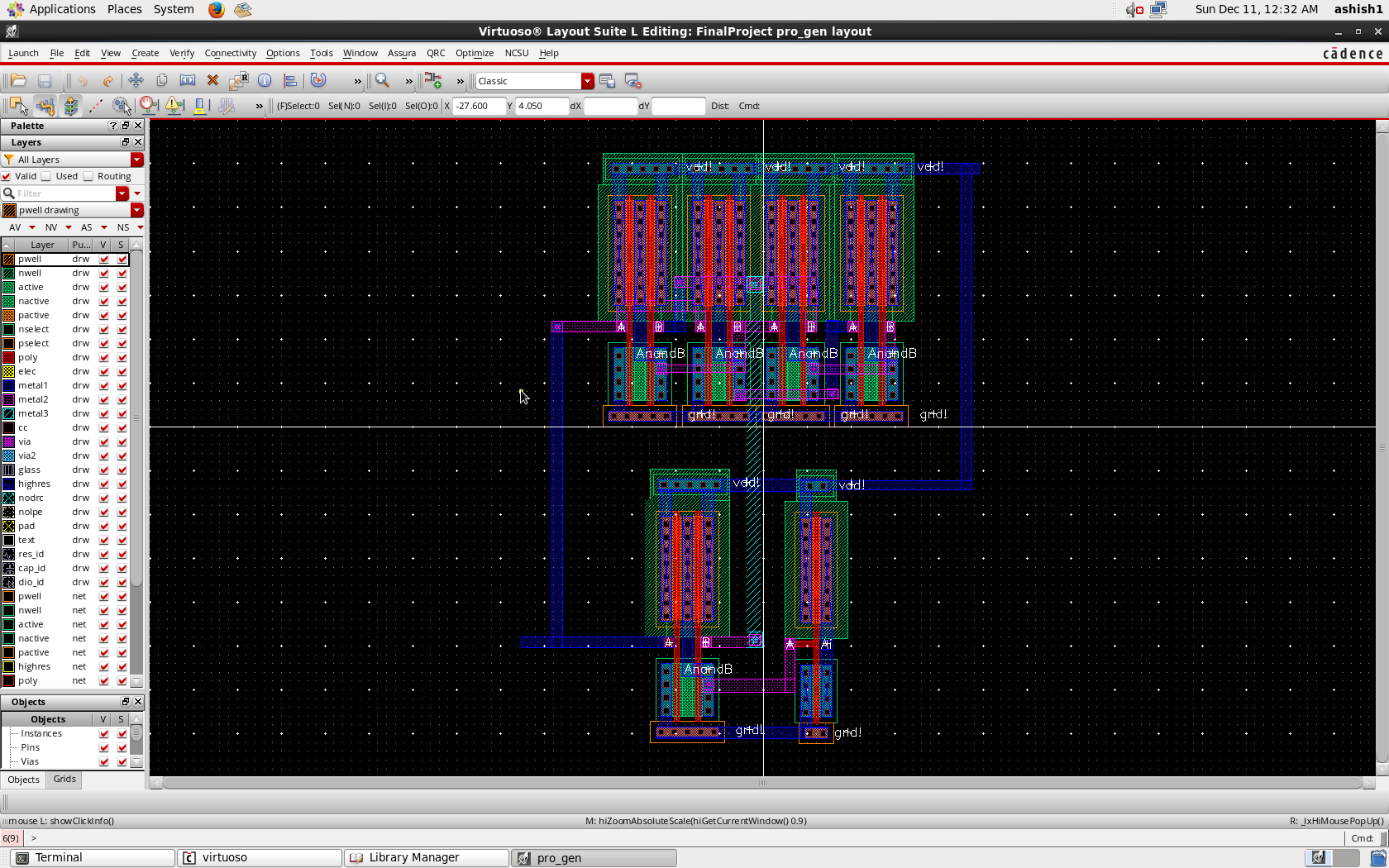


Fig 6. Propagate and Generate Layout



Fig 7. Propagate and Generate Analysis

Carry Look Ahead Adder

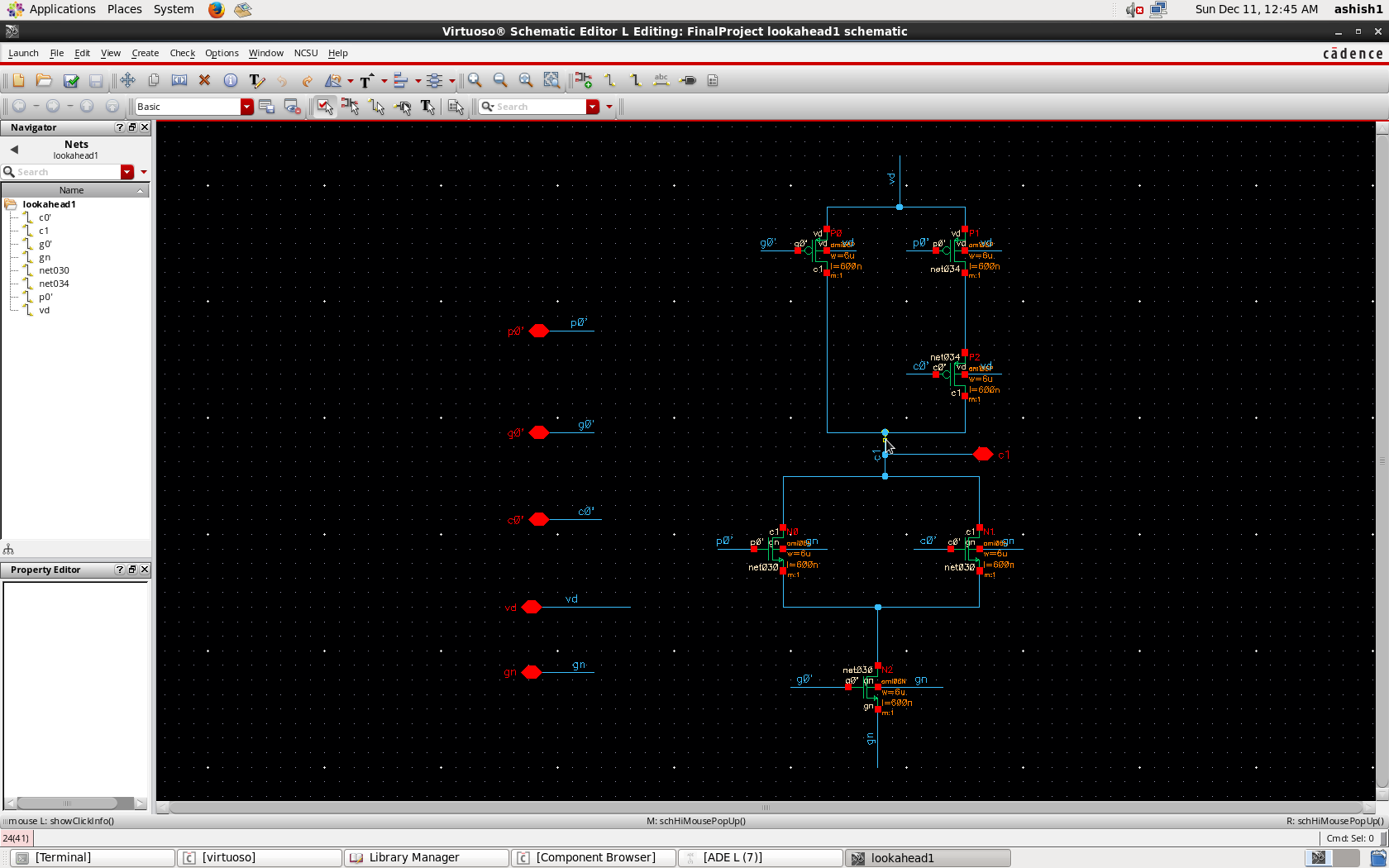


Fig 8. Schematic for C1

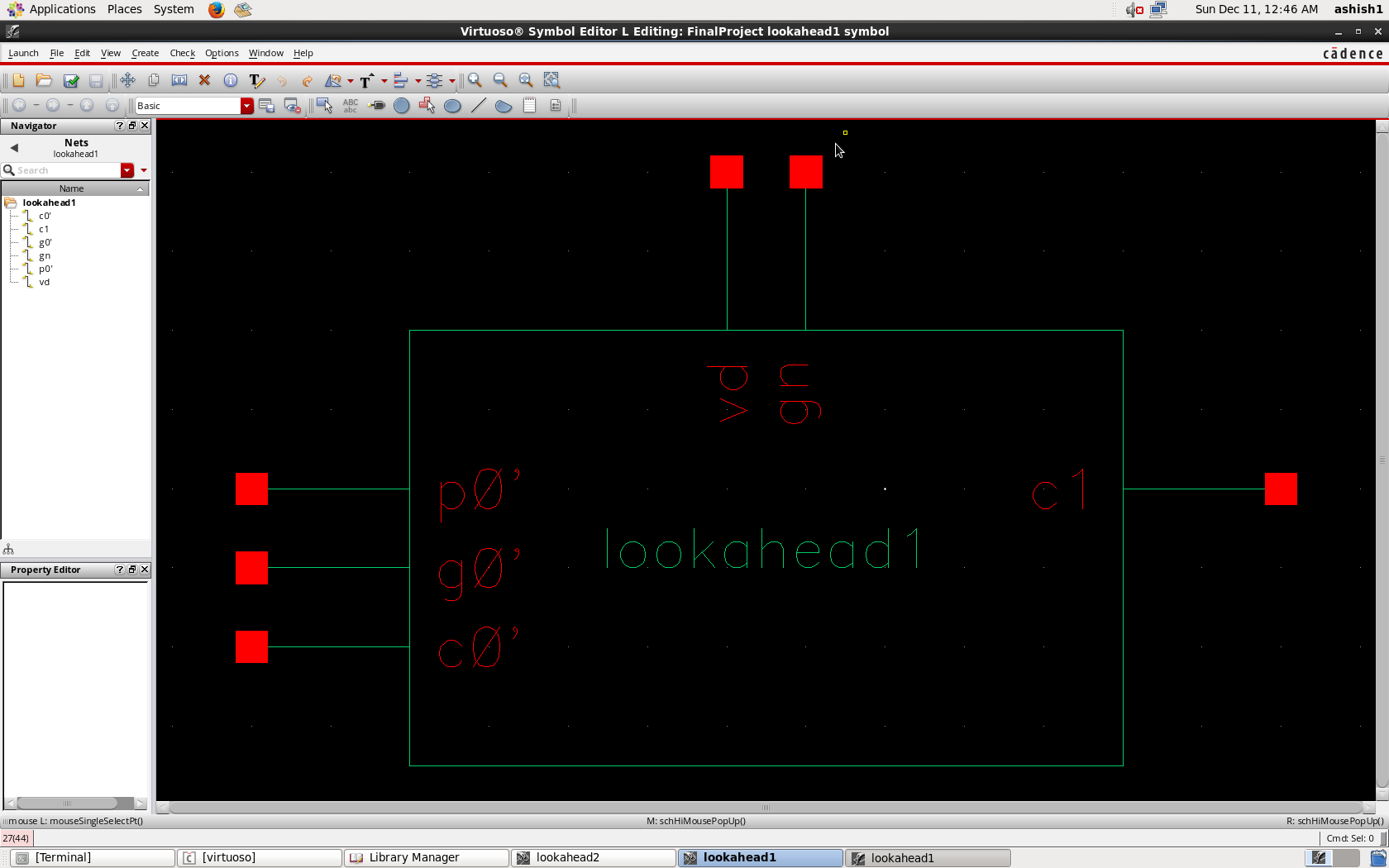


Fig 9. Symbol for C1

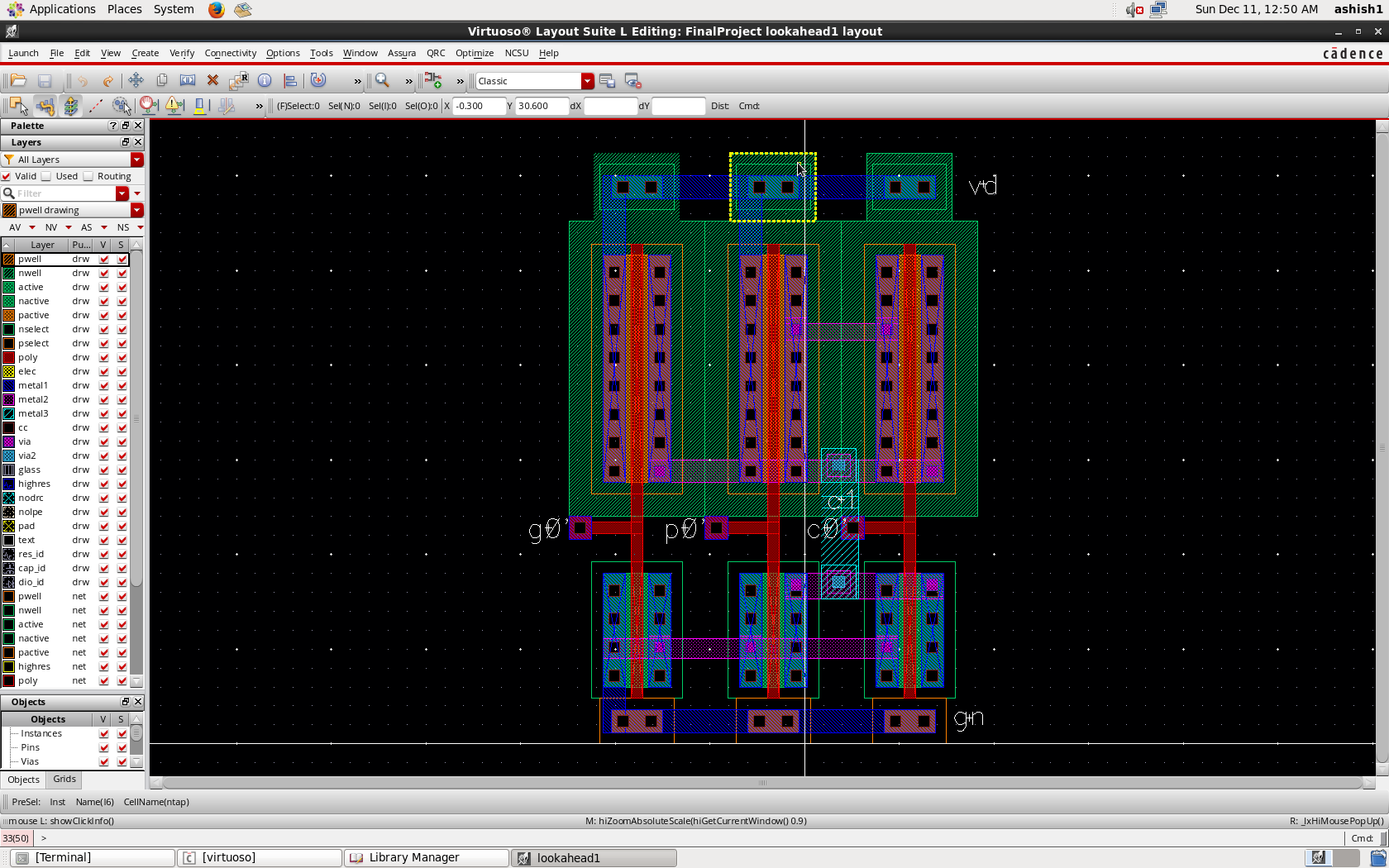


Fig 10. Layout for C1

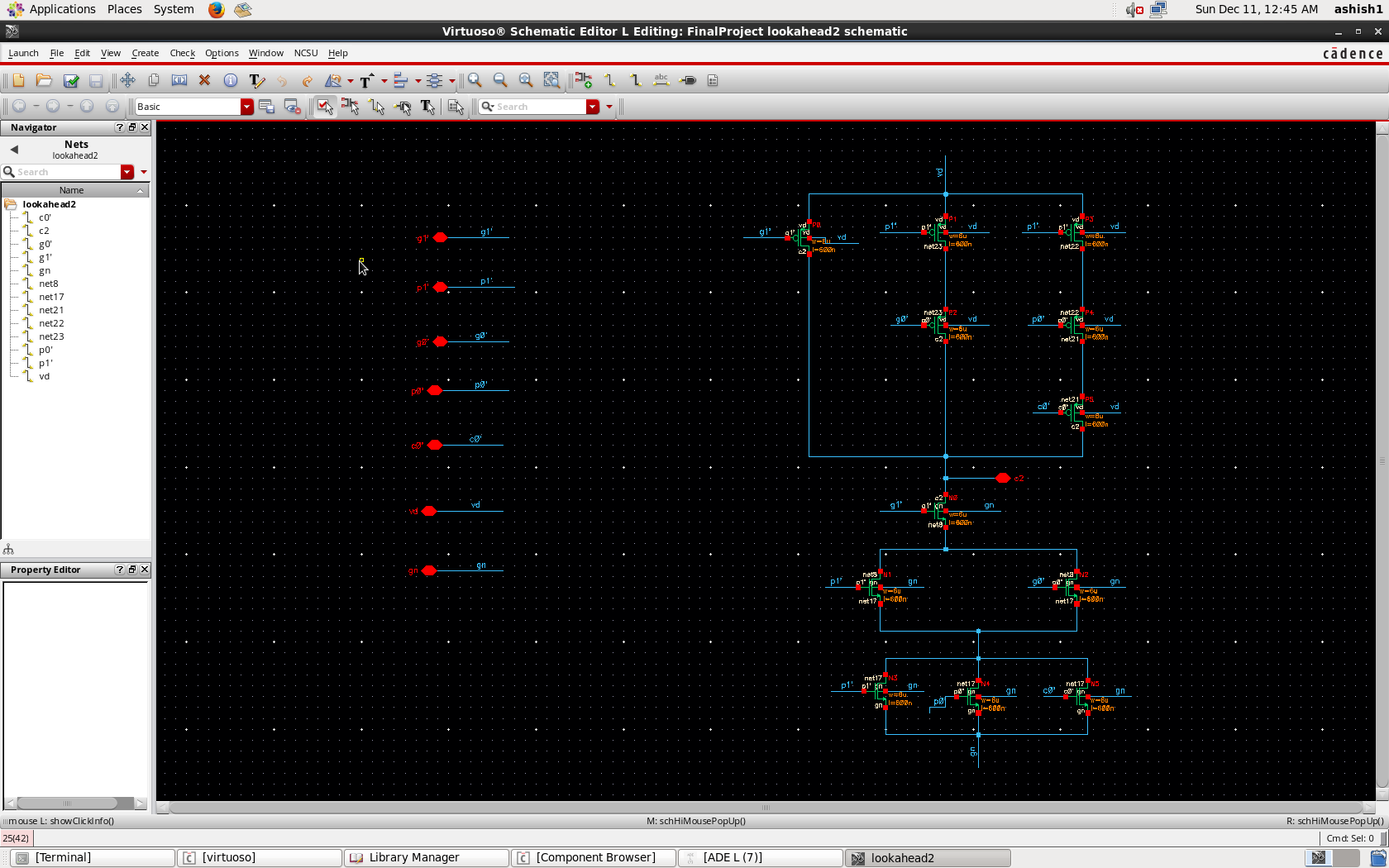


Fig 11. Schematic for C2

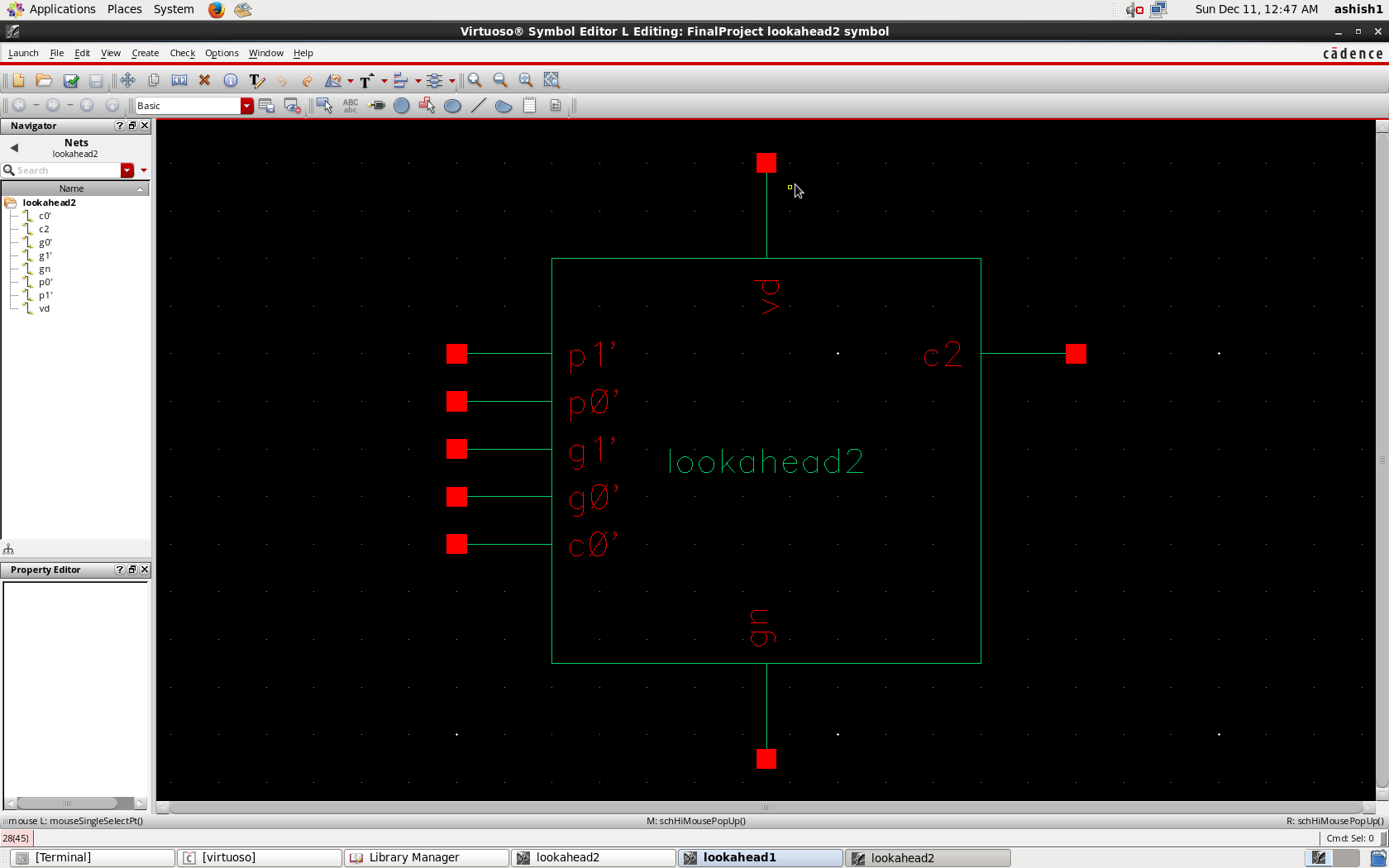


Fig 12.Symbol for C2

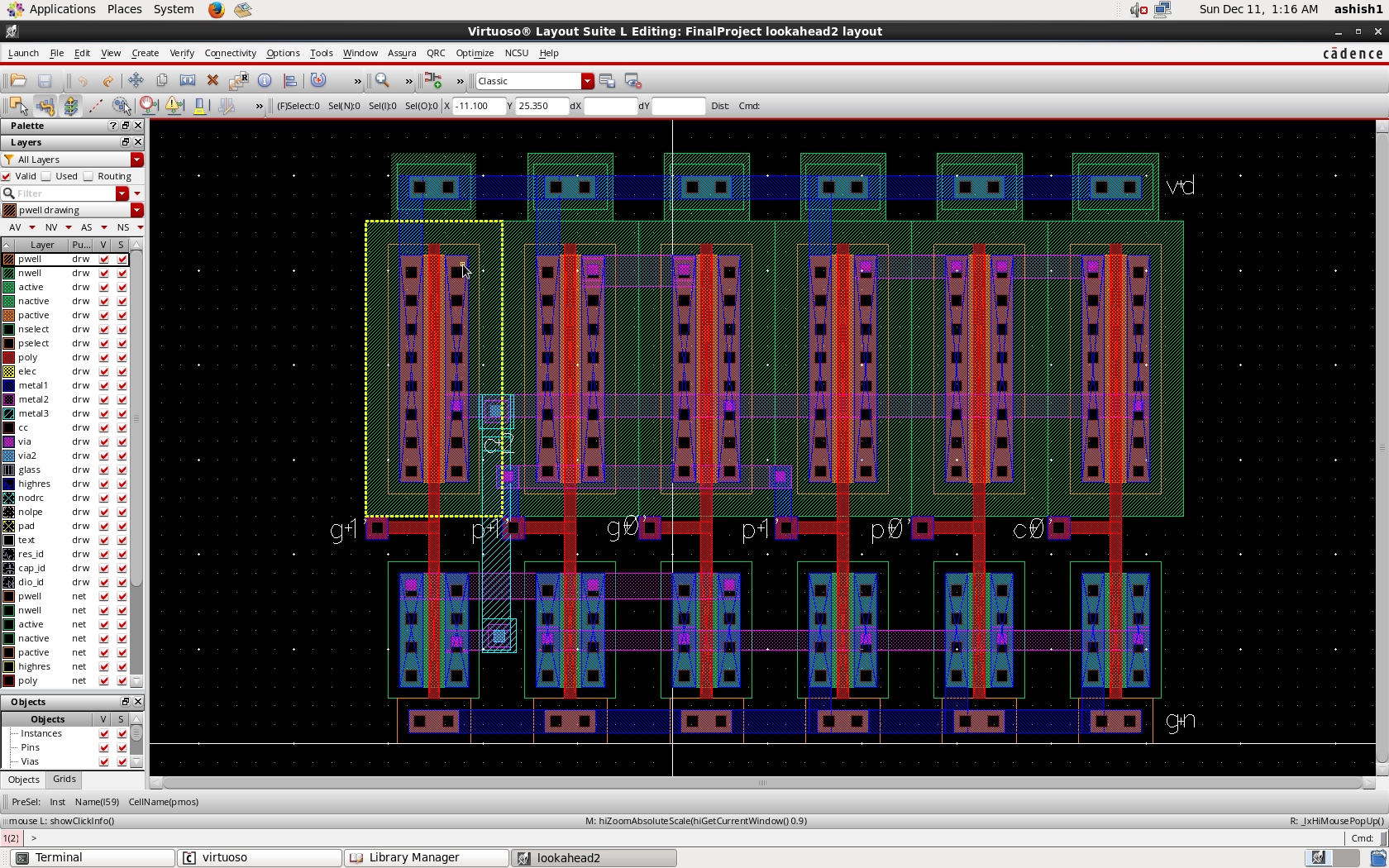


Fig 13. Layout for C2

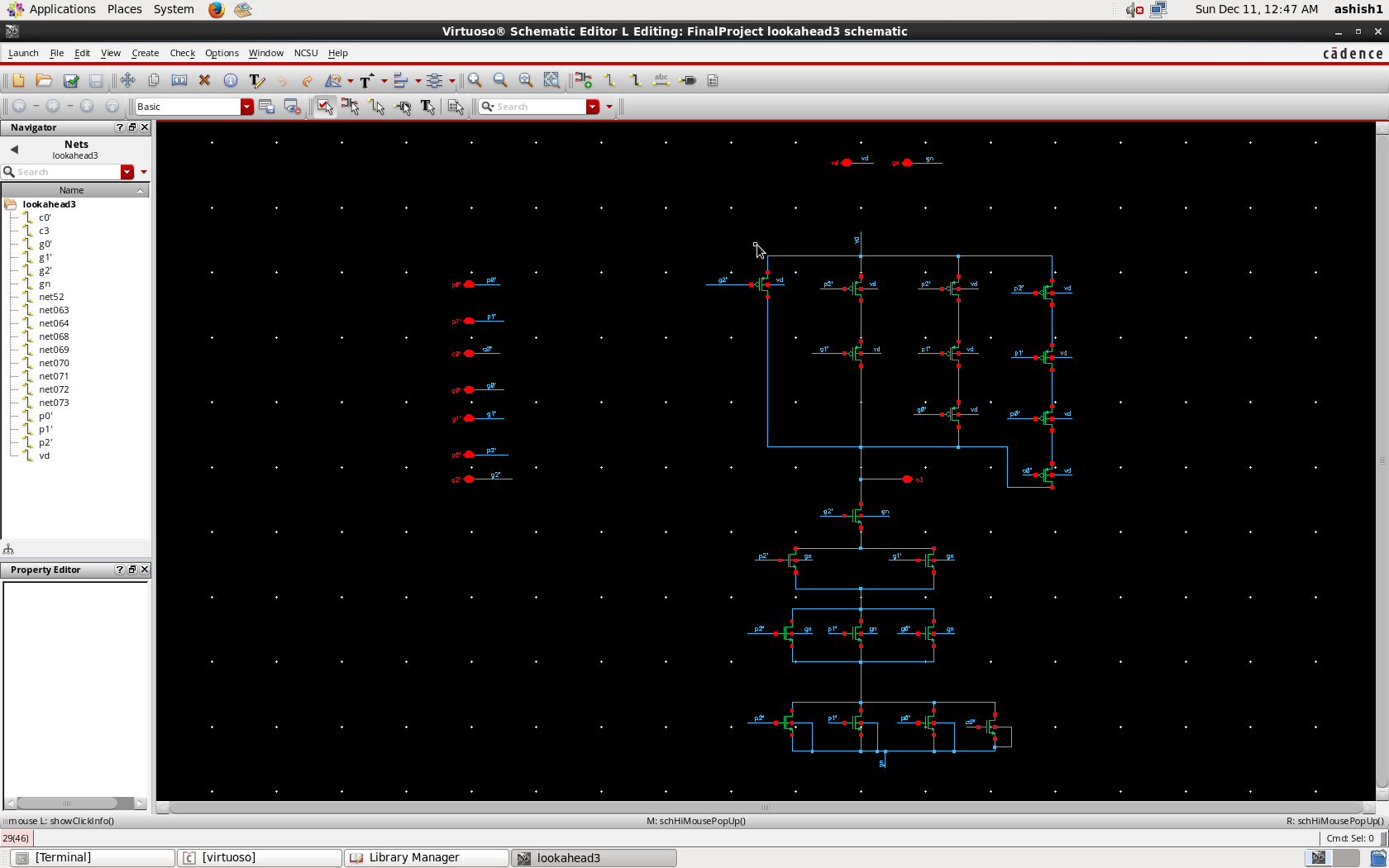


Fig 14. Schematic for C3

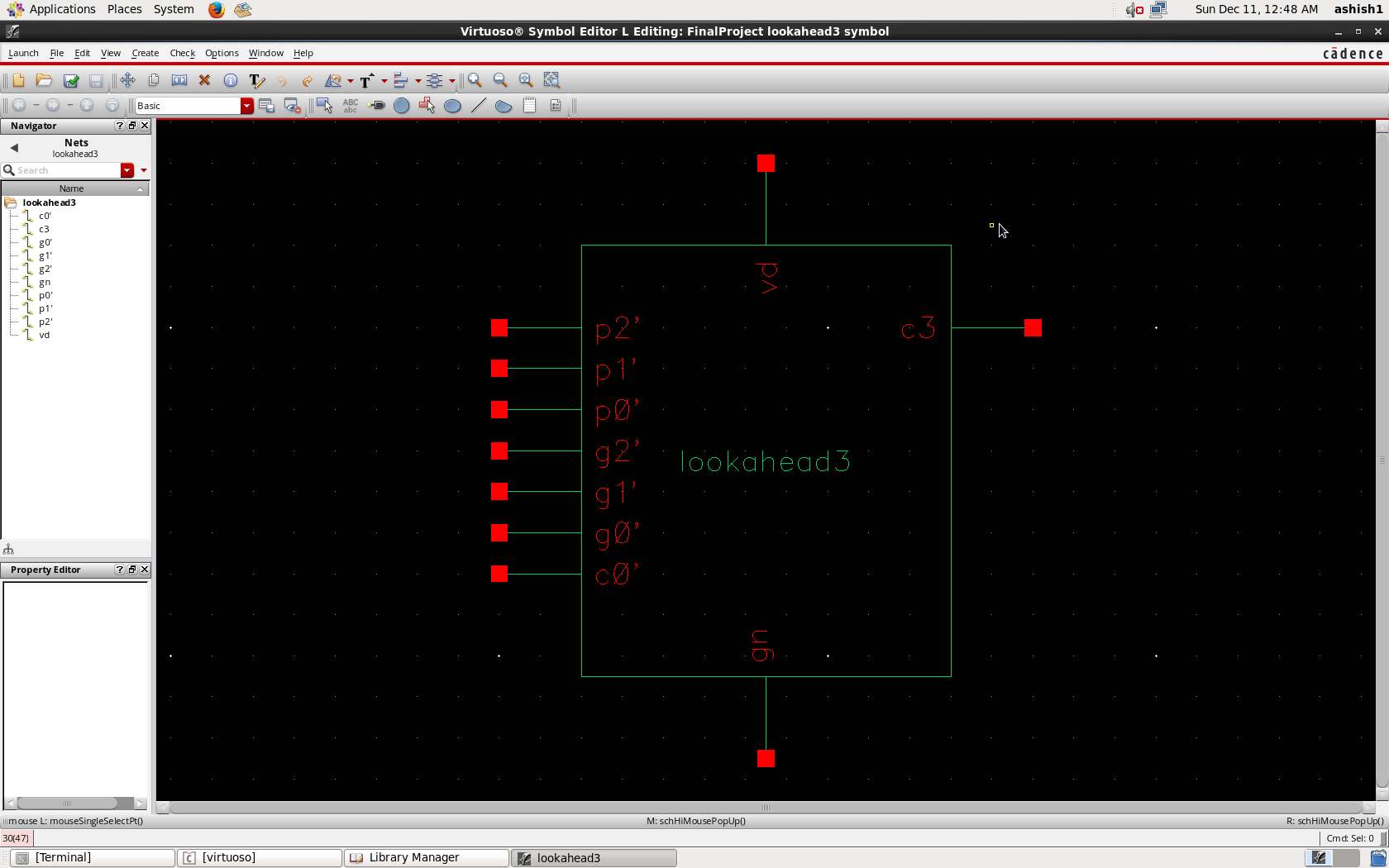


Fig 15. Symbol for C3

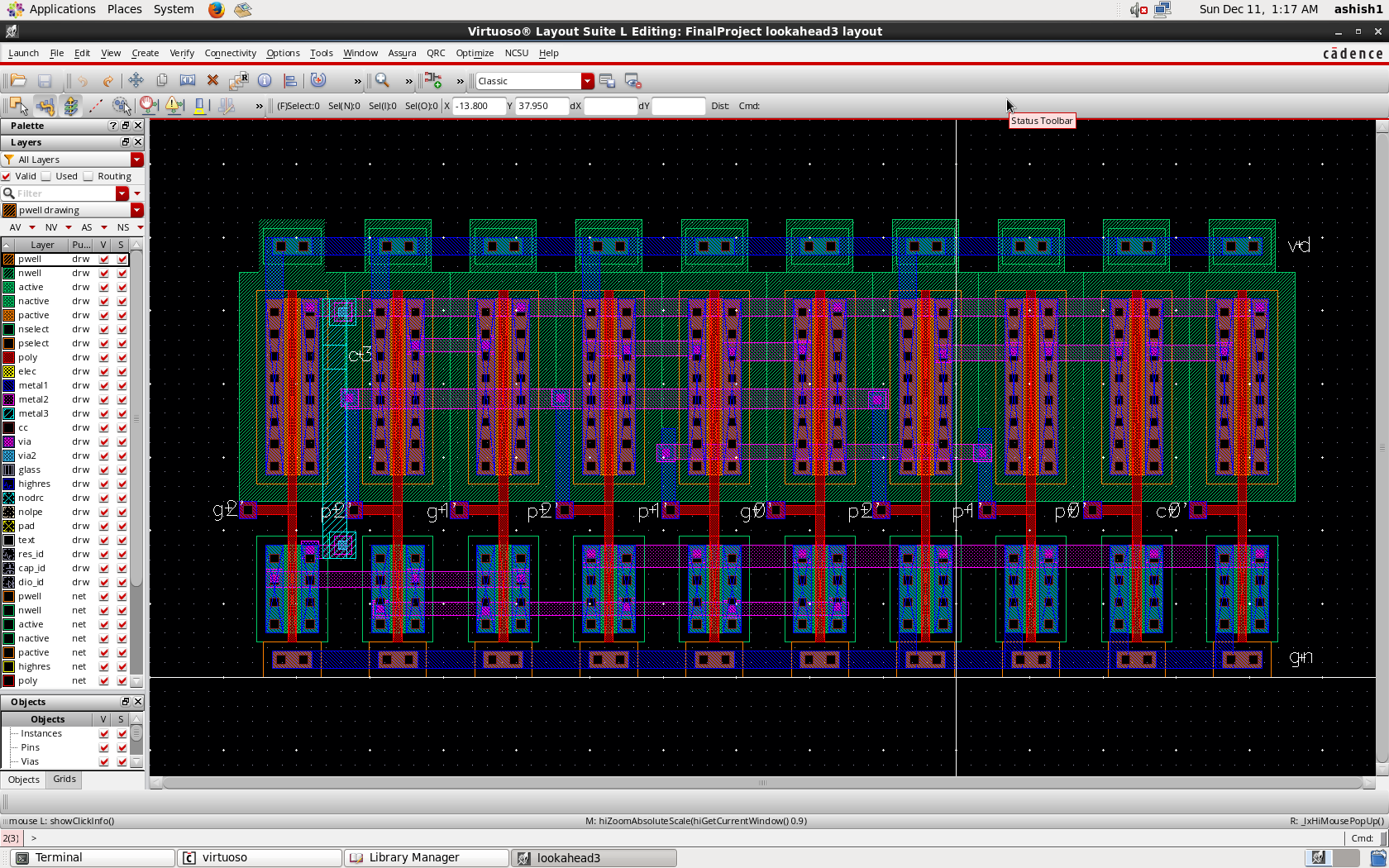


Fig 16. Layout for C3

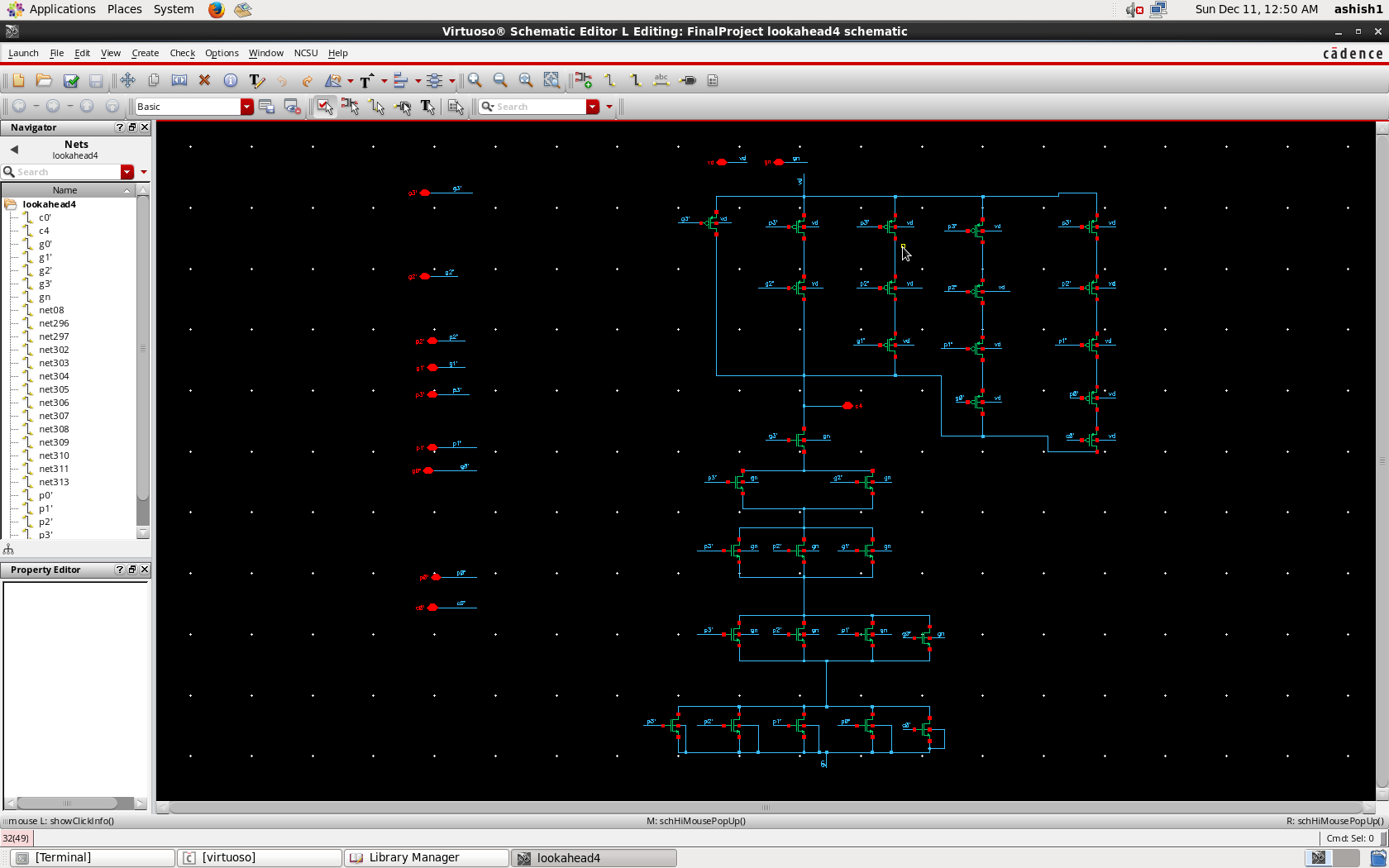


Fig 17. Schematic for C4

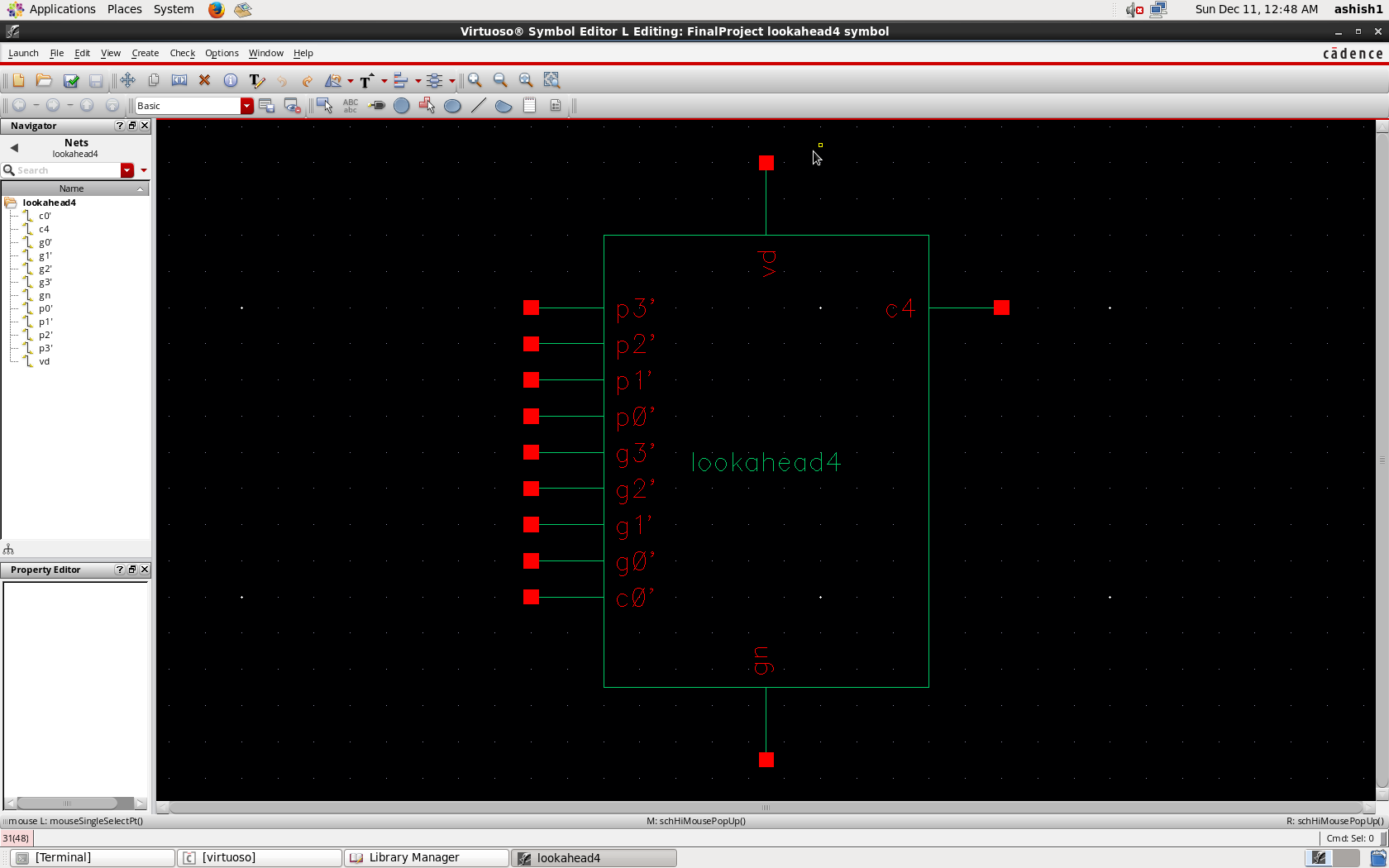


Fig 18. Symbol for C4

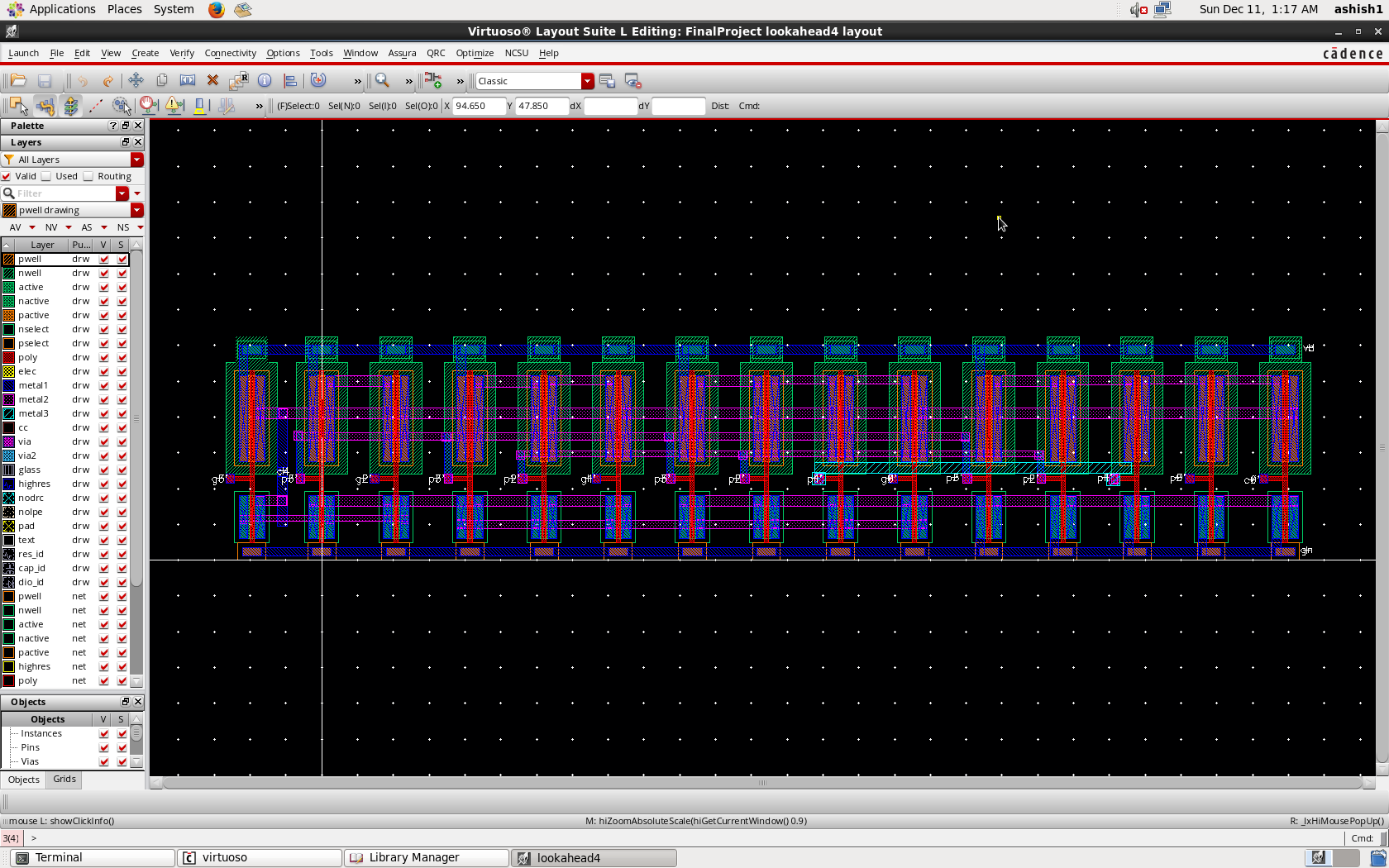
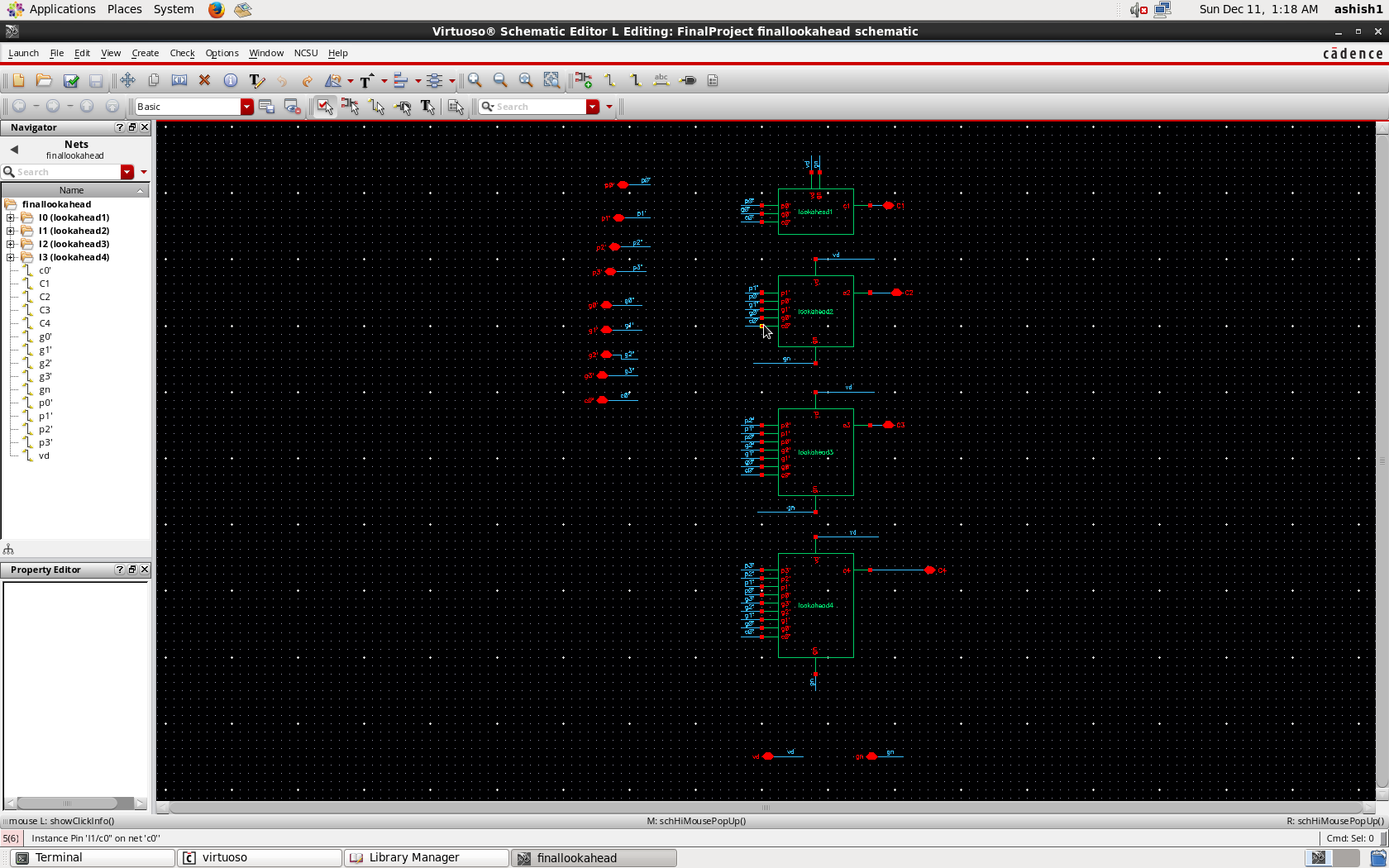
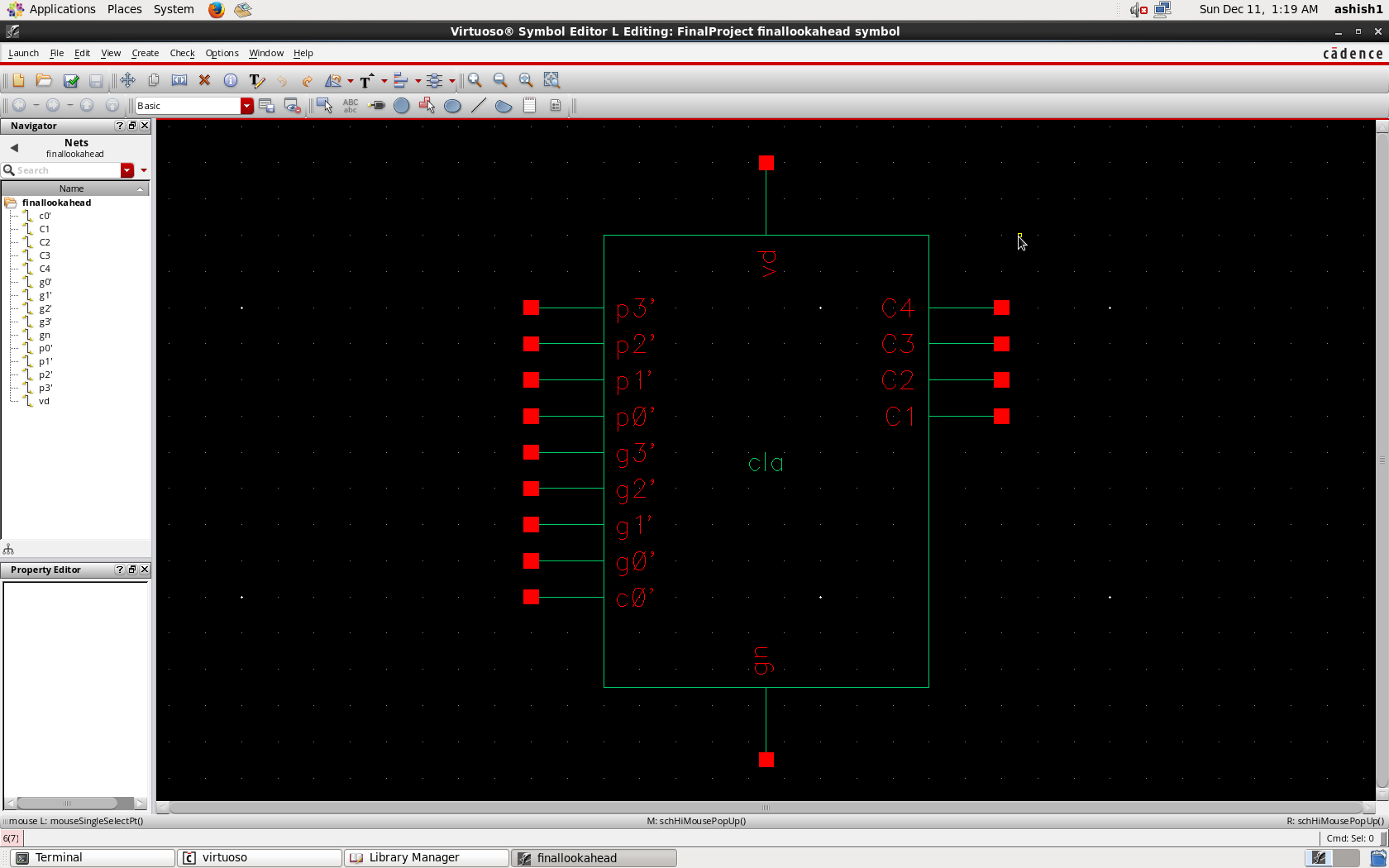


Fig 19. Layout of C4

 Fig 20. Carry Look Block Schematic Fig 21. Carry Look Ahead Block

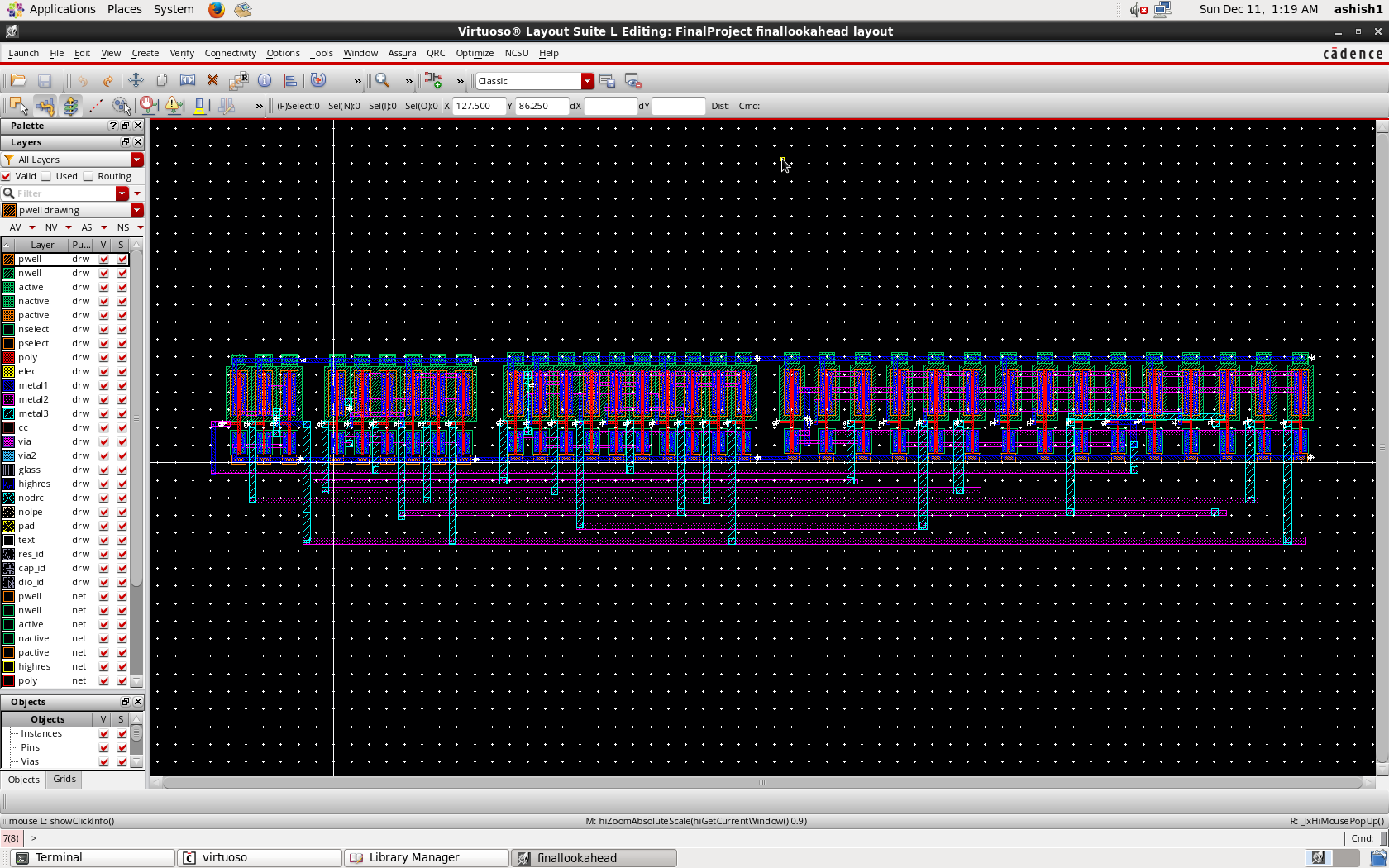


Fig 22. Layout for Carry Look Ahead Adder

Final Circuit

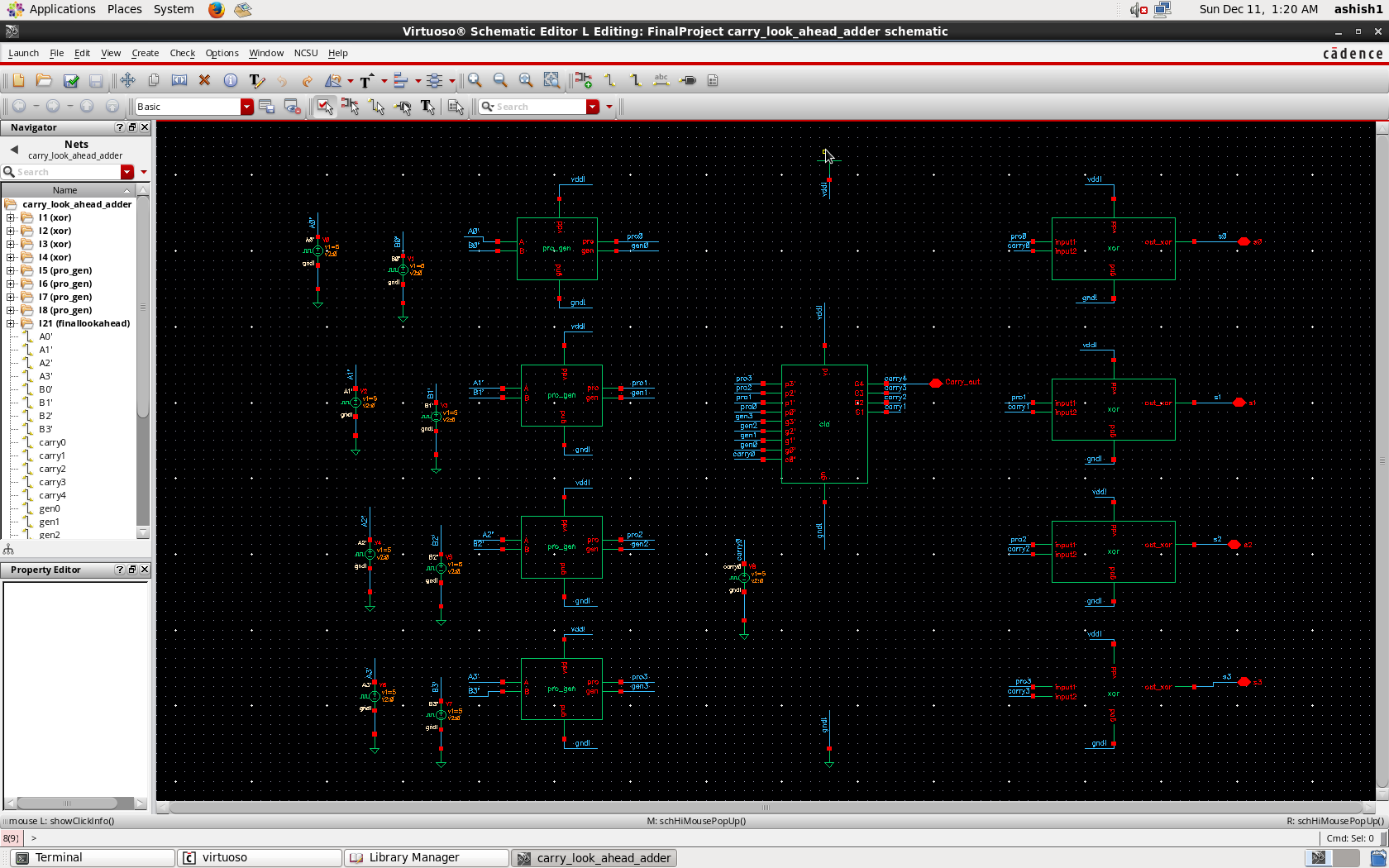


Fig 23. Final 4-bit Carry Look Ahead Adder Circuit



Fig 24. 4-bit CLA Analysis

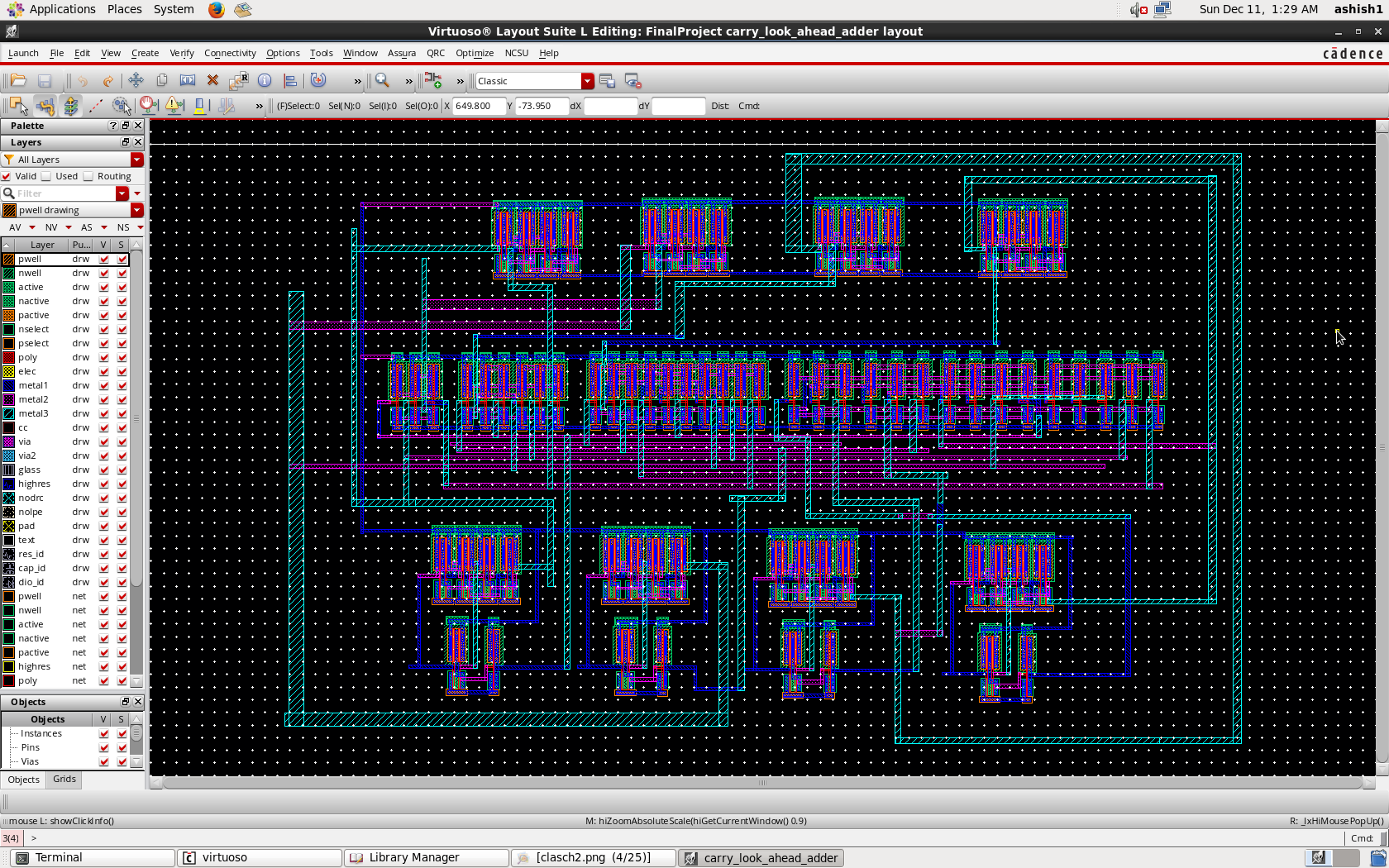


Fig 25. Final Layout for 4-bit CLA

Issues & Troubleshooting

We faced routing issues while designing the Carry look ahead block. Since, we knew to use only two metals (M1 and M2).We solved this problem using using Metal 1 for vertical and metal 2 for horizontal connections and metal 3 for both of them to avoid shorts in the final layout.

Another problem that we faced was power supply. To avoid the problem, we used Global Power supply in the Analog Design Environment. Final problem that we faced was sizing issues. Since the inverter usually has 2:1 sizing ratio, we tried using the same but at times it caused errors. Thus, to overcome this unstable errors we kept the size as 6 um for every transistor we placed in the circuits.

Conclusions

We designed 4- bit carry look ahead adder in Cadence virtuoso using AMI 0.60u C5N technology and simulated it using Analog Design environment. The output of each of the Block that we have created has been put in the project paper for future references.

References

[1]Analysis & implementation of ultra low-power 4-bit CLA in subthreshold regime by Priya Gupta; Ishan Munje; Nikhil Kaswan; Anu Gupta; Abhijit Asati  
2014 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2014]

[2]CMOS Logic Design Circuit - A Circuit and Systems Perspective by Neil H.E Weste And David Money Harris

[3]Carry Look Ahead - Wikipedia