Design of a 4- Bit Carry Look Ahead Adder Using Cadence Virtuoso Tool

**Abstract:**

Based on the truth table for Full-adder, the algorithms for Sum and Carry-out have been carried out for

A3 A2 A1 A0

+ B3 B2 B1 B0

C4 S3 S2 S1 S0

The initial carry has been grounded which makes it as a half adder which assures that no carry is propagating. This distinguishes the 4-bit carry look ahead adder from ripple carry adder. The timing for 4-bit carry look ahead adder as well as 4-bit ripple carry adder are also simulated.

In this paper the design and implementation of 4-Bit carry look ahead adder is made using cadence virtuoso. The AMI 600nm C5N Technology is used and the simulations are done using the Analog Design Environment. This approach reduces the power consumption by calculating the carry bits in parallel there by reducing the time required to calculate the carry bits. A bottom up design approach is adopted with the sum, propagate-generate and carry block are designed and tested and finally all the components are put together and design layout is created and simulations are tested. This adder predicts the carry signal within 4 clock cycles and reduces the number of gates through which carry signal is propagated.