Memory Subsystem

For UMass Lowell 16.480/552

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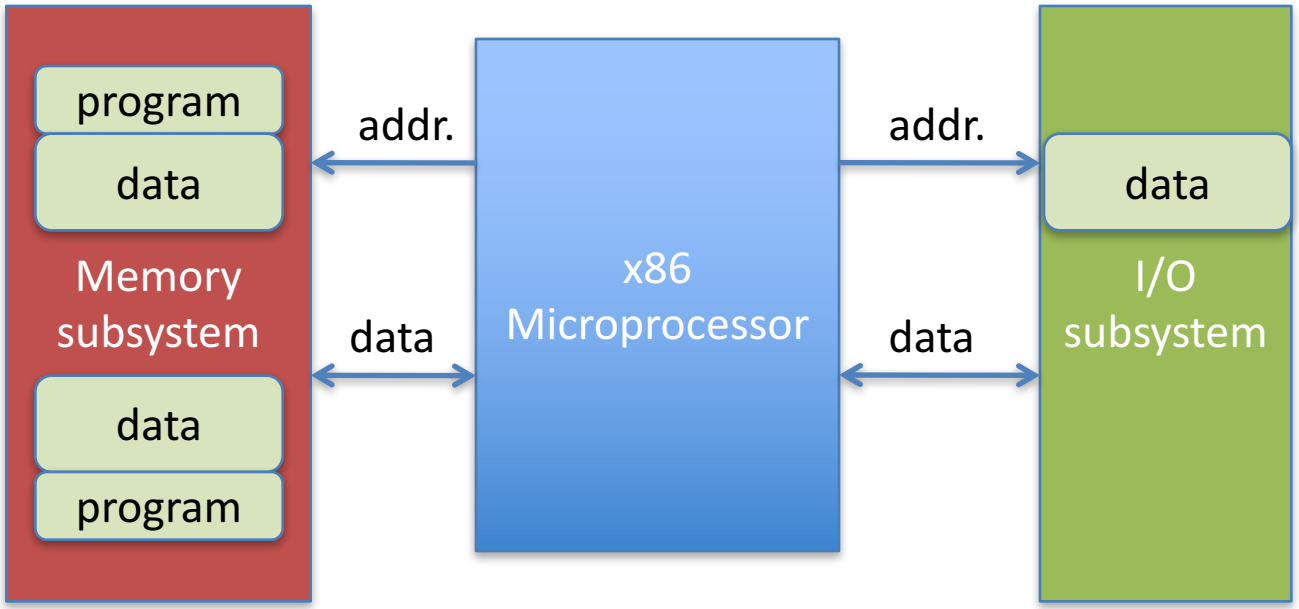
Outline

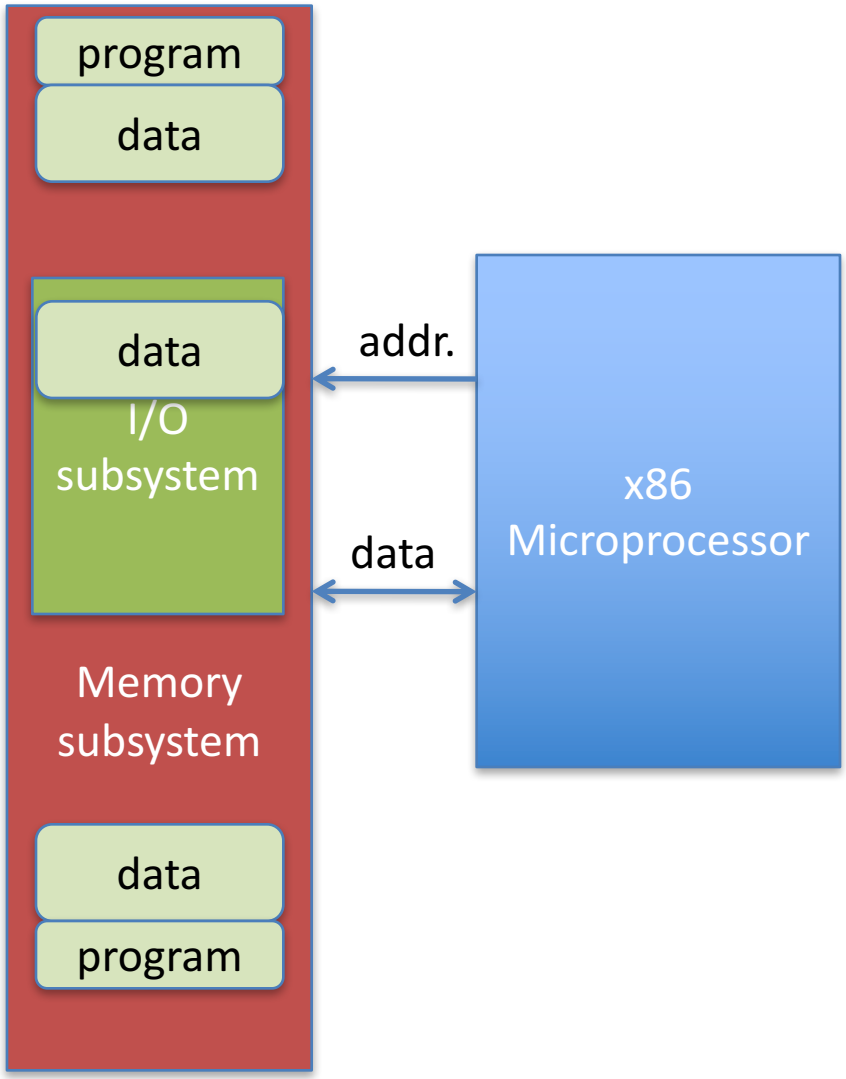
- Overview of x86 memory and software architecture
- Memory types
- Memory interfacing
- Virtual memory

Acknowledgment:
Some of the figures used in the slides are from Brey's "Intel Microprocessors", 8th ed.

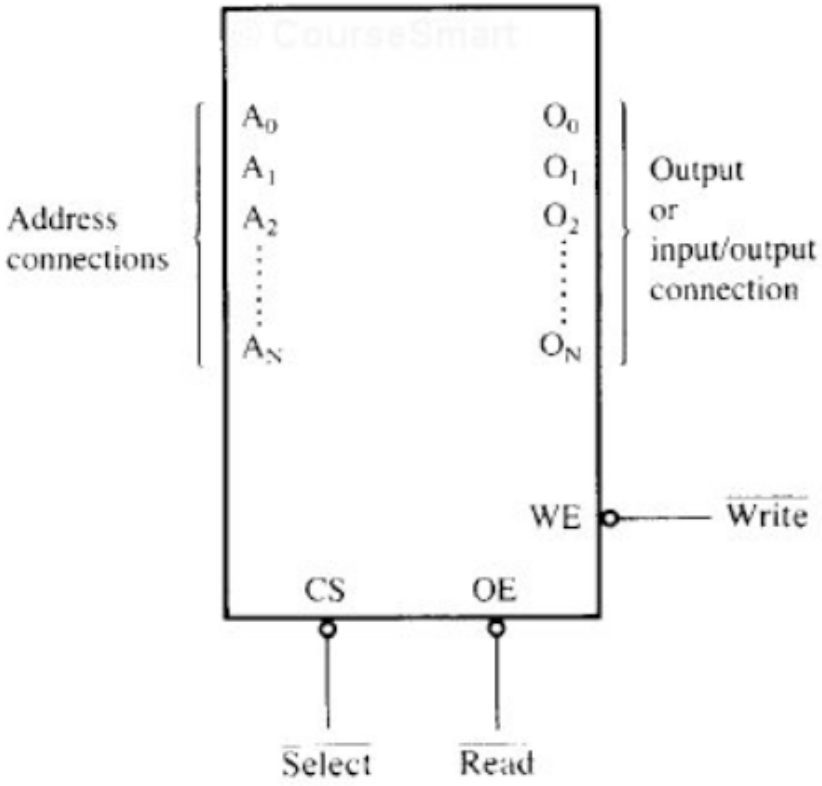
Isolated memory and I/O



Memory mapped I/O



A Memory Component



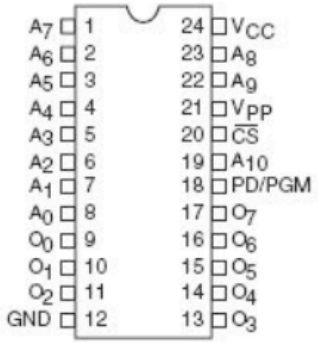
- Figure 10-1 in Brey's book

Types of Memory Components

- ROM, PROM, EPROM, EEPROM
- RAM:
  - SRAM
  - DRAM (DDR, DDR2, DDR3)
- Flash memory (EEPROM, NOVRAM)
  - requires more time to erase than RAM

EPROM

PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

MODE SELECTION

PINS / MODE	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM

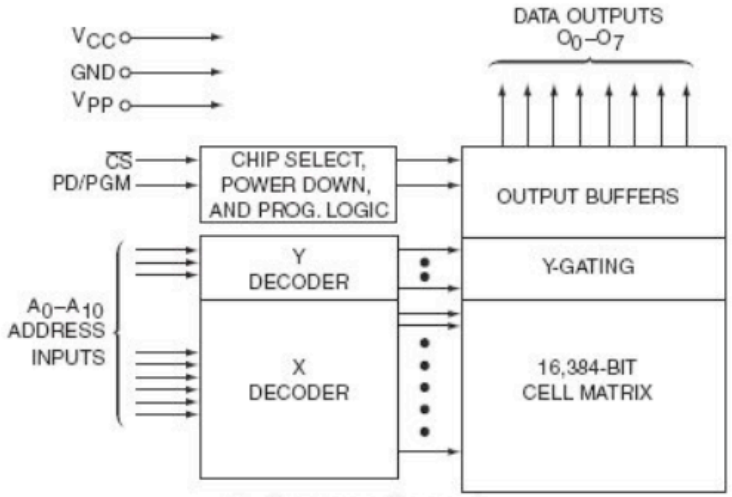


FIGURE 10–2 The pin-out of the 2716, 2K × 8 EPROM. (Courtesy of Intel Corporation.)

Timing of EPROM 2716

A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

WAVEFORMS

A. Read Mode

PD/PGM = V_{IL}

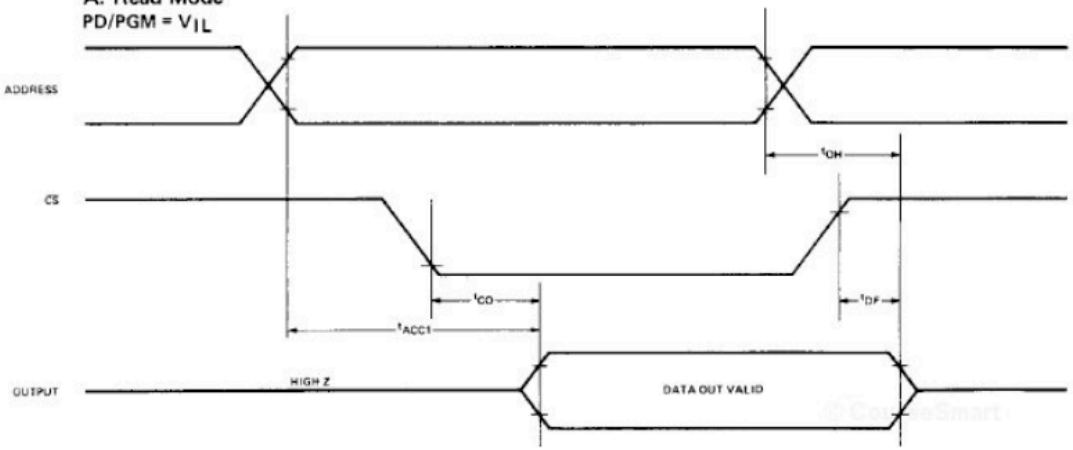
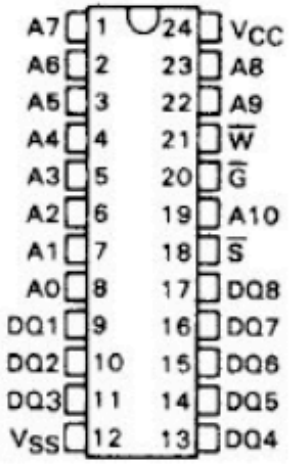


FIGURE 10–3 The timing diagram of AC characteristics of the 2716 EPROM. (Courtesy of Intel Corporation.)

SRAM

FIGURE 10–4 The pin-out of the TMS4016, 2K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)

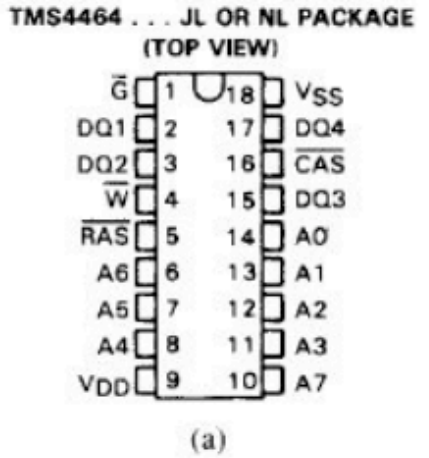
TMS4016 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

DRAM

FIGURE 10–7 The pin-out of the TMS4464, 64K × 4 dynamic RAM (DRAM). (Courtesy of Texas Instruments Incorporated.)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

(b)

- retains data only 2 or 4ms on integrated capacitor
- needs rewritten (refreshed)
- too many address pins!
  - 64K x 4 DRAM (16-bit address required)
  - use 8 address pins in two 8-bit increments
  - require: column address strobe (**CAS***) and row address strobe (**RAS***)
  - CAS* is also chip select

DRAM timing

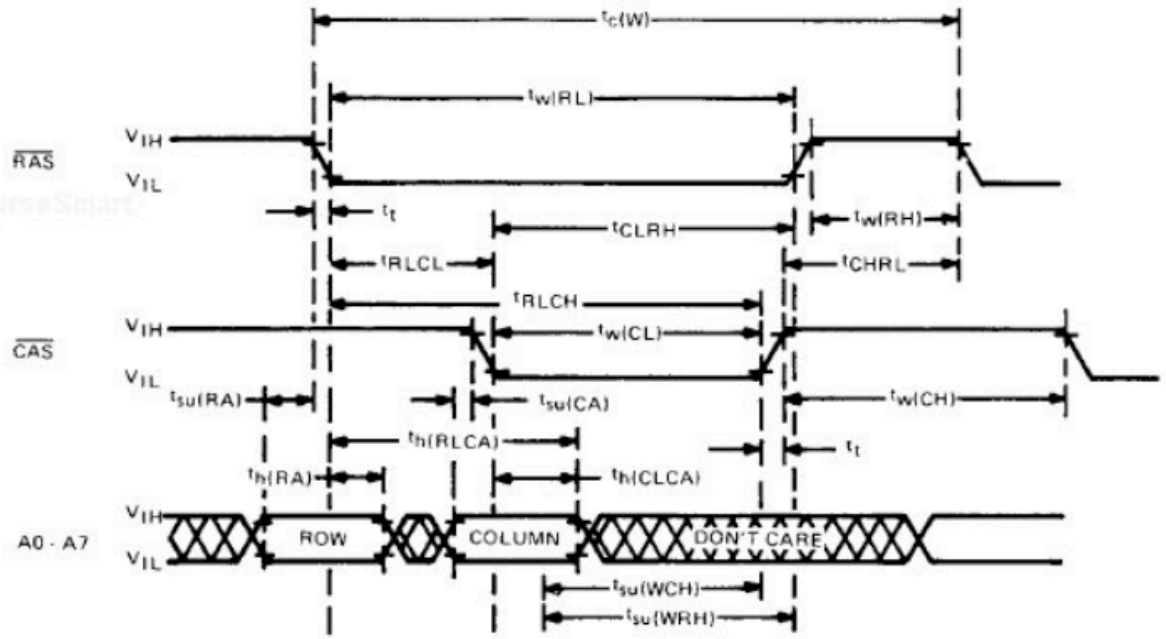


FIGURE 10–8 $\overline{RAS}$, $\overline{CAS}$, and address input timing for the TMS4464 DRAM. (Courtesy of Texas Instruments Incorporated.)

Address Multiplexer for DRAM

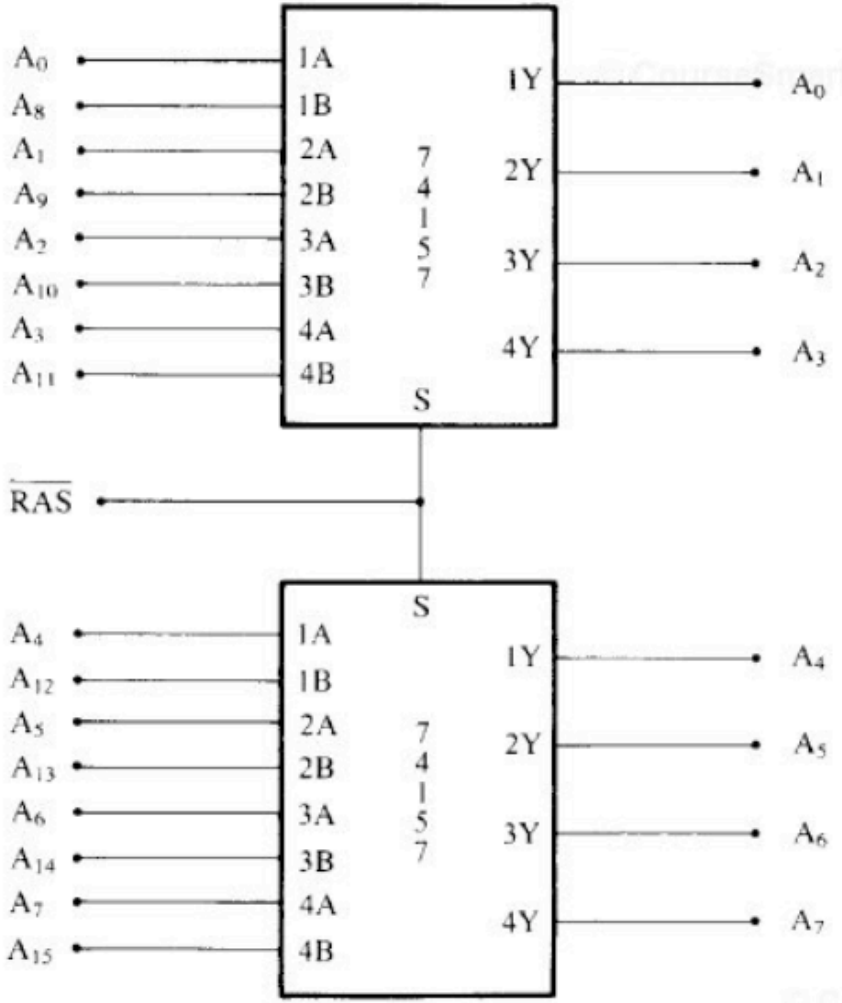


FIGURE 10–9 Address multiplexer for the TMS4464 DRAM.

- Single Inline Memory Module (SIMM)

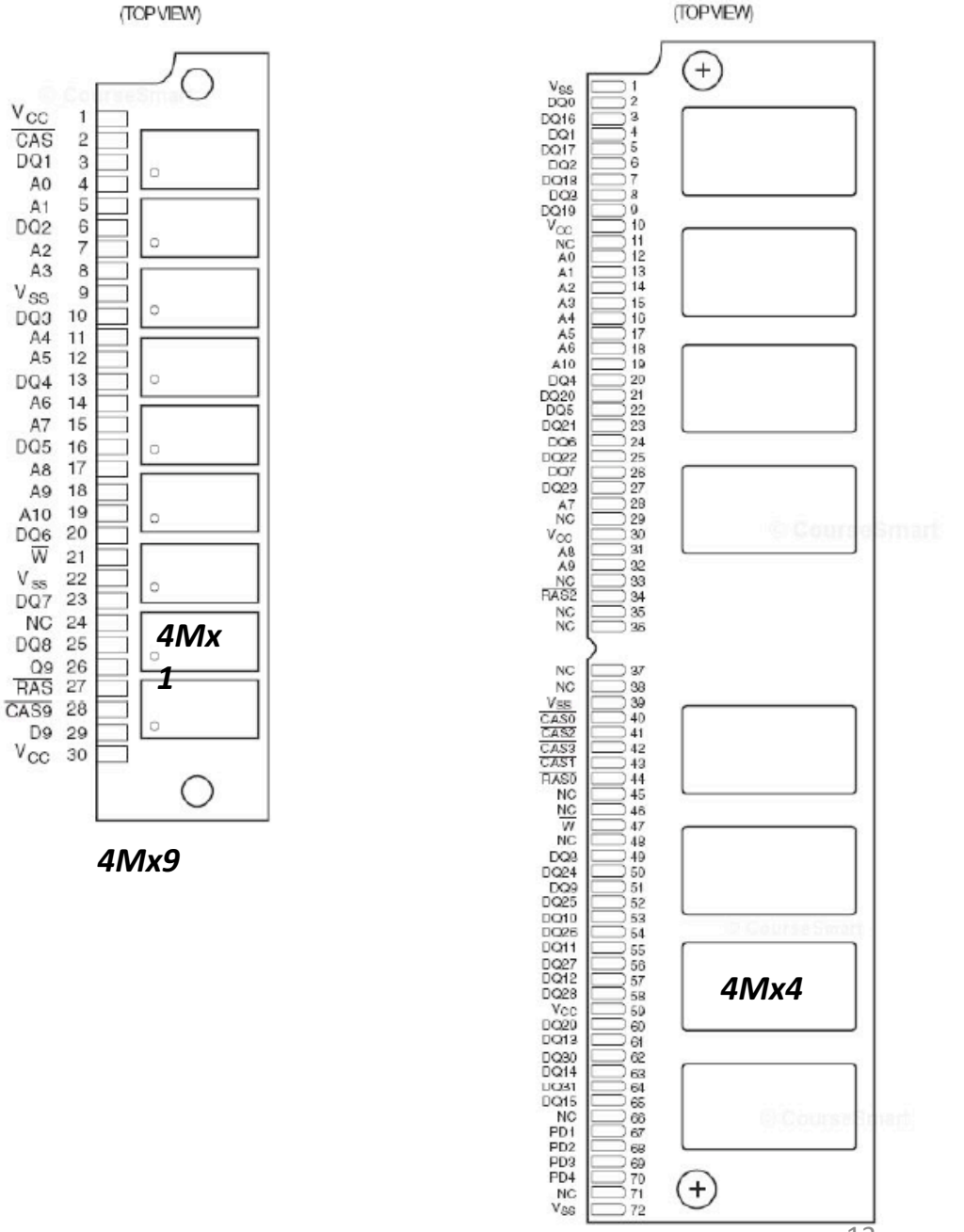


FIGURE 10–11 The pin-outs of the 30-pin and 72-pin SIMM. (a) A 30-pin SIMM organized as 4M × 9 and (b) a 72-pin SIMM organized as 4M × 36.

Dual Inline Memory Module (DIMM)

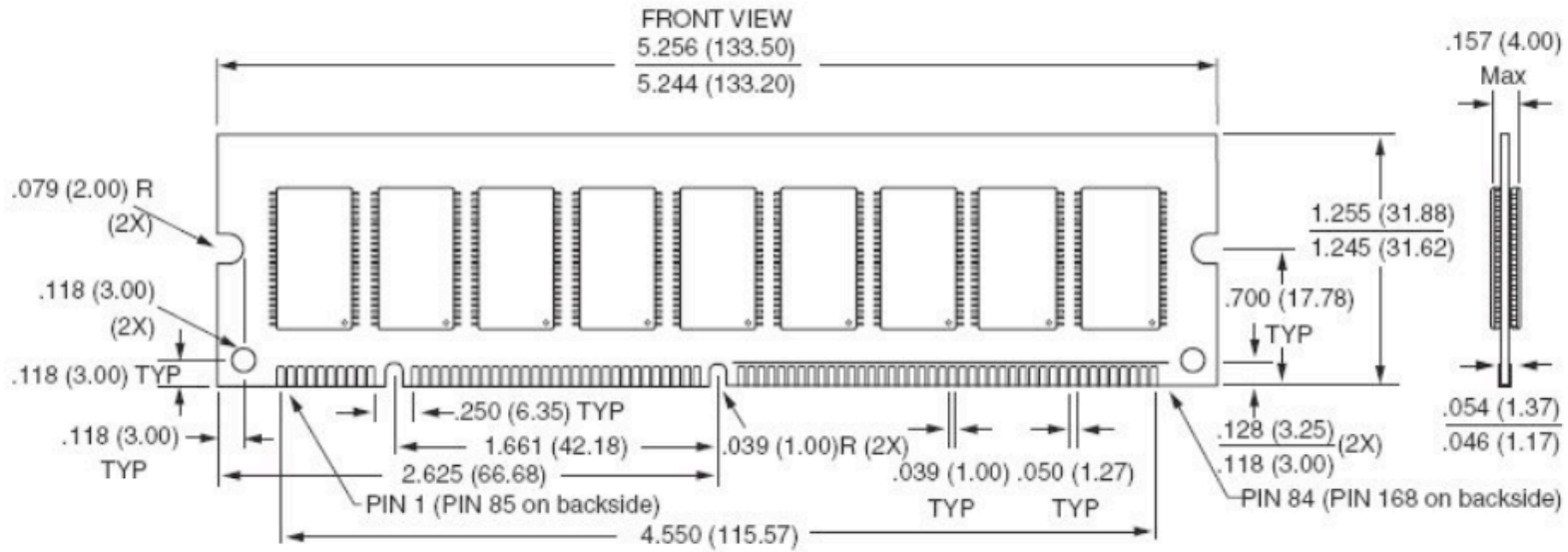


FIGURE 10–12 The pin-out of a 168-pin DIMM.

Flash Memory

- To store information changed occasionally
  - Fast read, slow write
- Requires 12V to erase and write data
  - Newer ones require 5V or even 3.3V
- Operation
  - Signals similar to SRAM, e.g. CE*, OE*, WE*
  - Erase and write data: V_{PP} (12V) and PWD*

Serial EEPROM

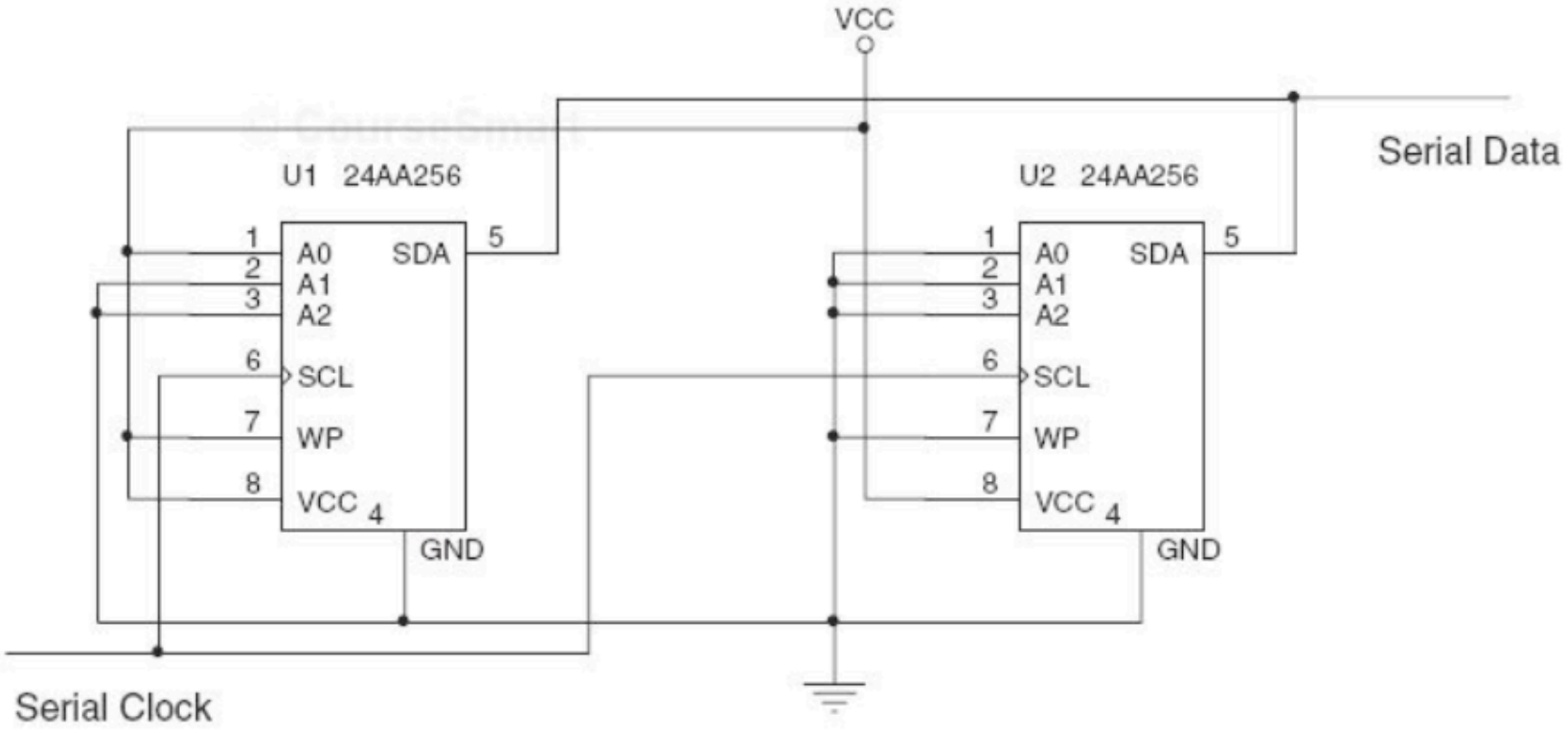


FIGURE 10–23 A serial EEPROM interface.

Serial Data Transfer Protocol

Write Address

S	1	0	1	0	A2	A1	A0	0	ACK	x	A14	A13	A12	A11	A10	A9	A8	ACK	A7	A6	A5	A4	A3	A2	A1	A0	ACK

Followed by for a Read Byte

S	1	0	1	0	A2	A1	A0	1	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	P

or Followed by for a Write Byte

D7	D6	D5	D4	D3	D2	D1	D0	ACK	P

S = Start
P = Stop
ACK = acknowledge

FIGURE 10–24 The data signals to the serial EEPROM for a read or a write.

Address Decoding

- the number of address pins mismatch
  - e.g. 8088 20-bit address vs EPROM2716 with 11-bit address
  - 8088 thinks it has 1MB, but only a 2KB EPROM is available
  - A10-A0 are connected directly
  - what about A19-A11 ?
  - ***decode*** the address pins that do not connect to memory components

Example

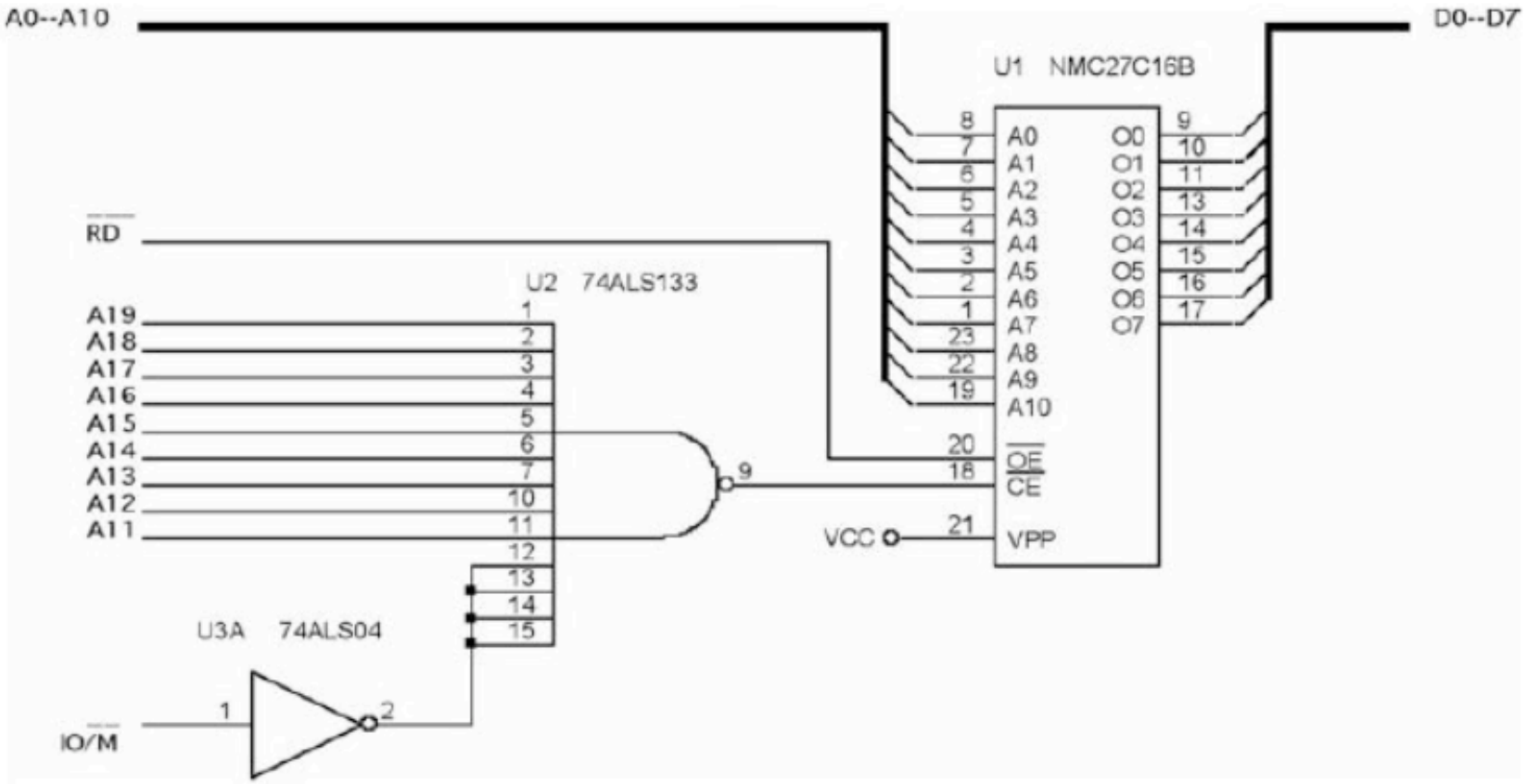
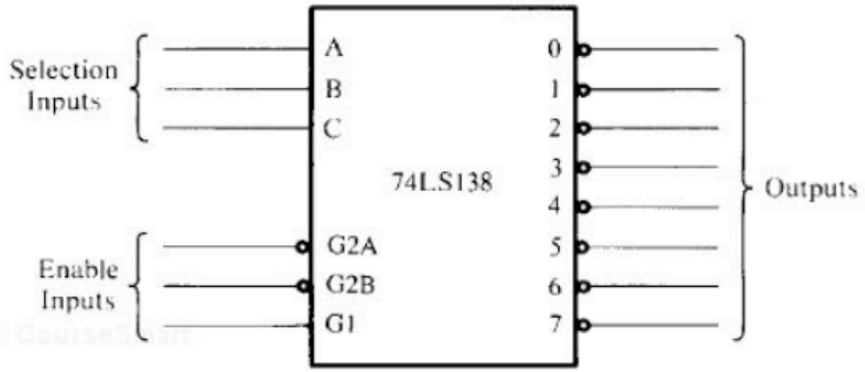


FIGURE 10–13 A simple NAND gate decoder that selects a 2716 EPROM for memory location FF800H–FFFFFH.

3-8 decoder



Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Exercise [30 minutes]

Problem: given enough 2764 EPROMs, build a 64K x 8 section of memory starting from **E0000H**.

Hints:

- 2764 has 8K bytes : ?-bit address bus, 8-bit data bus
- signals coming from the processor: A19-A0, RD*, M*/IO
- use 3-8 decoder(s)

DRAM revisited

- Benefits
  - Higher density than SRAM
  - Less expensive than SRAM
- Requires address multiplexing
  - Break long address into Row and Column
- refreshing
  - Refresh needed as internal capacitor lose charge in a short period of time
  - Any read or write automatically refresh a section
  - Special refresh cycle (i.e. hidden refresh or cycle stealing)
- Often works with DRAM controller

Internal Structure of DRAM

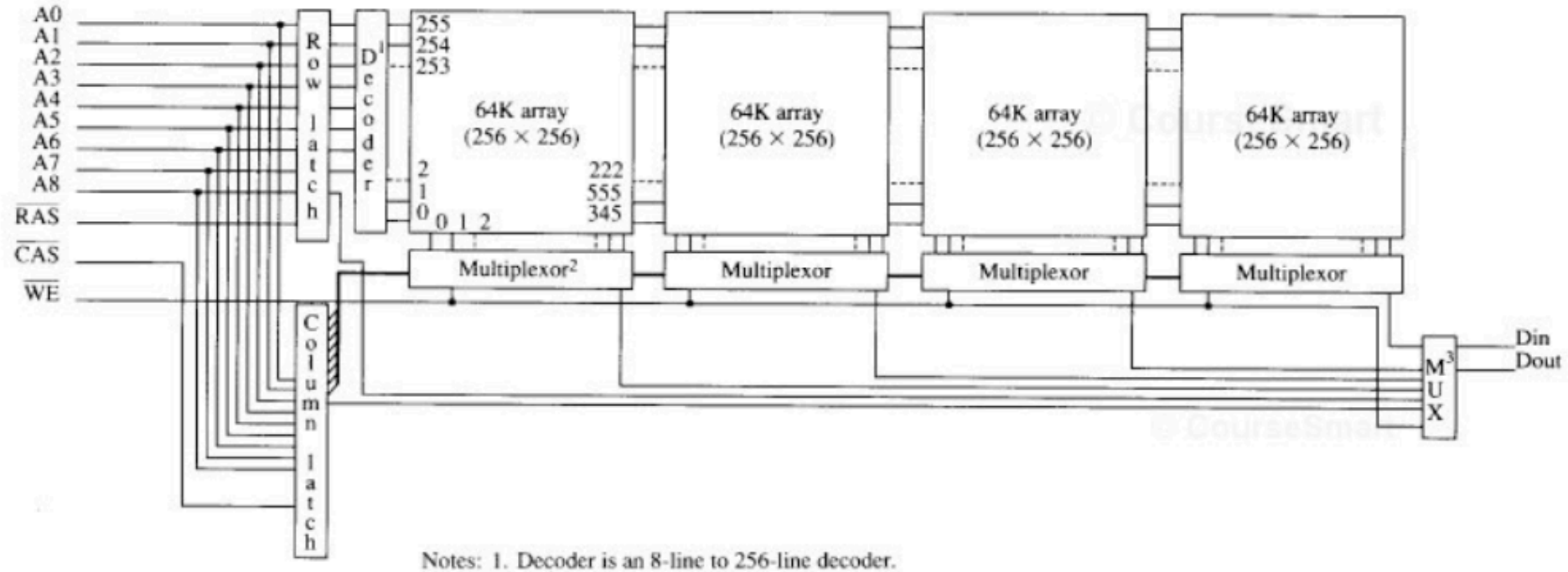


FIGURE 10–39 The internal structure of a 256K × 1 DRAM. Note that each of the internal 256 words are 1024 bits wide.

Refreshing DRAM

- Refresh counter supplies a refresh address
  - Counter size determined by type of DRAM
  - Increment counter after every refresh
  - E.g. 256 rows in 4ms -> one row per 15.6us. Assuming a 5MHz 8088 processor, 800ns per read. So every 19 memory read or write, the memory needs to run a refresh cycle. About 5% performance loss for 8088.

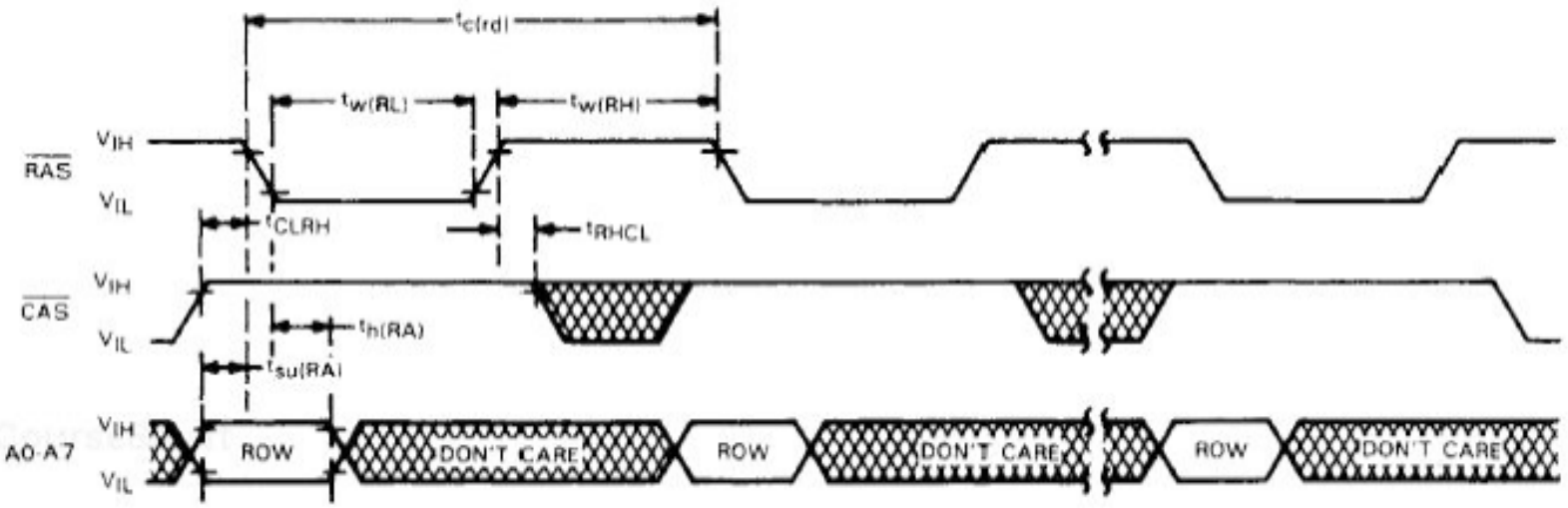


FIGURE 10–40 The timing diagram of the $\overline{\text{RAS}}$ refresh cycle for the TMS4464 DRAM. (Courtesy of Texas Instruments Corporation.)

SDRAM, DDR, DRAM controller

- Burst reads
  - Reading the first 64-bit is as fast(slow) as standard DRAM, 4 bus cycles including a wait state
  - 2^{nd}, 3^{rd} and 4^{th} number can be read in one bus cycle each
  - Total 7 bus cycles for four 64-bit numbers vs 12 bus cycles for standard DRAM
- DDR
  - Transfer data on each edge of the clock
  - Doubles the transfer rate, but the access time still exists
- DRAM controller
  - Handle address multiplexing and signal generation
  - Often built into the processors.

Quiz

1. What types of connections are common to all memory devices?
2. List the number of words found in each memory device for the following numbers of address connections:
   (a) 8
   (b) 11
   (c) 12
   (d) 13
   (e) 20
3. List the number of data items stored in each of the following memory devices and the number of bits in each datum:
   (a) $2K \times 4$
   (b) $1K \times 1$
   (c) $4K \times 8$
   (d) $16K \times 1$
   (e) $64K \times 4$
4. What is the purpose of the $\overline{CS}$ or $\overline{CE}$ pin on a memory component?
5. What is the purpose of the $\overline{OE}$ pin on a memory device?
6. What is the purpose of the $\overline{WE}$ pin on a SRAM?