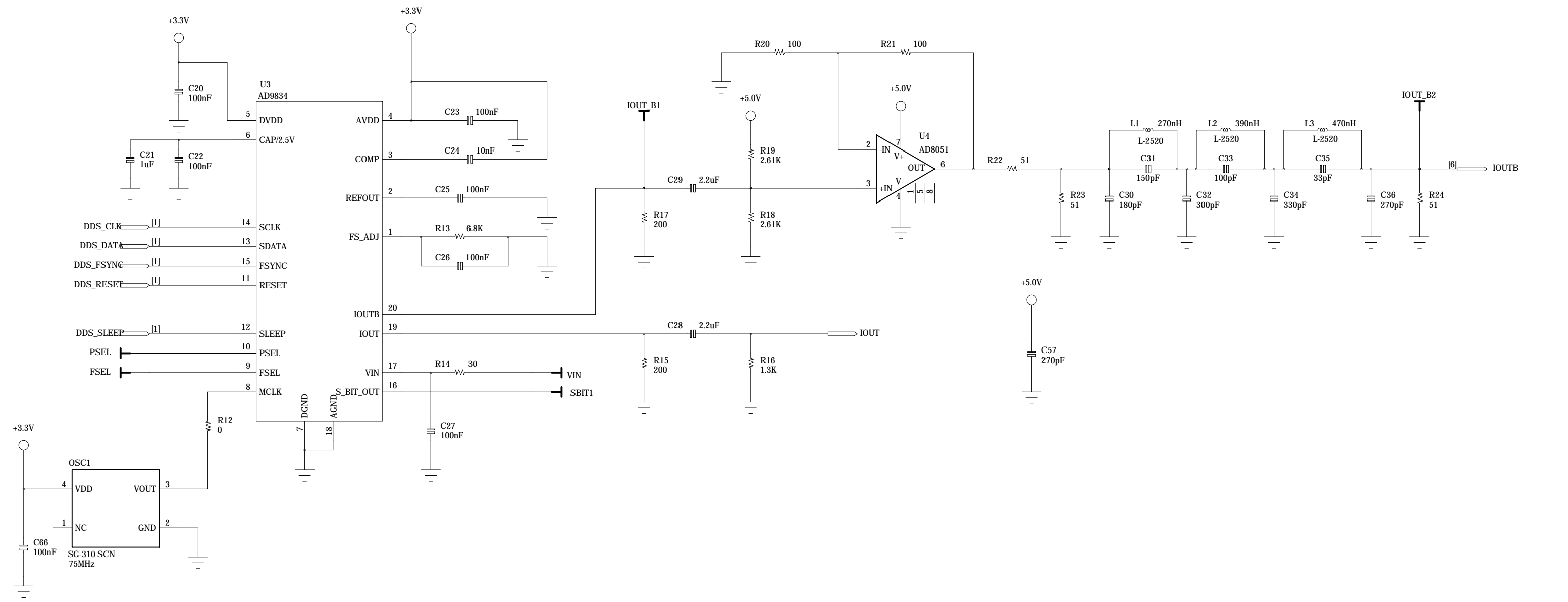
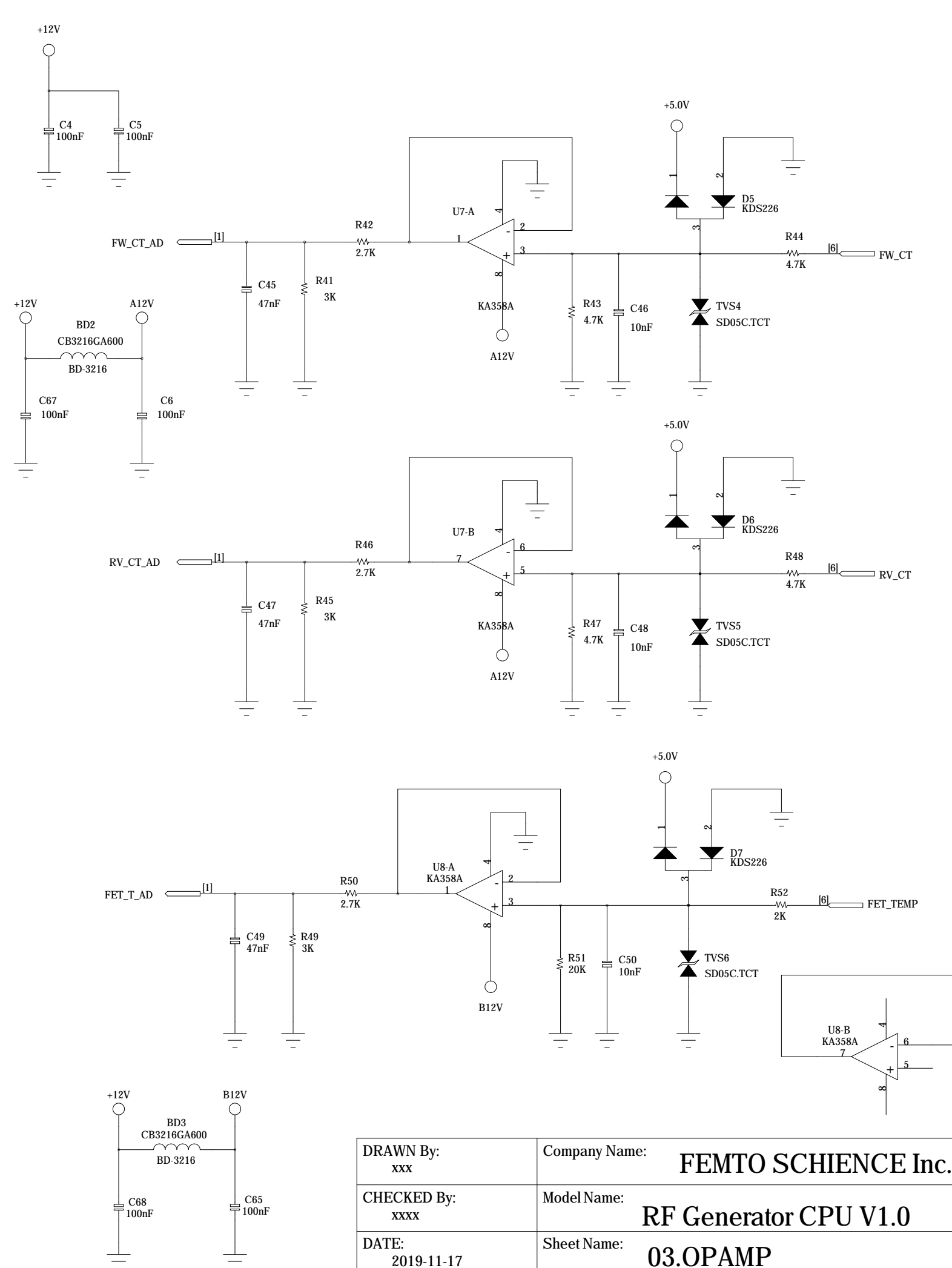
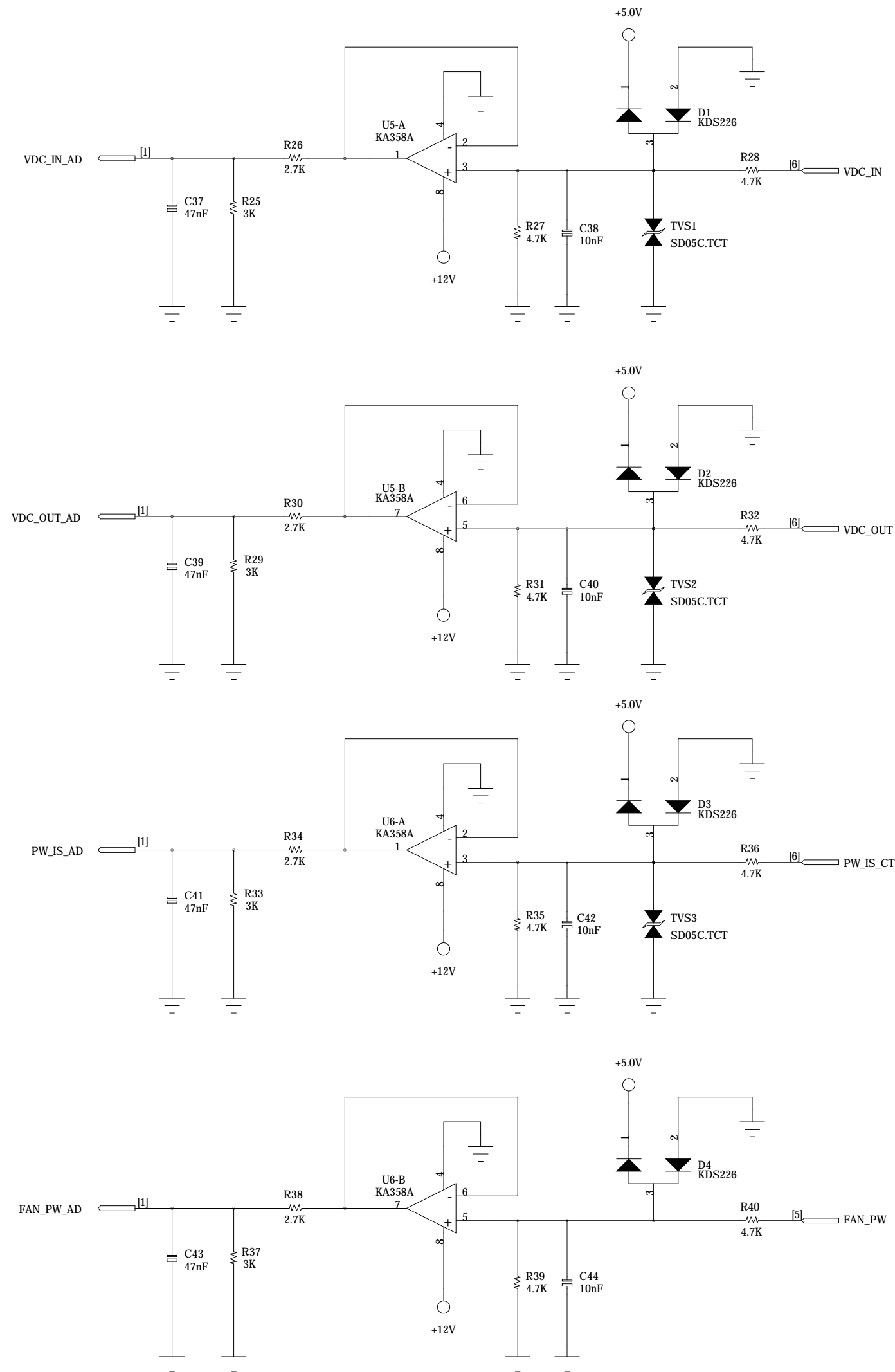


DRAWN By: xxx	Company Name: FEMTO SCHIENCE Inc.	
CHECKED By: xxxx	Model Name: RF Generator CPU V1.0	
DATE: 2019-11-17	Sheet Name: 01.MCU	
Revision:	TEAM: HW Team	PAGE: 1 / 6

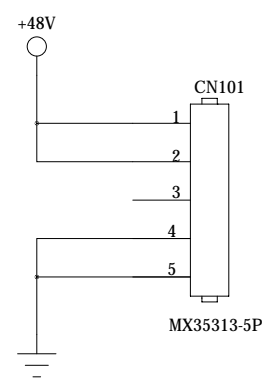


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DATE: 2019-11-17	Sheet Name: 02.DDS	
Revision:	TEAM: HW Team	PAGE: 2 / 6

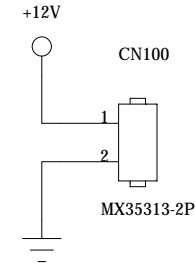


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DATE: 2019-11-17	Sheet Name: 03.OPAMP	
Revision:	TEAM: HW Team	PAGE: 3 / 6

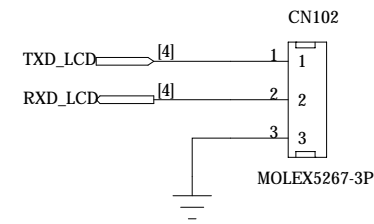
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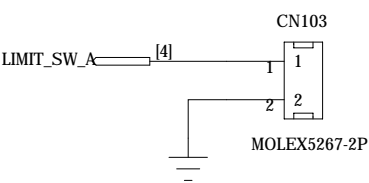
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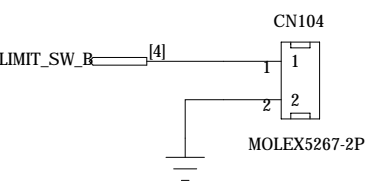
LCD Comm.



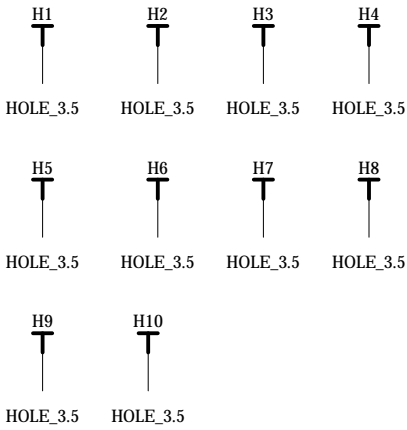
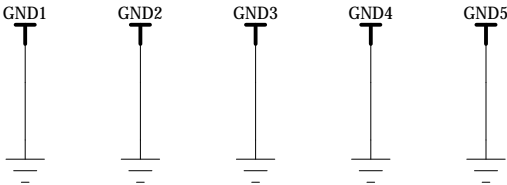
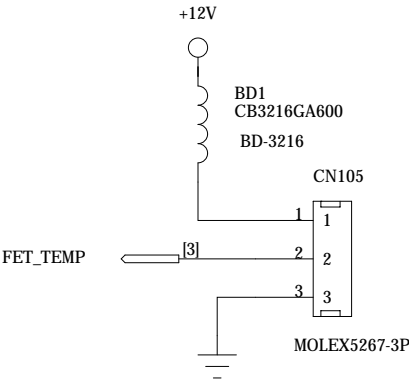
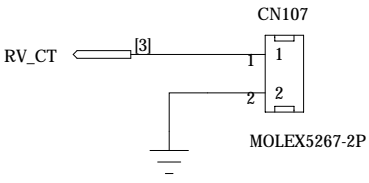
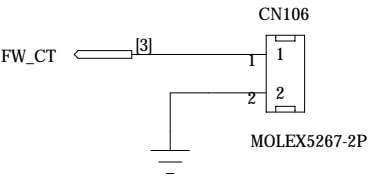
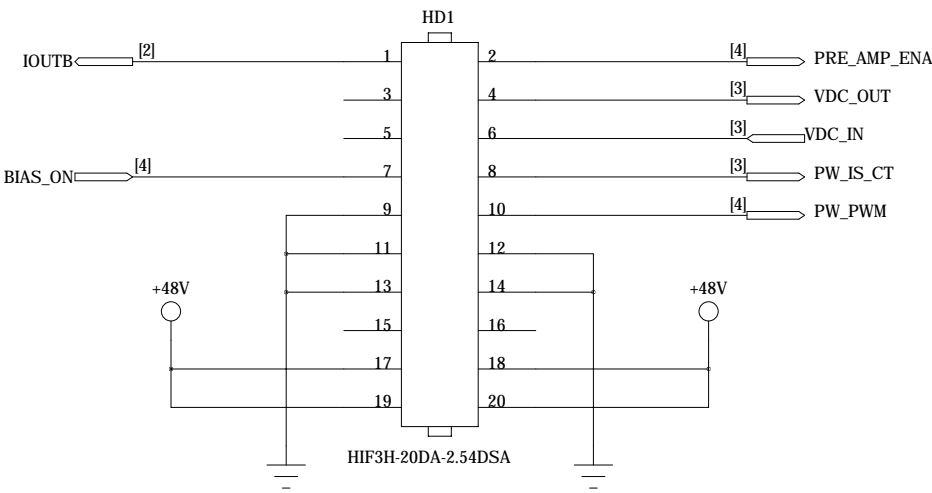
RF CON Limit S/W



Case Limit S/W



PWR PCB INTERFACE



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CHECKED By: xxxx	Model Name: RF Generator CPU V1.0	
DATE: 2019-11-17	Sheet Name: 06.CON	
Revision:	TEAM: HW Team	PAGE: 6 / 6