NOTE: This schematic needs to be viewed in color.

Text in BLUE are not net names. They are labels to reference the v6X PAB pinout.

REVISIONS				
Authority	Rev	Description	Date	Approved
ENGR	01	Initial Release	11/03/2022	DBS
ENGR	01	Delete C74, C90, C93 DCDC_DIG_1V0 0.1uF caps.	1/23/2023	DBS

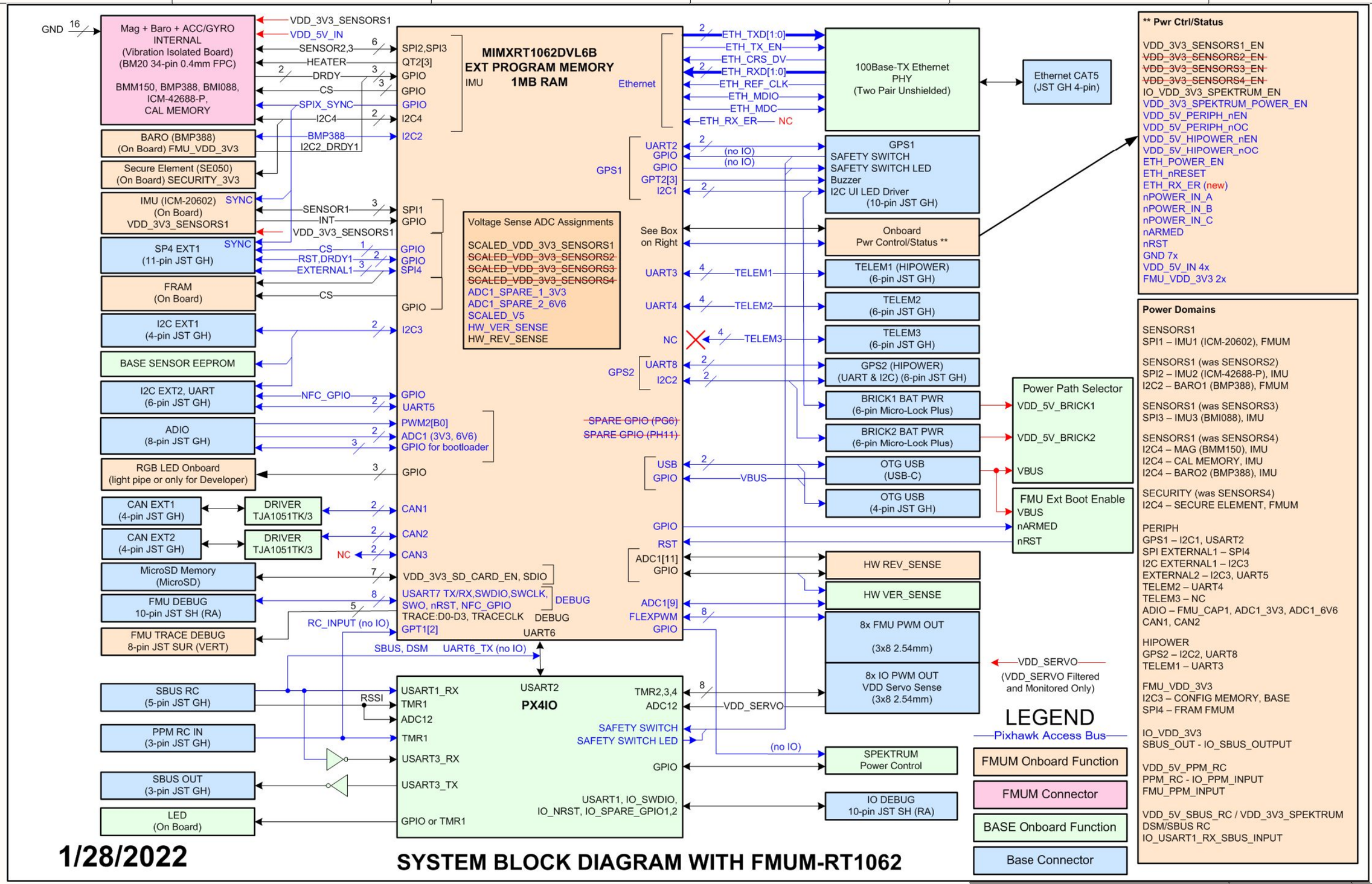
TABLE OF CONTENTS

NOTES, unless otherwise specified

- All Resistors 1%, 1/16 W
- All Capacitors are in micro Farads, +/- 10%, 50V

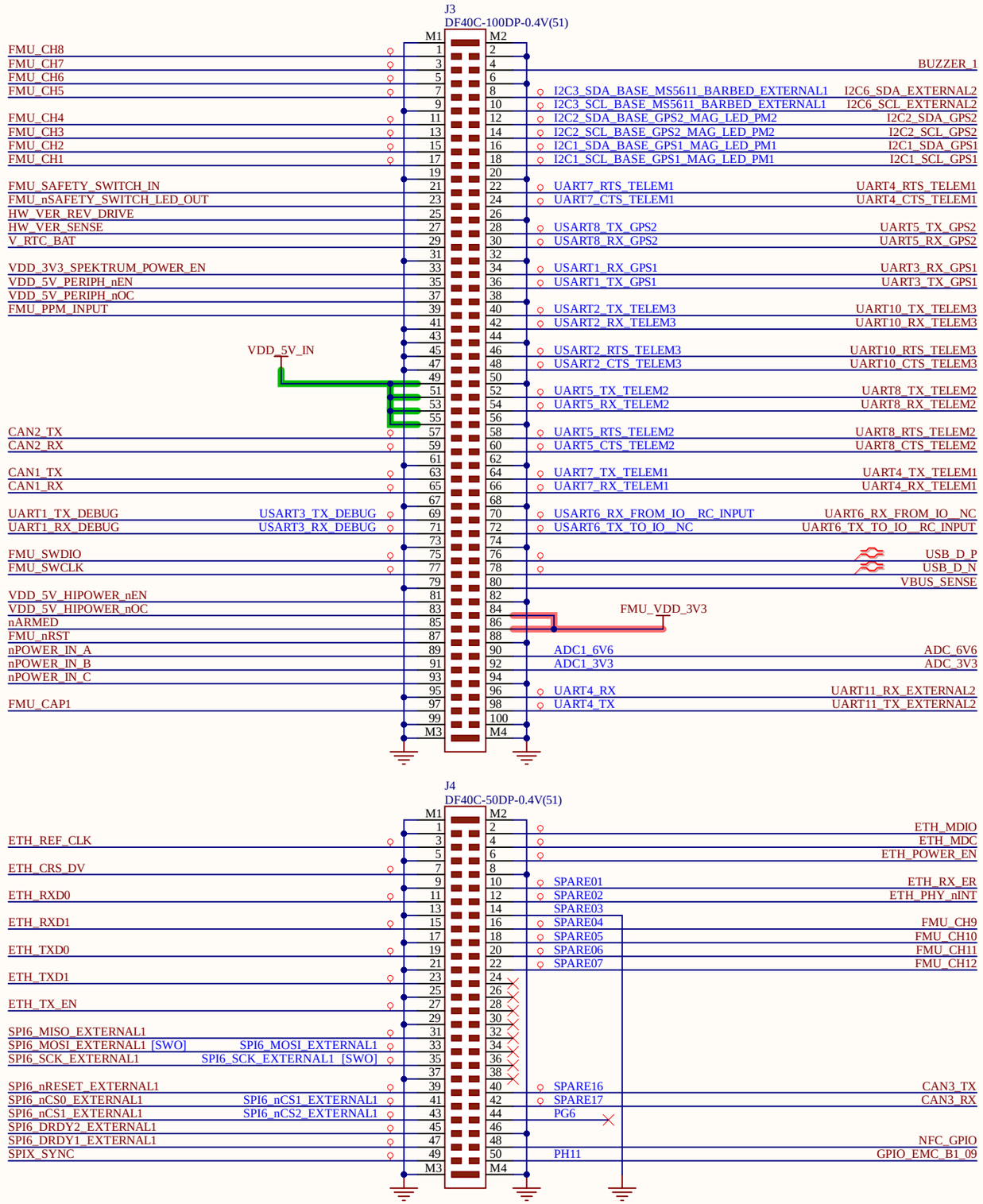
COVER SHEET

Title *FMUM-RT117X*			*6501 William Cannon Dr. West Austin, TX 78735-8598*
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 1 of 9		Checked: David Sidrane
File: 01_cover.SchDoc			



This block diagram needs to be updated

Title	*FMUM-RT117X*		6501 William Cannon Dr. West Austin, TX 78735-8598
Size: B	Number: 725002	Rev: 01	
Date: 1/23/23	Sheet 2 of 9		Author: Dugan Yoon
File: 02_block_diagram.SchDoc			Checked: David Sidrane

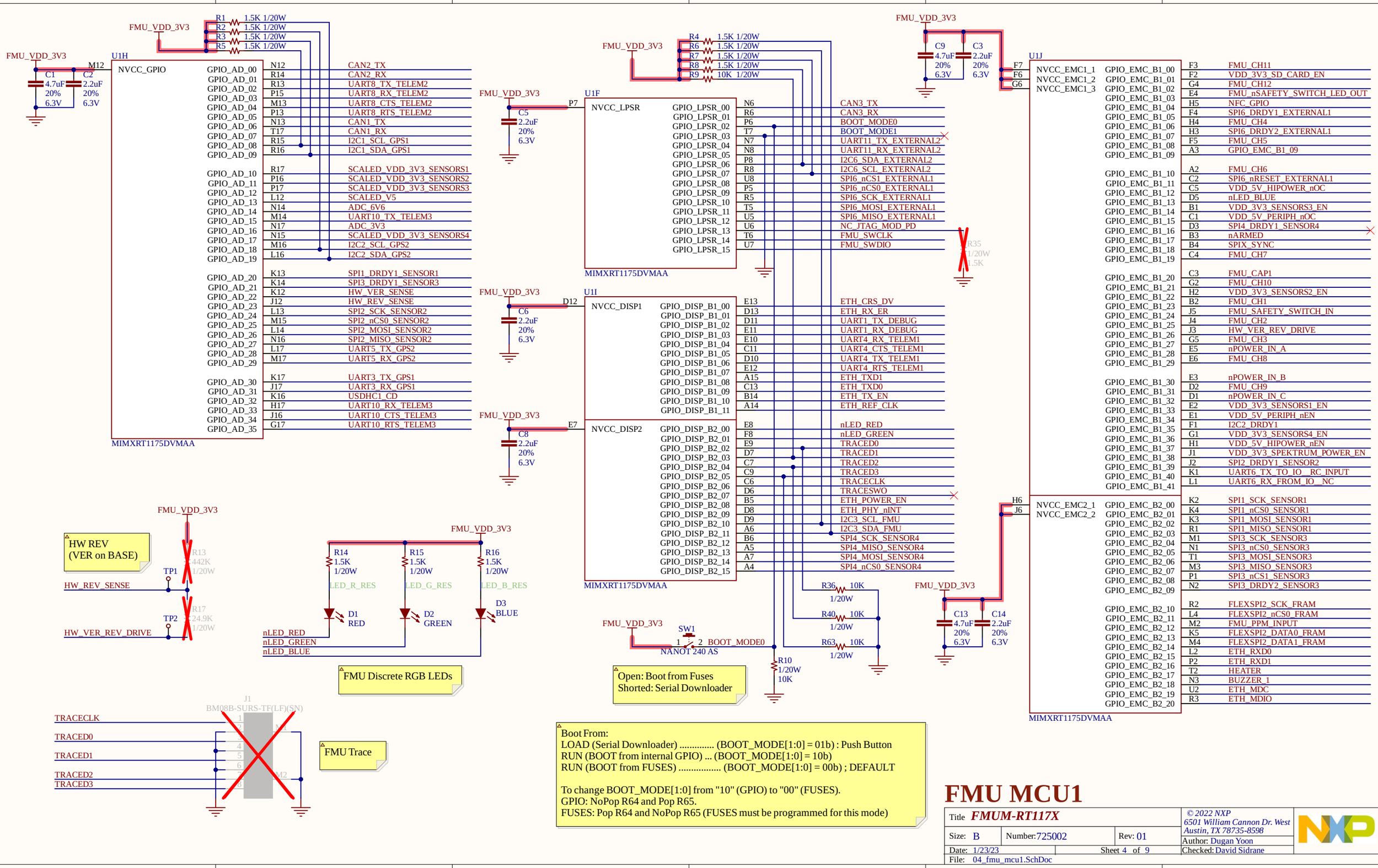


PIXHAWK AUTOPILOT BUS
Connectors to BASE

Text in BLUE are not net names.
They are labels to reference the v5X PAB pinout.

PIXHAWK AUTOPILOT BUS (PAB)

Title: *FMUM-RT117X*			*© 2022 NXP* *6501 William Cannon Dr. West Austin, TX 78735-8598*
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 3 of 9		Checked: David Sidrane
File: 03_PAB.SchDoc			


FMU_VDD_3V3
R1 1.5K 1/20W
R2 1.5K 1/20W
R3 1.5K 1/20W
R5 1.5K 1/20W
U1H
NVCC_GPIO
M12
C1 4.7uF 20% 6.3V
C2 2.2uF 20% 6.3V
GPIO_AD_00 N12 CAN2_TX
GPIO_AD_01 R14 CAN2_RX
GPIO_AD_02 R13 UART8_TX_TELEM2
GPIO_AD_03 P15 UART8_RX_TELEM2
GPIO_AD_04 M13 UART8_CTS_TELEM2
GPIO_AD_05 P13 UART8_RTS_TELEM2
GPIO_AD_06 N13 CAN1_TX
GPIO_AD_07 T17 CAN1_RX
GPIO_AD_08 R15 I2C1_SCL_GPS1
GPIO_AD_09 R16 I2C1_SDA_GPS1
GPIO_AD_10 R17 SCALED_VDD_3V3_SENSORS1
GPIO_AD_11 P16 SCALED_VDD_3V3_SENSORS2
GPIO_AD_12 P17 SCALED_VDD_3V3_SENSORS3
GPIO_AD_13 L12 SCALED_V5
GPIO_AD_14 N14 ADC_6V6
GPIO_AD_15 M14 UART10_TX_TELEM3
GPIO_AD_16 N17 ADC_3V3
GPIO_AD_17 N15 SCALED_VDD_3V3_SENSORS4
GPIO_AD_18 M16 I2C2_SCL_GPS2
GPIO_AD_19 L16 I2C2_SDA_GPS2
GPIO_AD_20 K13 SPI1_DRDY1_SENSOR1
GPIO_AD_21 K14 SPI3_DRDY1_SENSOR3
GPIO_AD_22 K12 HW_VER_SENSE
GPIO_AD_23 J12 HW_REV_SENSE
GPIO_AD_24 L13 SPI2_SCK_SENSOR2
GPIO_AD_25 M15 SPI2_nCS0_SENSOR2
GPIO_AD_26 L14 SPI2_MOSI_SENSOR2
GPIO_AD_27 N16 SPI2_MISO_SENSOR2
GPIO_AD_28 L17 UART5_TX_GPS2
GPIO_AD_29 M17 UART5_RX_GPS2
GPIO_AD_30 K17 UART3_TX_GPS1
GPIO_AD_31 J17 UART3_RX_GPS1
GPIO_AD_32 K16 USDHC1_CD
GPIO_AD_33 H17 UART10_RX_TELEM3
GPIO_AD_34 J16 UART10_CTS_TELEM3
GPIO_AD_35 G17 UART10_RTS_TELEM3
MIMXRT1175DVMAA
FMU_VDD_3V3
R4 1.5K 1/20W
R6 1.5K 1/20W
R7 1.5K 1/20W
R8 1.5K 1/20W
R9 10K 1/20W
U1F
NVCC_LPSR
P7
C5 2.2uF 20% 6.3V
GPIO_LPSR_00 N6 CAN3_TX
GPIO_LPSR_01 R6 CAN3_RX
GPIO_LPSR_02 P6 BOOT_MODE0
GPIO_LPSR_03 T7 BOOT_MODE1
GPIO_LPSR_04 N7 UART11_TX_EXTERNAL2
GPIO_LPSR_05 N8 UART11_RX_EXTERNAL2
GPIO_LPSR_06 P8 I2C6_SDA_EXTERNAL2
GPIO_LPSR_07 R8 I2C6_SCL_EXTERNAL2
GPIO_LPSR_08 U8 SPI6_nCS1_EXTERNAL1
GPIO_LPSR_09 P5 SPI6_nCS0_EXTERNAL1
GPIO_LPSR_10 R5 SPI6_SCK_EXTERNAL1
GPIO_LPSR_11 T5 SPI6_MOSI_EXTERNAL1
GPIO_LPSR_12 U5 SPI6_MISO_EXTERNAL1
GPIO_LPSR_13 U6 NC_JTAG_MOD_PD
GPIO_LPSR_14 T6 FMU_SWCLK
GPIO_LPSR_15 U7 FMU_SWDIO
MIMXRT1175DVMAA
R35 1/20W 1.5K
U1I
NVCC_DISP1
D12
C6 2.2uF 20% 6.3V
GPIO_DISP_B1_00 E13 ETH_CRS_DV
GPIO_DISP_B1_01 D13 ETH_RX_ER
GPIO_DISP_B1_02 D11 UART1_TX_DEBUG
GPIO_DISP_B1_03 E11 UART1_RX_DEBUG
GPIO_DISP_B1_04 E10 UART4_RX_TELEM1
GPIO_DISP_B1_05 C11 UART4_CTS_TELEM1
GPIO_DISP_B1_06 D10 UART4_TX_TELEM1
GPIO_DISP_B1_07 E12 UART4_RTS_TELEM1
GPIO_DISP_B1_08 A15 ETH_TXD1
GPIO_DISP_B1_09 C13 ETH_TXD0
GPIO_DISP_B1_10 B14 ETH_TX_EN
GPIO_DISP_B1_11 A14 ETH_REF_CLK
NVCC_DISP2
E7
C8 2.2uF 20% 6.3V
GPIO_DISP_B2_00 E8 nLED_RED
GPIO_DISP_B2_01 F8 nLED_GREEN
GPIO_DISP_B2_02 E9 TRACED0
GPIO_DISP_B2_03 D7 TRACED1
GPIO_DISP_B2_04 C7 TRACED2
GPIO_DISP_B2_05 C9 TRACED3
GPIO_DISP_B2_06 C6 TRACECLK
GPIO_DISP_B2_07 D6 TRACESWO
GPIO_DISP_B2_08 B5 ETH_POWER_EN
GPIO_DISP_B2_09 D8 ETH_PHY_nINT
GPIO_DISP_B2_10 D9 I2C3_SCL_FMU
GPIO_DISP_B2_11 A6 I2C3_SDA_FMU
GPIO_DISP_B2_12 B6 SPI4_SCK_SENSOR4
GPIO_DISP_B2_13 A5 SPI4_MISO_SENSOR4
GPIO_DISP_B2_14 A7 SPI4_MOSI_SENSOR4
GPIO_DISP_B2_15 A4 SPI4_nCS0_SENSOR4
MIMXRT1175DVMAA
FMU_VDD_3V3
C9 4.7uF 20% 6.3V
C3 2.2uF 20% 6.3V
F7
F6
G6
U1J
NVCC_EMC1_1
NVCC_EMC1_2
NVCC_EMC1_3
GPIO_EMC_B1_00 F3 FMU_CH11
GPIO_EMC_B1_01 F2 VDD_3V3_SD_CARD_EN
GPIO_EMC_B1_02 G4 FMU_CH12
GPIO_EMC_B1_03 E4 FMU_nSAFETY_SWITCH_LED_OUT
GPIO_EMC_B1_04 H5 NFC_GPIO
GPIO_EMC_B1_05 F4 SPI6_DRDY1_EXTERNAL1
GPIO_EMC_B1_06 H4 FMU_CH4
GPIO_EMC_B1_07 H3 SPI6_DRDY2_EXTERNAL1
GPIO_EMC_B1_08 F5 FMU_CH5
GPIO_EMC_B1_09 A3 GPIO_EMC_B1_09
GPIO_EMC_B1_10 A2 FMU_CH6
GPIO_EMC_B1_11 C2 SPI6_nRESET_EXTERNAL1
GPIO_EMC_B1_12 C5 VDD_5V_HIPOWER_nOC
GPIO_EMC_B1_13 D5 nLED_BLUE
GPIO_EMC_B1_14 B1 VDD_3V3_SENSORS3_EN
GPIO_EMC_B1_15 C1 VDD_5V_PERIPH_nOC
GPIO_EMC_B1_16 D3 SPI4_DRDY1_SENSOR4
GPIO_EMC_B1_17 B3 nARMED
GPIO_EMC_B1_18 B4 SPIX_SYNC
GPIO_EMC_B1_19 C4 FMU_CH7
GPIO_EMC_B1_20 C3 FMU_CAP1
GPIO_EMC_B1_21 G2 FMU_CH10
GPIO_EMC_B1_22 H2 VDD_3V3_SENSORS2_EN
GPIO_EMC_B1_23 B2 FMU_CH1
GPIO_EMC_B1_24 J5 FMU_SAFETY_SWITCH_IN
GPIO_EMC_B1_25 J4 FMU_CH2
GPIO_EMC_B1_26 J3 HW_VER_REV_DRIVE
GPIO_EMC_B1_27 G5 FMU_CH3
GPIO_EMC_B1_28 E5 nPOWER_IN_A
GPIO_EMC_B1_29 E6 FMU_CH8
GPIO_EMC_B1_30 E3 nPOWER_IN_B
GPIO_EMC_B1_31 D2 FMU_CH9
GPIO_EMC_B1_32 D1 nPOWER_IN_C
GPIO_EMC_B1_33 E2 VDD_3V3_SENSORS1_EN
GPIO_EMC_B1_34 E1 VDD_5V_PERIPH_nEN
GPIO_EMC_B1_35 F1 I2C2_DRDY1
GPIO_EMC_B1_36 G1 VDD_3V3_SENSORS4_EN
GPIO_EMC_B1_37 H1 VDD_5V_HIPOWER_nEN
GPIO_EMC_B1_38 J1 VDD_3V3_SPEKTRUM_POWER_EN
GPIO_EMC_B1_39 J2 SPI2_DRDY1_SENSOR2
GPIO_EMC_B1_40 K1 UART6_TX_TO_IO__RC_INPUT
GPIO_EMC_B1_41 L1 UART6_RX_FROM_IO__NC
H6
J6
NVCC_EMC2_1
NVCC_EMC2_2
GPIO_EMC_B2_00 K2 SPI1_SCK_SENSOR1
GPIO_EMC_B2_01 K4 SPI1_nCS0_SENSOR1
GPIO_EMC_B2_02 K3 SPI1_MOSI_SENSOR1
GPIO_EMC_B2_03 R1 SPI1_MISO_SENSOR1
GPIO_EMC_B2_04 M1 SPI3_SCK_SENSOR3
GPIO_EMC_B2_05 N1 SPI3_nCS0_SENSOR3
GPIO_EMC_B2_06 T1 SPI3_MOSI_SENSOR3
GPIO_EMC_B2_07 M3 SPI3_MISO_SENSOR3
GPIO_EMC_B2_08 P1 SPI3_nCS1_SENSOR3
GPIO_EMC_B2_09 N2 SPI3_DRDY2_SENSOR3
GPIO_EMC_B2_10 R2 FLEXSPI2_SCK_FRAM
GPIO_EMC_B2_11 L4 FLEXSPI2_nCS0_FRAM
GPIO_EMC_B2_12 M2 FMU_PPM_INPUT
GPIO_EMC_B2_13 K5 FLEXSPI2_DATA0_FRAM
GPIO_EMC_B2_14 M4 FLEXSPI2_DATA1_FRAM
GPIO_EMC_B2_15 L2 ETH_RXD0
GPIO_EMC_B2_16 P2 ETH_RXD1
GPIO_EMC_B2_17 T2 HEATER
GPIO_EMC_B2_18 N3 BUZZER_1
GPIO_EMC_B2_19 U2 ETH_MDC
GPIO_EMC_B2_20 R3 ETH_MDIO
MIMXRT1175DVMAA
FMU_VDD_3V3
C13 4.7uF 20% 6.3V
C14 2.2uF 20% 6.3V
R36 10K 1/20W
R40 10K 1/20W
R63 10K 1/20W
R10 1/20W 10K
FMU_VDD_3V3
SW1
1 2 BOOT_MODE0
NANO1 240 AS
Open: Boot from Fuses
Shorted: Serial Downloader
FMU_VDD_3V3
HW REV
(VER on BASE)
R13 3.442K 1/20W
R17 24.9K 1/20W
TP1
TP2
HW_REV_SENSE
HW_VER_REV_DRIVE
FMU_VDD_3V3
R14 1.5K 1/20W
R15 1.5K 1/20W
R16 1.5K 1/20W
LED_R_RES
LED_G_RES
LED_B_RES
D1 RED
D2 GREEN
D3 BLUE
nLED_RED
nLED_GREEN
nLED_BLUE
FMU Discrete RGB LEDs
J1
BM08B-SURS-TF(LF)(SN)
TRACECLK
TRACED0
TRACED1
TRACED2
TRACED3
FMU Trace
Boot From:
LOAD (Serial Downloader) ..... (BOOT_MODE[1:0] = 01b) : Push Button
RUN (BOOT from internal GPIO) ... (BOOT_MODE[1:0] = 10b)
RUN (BOOT from FUSES) ..... (BOOT_MODE[1:0] = 00b) ; DEFAULT
To change BOOT_MODE[1:0] from "10" (GPIO) to "00" (FUSES).
GPIO: NoPop R64 and Pop R65.
FUSES: Pop R64 and NoPop R65 (FUSES must be programmed for this mode)
FMU MCU1
Title FMUM-RT117X
Size: B
Number:725002
Rev: 01
Date: 1/23/23
Sheet 4 of 9
File: 04_fmu_mcu1.SchDoc
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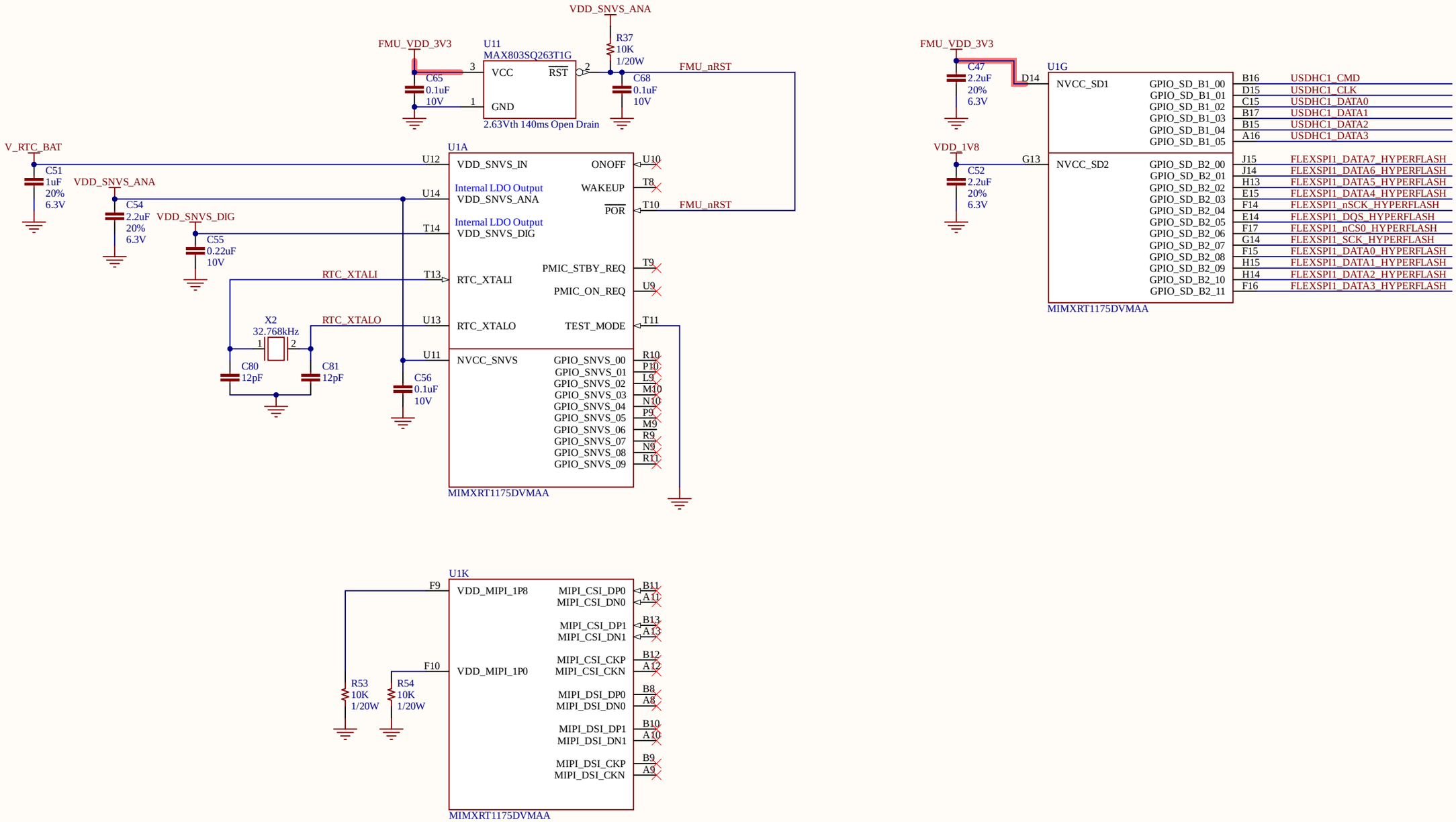
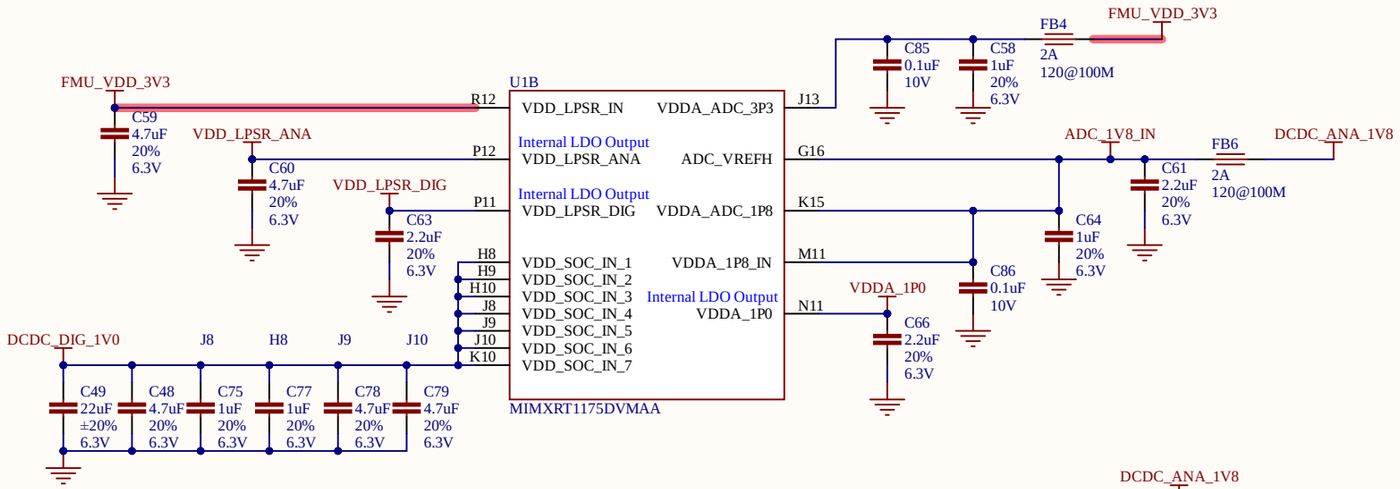
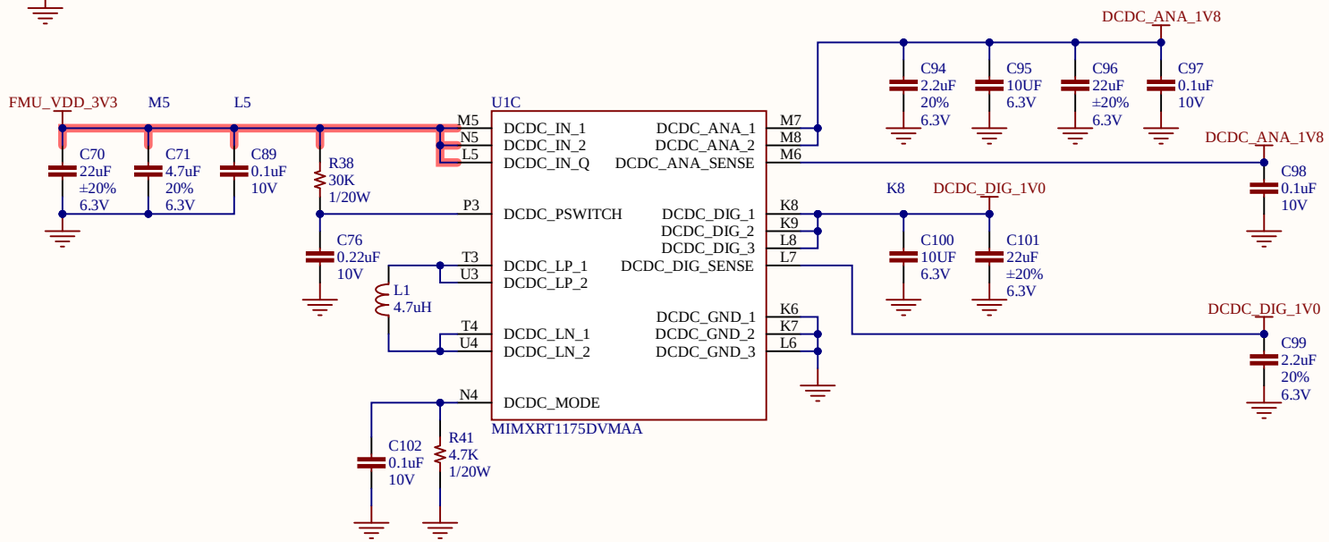
Austin, TX 78735-8598
Author: Dugan Yoon
Checked: David Sidrane

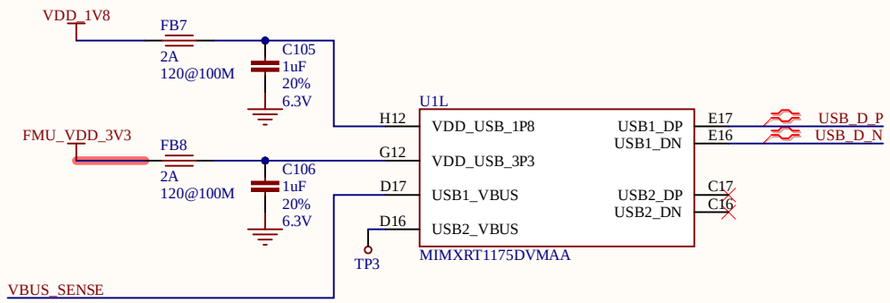


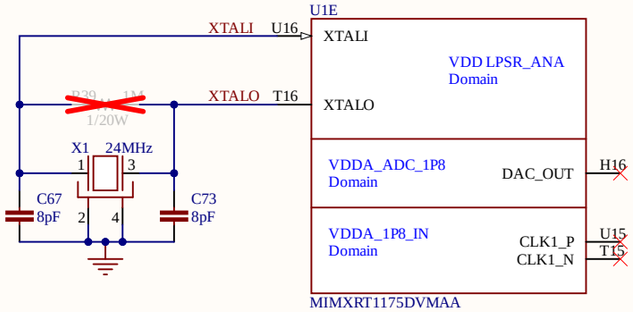
FMU MCU2

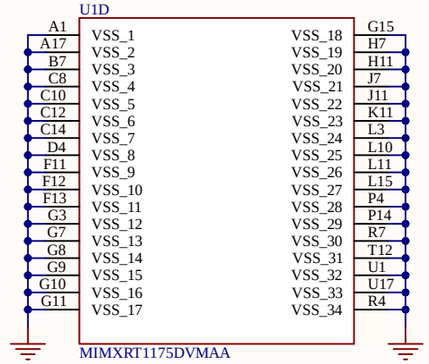
Title	*FMUM-RT117X*		*© 2022 NXP 6501 William Cannon Dr. West Austin, TX 78735-8598*
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 5 of 9		Checked: David Sidrane
File: 05_fmu_mcu2.SchDoc			







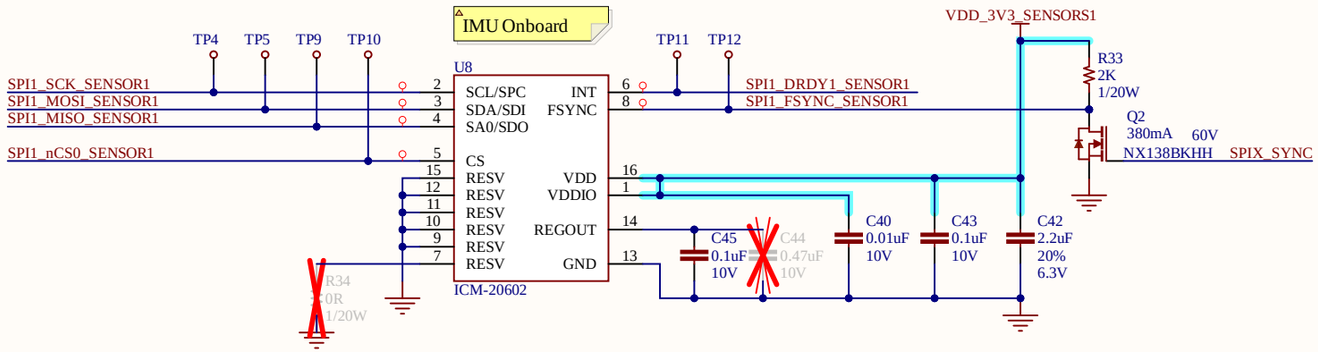


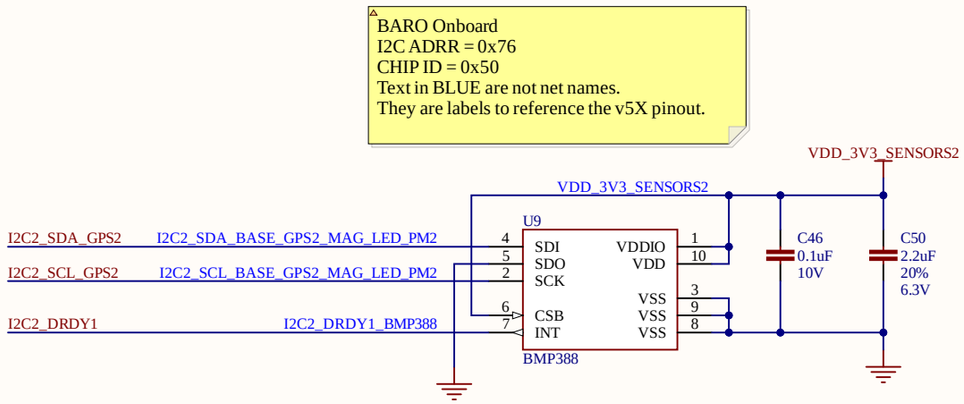


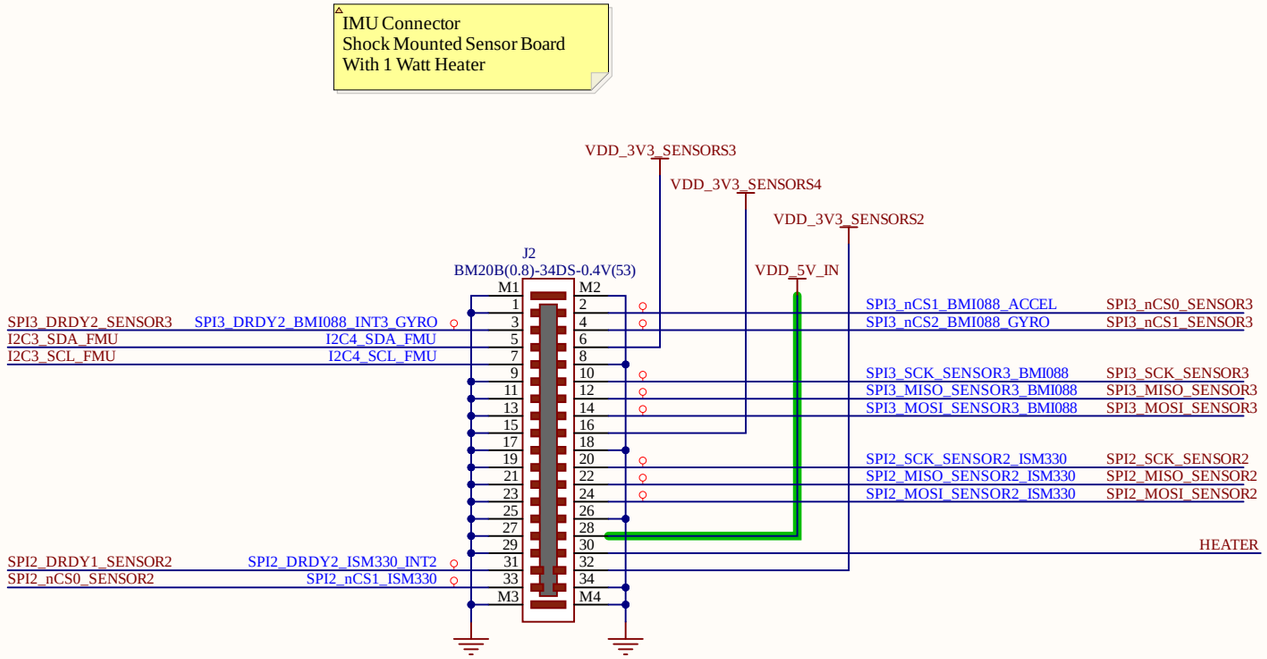
FUNCTION	FUSES	S
xSPI FLASH AUTO PROBE	BOOT_CFG1[0]	1
ENCRYPTED XIP (0 Disable)	BOOT_CFG1[1]	0
xSPI FLASH HOLD TIME	BOOT_CFG1[2]	0
	BOOT_CFG1[3]	0
Serial NOR boot via FlexSPI	BOOT_CFG1[4]	0
	BOOT_CFG1[5]	0
	BOOT_CFG1[6]	0
	BOOT_CFG1[7]	0
FLASH TYPE 010 - 1.8V HYPERFLASH	BOOT_CFG2[8]	0
	BOOT_CFG2[9]	1
	BOOT_CFG2[10]	0
Infinite-Loop (0 Disable)	BOOT_CFG2[11]	0

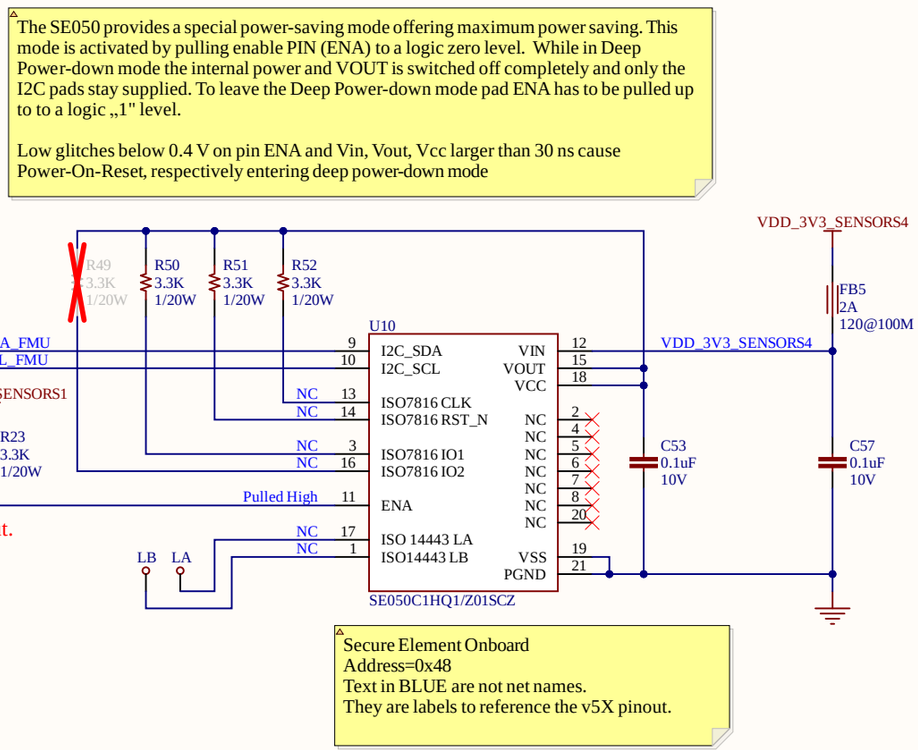
FMU MCU3

Title	*FMUM-RT117X*		*© 2022 NXP* *6501 William Cannon Dr. West* *Austin, TX 78735-8598*
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 6 of 9		Checked: David Sidrane
File: 06_fmu_mcu3.SchDoc			









Sensor Interfaces

Text in BLUE are not net names.
They are labels to reference the v5X pinout.

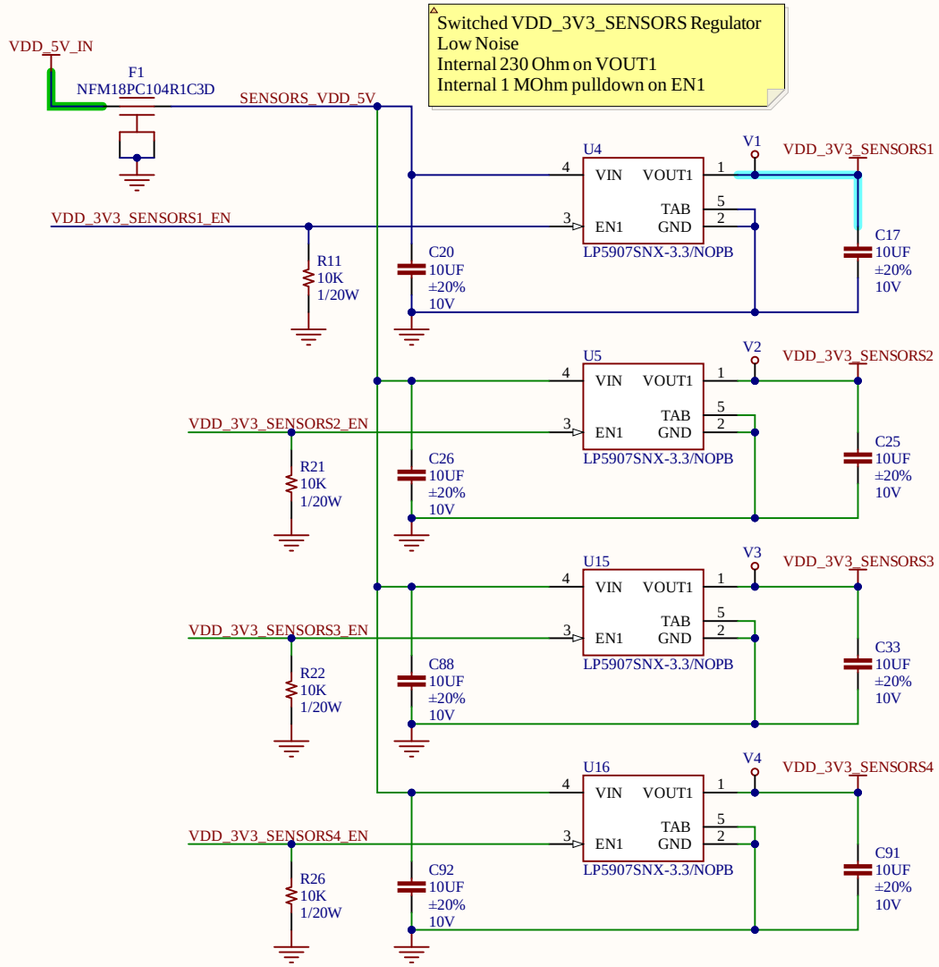
Secure Element Onboard
Address=0x48
Text in BLUE are not net names.
They are labels to reference the v5X pinout.

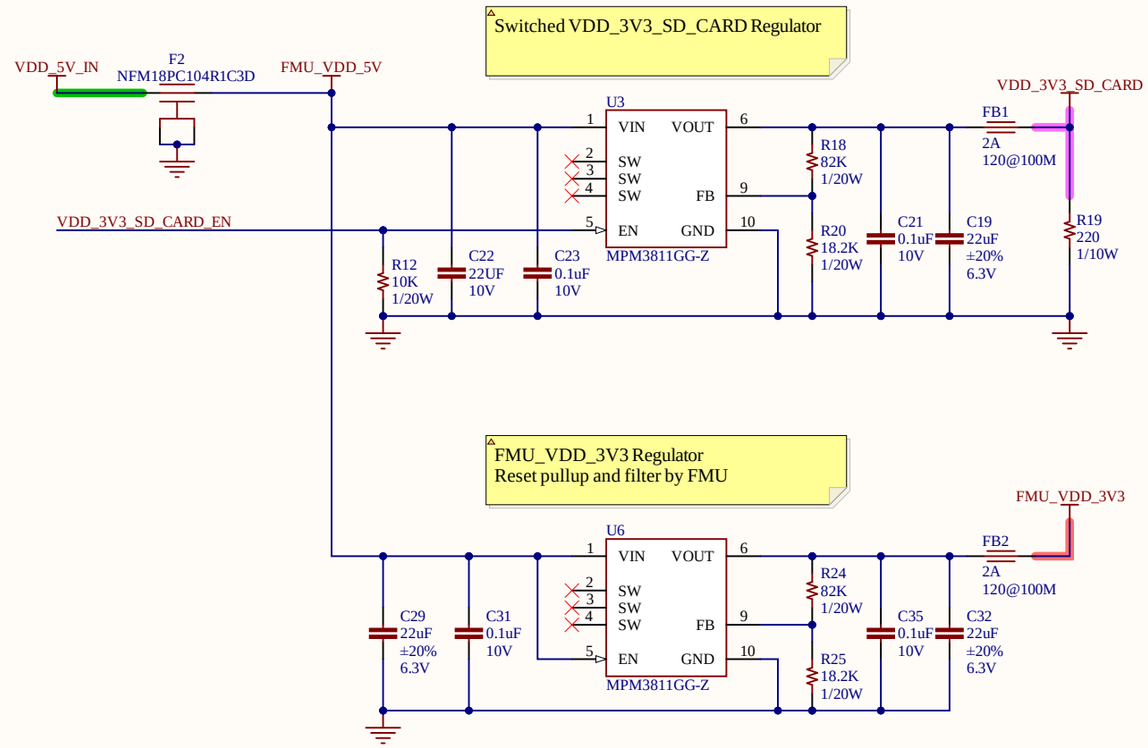
To enable SE050 drive HW_VER_REV_DRIVE low.

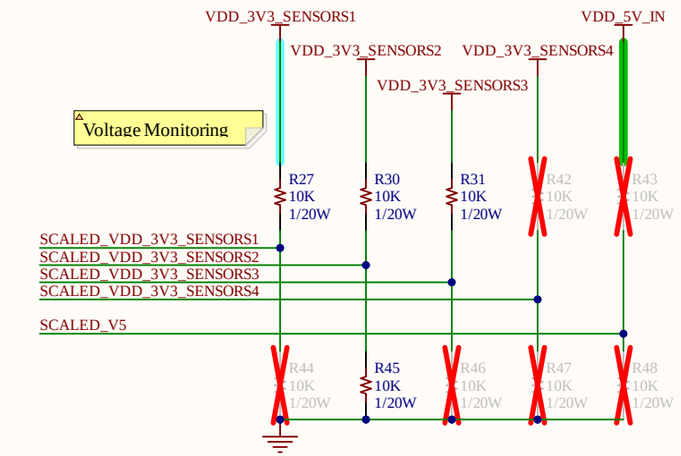
Power on sequence:
1) Drive I2C4 lines to output low (avoid backfeeding SE050)
2) Do HW versioning with VDD_3V3_SENSORS1 off which will leave HW_VER_REV_DRIVE high (SE050 disabled).
3) Then set HW_VER_REV_DRIVE low (SE050 enabled).
4) Then power on VDD_3V3_SENSORS1.
5) HW_VER_REV_DRIVE can be used to toggle SE050_ENA later if needed.

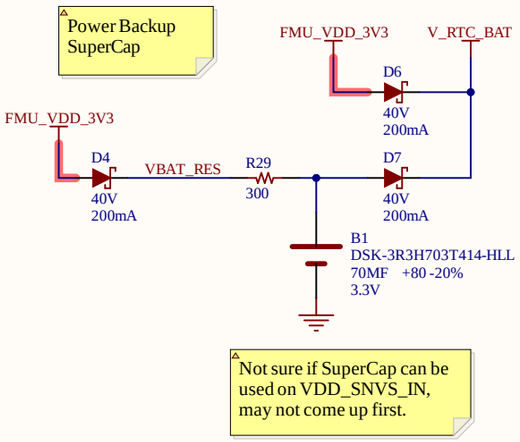
SENSORS

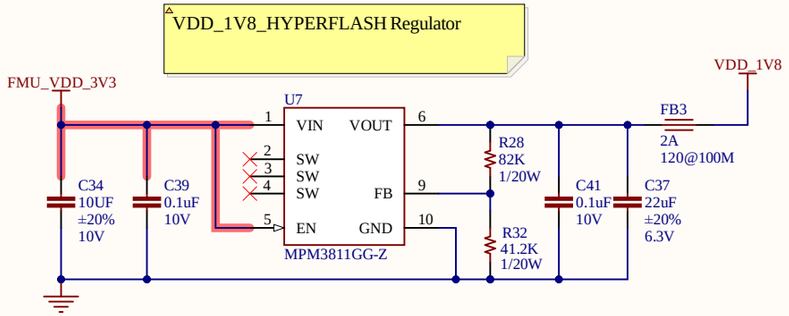
Title	*FMUM-RT117X*		6501 William Cannon Dr. West Austin, TX 78735-8598
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 7 of 9		Checked: David Sidrane
File: 07_sensors.SchDoc			





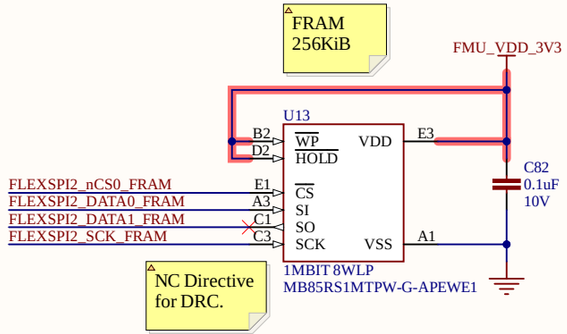


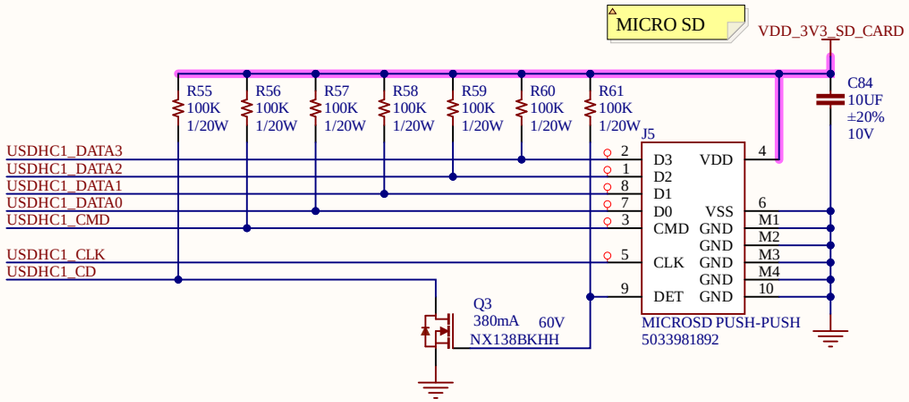


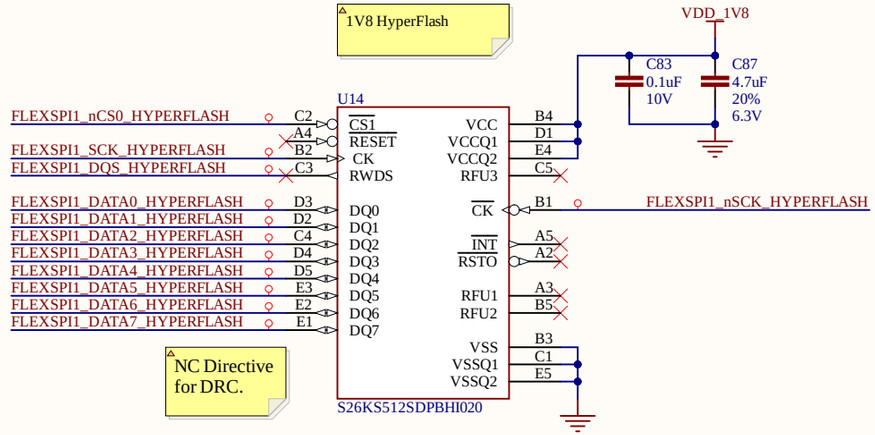


POWER

Title	*FMUM-RT117X*		*© 2022 NXP 6501 William Cannon Dr. West Austin, TX 78735-8598*
Size: B	Number: 725002	Rev: 01	Author: Dugan Yoon
Date: 1/23/23	Sheet 8 of 9		Checked: David Sidrane
File: 08_power.SchDoc			







MEMORY

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