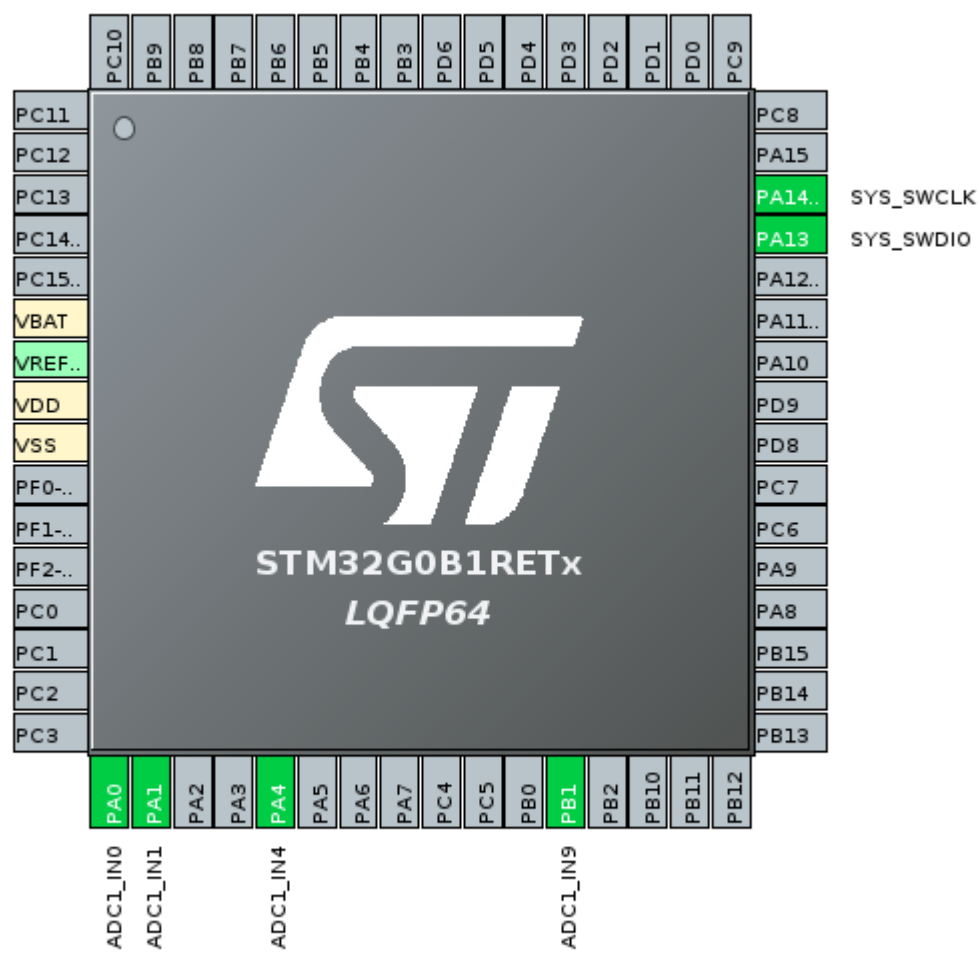
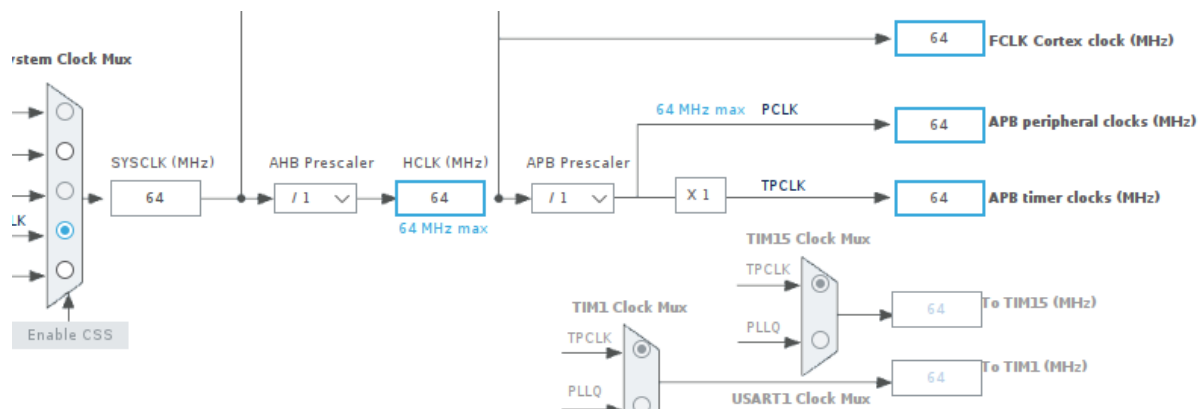


Configurando o DMA

Microcontroladores

Exemplo do professor - Pablo





main.c

MX configuracao-dma.ioc

Pinout & Configuration

Clock Configuration

Software Packs

Pinout

ADC1 Mode and Configuration

Configuration

Reset Configuration

NVIC Settings

DMA Settings

GPIO Settings

Parameter Settings

User Constants

NVIC Interrupt Table	Enabl...	Preemption Prior...
DMA1 channel 1 interrupt	<input checked="" type="checkbox"/>	0
ADC1, COMP1,COMP2, COMP3 Interrupts (combined with EXTI 17 &...	<input checked="" type="checkbox"/>	0

Categories

A->Z

System Core

Analog

ADC1

COMP1

COMP2

COMP3

DAC1

Timers

Connectivity

Multimedia

Computing

Middleware

Utilities

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User Constants

DMA Request	Channel	Direction	Priority
C1	DMA1 Channel 1	Peripheral To Memory	Low

Add

Delete

MA Request Settings

ModeCircular

Increment Address

Peripheral

Memory

Data Width

Half Word

Half Word

enable synchronization

synchronization signal

signal polarity

enable event

request number

main.c

MX*configuracao-dma.ioc

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>

Computing

>

ADC1 Mode and Configuration

Mode

☒ IN0

☒ IN1

☐ IN2

☐ IN3

☒ IN4

☐ IN5

☐ IN6

☐ IN7

☐ IN8

☒ IN9

☐ IN10

☐ IN11

☐ IN15

main.c

*configuracao-dma.ioc

Pinout & Configuration

Clock Configuration

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User Constants

Search (Ctrl+F)

Data Alignment

Sequencer

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

DMA Continuous Requests

End Of Conversion Selection

Overrun behaviour

Low Power Auto Wait

Auto Off

Oversampling Mode

ADC_Regular_ConversionMode

SamplingTime Common 1

SamplingTime Common 2

Number Of Conversion

External Trigger Conversion Source

External Trigger Conversion Edge

Trigger Frequency

Rank

Channel

Sampling Time

Rank

Channel

Sampling Time

Rank

Channel

Sampling Time

Rank

Channel

Sampling Time

Analog Watchdog 1

Enable Analog WatchDog1 Mode

Analog Watchdog 2

Right alignment

Sequencer set to fully configurable

Enabled

Enabled

Disabled

Enabled

End of single conversion

Overrun data preserved

Disabled

Disabled

Disabled

79.5 Cycles

79.5 Cycles

4

Regular Conversion launched by software

None

High frequency

1

Channel 0

Sampling time common 1

2

Channel 1

Sampling time common 1

3

Channel 4

Sampling time common 1

4

Channel 9

Sampling time common 1

Faz a parada do ciclo (uma interrupção):

DMA Continuous Requests

Enabled

End Of Conversion Selection

End of single conversion

Overrun behaviour

End of single conversion

Low Power Auto Wait

End of sequence of conversion

Auto Off

Disabled