

Title: Construct full adder using two half adders

Aim: Construct a full adder using two half adders using the kits available in the lab.

Resources needed: Logic experimentation kits

Theory:

Half Adder

This circuit needs two binary inputs and two binary outputs. The input variables designated the augend and addend bits; the output variables produce the sum and carry. We assign symbols x and y to the inputs and S (for sum) and C (for carry) to the outputs. The truth table for the half adder is listed in Table 1. The C output is 1 only when both inputs are 1. The S output represents the least significant bit of the sum. The simplified Boolean functions for the two outputs can be obtained directly from the truth table.

Table 1. Truth Table for half adder

	/ > / /		. KZII I
X	SOMALYA CO	LL EGE OF F	S
0	0	0	0
0	10		0
1		1	0
1	1	0	1

The simplified sum of products expressions are:

$$S = a \oplus b = a'b + ab'$$

$$C = a.b$$

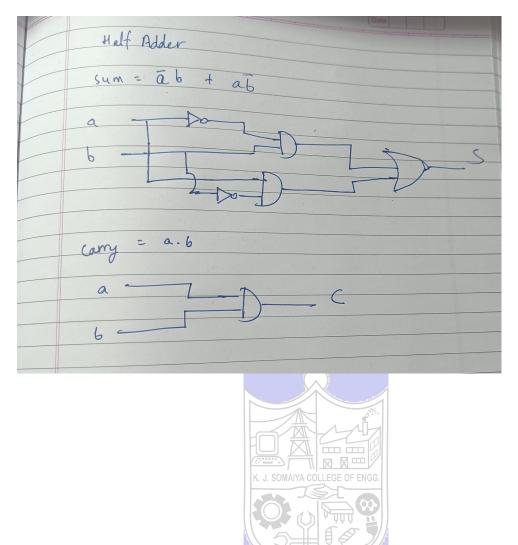


Fig 1.(a) The logic diagram of the half adder implemented in sum of product (using AND-OR gates)

It can be also implemented with an exclusive-OR and AND gate

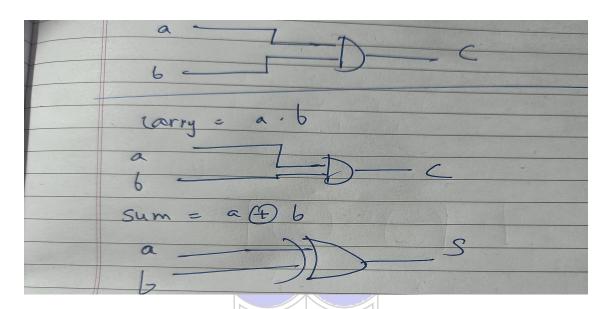


fig. 1(b). The logic diagram of the half adder implemented exclusive-OR and AND gate

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This form is used to show that two half adders can be used to construct a full adder.

Full adder:

A full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs. Two of the inputs variables, denoted by x and y, represent the two significant bits to be added. The third input, z, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum. The binary variable C gives the output carry. The truth table of the full adder is listed in table 2. The eight row under the input variables designate all possible combinations of the three variables. The output variables are determined from the arithmetic sum of the input bits. When all input bits are 0, the output is 0. The S output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The C output has a carry of 1 if two or three inputs are equal to 1.

Table 2: Truth Table for Full Adder

X	Y	C (in)	S	C _(out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0

1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The simplified expressions are:

$$S = a \oplus b \oplus c$$

$$C = ab + bc_{(in)} + c_{(in)}a$$

It can be also implemented with two half adders and OR gate. As shown in fig 2. The S output from the second half adder is the exclusive-OR of z and the output of the first half adder,

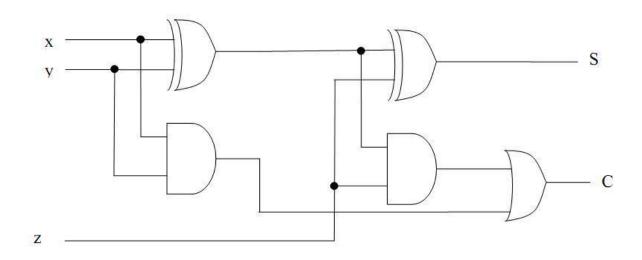


Fig 2: Implement of Full – Adder with two half adders and an OR gate

Thus from fig 2. Expressions for sum and carry are:

$$S = X \oplus Y \oplus Z$$

$$C = Z.(X \oplus Y) + XY$$

Procedure:

- a) Design Half Adder using basic logic gates as well as EX OR and AND gates.
- b) Simulate half adder circuit using EX OR and AND gate on simulator
- c) Verify the truth table.
- d) Simulate full adder using half adder circuits on simulator.
- e) Verify the truth table
- f) Upload the Schematic Diagram generated on Simulation Software as well as Writeup

containing Questions asked in writeup, CO and Conclusion.

g) Please note every Write-up uploaded should be labelled as Exp_<No>_<RollNo>_<writeup>.pdf

Observations and Results: Observe the output for different input combinations.

Outcomes: CO 3. Design the combinational and sequential circuits using basic building blocks.

Conclusion:

The basic concept of adder was understood, implemented and verified using the logic experimentation kits

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.