Experiment No. 5

Title: Conversion of D flip flop to JK flip flop

Batch: A2 **Roll No.:16010421063** **Experiment No.: 5**

Aim: To study flip flop conversion. As an example, we will convert a D flip flop to a JK flip flop.

Resources needed: Simulation Platform (Circuitverse or Proteus)

Theory:

"Flip-flop" is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

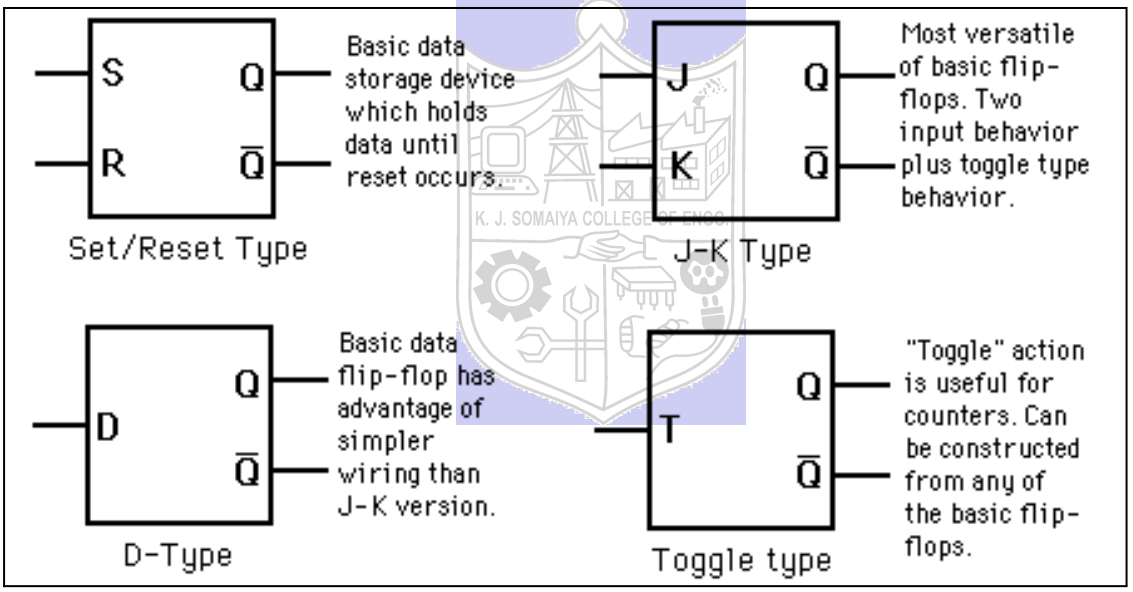


Fig: Types of Flip-flops

Set-Reset FlipFlop:

The set/reset type flip-flop is triggered to a high state at Q by the "set" signal and holds that value until reset to low by a signal at the Reset input. This can be implemented as a NAND gate latch or a NOR gate latch and as a clocked version.

One disadvantage of the S/R flip-flop is that the input S=R=1 gives ambiguous results and must be avoided. The J-K flip-flop gets around that problem.

JK FlipFlop:

JK-flip flop has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

D FlipFlop:

D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate as shown in fig.

T FlipFlop:

T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

Table: Characteristic table and Excitation Table of flipflops

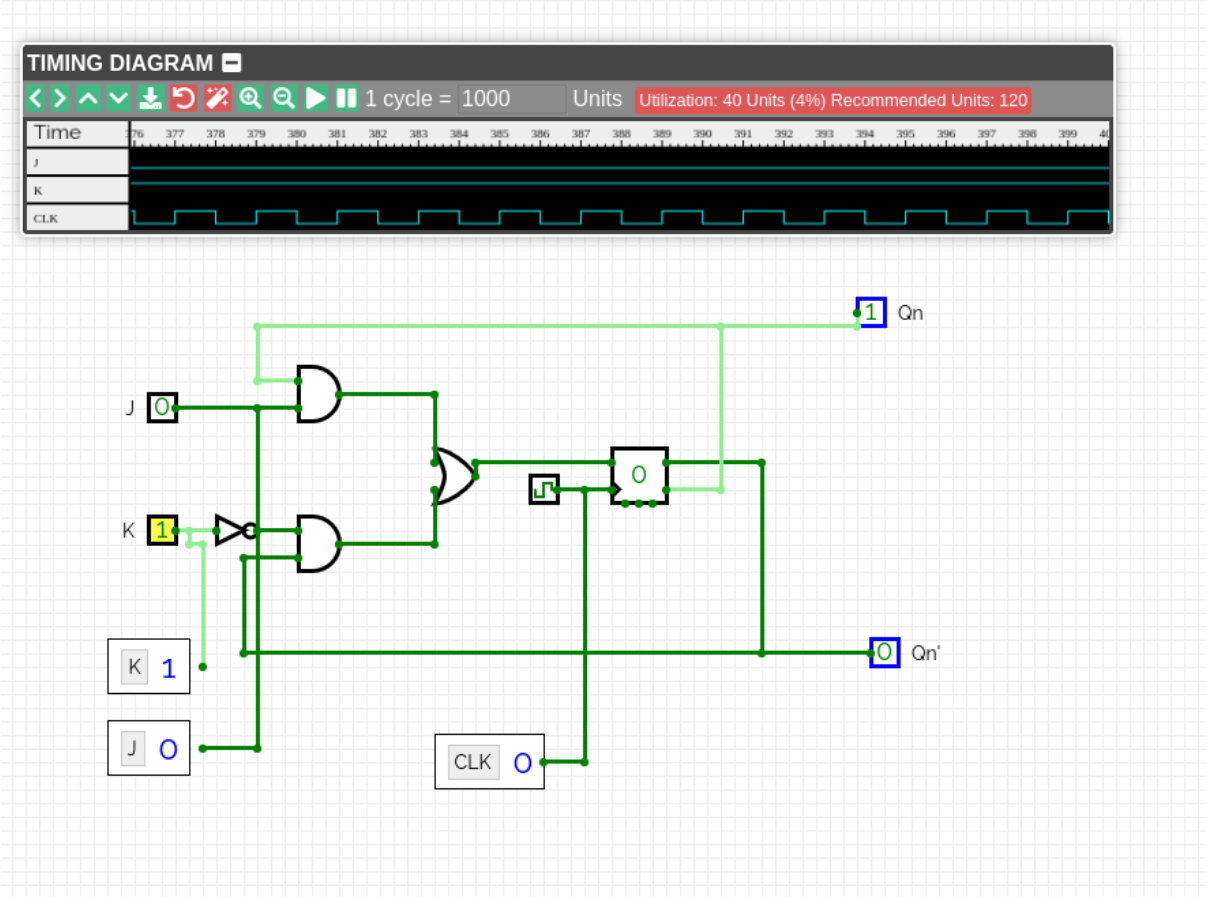
FlipFlop name	Characteristic Table			Characteristic Equation	Excitation Table			
SR	S	R	Qnext		Q	Qnext	S	R
	0	0	Qn	Qnext= S+R'Q Where SR=0	0	0	0	X
	0	1	0		0	1	1	0
	1	0	1		1	0	0	1
	1	1	invalid		1	1	X	0
JK	J	K	Qnext		Q	Qnext	J	K
	0	0	Qn	Qnext= JQ'+K'Q	0	0	0	X
	0	1	0		0	1	1	X
	1	0	1		1	0	X	1
	1	1	Qn'		1	1	X	0
D	D		Qnext		Q	Qnext	D	
	0		0	Qnext=D	0	0	0	
	1		1		0	1	1	
					1	0	0	
					1	1	1	
T	T		Qnext		Q	Qnext	T	
	0		Qn	Qnext= TQ'+T'Q	0	0	0	
	1		Qn'		0	1	1	
					1	0	1	
					1	1	0	

Procedure:

1) Write the characteristic table of the desired (target) flip flop, in this case JK flip flop.
2) Write the excitation table of the given flip flop (in this case D flip flop).
3) Combine the two tables to create a conversion table.
4) Using the conversion table draw K maps for the J and K inputs in terms of D and Q.
5) Use the equations to draw the circuit.
6) Start the Circuitverse simulator and perform the simulation.
7) Complete the write up and upload it to LMS.

Observations and Results:

1. Simulate the circuit using the online Circuitverse simulator.
2. Observe the timing diagrams to verify your design.
3. Download the image of timing diagram and paste it in the write up.



Outcomes:

CO3: Design the combinational and sequential circuits using basic building blocks

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Questions:-

(a) Why do we need to know how to convert one flip flop to another?

The conversion of flip-flops from one type to another is done by connecting a combinational circuit prior to the flip-flop. The output of the combinational circuit is given to the input of the flip-flops. While designing a flip-flop, the excitation tables for both flip-flops are combined and a truth table is made for the data inputs and data outputs.

Conclusion: We were able to verify JK to D flip flop using timing diagram

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/flipflop.html