Experiment No. 6

Title: Implementation of 4-bit synchronous Johnson counter using JK flips flops

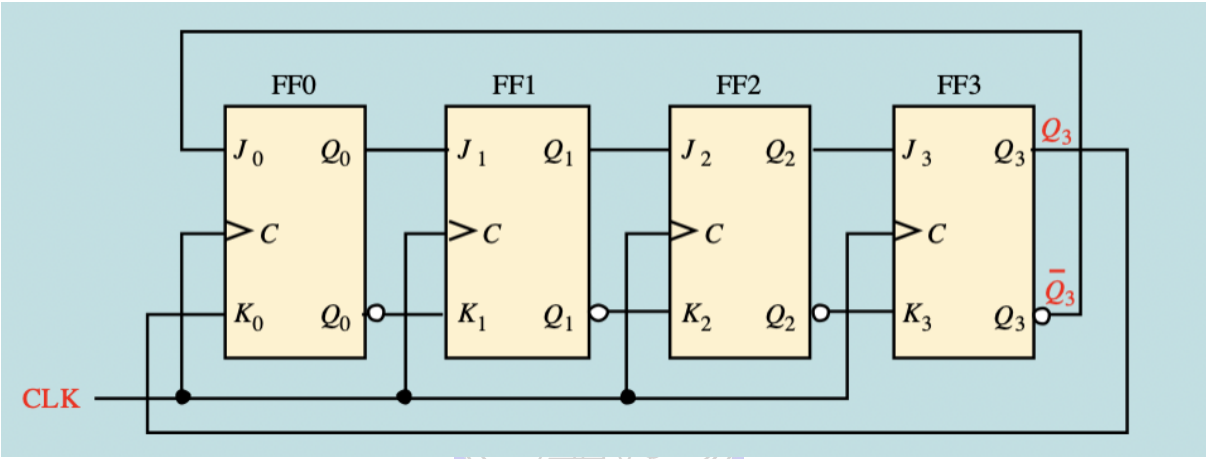
Batch: A2 **Roll No.: 16010421063** **Experiment No.: 6**

Aim: Implementation of a 4-bit synchronous Johnson counter using a JK flip flop.

Resources needed: Simulation Software, (Circuitverse)

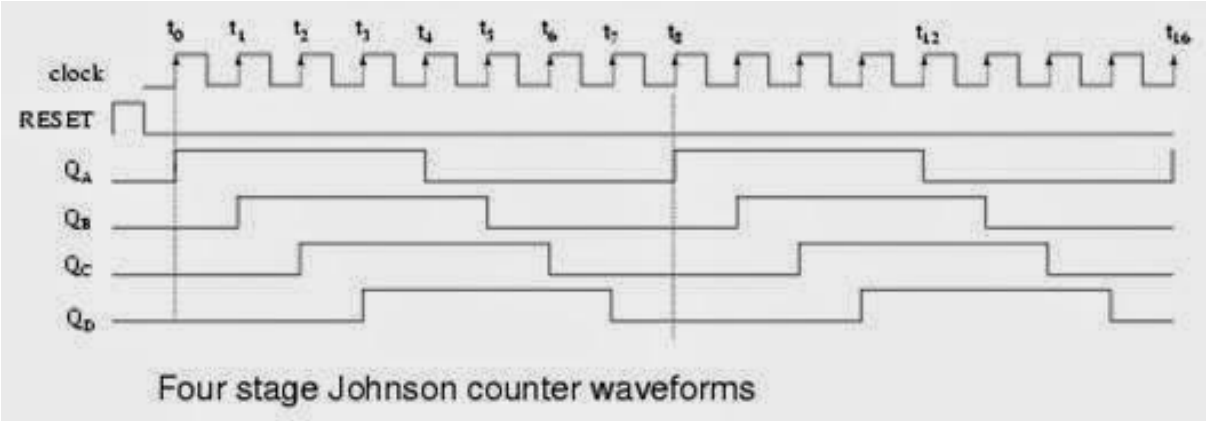
Theory:

The Johnson counter is also known as modified ring counter or switched tail counter.
It is basically a ring counter, but with the modification that **the complement of the output of the final flip flop is fed back to the input of the first flip flop.**



In table form the output would look like this:-

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1



Four stage Johnson counter waveforms

Applications of Johnson counter:

- Johnson counter is used as a synchronous decade counter or divider circuit.
- It is used in hardware logic design to create complicated Finite states machine. ex: ASIC and FPGA design.
- The 3 stage Johnson counter is used as a 3 phase square wave generator which produces 1200 phase shift.
- It is used to divide the frequency of the clock signal by varrying their feedback.

Advantages of Johnson counter:

- The Johnson counter has same number of flip flop but it can count twice the number of states the ring counter can count.
- It can be implemented using D and JK flip flop.
- Johnson ring counter is used to count the data in a continuous loop.
- Johnson counter is a self-decoding circuit.

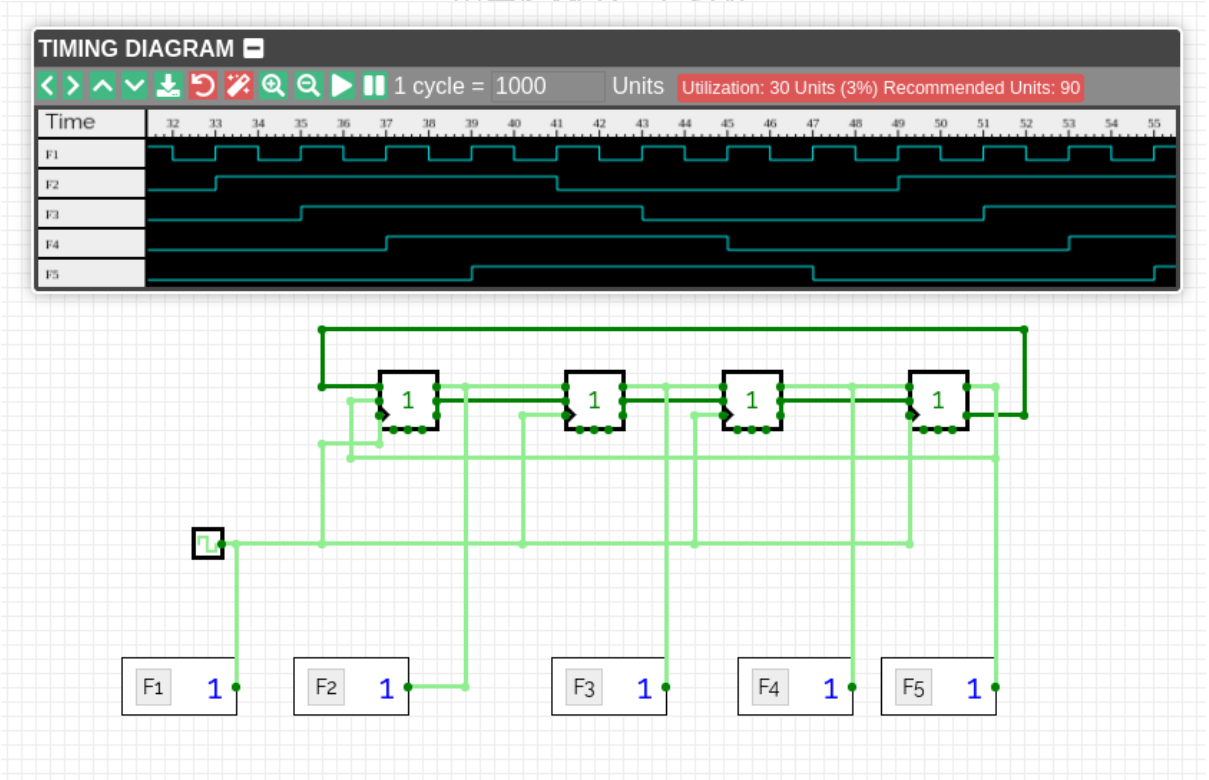
Disadvantages of Johnson counter:

- Johnson counter doesn't count in a binary sequence.
- In Johnson counter more number of states remain unutilized than the number of states being utilized.
- The number of flip flops needed is one half the number of timing signals.
- It can be constructed for any number of timing sequence.

Procedure:

1. Design a 4 bit synchronous counter using JK flip-flop as per the design procedure mentioned in theory.
2. Simulate the logic design using JK flip-flops on the simulation software.
3. Verify the output of the designed and simulated counter for the proper sequence.
4. Generate the output timing diagram on simulator.
5. Upload Schematic and Timing Diagram generated on Simulator as instructed during lab session.

Observations: Generate the timing diagrams (waveforms) and download a snapshot to verify the output.



Questions:

(a) Will the sequence change if we use negative edge triggered FF instead of positive edge triggered FF?

This is an issue when you have one flip-flop output driving the input of the next. If both flip-flops update on a rising edge, then the second one will be sampling its input at the same time the first is updating the output. If the clock has more delay (due to trace length or capacitive loading) than the signal, then the second flip-flop can miss the value. Note that this problem is independent of the clock frequency, slowing down the clock doesn't fix it, only fixing the relative delays will help.

Outcomes:

CO3: Design the combinational and Sequential circuits using basic building blocks and MSI devices

---

Conclusion:

A 4 bit Johnson counter is implemented using JK flip flop and appropriate logic gates

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.
2. http://www.electronics-tutorials.ws/counter/count_4.html