Expertiment1:

RC Circuits and diode characterization

1. Oscilloscope and function generator

Aim: Understanding our equipment's.

Equipment used: Keysight EDUX1052G Digital Storage Oscilloscope (DSO)

Observations:

b) i) RC specifications of oscilloscope: 1Mohm, 16pF respectively.

RC specifications of probes: 10:1 mode->10Mohm, 15pF respectively.

1:10 mode->1Mohm, 100pf respectively.

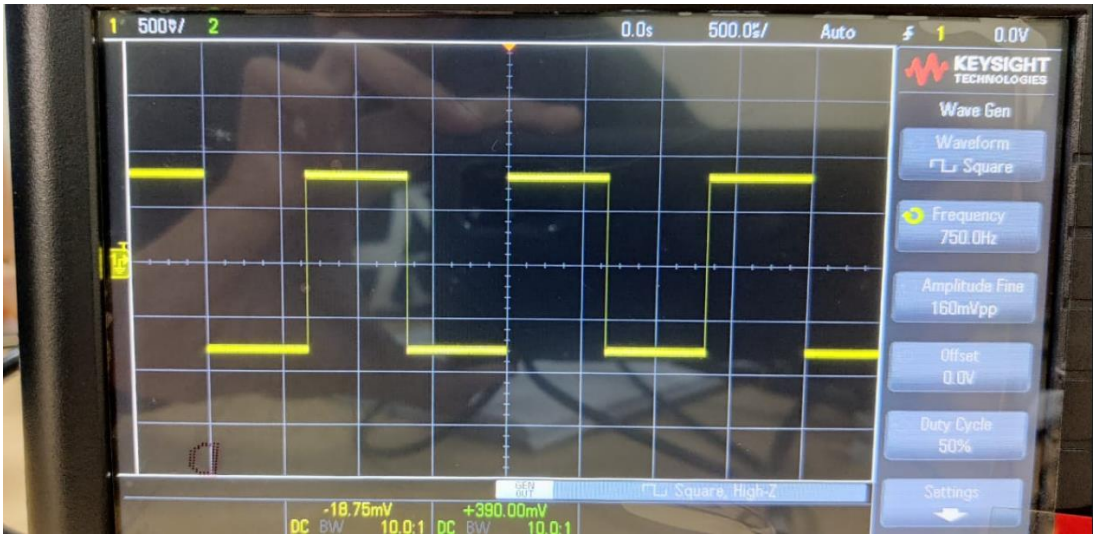
The modes are the attenuation factors, that is the amount by which the probe reduces the amplitude of the signal. Ex. 10X reduces the amplitude by ten times of the input signal.

The modes on the OSC by which it increases the amplitude of the input signal.

ii)Plotting demo graphs -> Sinusoid and square wave.

1.Shape: Sine plot, frequency: 940Hz, Amplitude: 160mVpp.

2.Shape: Square, frequency: 750Hz, Amplitude: 160 Vpp.



iii)Playing with different modes:

Observations:

Input: Square wave, Amplitude 160mVPP, frequency: 750 Hz

In 1X mode(probe): Amplitude and frequency both remain same

In 10X mode(probe): Amplitude = 80mVpp, frequency remained same.

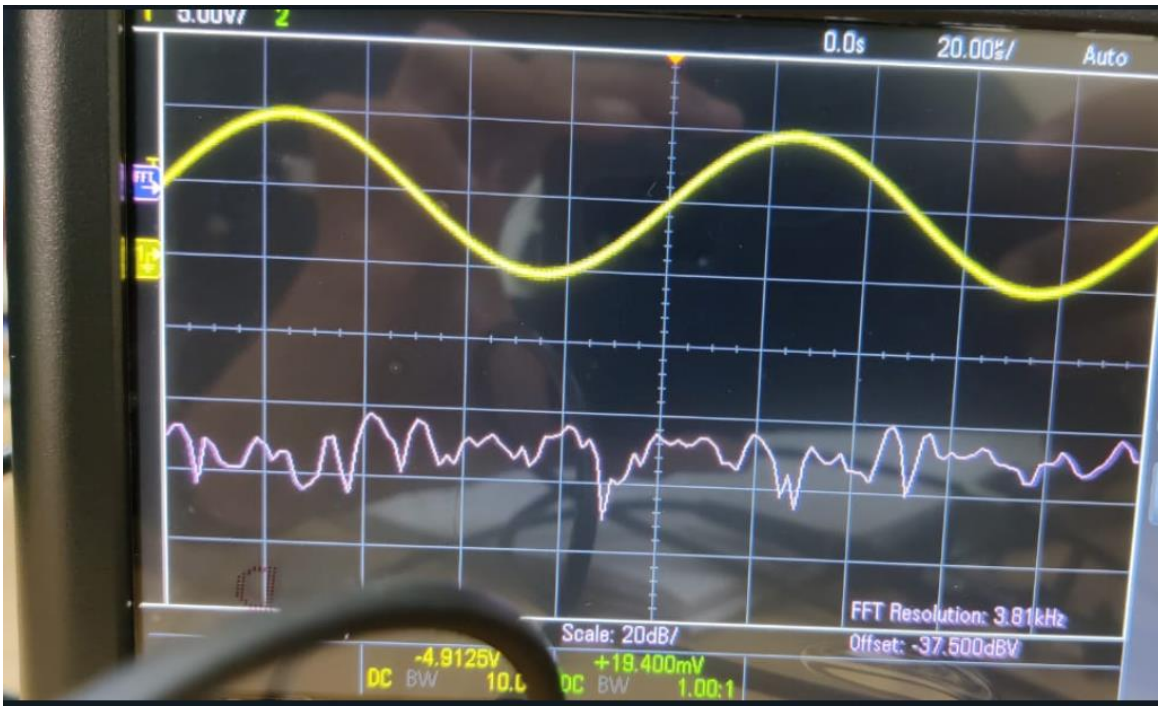
If OSC factor and probe factor are the same either 1:10 or 1:1 then Vin is equal to Vosc.

If OSC is 10 times probe factor, Vosc = 10*Vin, but if Probe factor is 10 times OSC, Vosc = 1/10*Vin.

Conclusion:

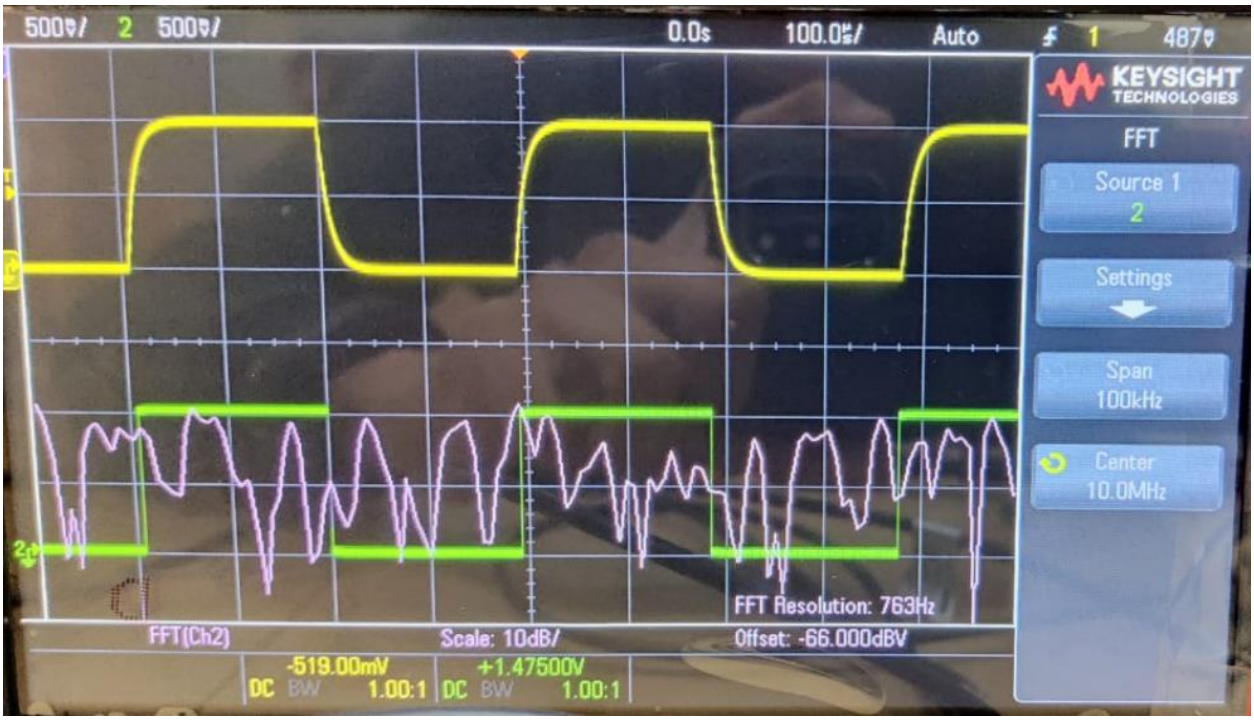
Vosc = (OSC factor / probe factor) * Vin.

iv) Generate 10 kHz sine wave with 1V_{pp} amplitude and observe its spectrum using FFT feature on DSO.

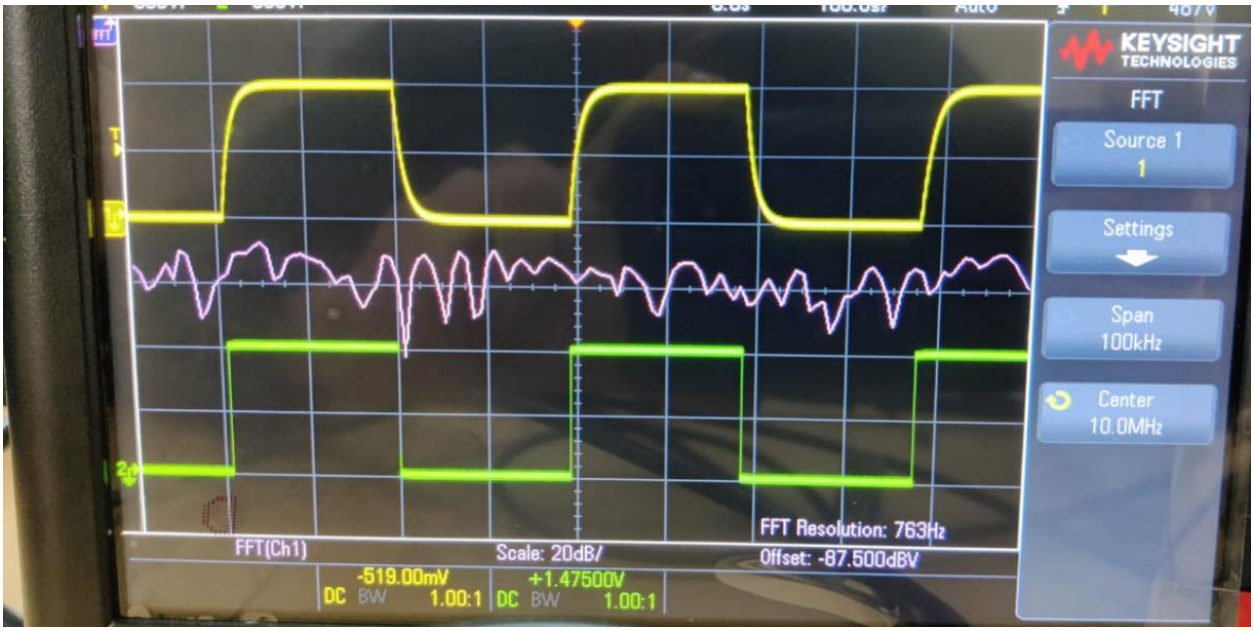


v) Changing the wave type from sine to square and observing spectrum

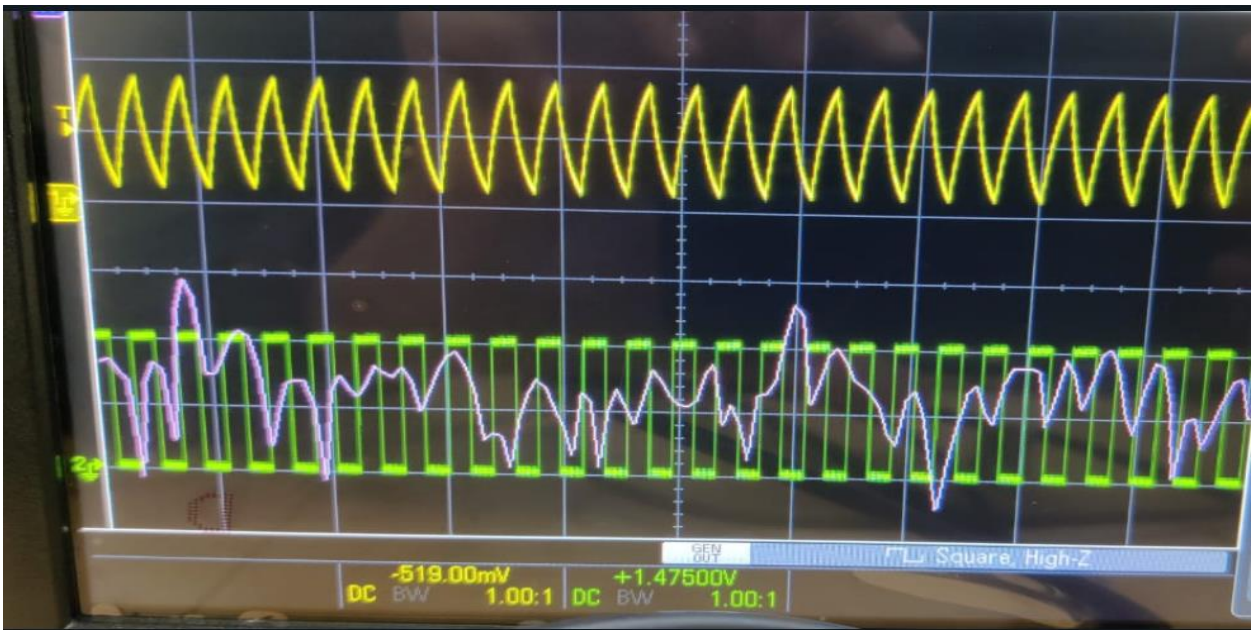
The FFT plotted here is the FFT of input square wave. We can see it is harmonic.



Now to reduce the strength of the harmonic we pass the input signal through a low pass RC filter and the output of the low pass filter along with the outputs FFT is plotted below, we see that the amplitude of the output signal is low as well as of the FFT output.



Now on increasing the frequency of the input signal, as the circuit is low pass filter it will output the signal with amplitude quite low than the input signal, and so the FFT amplitude future decreases. Below is the FFT of input square wave having higher frequency.



FFT amplitude of the output voltage is less than the previous plots. The FFT output decreases with increasing frequency.

We can reduce the Harmonic strength by increasing the time constant of the circuit(=RC).

Frequency = 10KHz = ½*PI*R*c

If R is 10kohm, C comes out to be 1.6 Pf.

On making C= 1nF,

The practically calculated time period comes out to be 9.8 Us and the harmonic strength is significantly reduced.

Part 2: Estimate the effective probe-capacitance

Given: R=1Mohm, Capacitor: 10pF

Observations:

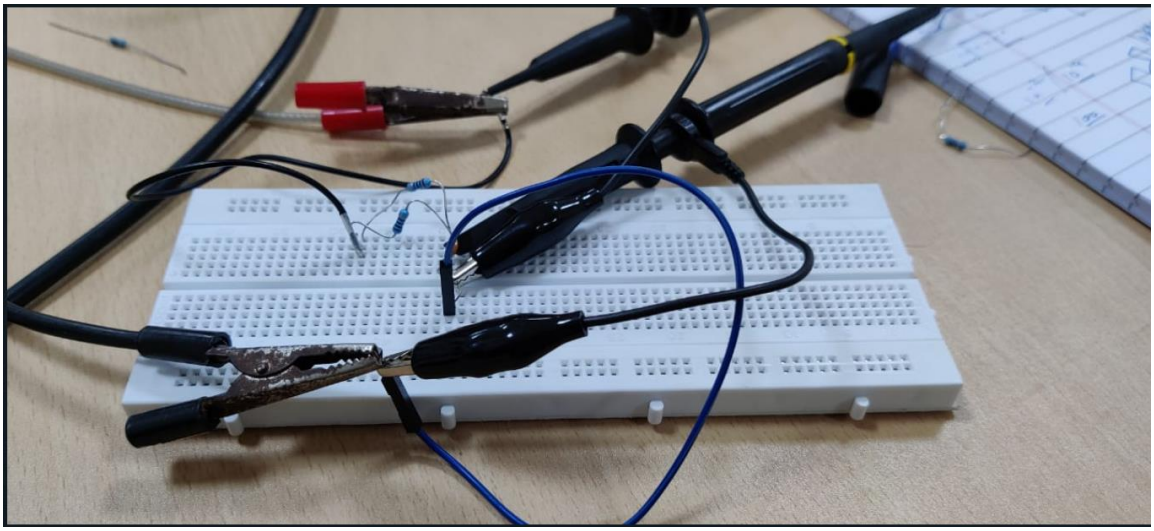
On calculating time constant of the circuit the time constant (RC) comes out to be 10^-5 sec,

i.e 10us.

Next: we practically calculate the time constant by finding the setting time through the below graph and as we know that setting time is nearly 5 times the time constant, therefore we calculate the time constant by dividing the settling time by 5.

In the below graph the settling time comes out to be 37.5 usec.

Circuit:



Let c2 be the probe capacitance.

Therefore: R(C1+C2) = 37.5 us (practical value) and R(C1) = 10uS.

Therefore: R*C2 = 27.5 uS.

i.e C2 ~ 27.5 pF

This is verified through creating a circuit as:

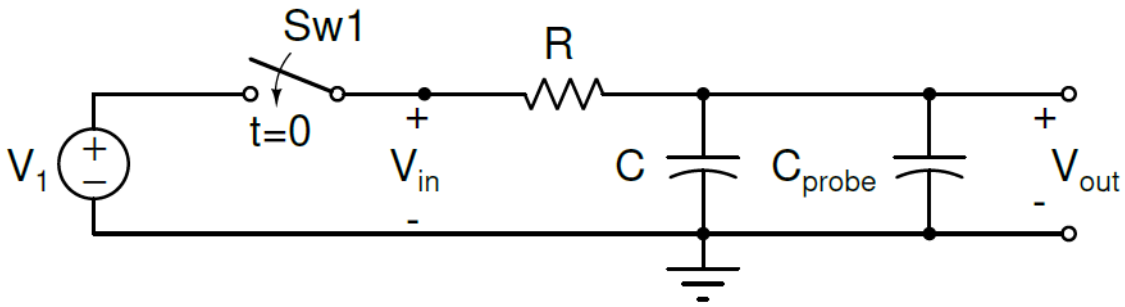


Figure 1

And the value of the Cprobe is set to 27 Pf.

Now when I passed the same signal the output signal had settling time: 55 uS,

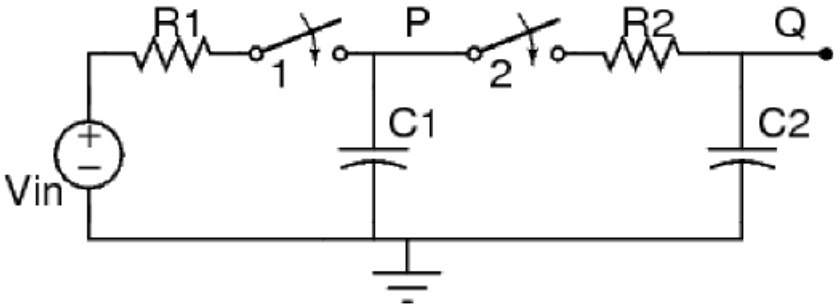
Therefore, time constant as 55/5 us = 11uS.

Hence our calculated result matches with practical implementation.

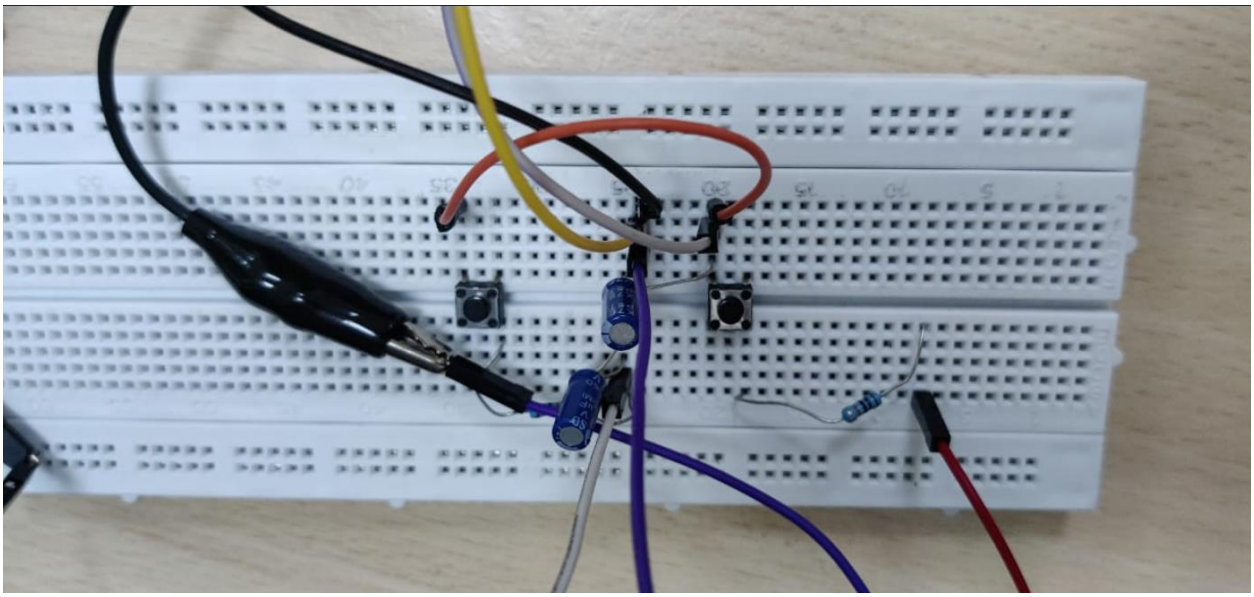
Part 3:

Aim: In this experiment we will be observing the switching behaviour (charging and dis-charging) of Capacitors.

Circuit:



a) $C_1 = C_2 = 1\ \mu F$ and $R_1 = R_2 = 100\ \text{Kohm}$.
In this case when the 1st switch is switched on, the capacitor requires 5*RC time to reach saturation, RC = 100ms, time to reach saturation is 500ms.

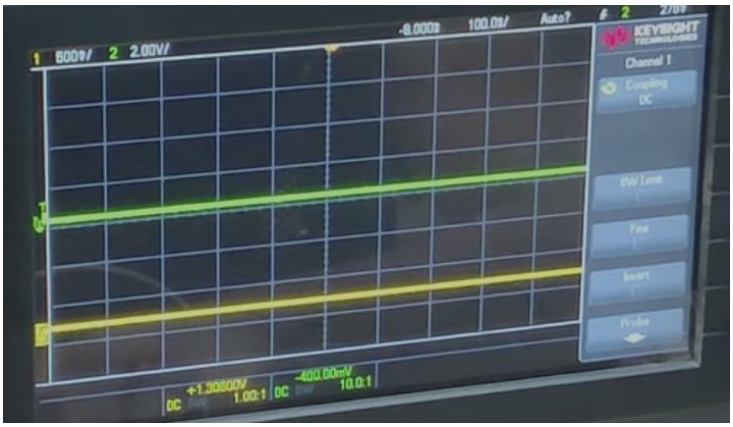


B) Applying the 1v Dc voltage at Vin with the help of the function generator integrated in the Oscilloscope ('Wave Gen').

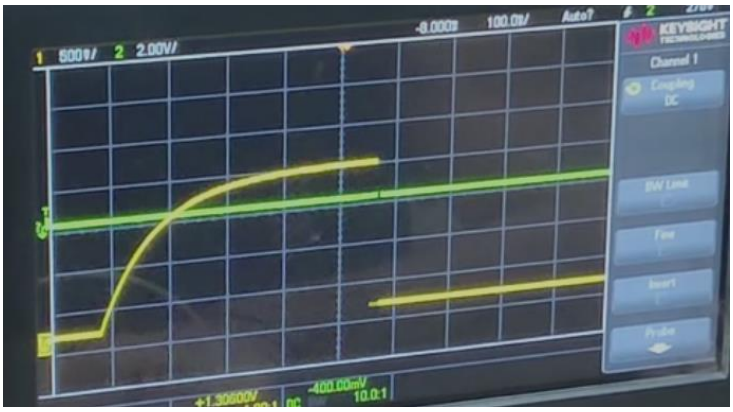
C)Initially, switch 1 is closed (push button is kept pressed) and switch 2 is opened, which allows the capacitor C_1 to charge to the supply voltage(1V).

Observation on OSC:

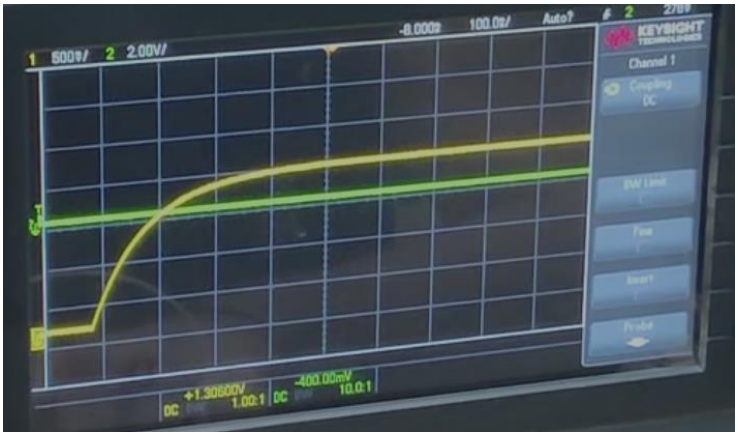
1.Initially none of the capacitor is charged(0ms):



2.Capacitor(C1) starts charging(100ms):

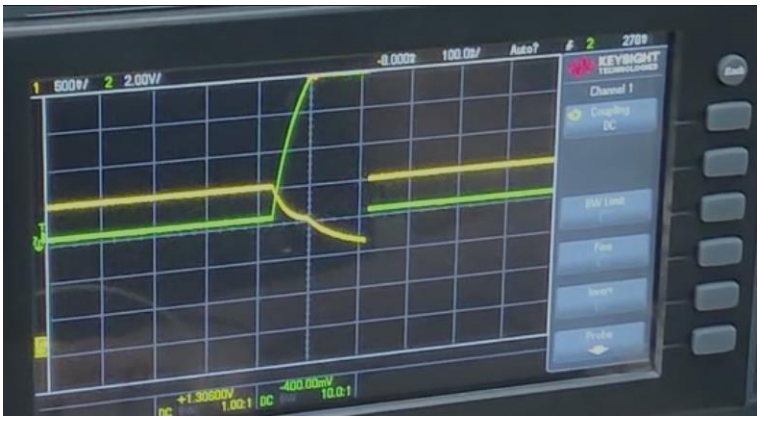


3.Reaches saturation(600ms):

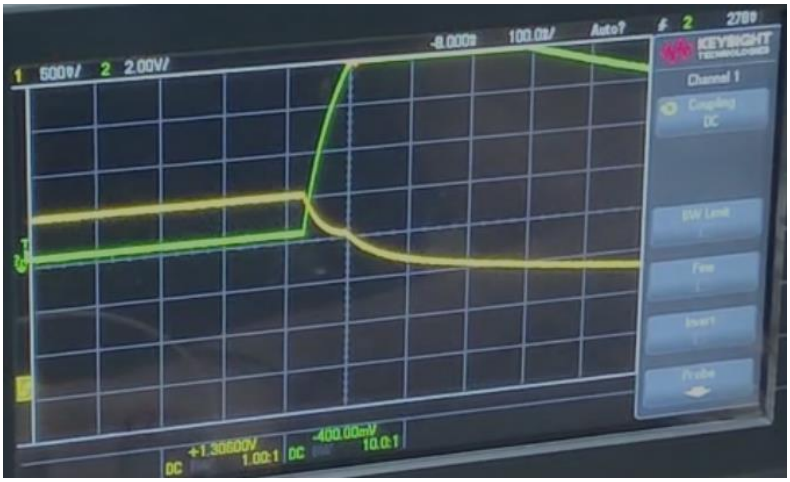


d) Now C_1 is completely charged, opening switch 1 and closing switch 2, and observing the voltage across nodes P and Q using probes in the oscilloscope.

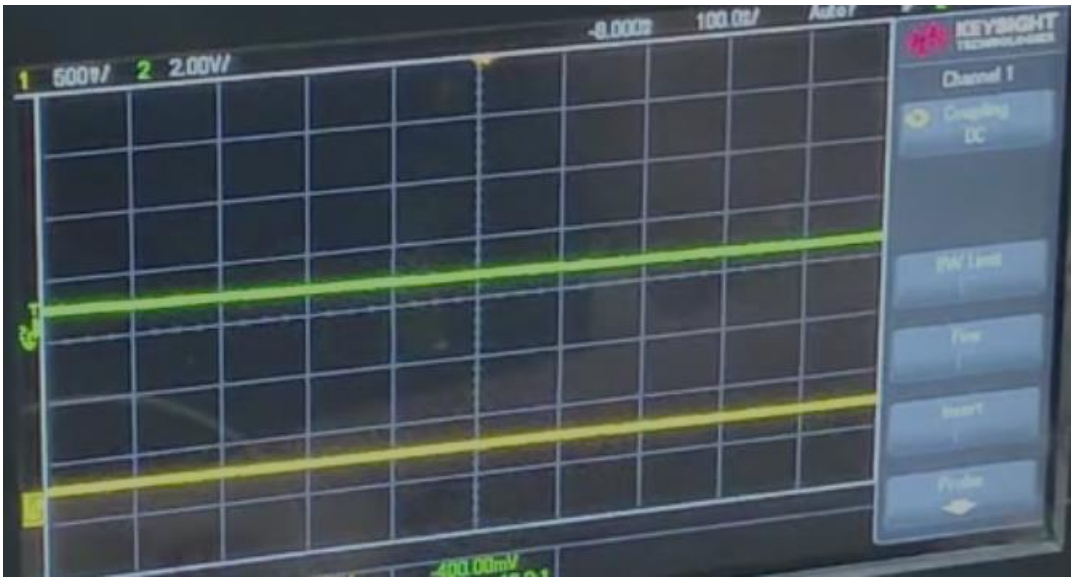
The time when C1 start to discharge and C2 starts charging:



The capacitors reaching the same voltage:



Capacitors reached the same voltage:



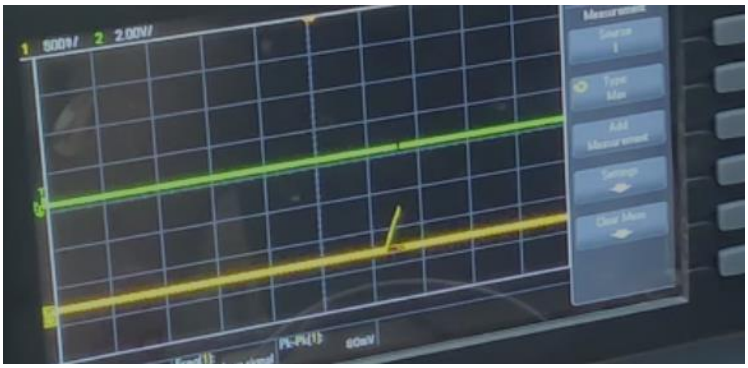
e) As initial both the capacitors are uncharged and then switch 1 in switched on, the capacitor C1 voltage rises exponentially from 0 to V0, it starts from 0 because initially when there is no charge on capacitor it behaves as short circuit, and at time t = 5* time constant it reaches its saturation value, a position at which it cannot acquire any more charge and so there cannot be a current in the circuit, now the potential drop across capacitor is equal to Vin(1Vpp). The rise is exponential because i = c(dv/dt), current and voltage are not related linearly but form a LDE on applying KVL to the circuit.

After complete charging of C1, switch 1 is opened and switch 2 is closed, now the capacitor C1 discharges while charging capacitor C2, this process continues till both the capacitors are

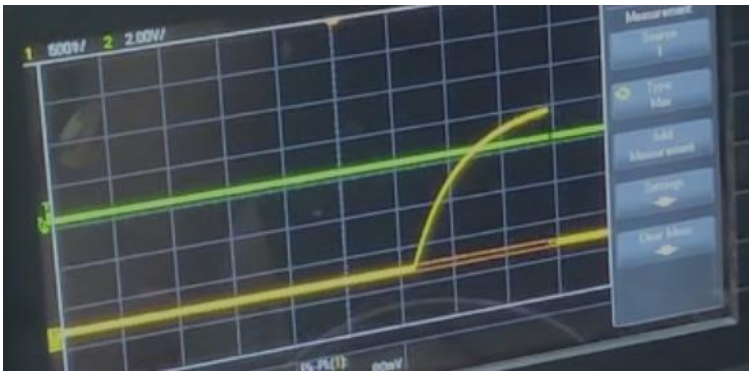
charged such a way that voltage across both of them is same (i.e Q1/C1 = Q2/C2) .In this stage there would be no current flowing in the circuit.

f) Now, changing the values of R_2 = 10 Kohm and observing the changes in the plot on oscilloscope.

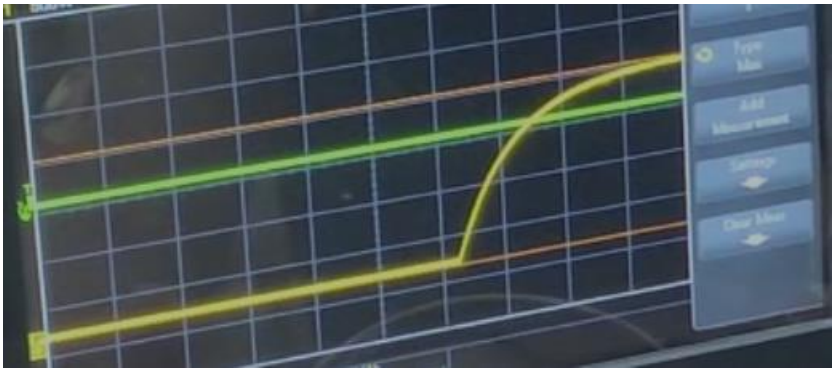
1.Initially none of the capacitor is charged(0ms):



2.Capacitor(C1) starts charging(100ms):

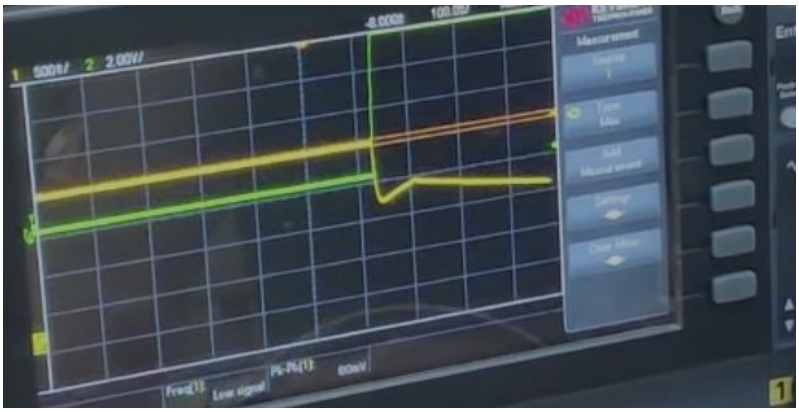


3.Reaches saturation(600ms):



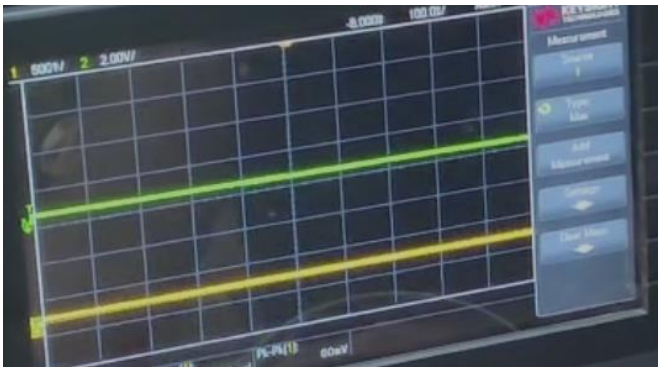
Now C_1 is completely charged, opening switch 1 and closing switch 2, and observing the voltage across nodes P and Q using probes in the oscilloscope.

The time when C1 start to discharge and C2 starts charging:



The capacitors reaching the same voltage:

Capacitors reached the same voltage:



Observation: Here the discharging of C1 and charging of C2 to reach a same voltage was faster than the previous case when R2 was 100kohm.

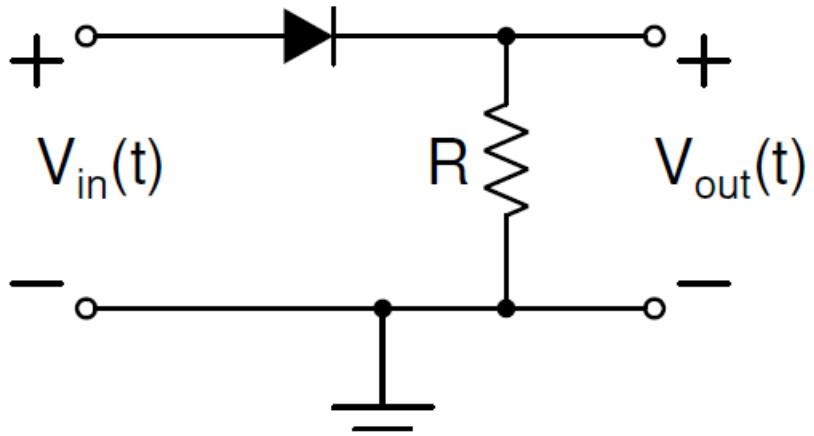
If we consider the time at which Switch 2 was closed as 0:

Time taken to reach final values is 0.24ms for R2=10kohm and 230ms for R2=100Kohm.

Part 4:

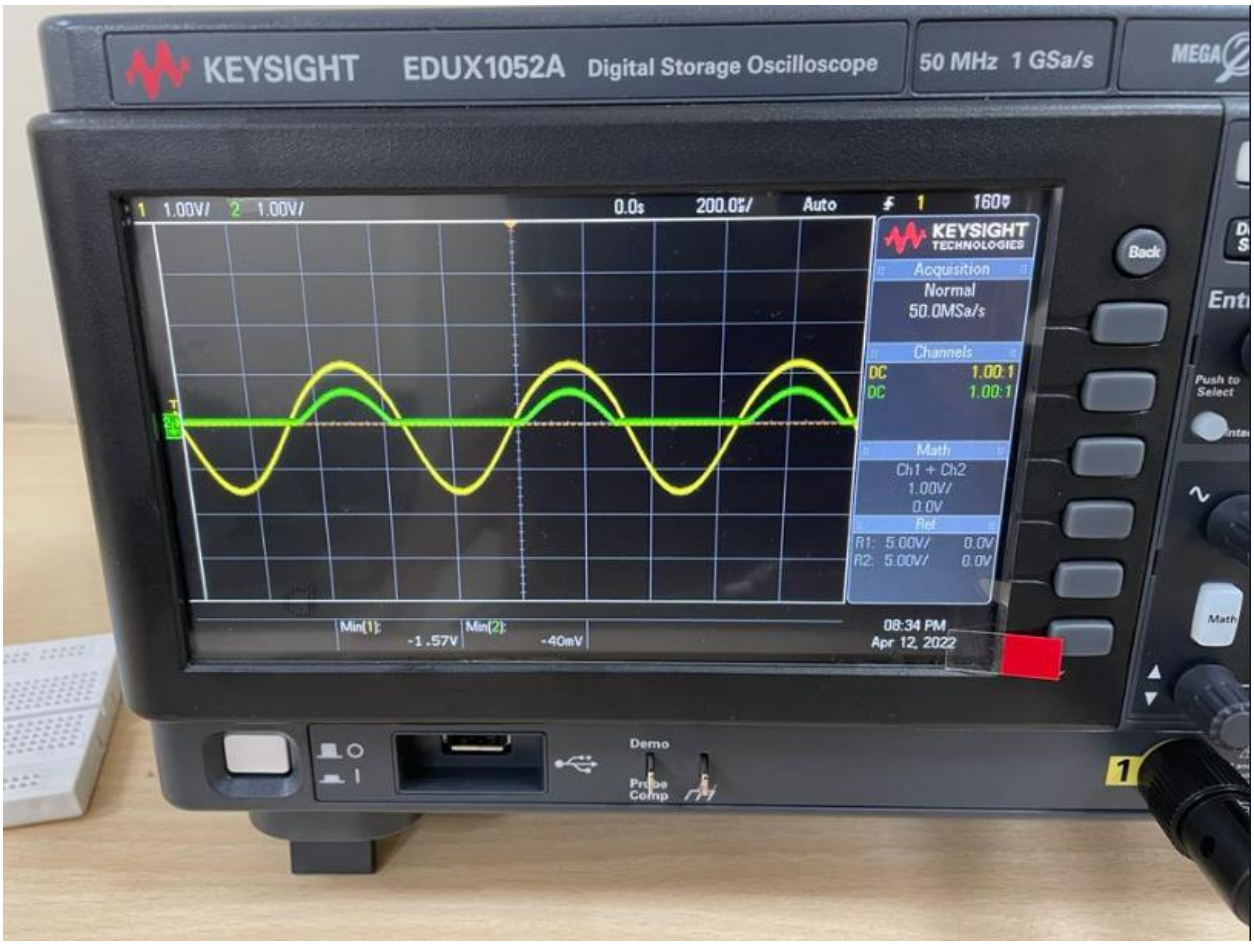
4. Diode Characteristics

Circuit:

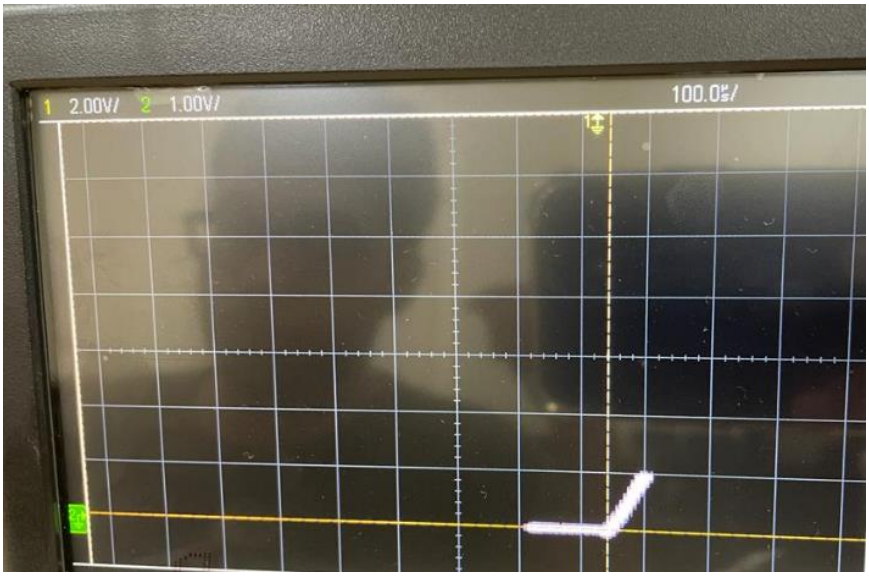


a) We apply input signal as sine wave of amplitude 1Vpp, the output is shown below.

When the sine wave rises from 0 to 0.425 the diode doesnt conduct any current, hence the output across the resistor is 0, after the 0. 425 V mark,the V across the diode is constant at 0. 425V and so now the output =Vin-0. 425 v. The current in the circuit is again 0, after the Vin value is less than 0.425 V, also the current is negligible when input signal has negative amplitude, because at that time the diode behaves as reverse bias, and the current through is neglible.



b)I-V characteristic on the OSC



C) The cut in voltage is nearly: 0.425 V.

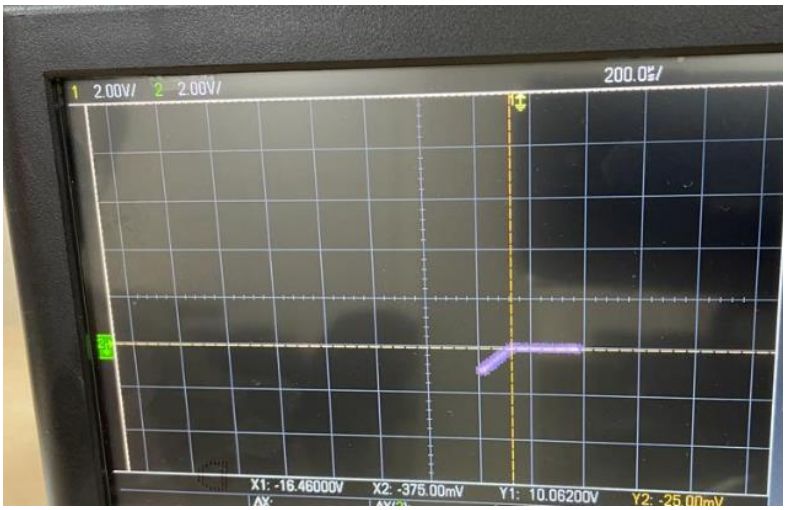
d) The current through R= Vout/330 ohms.

For Vin<0.425 -> Current through the circuit is 0.

For Vin<0 the current is negligible, of order of uA, as explained earlier.

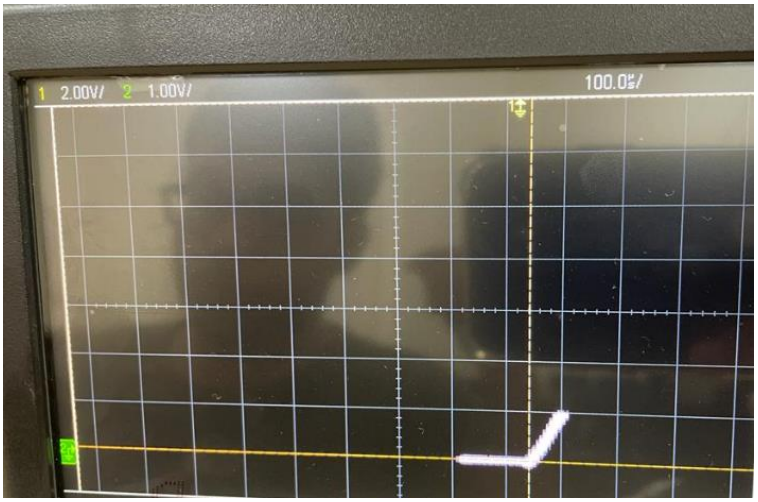
e) Connecting the diode in reverse bias:

Output:



Initially at low negative voltage the current is nearly 1uA(or equal to leakage current), and then after breakdown voltage the circuit behaves as voltage regulator.

F) Forward bias:



Reverse bias: