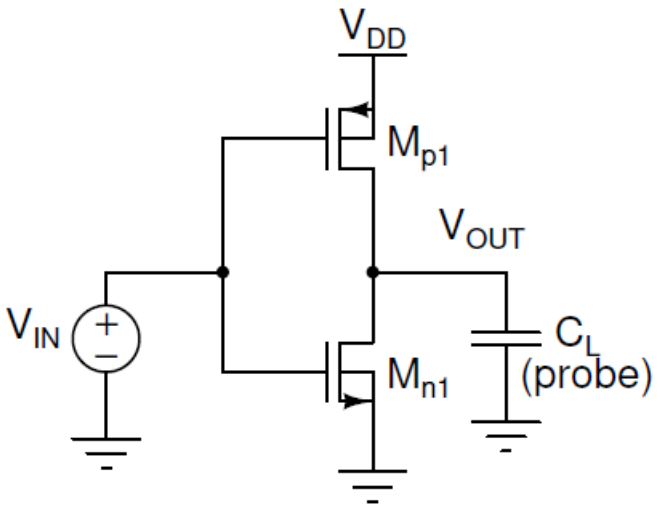
Experiment-8
Operational Amplifiers

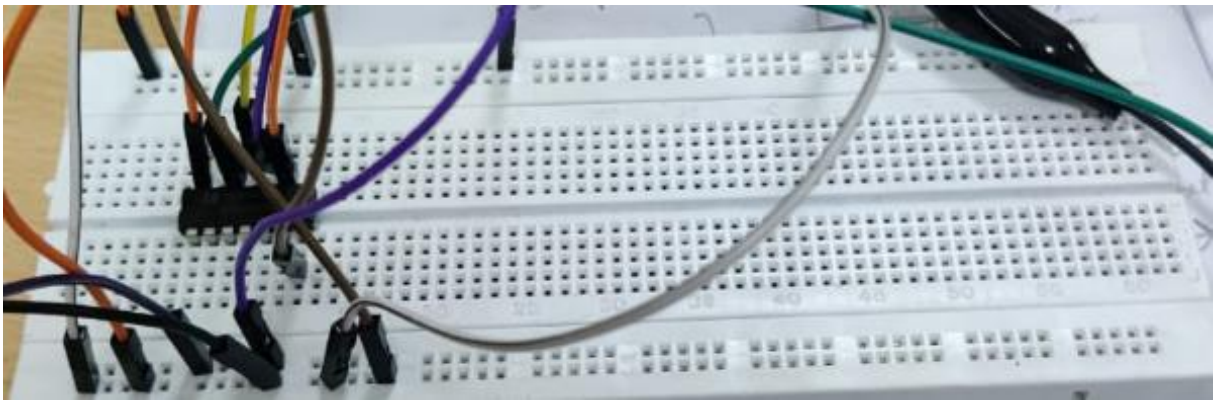
Part 1:
(A) To plot the voltage transfer characteristics (VOUT vs VIN) and identify the valid input output region for the circuit to act as an amplifier.

Schematic circuit:

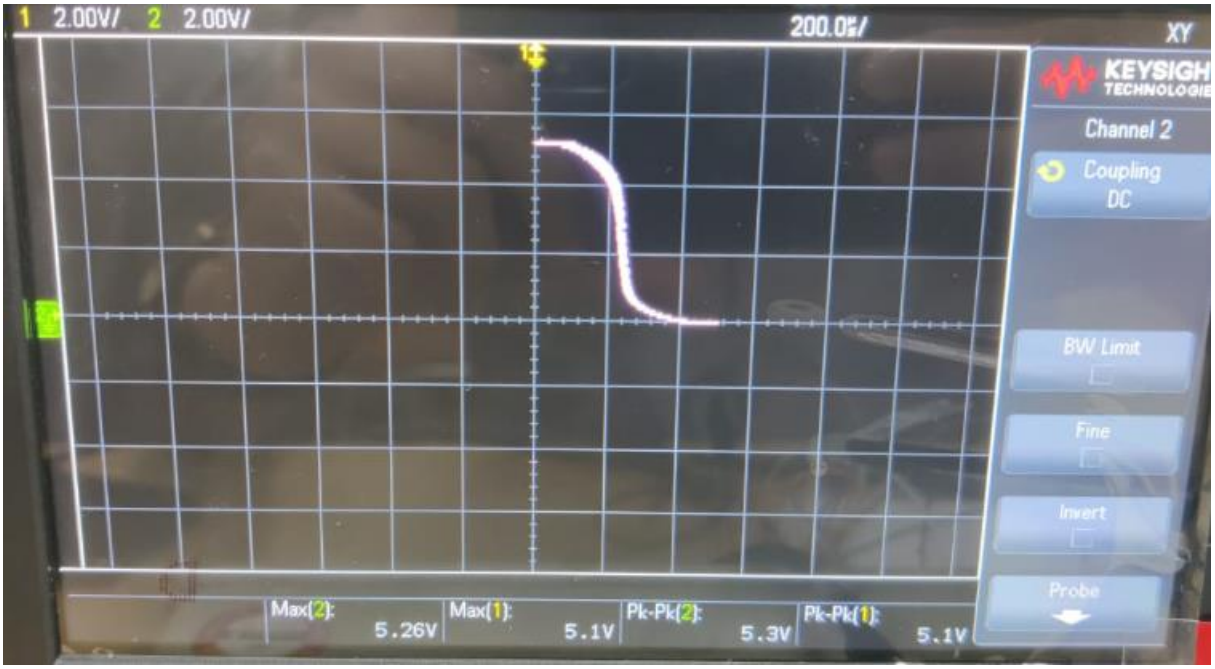


Where V_{DD} is 5 V.

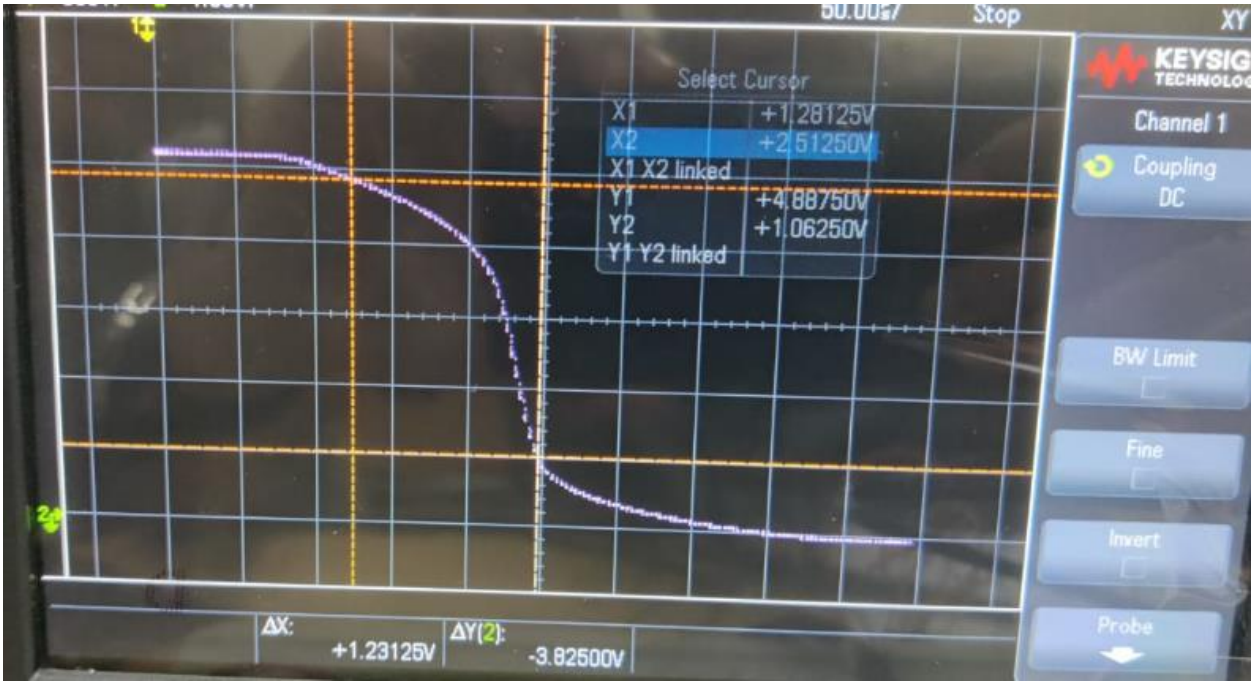
Circuit:



Plot:

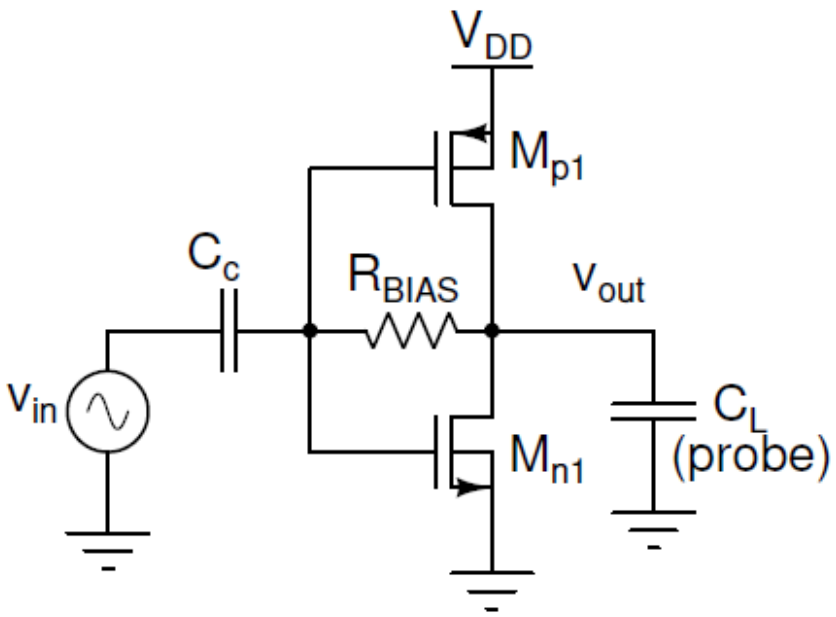


Approximate points where gain (Slope of graph) is greater than 1 in magnitude.



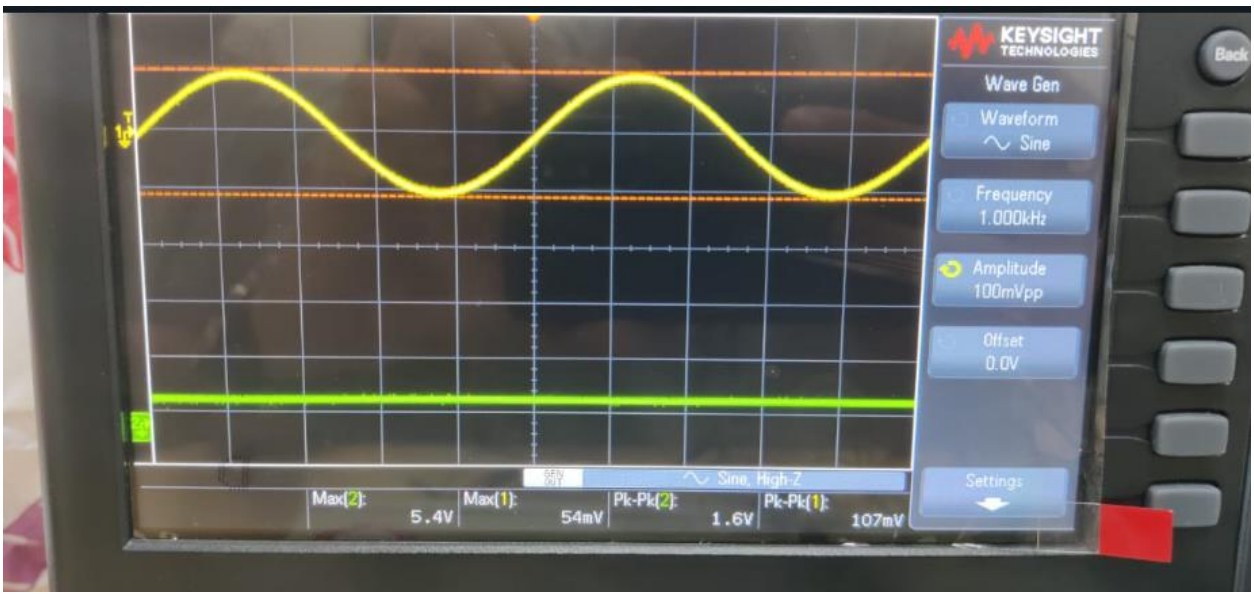
Start: V_{IN} = 1.28125V End: V_{IN} =2.51250V

(B) Schematic circuit:

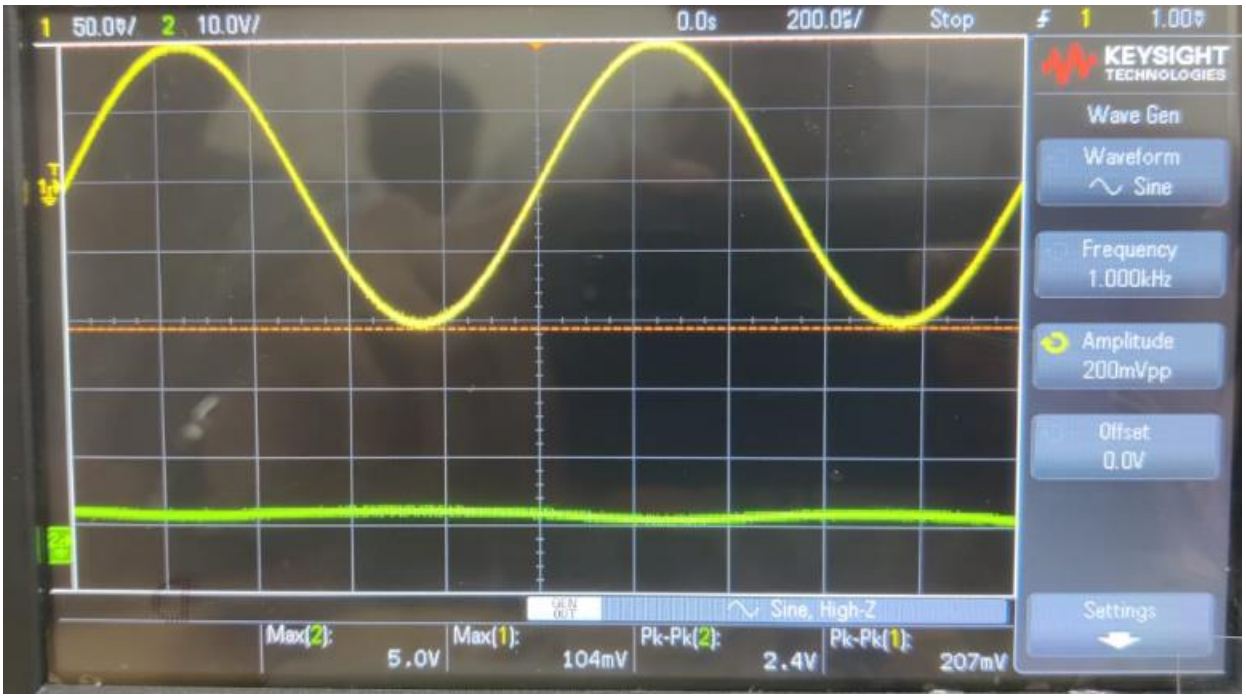


Observing gain of the circuit for different input values of V_{in}.

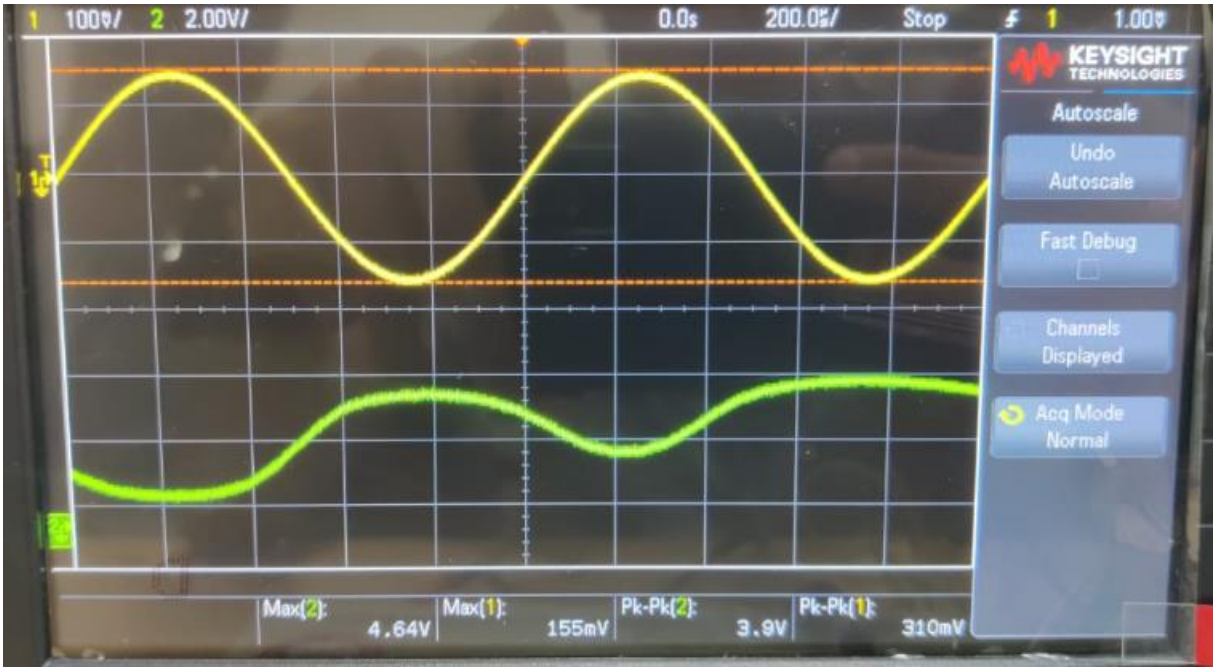
For Vin: 100mVPP



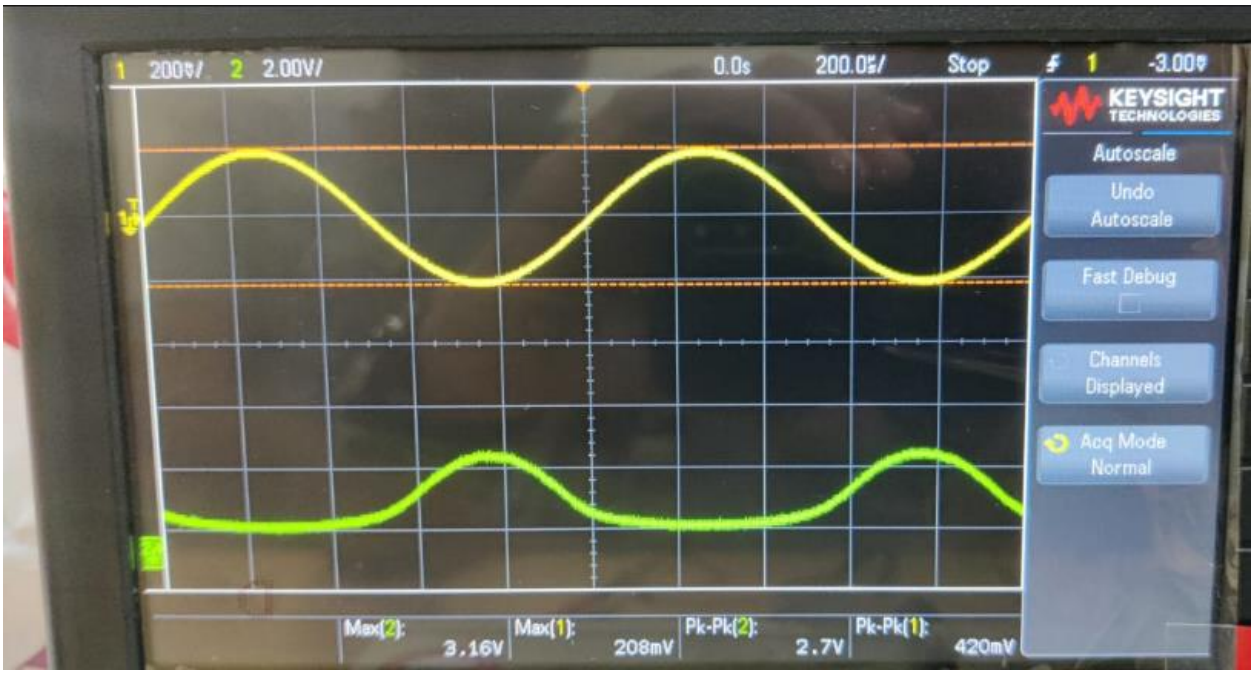
Vin: 200mVPP



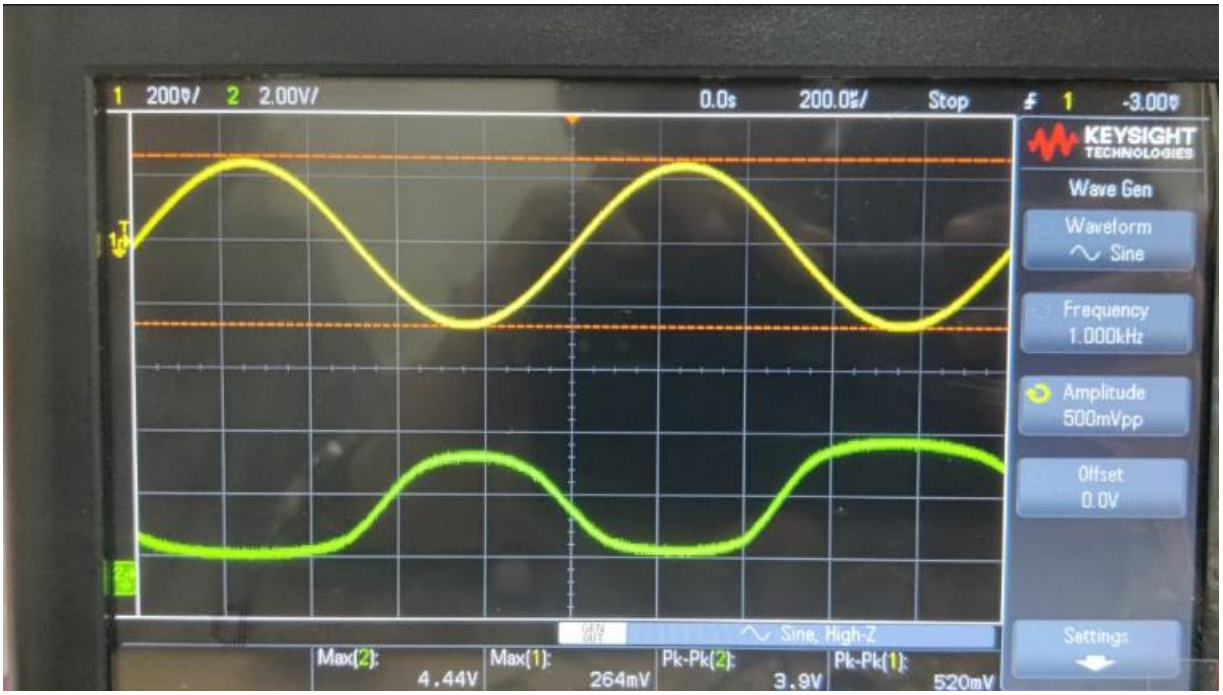
Vin: 300mVPP



Vin: 400mVPP



Vin :500mVPP



Vin (mVolts)	Vout (Volts)	Gain

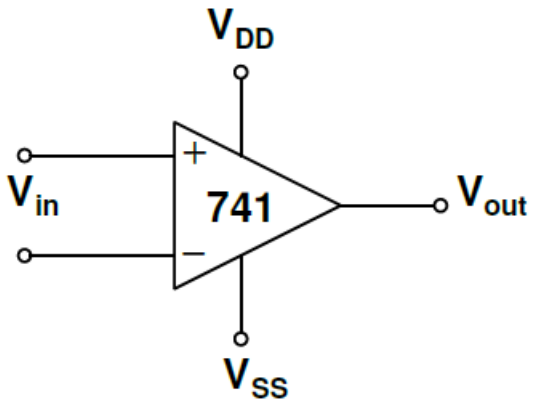
100	1.6	16
200	2.4	12
300	3.9	13
400	2.7	6.75
500	3.9	7.8

There is a clip off because for higher values of Vin the circuit reaches in a region where Vin - Vth> Vout, hence it enters triode region hence we instead getting a sinusoidal input get a clip off.

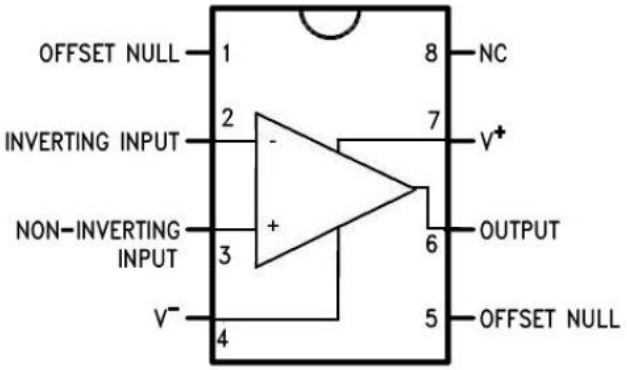
DC values at gate= 756mV and drain= 100mV

2. Characterization of an operational amplifier

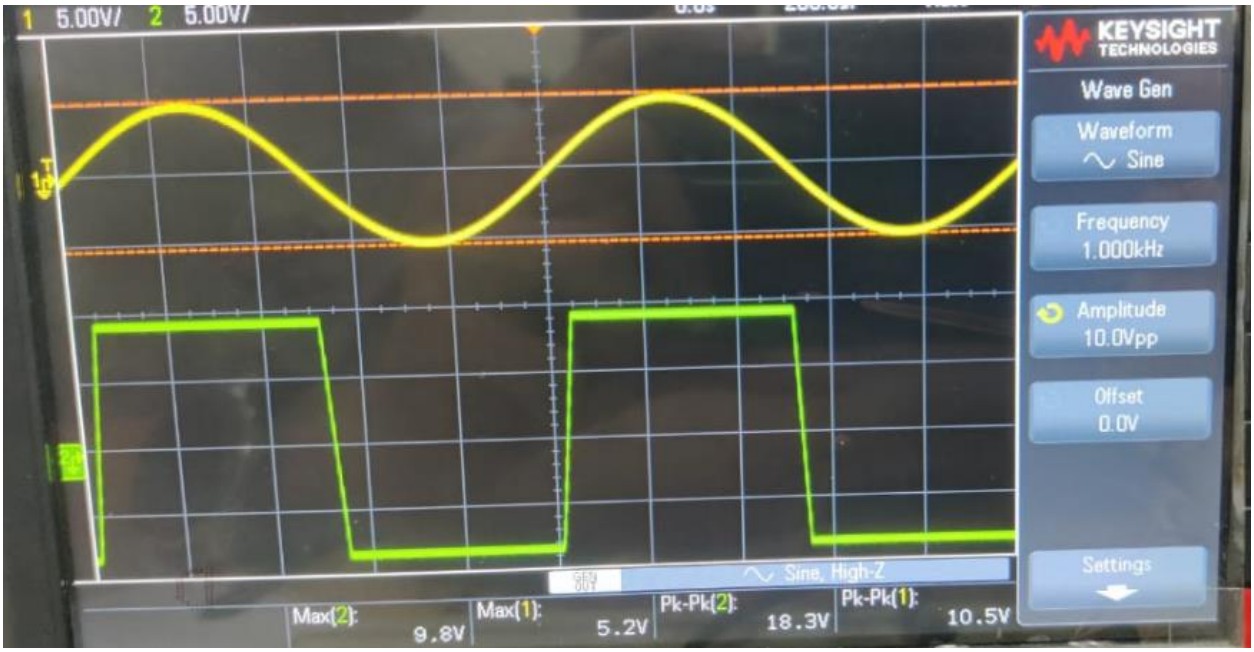
Schematic view of circuit:



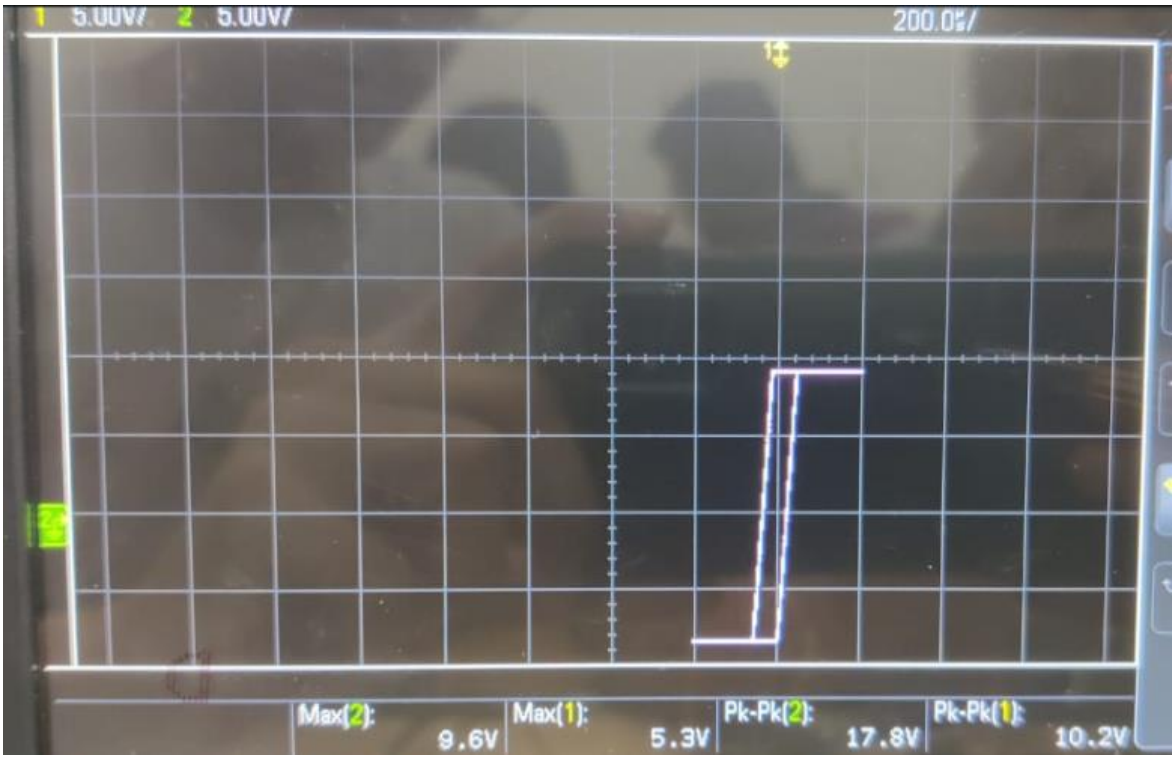
Opamp:



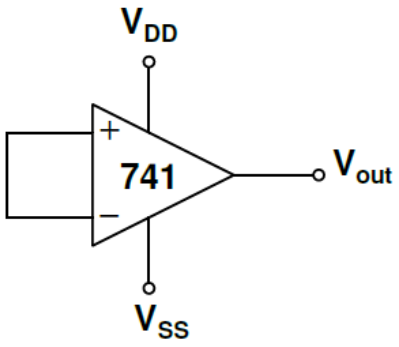
Vin : 10Vpp and frequency = 5 kHz and VDD = 10 V, VSS = −10 V



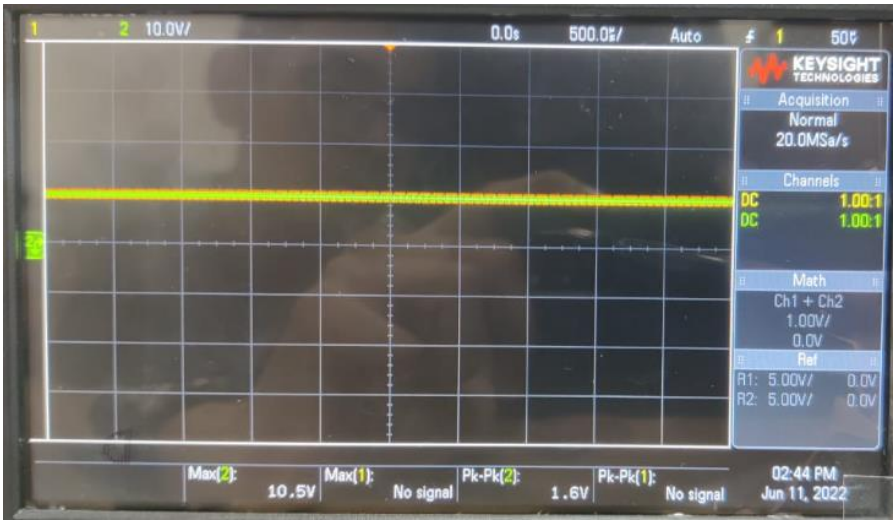
X-Y characteristic:



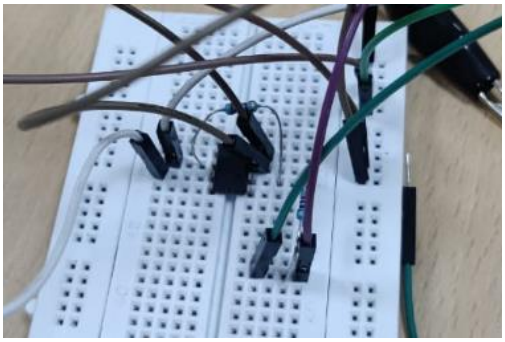
(B)



Output:

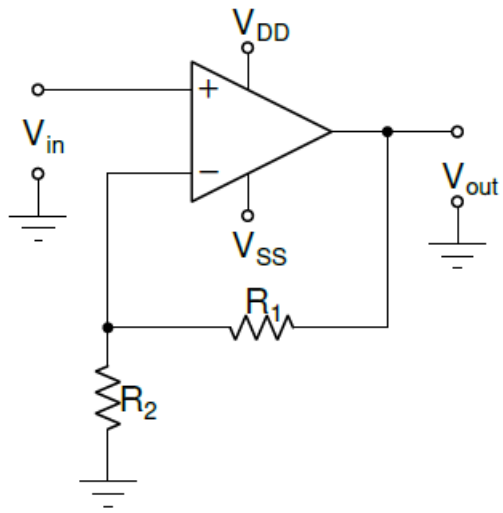


On reducing the DC voltage VDD and VSS to near 0.8V the DC off set in the output reduces to 0.

Circuit: 

3. Non-inverting amplifier

schematic view of the circuit:



(A)
Vin = R2 / R2 + R1 * Vout
Vout/Vin = 1+R1/R2.

Circuit:

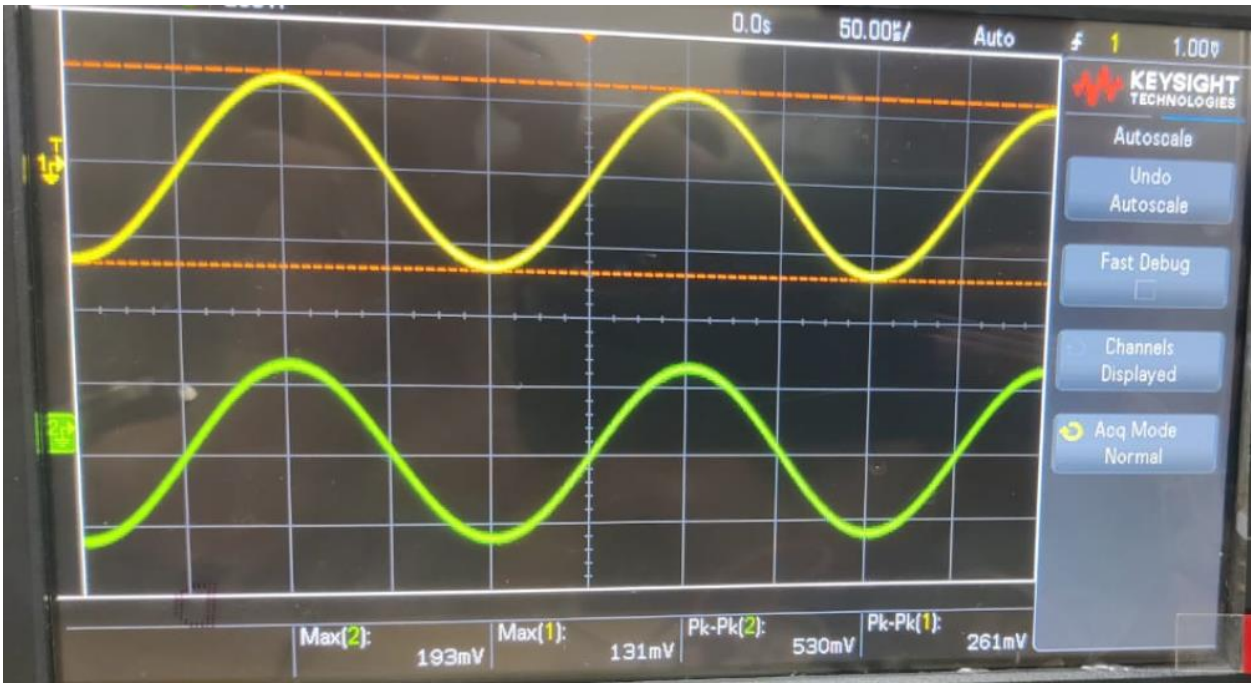
(b) Vin = 250mV and frequency = 5 kHz from the function generator, VDD = 12 V, VSS = −12 V

R1	R2	Vout	Gain(theoretical)	Gain(Practicall)
10K	10K	530mV	2	2.12
10K	4.7K	840mV	3.127	3.218

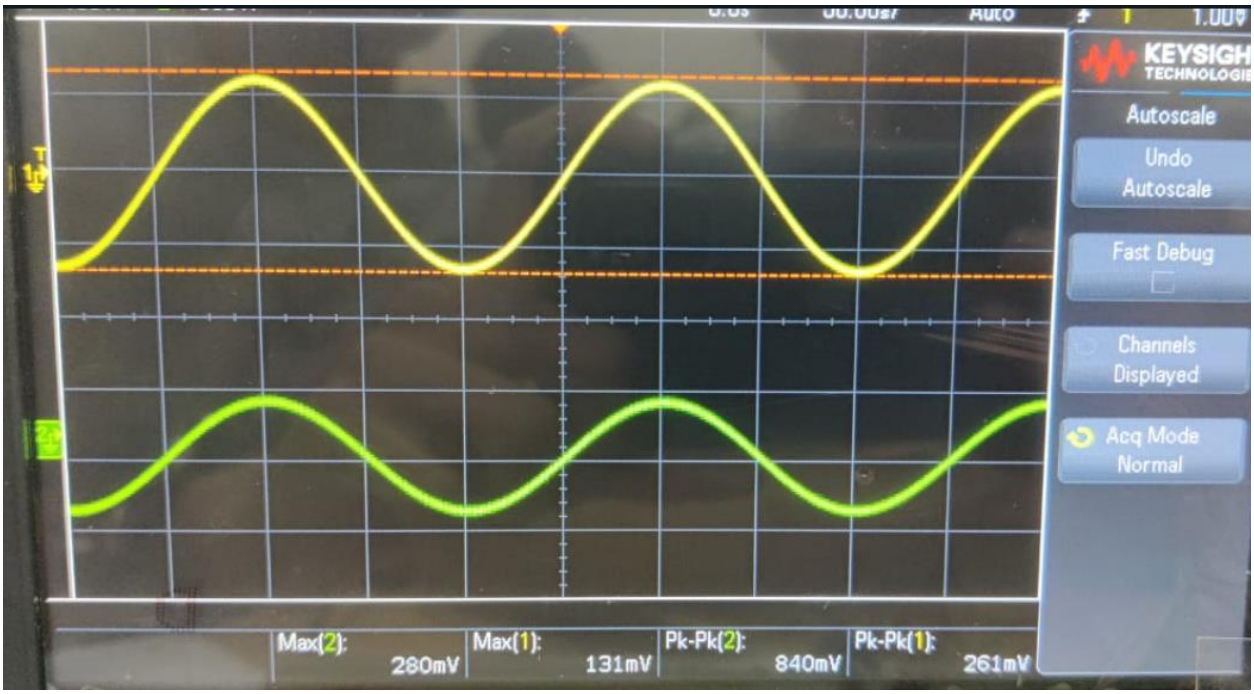
Gain of amplifier when R1 and R2 are shorted is 1.
The voltage follower or unity gain buffer is a special and very useful type of **Non-inverting amplifier** circuit.The use of voltage follower is that it has got very ***high input impedance*** and very ***low output impedance***, which makes it a perfect circuit for ***impedance matching***.

Plots:

R1 = R2 = 10K

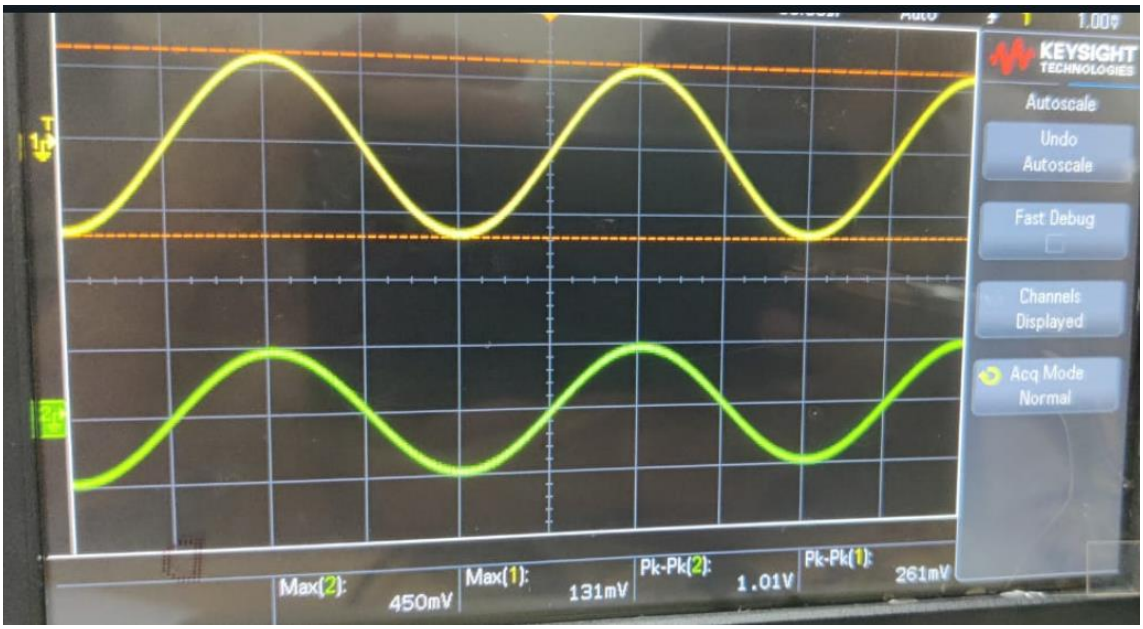


R1 = 10K, R2 = 4.7K

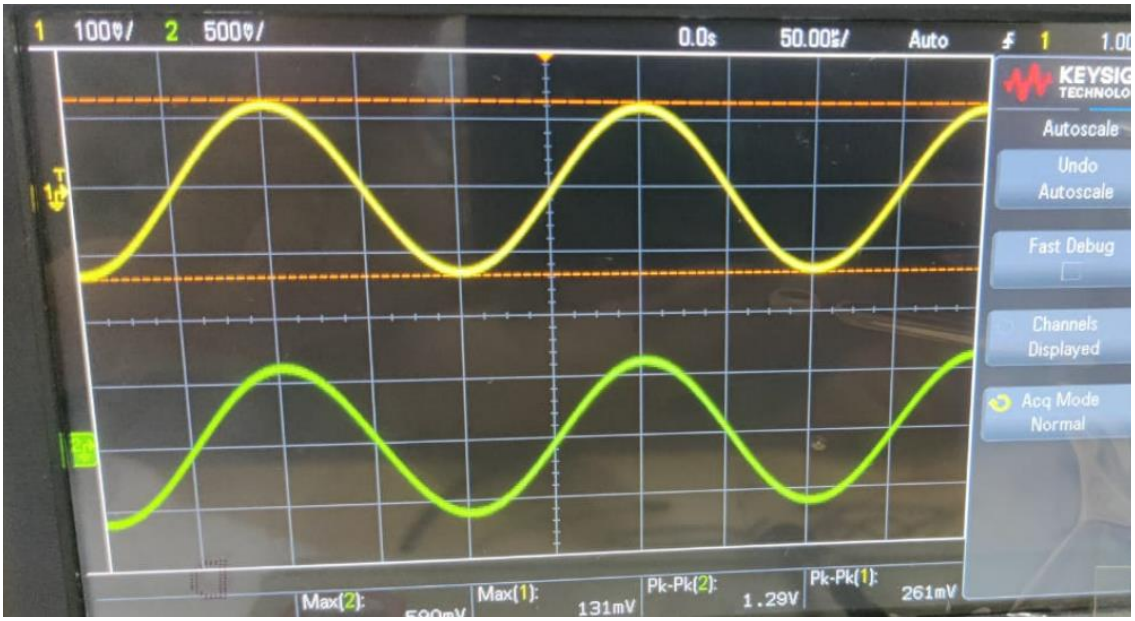


Expected gain	R1	R2	Vout	Gain
4	30K	10K	1.01 V	4.04
5	39K	10K	1.27 V	5.08

R1 = 30K, R2 = 10K

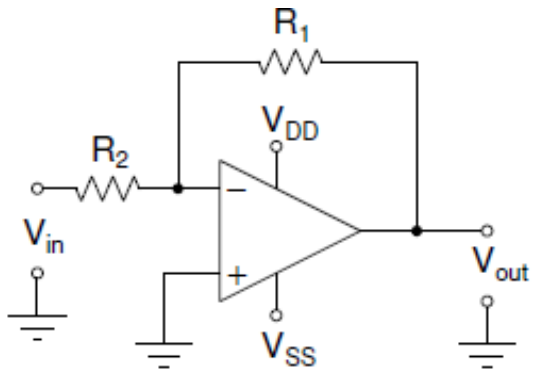


R1 = 39K, R2 = 10K



4. Inverter amplifier

schematic view of the circuit:



Deriving gain relation:

Let current through R2 be i
I = (Vin – Vout) / R2 + R1
Let v2 be voltage at common node of R1 and R2.

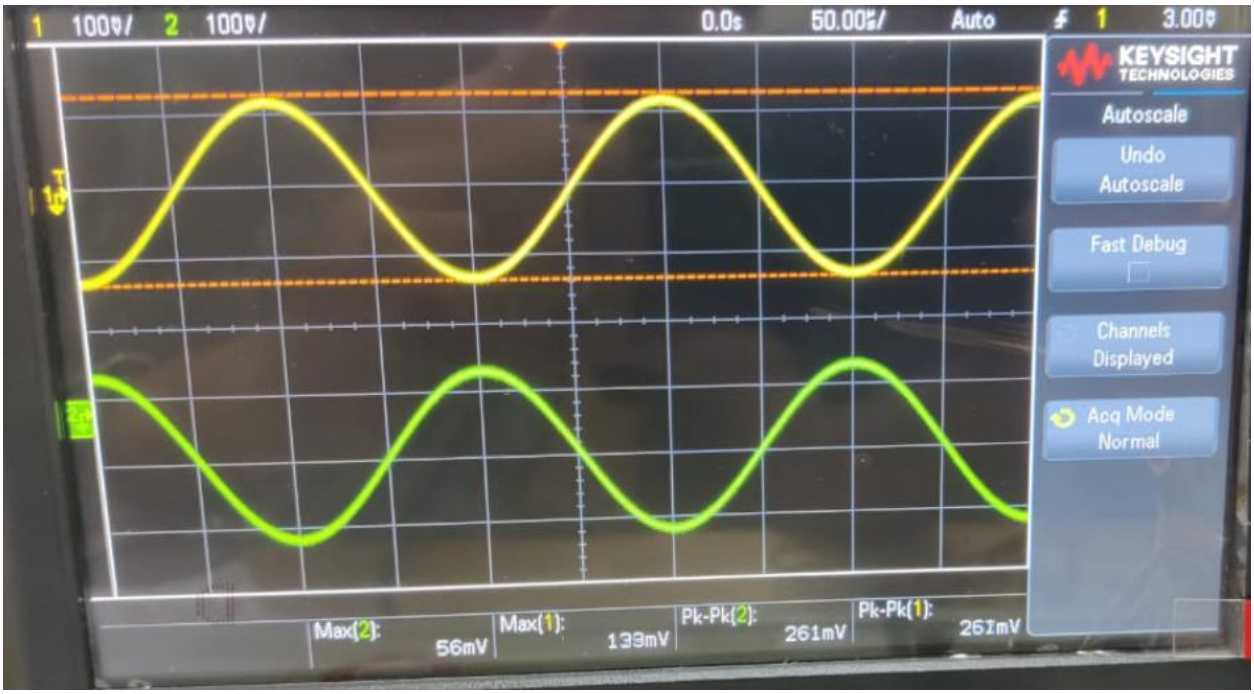
I = (Vin – V2)/Rin = (V2 - Vout)/Rf

Vin / R2 = V2[1/R2 + 1/R1] – Vout/R1
I = (Vin – 0)/R2 = 0-Vout / R1
Vout / vin = -R1 / R2.

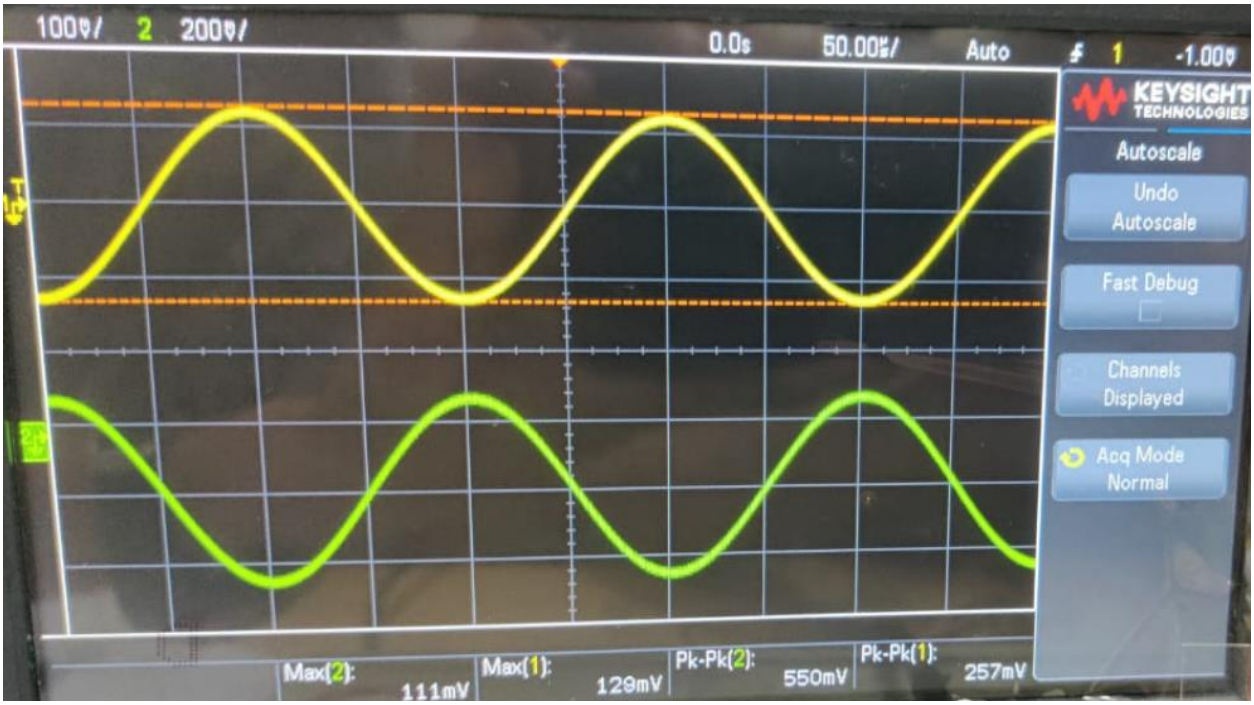
R1	R2	Vout	Gain(Theoretical)	Gain(Practical)
10K	10K	261mV	1	1.044
10K	4.7K	550mV	2.12	2.2

Gain	R1	R2	Vout	Gain(Practical)
4	40K	10K	1.03V	4.12
5	50K	10K	1.33V	5.32

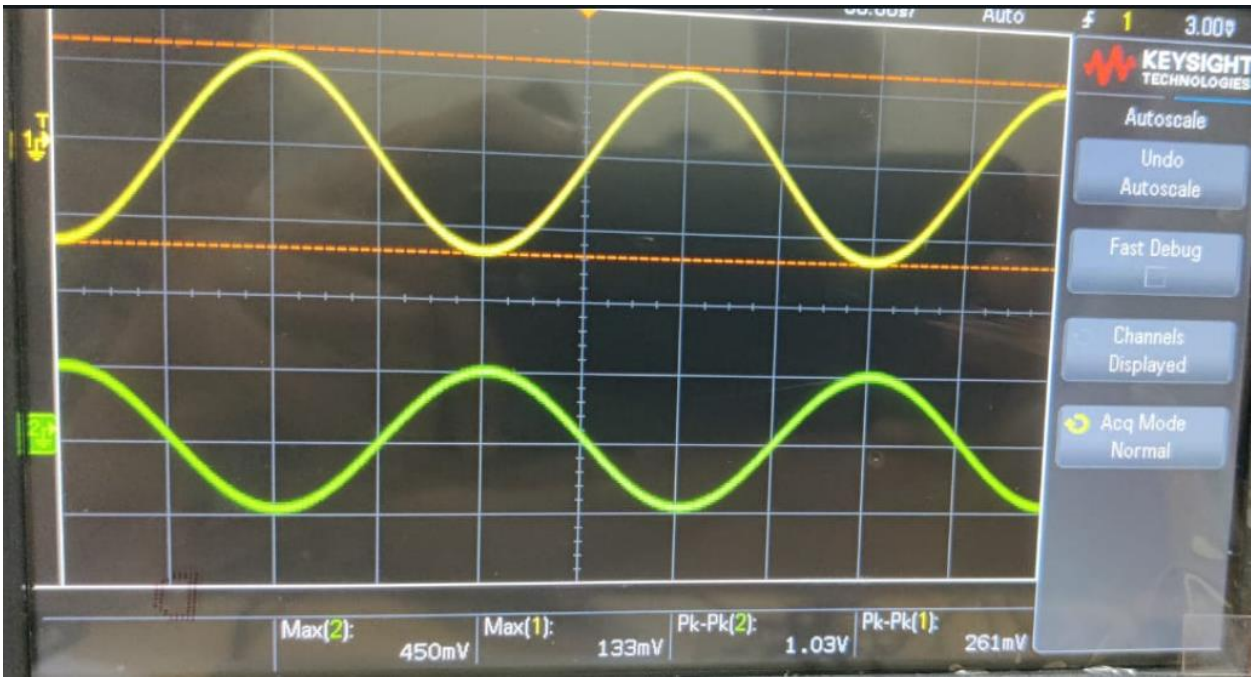
Gain: 1



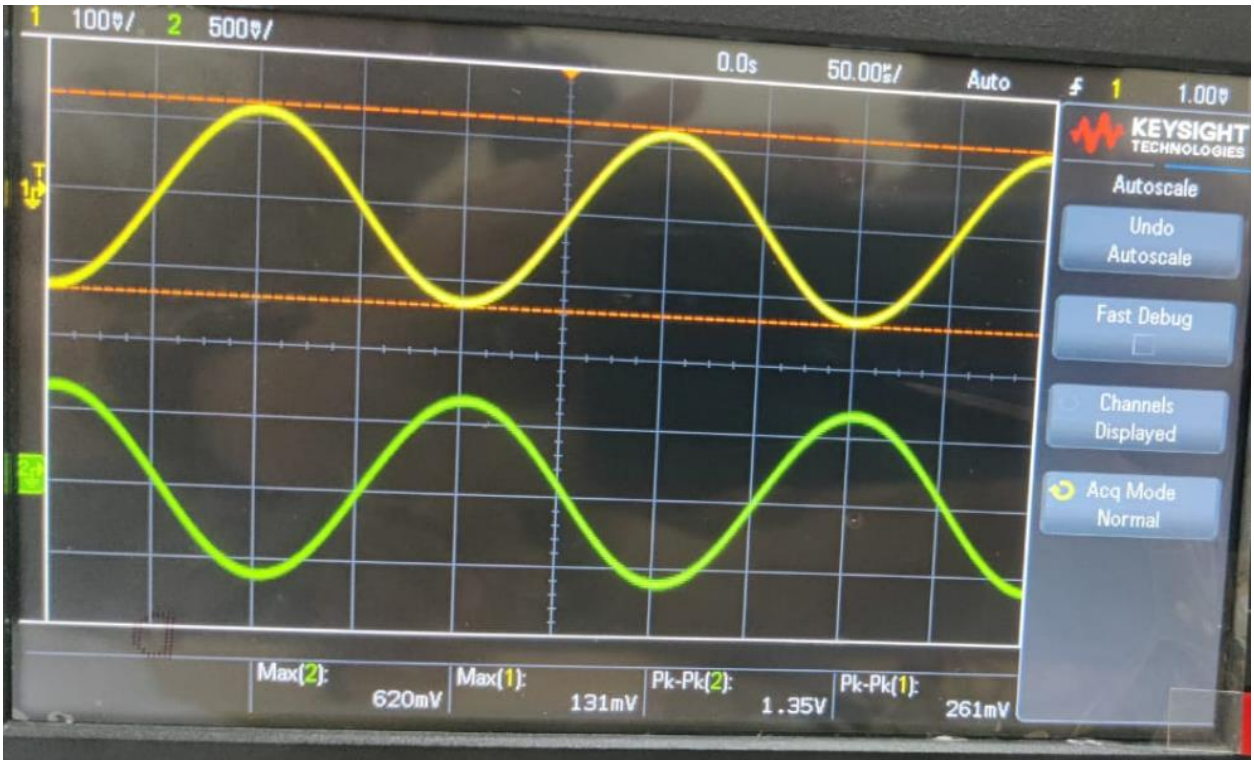
Gain: 2.12



Gain: 4


Auto
1 3.00
KEYSIGHT TECHNOLOGIES
Autoscale
Undo Autoscale
Fast Debug
Channels Displayed
Acq Mode Normal
Max(2): 450mV
Max(1): 133mV
Pk-Pk(2): 1.03V
Pk-Pk(1): 261mV

Gain: 5


1 100mV/ 2 500mV/
0.0s
50.00ns/
Auto
1 1.00
KEYSIGHT TECHNOLOGIES
Autoscale
Undo Autoscale
Fast Debug
Channels Displayed
Acq Mode Normal
Max(2): 620mV
Max(1): 131mV
Pk-Pk(2): 1.35V
Pk-Pk(1): 261mV