VLSI PROJECT REPORT

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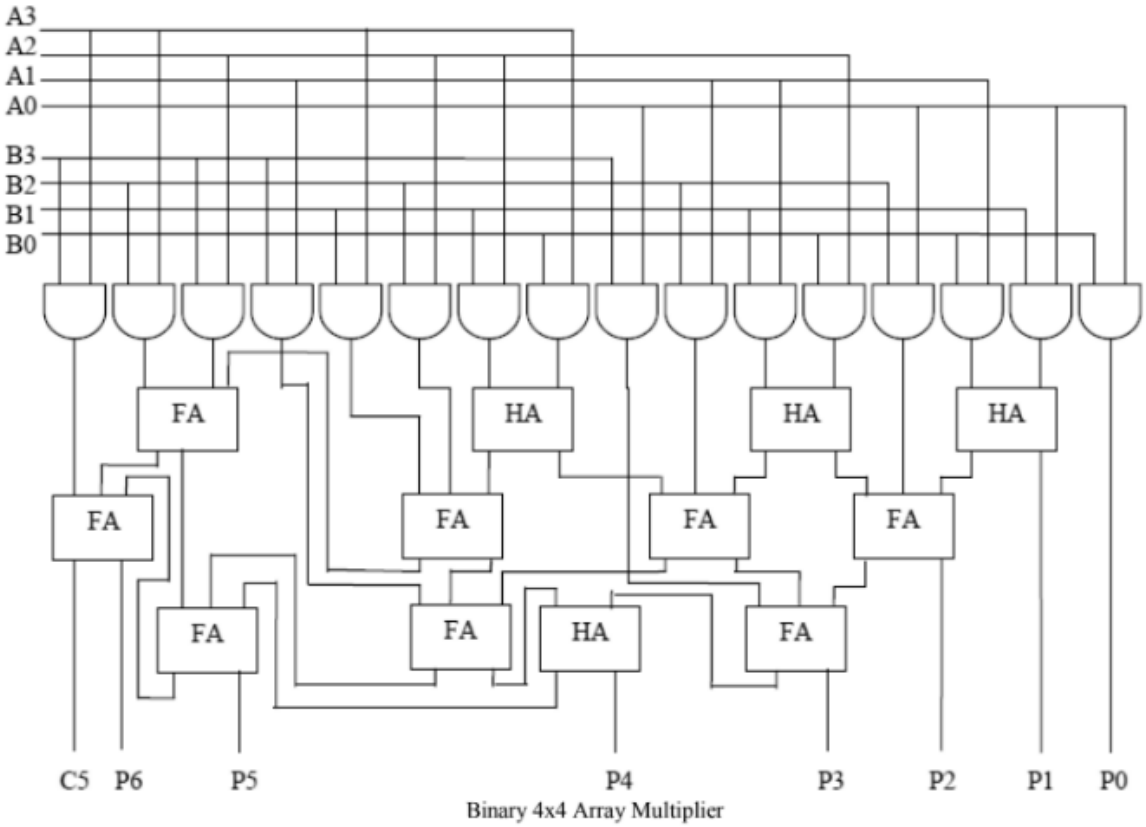
Roll no: 2021102021



Binary 4x4 Array Multiplier

Circuit Diagram used for

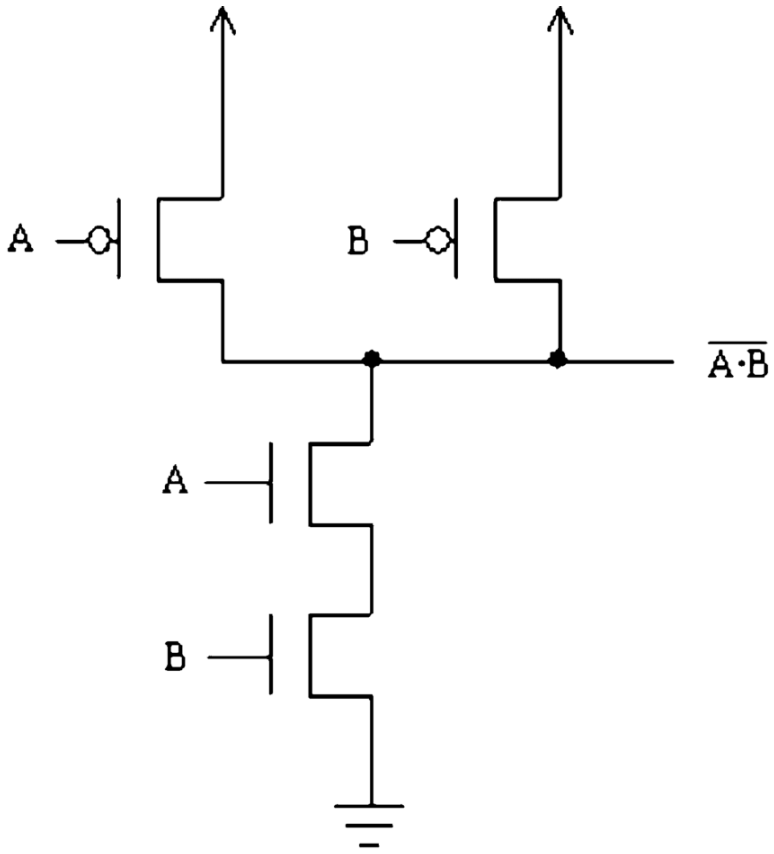
Binary 4x4 Multiplier

Individual Components used (Sub-circuits created)

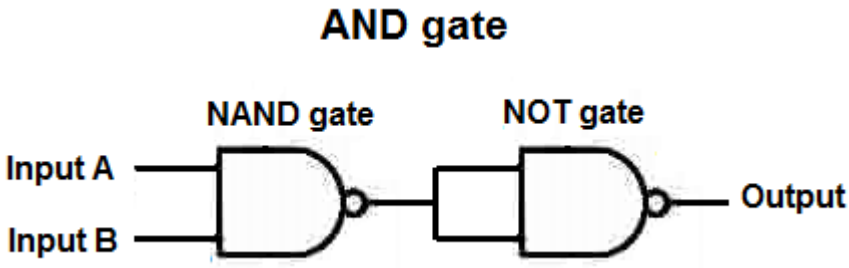
- NAND GATE
- AND GATE
- OR GATE
- XOR GATE
- HALF ADDER
- FULL ADDER

1.NAND GATE

CMOS DESIGN:

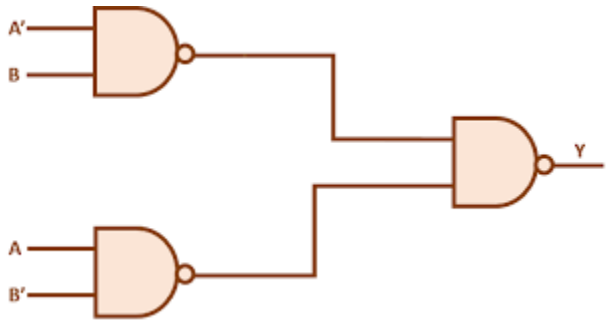


2. AND GATE

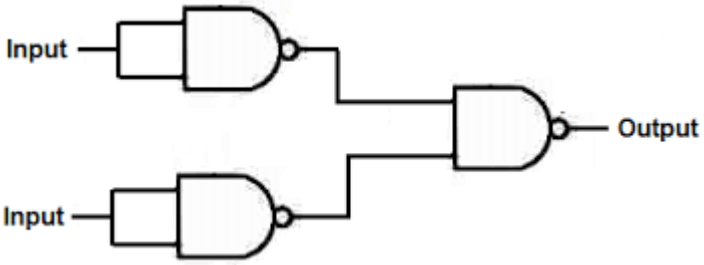


3. XOR GATE

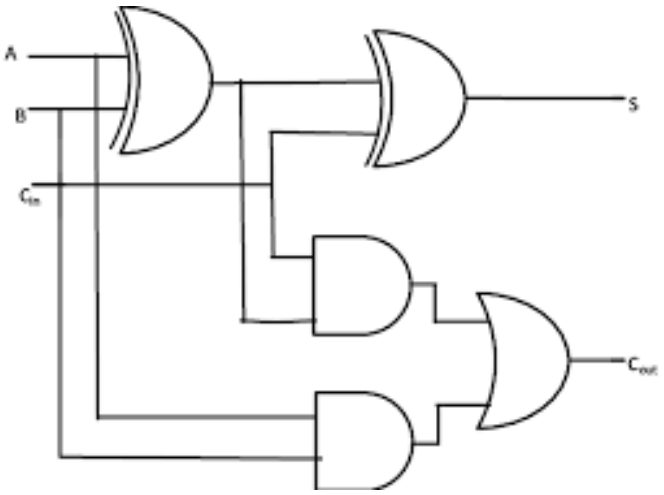
Circuit I implemented:



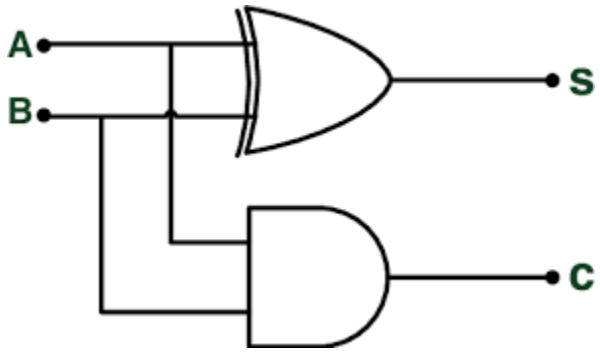
4. OR GATE:



5. FULL ADDER:



6. HALF ADDER:



PRE AND POST LAYOUT RESULTS:

Pre-layout: Results from Ngspice circuit(.cir) file.

Ng-spice circuit file: /Ngspice/circuit.cir.

This file has code to callculate static power and current.

This file should be auto compiled and executed using main.py (a script) file, present in the same directory.

Code to calculate propagation delays is in “delay.cir”.

40 dealys value are stored in delay.txt file in the same directory.

Static power and current are stored in: “result_ngspice.txt”

“delay.txt” in a decreasing sorted order.

Post-layout:

Results from Magic circuit(.mag) file.

Magic circuit file: /Mgspice/NAND.spice.

This file has code to callculate static power and current.

This file should be auto compiled and executed using main.py (a script) file, present in the same directory.

Code to calculate propagation delays is in “delay.cir”.

40 dealys value are stored in delay.txt file in the same directory.

Static power and current are stored in: “result_magic.txt”

“delay.txt” in a decreasing sorted order.

Note: All the other files in Magic and Verilog folder are helper files.

RESULTS:

Leakage Current:

We see that the power in post layout design is of the order 10^{-9} .

The leakage power in the pre layout design which is of the order 10^{-5}

Propagation Delays:

In prelayout design delay is of order 10^{-10} and 10^{-11}

In postlayout design delay is of order 10^{-9} to 10^{-10}

Maximum Propagation Delays:

Pre-Layout: 4.38815E-10

Post-Layout: 4.88815E-09

VERILOG:

The subcircuits used in this are the half_adder.v, full_adder.v, multiplier.v with the test bench main_tb.v

Output is stored in the file “output._verilog.txt”

COMMANDS TO RUN THE FILES:

1. To Run ngspice for power calculation(Pre-Layout)

python3 main.py (In the Ngspice folder)

2. To run ngspice for propagation delay calculation:

-ngspice delay.cir (In the Ngspice folder)

3. To run Magic file:

- magic -T SCN6M_DEEP.09.tech27 NAND.mag

save NAND.mag

extract all

ext2spice -c NAND.spice

(All above commands should be implemented in the Magic folder)

4. To run the spice file extracted from Magic for power calculation

- python3 main.py (Implemented in the Magic folder)

5. To run spice file extracted from magic for propagation delay calculation

-ngspice delay.cir

6.To run the verilog file to verify the results

-python3 main.py (In iverilog folder)