تکلیف 9 درس ریز پردازنده

آریا بنایی زاده 9431029

.1

الف)

تراشه انتخاب شده، تراشه IDT7134SA است.

پارامتر های زمانی

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[3,4]

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Military		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

2720 tbl 09a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	45	—	50	—	50	ns

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5,7]

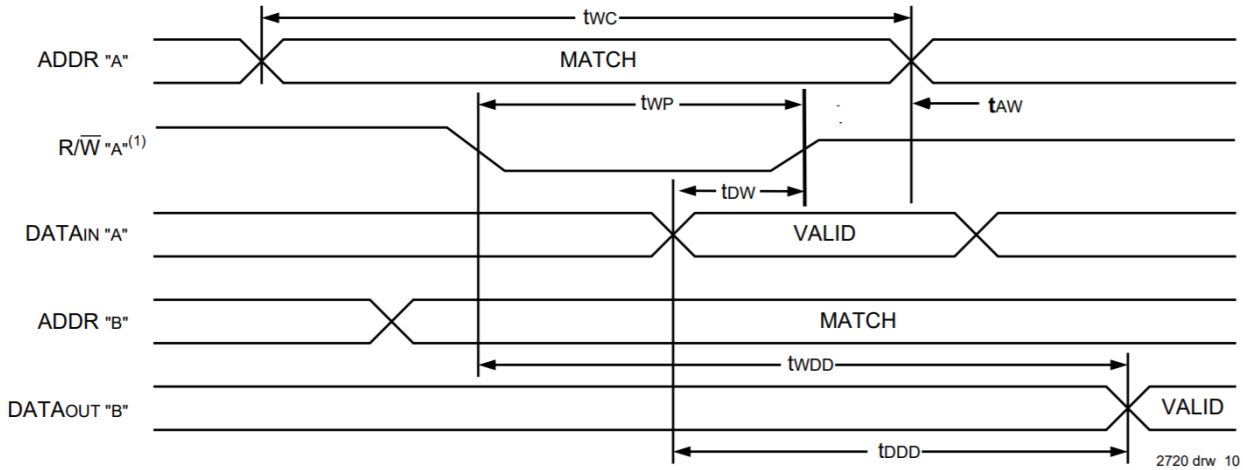
Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Military		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	3	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay[4,6]	—	30	—	30	—	35	ns

2720 tbl 10a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[3]	3	—	3	—	3	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	20	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4,6]	—	45	—	55	—	70	ns

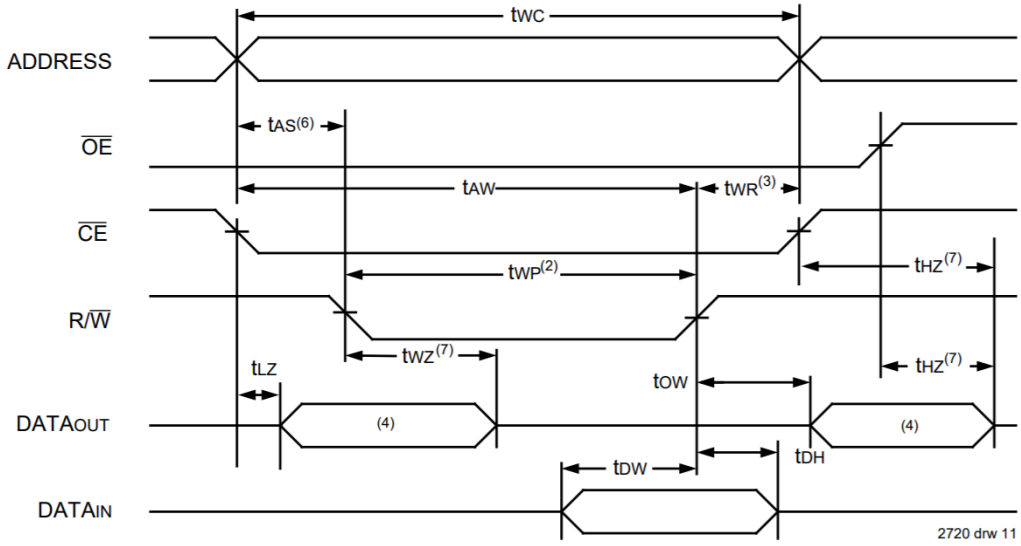
2720 tbl 10b

TIMING WAVEFORM OF WRITE WITH PORT - TO - PORT READ(2,3)

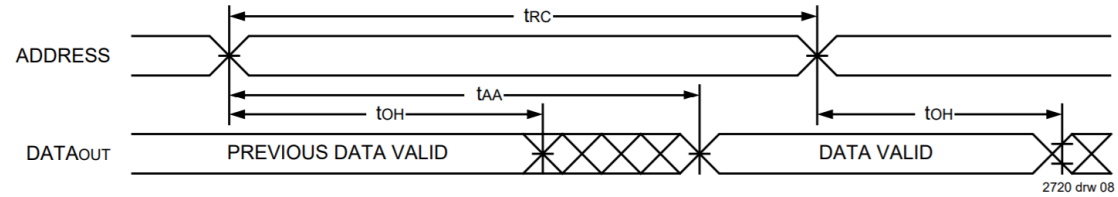


NOTES:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$. $\overline{OE}_{"B"} = V_{IL}$.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)

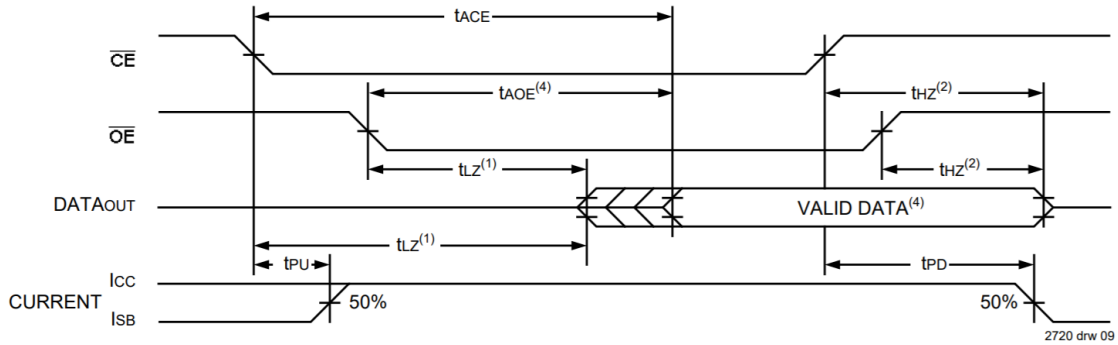


TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1,2,4)



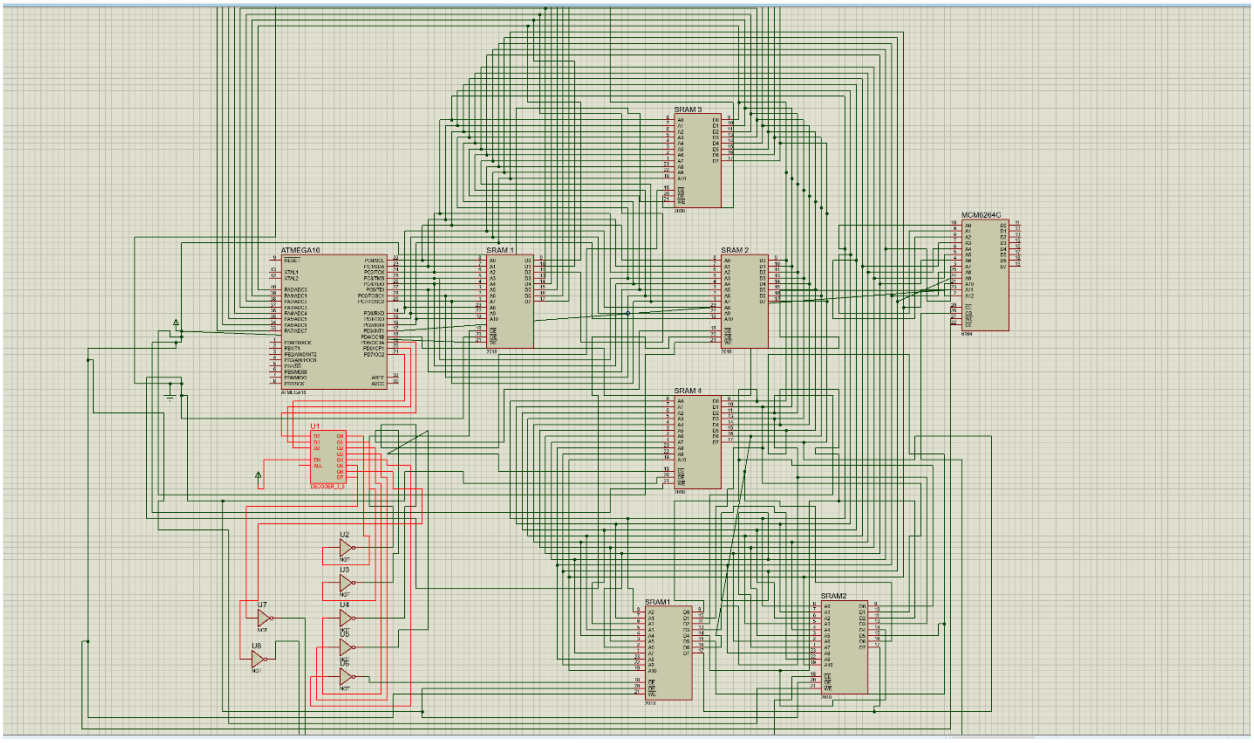
NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH}.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1,3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH}.
4. Start of valid data depends on which timing becomes effective, t_{AOE}, t_{ACE} or t_{AA}
5. t_{AA} for RAM Address Access and t_{SAA} for Semaphore Address Access.

ب)



با توجه به شکل بالا مدار را میبندیم (همچنین فایل شبیه سازی در پیوست قرار دارد)

توجه شود که قطعه 4 کیلوبایتی در هیچ یک از کتابخانه های (در اینترنت و در خود پروتئوس یافت نشد) بنابراین در شکل بالا به جای sram های 4 کیلوبایتی از sram 2 کیلوبایتی استفاده نمودیم اما کلیت شکل با حالت مورد نظر تفاوتی ندارد صرفا اگر قطعا 4 کیلوبایتی را جایگزین کنیم، پایه های A11 را در امتداد پایه های قبل و به PD4 وصل میکنیم.

ج)

با توجه به شکل دیکودر سه به هشت مناسب است

د)

READ

; **Read** Data from Address 0700, SRAM with 20ns tAVQV (Address Access time), Result in R0

LDI R16, 0; Address: Low Byte

LDI R17, 7; Address: High Byte

CALL MemRead

MemRead:

LDI R18, FFH

OUT DDRC, R18 ; PORTC is Output

OUT DDRD, R18 ; PORTD is Output

LDI R18, 00H

OUT DDRA, R18 ; PORTA is Input

OUT PORTC, R16

ANDI R17, 3FH; SRAM #1 Enabled; decoder number should be zero

ORI R17, 0; Read Enabled

OUT PORTD, R17

NOP ; 1NOP=1Clock=62.5ns>tAVQV=20ns

IN R0, PINA

RET

WRITE

; Write Data to Address 1FFFH, SRAM with 20ns tWLWH (Write Pulse width), ; 12ns tDVWH (Data Valid To End of Write), and 0ns tWHDX (Data Hold Time), Data in R20

LDI R16, 0; Address: Low Byte

LDI R17, 40H; Address: High Byte ; 01000000 00000000 ;**5th sram address**

LDI R20, 60H

CALL MemWrite

MemWrite:

LDI R18, FFH

OUT DDRC, R18 ; PORTC is Output

OUT DDRD, R18 ; PORTD is Output

OUT DDRA, R18 ; PORTA is Output

OUT DDRB, R18 ; PORTB is Output

OUT PORTA, R20 ; data

OUT PORTC, R16

ANDI R17, 3FH; ; SRAM #1 Enabled; SRAM #2 Disabled,

ORI R17, A0H; ; Output Disabled, Write Pin=0; OUT PORTB, R17 ;A0

NOP ; 1NOP=1Clock=62.5ns> tWLWH=20ns

SBI PORTB, 0 ; Write Pin=1

NOP ; 1NO ;1Clock=62.5ns> tDVWH=12ns

RET

We به پورت b متصل شده است با توجه به شکل آدرس 4000 شکل در واقع آدرس صفر sram پنجم است بنابراین در برنامه تنظیمات را به این حالت قرار میدهیم(عدد دیکودر باید 4 شود)

.2

حافظه ی برنامه این خانواده عموما از جنس فلش و حافظه رم آن ها SRAM می باشد.

در جدول زیر حجم حافظه ها را بر اساس هر کدام از این ریزپردازنده ها می بینیم.

Mouser Part #	Series	Core	Program Memory Size	Data RAM Size
511-STM32F303VBT6TR	STM32F3	ARM Cortex M4	128 kB	32 kB
511-STM32F051C8T6TR	STM32F0	ARM Cortex M0	64 kB	8 kB
511-STM32F301C8T6	STM32F3	ARM Cortex M4	64 kB	16 kB
511-STM32F303RBT7	STM32F3	ARM Cortex M4	128 kB	32 kB
511-STM32F439BIT6	STM32F4	ARM Cortex M4	2 MB	256 kB
511-STM32F437ZIT7	STM32F4	ARM Cortex M4	2 MB	256 kB
511-STM32F301R6T6	STM32F3	ARM Cortex M4	32 kB	16 kB
511-STM32F765VGT7	STM32F7	ARM Cortex M7	1 MB	512 kB
511-STM32F215VGT7	STM32F2	ARM Cortex M3	1 MB	128 kB
511-STM32F070C6T6TR	STM32F0	ARM Cortex M0	32 kB	6 kB
511-STM32F103ZEH7TR	STM32F1	ARM Cortex M3	512 kB	64 kB
511-STM32F071CBT7TR	STM32F0	ARM Cortex M0	128 kB	16 kB
511-STM32F100RDT7B	STM32F1	ARM Cortex M3	384 kB	32 kB
511-STM32F745VEH6TR	STM32F7	ARM Cortex M7	512 kB	320 kB
511-STM32F437AIH6TR	STM32F4	ARM Cortex M4	2 MB	256 kB