# ECE2031 In-Class Exam      Summer 2014

**Name** _____ **Lab Section** L0__ **Student No.** _____

Fill in all three items above (name, section, student number).  Failure to do so will result in lost points.

Closed Books, Closed Notes, No computers or calculators.

Having read the Georgia Institute of Technology Academic Honor Code, I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times. In addition, I understand my options for reporting honor violations as detailed in the code.


_____          _____
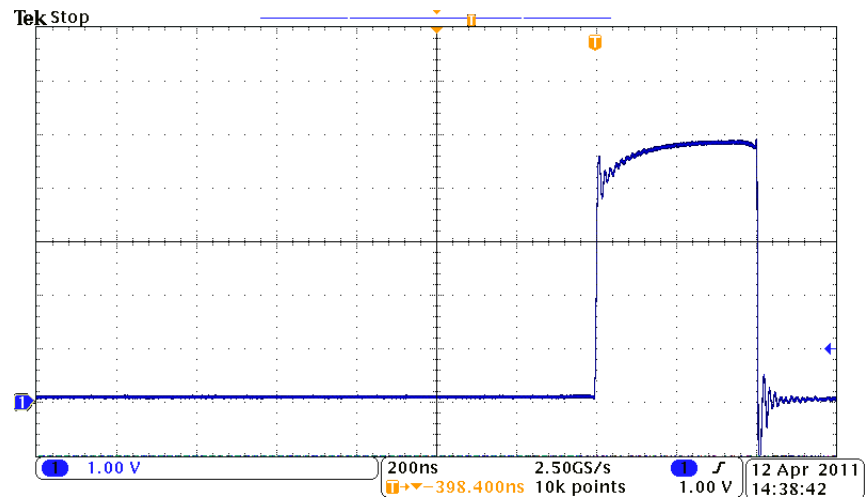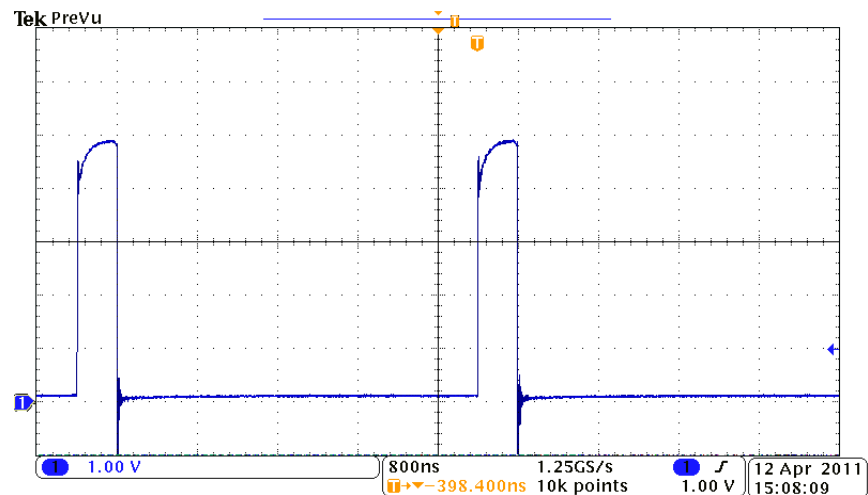
(Signature)                                      (Date)


CIRCLE YOUR SELECTED ANSWERS, FILL IN THE BLANK, OR DRAW AS NEEDED.


EXAMPLE of how to circle an answer (just circle the letter):

| CORRECT | INCORRECT | INCORRECT |
|---|---|---|
| What year is this? (Select one.)<br>a)  2010<br>b)  2031<br>c)  1942<br>**(d)** 2014 | What year is this? (Select one.)<br>a)  2010<br>b)  2031<br>c)  1942<br>(d)  2014 *(circled whole answer)* | What year is this? (Select one.)<br>a)  2010<br>b)  2031<br>c)  1942<br>d) (2014) *(circled number)* |
| INCORRECT | INCORRECT | INCORRECT |
| What year is this? (Select one.)<br>a)  2010<br>b)  2031   *d*<br>c)  1942<br>d)  2014 | What year is this? (Select one.)<br>a)  2010<br>(b)  2031<br>c)  1942<br>(d)  2014 | What year is this? (Select one.)<br>a)  2010<br>b)  2031   *2014*<br>c)  1942<br>d)  2014 |

1. (5 pts) What is the positive duty cycle of the waveform below? It has been acquired at two different scales to assist you. You may assume that the 0% level is 0.1 V, and the 100% level is 4.9 V. The arrow to the left of the waveform indicates the ground level, and the scales are displayed.

a) 90%

b) 7%

c) 10%

d) 25%

e) 800 ns

Tek PreVu

1.00 V    800ns    1.25GS/s    ♪  12 Apr 2011
T→▼−398.400ns  10k points   1.00 V  15:08:09

Tek Stop

1.00 V    200ns    2.50GS/s    ♪  12 Apr 2011
T→▼−398.400ns  10k points   1.00 V  14:38:42

2. (5 points) The train controller state machine (TCONTROL.VHD) designed in Lab 6 could direct a train to move at different forward speeds.

a) TRUE

b) FALSE

3. (5 pts) Quartus defines something called a "top-level entity," or a "top-level design file." What best describes the role of the top-level entity? (Select one.)

a) It is the only block diagram file in a project.

b) It is where the designer describes the entire project, possibly making reference to other design files.

c) It is the file that stores all simulation data

d) It is the file that is programmed directly into the FPGA.

4. (10 pts) When SCOMP executes an OUT to an addressed I/O device (such as the LEDs), which of the following must be true? (Select ALL that apply.)

   a) IO_WRITE must never be high at the same time that IO_CYCLE is high

   b) At some point, SCOMP must use its tri-state buffers to drive the IO_DATA bus with the value of the accumulator

   c) After IO_CYCLE goes high, the addressed I/O device must drive the IO_DATA bus with valid data until IO_CYCLE goes low

   d) All non-addressed I/O devices must drive the IO_DATA bus with 0x0000

   e) At some point, the addressed I/O device must latch the data that is on the IO_DATA bus

5. (5 points) A vector or group of associated signals is also called a

   a) Functional assembly

   b) Concurrent process

   c) Bus

   d) Boolean

   e) ASM

6. (5 points) Suppose that you have a version of the simple computer (a top-level BDF file, with SCOMP, I/O devices, etc. similar to that of Lab 8). But you find that a simple program which reads the slide switches and displays their state on the LEDs does NOT work at all. It compiles fine, downloads (programs) fine, but the LEDs never change. What would be reasonable steps to debug this system? SELECT ALL THAT APPLY, either by themselves or in combination with other steps, and regardless of the order in which you may try them.

   a) If another DE2 board is available, try it.

   b) Create and run a program that displays one or more known patterns on the LEDs, to verify that SCOMP runs and that it outputs correctly to the LEDs.

   c) Recompile and redownload until it behaves differently.

   d) Create a trivial schematic (BDF) that connects individual slide switches to individual LEDs, and make sure that when compiled and downloaded, each switch really does control an LED.

   e) Verify that the pin assignments of the project are correct.

7. (5 points) In VHDL, within a single ARCHITECTURE block, it is possible to have two different assignment statements that assign a value to the same signal under what conditions? (Select any or all that apply.)

   a) Within a PROCESS statement

   b) Anywhere

   c) Anywhere outside of a PROCESS statement

   d) In the PORT statement

   e) In the USE statement
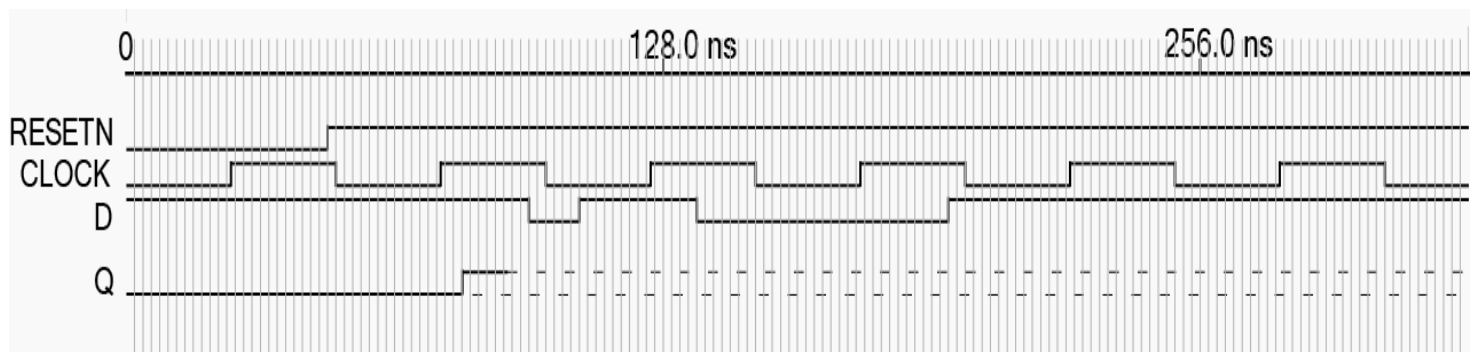
8. (5 pts) The figure above shows a positive edge-triggered D flip-flop with an asynchronous active-low reset, clocked at an acceptable rate below its maximum frequency. Everything up to the beginning of the dashed line on Q is correct. The propagation delay of the flip-flop is about two of the vertical grid intervals, as shown for the first Q transition. Using approximately that same propagation delay, draw in the expected behavior of Q up to the end of the simulation. (You can draw this badly for full credit, but there has to be some approximation of the delay!)

9. (5 pts) Suppose that you wanted to create an instruction for SCOMP called ABS that would take the absolute value of the accumulator, and put the result in the accumulator. Which of the following would most closely accomplish that, assuming that the decode stage correctly transitions to the EX_ABS stage for execution?

(AC is accumulator, MEM_ADDR is memory address register, and MDR is memory data register. You must pick the one best answer, even if you think you see a minor error.)

```
a) WHEN EX_ABS =>
     IF AC < 0 THEN
       MEM_ADDR <= AC(9 DOWNTO 0);
       STATE <= EX_ABS2;
     ELSE
       STATE <= FETCH;
     END IF;
   WHEN EX_ABS2 =>
     AC <= -MDR;
     STATE <= FETCH;

b) WHEN EX_ABS =>
     IF AC(1) < '0' THEN
       AC <= -AC;
     END IF;
     STATE <= FETCH;

c) WHEN EX_ABS =>
     IF AC(15) = '1' THEN
       AC <= NOT(AC) + 1;
     END IF;
     STATE <= FETCH;

d) WHEN EX_ABS =>
     MDR <= AC;
     IF MDR < 0 THEN
       AC <= -MDR;
     END IF;
     STATE <= FETCH;
```

10. (5 points)  In Lab 2 it was mentioned that real mechanical switches "bounce." The VHDL code for a switch debouncer is shown below, where the input  sw is assumed to be connected to a switch such as one of those on the DE2, and the debounced output appears at sw_debounced.  How does this work? (Select one answer.)

    a)  It averages successive values of the input sw

    b)  It ANDs the input sw with an external clock signal that knows when the switch is valid

    c)  It samples the input sw four times and only produces a low output when four successive samples are low.

    d)  It compares one switch with another switch many times

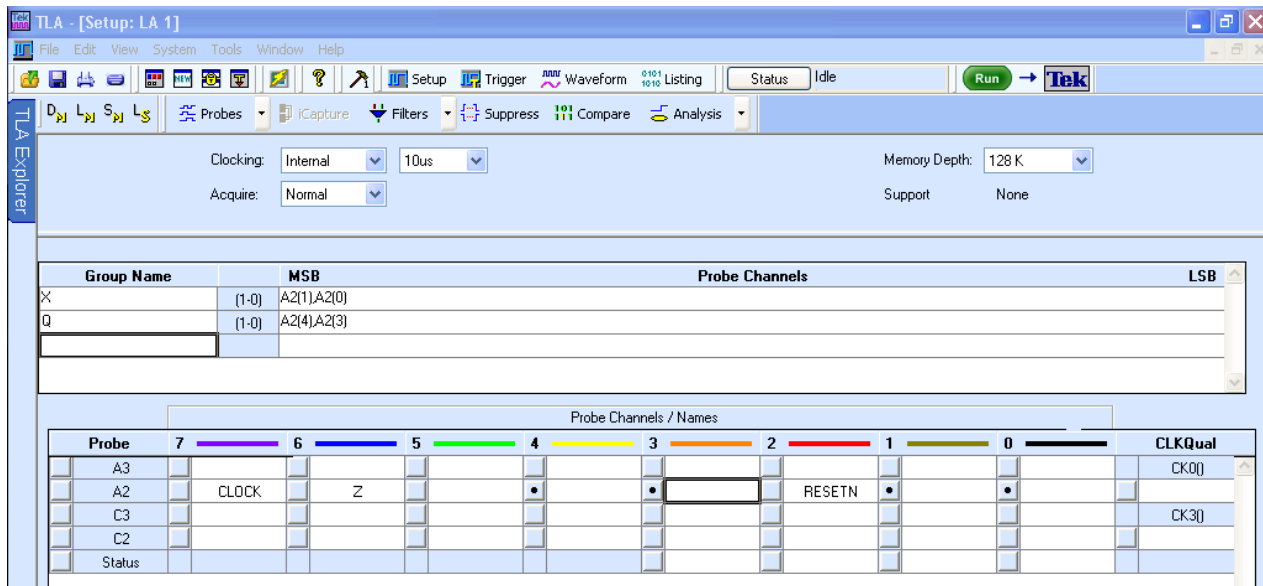    e)  None of the above

```
LIBRARY IEEE;
USE  IEEE.STD_LOGIC_1164.all;

ENTITY debouncer IS
    PORT( sw, clock_100Hz : IN    STD_LOGIC;
          sw_debounced, swcopy    : OUT     STD_LOGIC);
END debouncer;

ARCHITECTURE a OF debouncer IS
    SIGNAL shift_sw    : STD_LOGIC_VECTOR(3 DOWNTO 0);
BEGIN
    -- Debounce clock should be approximately 10ms or 100Hz
    PROCESS (clock_100Hz)
    BEGIN
        IF (clock_100Hz'EVENT) AND (clock_100Hz = '1') THEN
            shift_sw(2 DOWNTO 0) <= shift_sw(3 DOWNTO 1);
            shift_sw(3) <= sw;
            IF shift_sw(3 DOWNTO 0)="0000" THEN
                sw_debounced <= '0';
            ELSE
                sw_debounced <= '1';
            END IF;
     END IF;
    END PROCESS;
    swcopy <= sw;
END a;
```

11. (5 points)  Refer again to the debouncing code above.  The signal swcopy seems to be what its name implies, a copy of the signal sw.  When does swcopy change its value? (Select one answer.  Any references to the "clock" mean the signal clock_100Hz.)

    a)  Immediately after sw changes (as quickly as possible, given propagation delays in the device)

    b)  One rising clock edge after sw changes

    c)  One falling clock edge after sw changes

    d)  Never

**TLA - [Setup: LA 1]**

File  Edit  View  System  Tools  Window  Help

Setup  Trigger  Waveform  Listing  | Status | Idle  | Run → Tek

Probes  ▾  iCapture  Filters  ▾  Suppress  Compare  Analysis  ▾

Clocking: Internal ▾  10us ▾          Memory Depth: 128 K ▾

Acquire: Normal ▾                    Support      None

| Group Name | | MSB | Probe Channels | LSB |
|---|---|---|---|---|
| X | (1-0) | A2(1),A2(0) | | |
| Q | (1-0) | A2(4),A2(3) | | |
| | | | | |

Probe Channels / Names

| Probe | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | CLKQual |
|---|---|---|---|---|---|---|---|---|---|
| A3 | | | | | | | | | CK0() |
| A2 | | CLOCK | Z | • | • | | RESETN • | • | |
| C3 | | | | | | | | | CK3() |
| C2 | | | | | | | | | |
| Status | | | | | | | | | |

12. (5 points) For the example logic analyzer setup shown above, which probe was used for the least significant bit of X (i.e., X[0])?

   a) Probe Channel 1 on Connector A2

   b) Probe Channel 0 on Connector A2

   c) Probe Channel 3 on Connector A2

   d) Probe Channel 2 on Connector A3

   e) None of the above

13.  (5 pts) Near the end of Lab 4, you experimented with a large counter that failed to operate correctly.  What made it fail?  (Select one.)

   a) It did not have enough power

   b) It was not large enough to hold the required count value

   c) It was overclocked

   d) There was a flaw in the state machine that implemented counting

   e) None of the above

Refer to the following description and accompanying code for problems 14 and 15.

A student has a working SCOMP, with the Timer connected to a 10 Hz clock (as it was in Lab 8), with the following program running on it.  The I/O constants in the EQU statements of the program are correct.  The LEDs, as always, are active-high (they light when a '1' is OUT'ed to them).   &B indicates that the number that follows is binary, just as &H is used to designate hexadecimal numbers.

```
                ORG             &H00
                OUT             Timer
First:          LOAD            Zero
                SUB             One
                OUT             LEDS
Check:          IN              Timer
                AND             BitThree
                JZERO           First
                LOAD            Zero
                OUT             LEDS
                JUMP            Check

; Constants in memory
Zero:           DW              &H0000
One:            DW              &H0001
BitZero:        DW              &B0000000000000001
BitOne:         DW              &B0000000000000010
BitTwo:         DW              &B0000000000000100
BitThree:       DW              &B0000000000001000

; IO address space map
SWITCHES: EQU &H00   ; slide switches
LEDS:     EQU &H01   ; red LEDs
TIMER:    EQU &H02   ; timer, usually running at 10 Hz
```

14. (5 points) What is the first pattern displayed on the Red LEDs 0-15 (immediately prior to the "Check" label)?

    a) Only a single LED is on                 b) All LEDs 0-15 are off
    c) Only a single LED is off                d) All LEDs 0-15 are on
    e) Depends on where "Zero" is placed in memory

15. (5 points) What does the previous code do?  (Select the single best answer, ignoring any possible syntax errors which would be corrected, etc.)

    a) Displays a specific LED pattern until one thousand seconds have passed, then displays a different LED pattern

    b) Displays the same LED pattern all the time.

    c) Displays a specific LED pattern for less than a second, then displays another pattern for less than a second, and continues alternating patterns as long as the computer runs.

    d) Displays a specific LED pattern for about three seconds, then displays another pattern for a shorter period of time, and continues alternating patterns as long as the computer runs.

16. (10 points) Recall the sequence detector used as an example state machine, producing a Z output of 1 only when two or more consecutive X input values of 1 occurred. Draw a UML statechart for a sequence detector where the output Z is 1 only when the four most recent X input values have been 0, 1, 0, 1. (Specifically, just as with the example sequence detector, Z changes to 1 upon entry to a state just as the sequence is detected.)

Use the existing "Start" state without changing anything. Add as many states as you need (but no more than needed), giving each of them a unique name. Define the value of the Moore output Z in the same manner as is done in the Start state. Label every transition arc with X=0 or X=1, unless you want the transition to be unconditional.
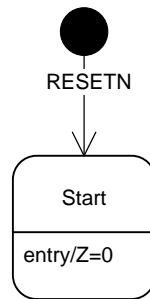
17. (10 points) What is the minimal sum of products expression that is logically equivalent to the following circuit? Use a Karnaugh map if you find it useful or necessary, and you can use the space on the bottom of the page.
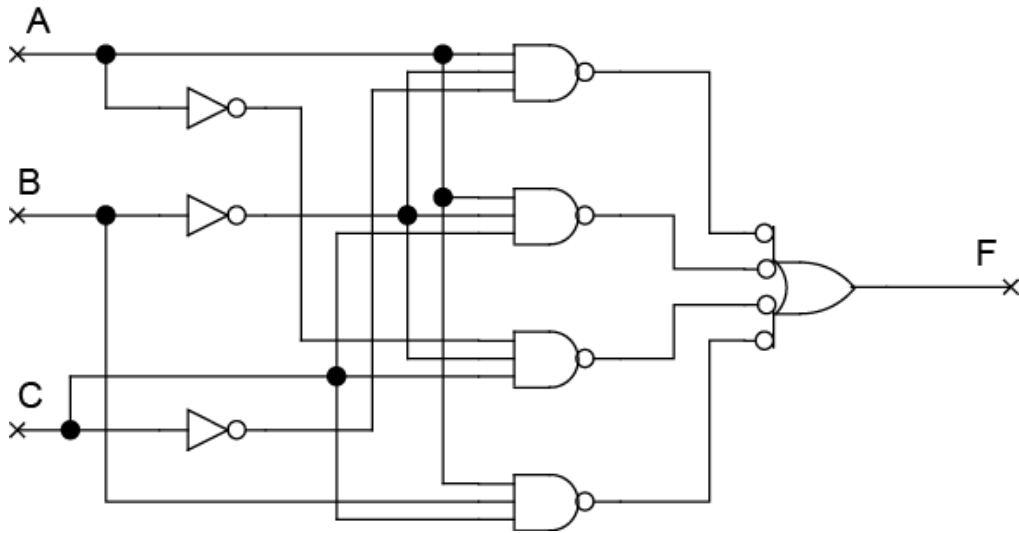


Write your answer in a form similar to this: $F = ABC + \overline{A}\,\overline{B}\,\overline{C}$ (Use BARS for complemented variables.)

F = _____