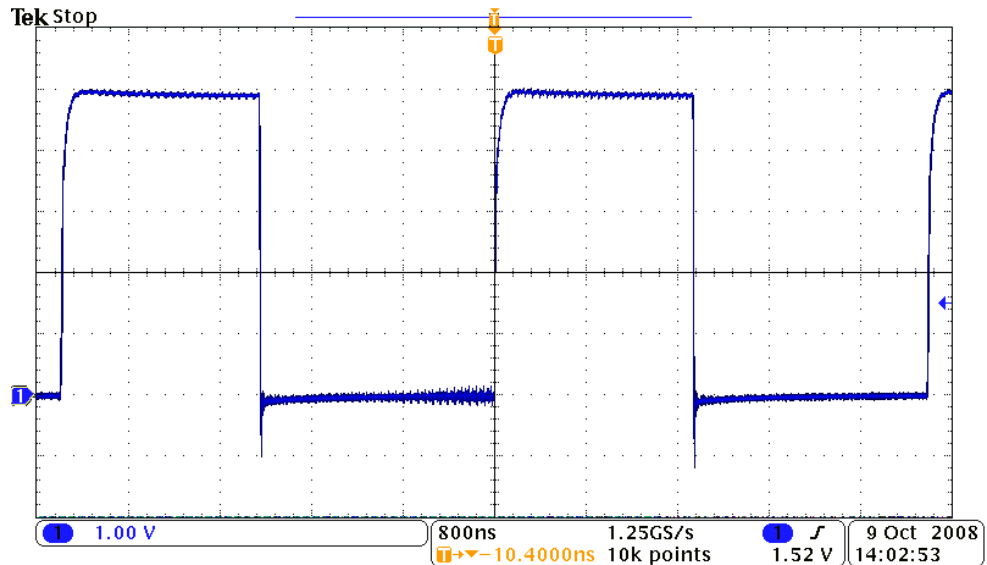


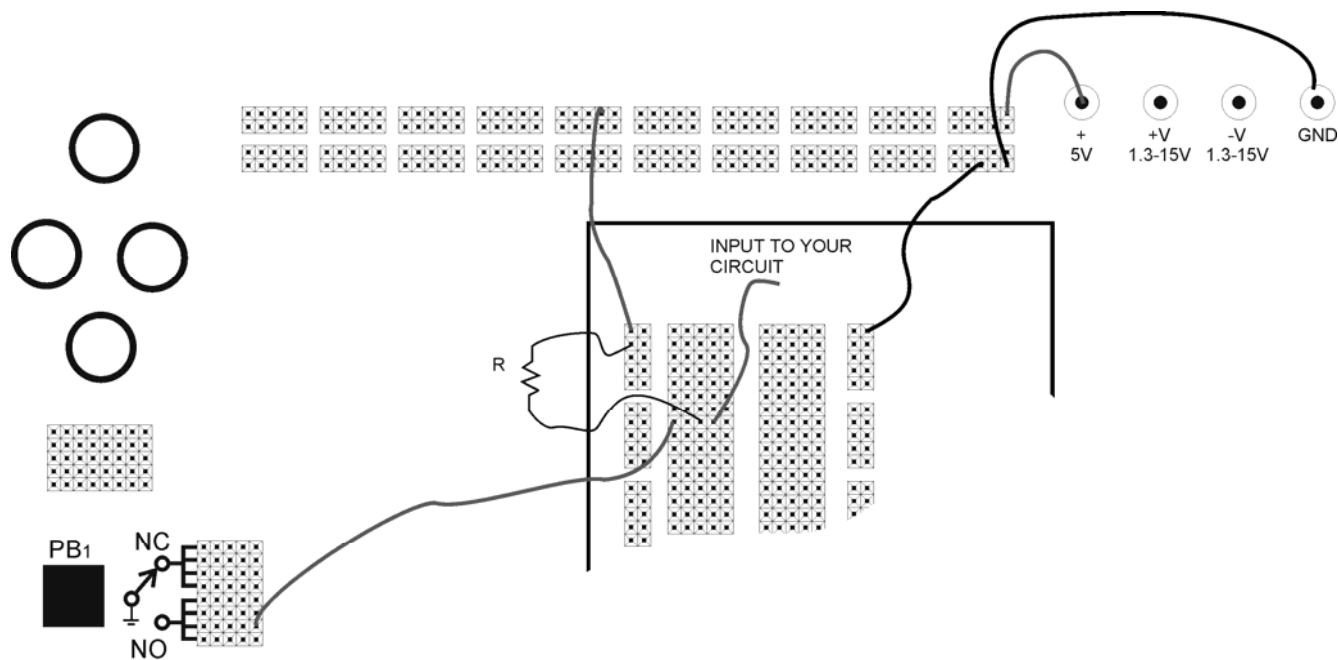
**Closed Books, Closed Notes, No computers or calculators.**  
**Mark all answers on the answer sheet.**

1. (5 pts) What is the positive duty cycle of the signal shown below? The arrows next to the waveform indicate the ground levels, and the scales are displayed (1.00 V/division, 4.00 ns/division)

- a) 2.4 ns
- b) 1.25 GS/s
- c) 46%
- d) 4.9 V
- e) 10%



2. (10 pts) Which of the following are minterms of the SOP expression  $F = A + \overline{B}C + \overline{A}C$  ? Recall that minterms correspond to individual cells of a Karnaugh map. (Select all that apply.)
- a)  $A \overline{B} \overline{C}$
  - b)  $A$
  - c)  $A B C$
  - d)  $\overline{B} C$
  - e)  $\overline{A} \overline{B} C$
3. (5 pts) In Lab 3, an appendix provided information about “propagating values” and “controlling values,” which were used to set up test conditions for measuring your worst-case propagation delay. What is the controlling value for an OR gate (the value on one input that controls the output, independent of the other input)?
- a) 0
  - b) 1
  - c) High-impedance
  - d) None of the above



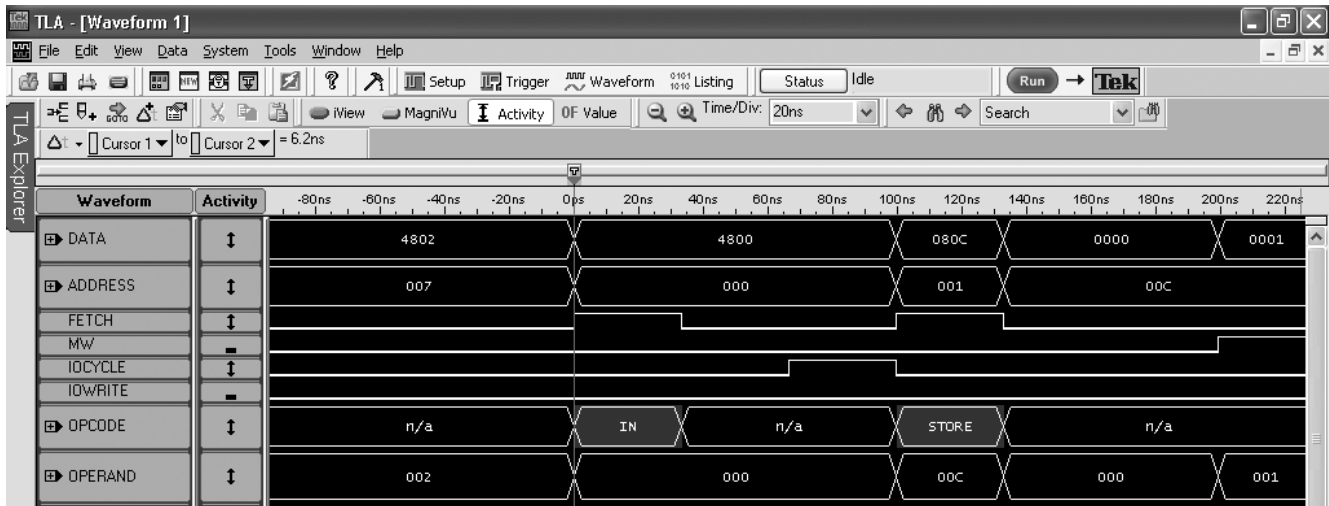
4. (5 pts) The picture above shows a depiction of the CADET workstation with a protoboard, wiring, and a resistor. Which of the following are correct statements **AS IT IS WIRED HERE**? You may assume that the CADET is powered on, and that the “input to your circuit” goes to a normal TTL-compatible input pin. (Select only one answer.)
  - a) There is a short between power and ground
  - b) Under the assumption that pushing PB1 produces the “active” level, the switch is wired as an “active-low” switch.
  - c) The resistor is not needed, and the “input to your circuit” would work just the same if the resistor were simply pulled out of that protoboard.
  - d) The resistor is needed for making a connection, but it could be replaced with a wire (a direct connection instead of a resistance).
  - e) Moving (unplugging and reconnecting) the wire from the “NO” region of PB1 to the “NC” region of PB1 will short power and ground.
5. (5 pts) Suppose you just implemented an eight-bit counter in a device like the Cyclone chip on the DE2 board, and you have access to all eight bits (i.e., you can probe them). If you wanted to see if it was counting properly, it would be most effective to use which of the following tools? (Select one.)
  - a) A logic probe
  - b) An oscilloscope similar to the one in the lab
  - c) A logic analyzer similar to the one in the lab
  - d) A voltmeter
  - e) None of these are useful

6. (5 pts) Suppose you just saw the Quartus warning: *Info: Automatically selected device <dev\_name> for design <proj\_name>*, where <dev\_name> and <proj\_name> are the name of an Altera device and the name of your project, respectively. What is the cause of this warning? (Select one.)
- a) One of the design files listed as part of your project is missing
  - b) The “init\_file=” parameter of a GENERIC MAP for an altsyncram device specifies a non-existing file
  - c) You chose “Save As” under “File” and gave the name of an existing file.
  - d) You started a compilation, but had not previously specified a particular target FPGA
  - e) You named a bus with an invalid name, and Quartus chose a different name

```
PROCESS (reset, clock)
BEGIN
    IF reset = '1' THEN
        Q3 <= '0';
    ELSIF ( clock 'EVENT AND clock = '0' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

7. (5 pts) The VHDL code above could best be described as
- a) A positive-edge triggered D flip-flop with an active-high reset
  - b) A negative-edge triggered D flip-flop with an active-high reset
  - c) A positive-edge triggered D flip-flop with an active-low reset
  - d) A negative-edge triggered D flip-flop with an active-low reset
  - e) None of the above
8. (5 pts) You have been instructed at times to make sure that Quartus treats unused pins as “input, tri-stated.” Why would this matter? (Select one.)
- a) Quartus has no special knowledge of the DE2 board other than what you specify, so a design compilation could accidentally drive a pin that may control DE2 devices in an adverse way
  - b) Quartus will connect those unused pins to some of the output pins from your design, and you shouldn't have outputs connected to outputs
  - c) Unused pins are always needed as extra inputs
  - d) It does not matter, actually.
9. (5 pts) You must be careful when monitoring the train sensor inputs because . . . (select one)
- a) they are deliberately designed to give occasional false readings
  - b) you cannot assume that they are active for only a single cycle
  - c) they go low to indicate a passing train, and low values are harder to see
  - d) they only become active when the train passes a second time

10. (5 pts) What part of a state machine circuit, implemented with D flip-flops, is most closely associated with the *next-state* variables of the state machine?
- The D inputs
  - The Q outputs

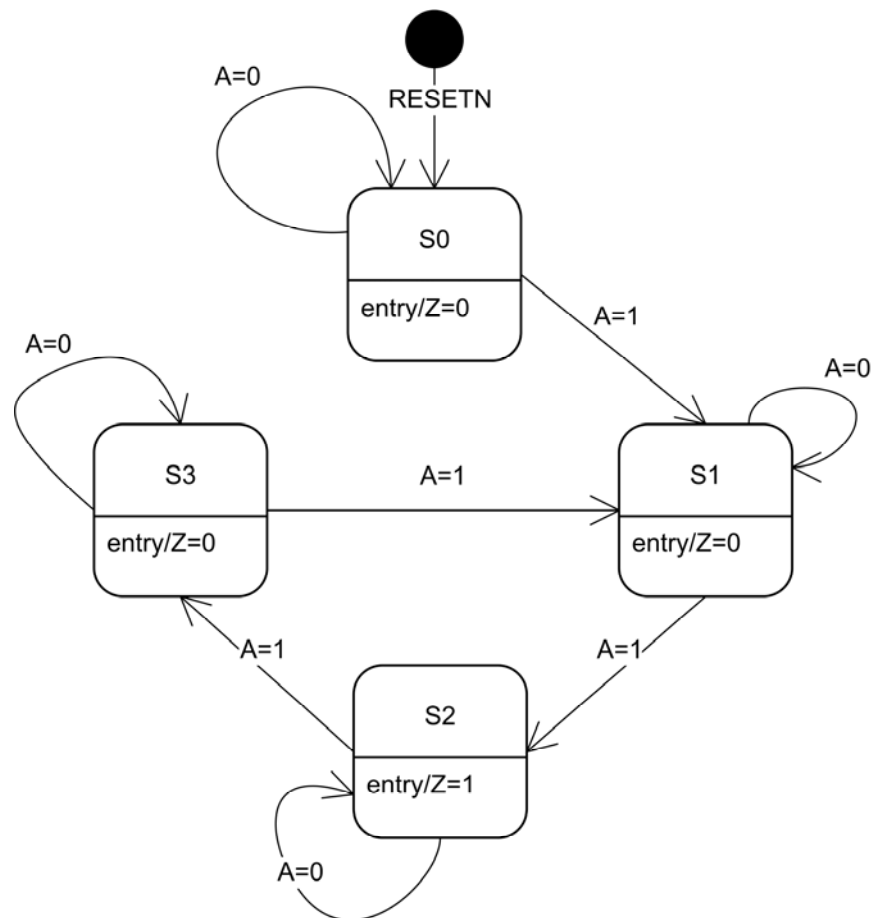


The image above is taken directly from the lab manual, showing the disassembly process for Lab 8.

11. (5 pts) What is the approximate period of the SCOMP clock?
- 6.2 ns
  - 20 ns
  - 33 ns
  - 100 ns
  - Impossible to estimate
12. (5 pts) Also with regard to the logic analyzer screen shown above, what is happening in the FETCH/DECODE/EXECUTE cycle beginning at around 100 ns on the timeline? (Select one.)
- A value of 0x80C is being written to memory address location 0x001
  - The value of the accumulator is being written to memory address location 0x00C
  - The input device at address 0x001 is being read
  - A value of 0x000 is being read from memory address location 0x00C
  - None of the above
13. (5 pts) Assume a D flip-flop has an asynchronous, active-low, “Clear” input. Initially, the Q output is low. If the Clear input is held low and the D input is held high as a positive clock edge occurs, what will the Q output do? (Select one.)
- Stay low
  - Go high
  - Go high, then low
  - Oscillate unpredictably
  - None of the above

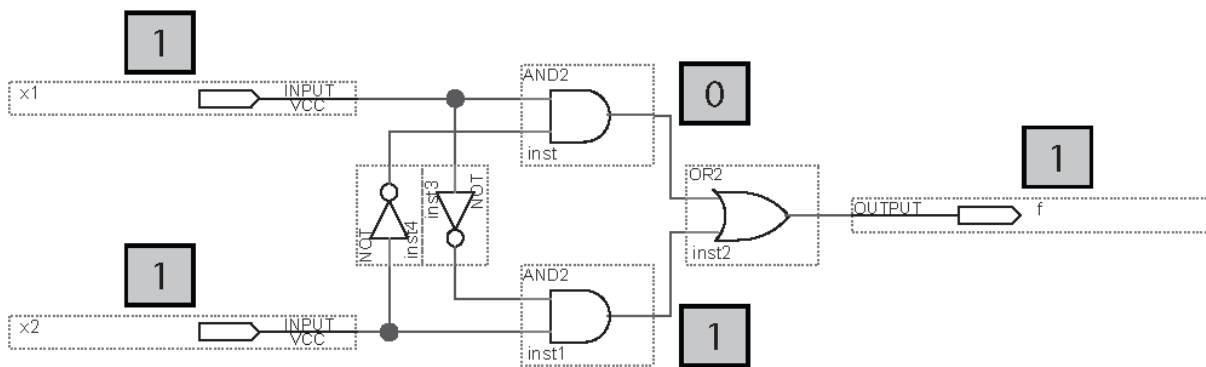
14. (5 pts) Which one of the following was not mentioned as a required or optional feature in your design project? (Select one.)
- a) A requirement to have a programmable presentation time, at least from 1-20 minutes
  - b) An allowed option of making the timer self-contained (no external peripherals)
  - c) Ease of use
  - d) An allowed option of using a state machine instead of an embedded processor
  - e) Optional support of variable warning times
15. (5 pts) The NIOS device is . . . (Select one.)
- a) A hard public-domain processor core
  - b) A soft IP processor core
  - c) A soft public-domain processor core
  - d) A hard IP multiplexer core
  - e) None of the above

FIGURE FOR NEXT PROBLEM:



16. (10 pts) Consider the Moore state machine described by the ASM diagram on the preceding page, which is based on positive edge-triggered D flip-flops. Assume that all inputs are valid in time for the clock edge (no setup violations). Which of the following are true with regard to this state machine? (Select all that apply).

- a) The output Z depends only on the number of times (sampled at positive clock edges) that the input A has been 1 (i.e., it does not matter how many times A has been sampled as 0 before, during, or after the times it was sampled as 1).
- b) The output Z will be asserted (=1) after the sequence RESETN, A=0, A=1
- c) Whenever A is a 0, state S0 is entered at the next positive clock edge.
- d) The output Z will be asserted (=1) after the sequence RESETN, A=1, A=1
- e) There is one state that can never be reached.



17. (10 pts) The figure above shows the circuit from the Lab 1 tutorial, with some observed logic levels alongside the point in the circuit where they were measured. If this circuit were built with discrete logic chips (on a protoboard), and if you were debugging this circuit, which would be the best choices for a first step? **Select all** that could fix the problem in one step, and don't select any that are unsupported guesses. You may assume that there is no relative advantage between replacing a gate or checking a connection – they are equally good choices when there is a fault that they could be causing.

- a) Replace the inverter named inst4
- b) Replace the inverter named inst3
- c) Replace the AND gate labeled inst
- d) Replace the AND gate labeled inst1
- e) Replace the OR gate labeled inst2