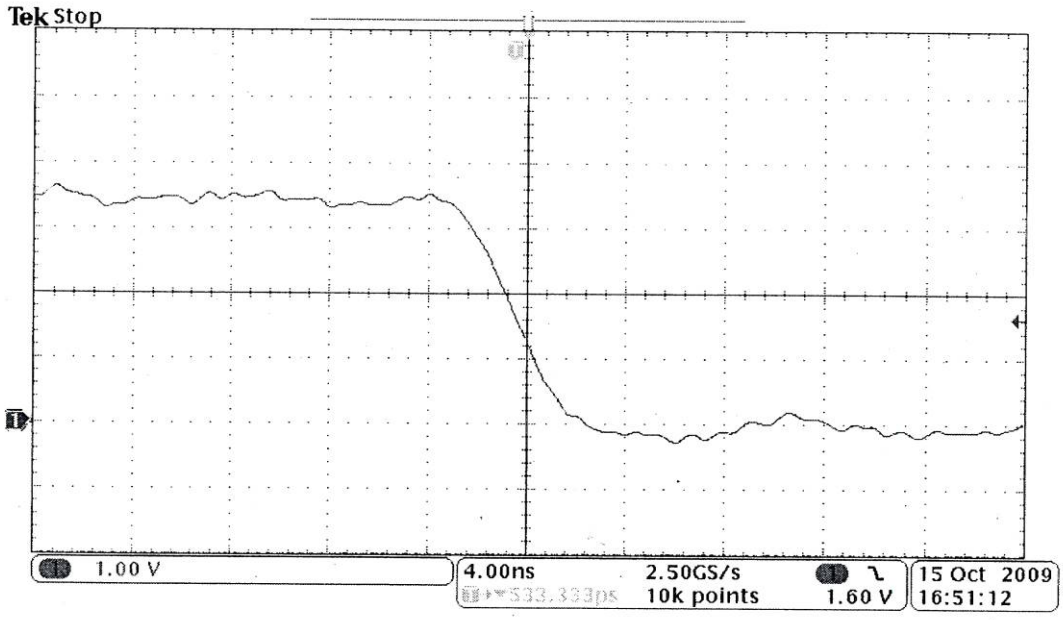
ECE2031 In-Class Exam Fall 2009

Closed Books, Closed Notes, No computers or calculators.
Mark all answers on the answer sheet.

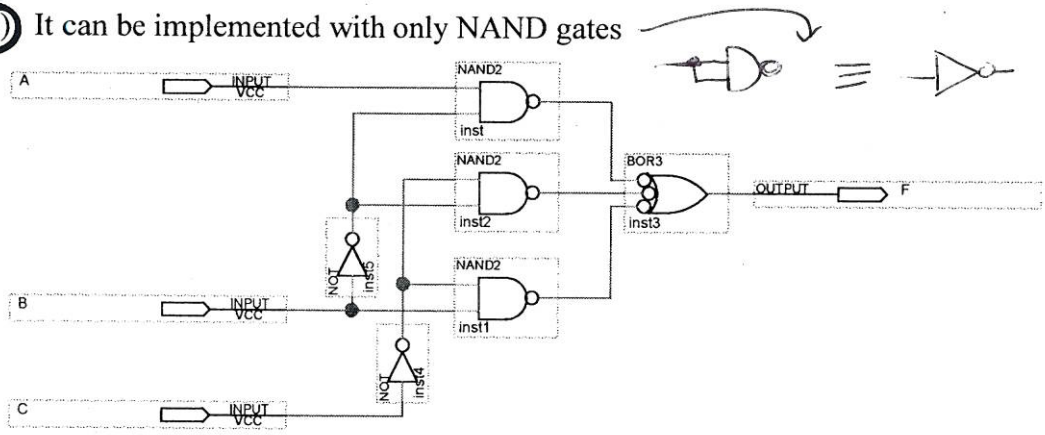
1. (5 points) What is the fall time of the signal shown below? The arrows next to the waveform indicate the ground levels, and the scales are displayed (1.00 V/division, 4.00 ns/division).

a) 3.7 ns
b) 0.4 ns
c) 10 kHz
d) 2.5 ns
e) 8.0 ns



2. (10 points) For the circuit shown below, which of the following are true? "Direct" means no additional manipulation or minimization. (Select all that apply.)

a) It is the direct implementation of a minimal sum of products expression
b) It is the direct implementation of a sum of products expression, but it is not minimal
c) It is not a direct implementation of a sum of products expression of any kind
d) It can be implemented with only NAND gates and inverters
e) It can be implemented with only NAND gates

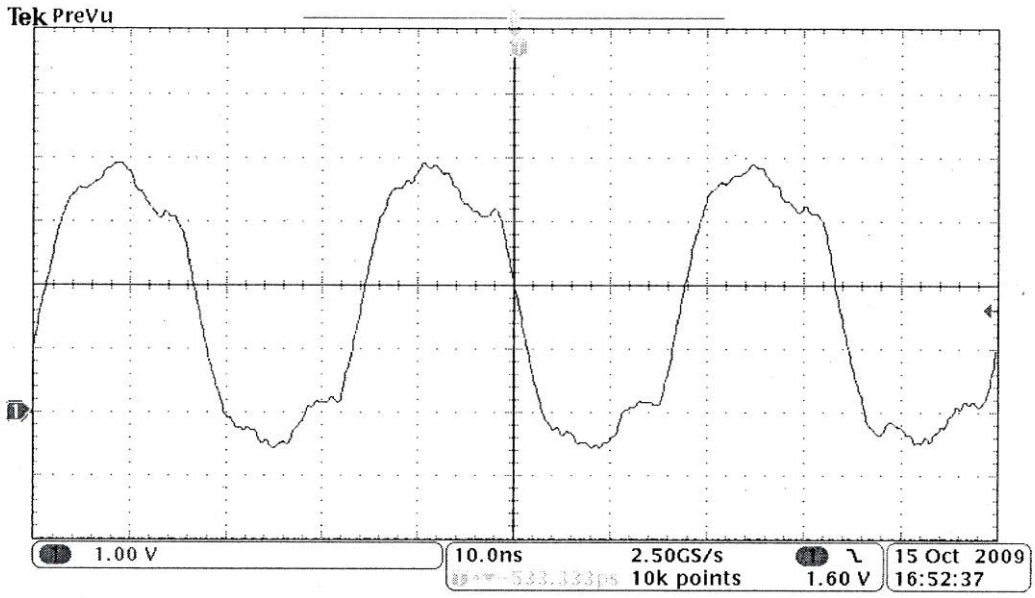


3. (5 points) If you had an instance of altsyncram in a VHDL file, and if you wanted to change the width of its address bus, you would

   a) Declare a new SIGNAL within the ARCHITECTURE
   b) Edit the PORT_MAP statement of altsyncram
   c) Edit the GENERIC_MAP statement of altsyncram
   d) None of the above

4. (5 points) What is the period of the signal shown below? The ground level is shown with the arrow on the left, and the scales are displayed (1.00 V/division, 10.00 ns/division).

   a) 2.50 GS/s
   b) 15.5 ns
   c) 33 ns
   d) 50%
   e) 10 ns



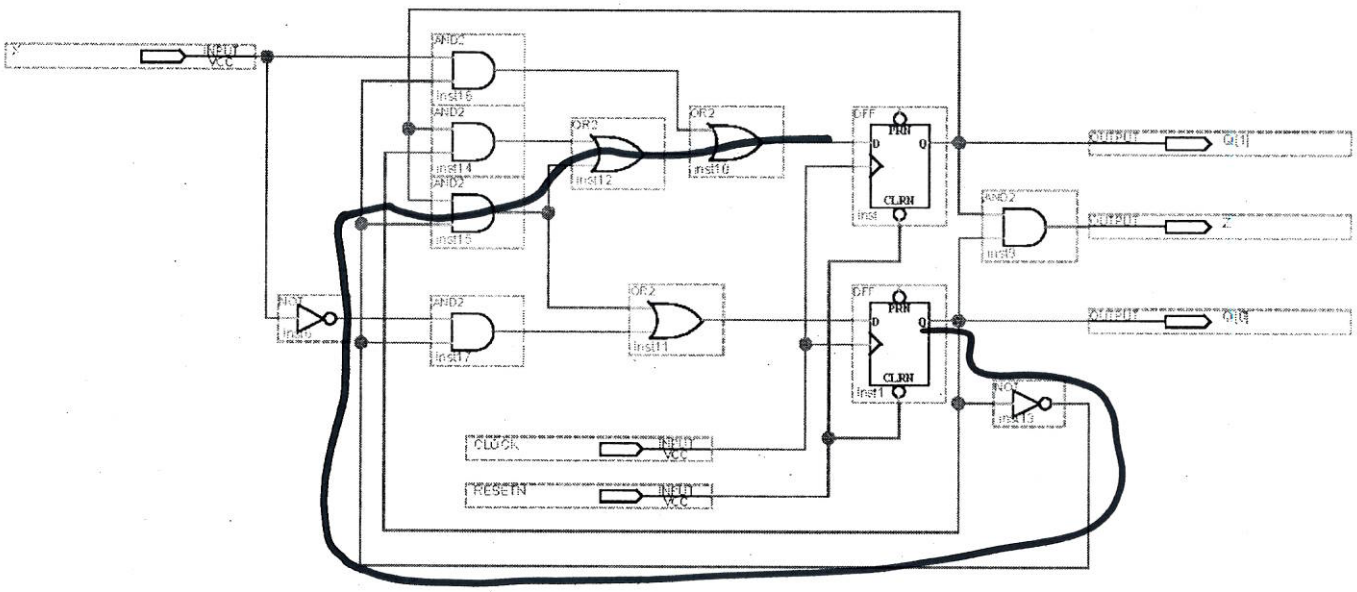
5. (5 points) What is the main difference between JUMP &H024 and CALL &H024? (Select one.)

   a) Only the JUMP instruction actually branches to &H024 in the next cycle
   b) The CALL pops the PC off of the stack, while the JUMP pushes the PC onto the stack
   c) Both instructions branch, but only CALL pushes the PC onto the stack
   d) After branching to &H024 with a JUMP, you must execute a RETURN instruction in order to get back to the instruction after JUMP
   e) None of the above

6. (5 points) Within the VHDL code for a device, where would the statement "PORT(A,B,C :IN STD_LOGIC);" be found?

   a) Under the "ENTITY"
   b) Under a "CASE"
   c) Under the "ARCHITECTURE"
   d) Under a "PROCESS"
   e) After a "USE"

7. (5 points) Given the circuit diagram below and the table of relevant timing parameters for various parts, find the worst-case timing path for the state machine. Do not attempt to minimize it or change it in any way. Then compute the minimum clock period (the time associated with that worst-case path).



Device	t_p (max propagation delay)	t_{su} (setup time)
D Flip Flop	11 ns	2 ns
NAND Gate	8 ns	N/A
OR Gate	13 ns	N/A
AND Gate	12 ns	N/A
Inverter	8 ns	N/A

a) 44

b) 46

c) 51

d) 57

e) 59

8. (5 points) The state machine shown above has five states.

a) TRUE

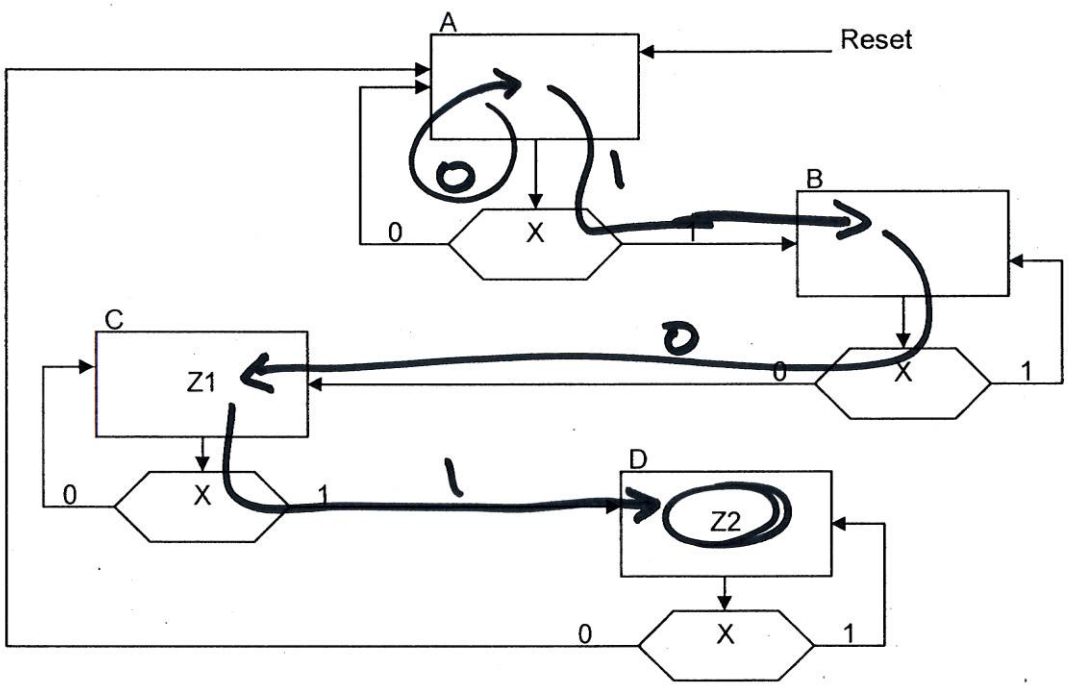
b) FALSE

c) Unable to determine from the information given

d) It has five states as shown, but could have fewer

Can't have more than four, with only two FF's

9. (5 points) Consider the state machine described by the ASM diagram below.



Starting from a reset condition, which output(s) will be active after the input has gone through the sequence 0, 1, 0, 1? You should assume that those four values are present at four successive positive clock edges, meeting the timing requirements. We are interested in the state of the machine after it has made a transition in response to that fourth input.

a) Z1

b) Z2

c) Both Z1 and Z2

d) Neither Z1 nor Z2

10. (5 points) For the specific train problem that you had to solve this semester, which train had to sometimes change direction?

a) Train A (the one using tracks 1, 2, and 4)

b) Train B (the one using tracks 2 and 3)

11. (5 points) For train problems in general, using the track setup as described, which of the following best describes the situation that occurs if both trains were to end up in the common section of Track 2 (at the bottom center of the track network)?

a) At any given instant, both trains will always move in the same direction and speed (or both will be stopped).

b) At any given instant, both trains will always move in the same direction, but perhaps at different speeds (or both will be stopped).

c) The speed and direction of both trains can be independently controlled by TCONTROL.

d) They can be started and stopped independently of each other, but since the speed of each is not controlled by TCONTROL, it is difficult to get them out on separate track sections again.

e) It is not possible to get both trains in that section of track.

For the next two questions, consider the following ASM code. Assume this has been assembled and run on SCOMP.

```
          ORG     &H000   ;Begin program at x000

Start:    LOAD    A
          SUB     B
          JNEG    Neg
          LOAD    C
          JUMP    Next
Neg:      LOAD    D
Next:     ADD     A
          STORE   E
Done:     JUMP    Done

A:        DW      &H0001
B:        DW      &H0002
C:        DW      &H0003
D:        DW      &HFFFF
E:        DW      &H0005
DD:       EQU     &HFFFF
```

12. (5 points) What is stored in location "E" at the end of program (i.e., after it starts looping forever at "Done")?

    a) &H0000
    b) &HFFFF
    c) &H0004
    d) &HFFFE
    e) None of the above

13. (5 points) How would the operation of the program change if the LOAD D instruction were replaced with with LOAD DD?

    a) Not at all, since D and DD are equivalent
    b) It would load D twice
    c) It would depend on how SCASM interprets the sixteen-bit operand &HFFFF, which is too long for a normal address operand
    d) DD is at the &H000E location in memory, so it would load &H000E.
    e) None of the above

14. (5 points) Which is the correct sequence in the simple computer?

    a) Fetch/Decode/Fetch/Execute

    b) Decode/Fetch/Execute

    c) Fetch/Decode/Execute

    d) Execute/Decode/Fetch

    e) None of the above

15. (5 points) The image on the next page shows a slightly modified version of the top_scomp.bdf file that you are given for Lab 8. You may assume that all pin & device assignments are done correctly, and that all of the symbols actually implement their functions correctly.

    SCOMP itself includes an output called FETCH_OUT. Which of the following is true regarding this output? (Select only one.)

    a) It was always in SCOMP, even in the starting point provided for Lab 7.

    b) It is added in Lab 8 so that the logic analyzer can disassemble instructions.

    c) It is a vector of multiple bits.

    d) Because it is not used anywhere else in the schematic, it will probably be minimized out of (i.e., eliminated from) the final design when Quartus compiles it.

    e) None of the above.

16. (10 points) For the same top_scomp.bdf file used in the previous problem, which of the following are true? (Mark all that apply.)

a) SCOMP is clocked at 30 MHz.

b) The unused hexadecimal digits HEX0-HEX3 (which all have active-low LED segments) are unlit (i.e., turned off).

c) At least one of the "NOTE" comments about I/O addressing is incorrect.

d) IO_DATA is not implemented here as a tri-state bus.

e) Only one device is actually reset DIRECTLY by the KEY[0] reset pushbutton

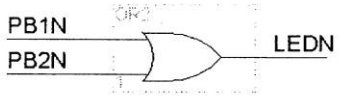
LEDs are decoding 9's not 1

17. (10 points) If you need an active-low signal to turn on an LED only when either or both of two active-low pushbuttons are pressed, you could use which of the following? (Select all that apply, and choose any that will logically work, even if they are not the most obvious to understand visually.)

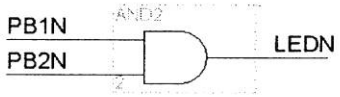
If you are unclear about the meaning of active-low, it may help if you remember the DE2 board, which has active-low pushbuttons (KEY[0] through KEY[3]) and active-low LED segements on the hexadecimal displays (as was mentioned in the previous question, too).

ALTPLL is the only device being reset. If resets everything else.

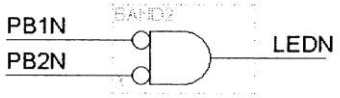
a) a two-input OR gate (or2 in Quartus II)



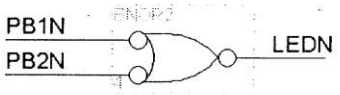
b) a two-input AND gate (and2)



c) a two-input bubbled-input AND gate (band2)



d) a two-input bubbled-input NOR gate (bnor2)



e) a three-input OR gate (or3)