



Review for In-Class exam

In-class exam



- Will take place in your assigned lecture period
- It will be a comprehensive written exam, emphasizing fundamentals:
 - Combinational logic design process
 - State machine design process
 - Instrument measurements (using diagrams, not real scopes or analyzers)
 - Simple Computer
 - Technical writing fundamentals
- Examples are on Canvas (same page you found this)
 - Some will use an older state diagram format (called Algorithmic State Machine or “ASM”) instead of the current UML statecharts, but you can translate the intent.
 - Ignore any problems that are clearly not applicable
 - E.g., questions related to other projects



General logic design coverage

- Basic combinational logic
 - K-maps, SOP, minimal SOP, schematics
- Basic circuit building
 - Protoboard usage
 - Switches & pull-ups
- Operation of a device, given its truth table, datasheet, etc.

Test equipment coverage



- Oscilloscope

- Make measurements from a screen capture given to you

- Logic analyzer

- Understand what it does
- Interpret typical logic analyzer screens

VHDL coverage



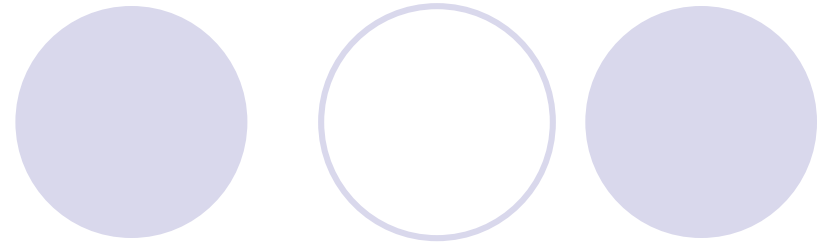
- Work with basic VHDL syntax and characteristics
- Describe the function and/or draw the circuit for a given section of VHDL code
- Write VHDL code (fill in code fragments or pick from multiple choices) to synthesize a given word description or circuit
- VHDL coding would be very limited on the closed-book class exam (i.e., not requiring students to begin with a blank sheet)

State machine coverage



- Understand a given UML statechart or classic state diagram
- Transition tables and K-maps for state machines
- Generate a UML statechart for a state machine from a word description
- Generate the VHDL CASE statement to synthesize a state machine from a UML statechart
- Recognize bugs in VHDL state machines, when compared with the corresponding state diagram
- Timing calculations (longest path & maximum clocking frequency)

Train lab coverage



- How trains function
 - Switches
 - Sensors
 - Direction
- What is allowed in a working train scenario
- Understand a simple train state machine controller

Simple Computer coverage



- Major components
- Structure and function
 - Architecture
 - Instruction word format
 - Assembly and machine language
 - Dataflow between registers, memory, ALU
 - I/O subsystem
 - Subroutines

Project coverage



- Basic project description
- Track, obstacles
- Robot features and characteristics
- Sonar and odometry basics