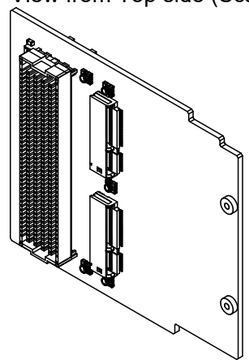
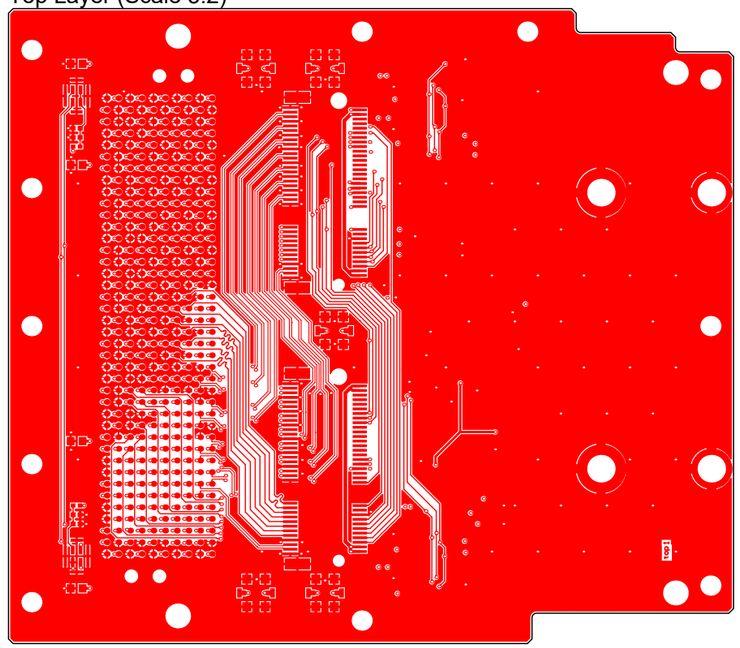
Layout:

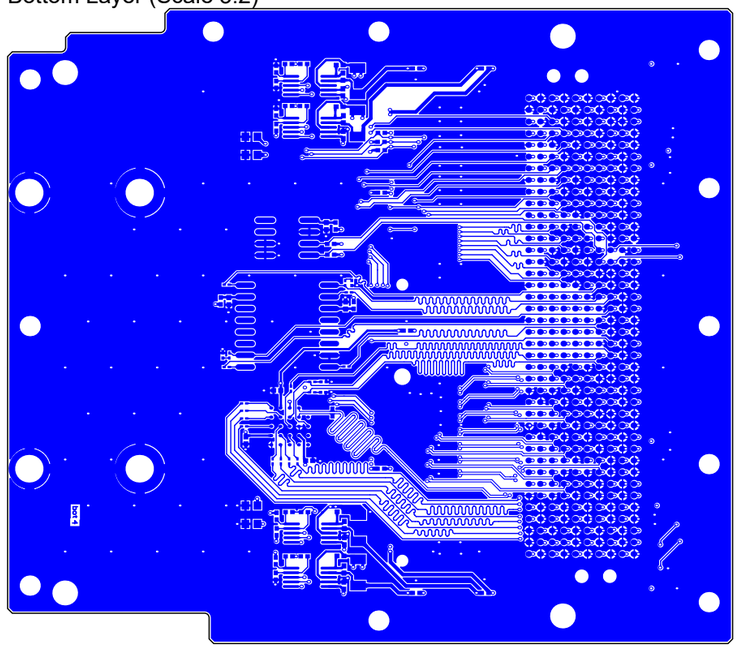
View from Top side (Scale 2:3)



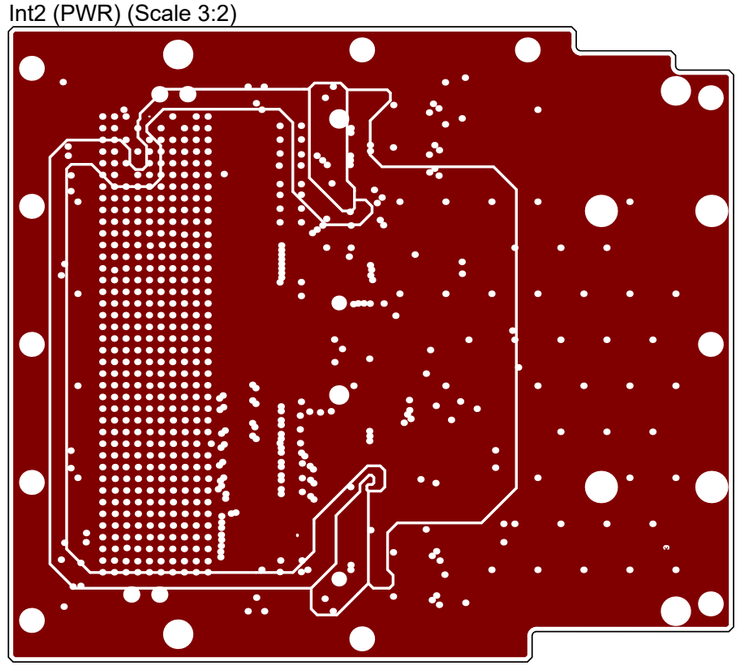
Top Layer (Scale 3:2)



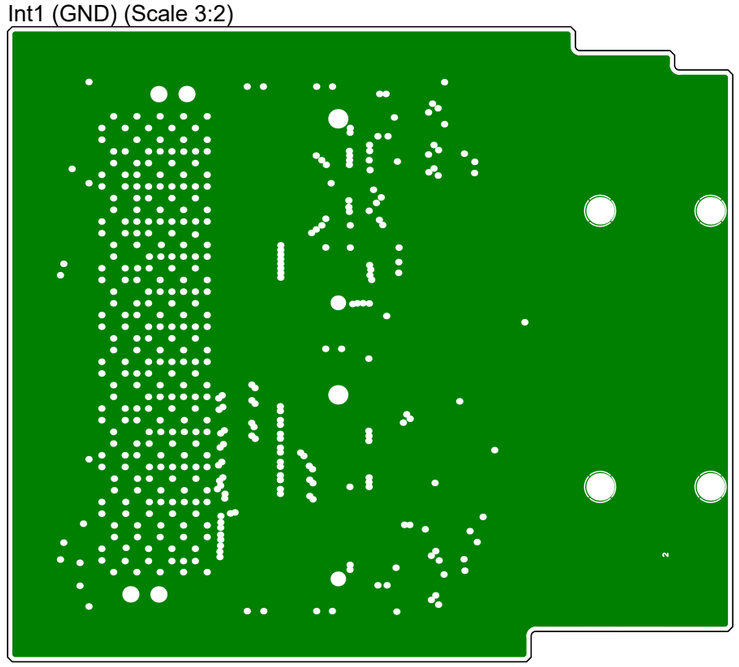
Bottom Layer (Scale 3:2)



Int2 (PWR) (Scale 3:2)



Int1 (GND) (Scale 3:2)



ETH zürich		Project: FPGA Peripherals Board	
Drawing number:	Rev: A	Format: A3	Laboratory: IIS
Date: 09.02.2021			Drawn by: MAYERPH
Sheet: FPGA_Peripheral_Board_layout.PCBDwf			
Page: 1 of 1			

File: C:\Users\phili\polybox\05_AltiumProjects\FPGA Peripheral Board\BaseBoard\FPGA_Peripheral_Board_layout.PCBDwf