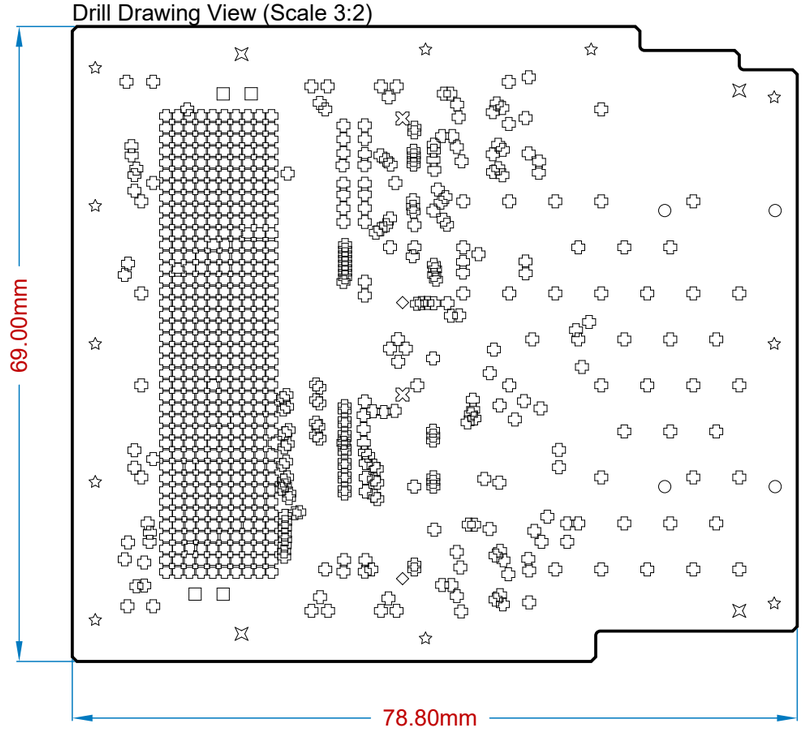
Manufacturing documentation:

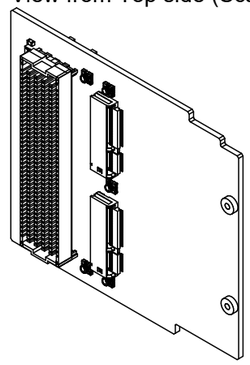
Drill Drawing View (Scale 3:2)



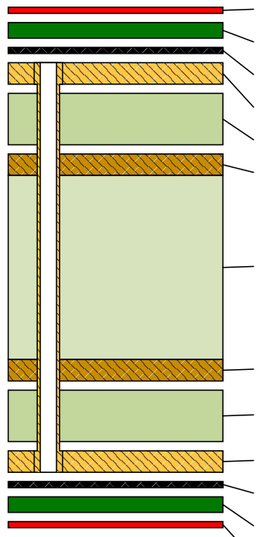
Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⌖	713	0.20mm	Plated	
◇	2	1.10mm	Non-Plated	+/-0.05mm
□	4	1.27mm	Non-Plated	
⊠	2	1.60mm	Non-Plated	+/-0.05mm
☆	11	2.20mm	Plated	
⛛	4	2.70mm	Plated	
○	4	3.00mm	Plated	
	740 Total			

View from Top side (Scale 2:3)



Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber	Comments
	Top Overlay			Legend	GTO	
Surface Material	Top Solder	0.025mm	SM-001	Solder Mask	GTS	black
Gold	Top Surface Finish	0.004mm		Surface Finish		
CF-004	Top Layer	0.035mm		Signal	GTL	
Prepreg		*0.084mm*	*PP-009*	*Dielectric*		-
CF-004	Int1 (GND)	0.035mm		Internal Plane	GP1	
Core		*1.200mm*	*Core-043*	*Dielctric*		-
CF-004	Int2 (PWR)	0.035mm		Internal Plane	GP2	
Prepreg		*0.084mm*	*PP-009*	*Dielectric*		-
CF-004	Bottom Layer	0.035mm		Signal	GBL	
Gold	Bottom Surface Finish	0.004mm		Surface Finish		
Surface Material	Bottom Solder	0.025mm	SM-001	Solder Mask	GBS	black
	Bottom Overlay			Legend	GBO	

Total thickness: 1.566mm

Notes:

1. Impedance matched stack-up
2. 0.1mm trace width / clearance

ETH zürich

Project: FPGA Peripherals Board

Drawing number: Rev: A	Format: A3	Laboratory: IIS	Sheet: FPGA_Peripheral_Board_fabrication.PCBD
Date: 09.02.2021		Drawn by: MAYERPH	Page: 1 of 1

File: C:\Users\phili\polybox\05_AltiumProjects\FPGA Peripheral Board\BaseBoard\FPGA_Peripheral_Board_fabrication.PCBDwf