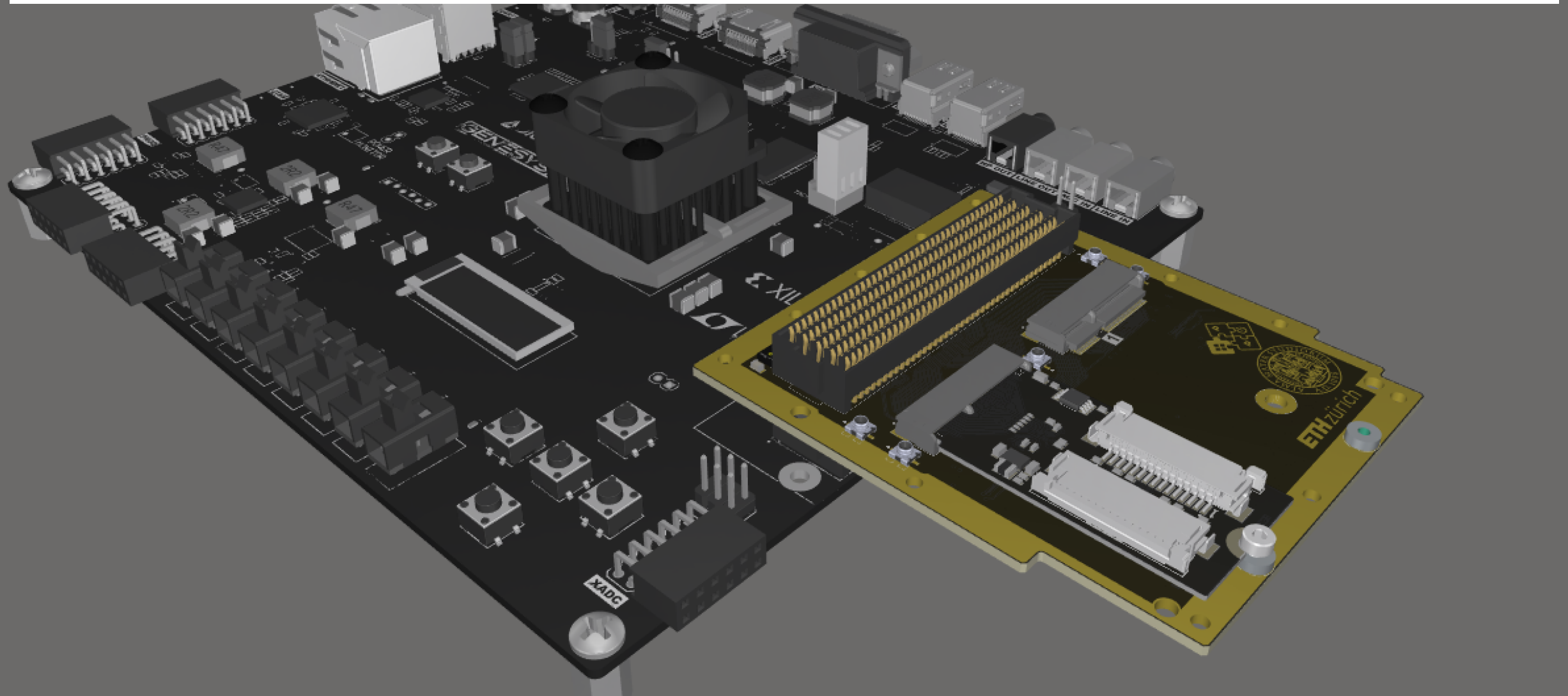
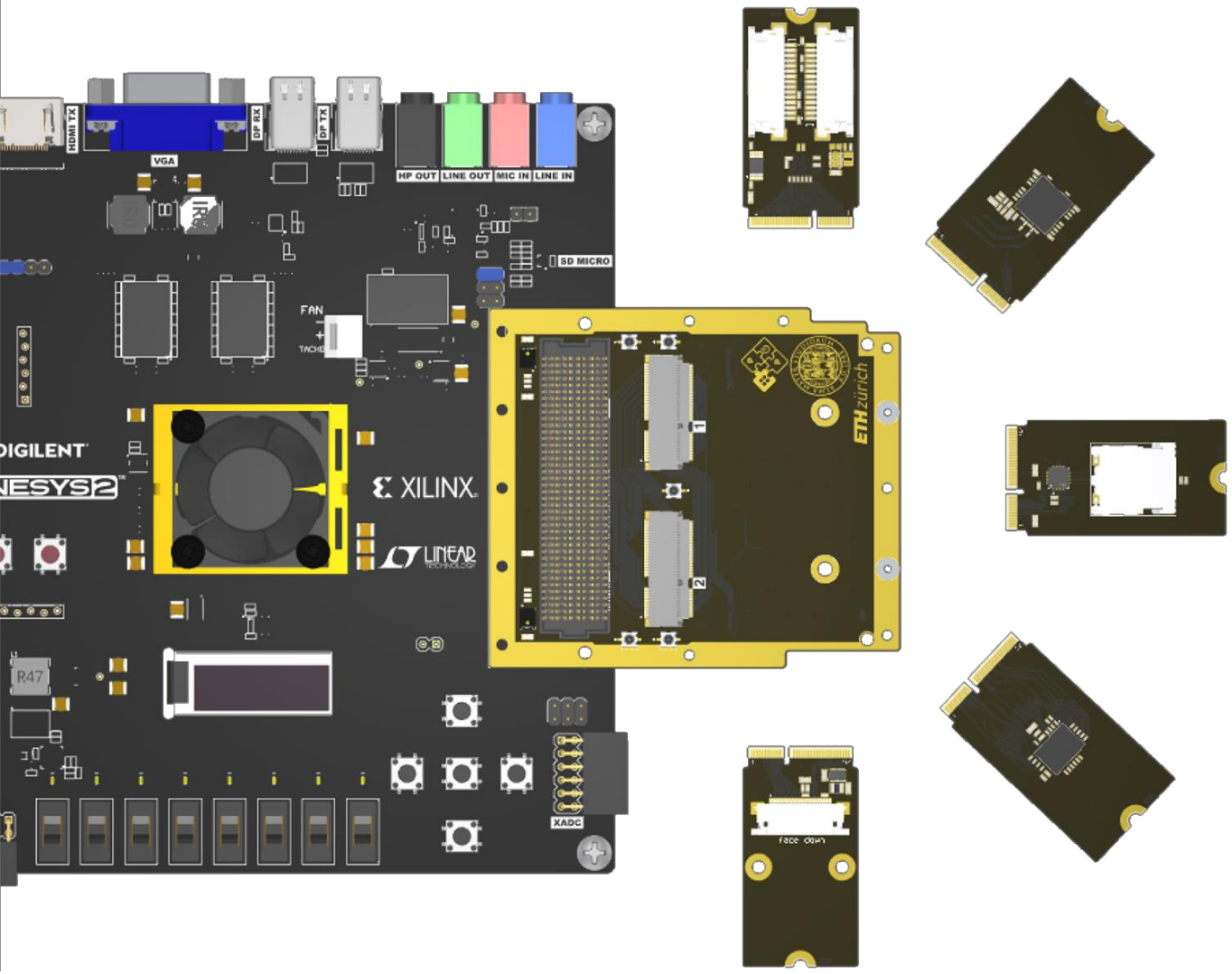
FPGA Peripheral Board

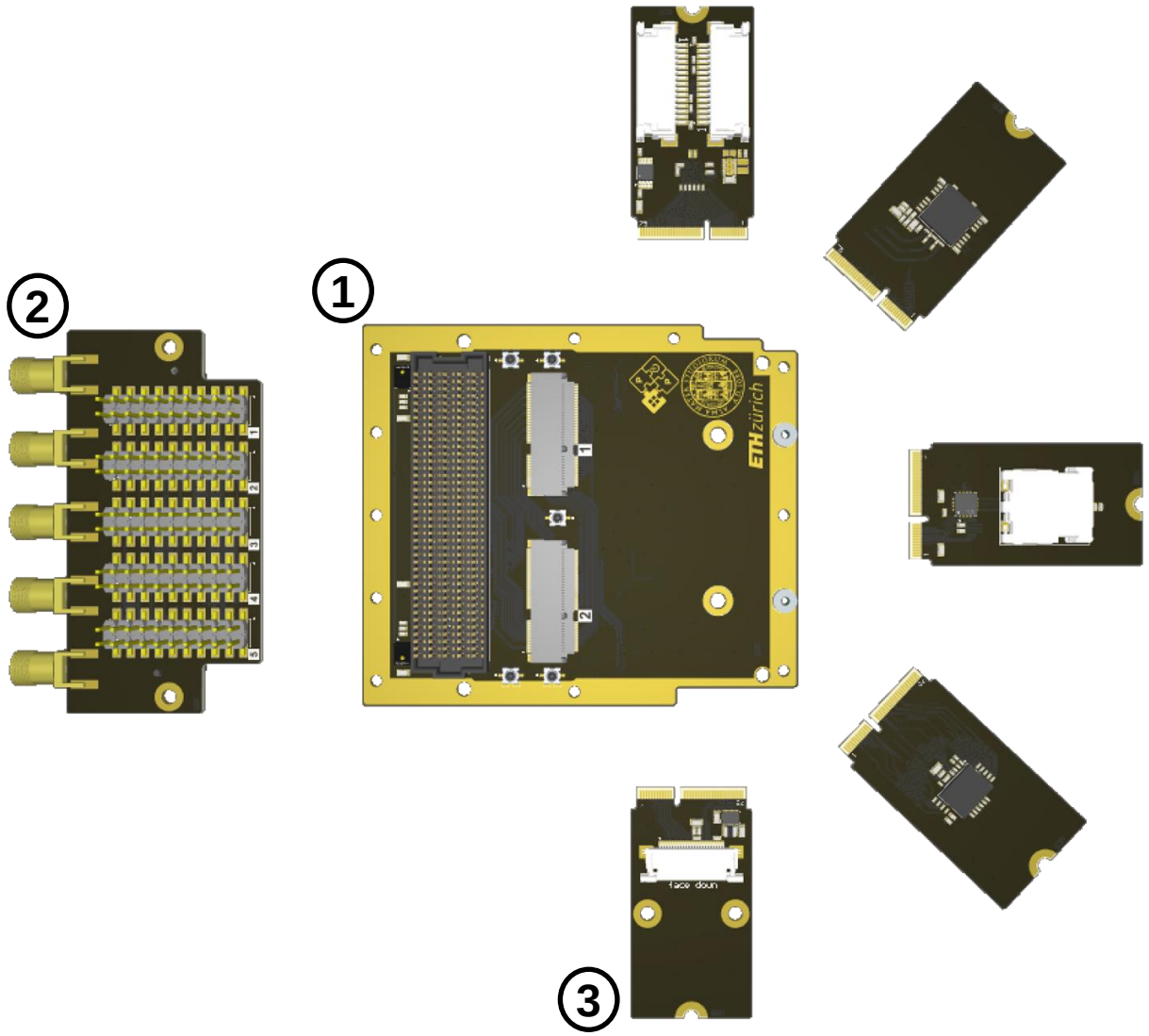


Motivation



- full-soc emulation with real-world hardware in the loop
- pre & post tape-out testing

Overview

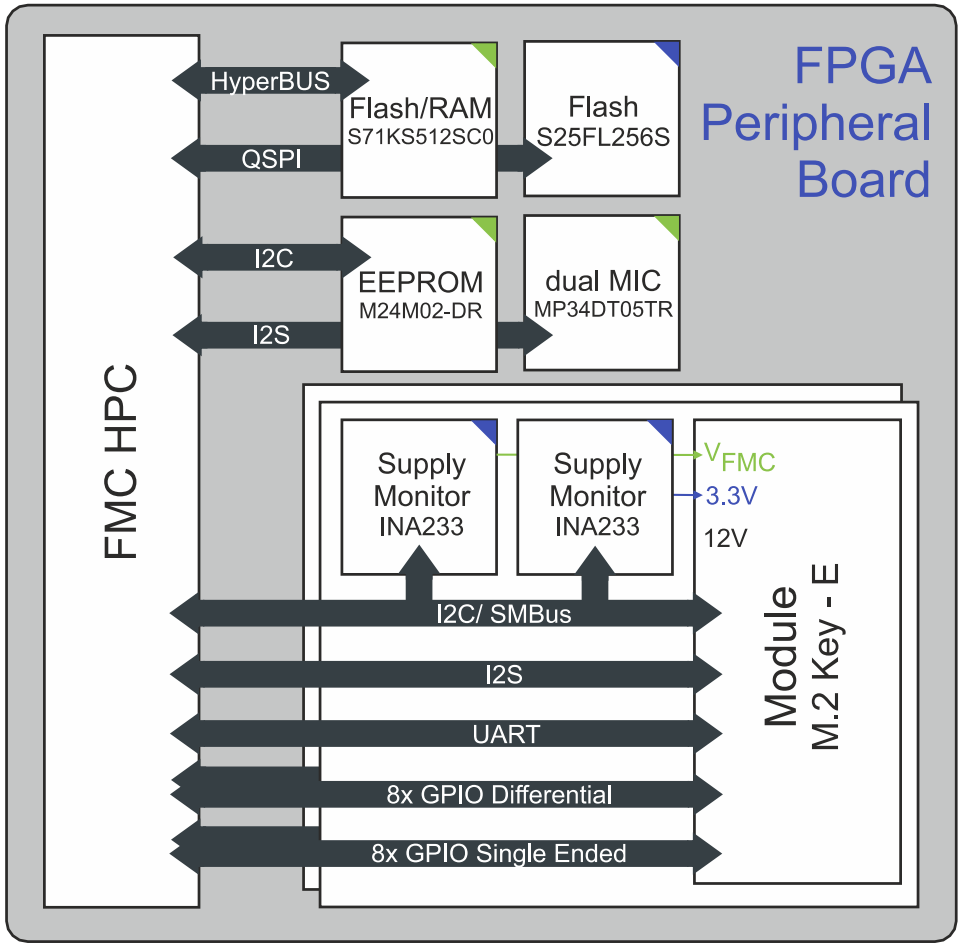


① «Carrier Board» with basic peripherals

② «Test Board» FPC signal pass through

③ «Expansion Modules» m.2 sized cards

Block Diagram



Onboard Peripherals

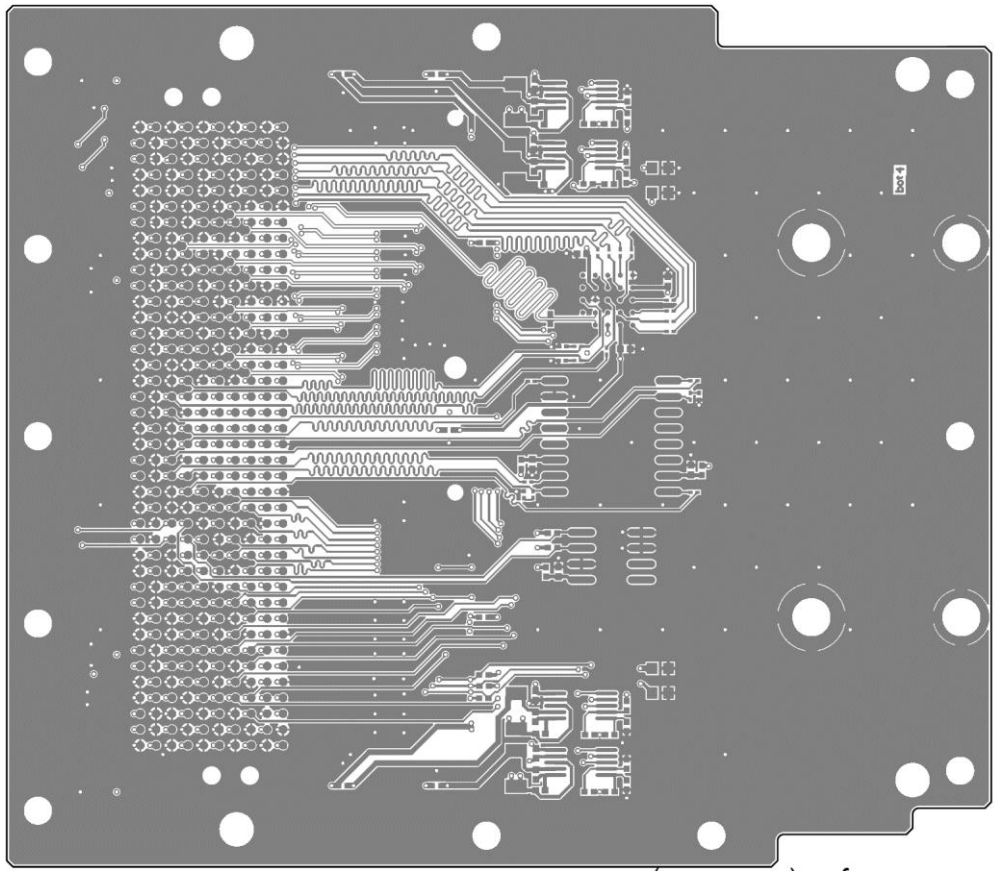
- Hyper Flash/RAM: S71KS512SC0
- SPI FLASH: S25FL256SAGMFIR03
- I2C EEPROM: M24M02-DRMN6TP
- 2x Microphone: M24M02

2x M.2 Type E expansion connector

- 8 individual single ended general-purpose lines
- 8 individual differential general-purpose lines
- shared I2C, I2S, UART
- power sensing

(Second module fully available on FMC HPC only)

Signal Speed

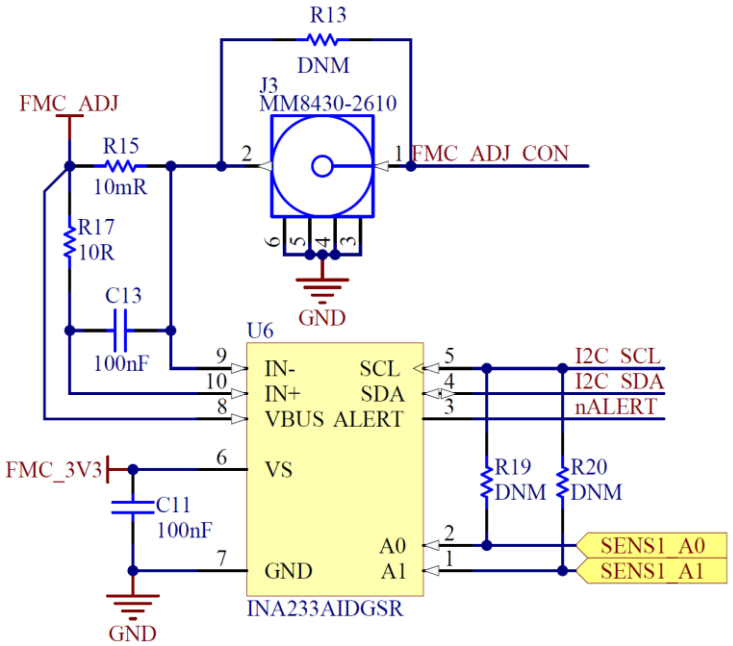


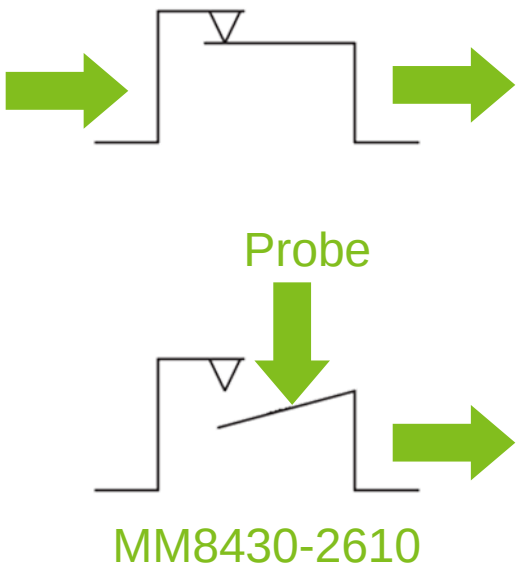
Signal Class	Routed Length	Delay Tolerance
HyperBUS	~65 mm	50 ps
QSPI	~45 mm	100 ps
CON1_GP_D[0..7	~50 mm	50 ps
CON1_GP_S[0..7]	~15 mm	5 ps
CON2_GP_D[0..7]	~14 mm	50 ps
CON2_GP_S[0..7]	~30 mm	5 ps

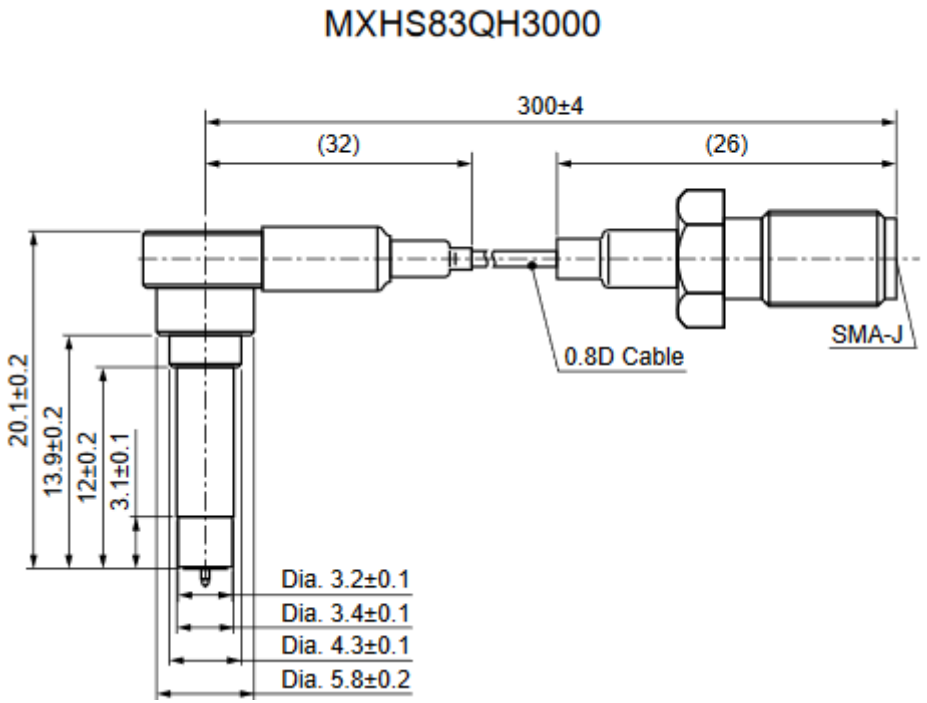
Only length matched in same signal group !

Power Measurements

1.) I2C current and power monitor
2.) External supply via coaxial probe







FMC

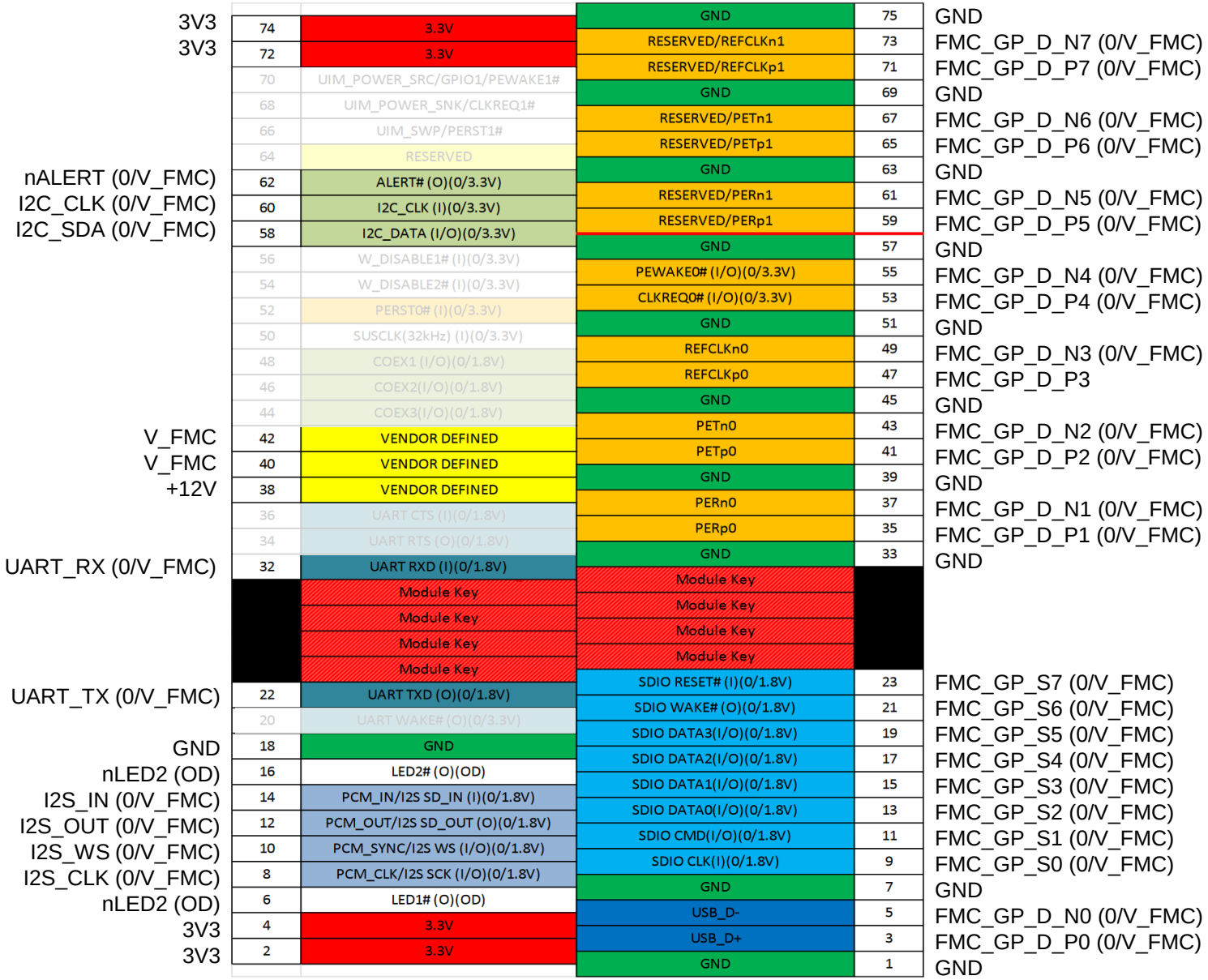
FMC HPC only

FMC HPC only

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Figure C-35: FMC HPC Connector Pinout

Modifications to M.2 Key E



Expansion Module Pin Selection

M.2 Pinout Key - E				
74	3V3		75	GND
72	3V3		73	FMC_GP_D_N7
70	RESERVED		71	FMC_GP_D_P7
68	RESERVED		69	GND
66	RESERVED		67	FMC_GP_D_N6
64	RESERVED		65	FMC_GP_D_P6
62	nALERT		63	GND
60	I2C_SCL		61	FMC_GP_D_N5
58	I2C_SDA		59	FMC_GP_D_P5
56	RESERVED		57	GND
54	RESERVED		55	FMC_GP_D_N4
52	RESERVED		53	FMC_GP_D_P4
50	RESERVED		51	GND
48	RESERVED		49	FMC_GP_D_N3
46	RESERVED		47	FMC_GP_D_P3
44	RESERVED		45	GND
42	FMC_ADJ (typ 1.8V)		43	FMC_GP_D_N2
40	FMC_ADJ (typ 1.8V)		41	FMC_GP_D_P2
38	FMC_12V		39	GND
36	RESERVED		37	FMC_GP_D_N1
34	RESERVED		35	FMC_GP_D_P1
32	UART_RX		33	GND
30	-		31	-
28	-		29	-
26	-		27	-
24	-		25	-
22	UART_TX		23	FMC_GP_S7
20	RESERVED		21	FMC_GP_S6
18	GND		19	FMC_GP_S5
16	LED2		17	FMC_GP_S4
14	I2S_IN		15	FMC_GP_S3
12	I2S_OUT		13	FMC_GP_S2
10	I2S_WS		11	FMC_GP_S1
8	I2S_CLK		9	FMC_GP_S0
6	LED1		7	GND
4	3V3		5	FMC_GP_D_N0
2	3V3		3	FMC_GP_D_P0
			1	GND

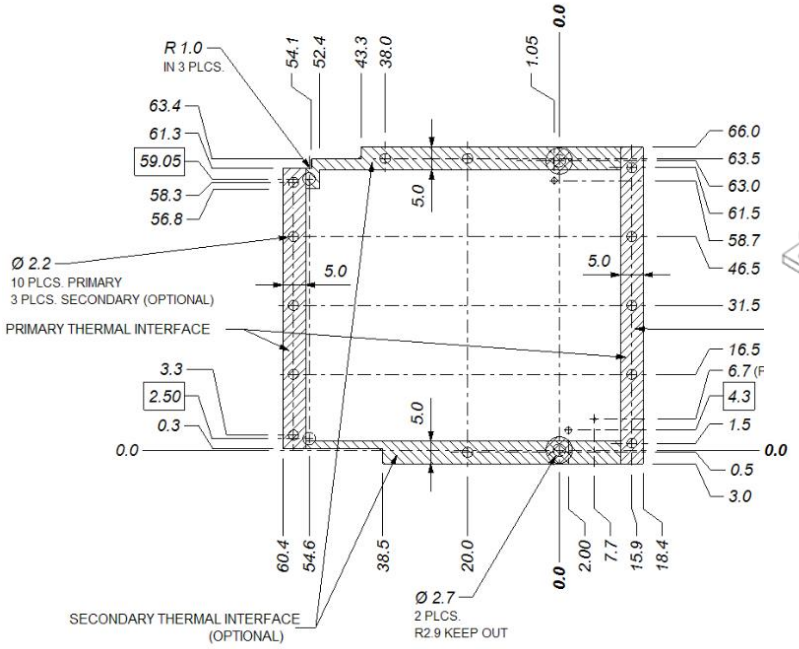
RPC DRAM (1V5) EM6GA16LBMA-10H	PSRAM (1V8) APS256XXN-OBRX-BG	CPI to CSI STMIPID02 (1V8)	CPI Himax (1V8)	SDIO uSD (1V8)
CLK_n	nCE	PCLK	PCLK	
CLK_p	CK		MCLK	
DQS_n	DQS/DM1	HSYNC	HSYNC	
DQS_p	DQS/DM0	VSYNC	VSYNC	
DQS1_n			INT	
DQS1_p			TRIG	
DB15	DQ15			
DB14	DQ14			
DB13	DQ13			
DB12	DQ12			
DB11	DQ11	D11		
DB10	DQ10	D10		
DB9	DQ9	D9		
DB8	DQ8	D8		
DB7	ADQ7	D7	D7	
DB6	ADQ6	D6	D6	CLK RET
DB5	ADQ5	D5	D5	SD_D3/nCS
DB4	ADQ4	D4	D4	SD_D2
DB3	ADQ3	D3	D3	SD_D1
DB2	ADQ2	D2	D2	SD_D0/MISO
DB1	ADQ1	D1	D1	SD_CMD/MOSI
DB0	ADQ0	D0	D0	CLK/SCLK
STB				
nCS				

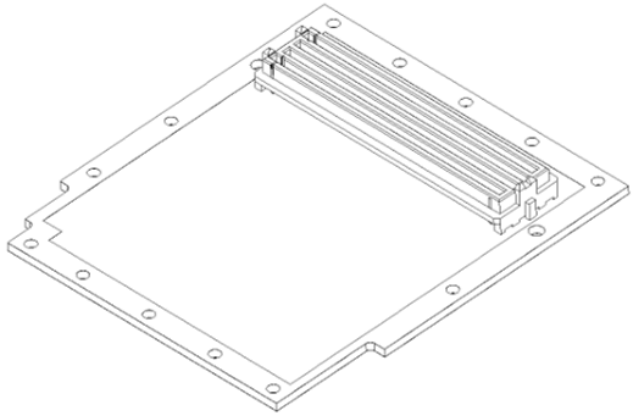
* Not designed to reach peak DRAM speed!

Board Dimensions

Carrier Board:

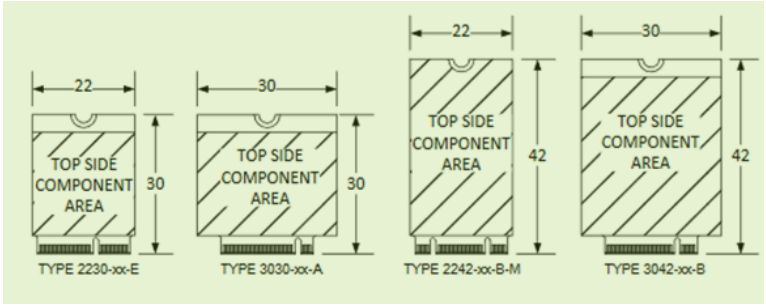
- ANSI/VITA 57.1-2008
  Single Width Conduction Cooled FMC Module
  (Does not follow 10mm board hight limit)

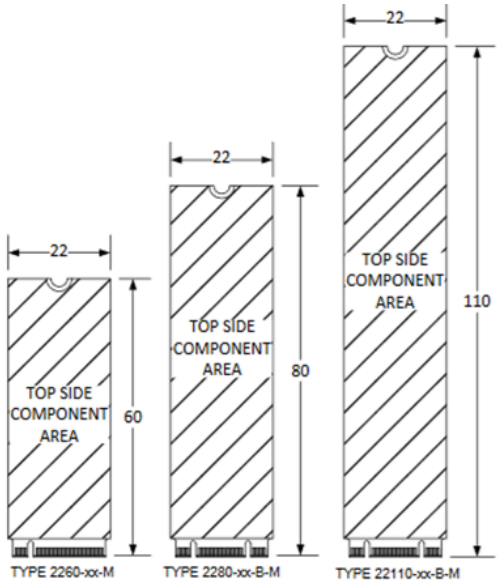




Expansion Modules:

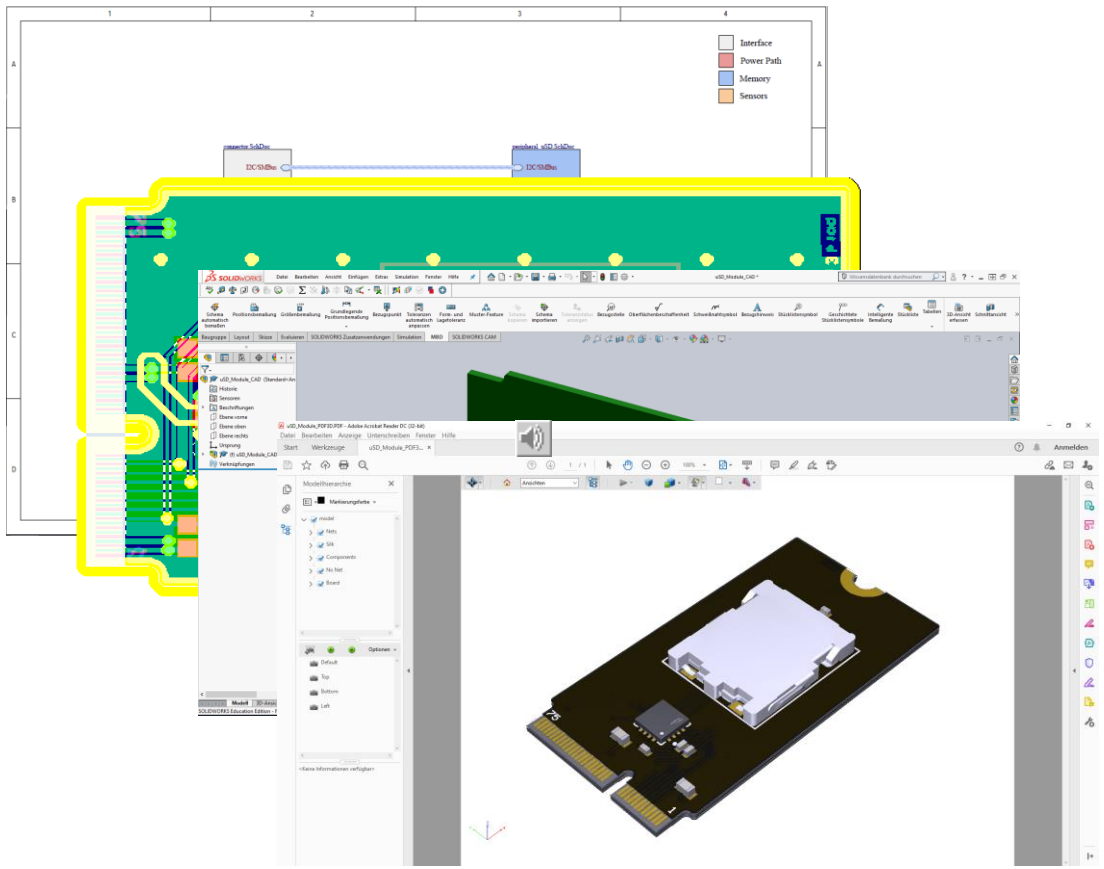
- PCI Express M.2
  Type 2230-D5-E
  Type 3030-D5-E
  Type 2242-D5-E
  Type 3042-D5-E



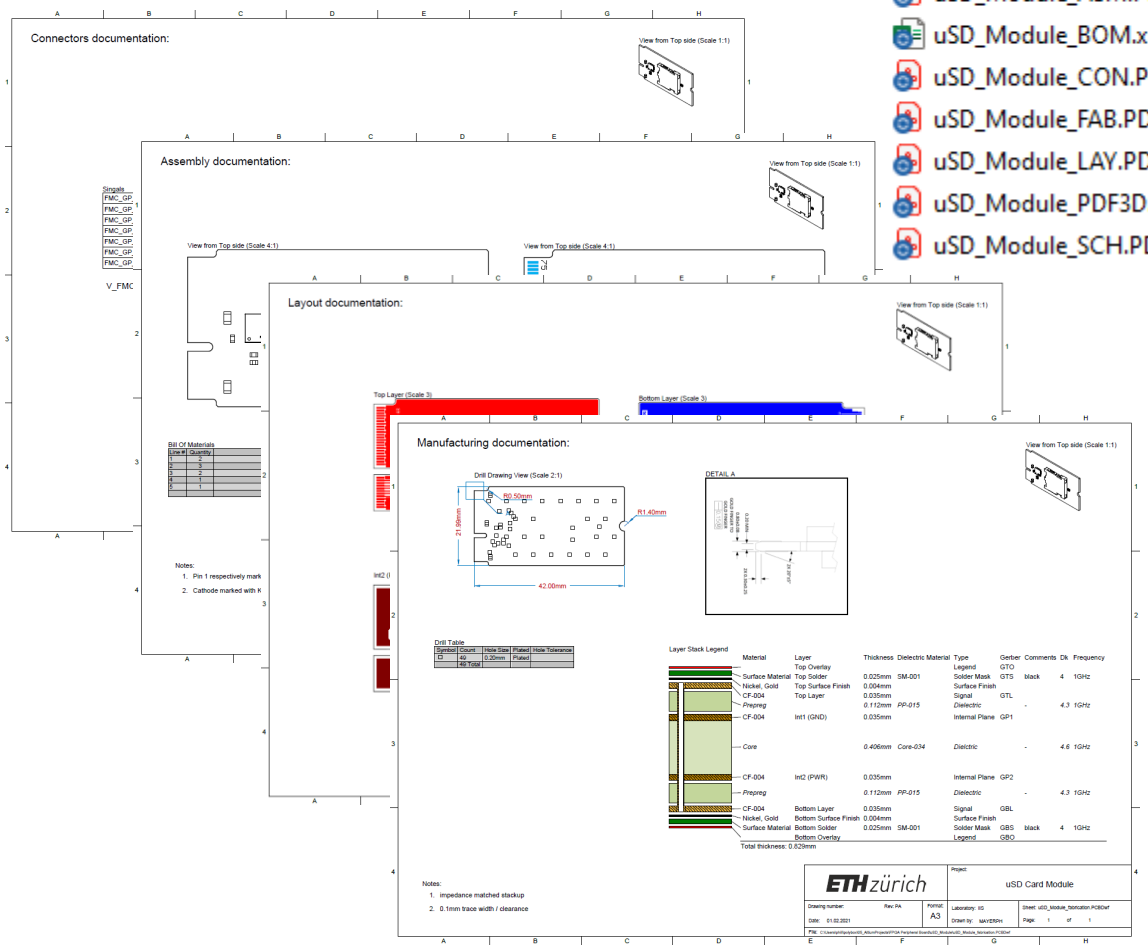


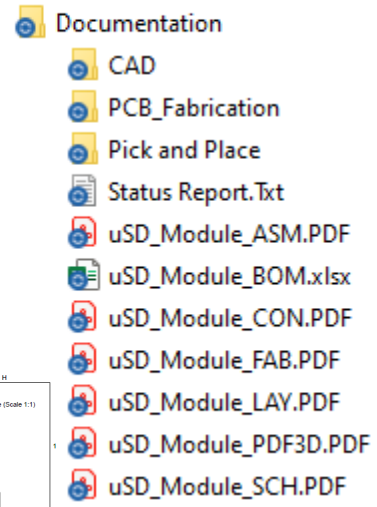
Documentation

“Conventional” board file



Supporting documentation

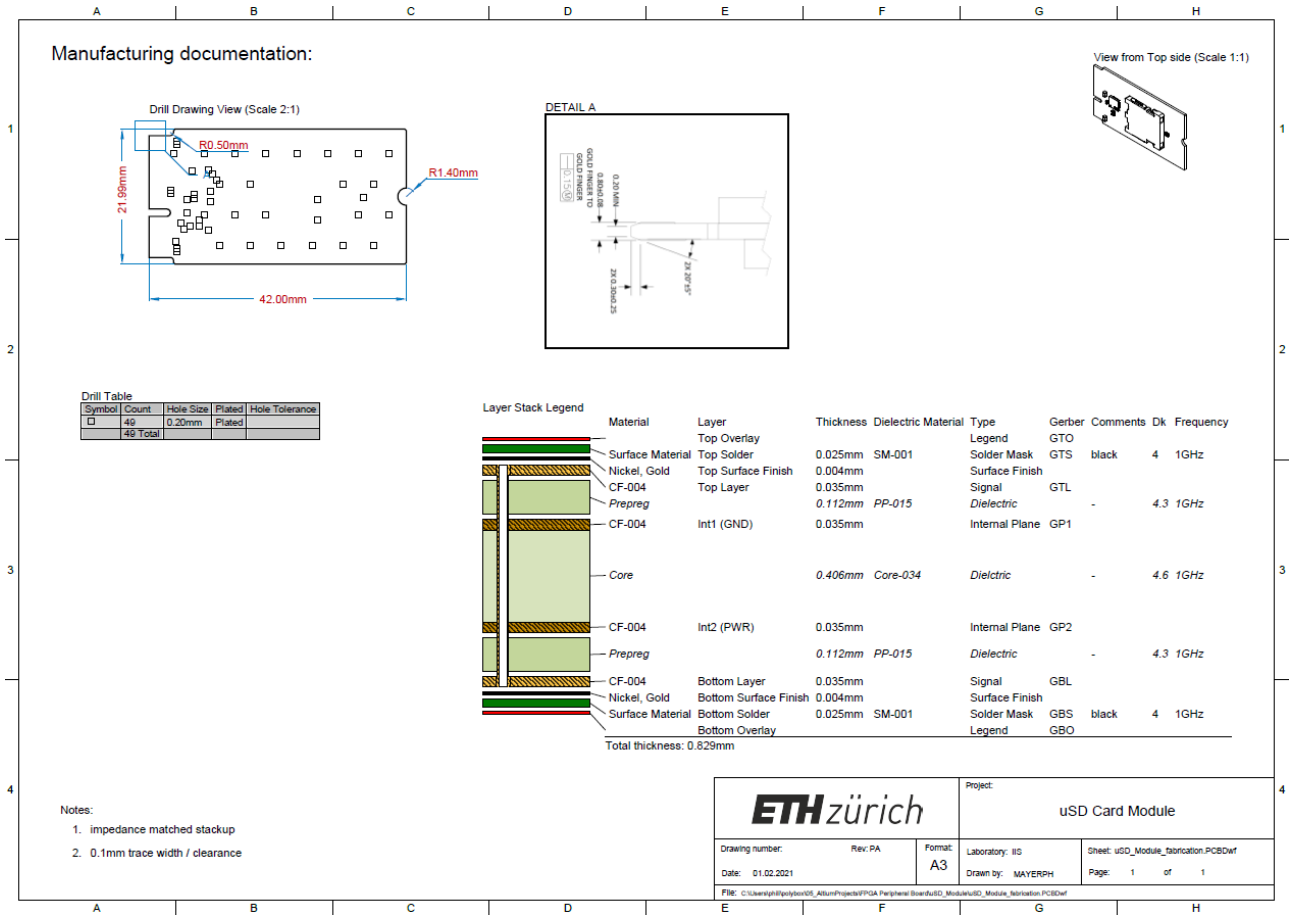




Documentation

Fabrication data:

- Gerber
- *_FAB.pdf
  board size,
  stack-up,
  clearance,
  isolate, etc.



Manufacturing documentation:

Drill Drawing View (Scale 2:1)

DETAIL A

View from Top side (Scale 1:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	49	0.20mm	Plated	
	49 Total			

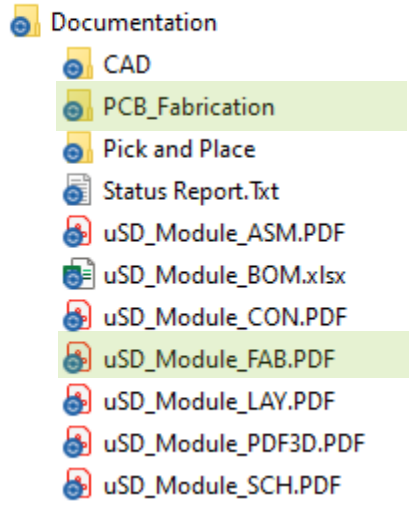
Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber	Comments	Dk	Frequency
		Top Overlay			Legend	GTO			
	Surface Material	Top Solder	0.025mm	SM-001	Solder Mask	GTS	black	4	1GHz
	Nickel, Gold	Top Surface Finish	0.004mm		Surface Finish				
	CF-004	Top Layer	0.035mm		Signal	GTL			
	Prepreg		*0.112mm*	*PP-015*	*Dielectric*		-	*4.3*	*1GHz*
	CF-004	Int1 (GND)	0.035mm		Internal Plane	GP1			
	Core		*0.406mm*	*Core-034*	*Dielctric*		-	*4.6*	*1GHz*
	CF-004	Int2 (PWR)	0.035mm		Internal Plane	GP2			
	Prepreg		*0.112mm*	*PP-015*	*Dielectric*		-	*4.3*	*1GHz*
	CF-004	Bottom Layer	0.035mm		Signal	GBL			
	Nickel, Gold	Bottom Surface Finish	0.004mm		Surface Finish				
	Surface Material	Bottom Solder	0.025mm	SM-001	Solder Mask	GBS	black	4	1GHz
		Bottom Overlay			Legend	GBO			

Total thickness: 0.829mm

Notes:
1. impedance matched stackup
2. 0.1mm trace width / clearance

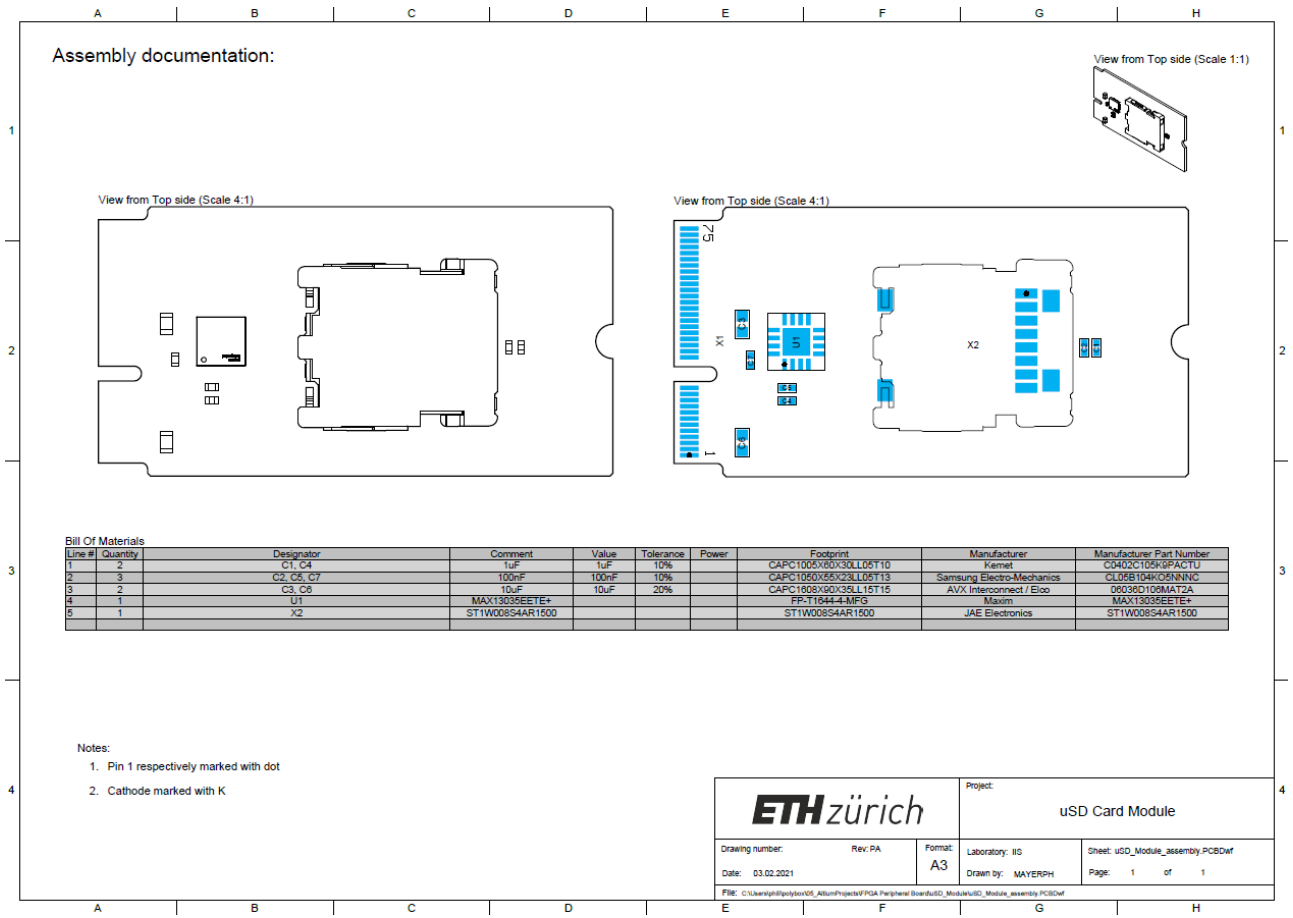
ETH zürich | Project: uSD Card Module | Drawing number: | Rev: PA | Format: A3 | Laboratory: IIS | Drawn by: MAYERPH | Date: 01.02.2021 | Sheet: uSD_Module_fabrication.PCBDwf | Page: 1 of 1



Documentation

Assembly data:

- Pick and Place
- *_ASM.pdf
  assembly plan, BOM



Assembly documentation:

View from Top side (Scale 1:1)

View from Top side (Scale 4:1)

View from Top side (Scale 4:1)

Bill Of Materials

Line #	Quantity	Designator	Comment	Value	Tolerance	Power	Footprint	Manufacturer	Manufacturer Part Number
1	2	C1, C4	1uF	1uF	10%		CAPC1005X60X30LL05T10	Kemet	C0402C105K9PACTU
2	3	C2, C5, C7	100nF	100nF	10%		CAPC1050X55X23LL05T13	Samsung Electro-Mechanics	CL05B104KO5NNNC
3	2	C3, C6	10uF	10uF	20%		CAPC1608X90X35LL15T15	AVX Interconnect / Elco	06036D106MAT2A
4	1	U1	MAX13035EETE+				FP-T1644-4-MFG	Maxim	MAX13035EETE+
5	1	X2	ST1W008S4AR1500				ST1W008S4AR1500	JAE Electronics	ST1W008S4AR1500

Notes:

1. Pin 1 respectively marked with dot
2. Cathode marked with K

ETH zürich

Project: uSD Card Module

Drawing number: Rev: PA

Format: A3

Date: 03.02.2021

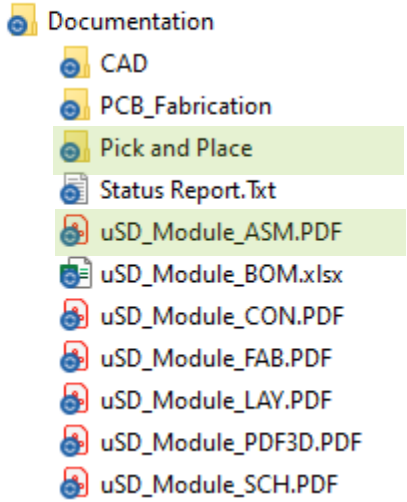
Laboratory: IIS

Drawn by: MAYERPH

Sheet: uSD_Module_assembly.PCBDwf

Page: 1 of 1

File: C:\Users\phil\Polybox\05_AltiumProjects\FPGA Peripheral Boards\uSD_Module\uSD_Module_assembly.PCBDwf

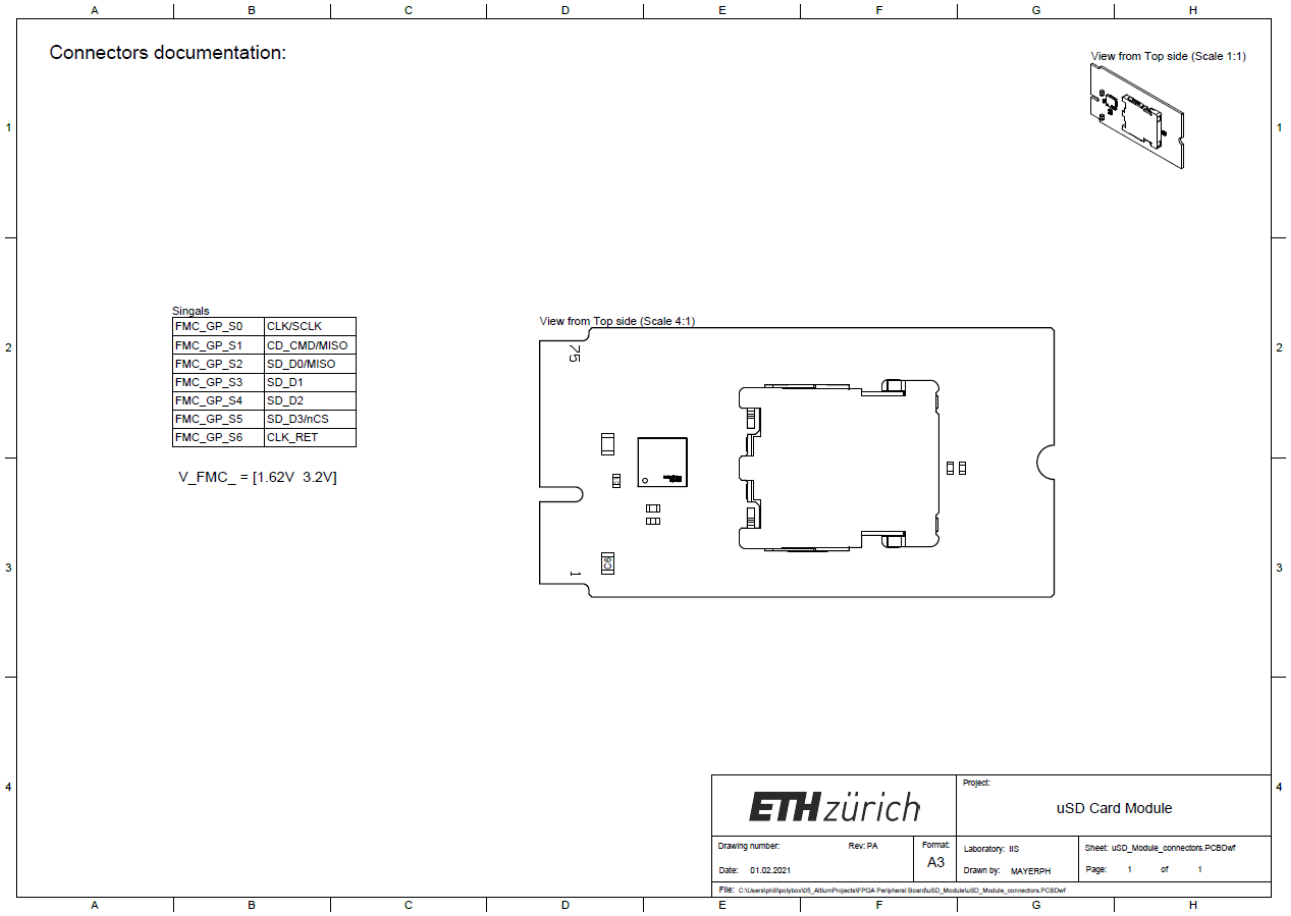


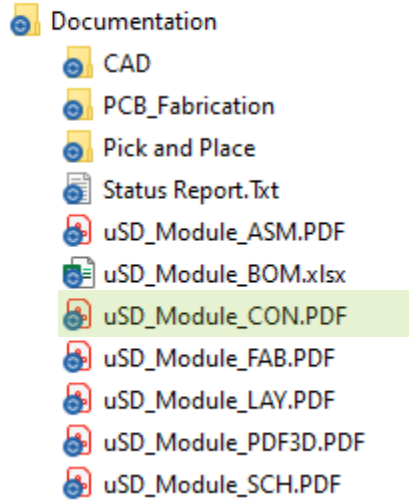
Documentation

Applicaiton data:

- *_CON.pdf

supported voltage levels
used IOs, etc.





Creating a New Module

- Modify the “Example Module” project
  - Predifined schematic and PCB skeleton
  - Inline comments to guide through the modifications
  - Semiautomated documentation