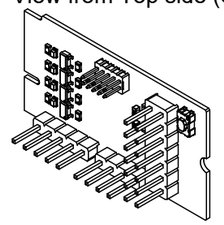
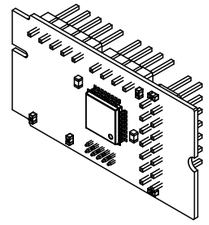
Layout documentation:

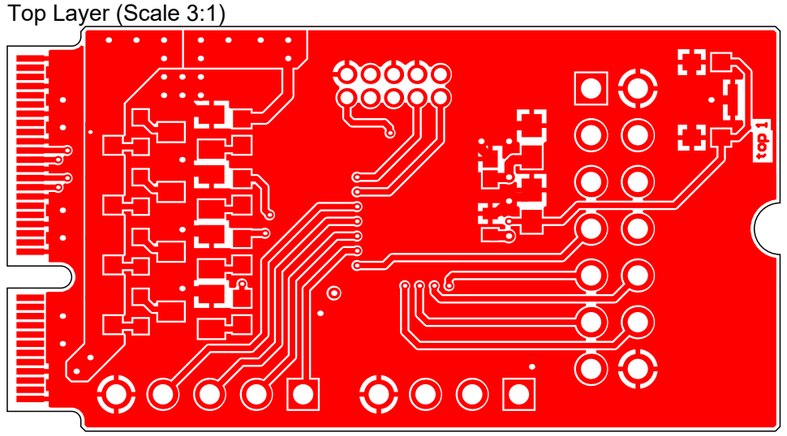
View from Top side (Scale 1:1)



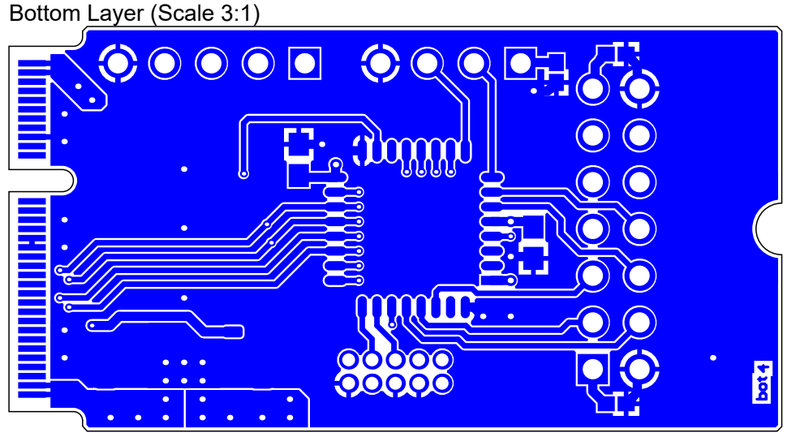
View from Bottom side (Scale 1:1)



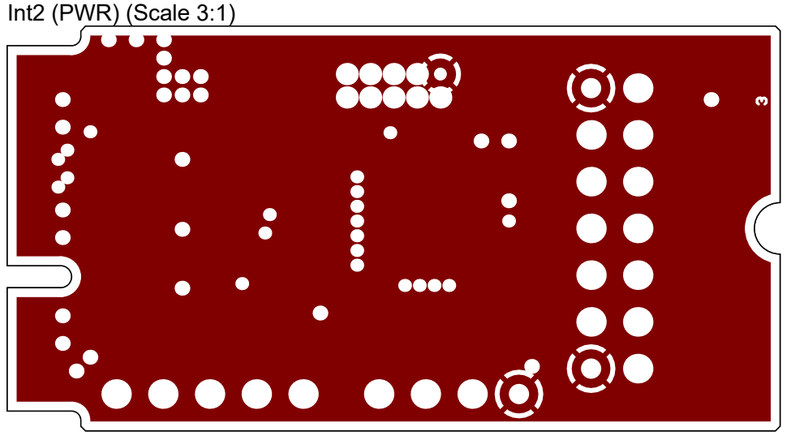
Top Layer (Scale 3:1)



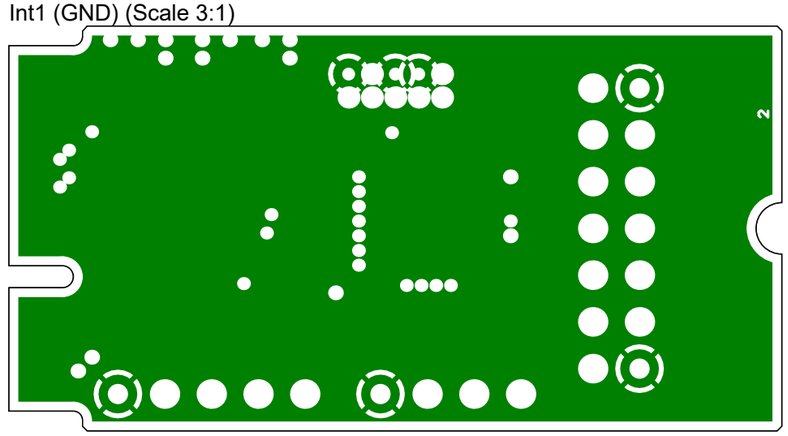
Bottom Layer (Scale 3:1)



Int2 (PWR) (Scale 3:1)



Int1 (GND) (Scale 3:1)



ETH zürich		Project: UART Module	
Drawing number: Rev: PA Date: 21/12/2022	Format: A3	Laboratory: IIS Drawn by: MAYERPH	Sheet: UART_Module_layout.PCBDwf Page: 1 of 1
File: C:\Users\admin\Desktop\tesi\FMC Peripheral Board\UART_Module\UART_Module_layout.PCBDwf			