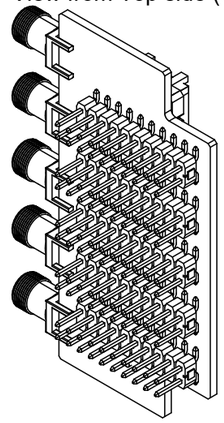
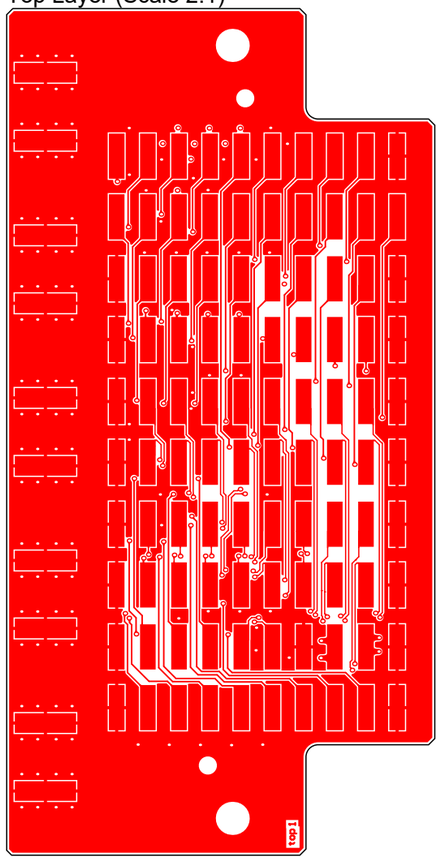
Layout:

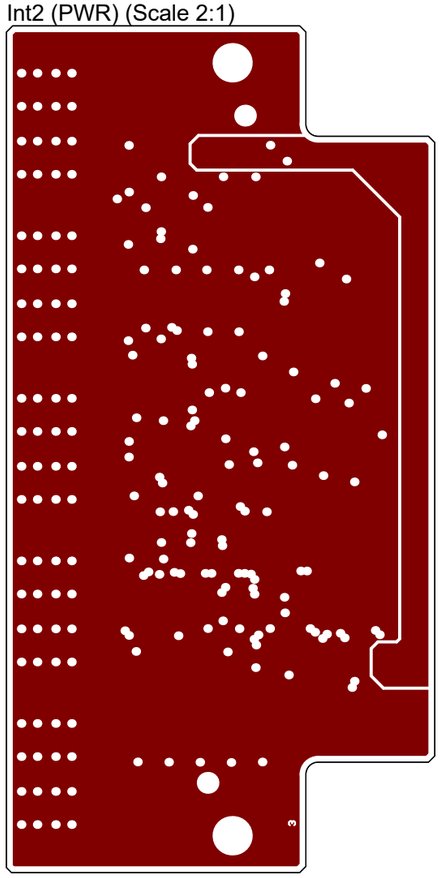
View from Top side (Scale 1:1)



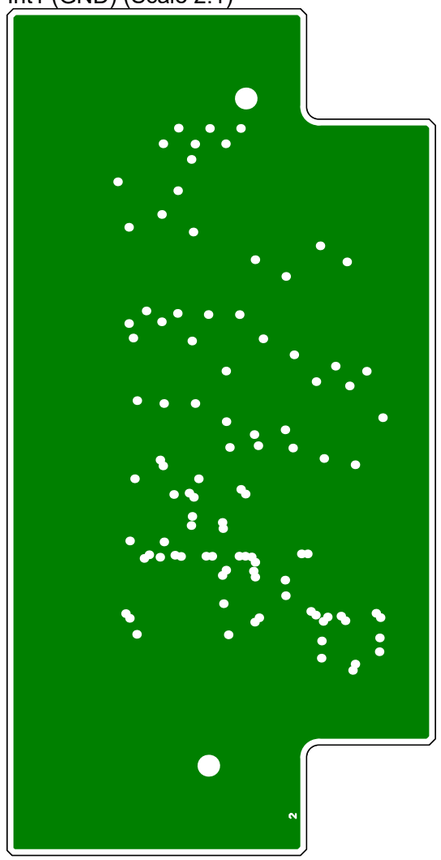
Top Layer (Scale 2:1)



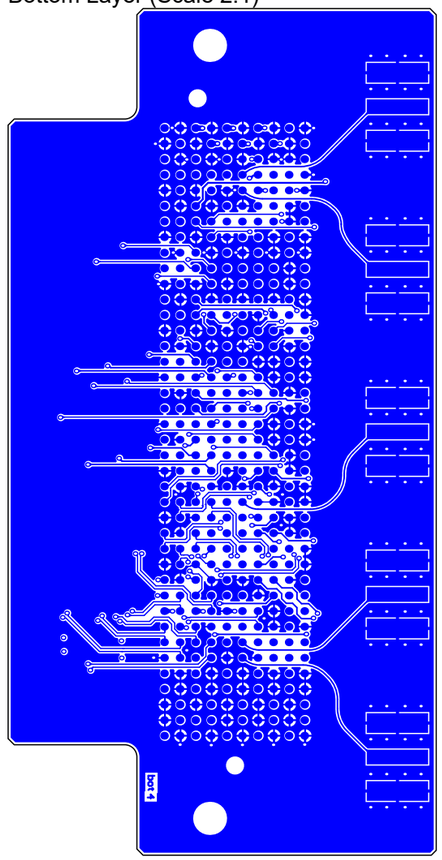
Int2 (PWR) (Scale 2:1)



Int1 (GND) (Scale 2:1)



Bottom Layer (Scale 2:1)



ETH zürich		Project: FMC Test Module	
Drawing number: Rev: A Date: 10.02.2021	Format: A3	Laboratory: IIS Drawn by: MAYERPH	Sheet: FMC_Test_Module_layout.PCBDwf Page: 1 of 1
File: C:\Users\phili\polybox\05_AltiumProjects\FPGA Peripheral Board\FMC_Test_Module\FMC_Test_Module_layout.PCBDwf			