

ETH

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

FPGA Peripherals Board - FMC

Drawing number:

Rev: PA

Format:

Laboratory: IIS

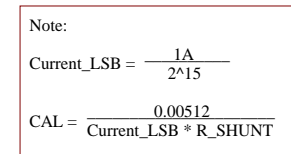
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Date: 11.02.2021 11:44:47

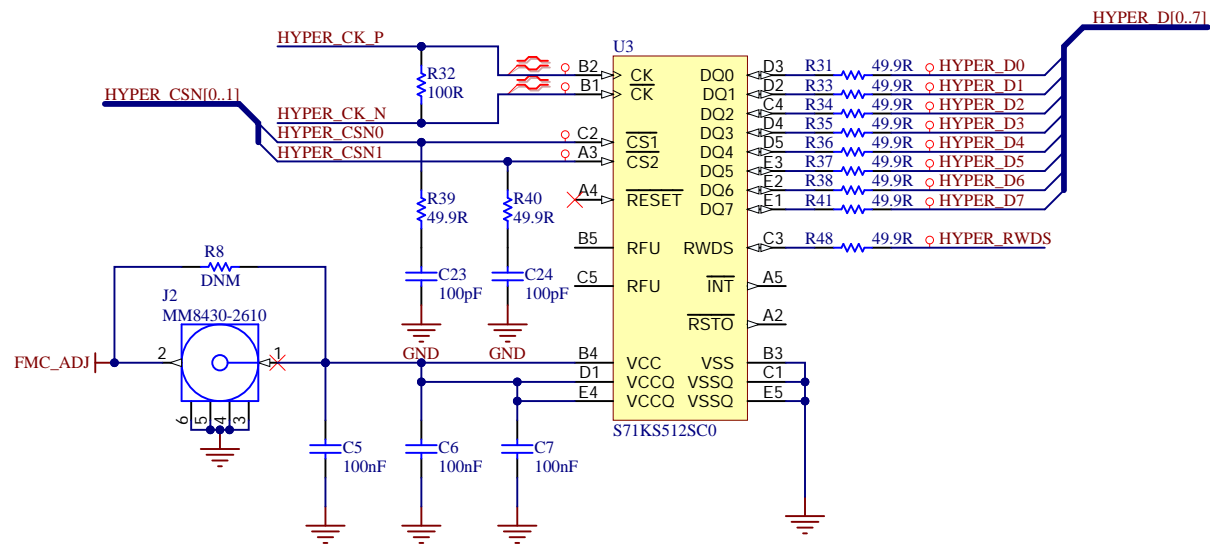
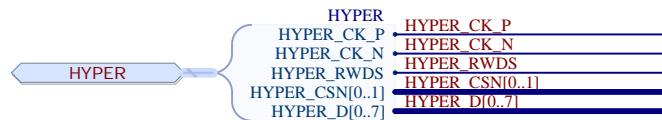
Drawn by: mayerph

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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

FPGA Peripherals Board - HyperRAM / FLASH

Drawing number:

Rev: PA

Format:

Laboratory: IIS

Sheet: HyperBUS_RAM-FLASH.SchDoc

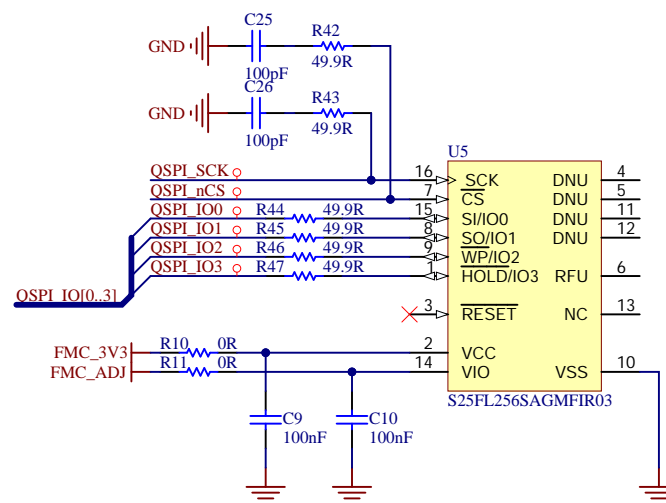
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A4 Q

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**ETH**

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

FPGA Peripherals Board - FLASH

Drawing number:

Rev: PA

Format:

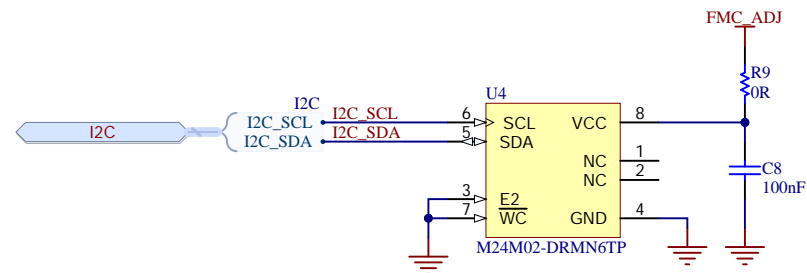
Laboratory: IIS

mayerph

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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

FPGA Peripherals Board - EEPROM

Drawing number:

Rev: PA

Format:

Laboratory: IIS

Sheet: I2C_EEPROM.SchDoc

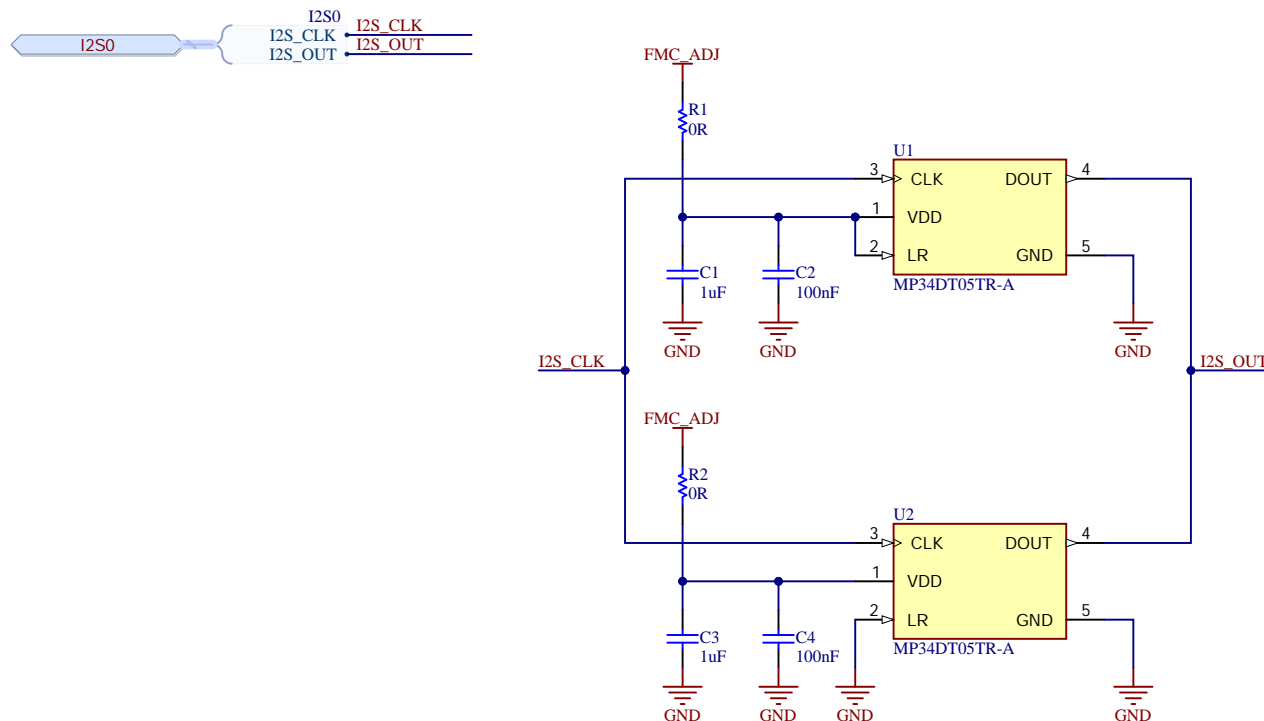
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Drawn by: mayerph

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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

FPGA Peripherals Board - MIC

Drawing number:

Rev: PA

Format:

Laboratory: IIS

Sheet: I2S_Mic.SchDoc

Date: 11.02.2021 11:44:48

A4 Q

Drawn by: mayerph

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