Interface
Power Path
Memory
Sensors

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: uSD Card Module - Main

Drawing number: Rev: PA	Format: A4 Q	Laboratory: IIS	Sheet: main.SchDoc
Date: 22/12/2022 17:15:01		Drawn by: mayerph	Page 1 of 3
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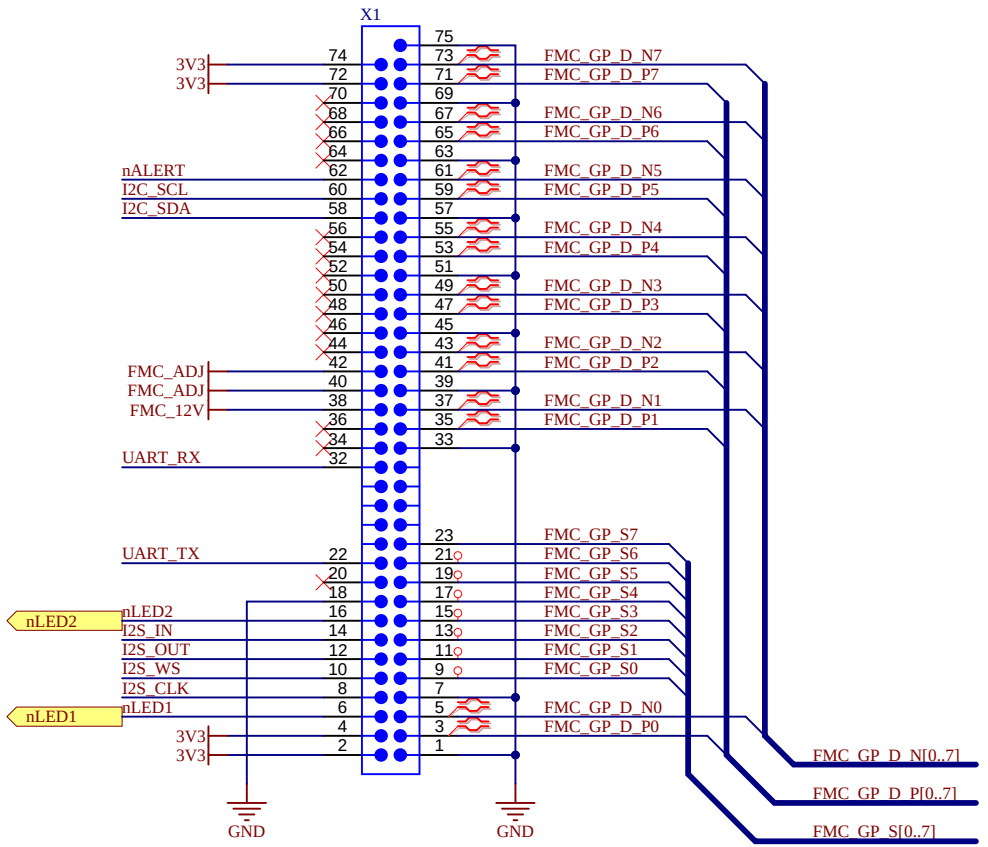

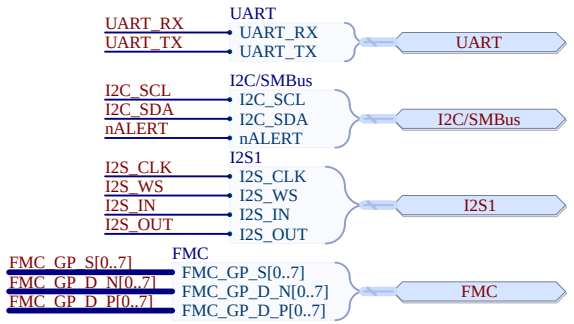

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: UART Module - Connector

Drawing number:	Rev: PA	Format: A4 Q	Laboratory: IIS	Sheet: connector.SchDoc	
Date: 22/12/2022 17:15:01			Drawn by: mayerph	Page 2	of 3
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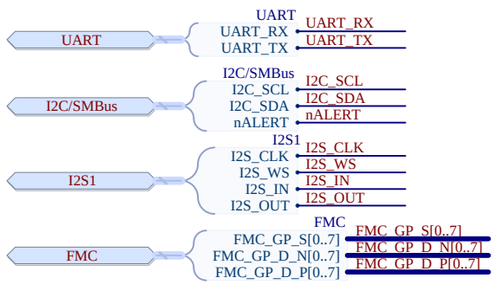
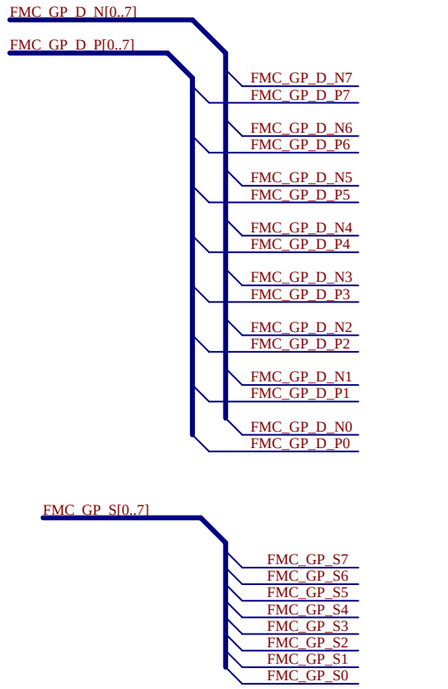
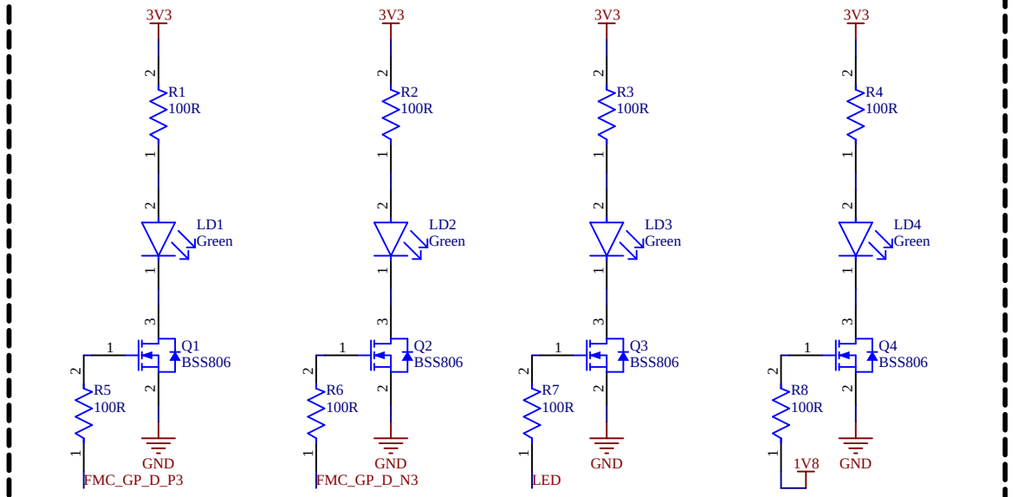
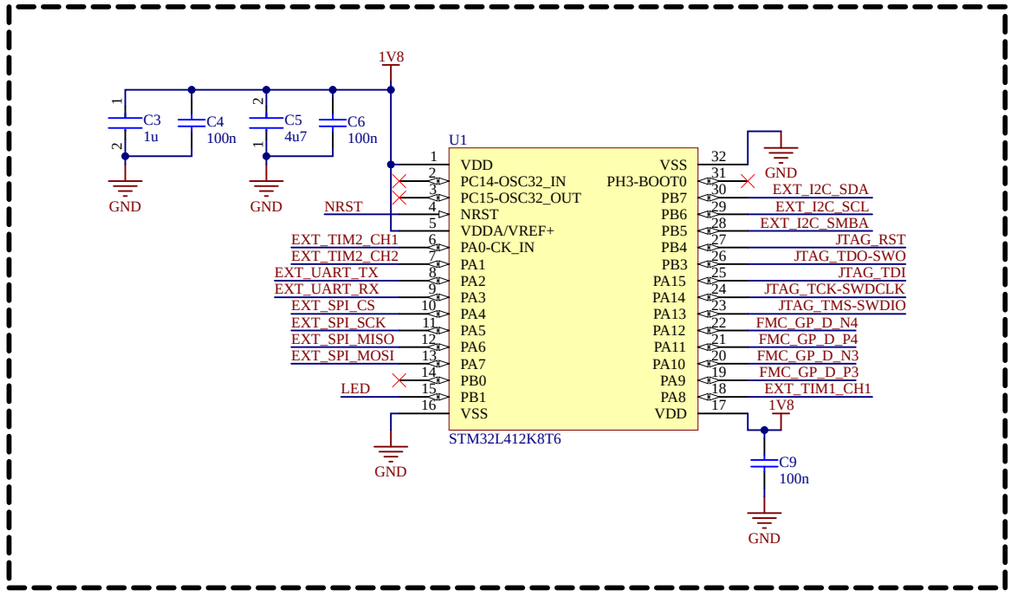




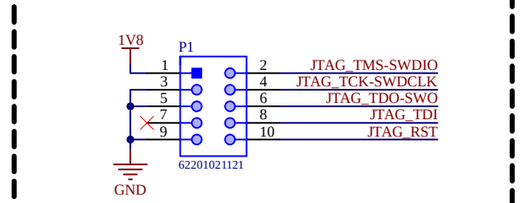
LED indicators



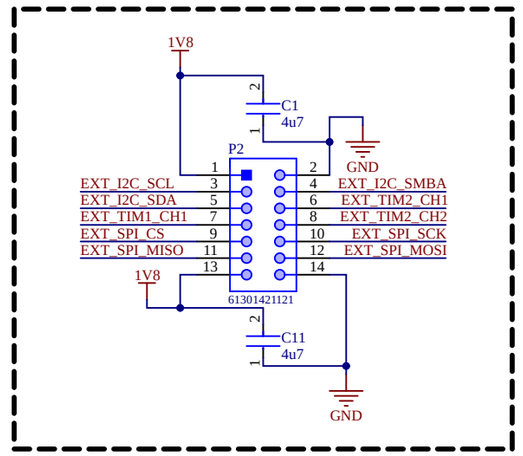
MCU



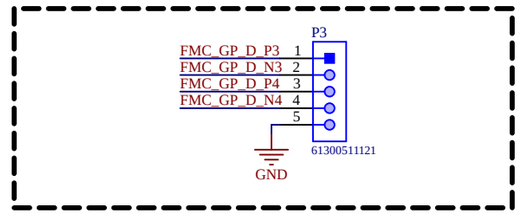
JTAG



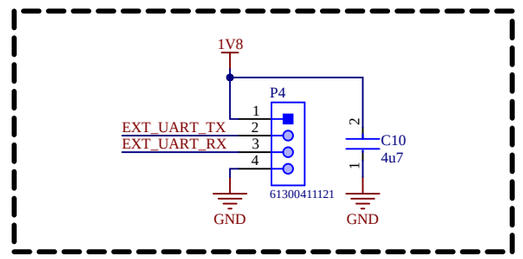
External GPIO



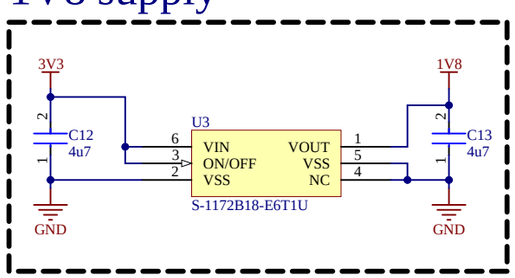
UART to FPGA



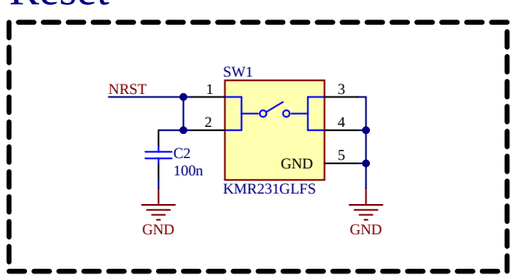
External UART



1V8 supply



Reset



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: UART Module
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