7. Design of Logic gates using NMOS, PMOS and Resistor

Course: ECE1008 – Electronic Hardware Troubleshooting LAB

-Dr Richards Joe Stanislaus

Assistant Professor - SENSE

Email: 51749@vitstudent.ac.in

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CHENNAI

1. Logic Level

- If V_{DD} is the power supply voltage
  Logic 1: Voltages close to V_{DD}
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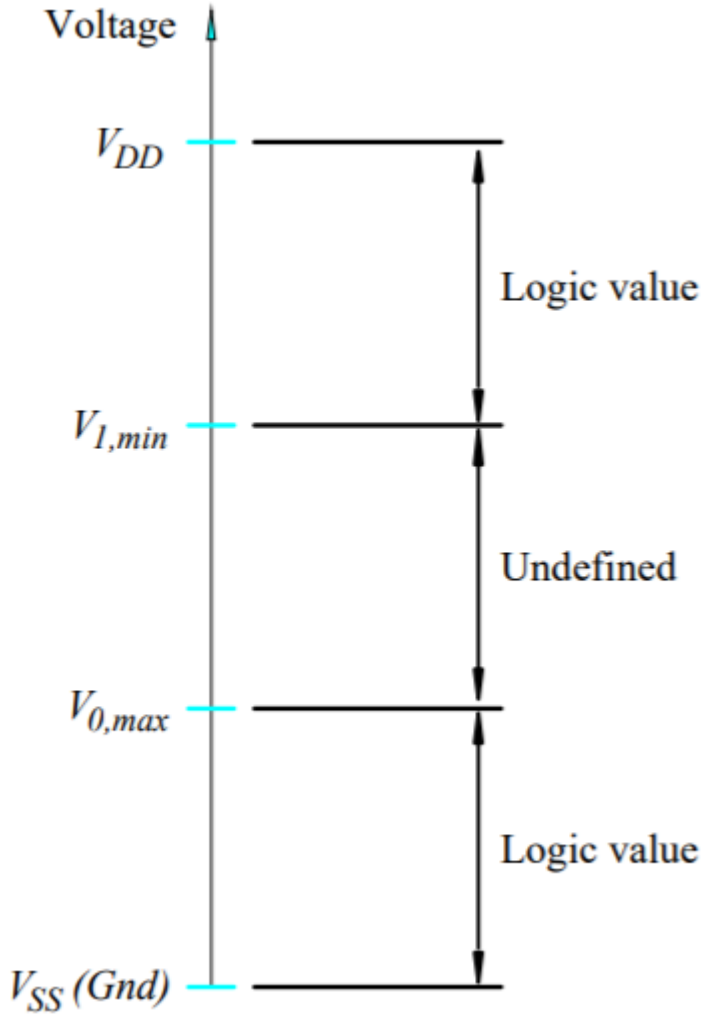

https://people.engr.tamu.edu/xizhang/ECEN248/Chapter_3_Lecture_Notes_Xi_Zhang.pdf

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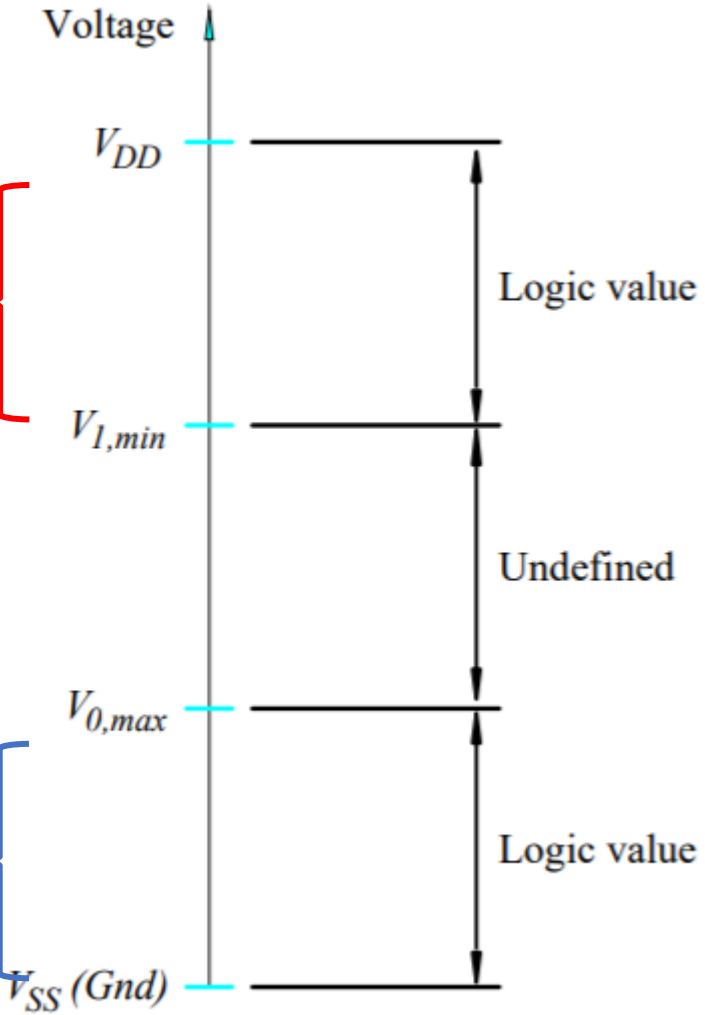

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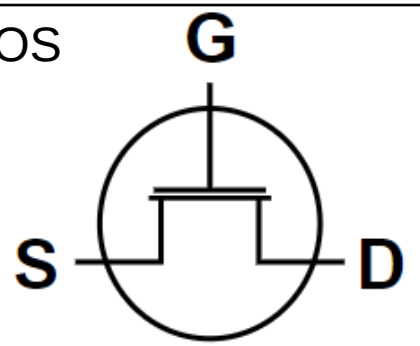
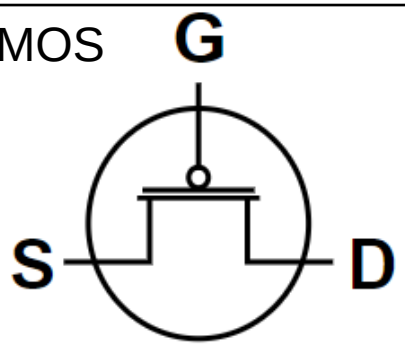
2. NMOS and PMOS – Gate control

	NMOS 	PMOS 

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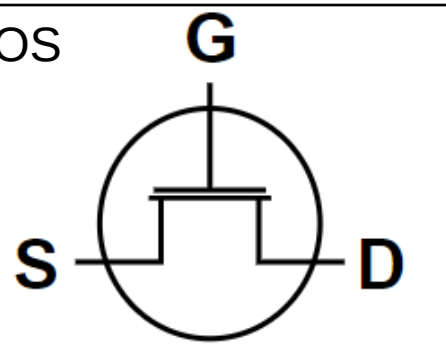
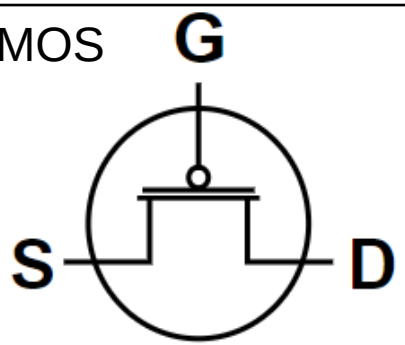
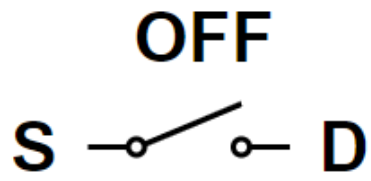
		
Gate is LOW		

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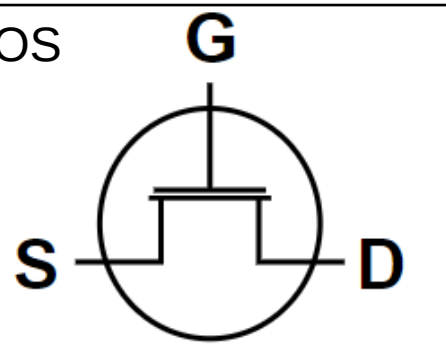
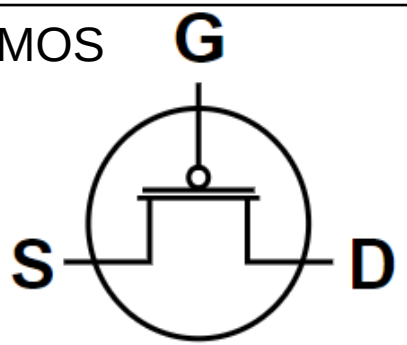
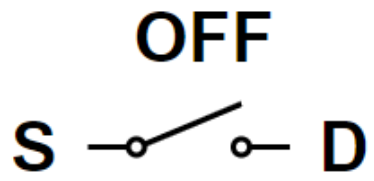
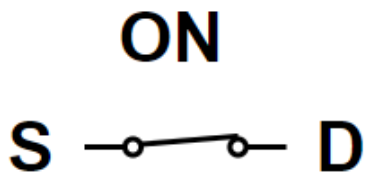
		
Gate is LOW		

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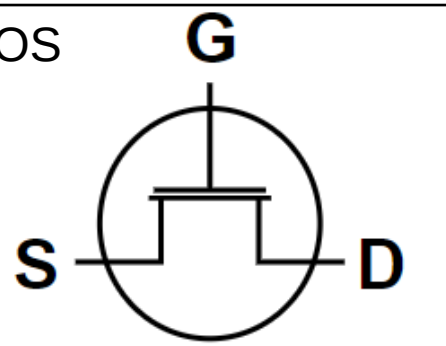
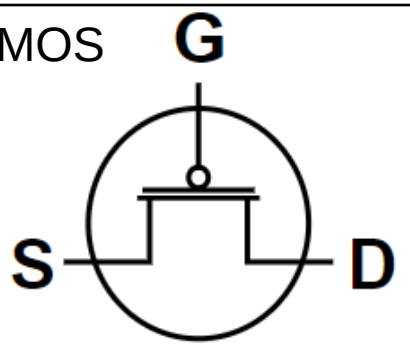
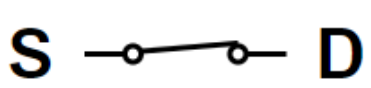
	NMOS 	PMOS 
Gate is LOW		
Gate is HIGH		

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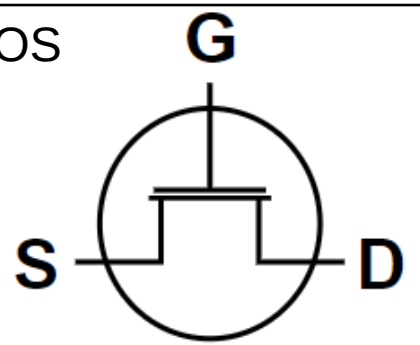
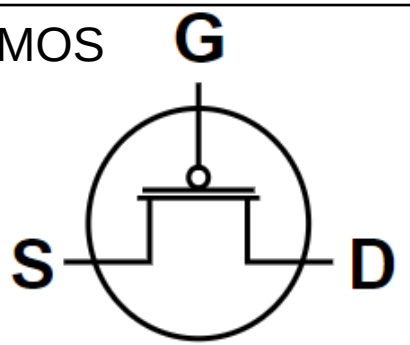
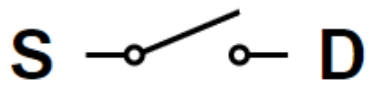
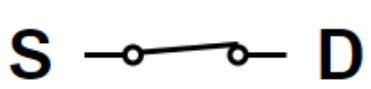
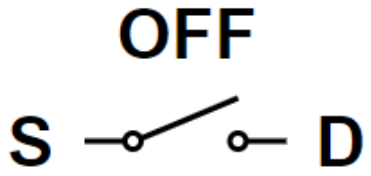
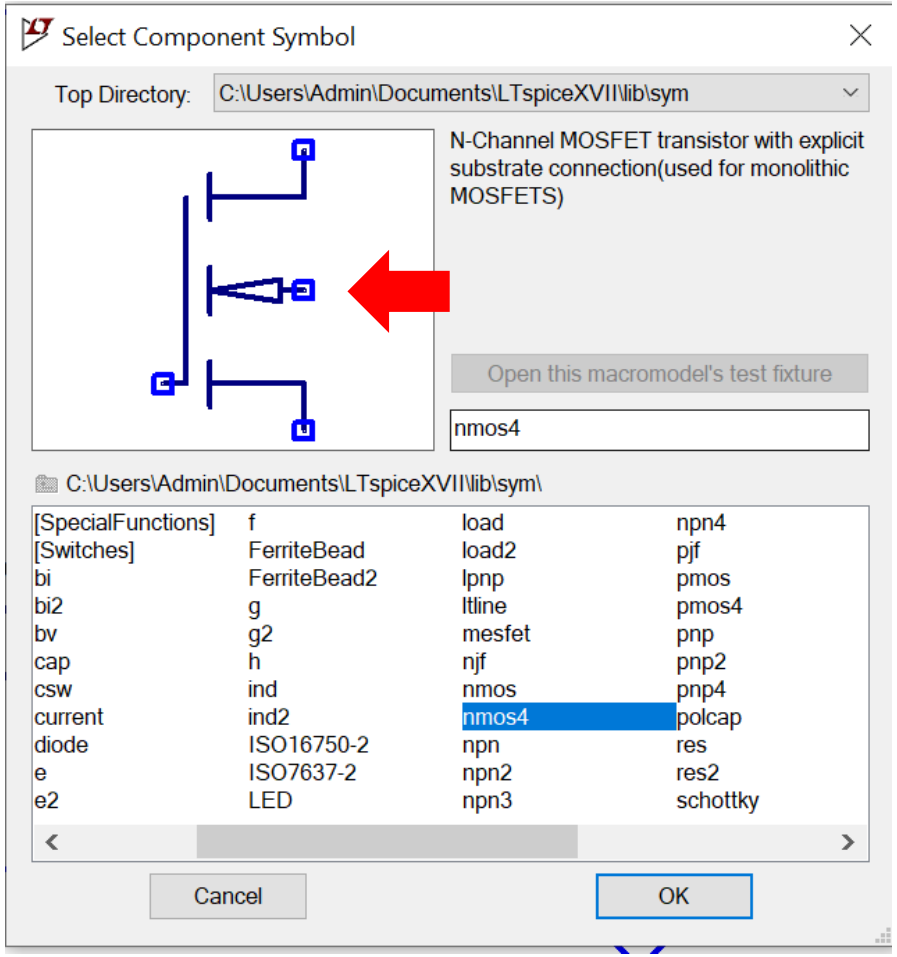
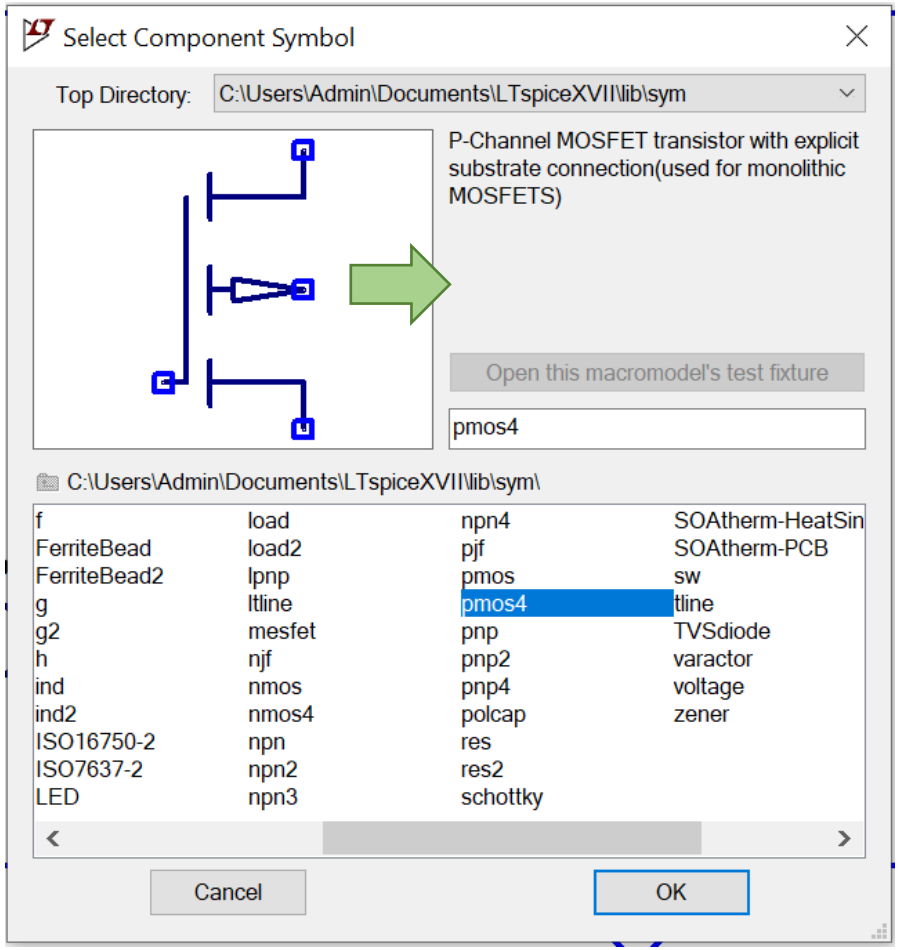
		
Gate is LOW		
Gate is HIGH		

2. NMOS and PMOS – Gate control

- Select NMOS4 and PMOS4 for this experiment (4 independent contacts)

NOTICE the arrow. **NMOS: Inward arrow** **PMOS: Outward arrow**





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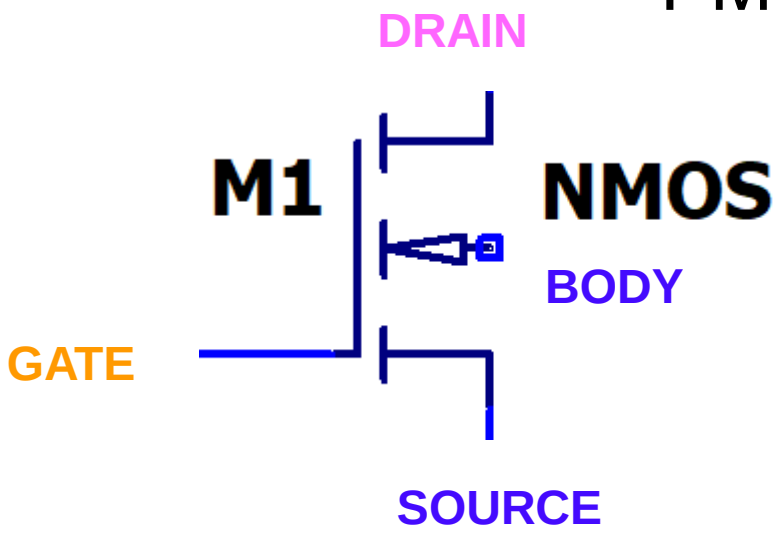
- Remember: NMOS – Source is at LOW(ground)
  PMOS – Source is at HIGH(V_dd) – Must rotate/mirror the symbol using (ctrl+R) or (ctrl+E)
- In both NMOS4 and PMOS4
  Source is near by Gate in the symbol.
  Remember to connect NMOS's body to ground and PMOS's body to Supply.



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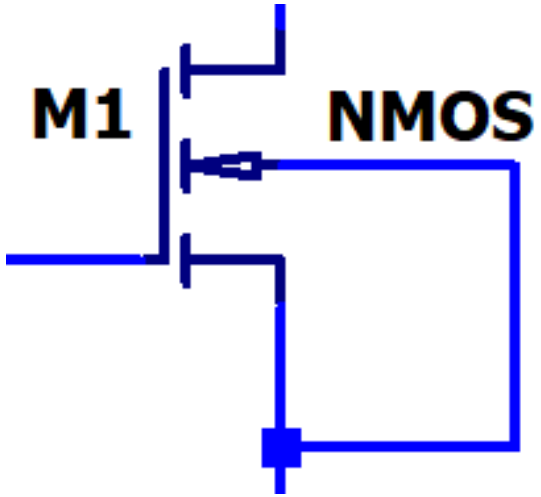


Important NOTE

- Enter your **registration number** and **Full Name** next to

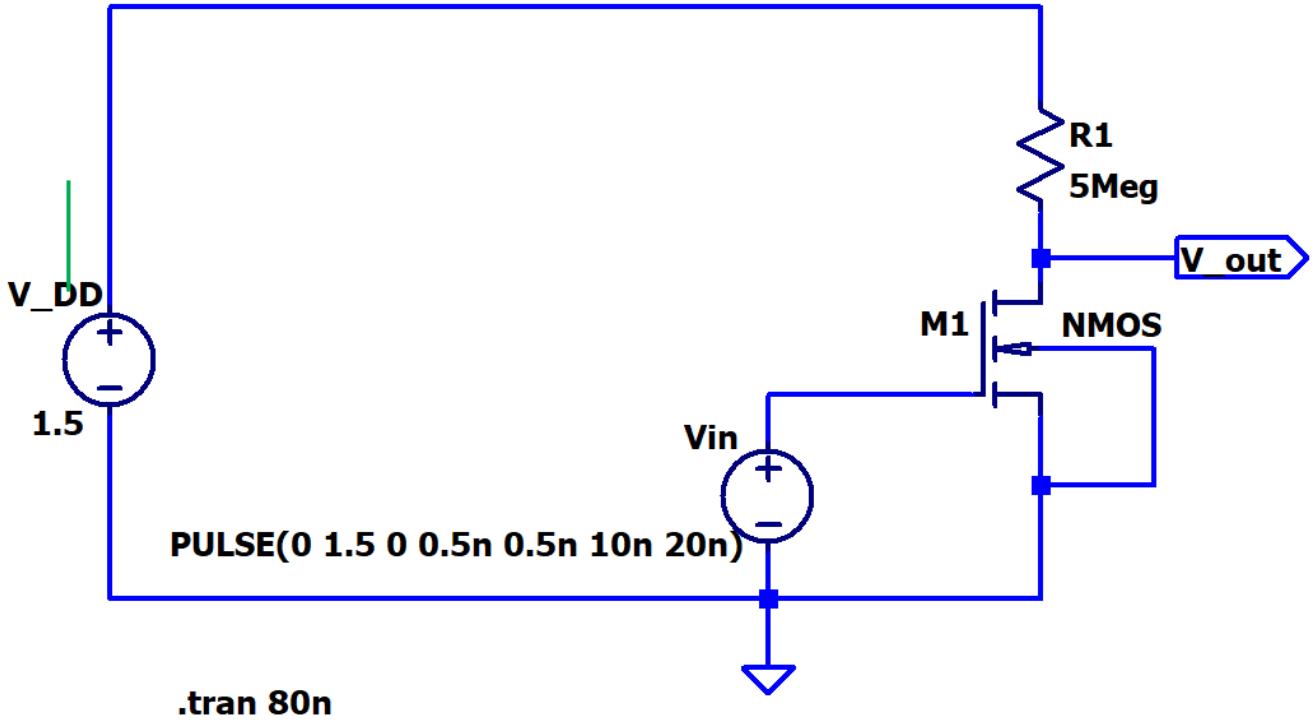
  all your circuits and the output plots.

- Keep the background of circuit and plot as white.

And place a truth table for each logic gate.

Task 1.1: NOT GATE with NMOS

- Remember to Connect NMOS body to ground.



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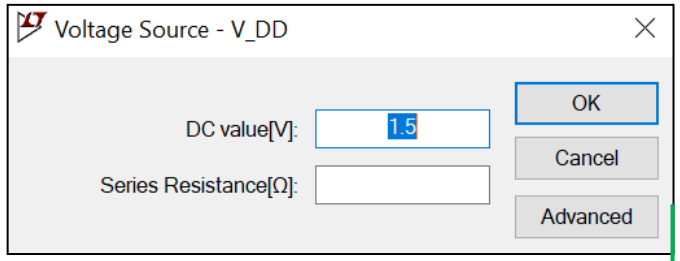
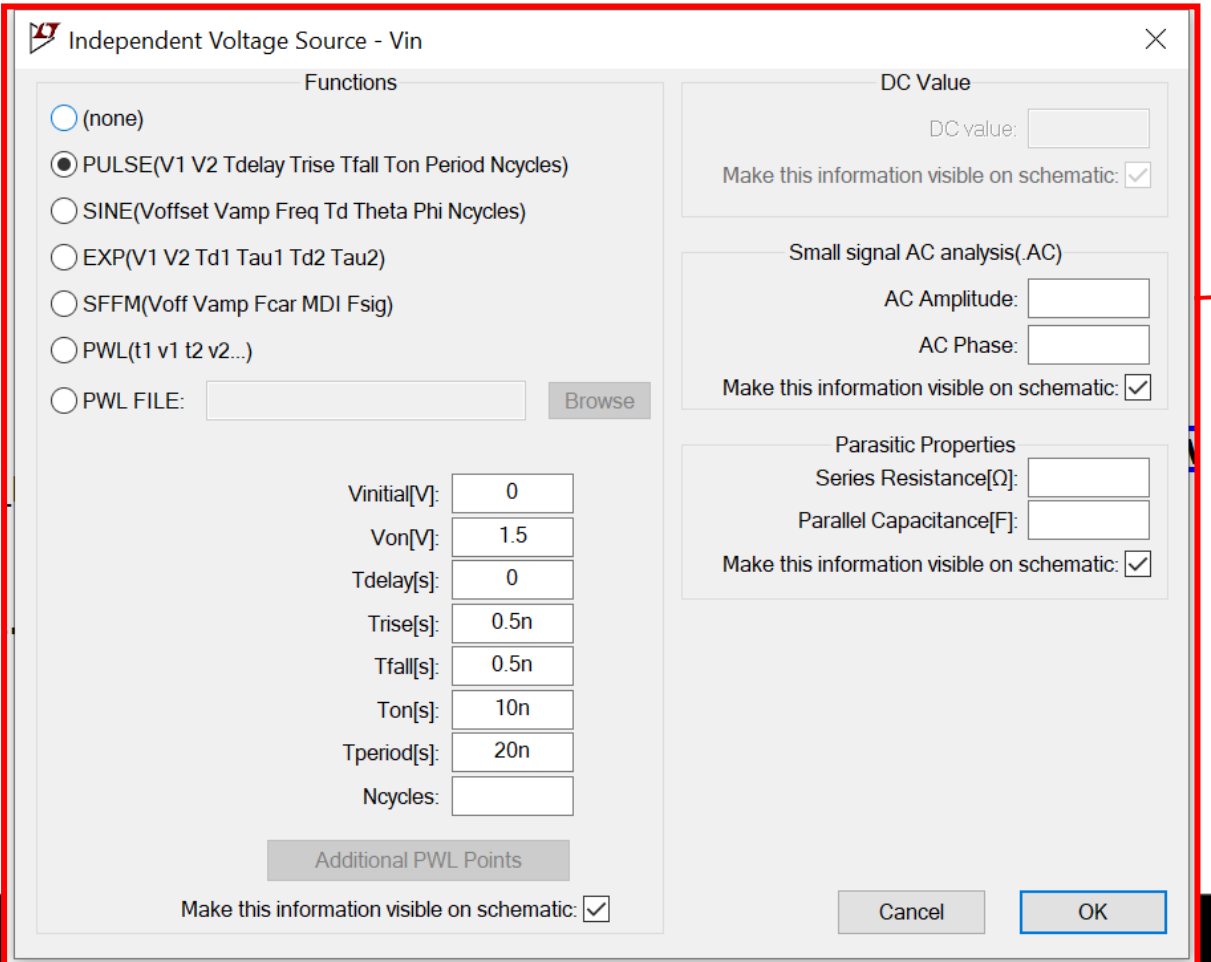
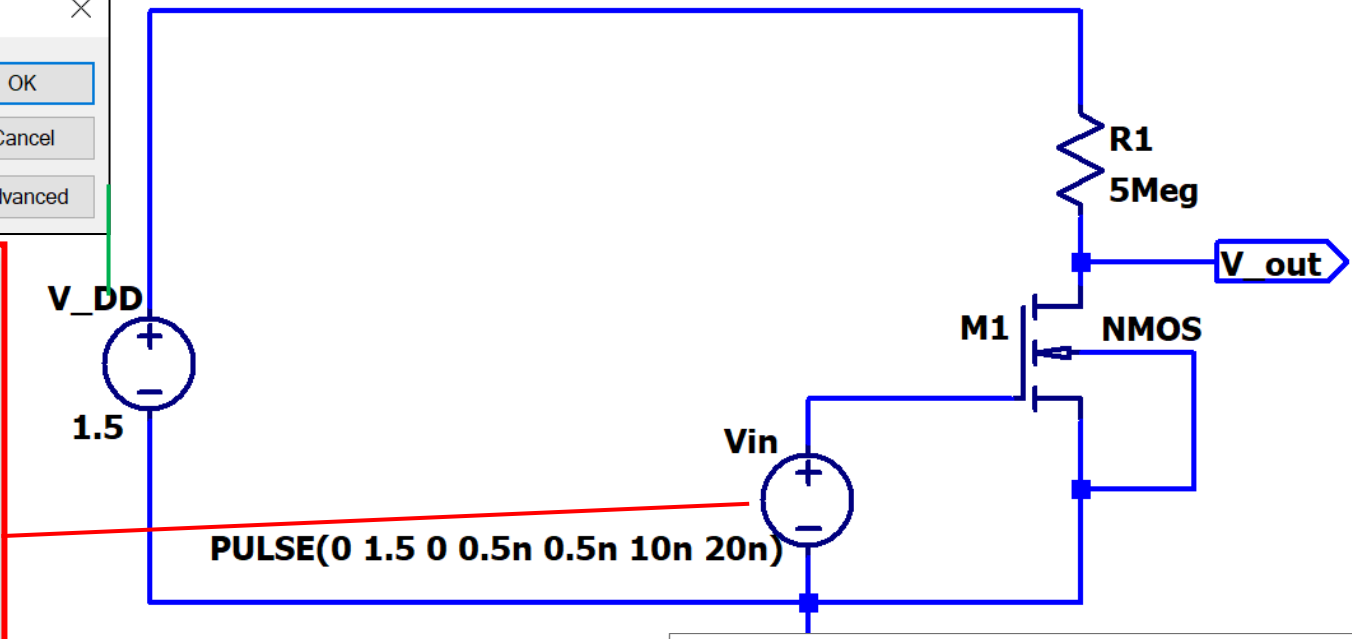
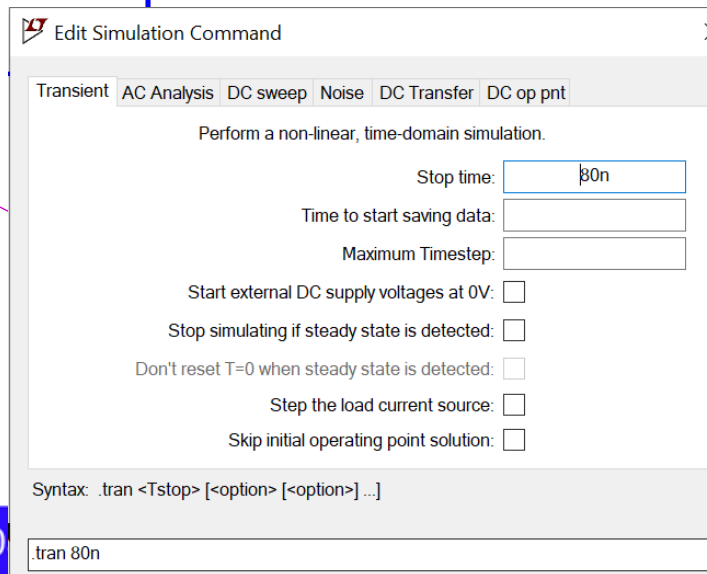






.tran 80n



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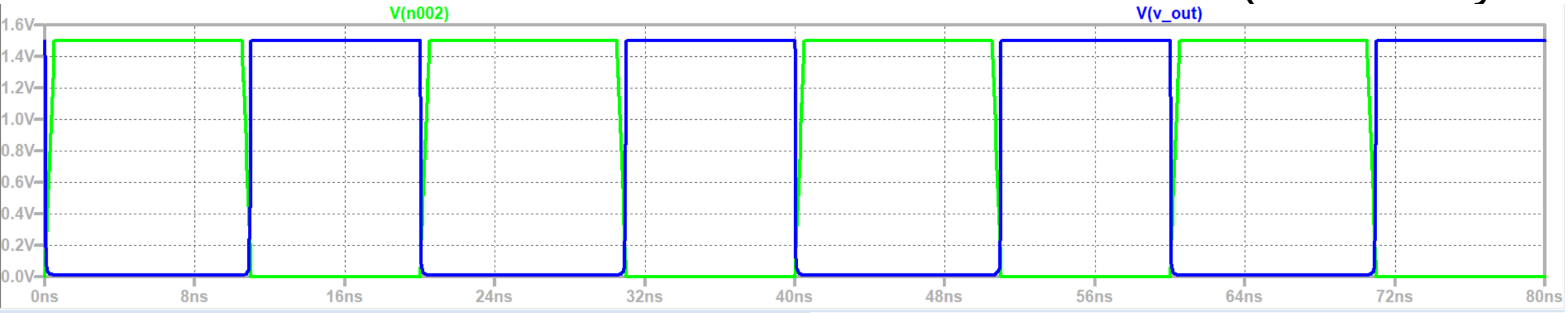

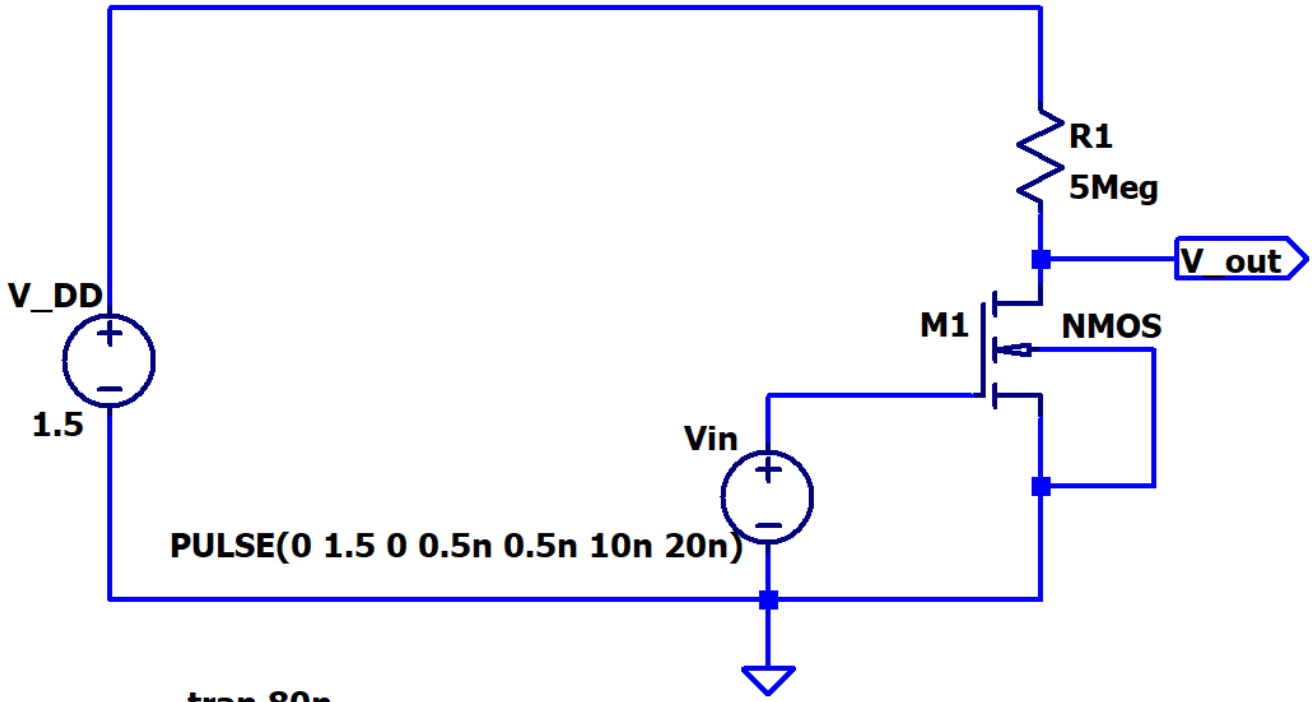

Task 1.2: NOT GATE with PMOS (PMOS4 symbol)

- Remember to rotate the PMOS such that Source (which is near gate) is towards V_{DD} (power supply) for PMOS.
- Also, remember to connect body and power supply

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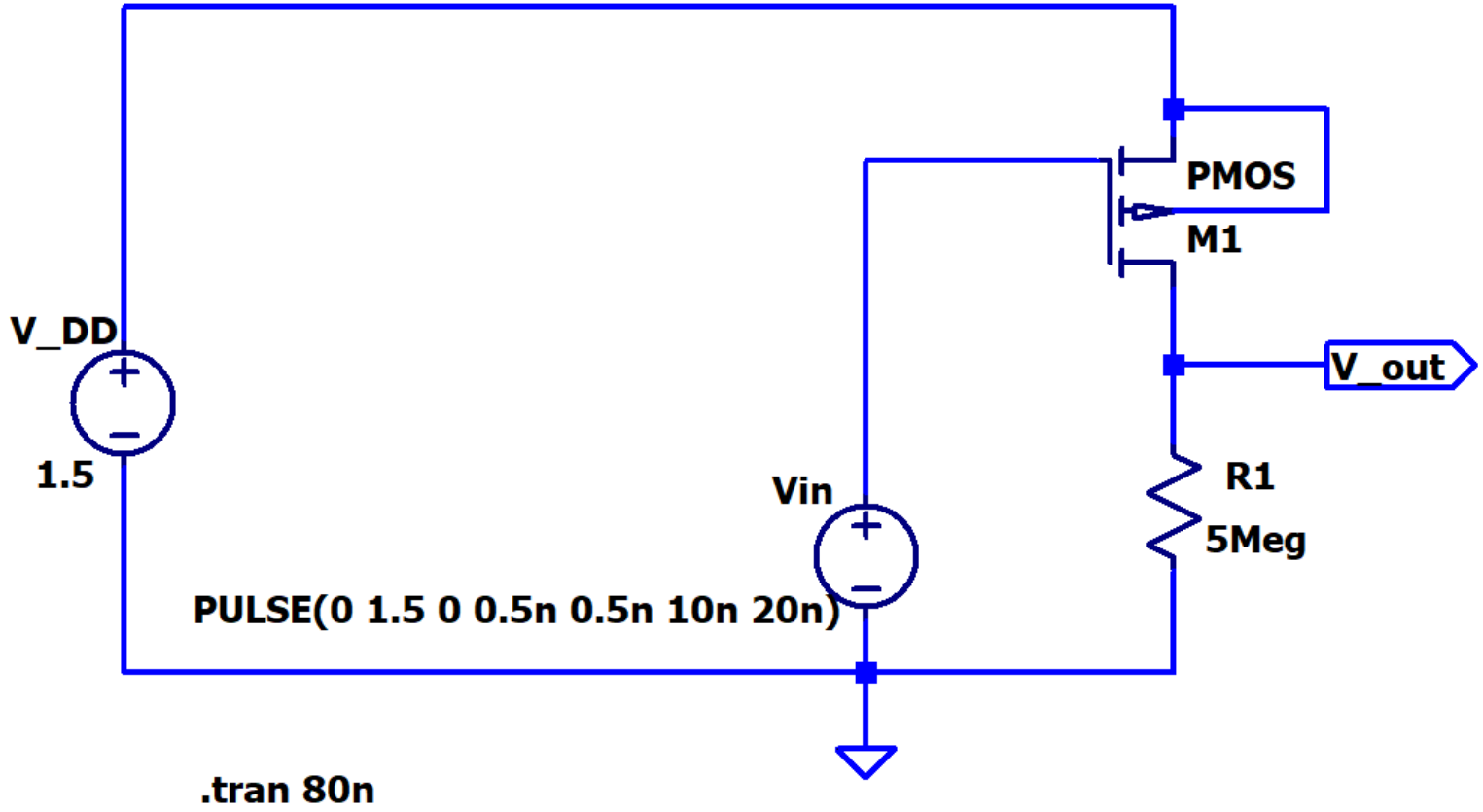

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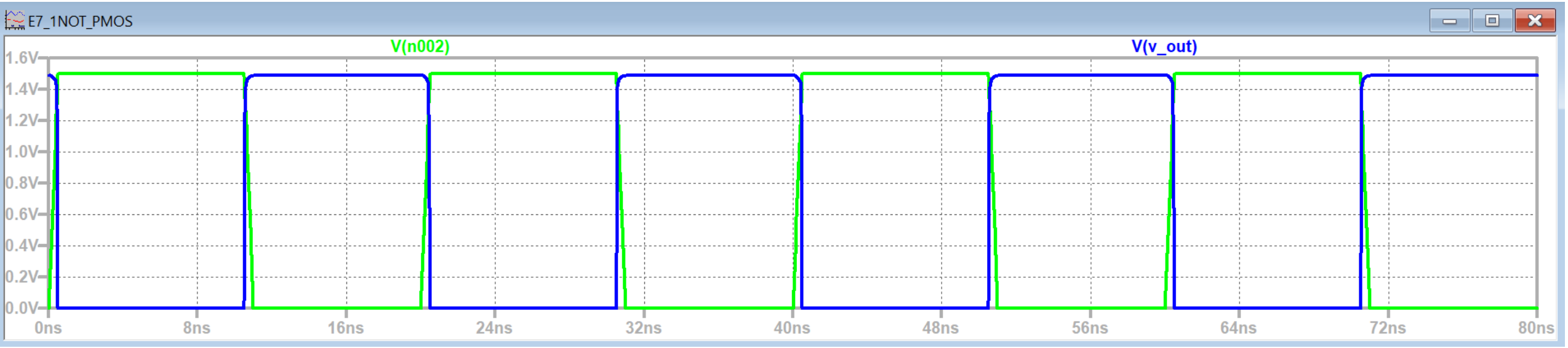

Task 2.1: NAND GATE Using NMOS(NMOS4 symbol)

- $V_{out} = \overline{V_A \cdot V_B}$

- In NMOS configuration rephrase the output expression under bar, and the expression which is under bar, implement that expression using NMOS.
- Note: SUM – Parallel; PRODUCT – SERIES.

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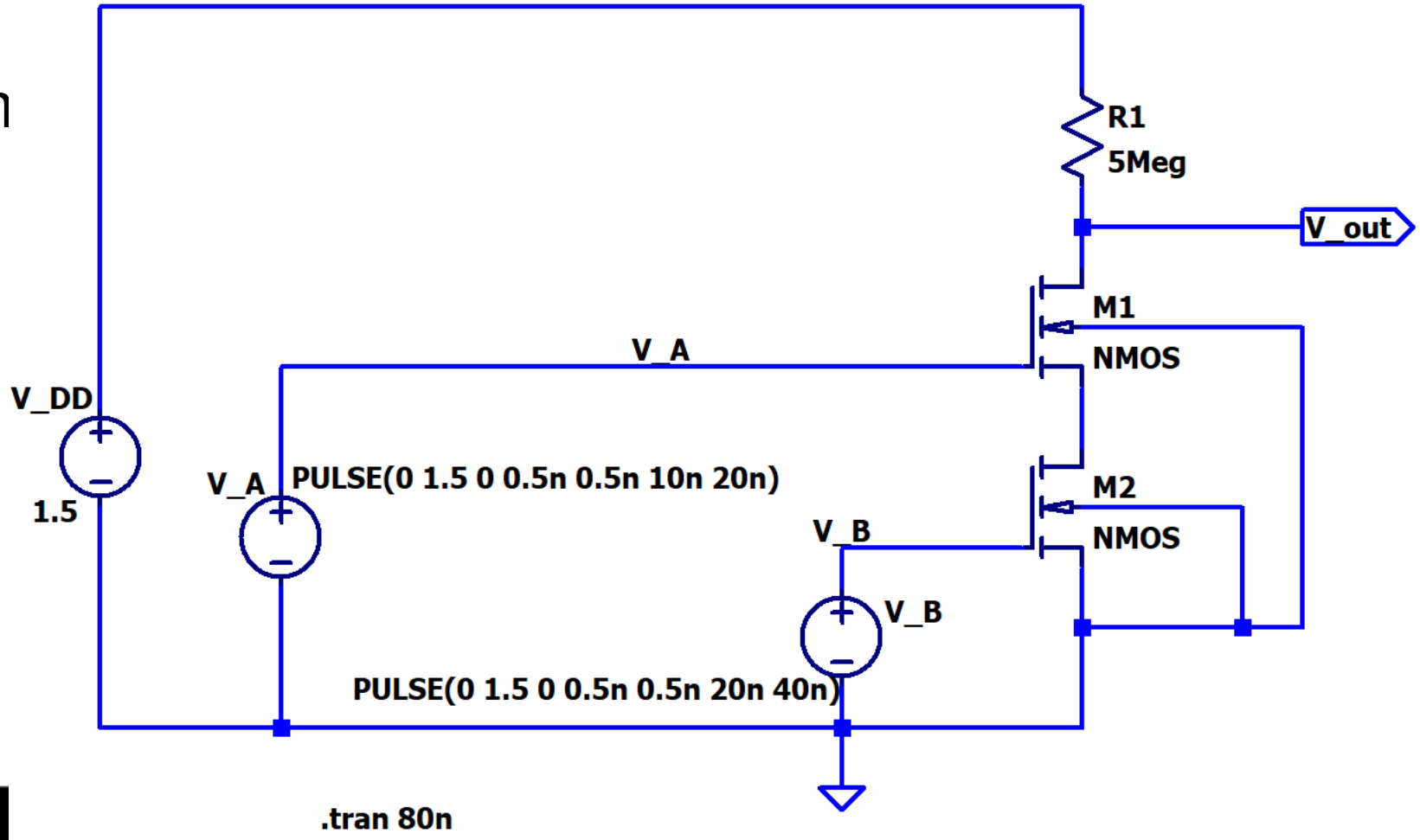
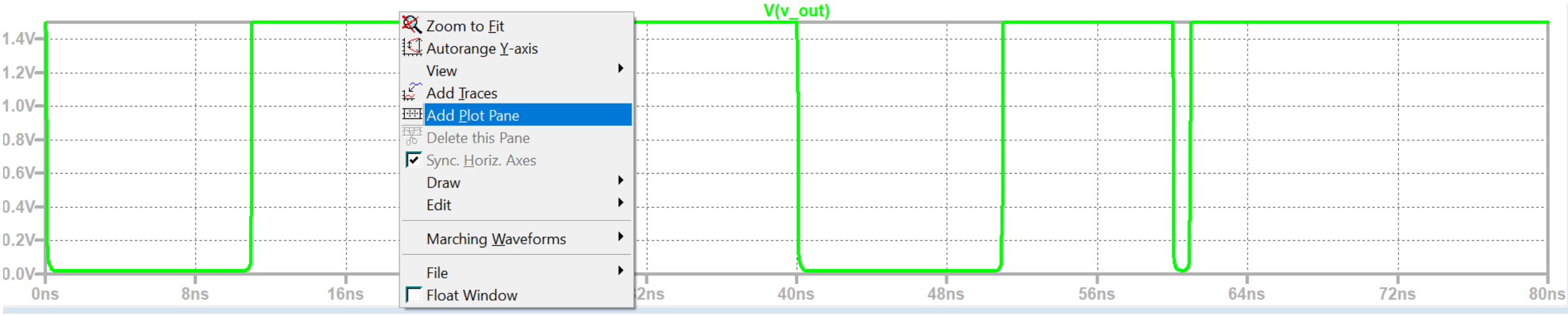


Task 2.1: NAND GATE Using NMOS(NMOS4 symbol)

- After plotting one plot
- Right click at plot and select “Add Plot Pane”



- Select the next output to be plotted in new sub plot

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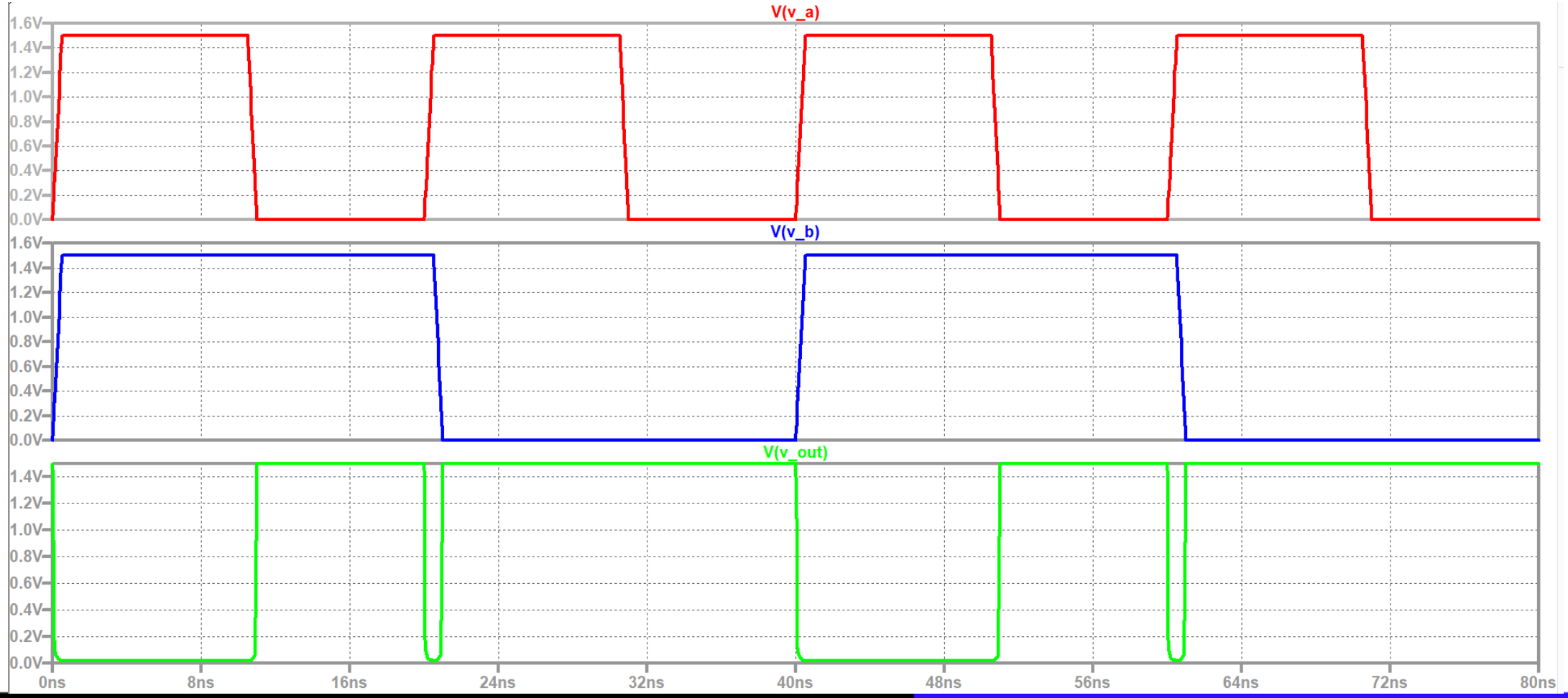
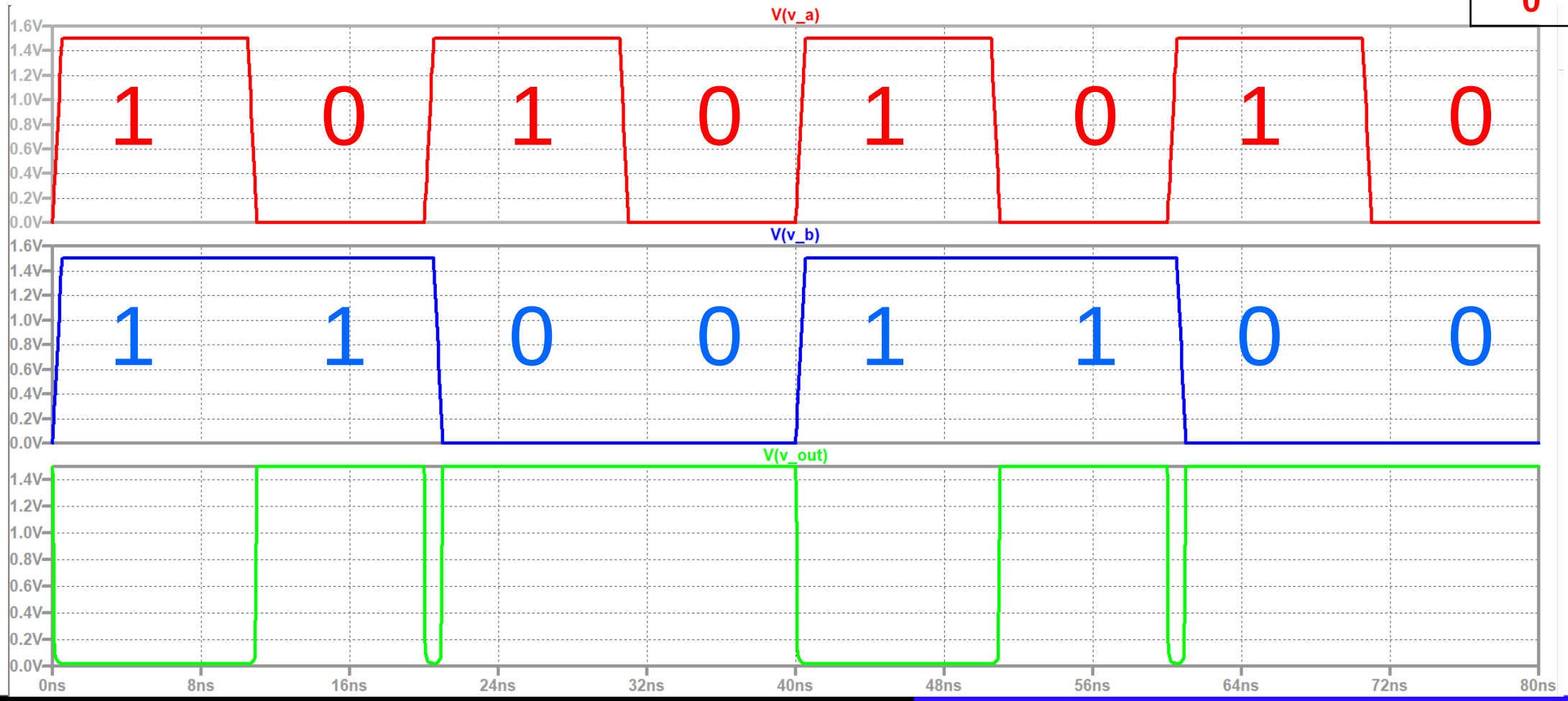


Task 2.1: NAND GATE Using NMOS

V_A	V_B	V_out
1	1	0
0	1	1
1	0	1
0	0	1



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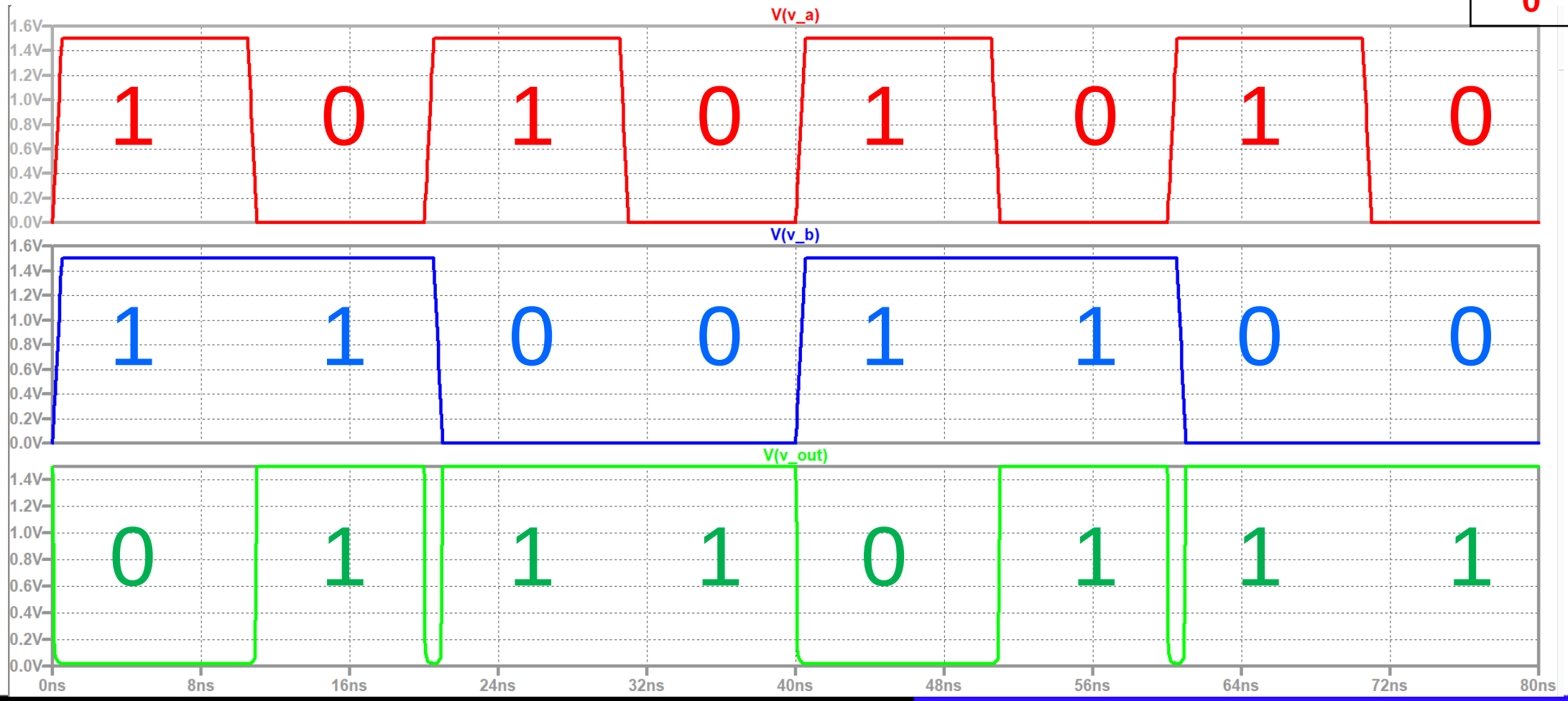

Task 2.2: NAND GATE Using PMOS(PMOS4 symbol)

- $V_{out} = \overline{V_A \cdot V_B} = \overline{V_A} + \overline{V_B}$ (DeMorgan's theorem)

- In PMOS configuration rephrase the output expression such that every element is under bar individually and then implement using PMOS.
- Note: SUM – Parallel; PRODUCT – SERIES.

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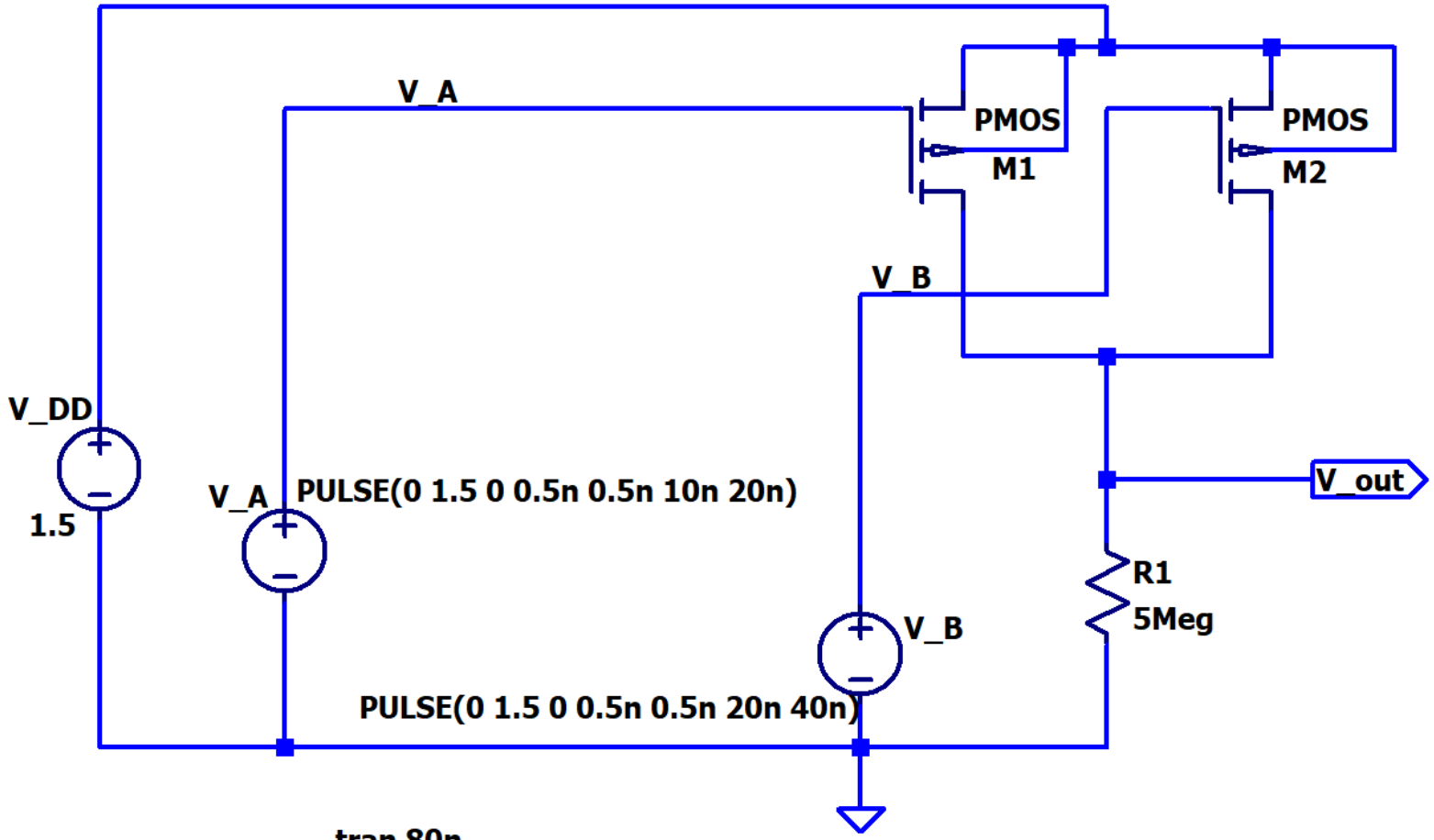

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- Remember to rotate the PMOS such that Source (which is near gate) is towards V_{DD} (power supply) for PMOS.
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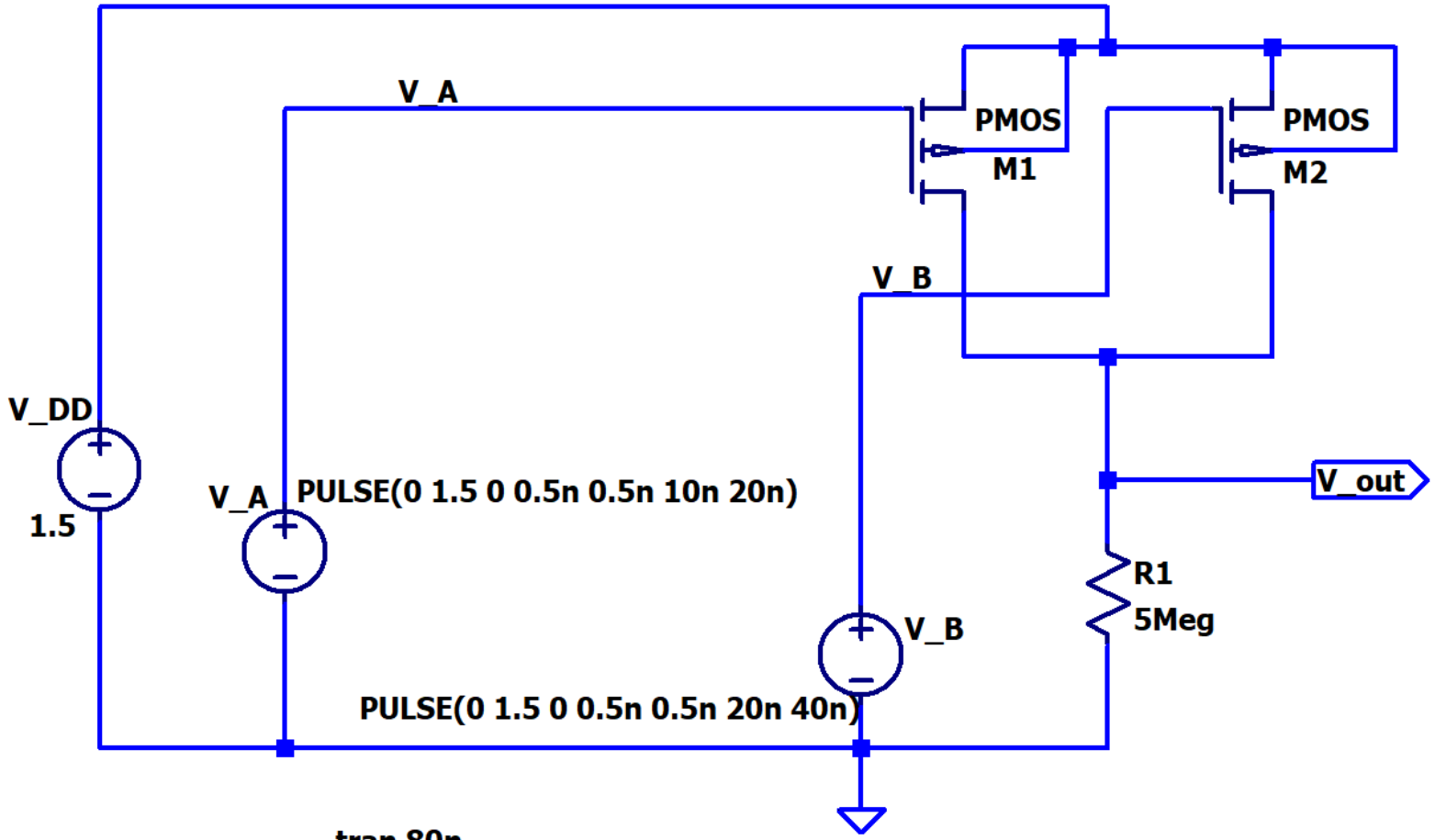

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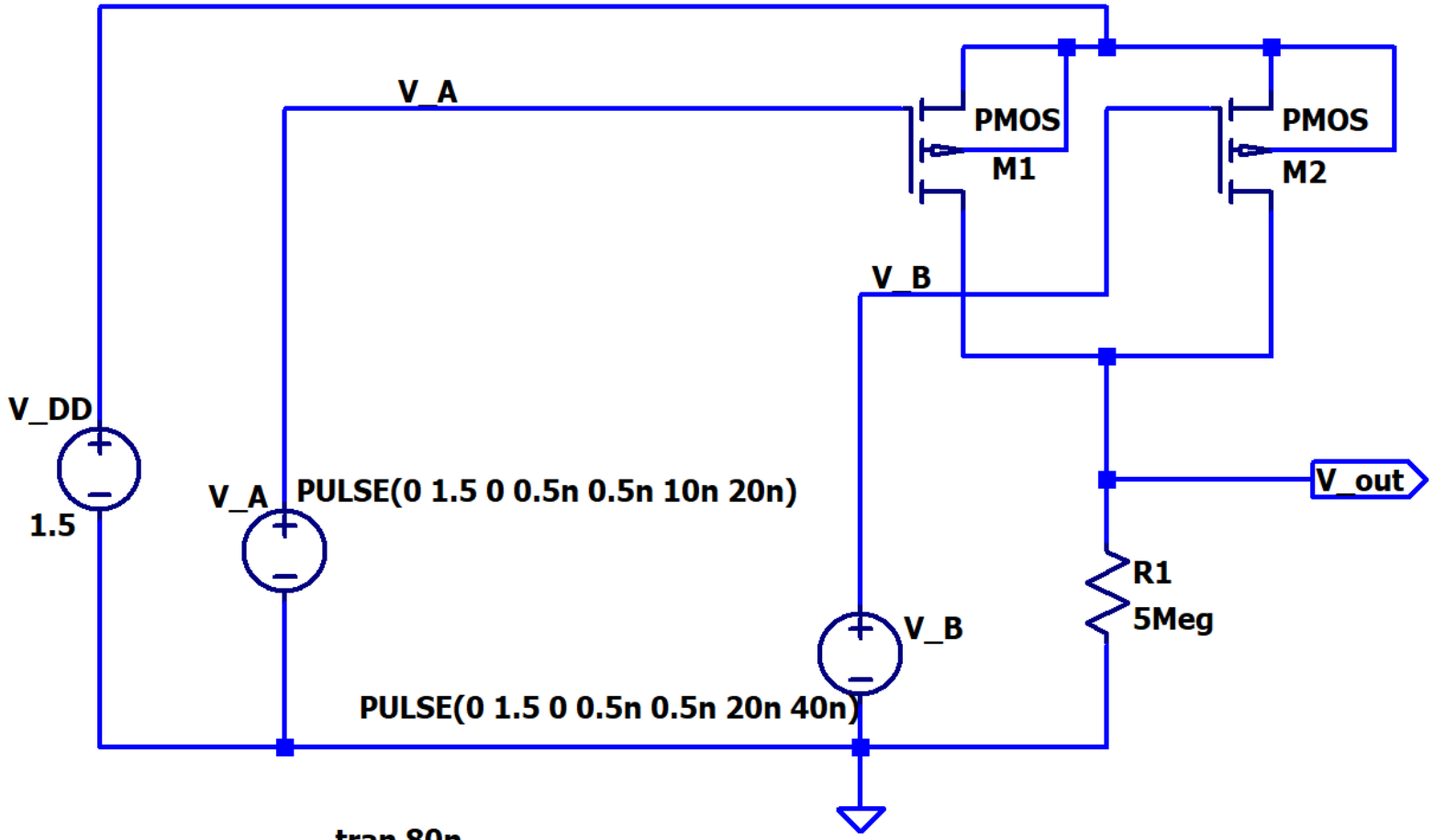
- Remember to rotate the PMOS such that Source (which is near gate) is towards V_{DD} (power supply) for PMOS.
- Also, remember to connect body and Supply
- Notice:
  In NAND using NMOS, we had two NMOS in series
- In NAND using PMOS, we have two PMOS in parallel



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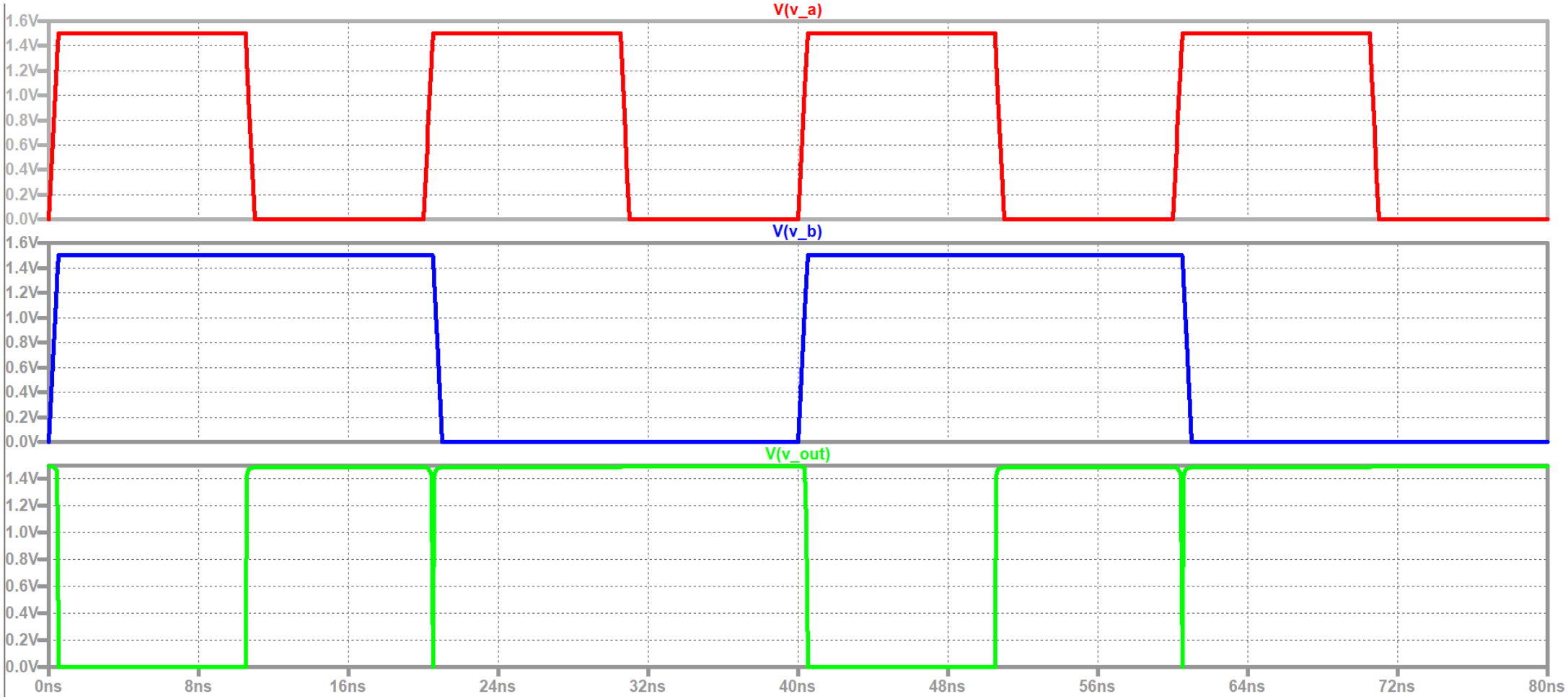

Task 3.1: NOR GATE Using NMOS(NMOS4 symbol)

- $V_{out} = \overline{V_A + V_B}$
- In NMOS configuration rephrase the output expression under bar, and the expression which is under bar, implement that expression using NMOS.
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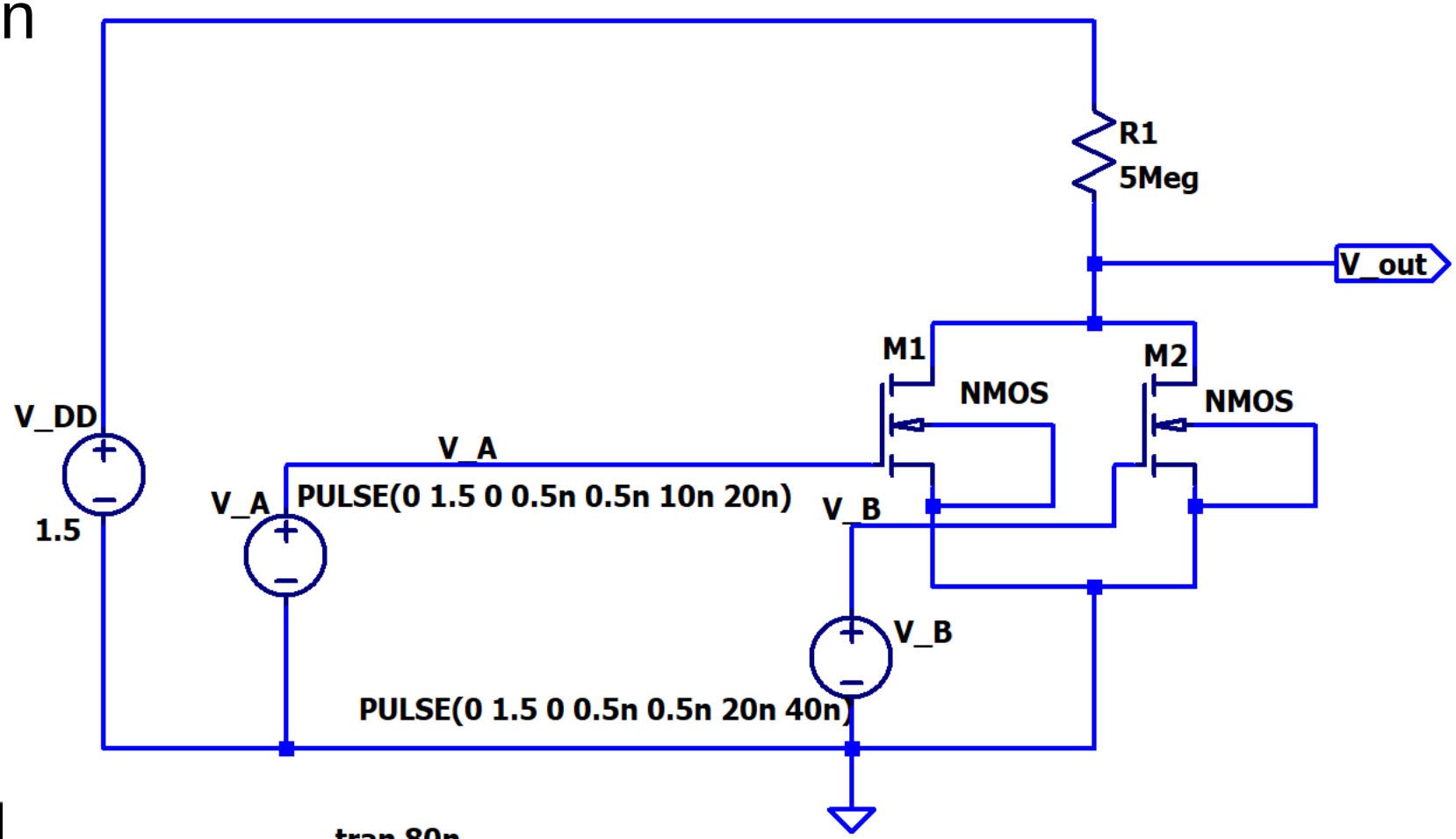

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- $V_{out} = \overline{V_A + V_B} = \overline{V_A} \cdot \overline{V_B}$

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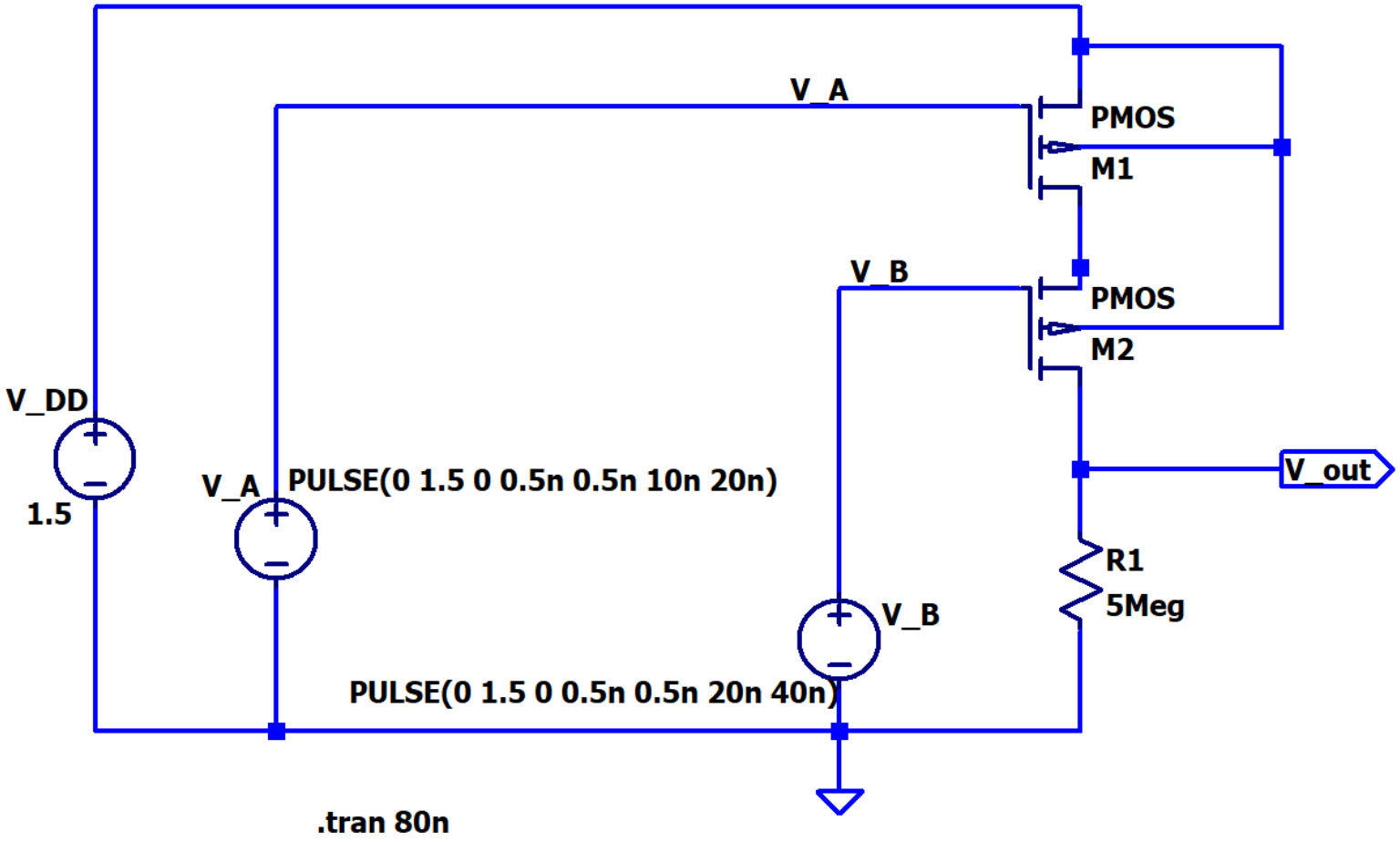
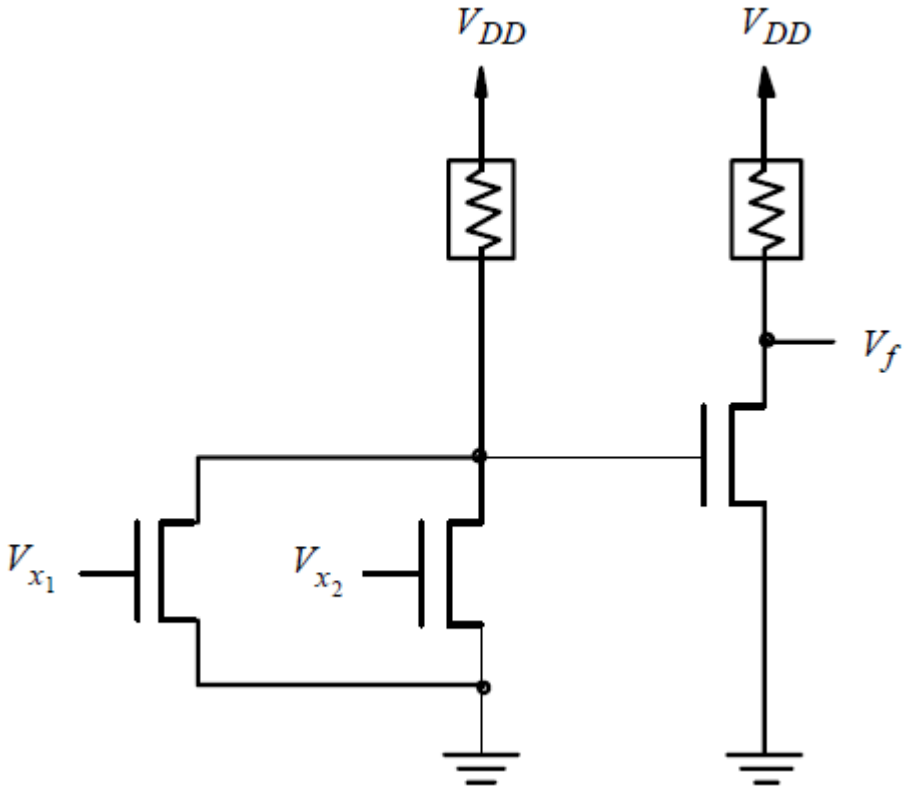


Task 4. OR GATE using NMOS(NMOS4 symbol)

- Perform OR Gate using NMOS



Task 4. OR GATE using NMOS(NMOS4 symbol)

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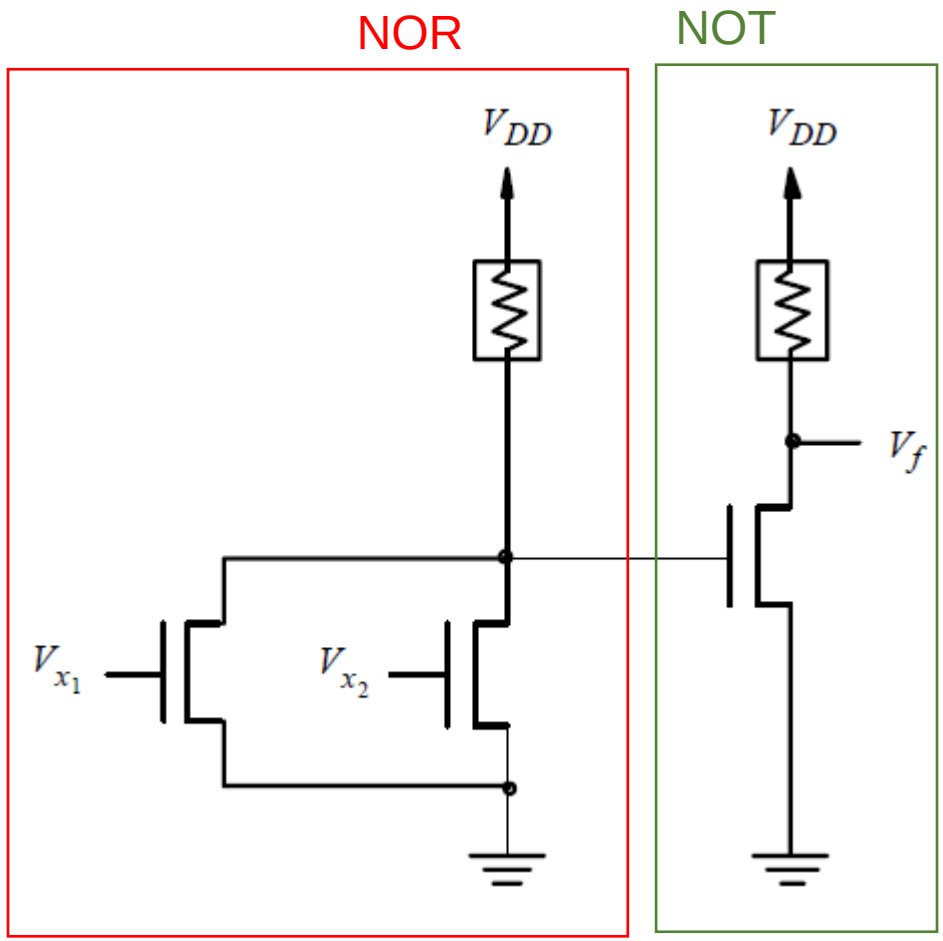

Task 5: AND GATE using PMOS(PMOS4 symbol)

- Perform AND gate using PMOS

Task 6: LOGIC using NMOS(NMOS4 symbol)

- Perform the logic $Y = \overline{(A + B)} \cdot \bar{C}$ in LT SPICE using NMOS and plot the truth table.
- Note: 3 Voltage sources: Use the following for obtaining all eight combinations

	V_A	V_B	V_C
ON TIME	10ns	20ns	40ns
PERIOD	20ns	40ns	80ns

Important NOTE

- Enter your **registration number** and **Full Name** next to

  all your circuits and
  the output plots.
- Keep the background of circuit and plot as white.

LAB record instructions:

For the lab experiment,

- Write the **Aim**.
- Complete the **Software/Hardware components used**.
- **Obtain the expression for the outputs.**
- Place the respective **circuits in LT Spice**.
- Connect the inputs and outputs. Name them and **write the same in the lab copy(inputs and outputs section)**.
- Use probe in LT spice to plot all possible combinations.
- Write a **concluding statement for each circuit**.
- **Submit** the document's soft copy **on time** in lms.vit.ac.in when available.