

Name: Aryaman Mishra  
Reg. no: 19BCE1027

### EXPERIMENT NO: 10

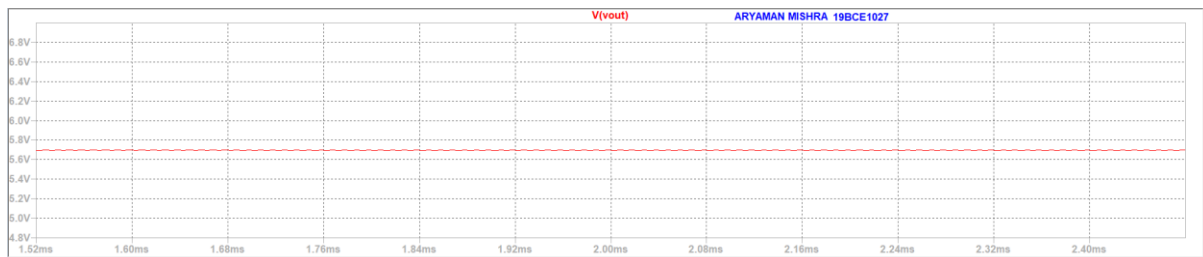
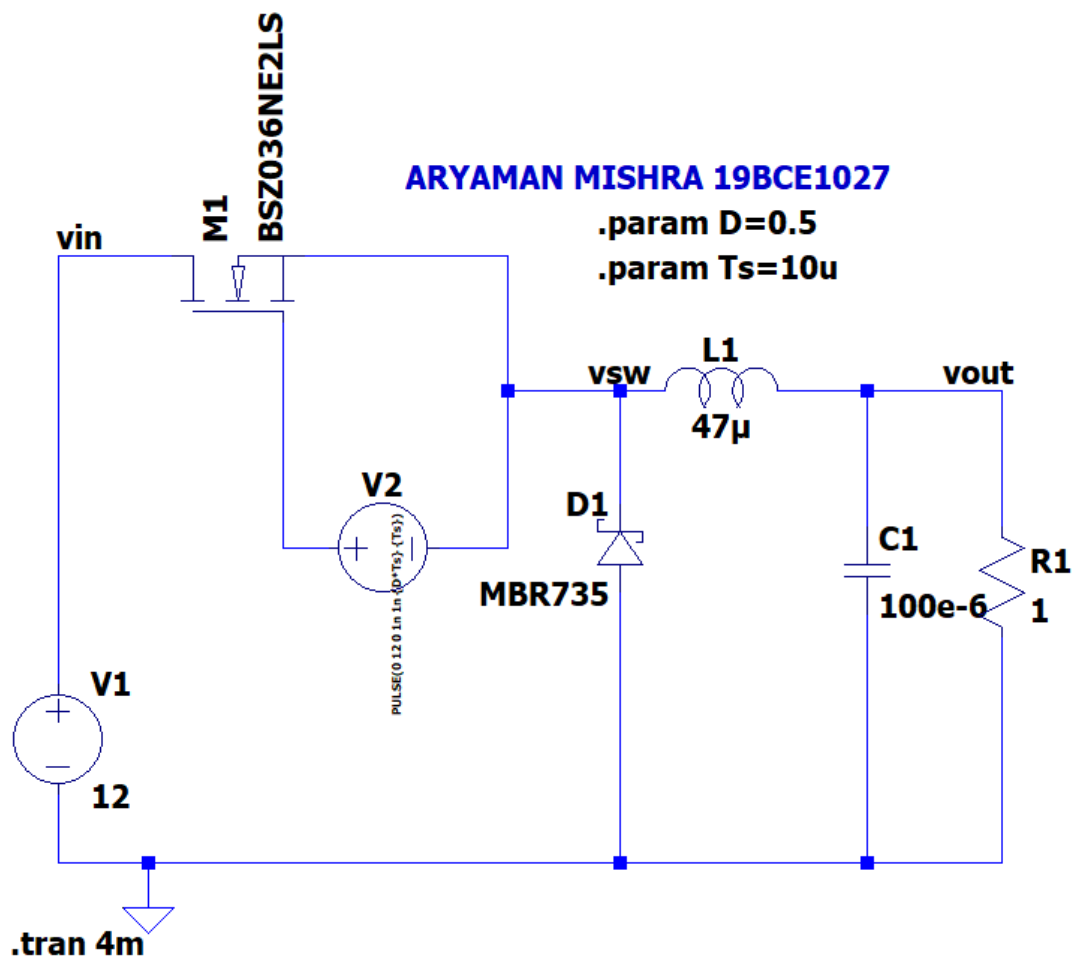
#### Design and analysis of Buck converter with realistic capacitance

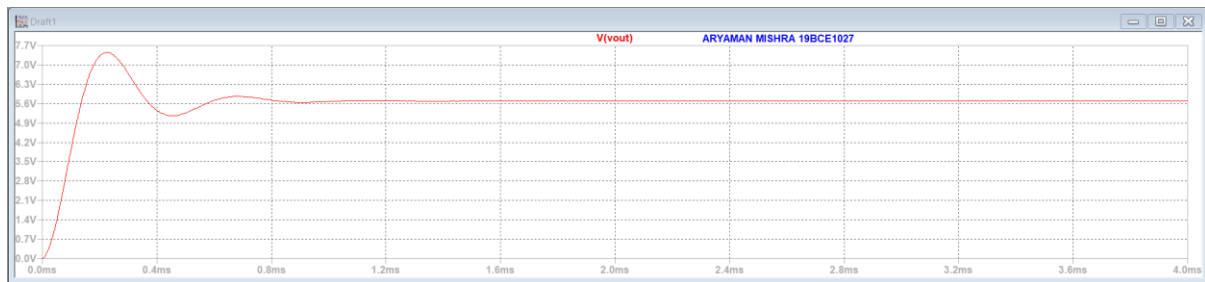
**Aim:** To design and analyze Buck converter with realistic capacitance

**Software used:** LTSpice

**Components required:** NMOS, Inductor, Voltage sources, ground, connecting wires, diode, capacitor, and resistor

**Task 1a:** Measure the output (vout) fluctuations in steady state

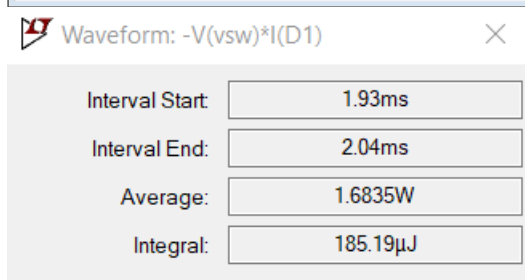
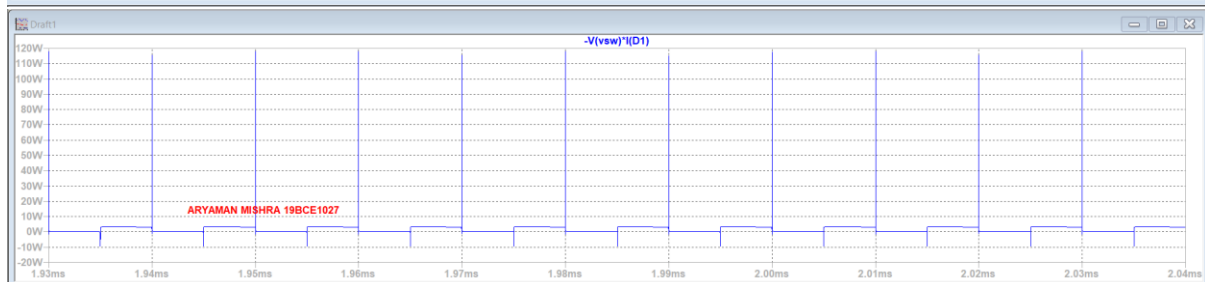
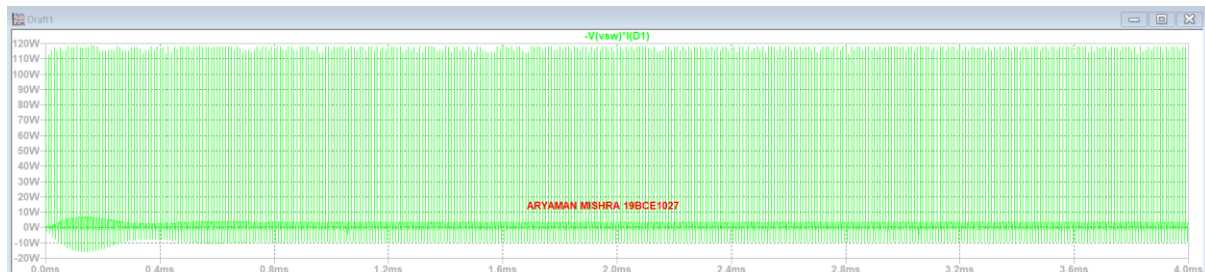


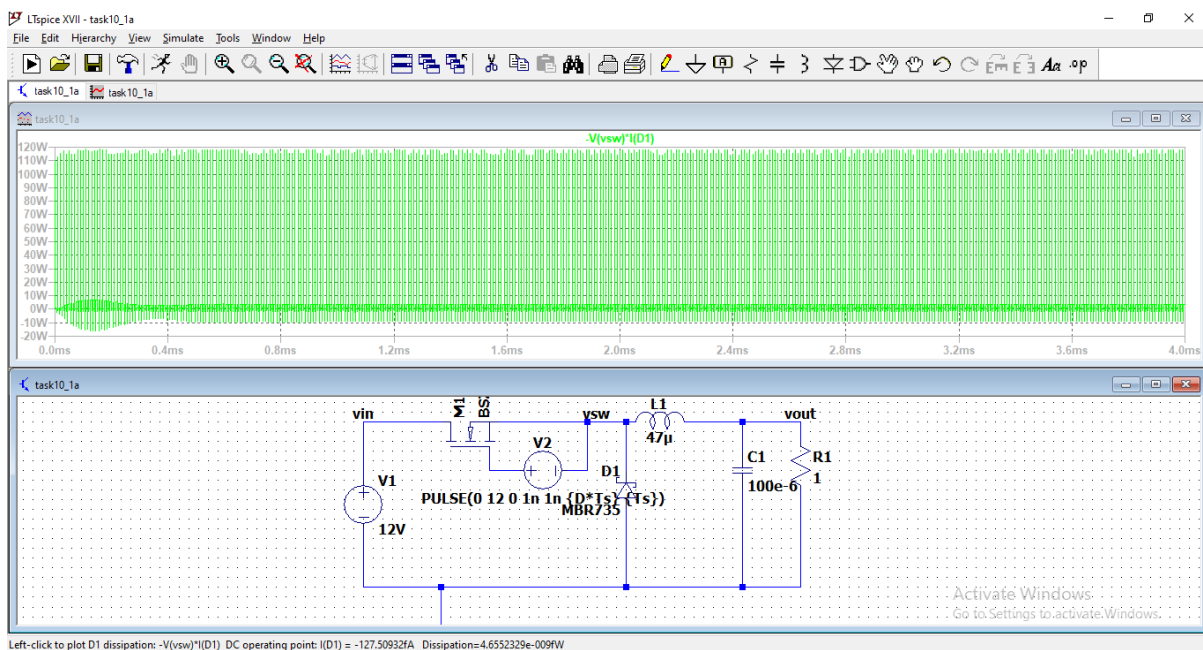
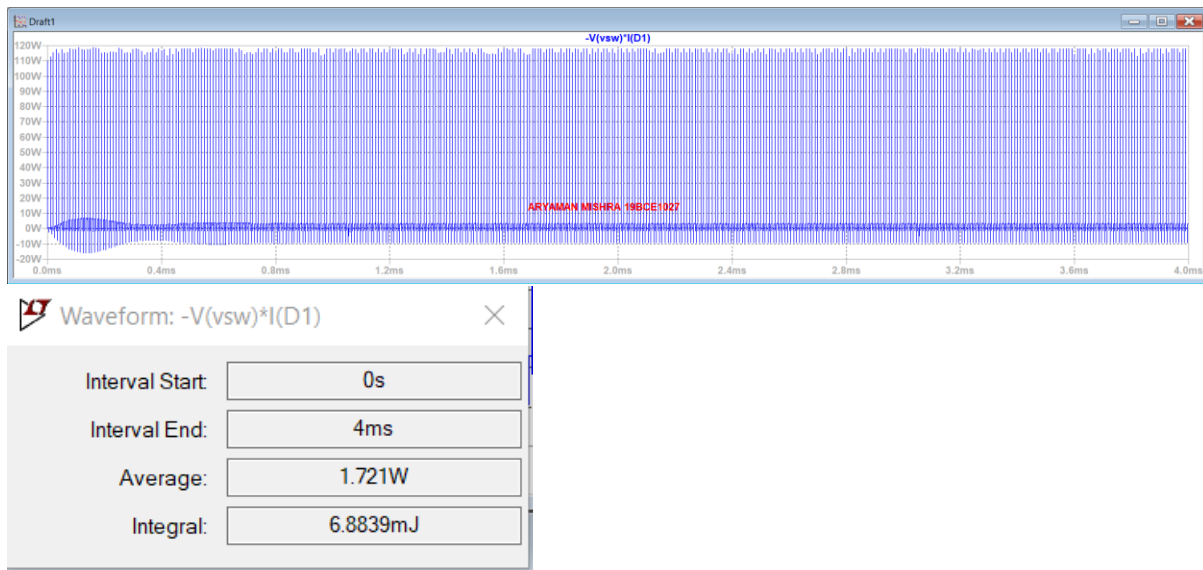


**Task 1b: Measure the voltage, current across inductor in steady state**



**Task 1c: Measure the instantaneous power and average power at components**



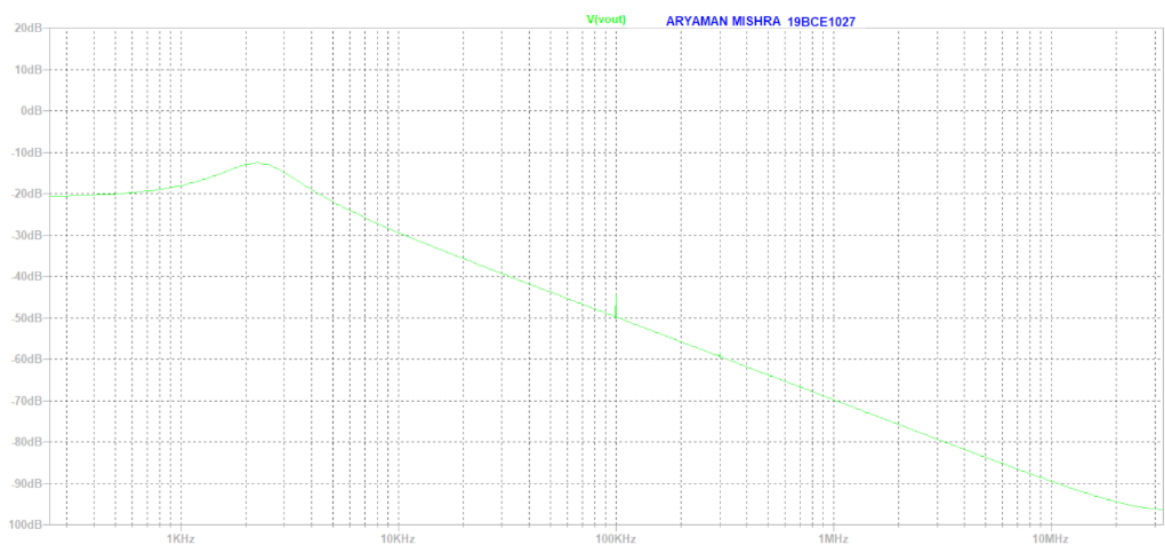
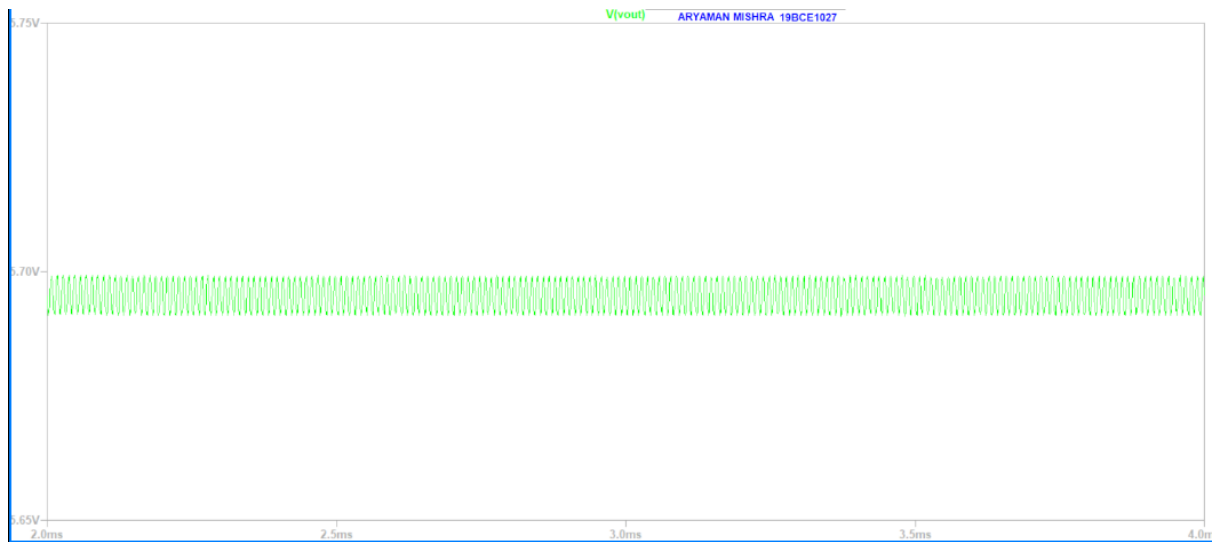


### Task 1d: Measure the instantaneous power and average power at output

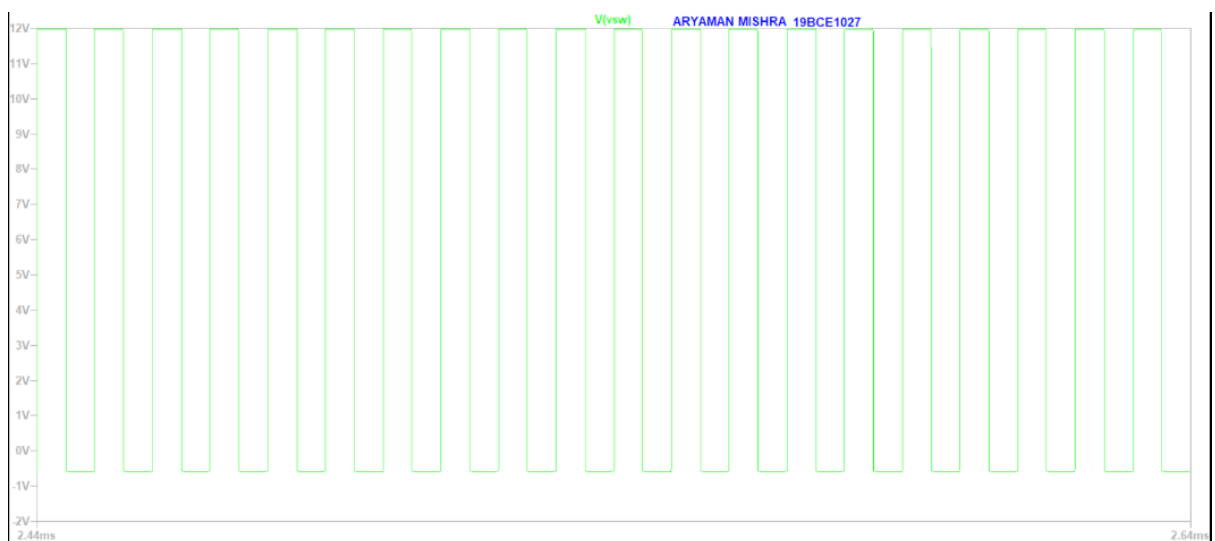


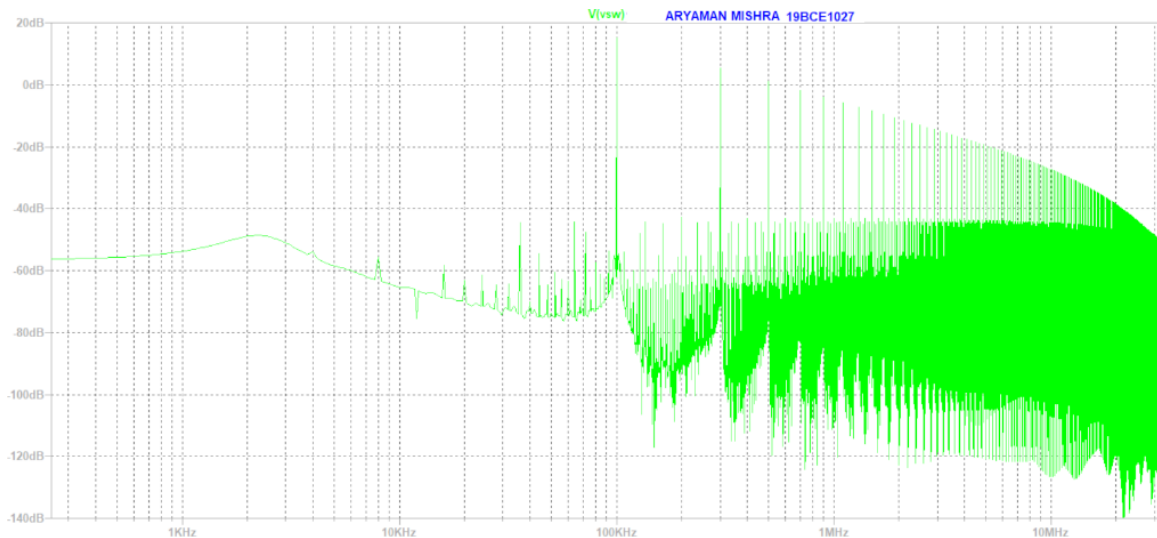
**Conclusion:** We measured the output ( $v_{out}$ ) fluctuations, voltage, current across inductor in steady state. We measured the average power at the components which is 1.6835W. The average power for the whole period was 1.721W. We measured the average power at the output.

### Task 2a: Select FFT of the signal (output voltage)



## Task 2b: Select FFT of the signal (Switch voltage)



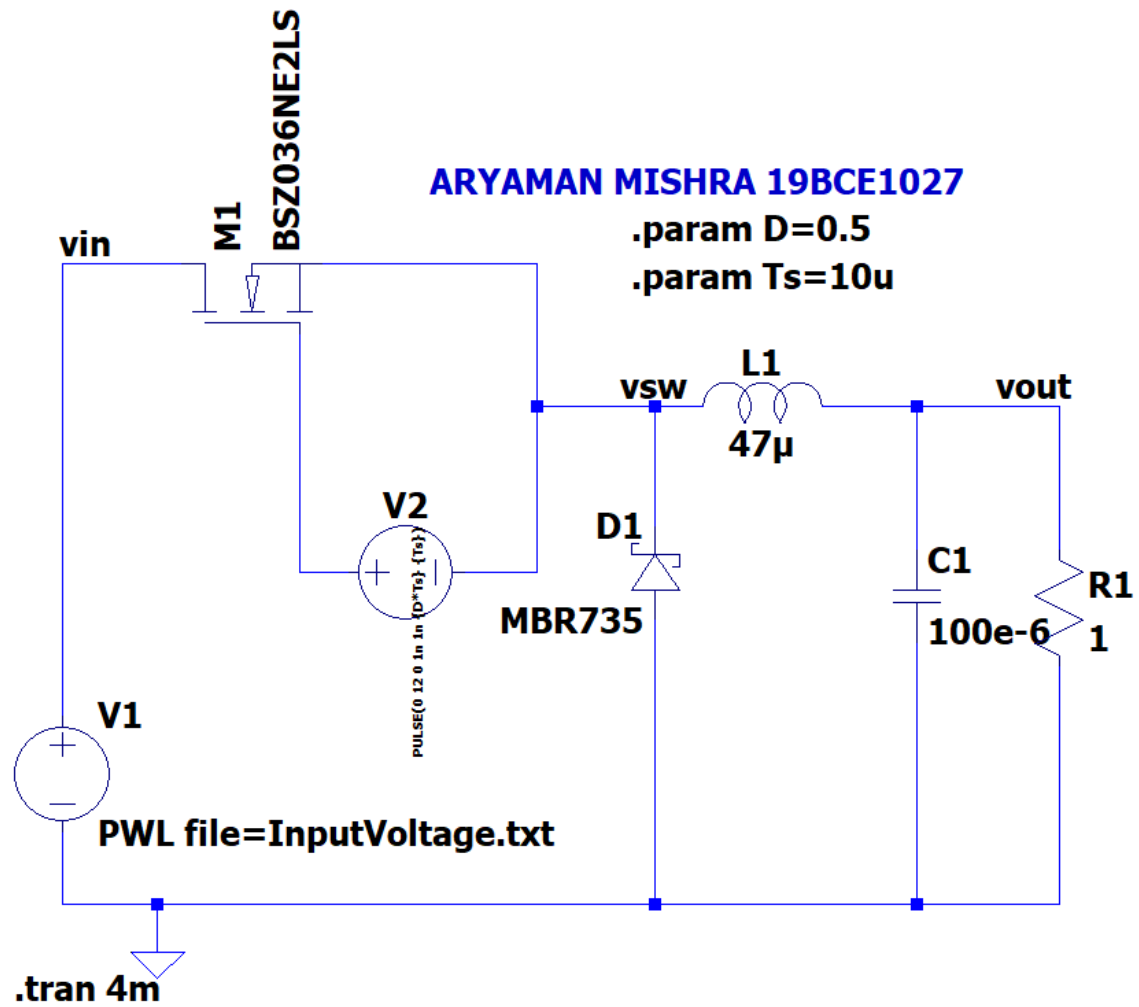


### Task 2c: Export switch voltage plot data

```
task10_1a - Notepad
File Edit Format View Help
time    V(vsw)
0.000000000000000e+000 3.650896e-011
1.658543547297397e-012 -1.179402e-005
3.317087094594793e-012 -2.378248e-005
4.975630641892190e-012 -3.596535e-005
6.634174189189587e-012 -4.834263e-005
8.292717736486983e-012 -6.091431e-005
9.951261283784381e-012 -7.368040e-005
1.160980483108177e-011 -8.664090e-005
1.332693002685756e-011 -1.014324e-004
1.676118041840914e-011 -1.351774e-004
2.362968120151229e-011 -2.179401e-004
3.461492456010995e-011 -3.896714e-004
4.717967069812458e-011 -6.430985e-004
6.000927741017301e-011 -9.634547e-004
7.77743673786539e-011 -1.508455e-003
9.878057516710655e-011 -2.302182e-003
1.267776326362887e-010 -3.607016e-003
1.605900103342909e-010 -5.550129e-003
2.046198424144894e-010 -8.664718e-003
2.588535042275850e-010 -1.337818e-002
3.288446774519605e-010 -2.082111e-002
Ln 1, Col 1 100% Windows (CRLF) UTF-8
```

**Conclusion:** We did an FFT (Fast Fourier Transform) on output and switch voltage. The switching frequency is 100kHz. We successfully exported switch voltage plot data.

### Task 3: Import txt file as source

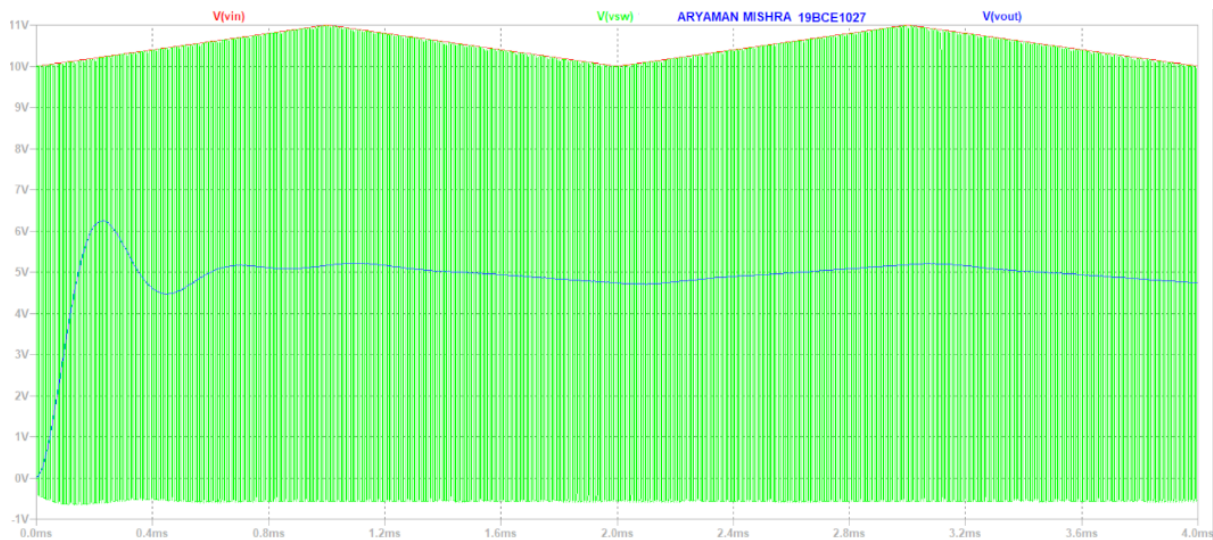


```

InputVoltage - Notepad
File Edit Format View Help
0 10
1m 11
2m 10
3m 11
4m 10

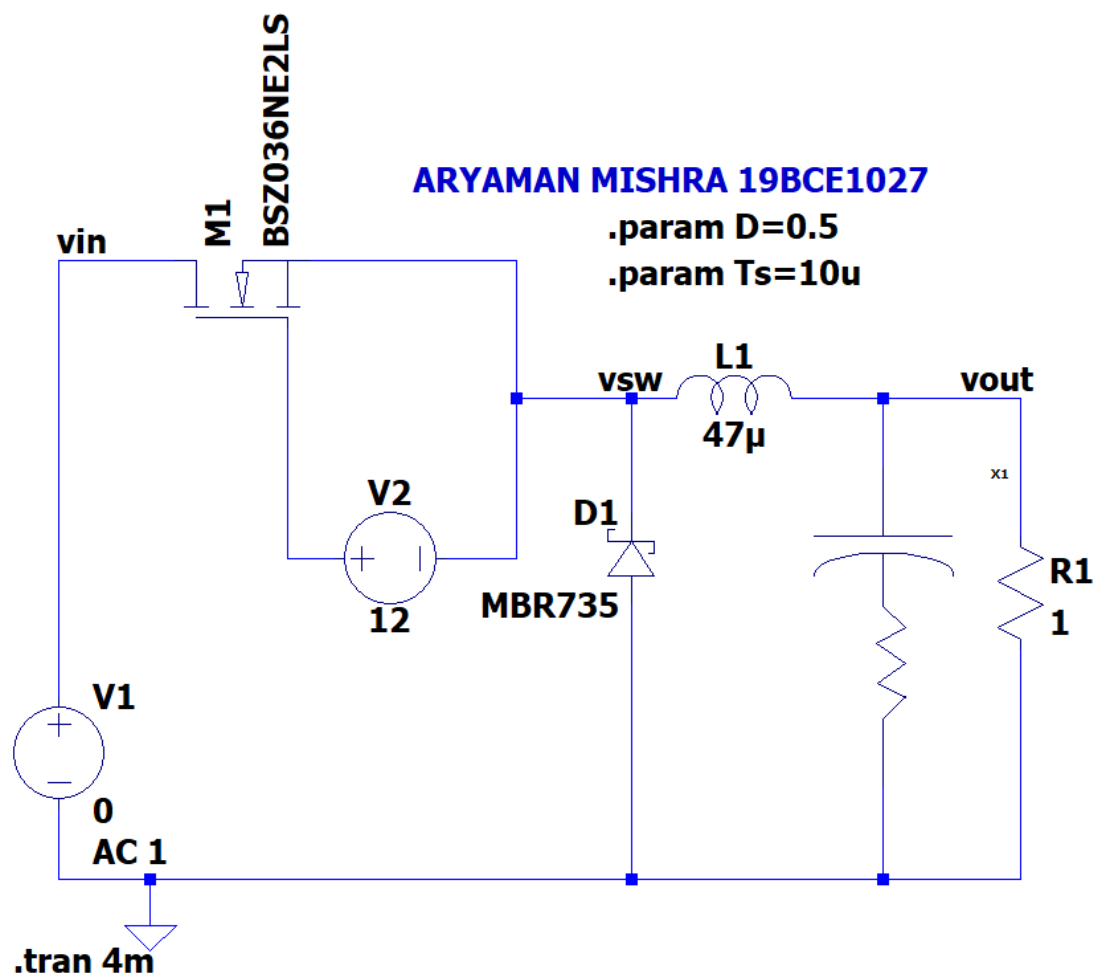
```

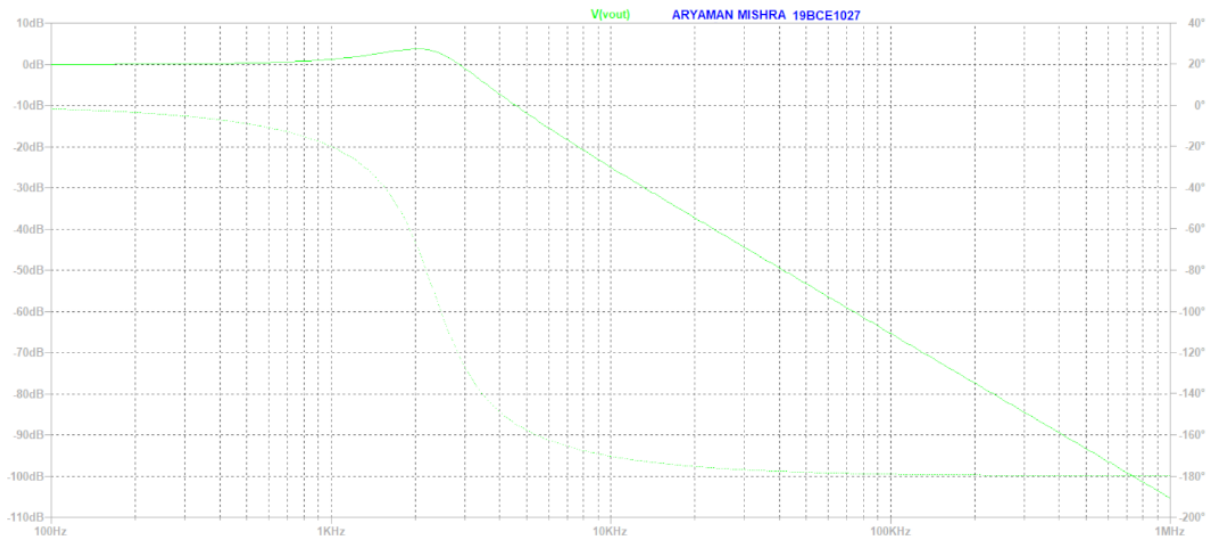
Ln 1, Col 1    100%    Windows (CRLF)    UTF-8



**Conclusion:** We successfully imported input text file as a voltage source and measured the voltage.

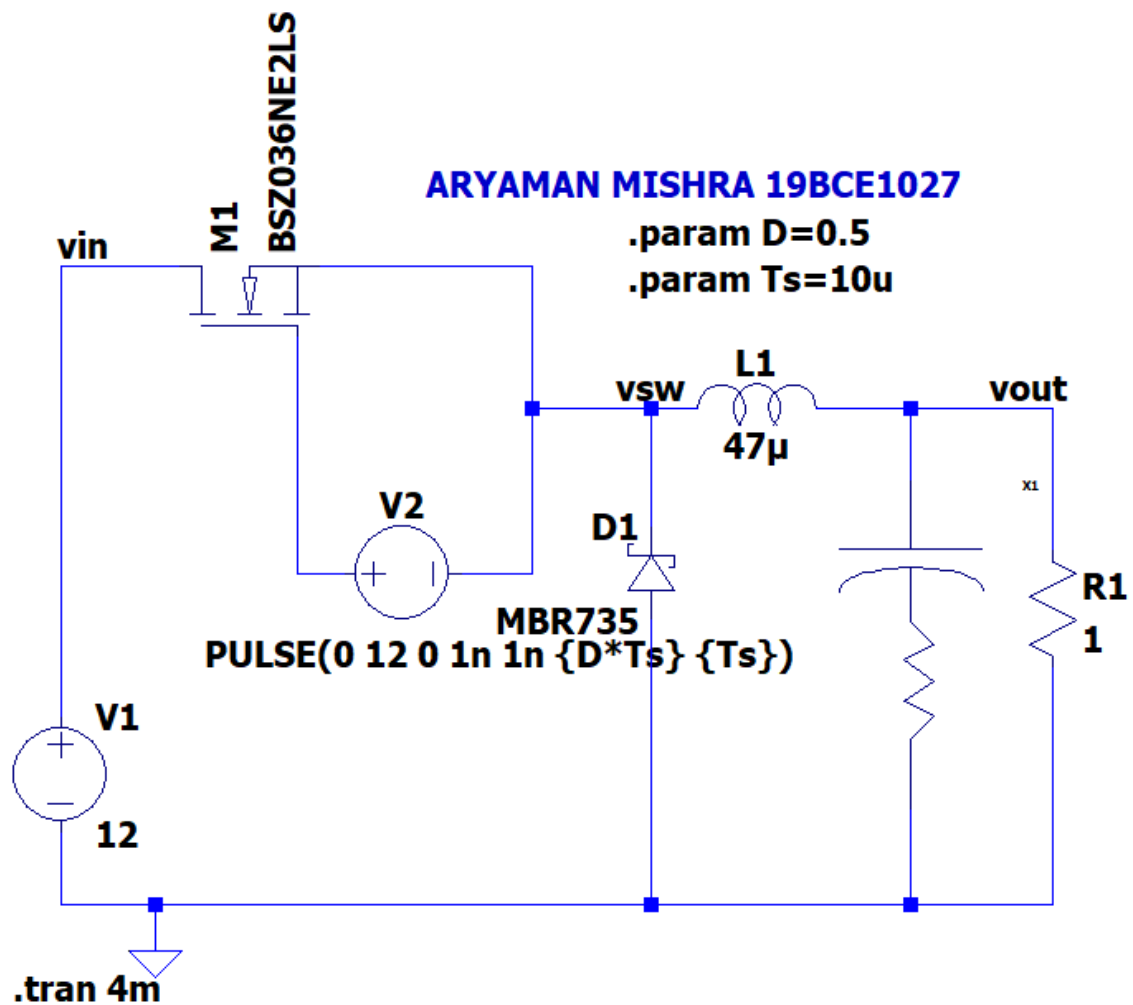
#### Task 4: AC analysis



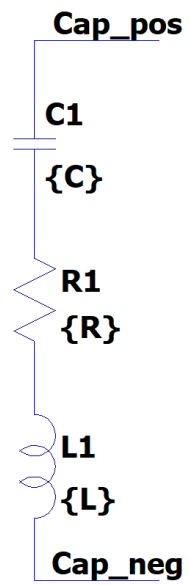


**Conclusion:** We observe that close to DC voltage, there is unity gain, after resonance, there is drop in gain, after DC, we notice the Phase shift.

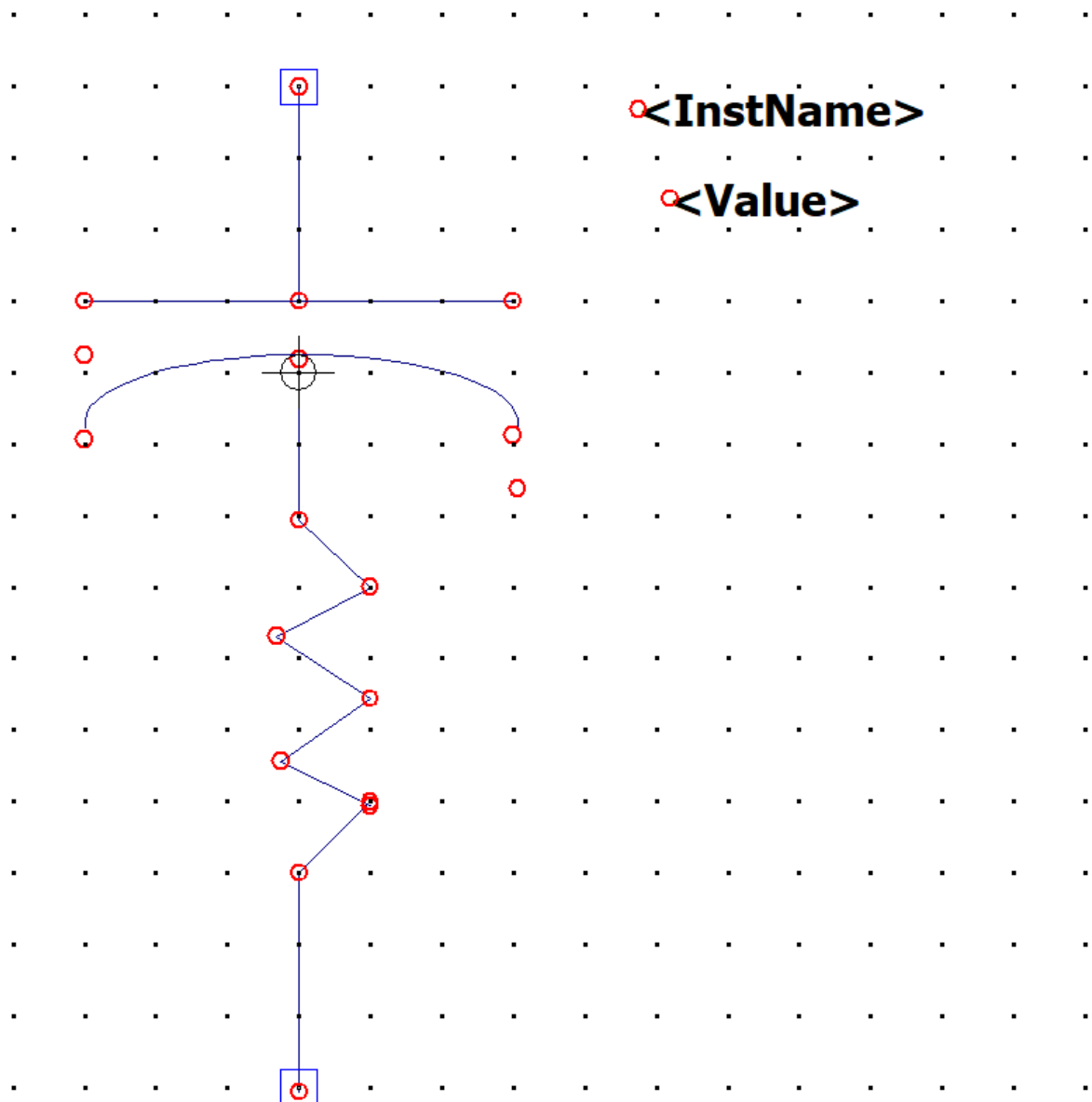
**Task 5:** To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance



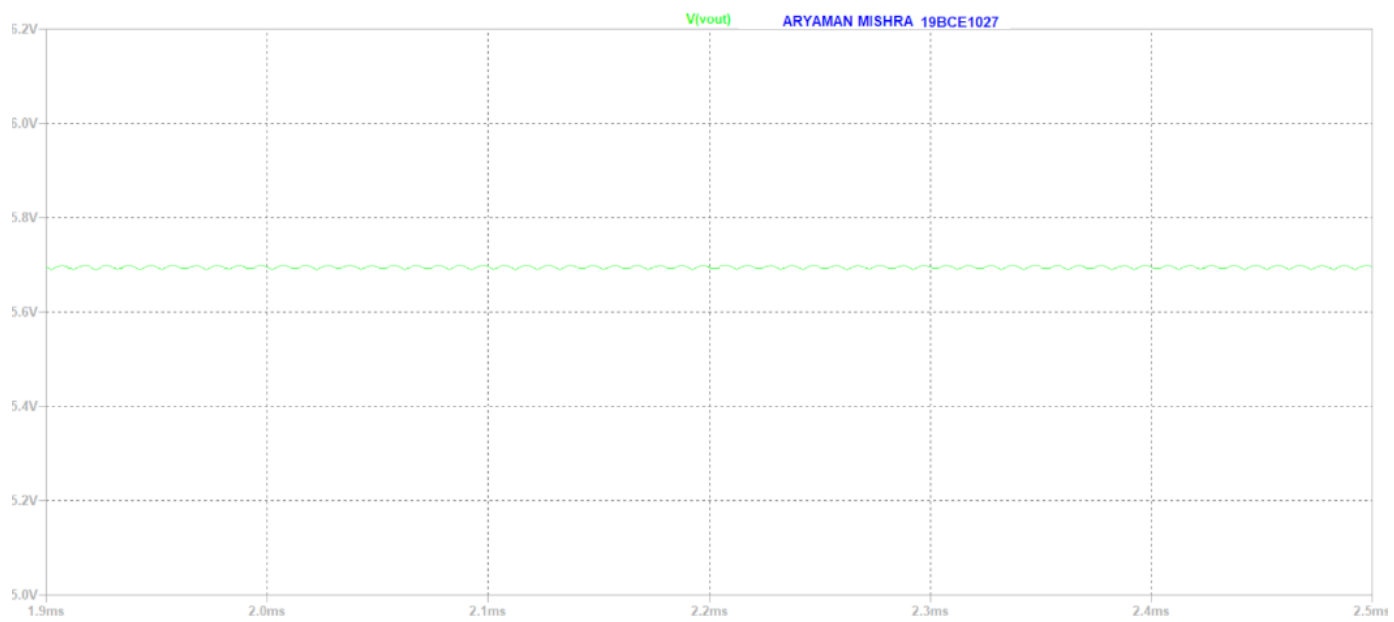
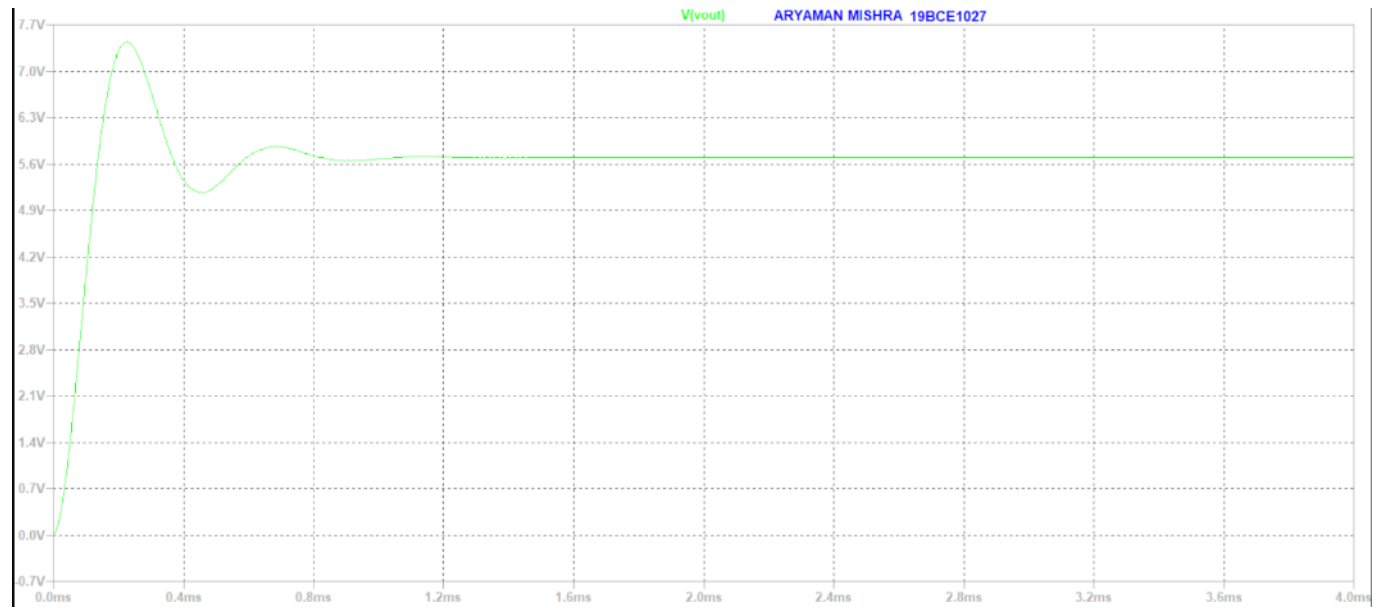




ARYAMAN MISHRA 19BCE1027

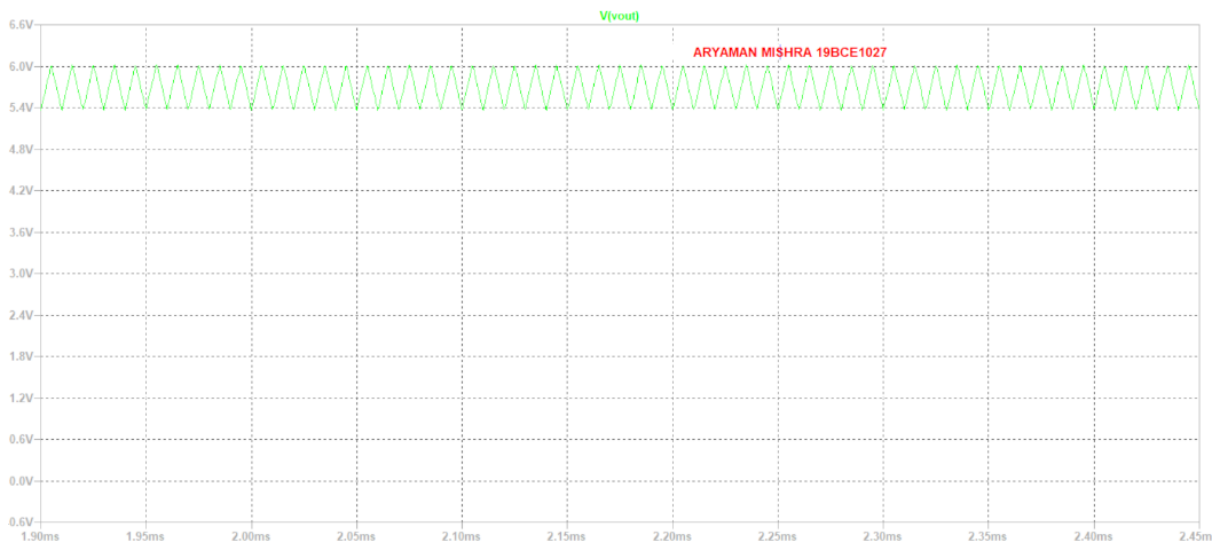
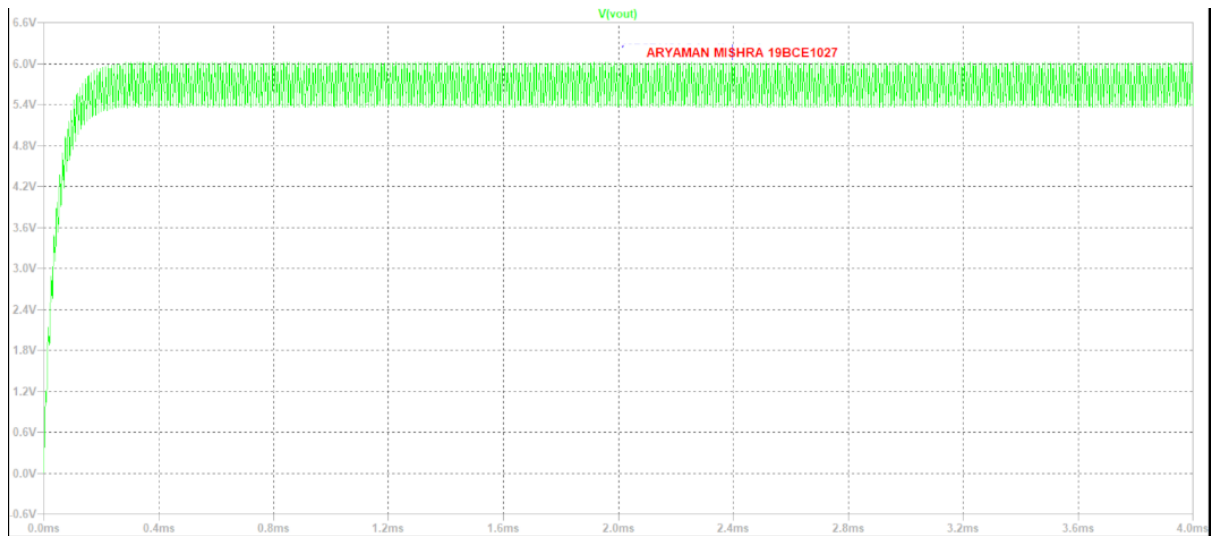


5a)  $C=100\mu$   $R=1m$   $L=1p$



**Conclusion:** We find less ripples as compared to the previous circuit.

**5b)  $C=100\mu$   $R=100$   $L=1\mu$**



**Conclusion:** If we increase the resistance to unrealistic values, the ripples will be more than the ideal condition.