

# 10. Design and analysis of Buck converter with realistic capacitance

**Course: ECE1008 – Electronic Hardware Troubleshooting LAB**

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**Vellore Institute of Technology**  
(Deemed to be University under section 3 of UGC Act, 1956)  
CHENNAI



# Introduction

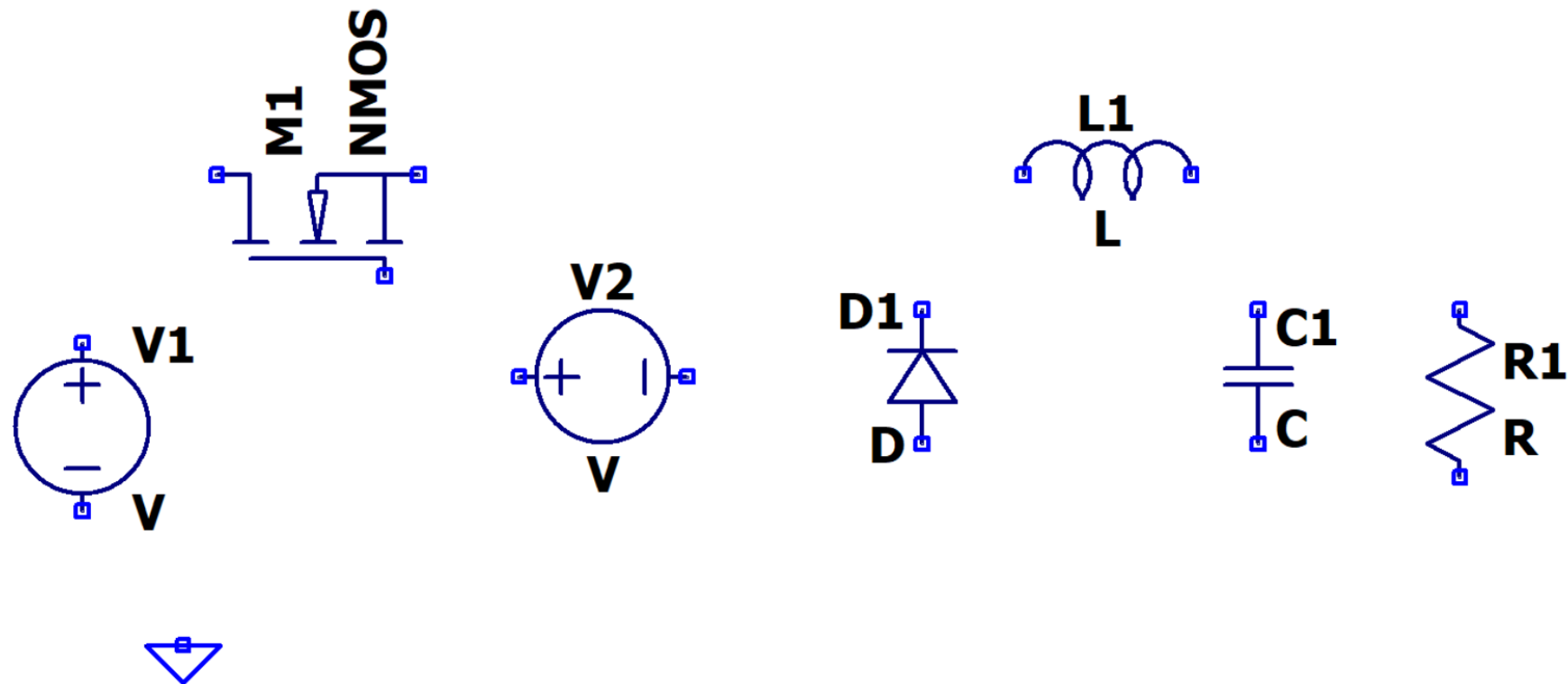
- Buck converter is used to provide Stable Stepped down dc voltage from a source of higher DC voltage.
- In this experiment, we will design a 12V DC to 5.7V DC signal using NMOS, Schottky diode (reverse biased) LC filter and a resistor.



# 1. Steps to design:

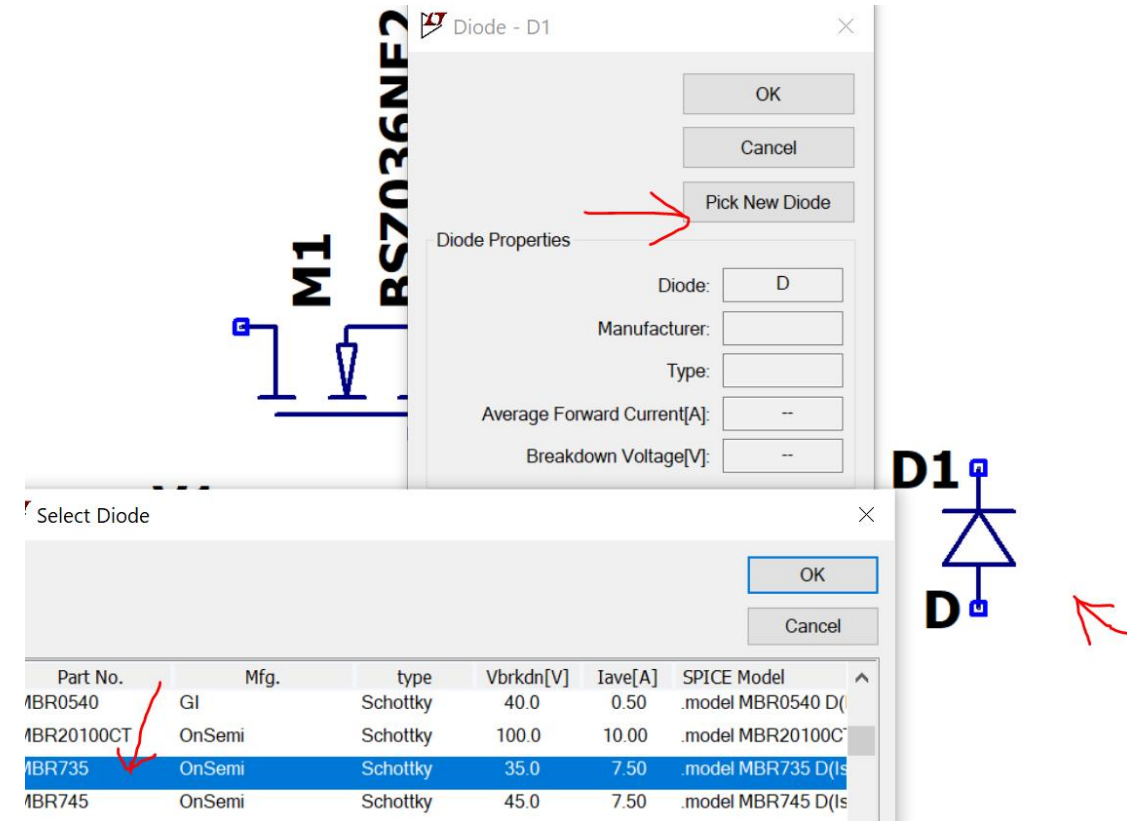
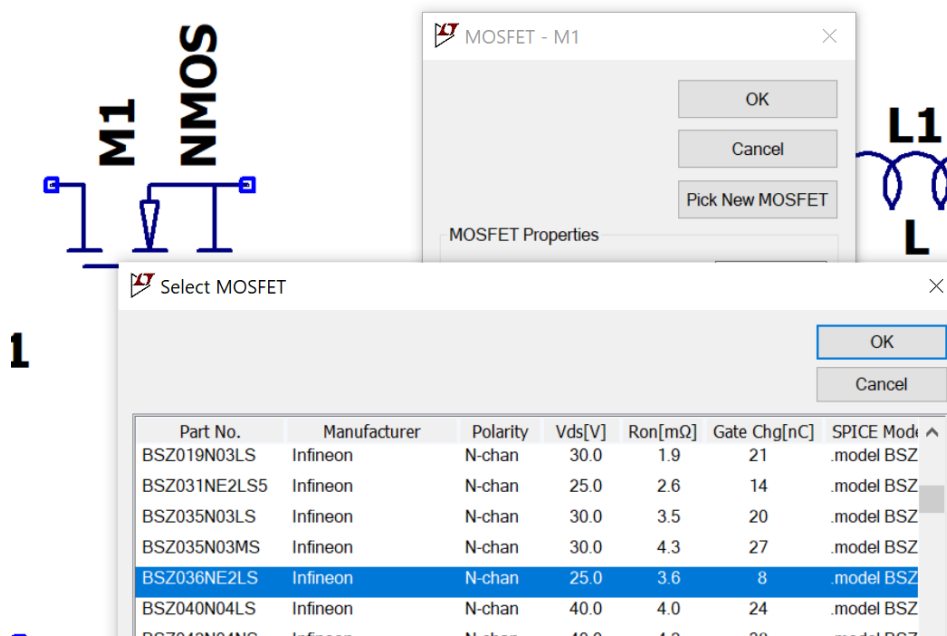
1a) Place all the components as shown below:

Note: Use CTRL+R for rotating a component.



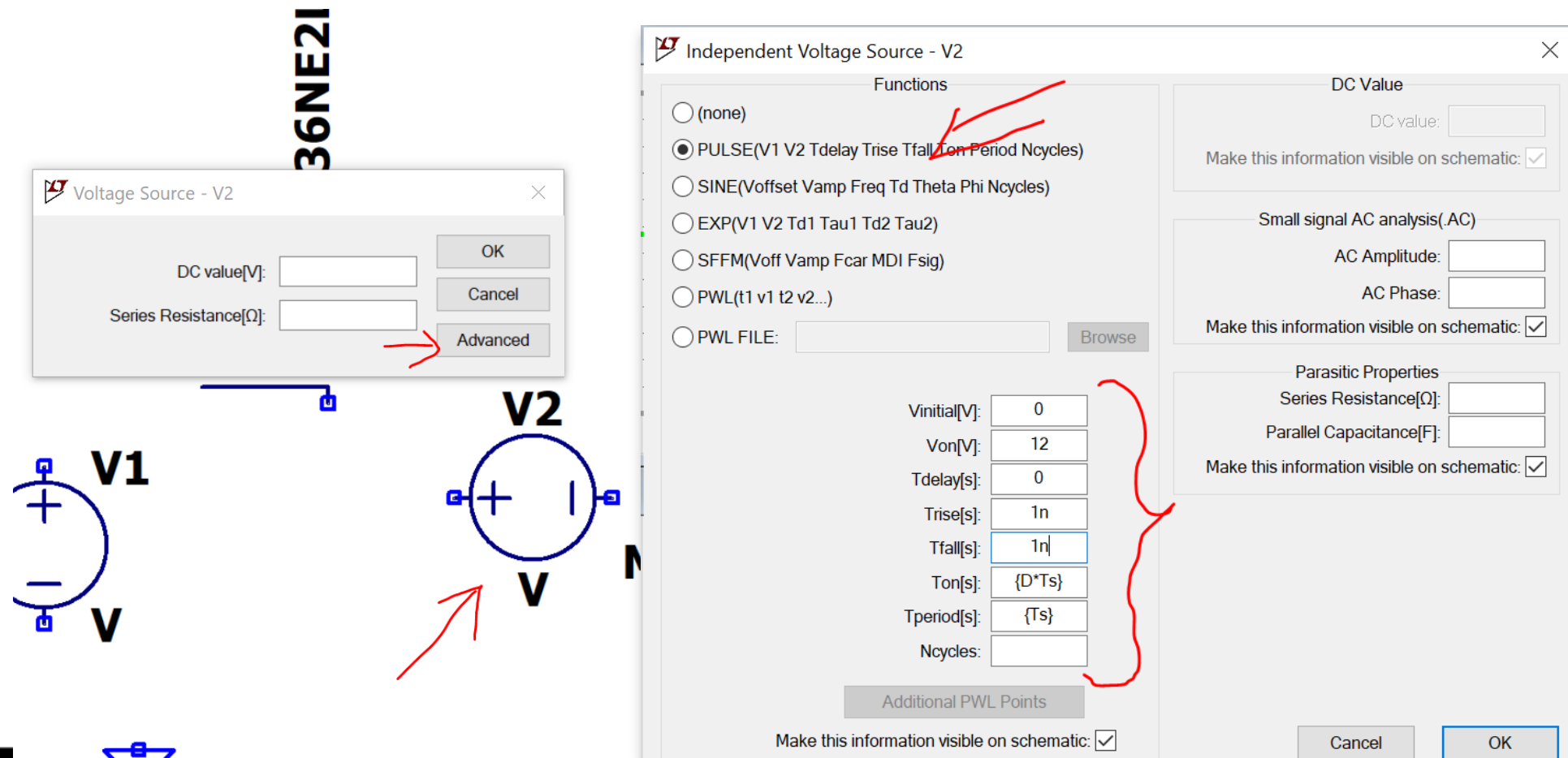
# 1. Steps to design:

- 1b) Right click at NMOS and select BSZ036NE2LS  
 Right click at diode, and pick new diode: MBR735



# 1. Steps to design:

2. Set input DC voltage V1 as 12V and second Voltage source V2 as Pulse source.



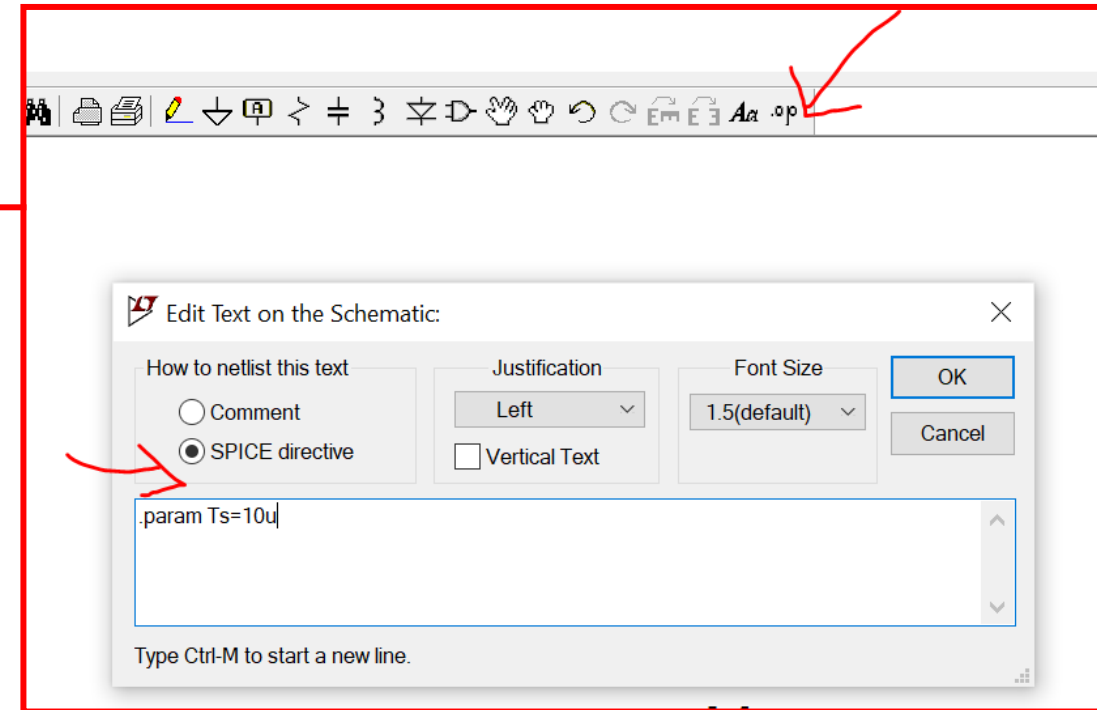
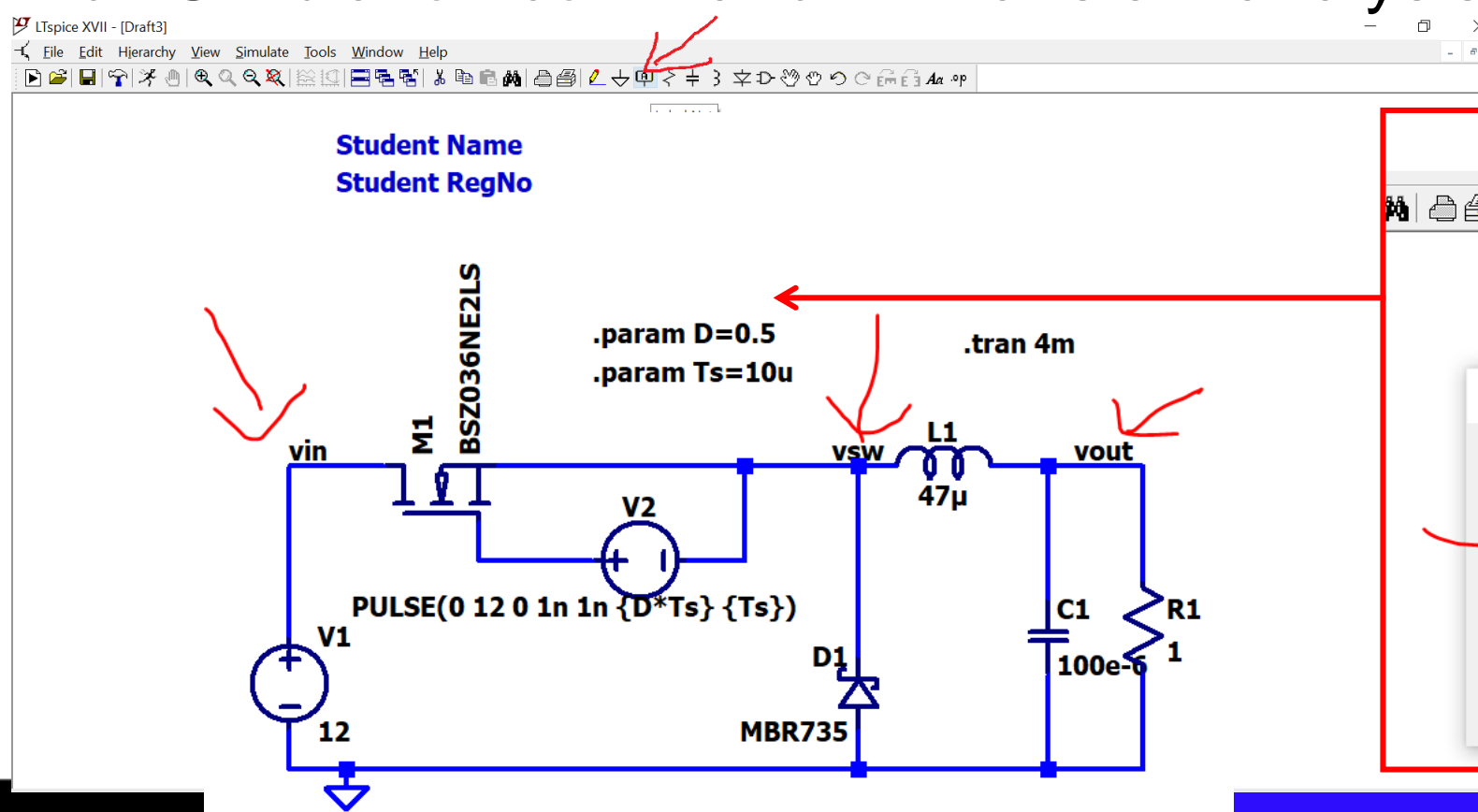
# 1. Steps to design:

Add labelnets Vin, VSW, Vout.

EditText on schematic -> Spice directive

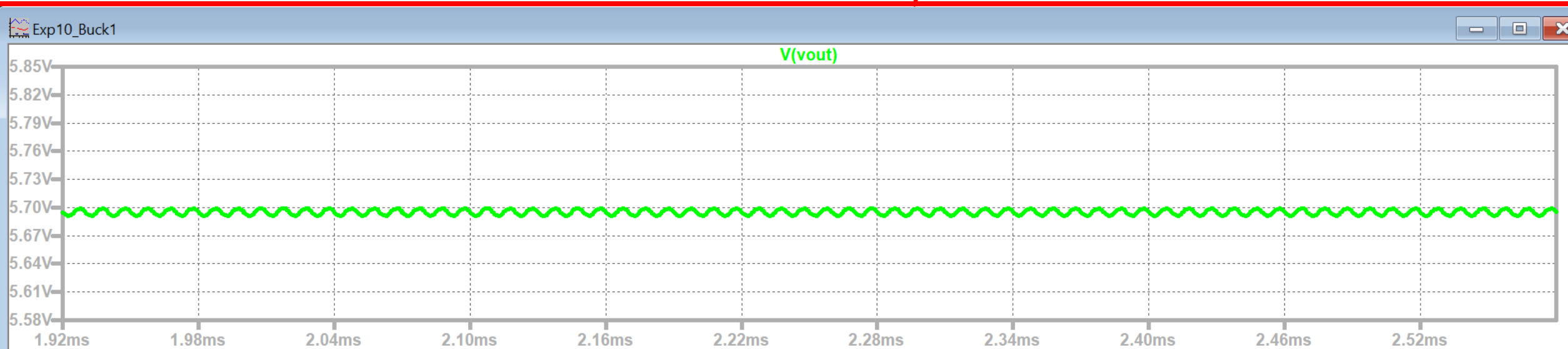
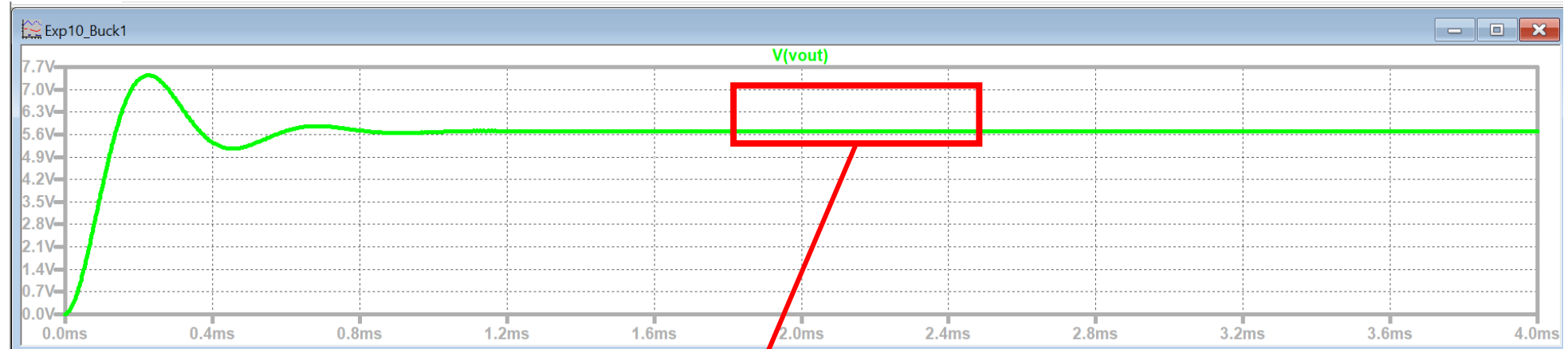
Include parameters D and Ts (pulse source's duty cycle time duration.)

Edit Simulation command -> Transient analysis -> 4m



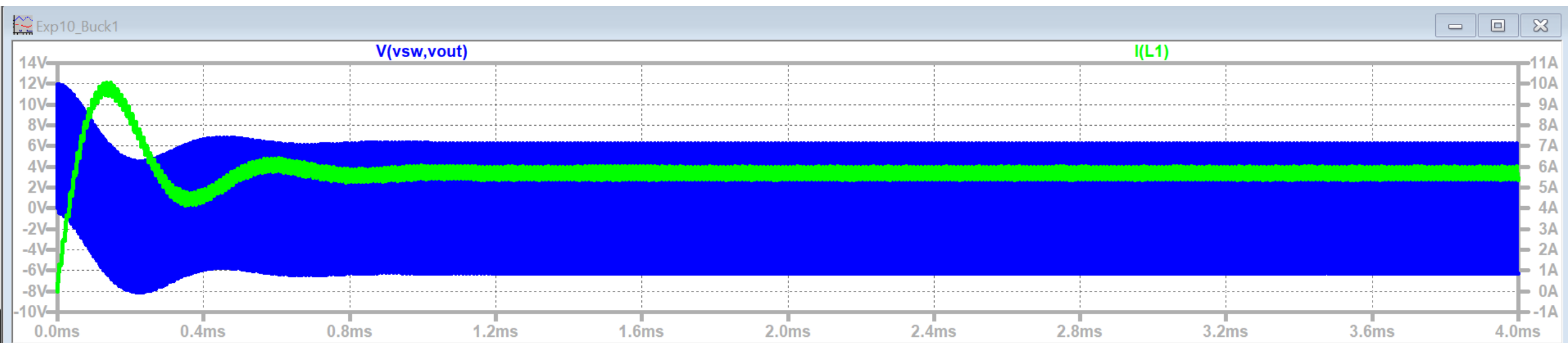
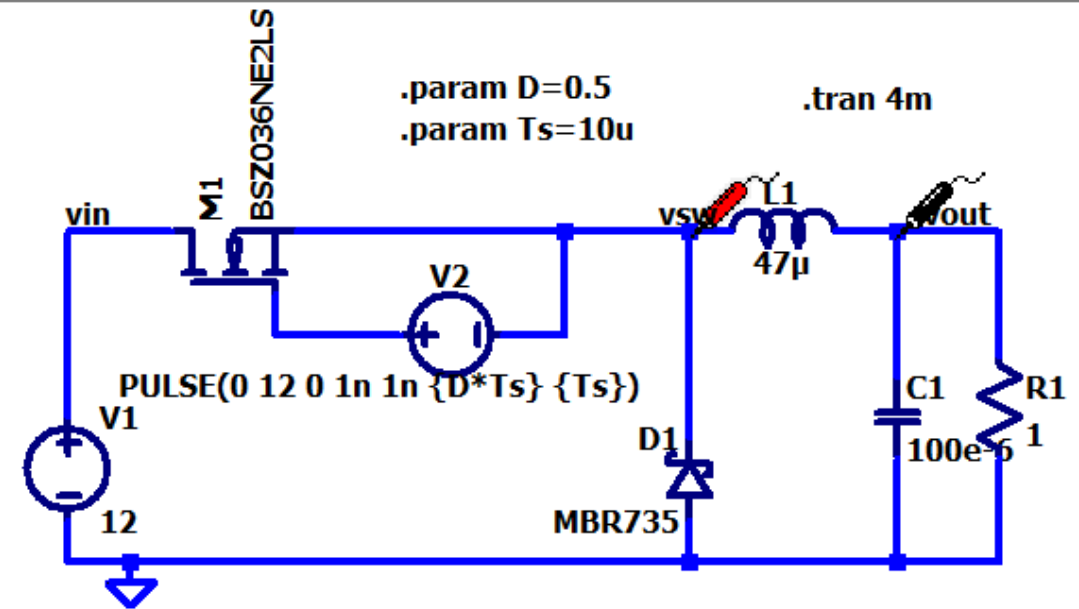
# Task 1a: Measure the output ( $v_{out}$ ) fluctuations in steady state

- Simulation > Edit simulation command  
.tran 4m
- Run



# Task 1b: Measure the voltage, current across inductor in steady state

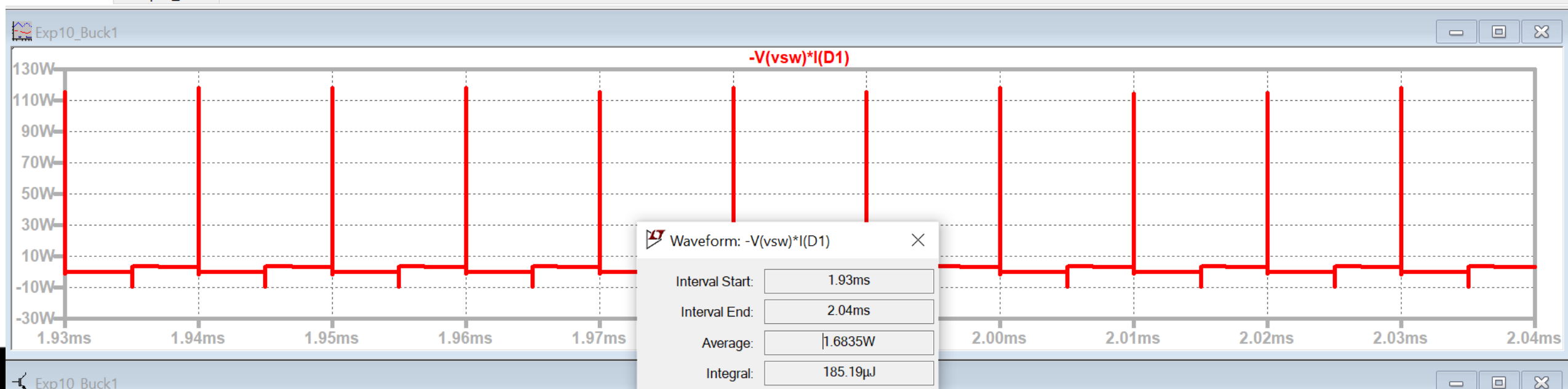
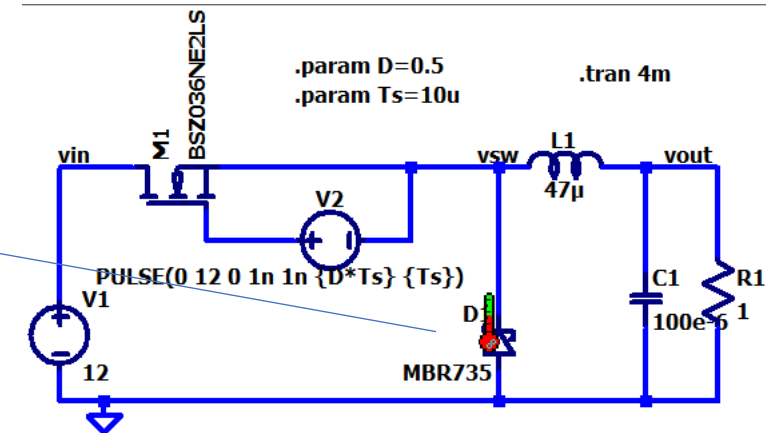
- Click at Inductor's vsw end, hold the mouse and move to vout and release the mouse click. This will measure voltage across the inductor.
- Measure the inductor current too.





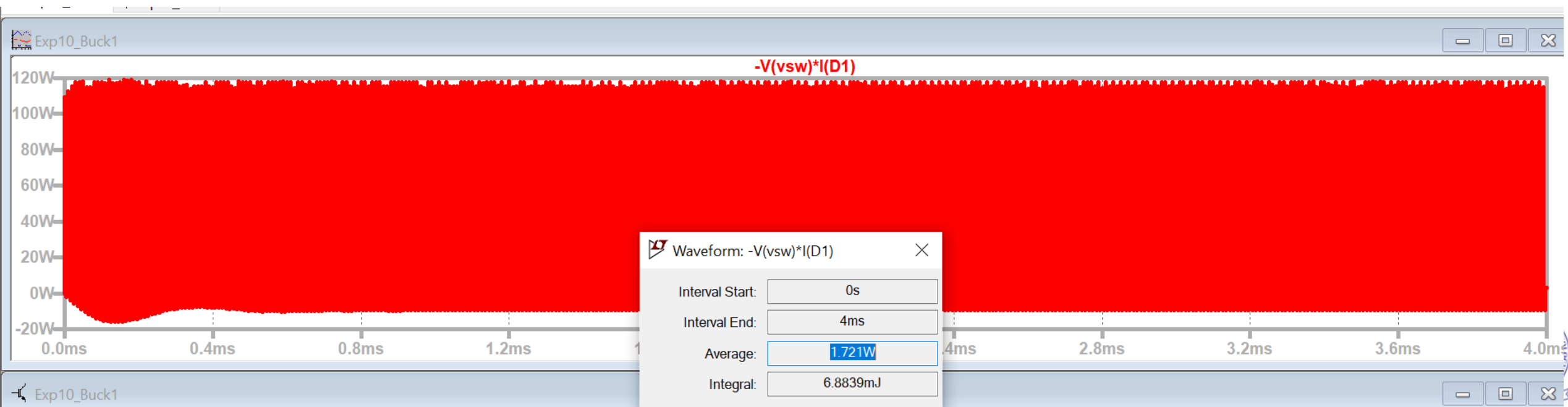
# Task 1c: Measure the instantaneous power and average power at components

- Press alt key and click on Diode
- Zoom in the plot and Hold CTRL key and click on the variable in plot (power)  
The pop-up window will display average power.



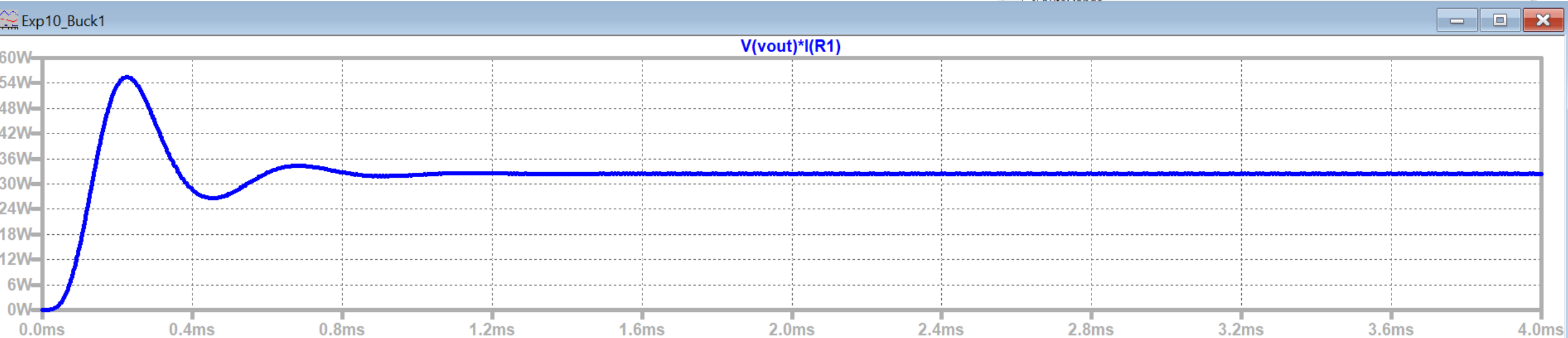
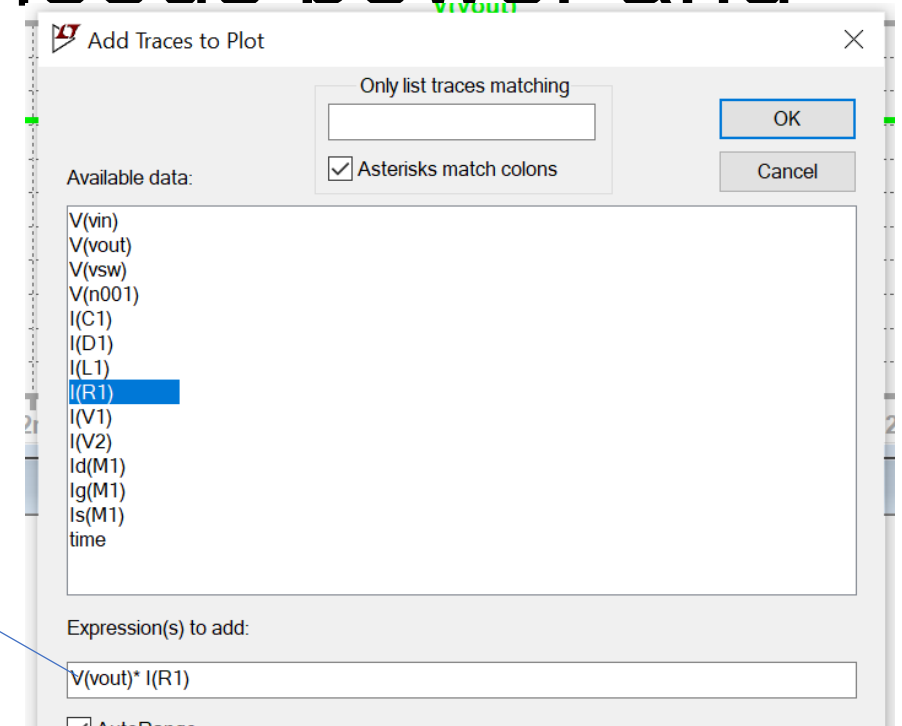
# Task 1c: Measure the instantaneous power and average power at components

- To calculate average for whole period:  
Zoom to fit the plot and find average:



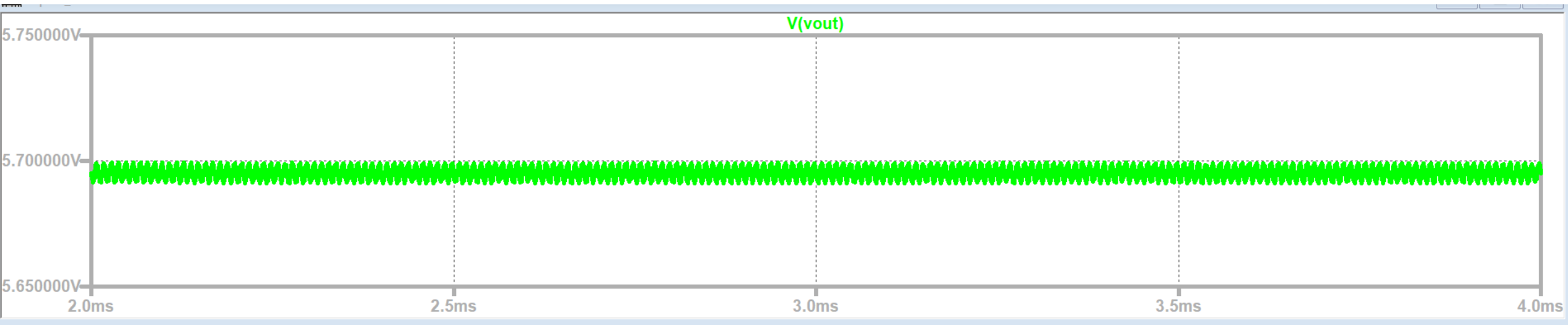
# Task 1d: Measure the instantaneous power and average power at output

- Alternatively, for instantaneous power at load resistor,  
Right click at plot -> Add trace->  
In expression: Type  $V(vout)*I(R1)$



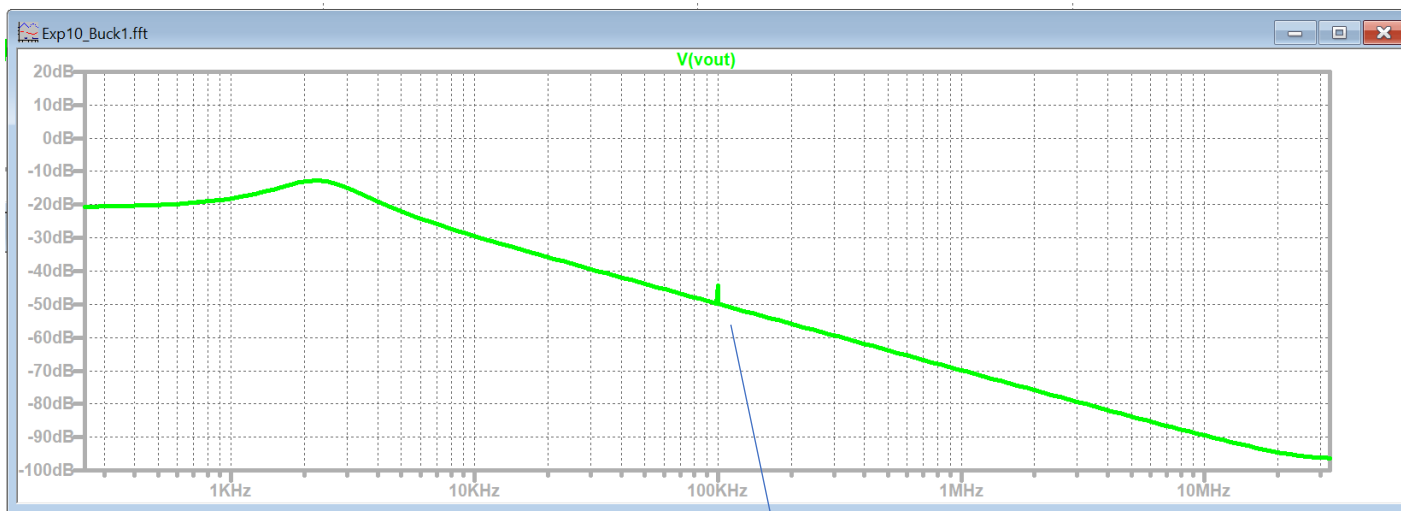
# Task 2a: Select FFT of the signal (output voltage)

- Select the region on the plot by clicking on y-tick marks and x tick marks  
x: 2ms to 3ms and y: 5.6V to 5.7V

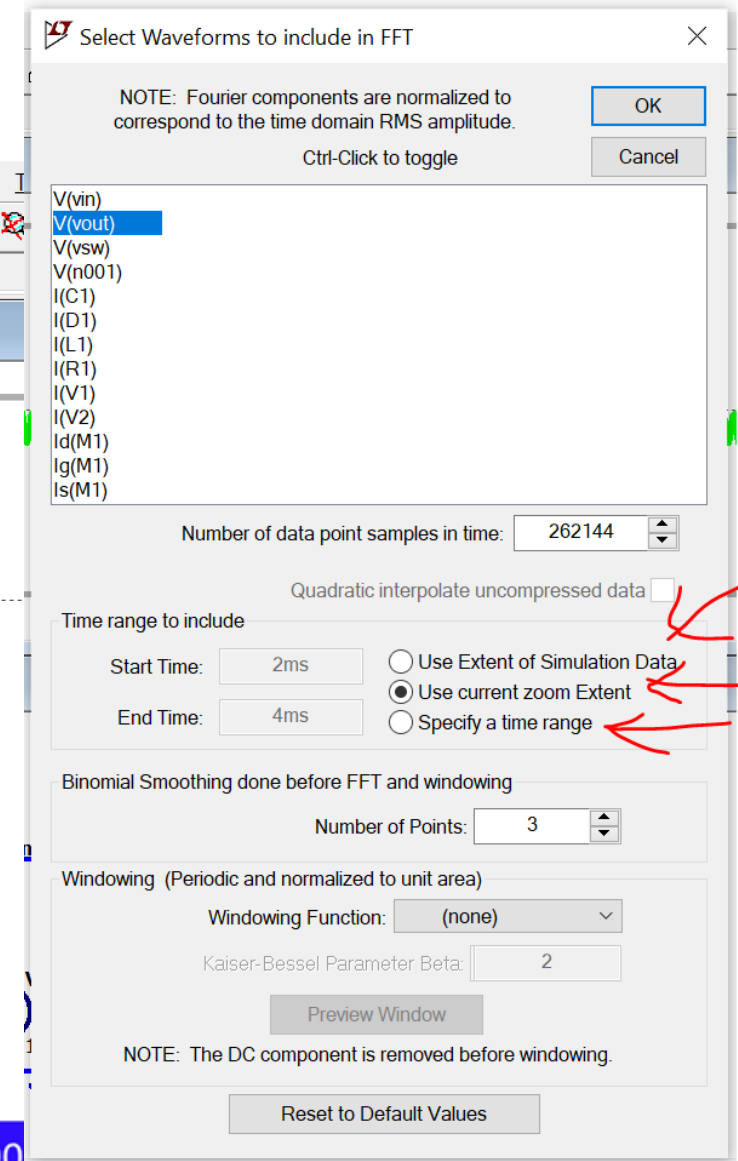
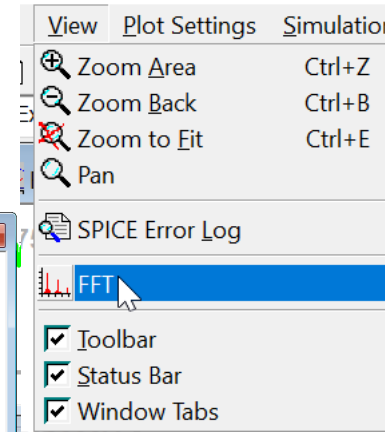


# Task 2a: Select FFT of the signal (output voltage)

- Select the plot window, and View-> FFT
- Select extent of simulation data

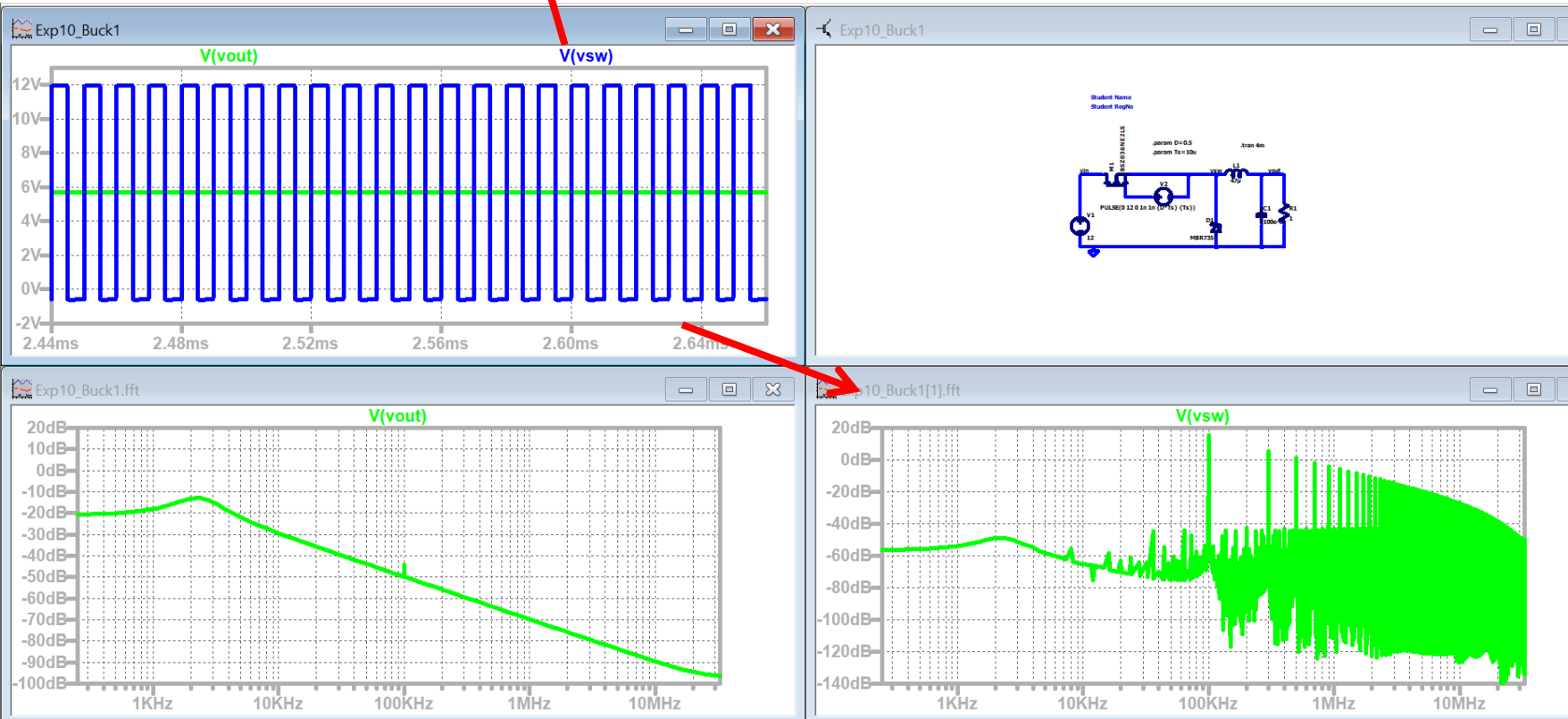


Switching frequency



# Task 2b: Select FFT of the signal (Switch voltage)

- Select the vsw in FFT and plot for entire range  
Notice the frequency and its harmonics.



Select Waveforms to include in FFT

NOTE: Fourier components are normalized to correspond to the time domain RMS amplitude.

Ctrl-Click to toggle

OK Cancel

V(vin)  
V(vout)  
V(vsw)  
V(n001)  
I(C1)  
I(D1)  
I(L1)  
I(R1)  
I(V1)  
I(V2)  
Id(M1)  
Ig(M1)  
Is(M1)

Number of data point samples in time: 262144

Quadratic interpolate uncompressed data ☐

Time range to include

Start Time: 0s ☒ Use Extent of Simulation Data  
End Time: 4ms ☐ Use current zoom Extent  
☐ Specify a time range

Binomial Smoothing done before FFT and windowing

Number of Points: 3

Windowing (Periodic and normalized to unit area)

Windowing Function: (none)

Kaiser-Bessel Parameter Beta: 2

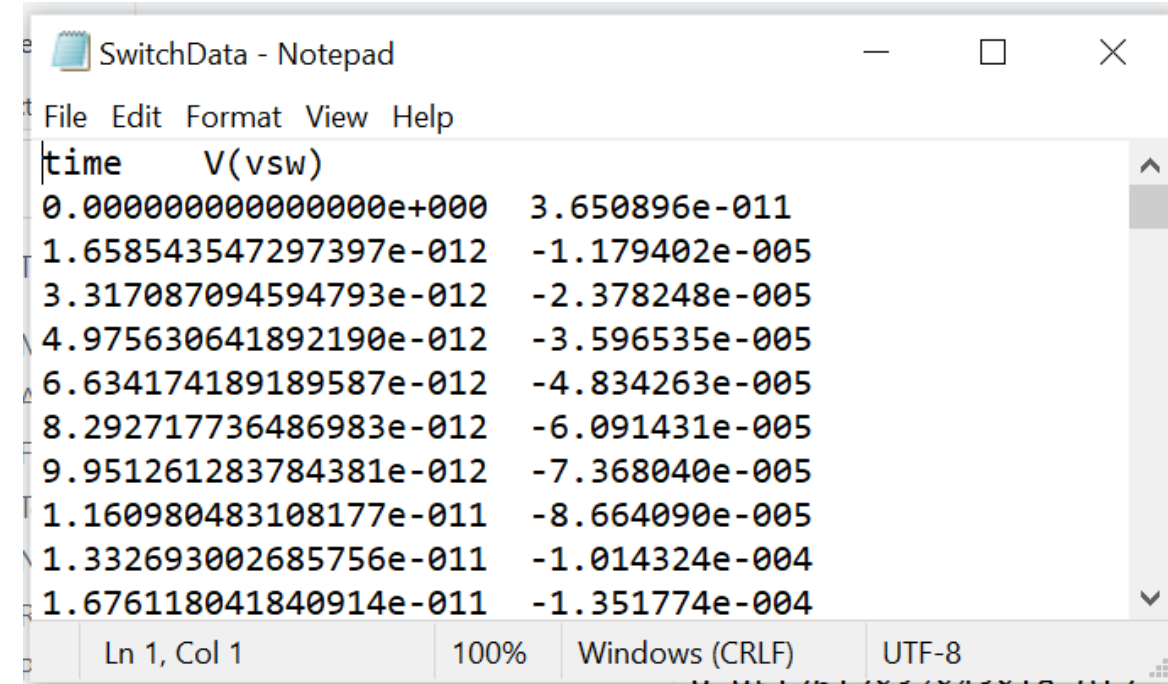
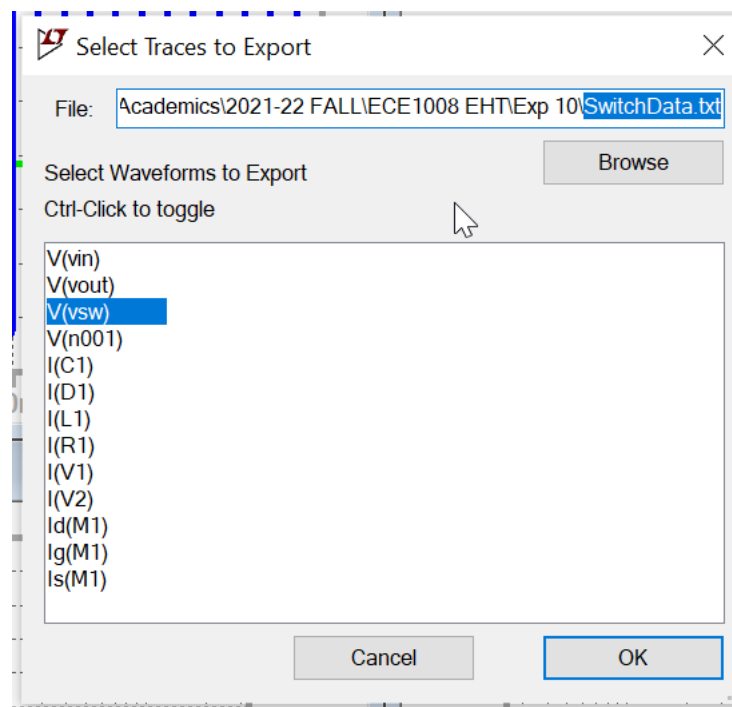
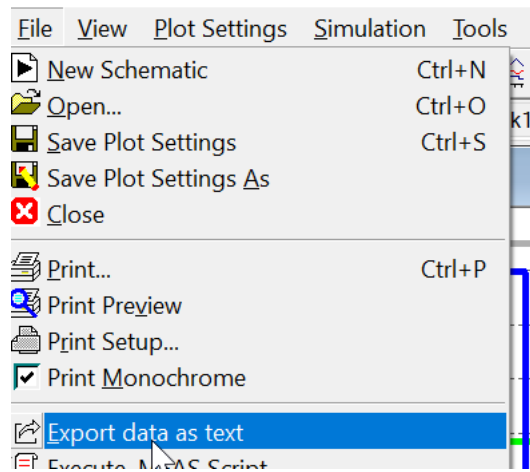
Preview Window

NOTE: The DC component is removed before windowing.

Reset to Default Values

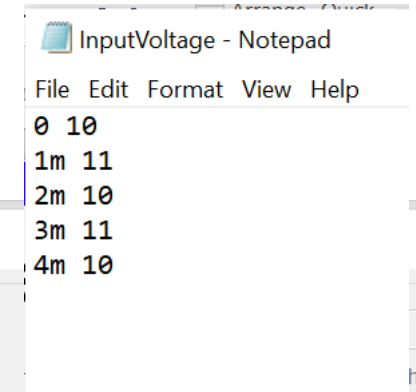
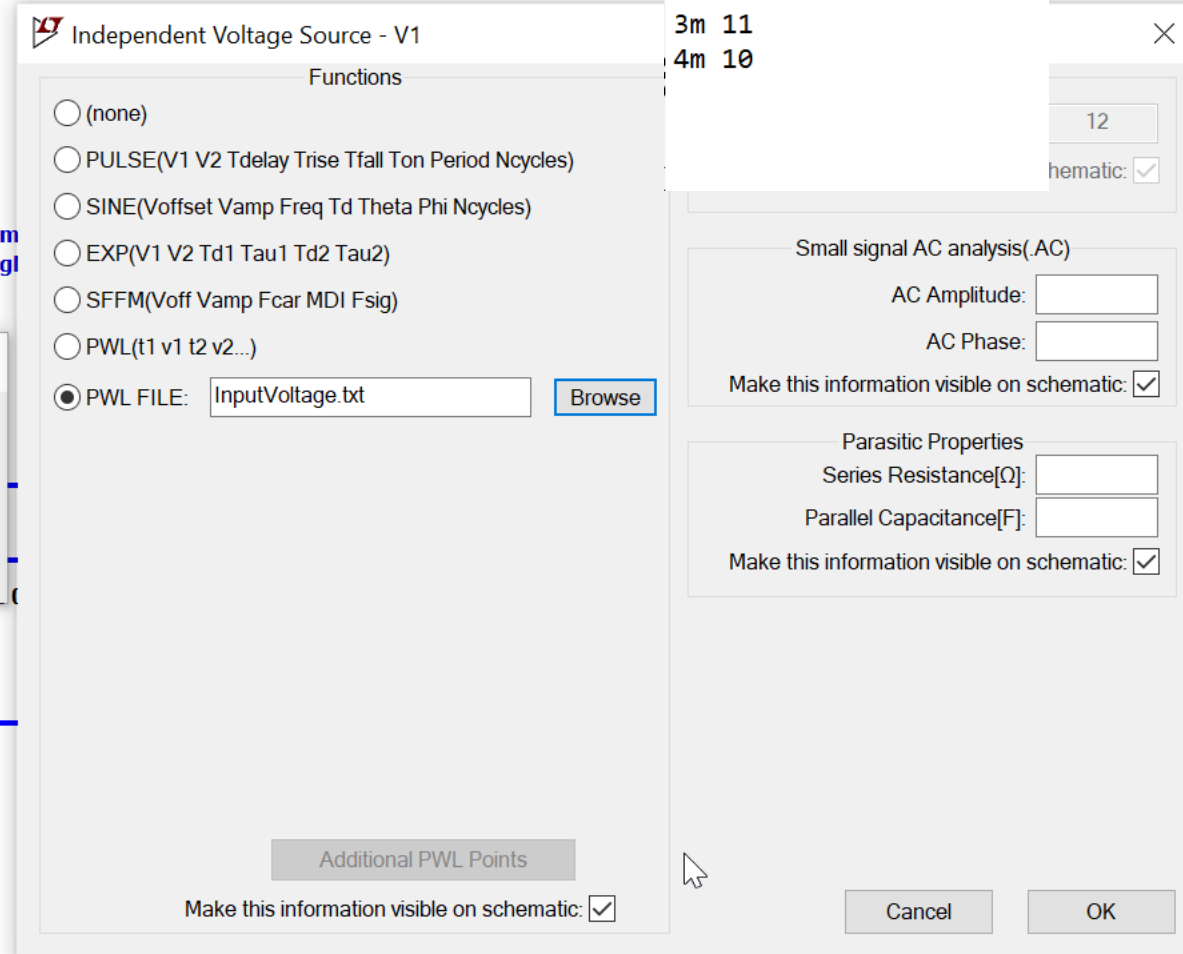
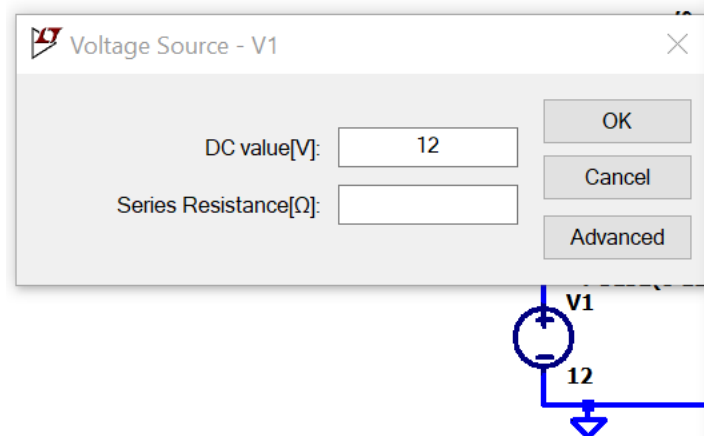
# Task 2c: Export switch voltage plot data

- File -> Export -> Select vsw(switch voltage)



# Task 3: Import txt file as source

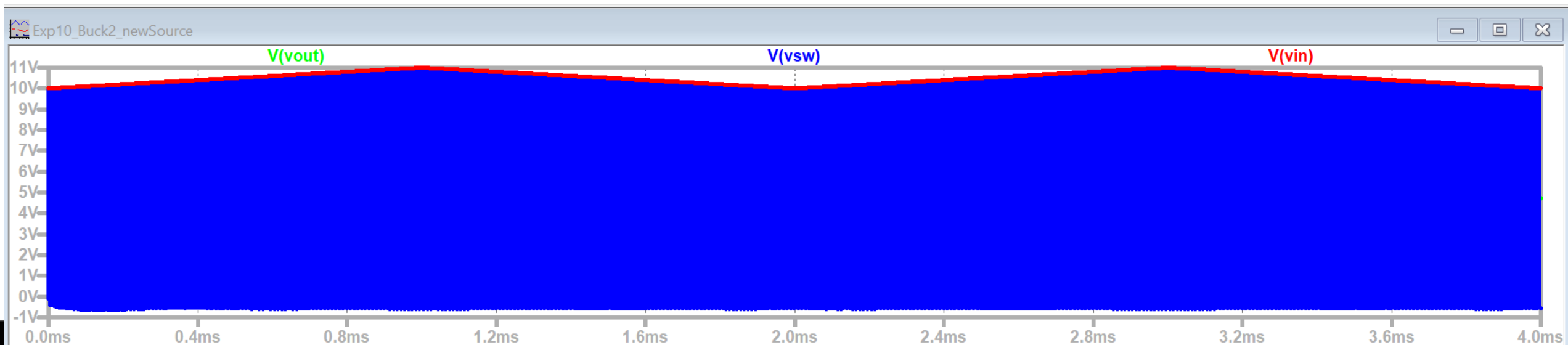
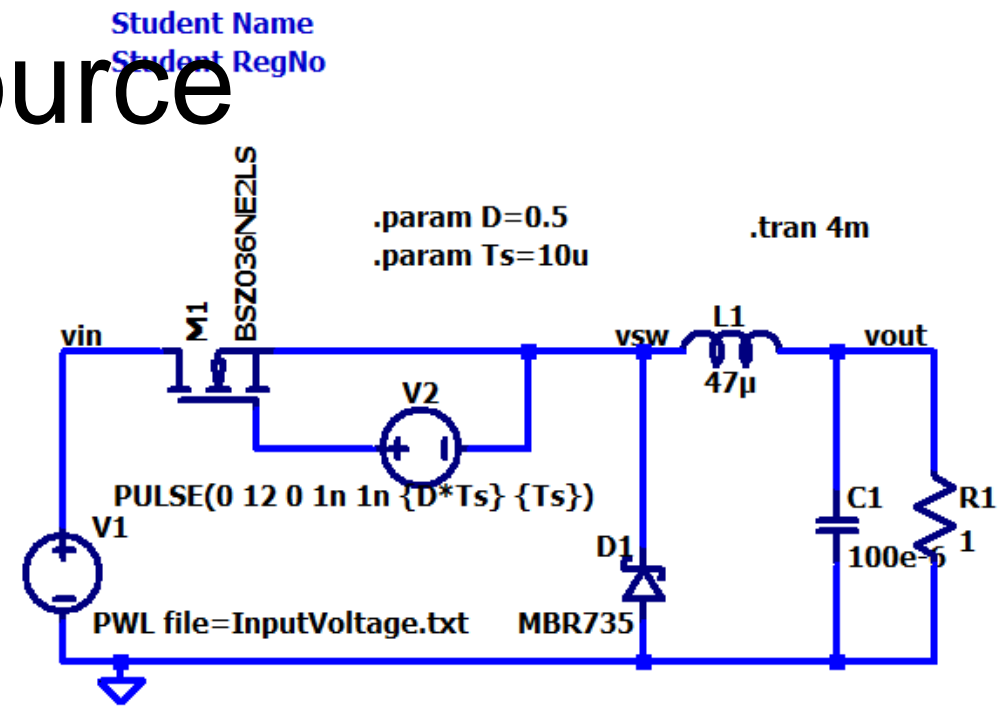
- Save a new text file with extension .txt with the data:
- Right click at input voltage source  
Select pwl(piece wise linear file)





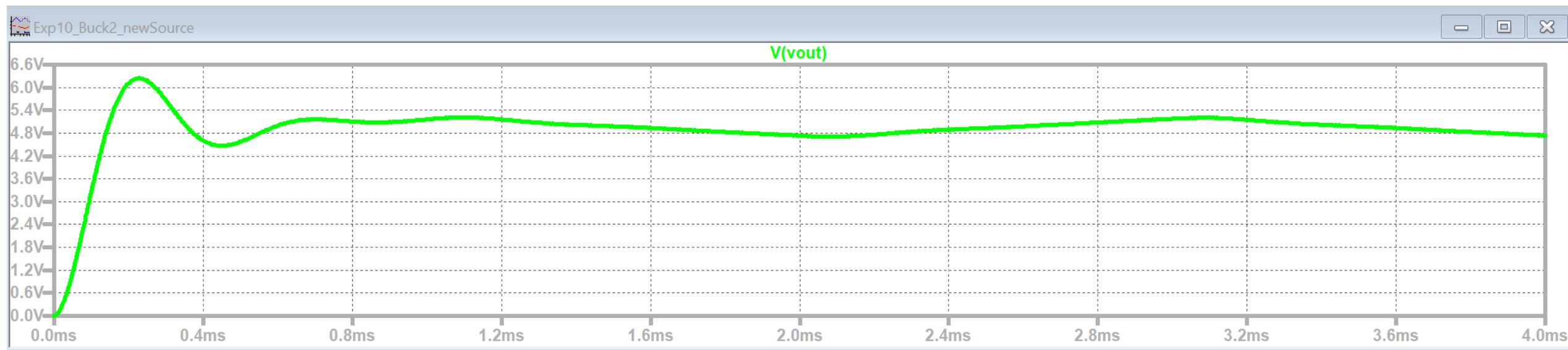
# Task 3: Import txt file as source

- Input voltage source is in RED
- Blue represents the switching voltage



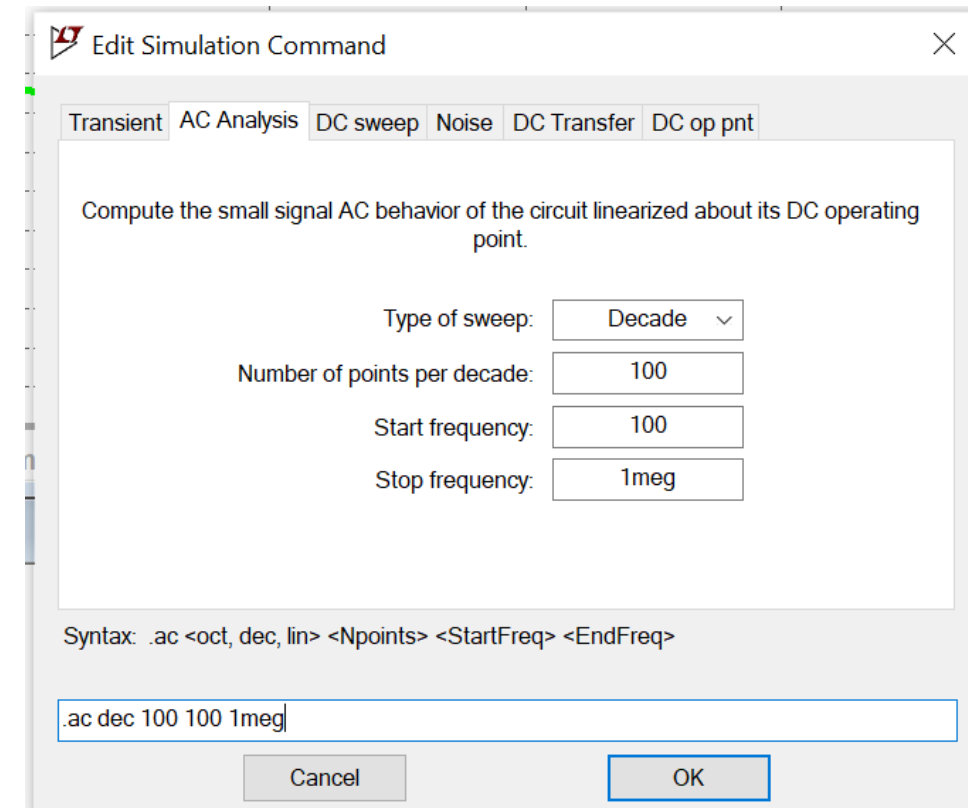
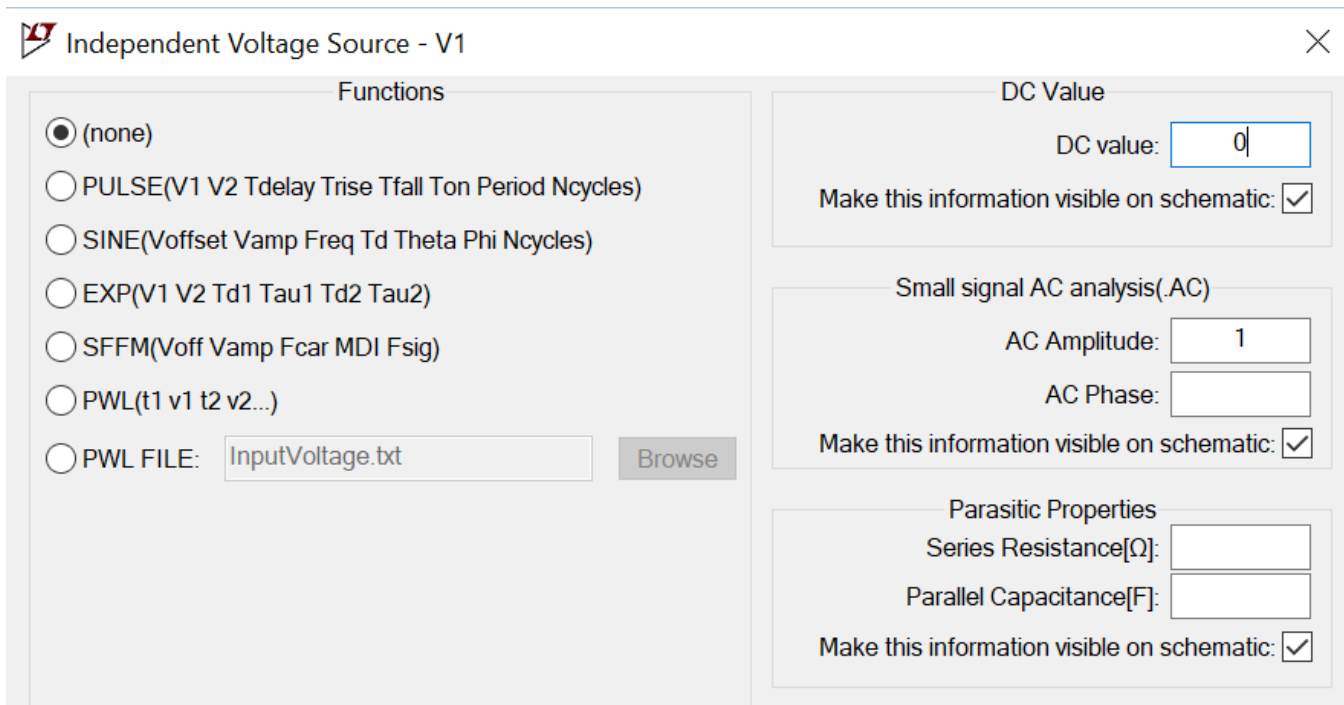
# Task 3: Import txt file as source

- Vout



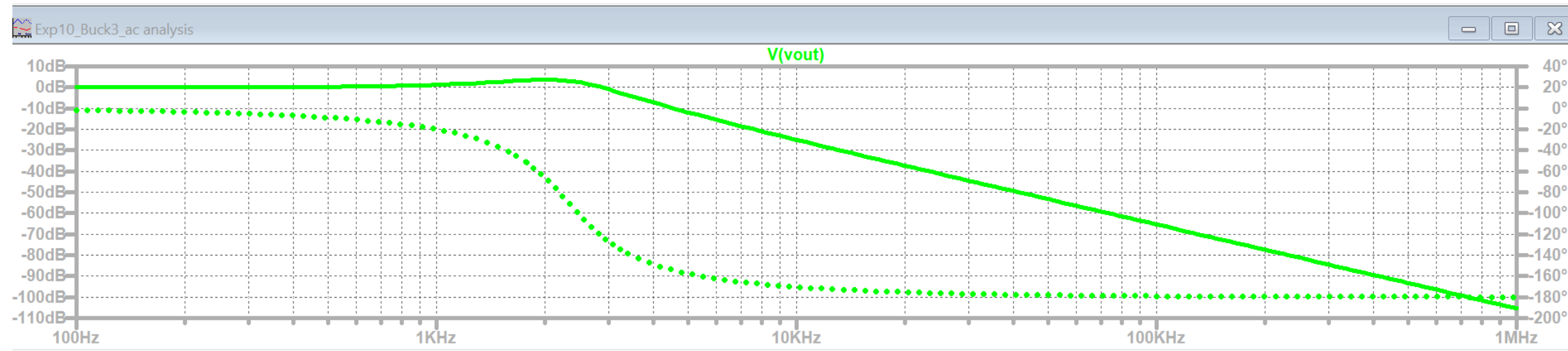
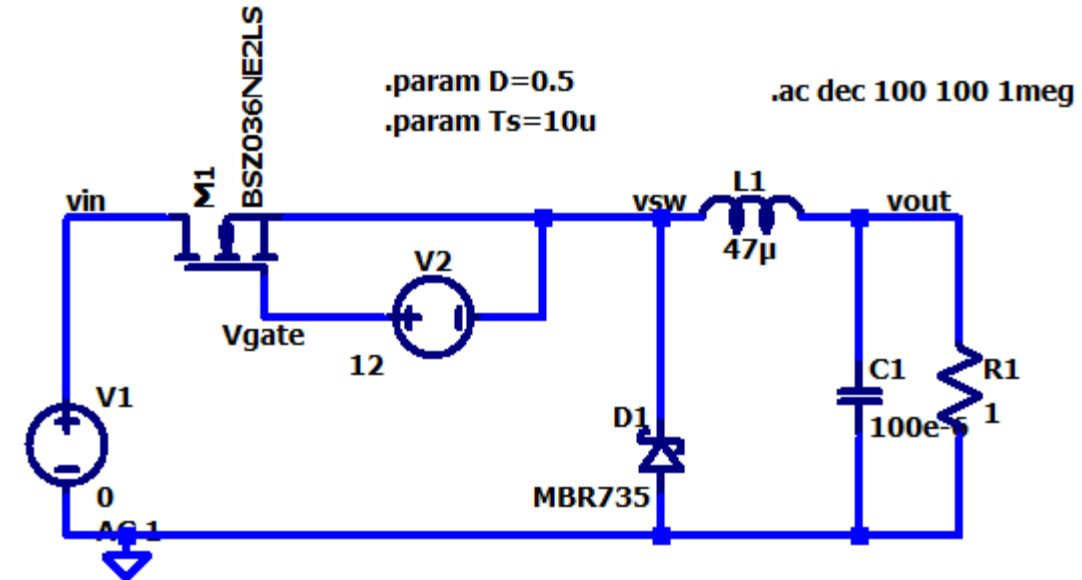
# Task 4: AC analysis

- Replace V2 pulse source to DC (12V)
- Replace V1 input voltage to DC (0V) with an ac amplitude of 1V
- Set simulation as ac analysis:



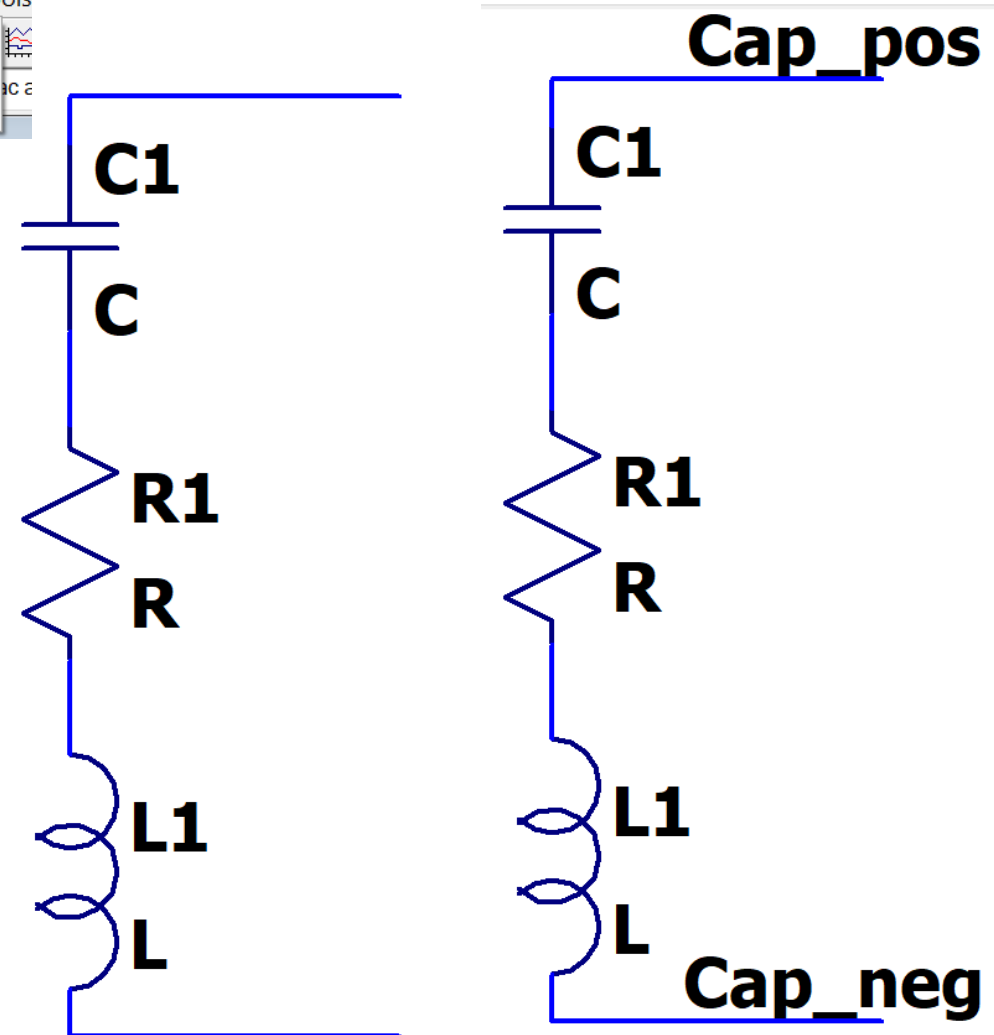
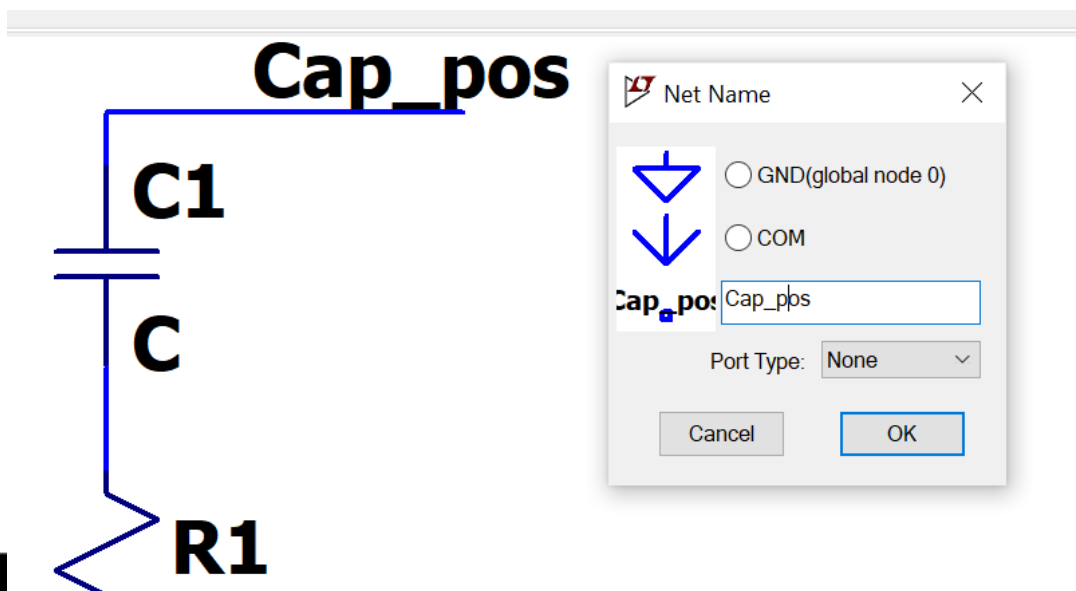
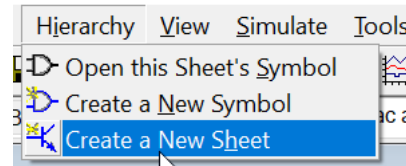
# Task 4: AC analysis

- Close to DC: unity gain  
After resonance: the drop in gain
- After DC: notice the Phase shift



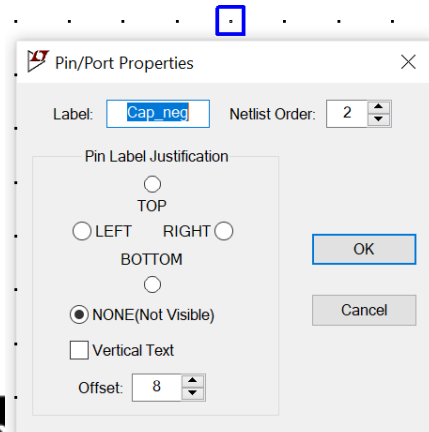
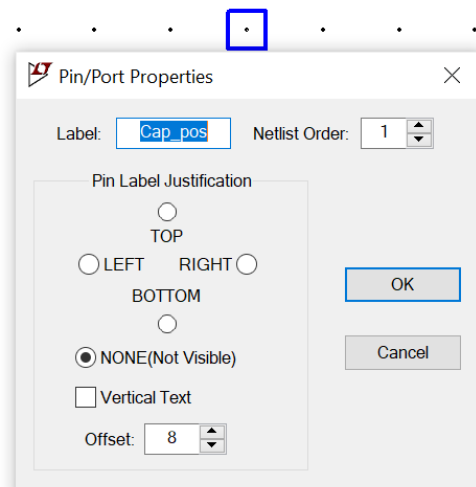
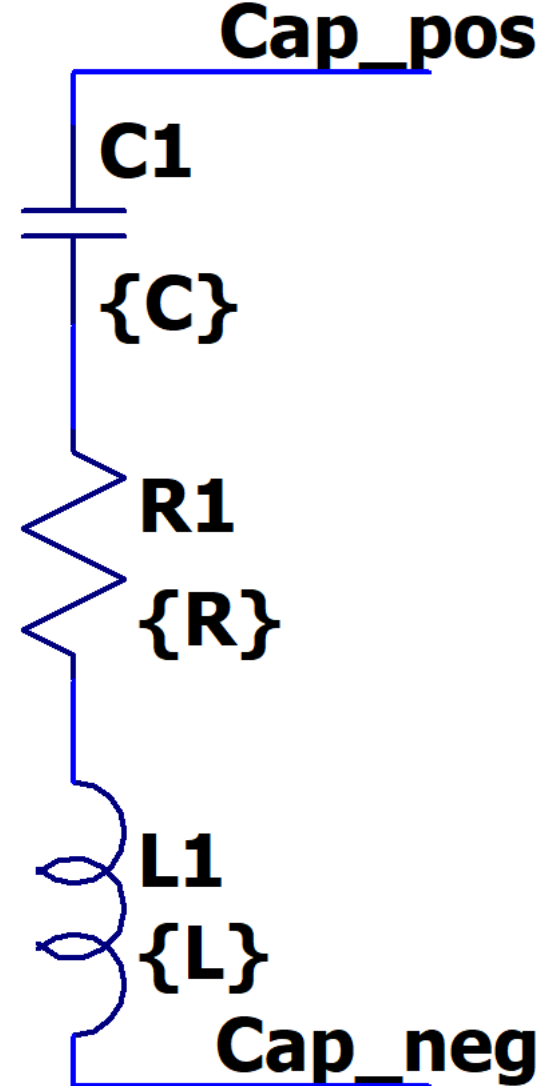
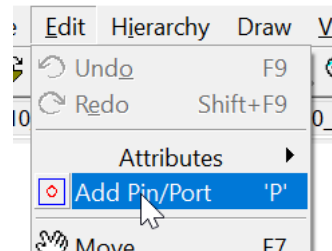
Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Delete the 100uF capacitor.
- Go to Hierarchy -> New sheet  
Place the three passive components (C, L and R) in series.  
Add labelnets to end terminals.



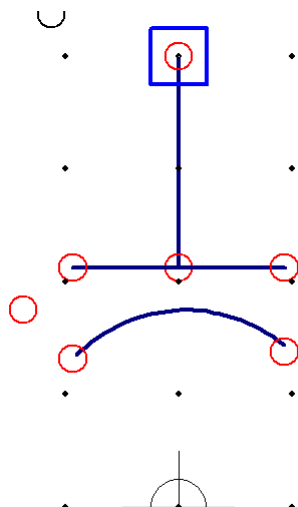
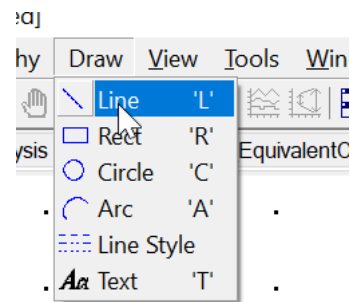
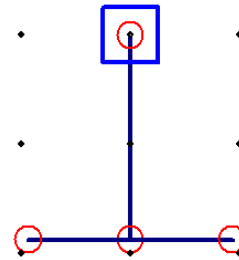
# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Change the values as parameters: {C}, {R} and {L}
- Save as "my\_cap.asc"
- Once sub-circuit is complete Hierarchy->Create New symbol
- Edit-> Add Pins/ports  
Use same label/net names



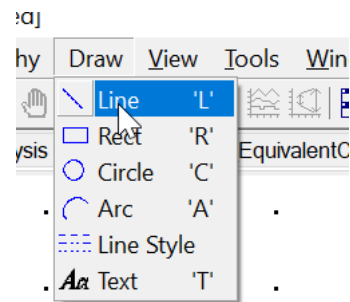
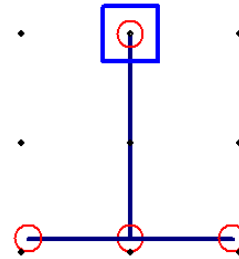
# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Remember the netlist order
- To draw between the pins,  
Draw -> line or arc

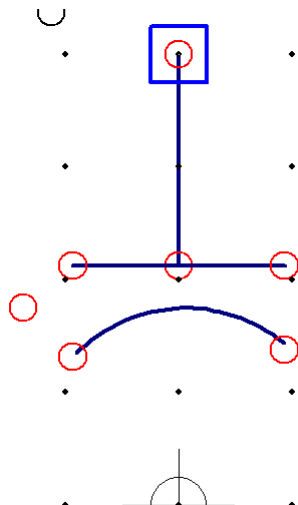


# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Remember the netlist order
- To draw between the pins,  
Draw -> line or arc



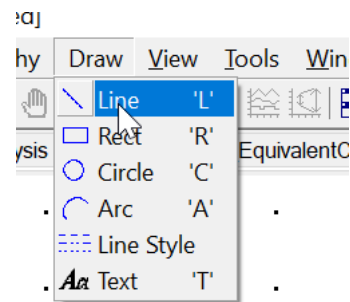
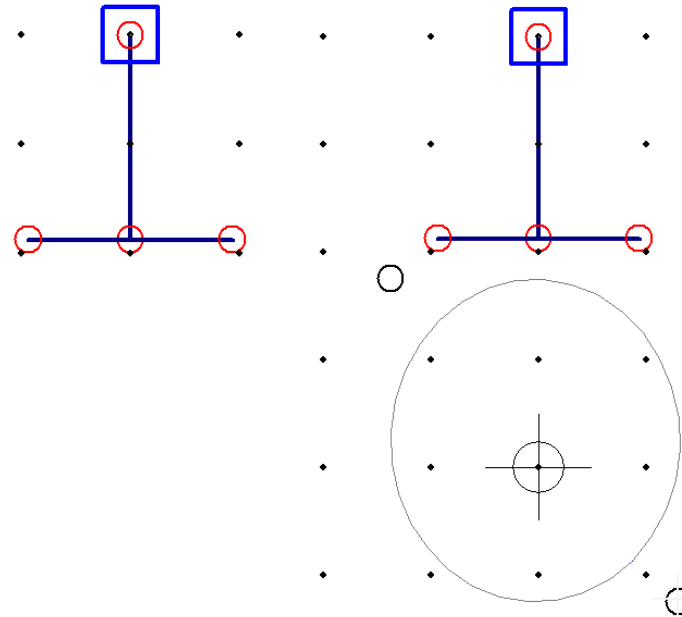
- To draw arc: select arc->



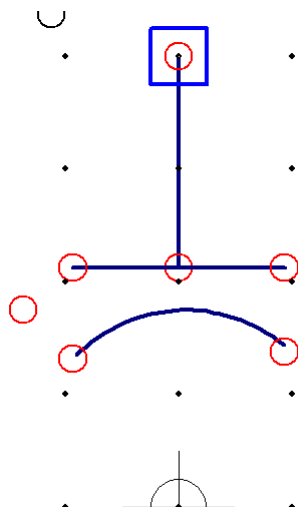


# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Remember the netlist order
- To draw between the pins,  
Draw -> line or arc

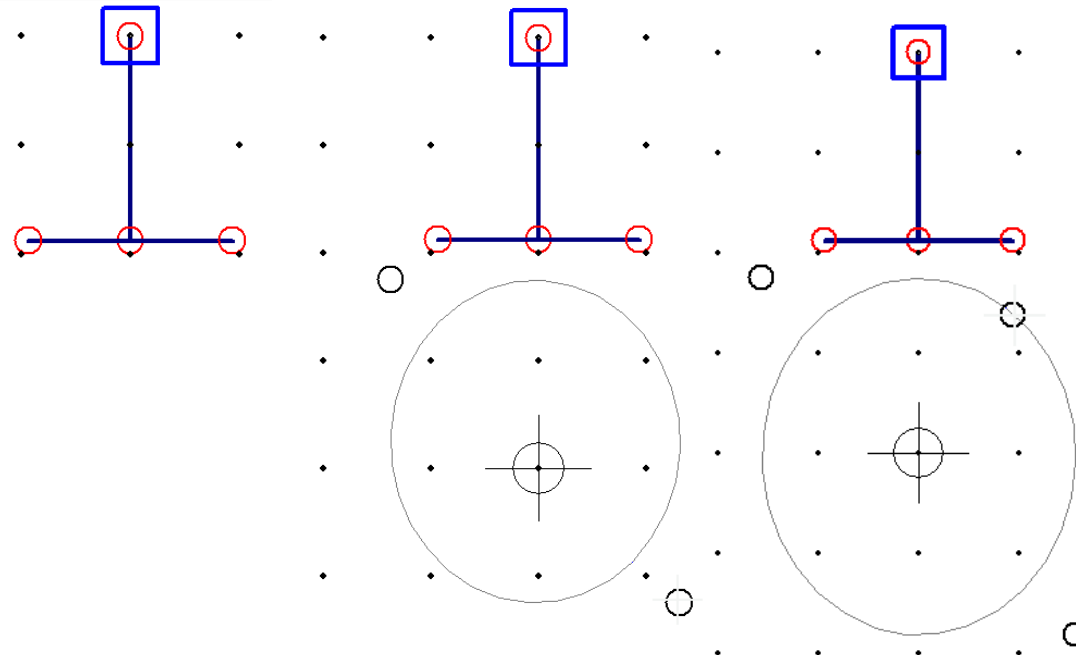
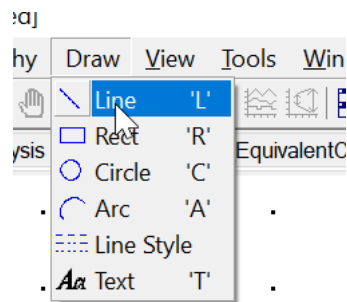


- To draw arc: select arc->  
Draw an ellipse,

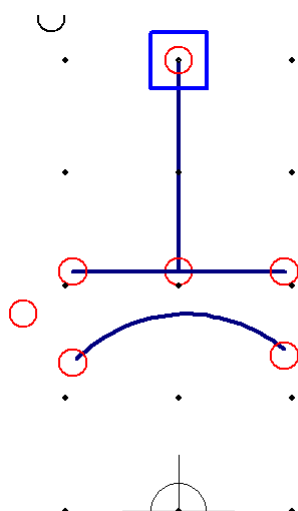


# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Remember the netlist order
- To draw between the pins,  
Draw -> line or arc

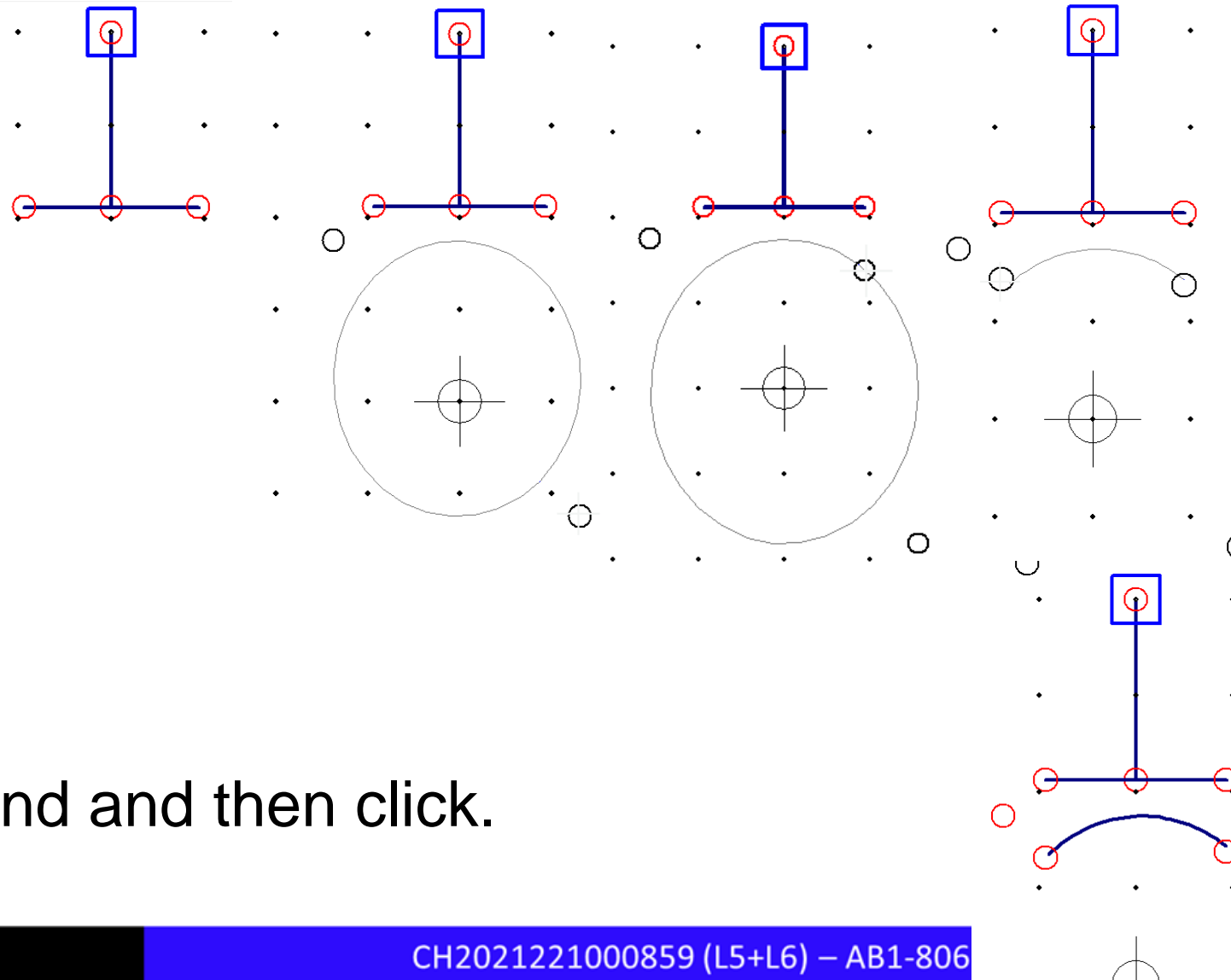
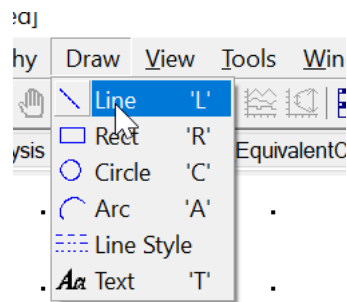


- To draw arc: select arc->  
Draw an ellipse,  
Select the right end of arc



# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

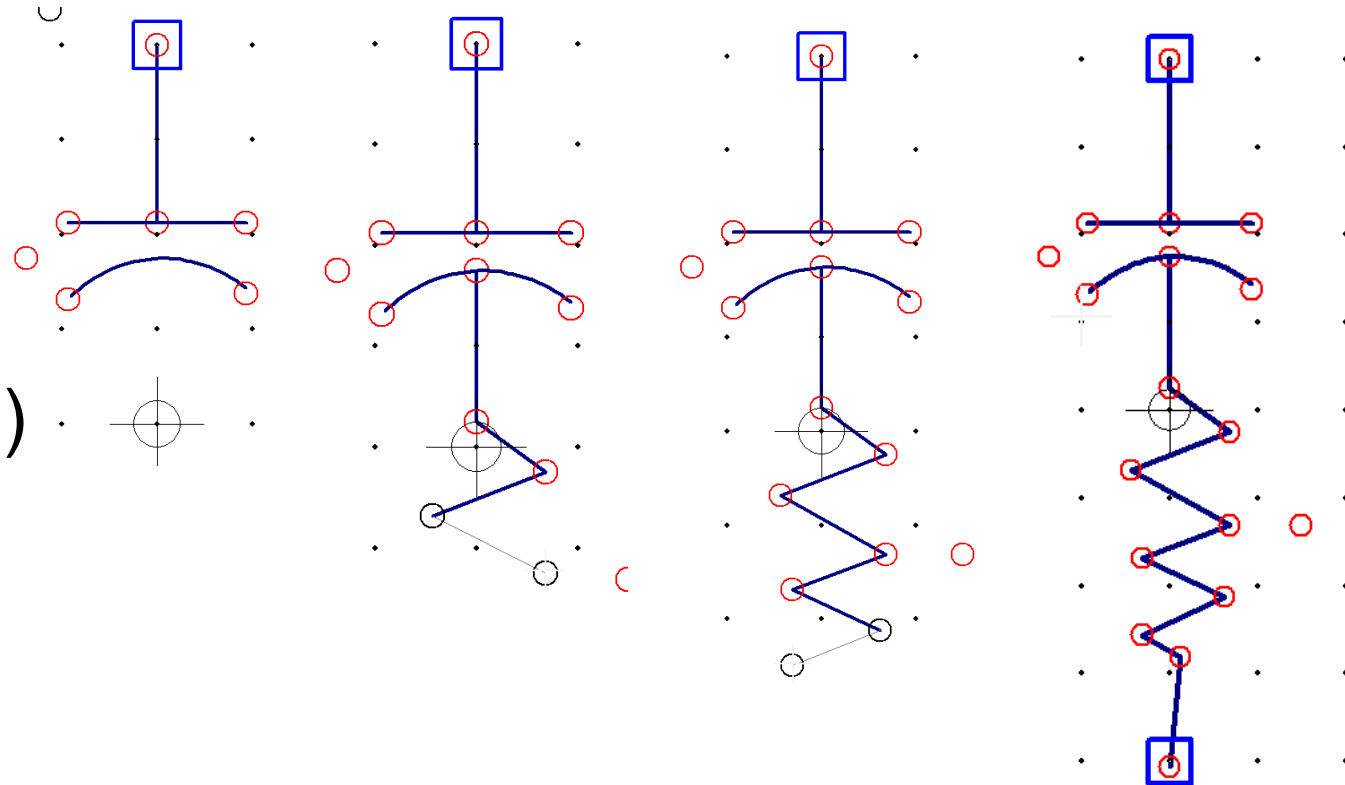
- Remember the netlist order
- To draw between the pins,  
Draw -> line or arc



- To draw arc: select arc->  
Draw an ellipse,  
Select the right end of arc  
Then select location of left end and then click.

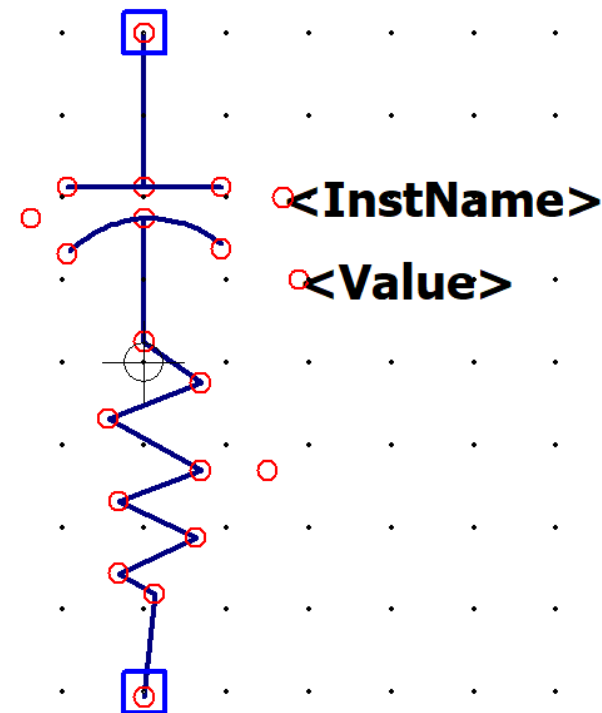
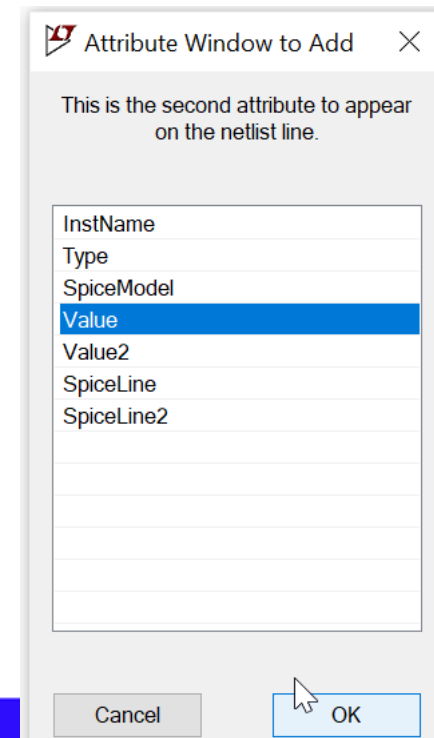
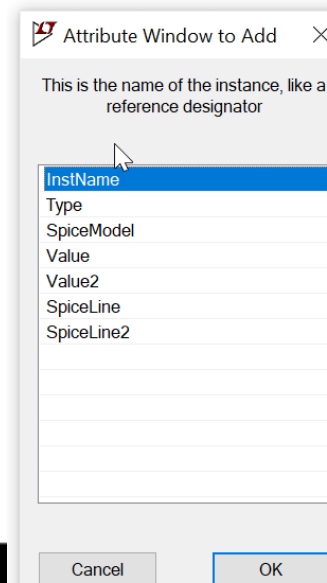
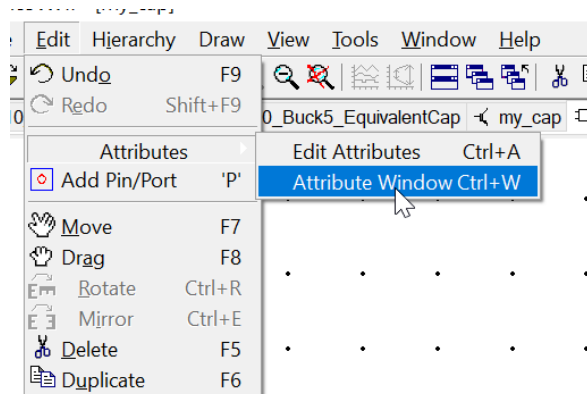
## Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Using Draw -> Line  
Complete the custom symbol as Capacitor with series resistor
- File-> Save-> my\_cap.asy  
(same name with .asy for symbol)



# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

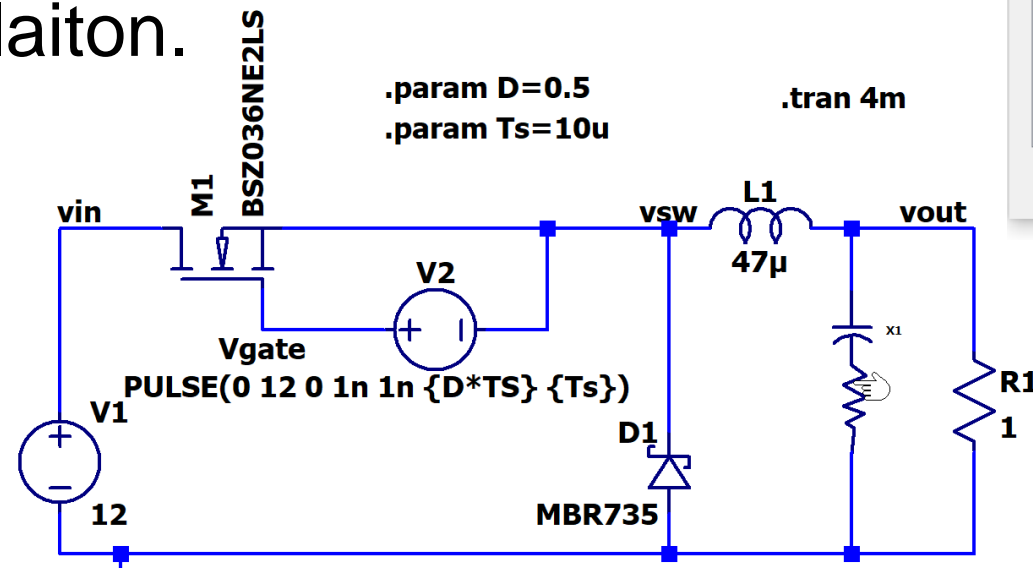
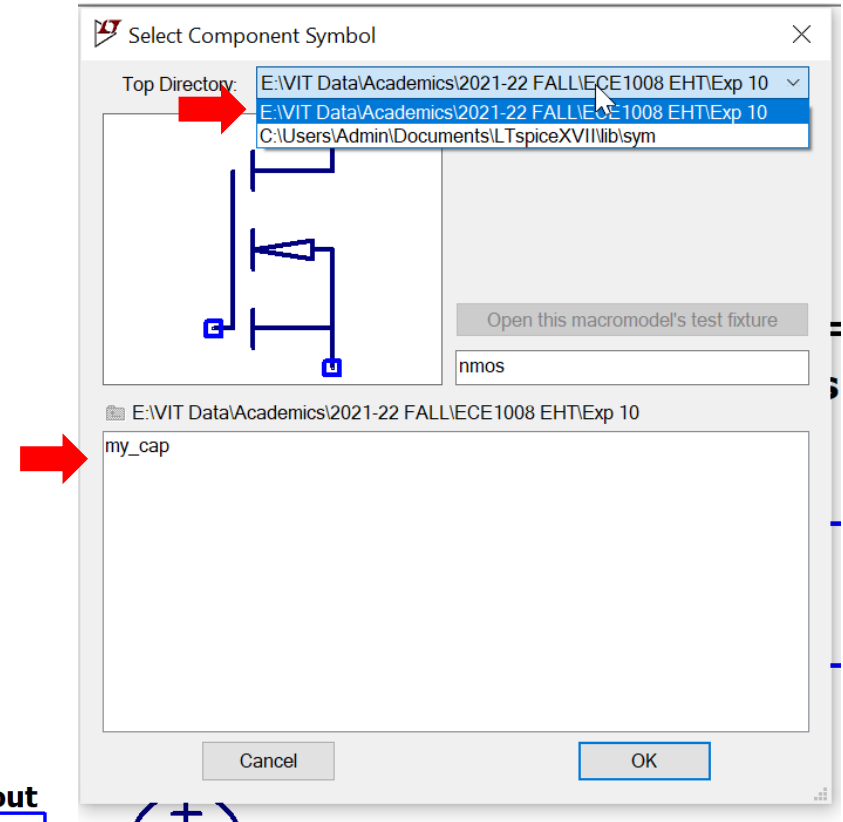
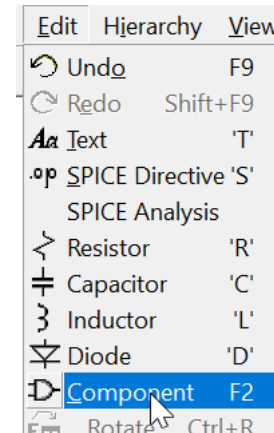
- Using Draw -> Line  
Complete the custom symbol as Capacitor with series resistor
- File-> Save-> my\_cap.asy (same name with .asy for symbol)
- Edit-> Attribute window-> Inst Name  
-> Value
- Close the symbol.



# Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Open circuit of Buck converter:  
Edit-> component ->  
Search the folder where you had saved the my\_cap symbol.  
Place the my\_cap symbol instead of Capacitor in the initial circuit of 4m transient simulation.

Student Name  
Student RegNo

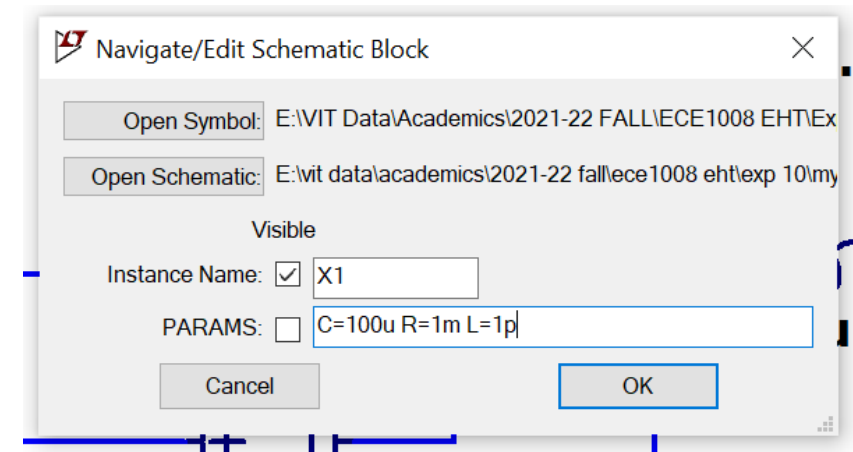
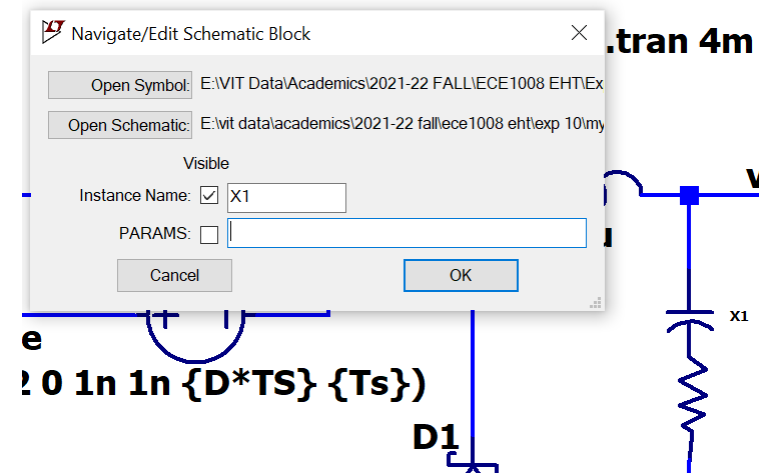
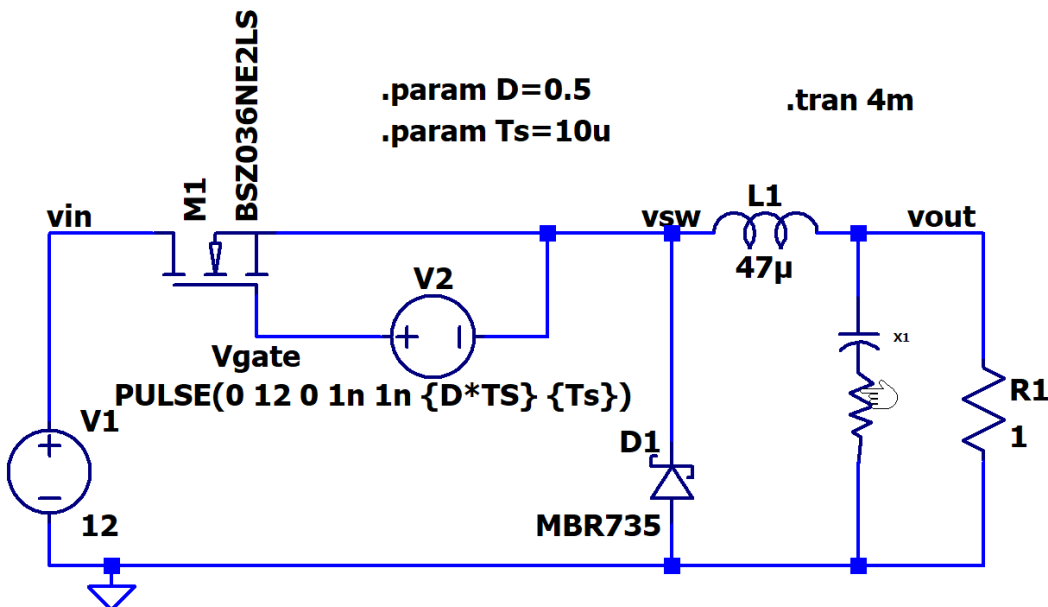


Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

5a) Right click at the my\_cap symbol and add values as  
 $C=100\mu$   $R=1m$   $L=1p$

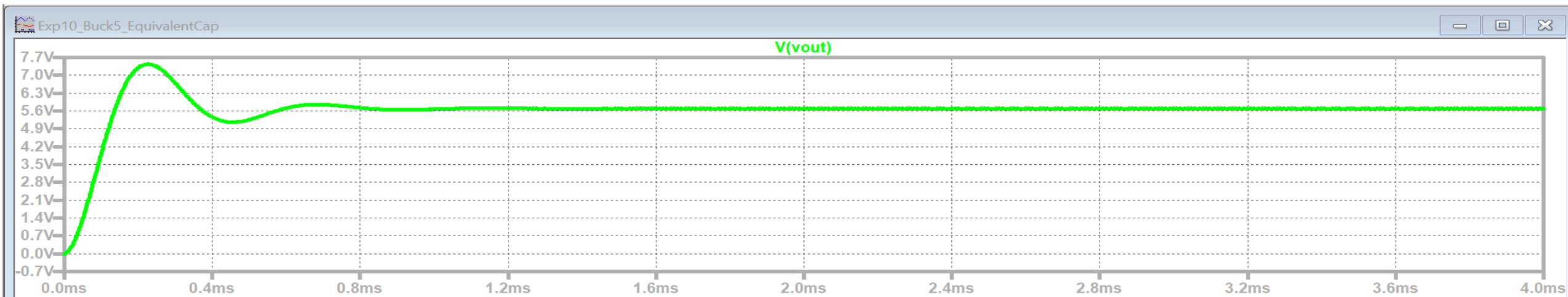
• Simulation -> RUN

Student Name  
 Student RegNo



Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

5a)  $C=100\mu$   $R=1m$   $L=1p$  (Similar to earlier circuit)

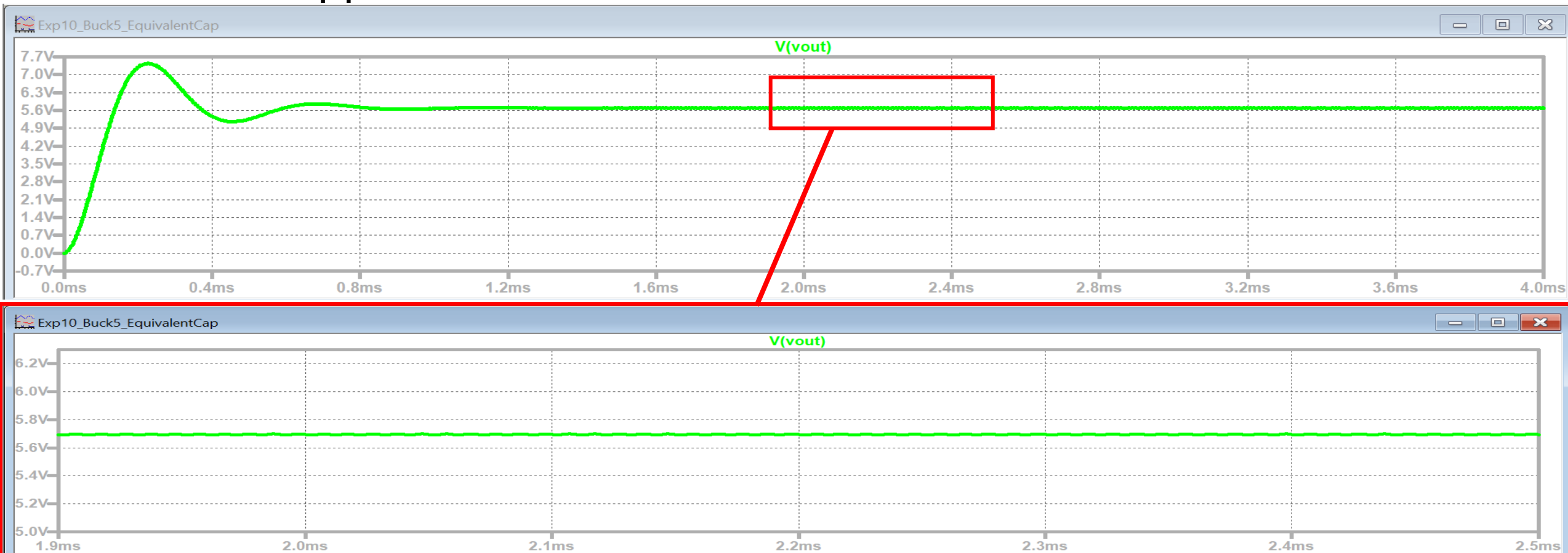




Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

5a)  $C=100\mu$   $R=1m$   $L=1p$  (Similar to earlier circuit)

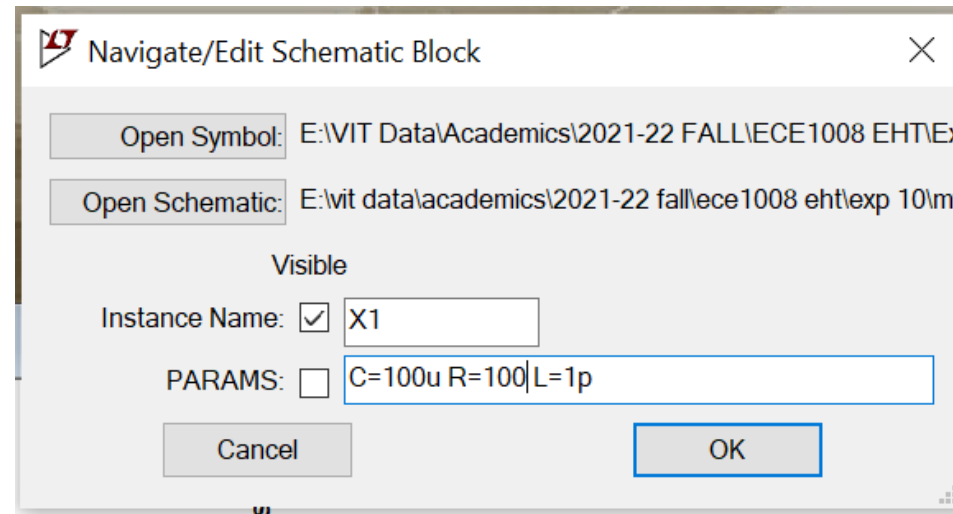
Less ripples as before.



Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

Change the resistance to 100 (unrealistic) to check if symbol works

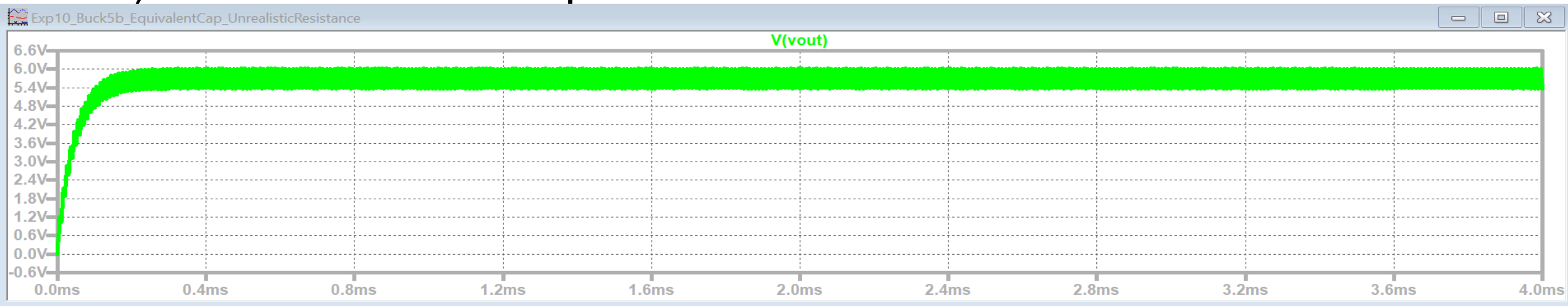
5b)  $C=100\mu$   **$R=100$**   $L=1p$  :



Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

Change the resistance to 100 (unrealistic) to check if symbol works

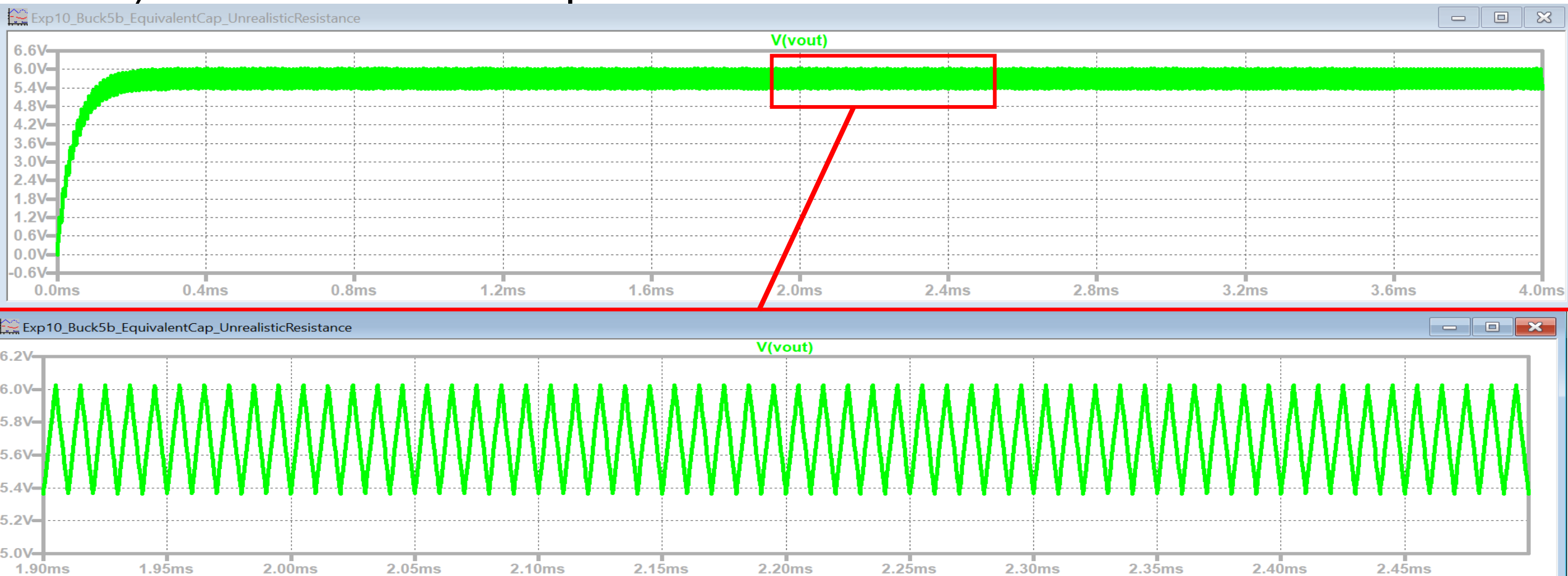
5b)  $C=100\mu$   **$R=100$**   $L=1p$  :



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# Important NOTE

- Enter your **registration number** and **Full Name** next to **all your circuits** and the **output plots**.
- Keep the background of circuit and plot as white.



# LAB record instructions:

For the lab experiment,

- Write the **Aim**.
- Complete the **Software/Hardware components used**.
- **Obtain the expression for the outputs.**
- Place the respective **circuits in LT Spice**.
- Connect the inputs and outputs. Name them and **write the same in the lab copy(inputs and outputs section)**.
- Use probe in LT spice to plot all possible combinations.
- Write a **concluding statement for each circuit**.
- **Submit** the document's soft copy **on time** in lms.vit.ac.in when available.

