5. Design and Analysis of Common Emitter Amplifier

Course: ECE1008 – Electronic Hardware Troubleshooting LAB

-Dr Richards Joe Stanislaus

Assistant Professor - SENSE

Email: 51749@vitstudent.ac.in

VIT®

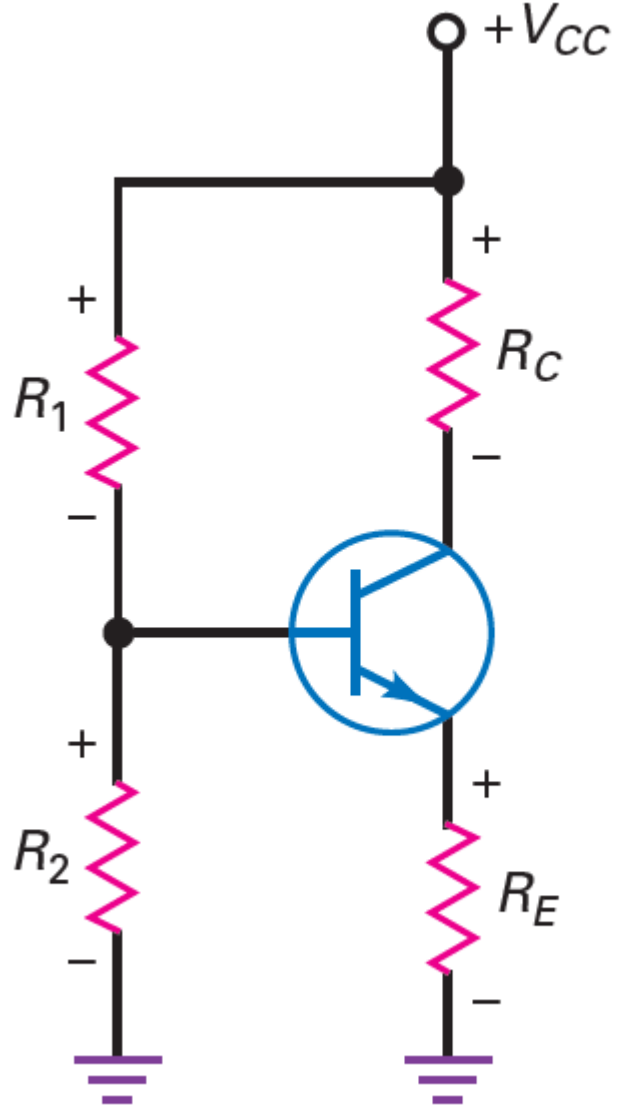
Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

CHENNAI

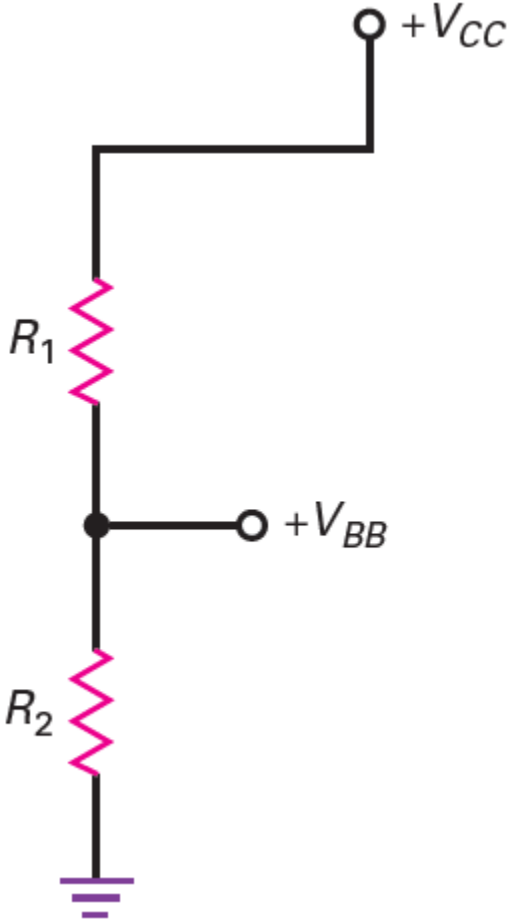
1. Voltage Divider Bias

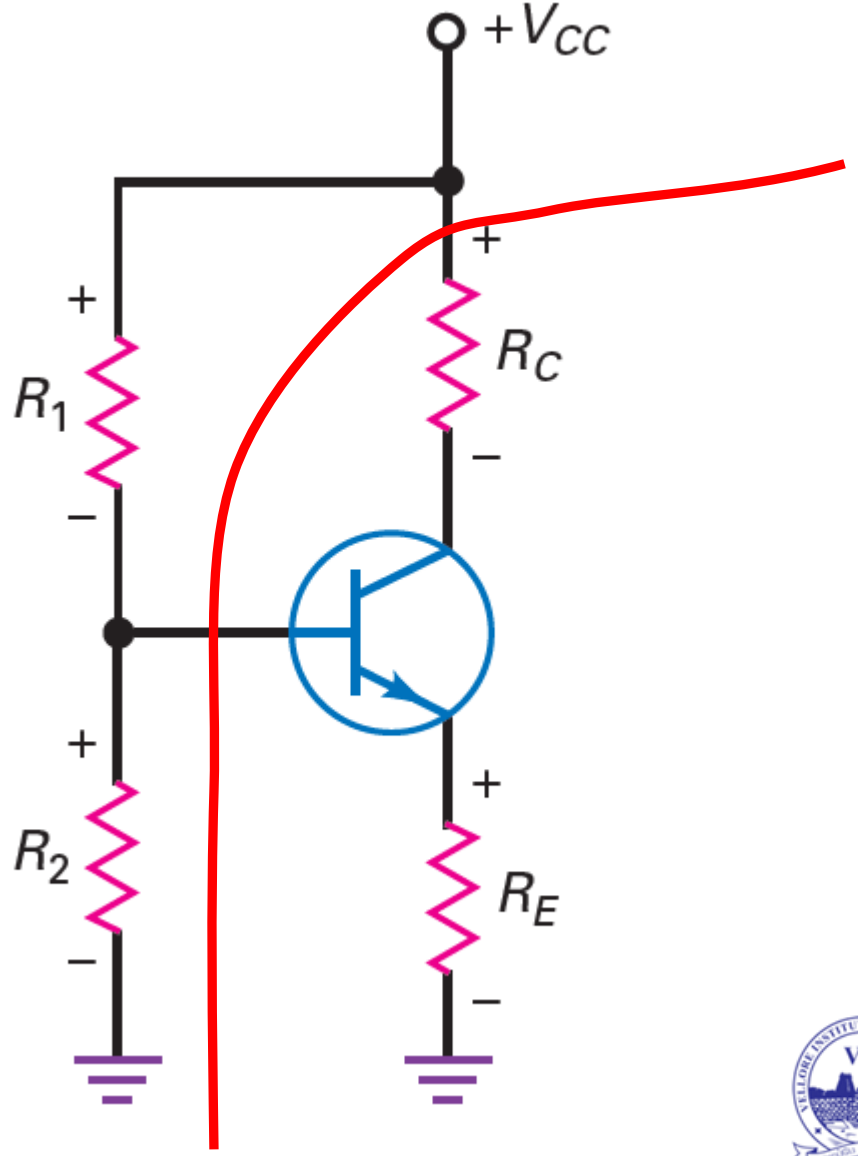
- $V_{BB} =$



1. Voltage Divider Bias

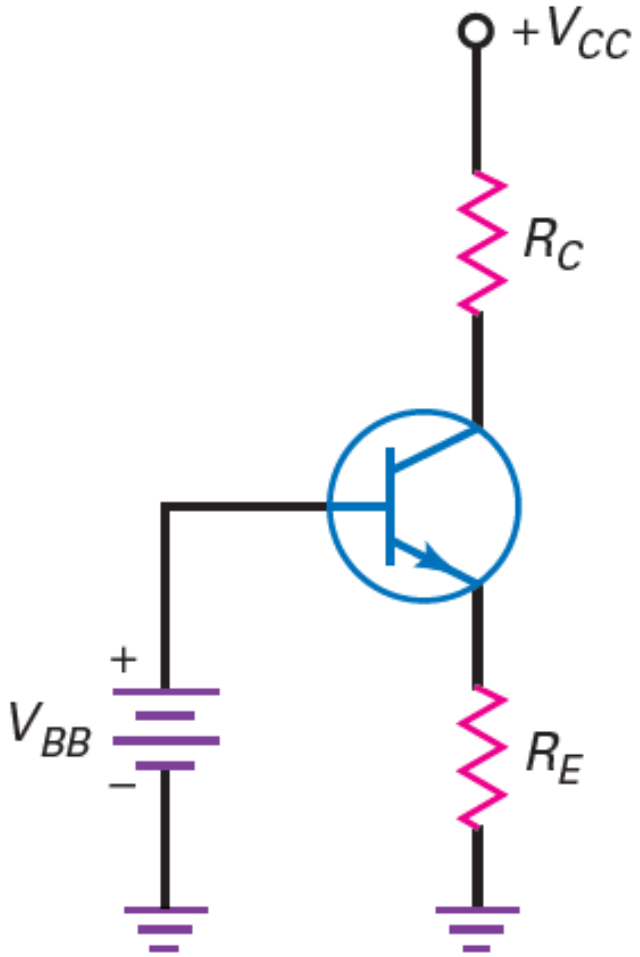
- $V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2}$





1. Voltage Divider Bias

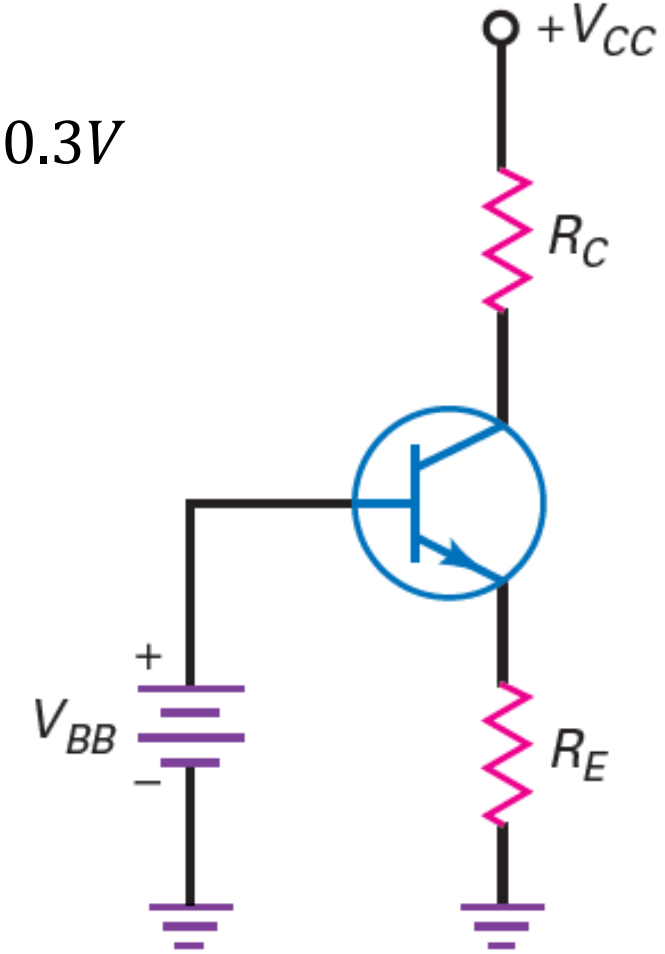
- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} =$



1. Voltage Divider Bias

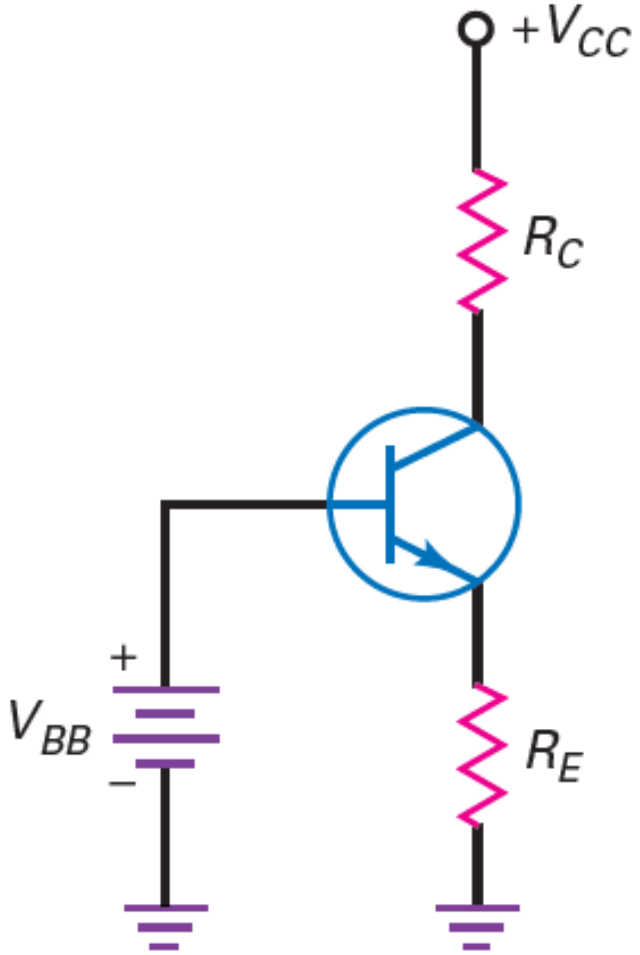
- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} = V_{BB} - V_{BE}$
- $I_E =$

Silicon: $V_{BE} = 0.7V$
Germanium: $V_{BE} = 0.3V$



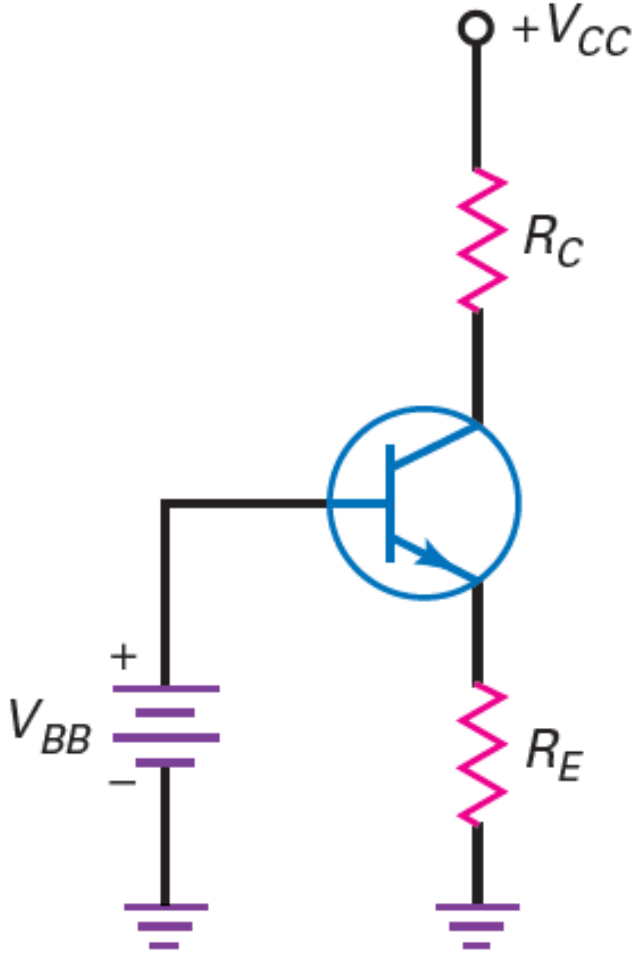
1. Voltage Divider Bias

- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} = V_{BB} - V_{BE}$
- $I_E = V_{EE}/R_E$
- $I_C \approx$



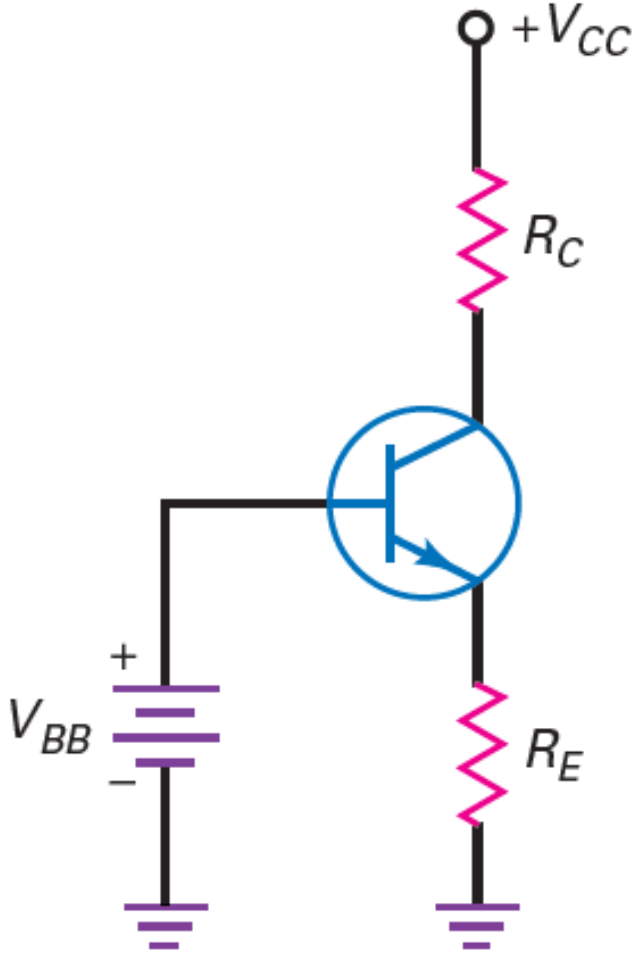
1. Voltage Divider Bias

- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} = V_{BB} - V_{BE}$
- $I_E = V_{EE}/R_E$
- $I_C \approx I_E$
- $V_C =$



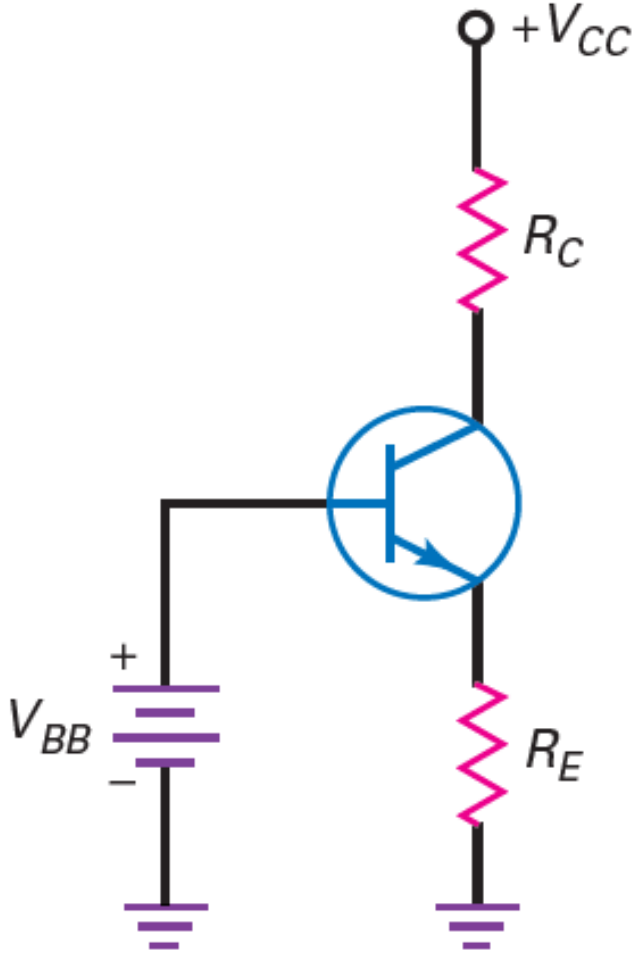
1. Voltage Divider Bias

- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} = V_{BB} - V_{BE}$
- $I_E = V_{EE}/R_E$
- $I_C \approx I_E$
- $V_C = V_{CC} - I_C R_C$
- $V_{CE} =$



1. Voltage Divider Bias

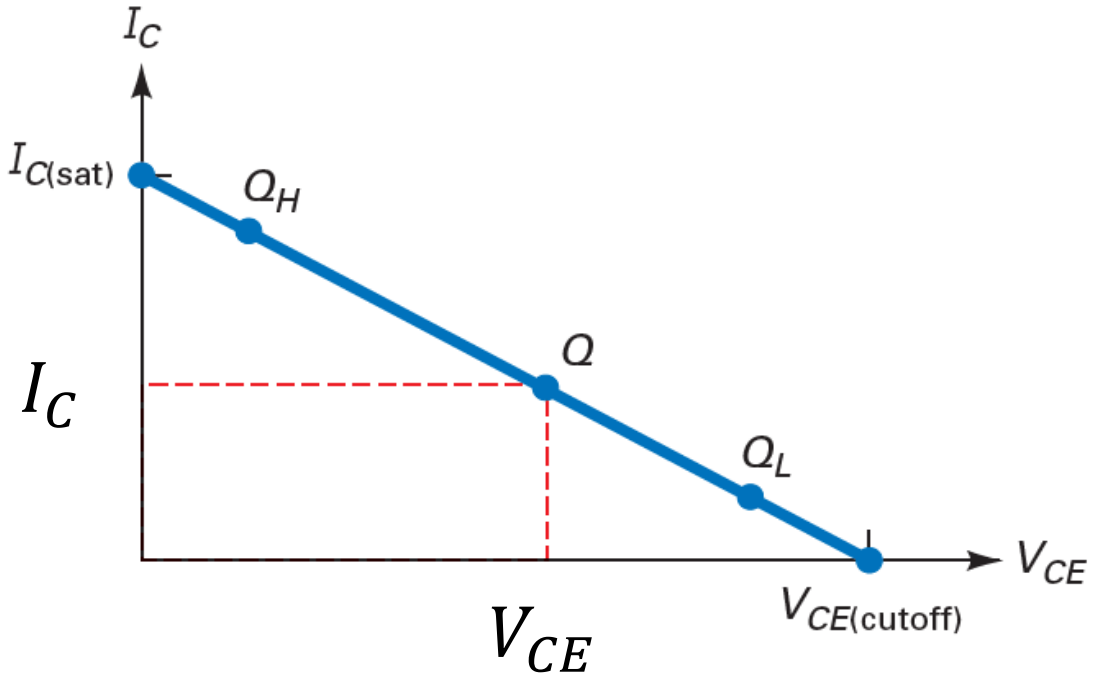
- $V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$
- $V_{EE} = V_{BB} - V_{BE}$
- $I_E = V_{EE}/R_E$
- $I_C \approx I_E$
- $V_C = V_{CC} - I_C R_C$
- $V_{CE} = V_C - V_E$

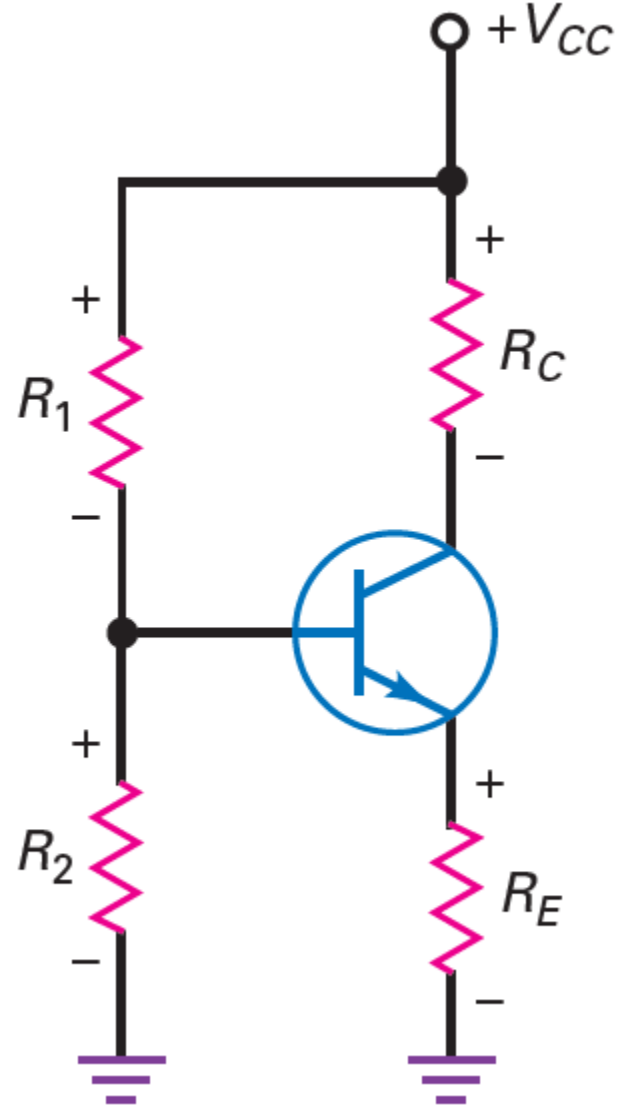


2. Q point(operating point along load line)

quiescent

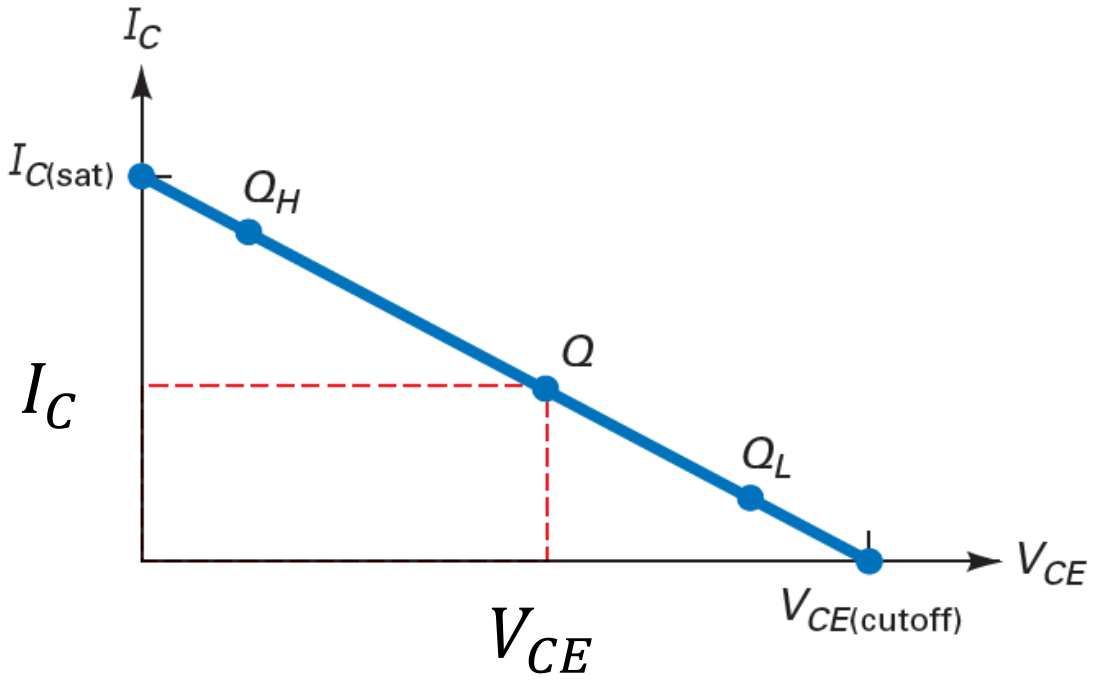
- Q point is generally moved by varying R_E:
- $I_E =$
- $V_C =$
- $V_{CE} =$

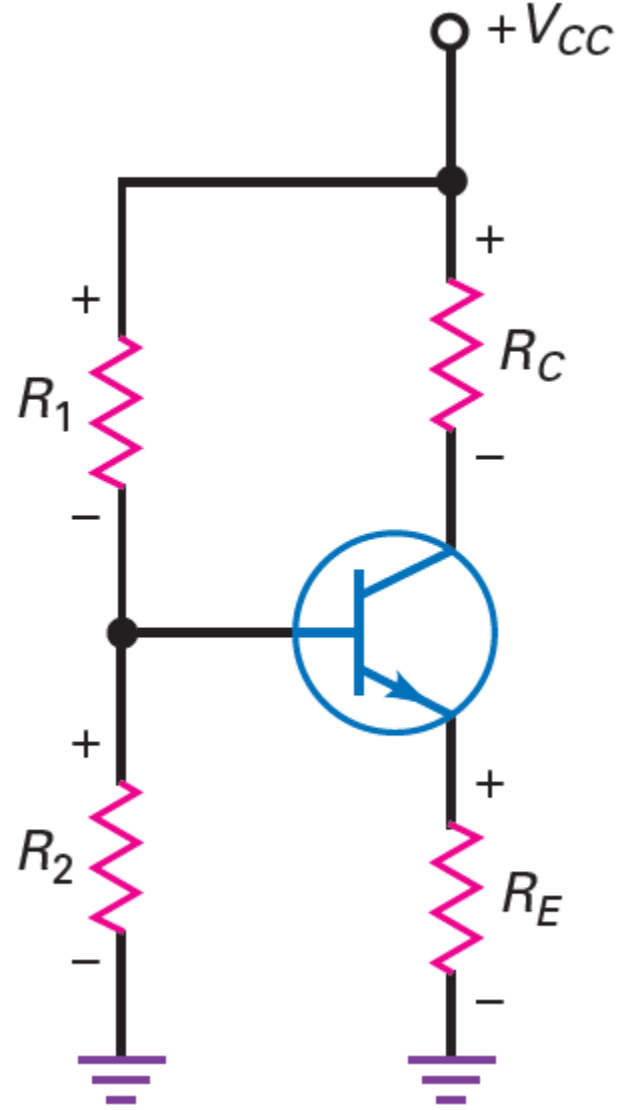




2. Q point(operating point along load line)

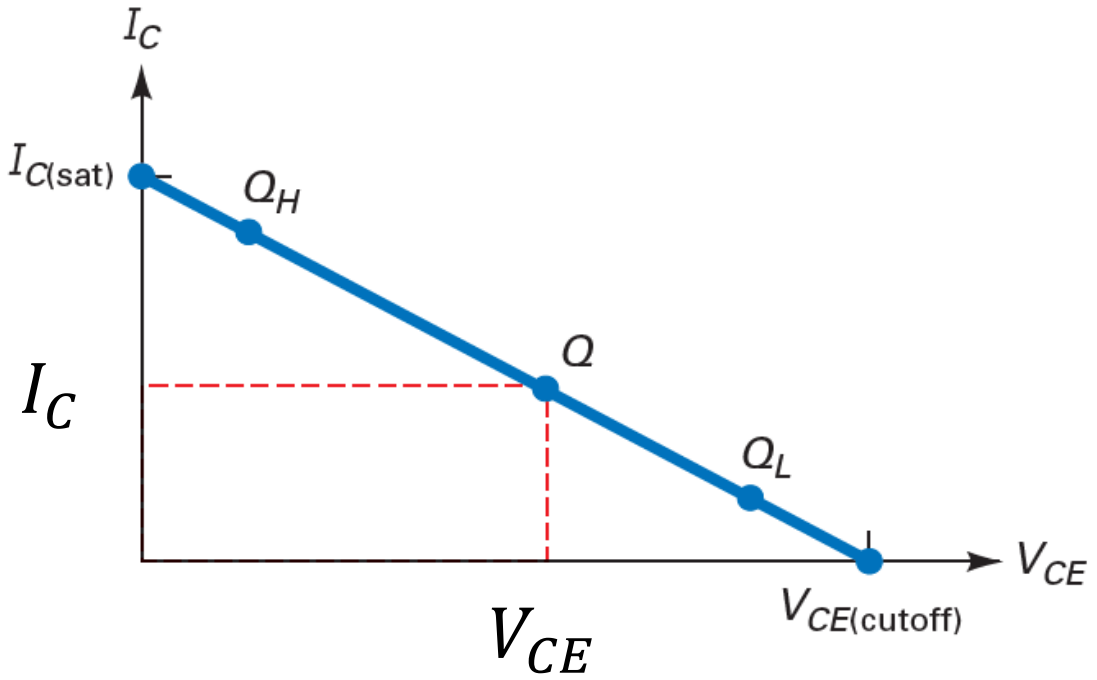
- Q point is generally moved by varying R_E:
- $I_E = V_{EE}/R_E$
- $V_C = V_{CC} - I_C R_C \approx V_{CC} - I_E R_C$
- $V_{CE} = V_C - I_E R_E$

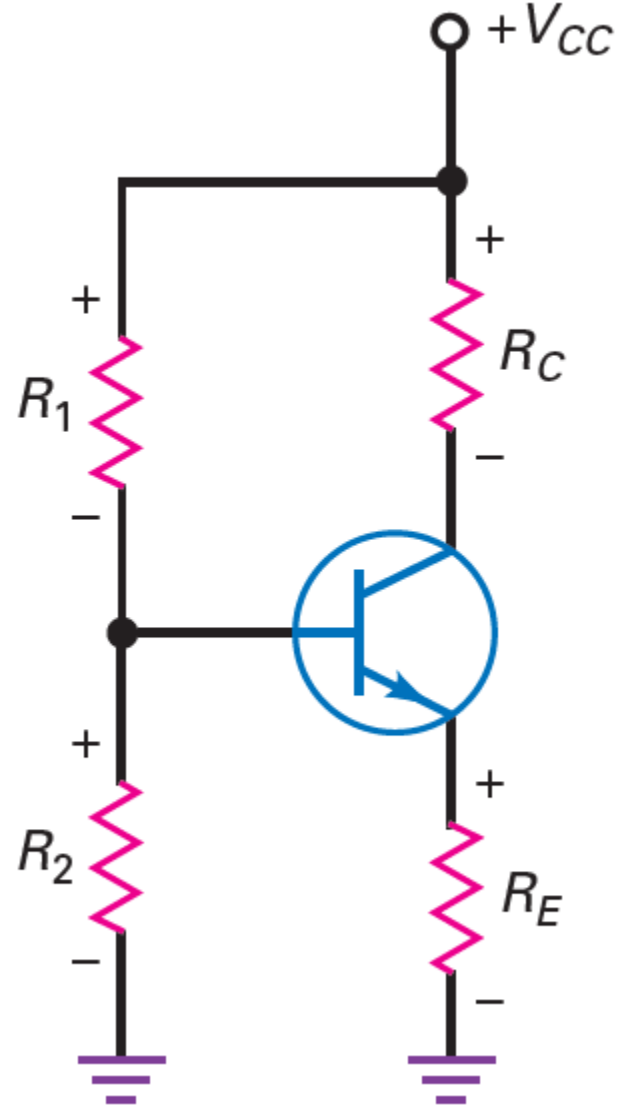




2. Q point(operating point along load line)

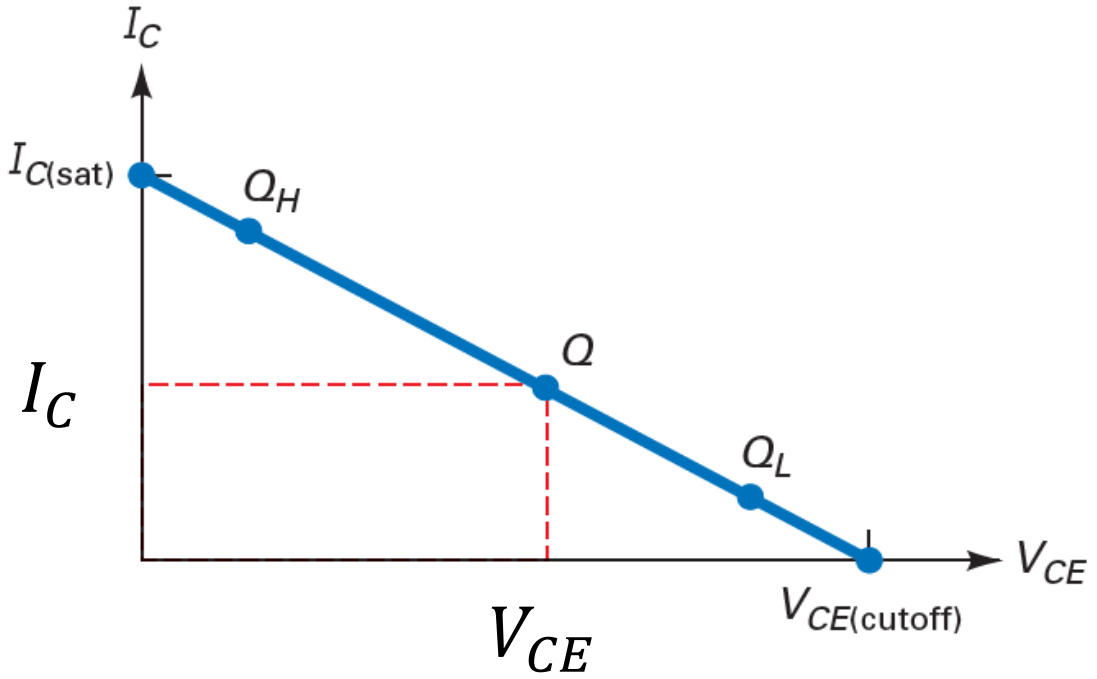
- V_{CC}, R_1, R_2 and R_C control the saturation current and cutoff voltage.

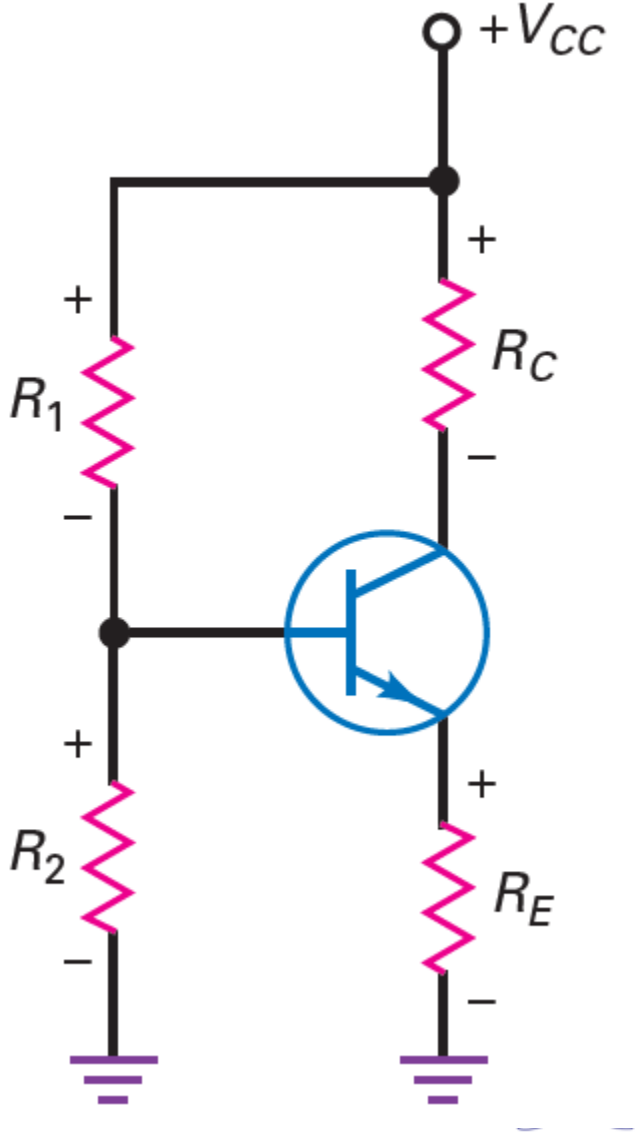




2. Q point(operating point along load line)

- V_{CC}, R_1, R_2 and R_C control the saturation current and cutoff voltage.
- A change in any of the values, results in change in $I_{C(sat)}$ and $V_{CE(cutoff)}$



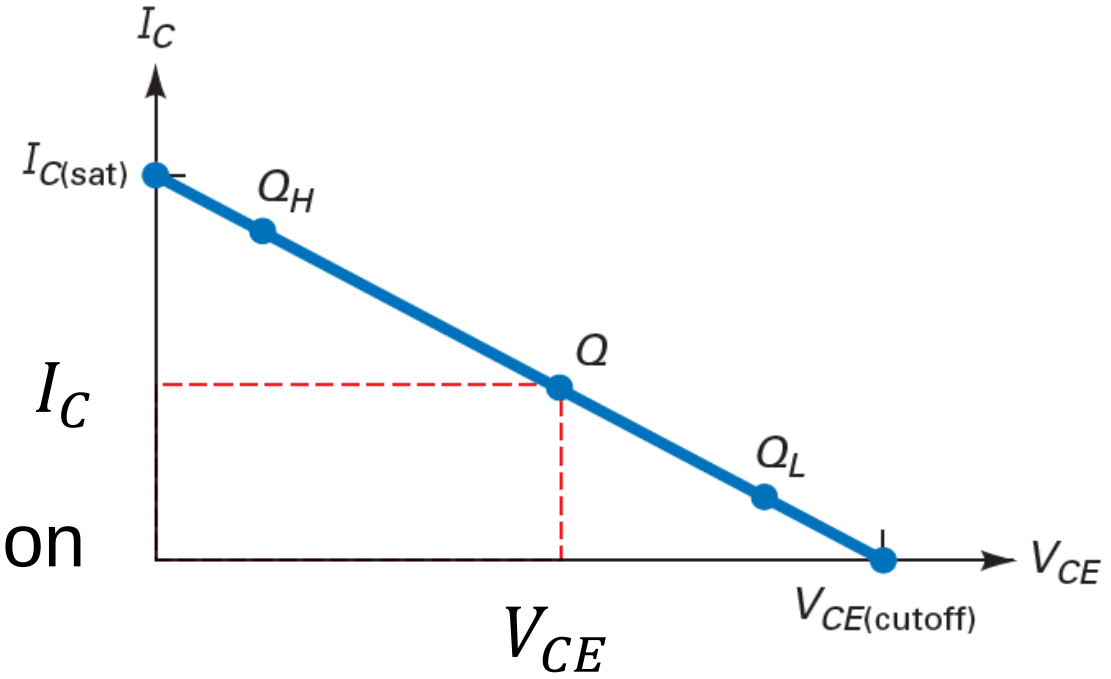


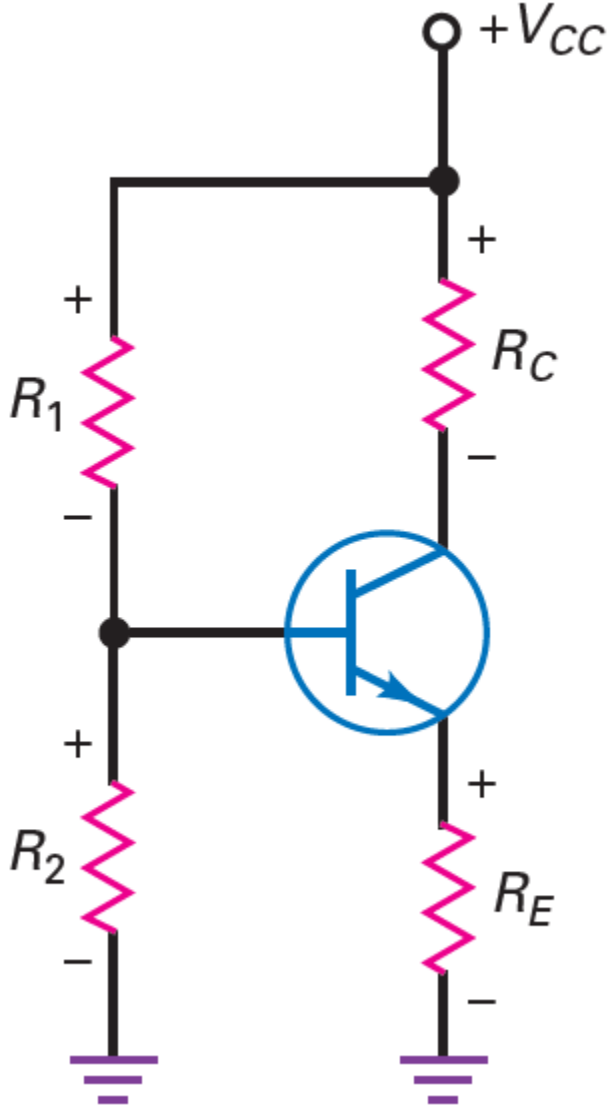
2. Q point(operating point along load line)

- V_{CC}, R_1, R_2 and R_C control the saturation current and cutoff voltage.
- A change in any of the values, results in change in $I_{C(sat)}$ and $V_{CE(cutoff)}$
- $V_{CE} = V_C - I_E R_E$

If R_E is too large.
Q point -> cutoff

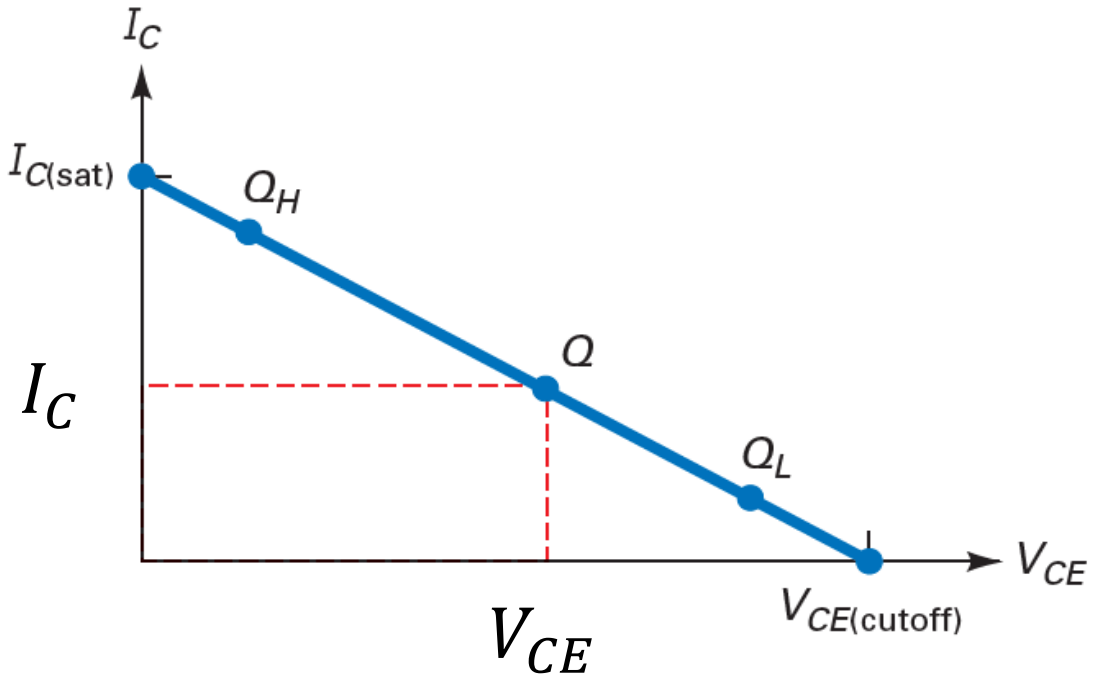
If R_E is too small,
Q point -> saturation

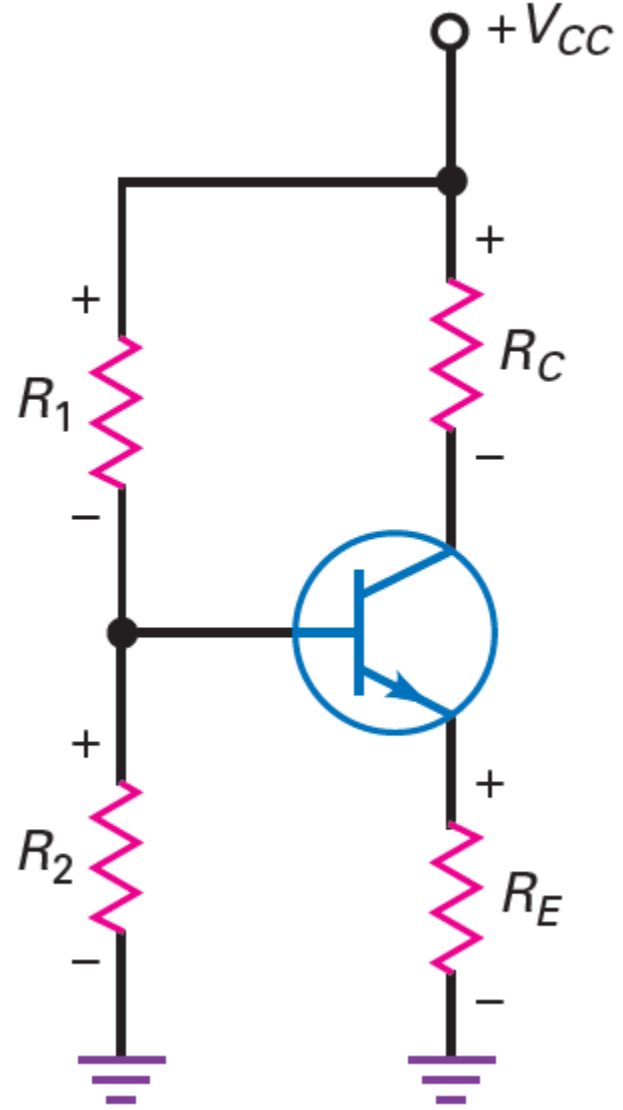




2. Q point(operating point along load line)

- For Maximum output signal, Q point is in middle of the Load line

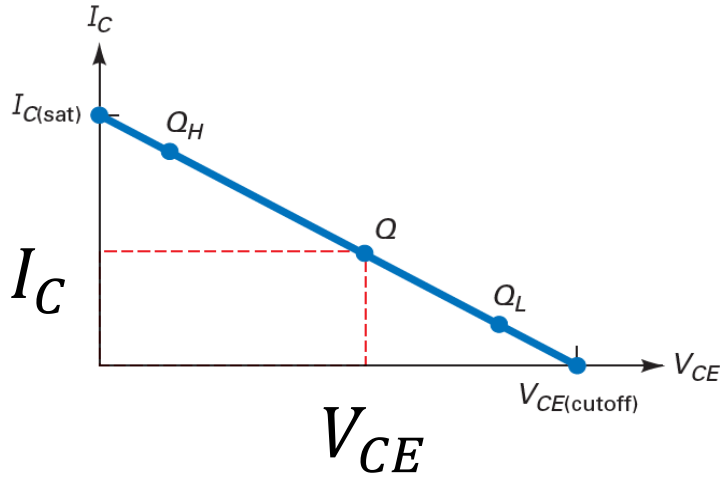


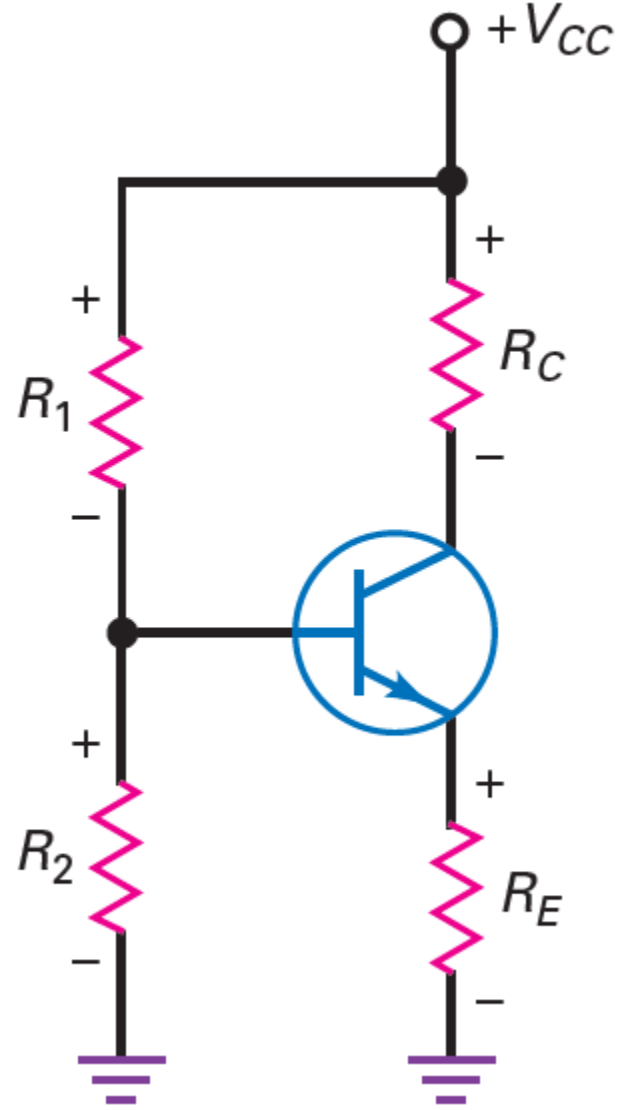


3. Instructions for CE Amplifier design with Voltage Divider Bias

- Circuit is normally biased for V_{CE} to be at midpoint with specified I_C. Follow the steps below:

$1)\ V_E =$



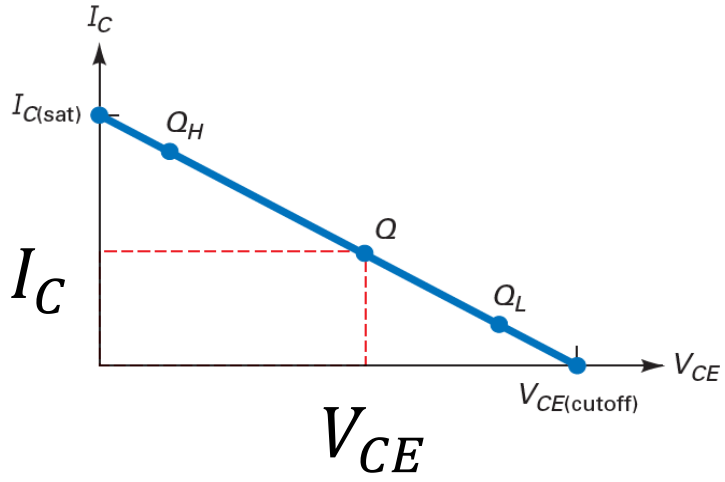


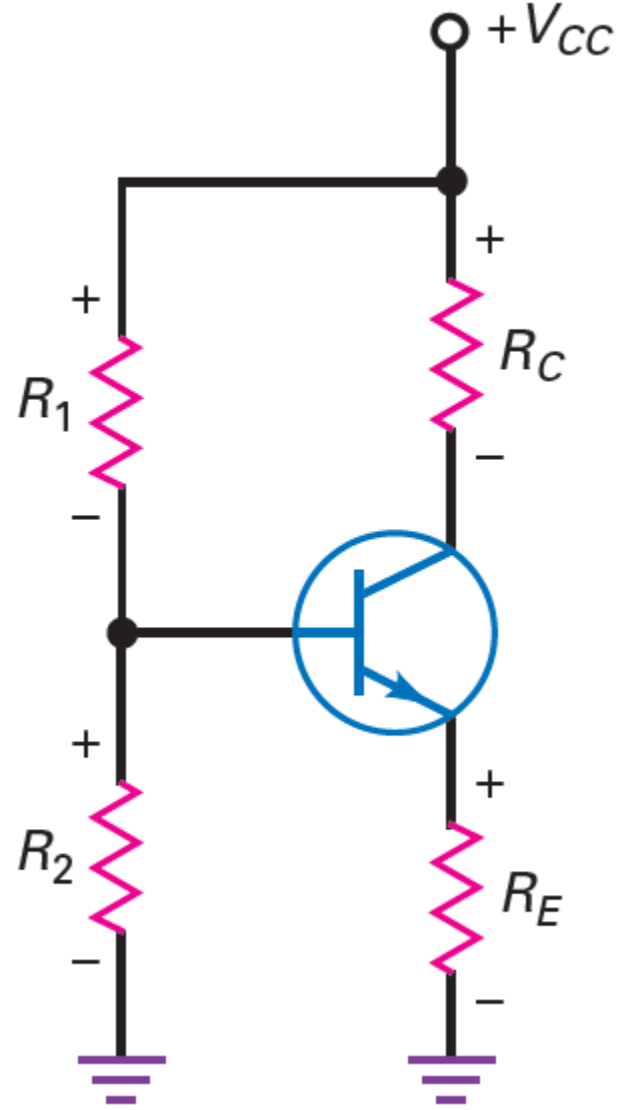
3. Instructions for CE Amplifier design with Voltage Divider Bias

- Circuit is normally biased for V_{CE} to be at midpoint with specified I_C. Follow the steps below:

1) $V_E = 0.1V_{CC}$

2) $R_E = V_E / I_E$





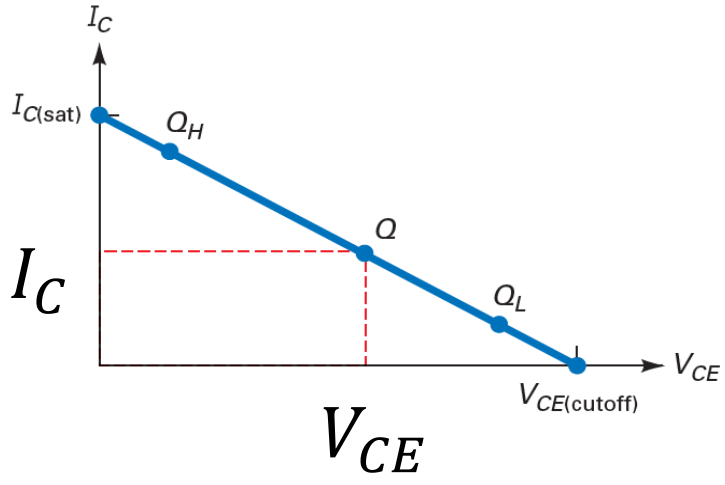
3. Instructions for CE Amplifier design with Voltage Divider Bias

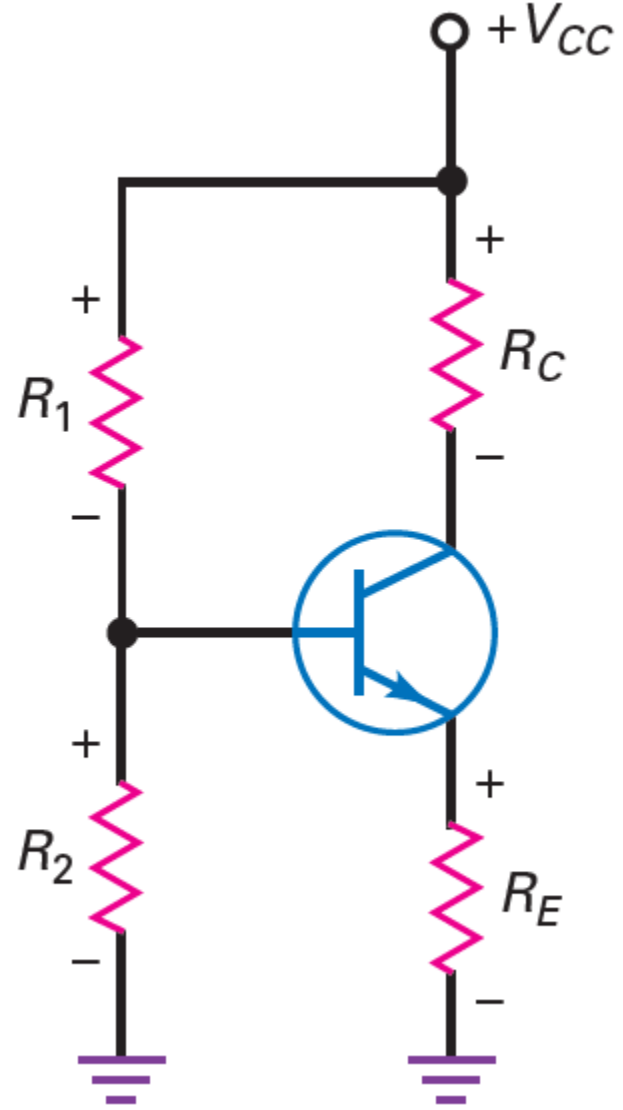
- Circuit is normally biased for V_{CE} to be at midpoint with specified I_C. Follow the steps below:

1) $V_E = 0.1V_{CC}$

2) $R_E = V_E/I_E$

3) For Q point at center, $V_{CE} \approx 0.5V_{CC}$
Remaining voltage across collector: $0.4V_{CC}$
Collector resistance: $\mathrm{R}_C = 0.4V_{CC}/I_C \quad (I_C \approx I_E)$





3. Instructions for CE Amplifier design with Voltage Divider Bias

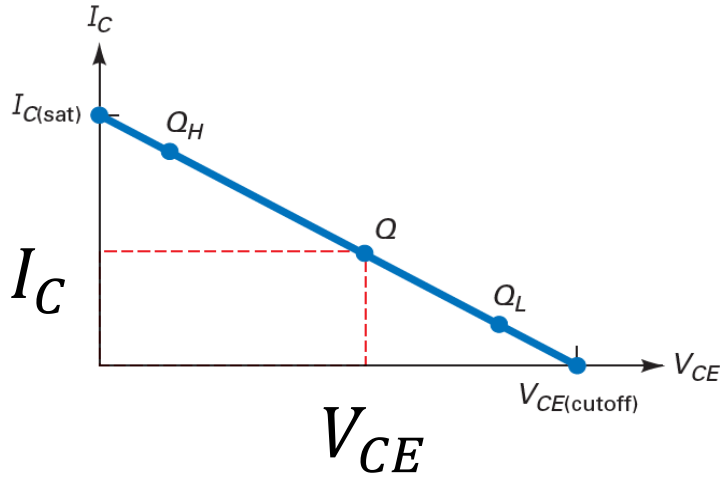
- Circuit is normally biased for V_{CE} to be at midpoint with specified I_C. Follow the steps below:

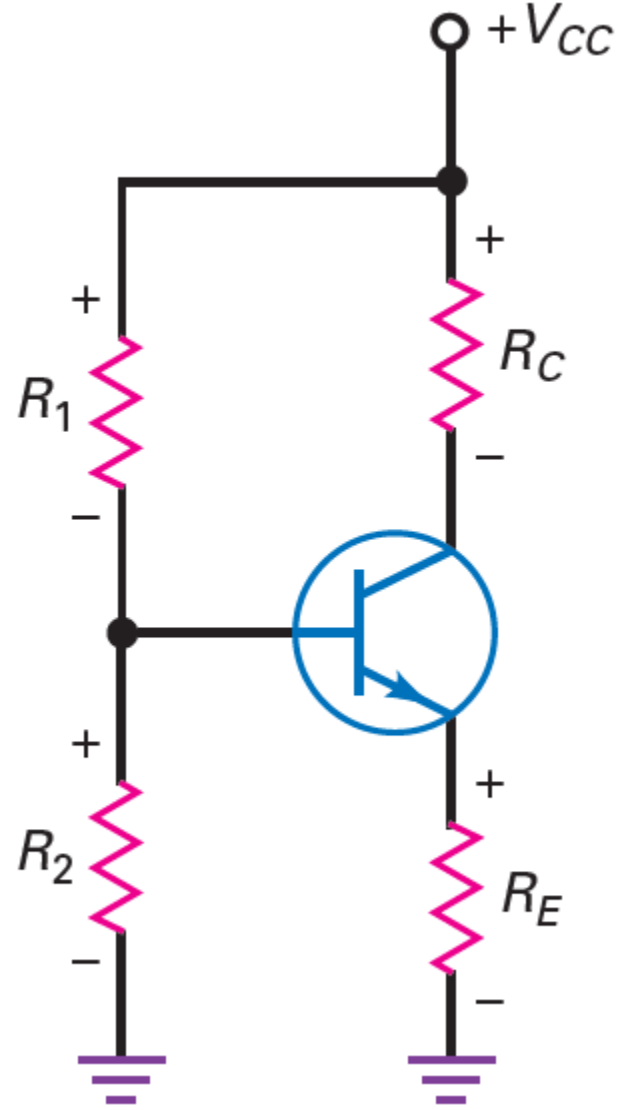
1) $V_E = 0.1V_{CC}$

2) $R_E = V_E/I_E$

3) $\mathrm{R}_C = 0.4V_{CC}/I_C \quad (I_C \approx I_E)$

4) Stiff voltage divider:
$R_2 \leq 0.01\,\beta_{dc}R_E$
Firm voltage divider:
$R_2 \leq 0.1\,\beta_{dc}R_E$ Where β_{dc}: minimum of range
Note: $\beta_{dc}\ is\ current\ gain$: I_C/I_B and is provided by manufacturer





3. Instructions for CE Amplifier design with Voltage Divider Bias

- Circuit is normally biased for V_{CE} to be at midpoint with specified I_C. Follow the steps below:

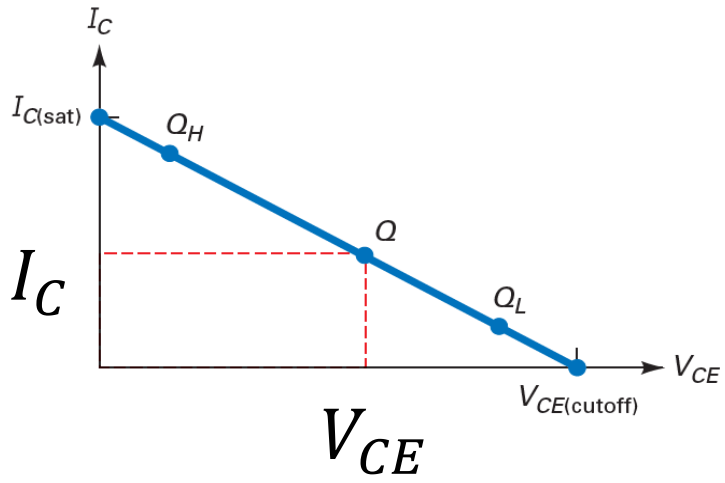
1) $V_E = 0.1V_{CC}$

2) $R_E = V_E / I_E$

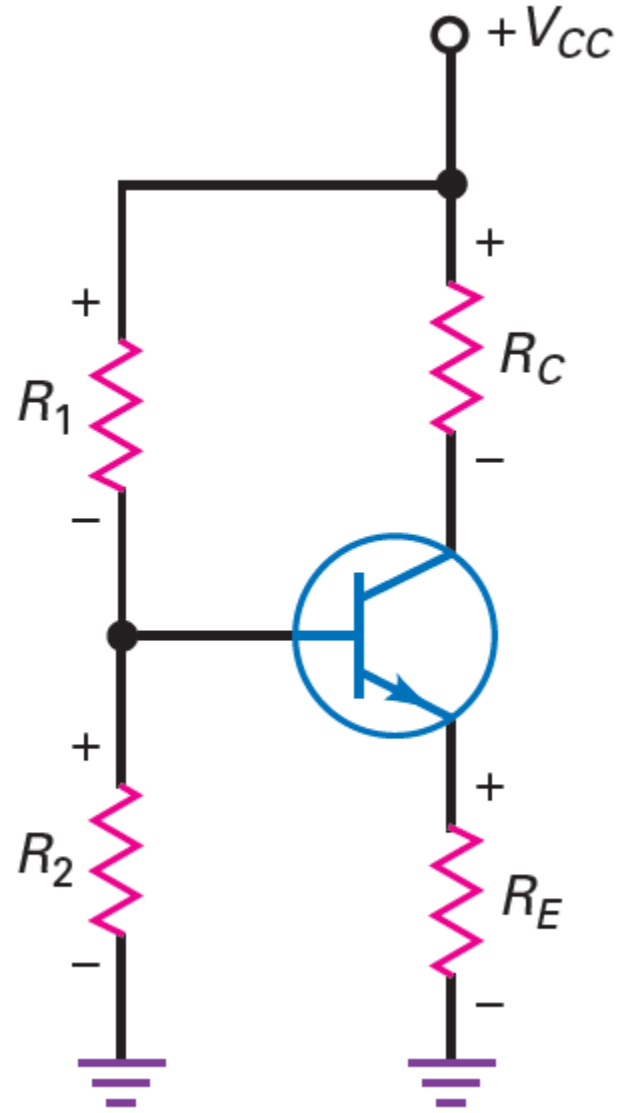
3) $\mathrm{R}_C = 0.4V_{CC}/I_C \quad (I_C \approx I_E)$

4) Stiff voltage divider:
$R_2 \leq 0.01\,\beta_{dc}R_E$
Firm voltage divider:
$R_2 \leq 0.1\,\beta_{dc}R_E$

5) $R_1 = \frac{V_1}{V_2}R_2$



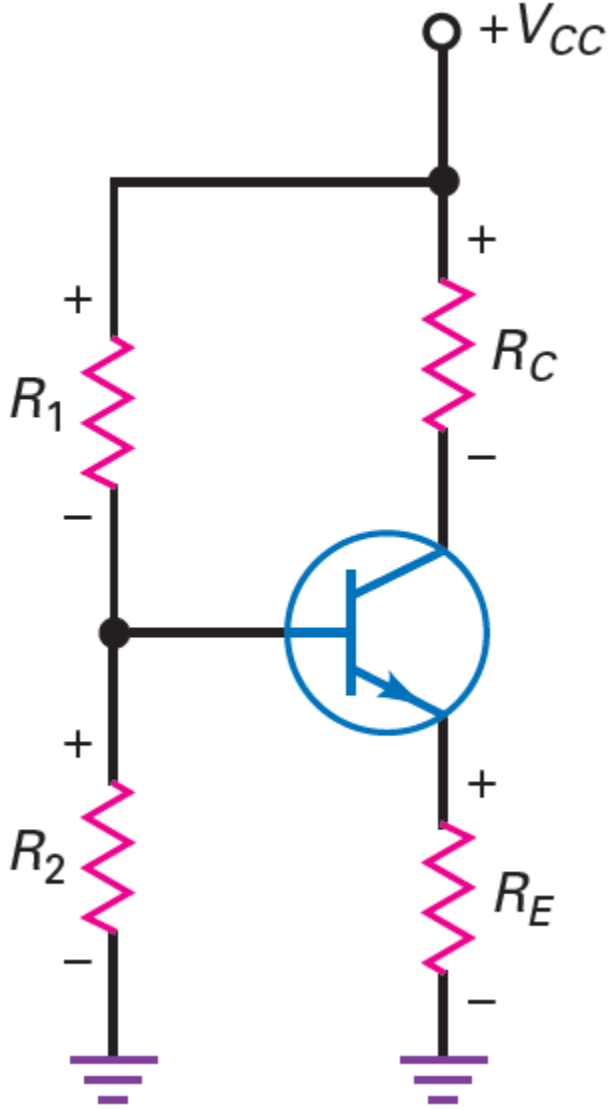
Where β_{dc}: minimum of range



4. Task 1.1: Stiff voltage divider

- **<u>Design the VDB circuit for Stiff Voltage divider</u>**
  $V_{CC} = 10V$, V_{CE} at midpoint
  $I_C = 10mA$
  Transistor: 2N3904's $\beta_{dc} = 100 - 300$

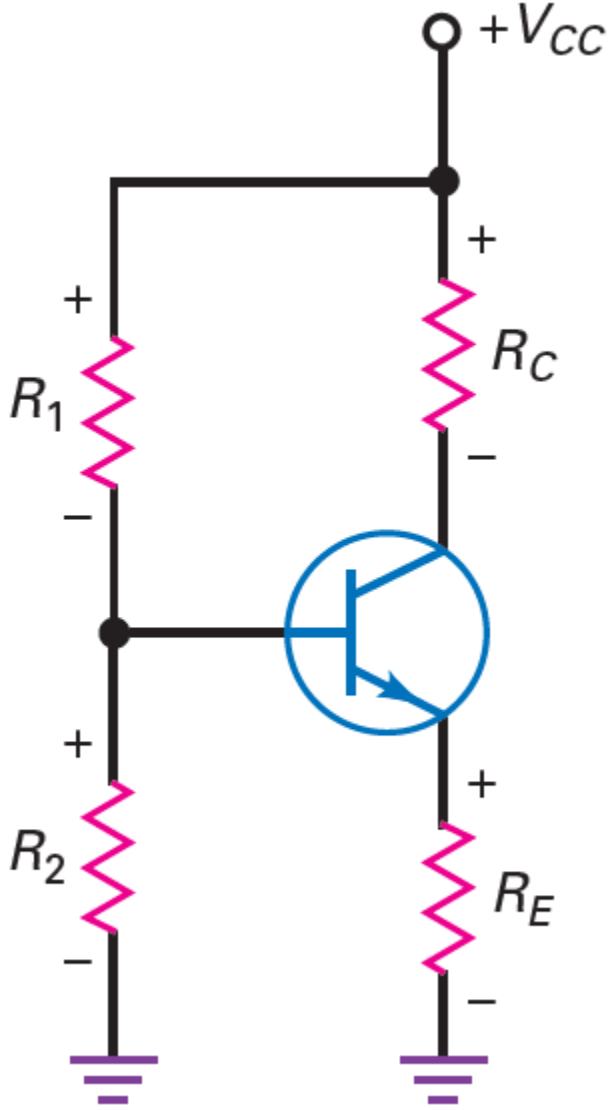
Find all the resistor values and write it down.
Note: For this task, No need to simulate in LT Spice.



4. Task 1.2: Firm Voltage divider

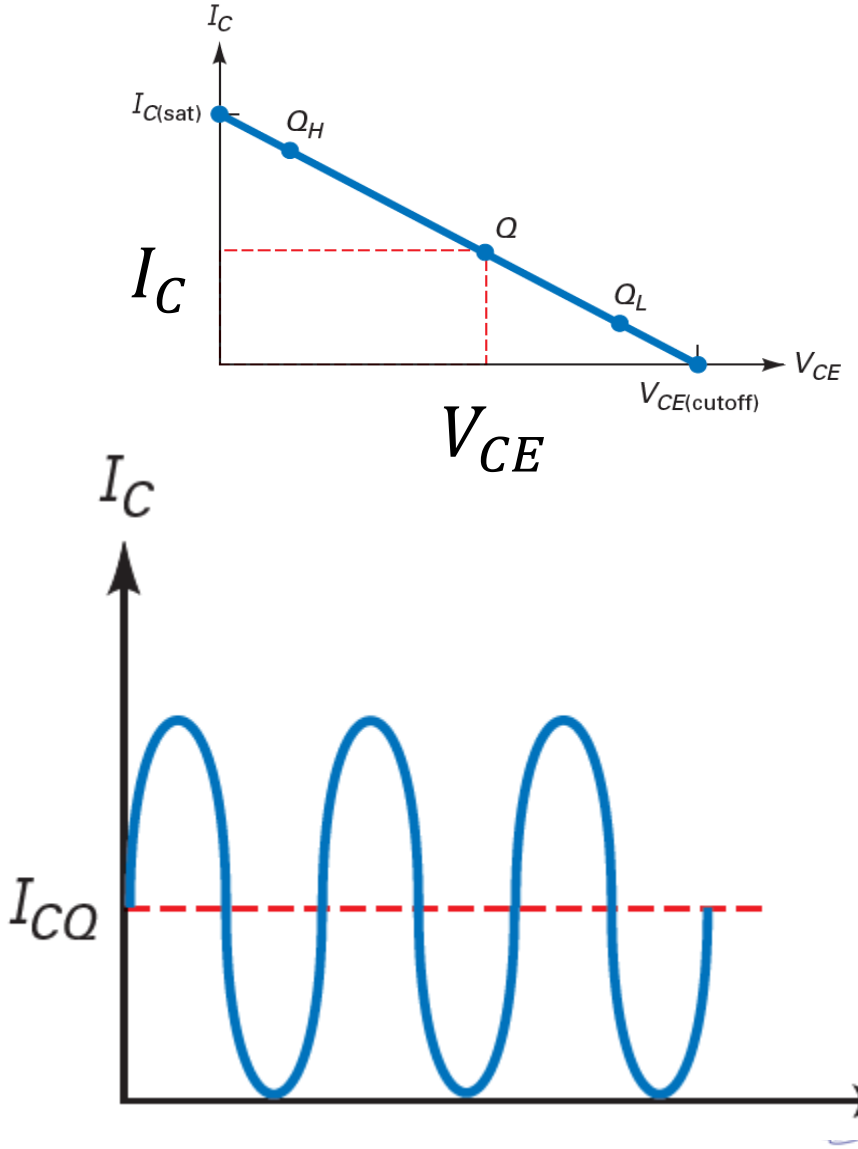
- **<u>Design the VDB circuit for Firm Voltage divider</u>**
  $V_{CC} = 10V$, V_{CE} at midpoint
  $I_C = 10mA$
  Transistor: 2N3904's $\beta_{dc} = 100 - 300$

Find all the resistor values and write it down.
Note: For this task, No need to simulate in LT Spice.



5. Amplifier types

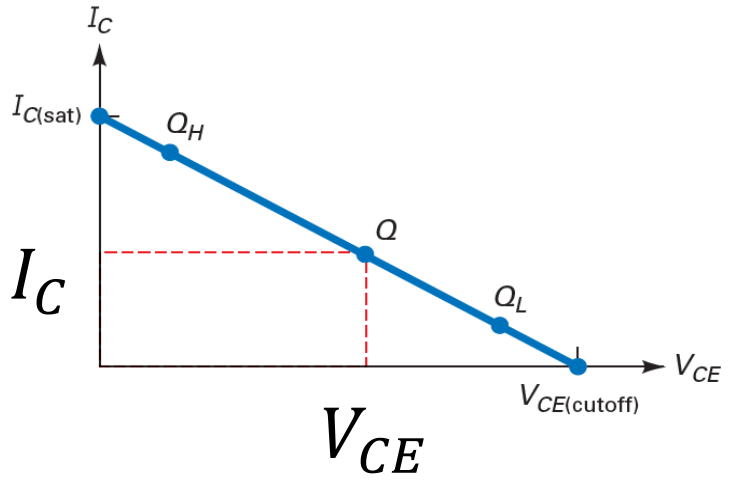
- **Class A operation**: the transistor operates in the active region at all times. This implies that collector current flows for 360° of the ac cycle.
  With a Class-A amplifier, the designer usually tries to locate the *Q* point somewhere near the middle of the load line.
- This way, the signal can swing over the maximum possible range without saturating or cutting off the transistor, which would distort the signal.

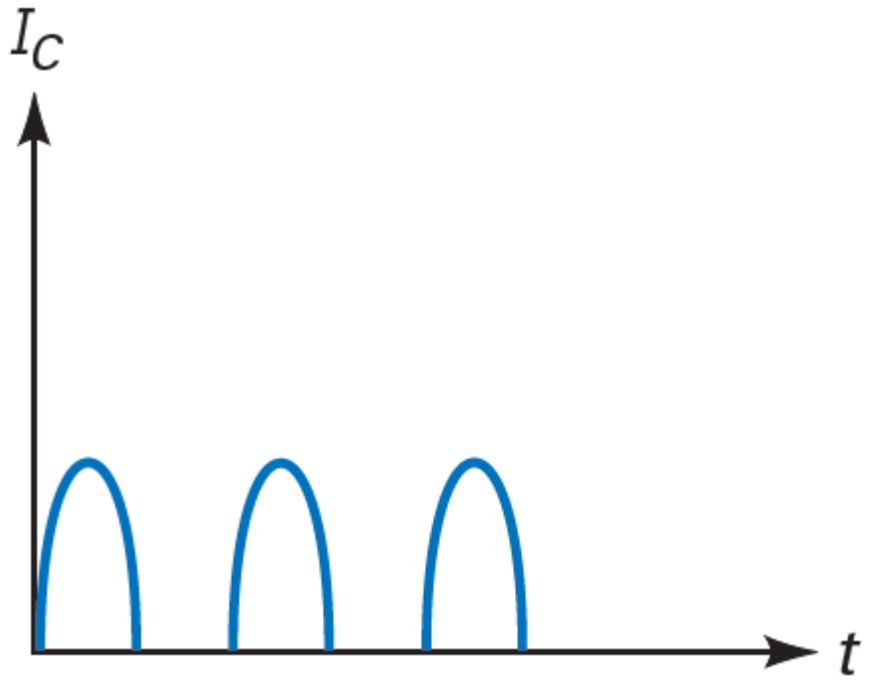


5. Amplifier types

Class-B operation

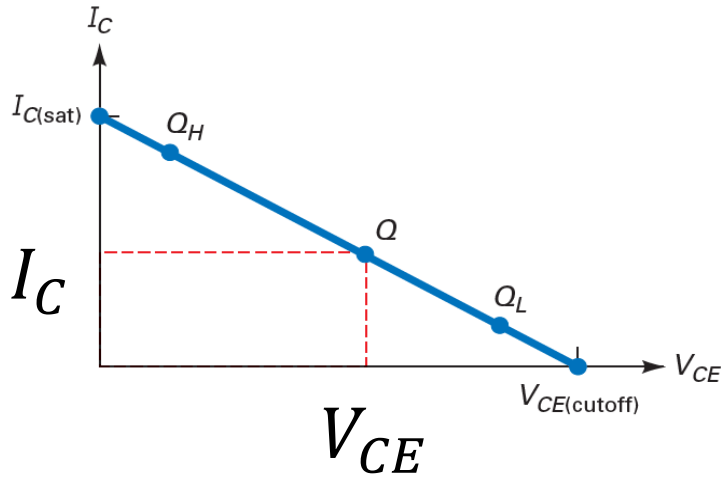
- It means that collector current flows for only half the cycle (180°).
- To have this kind of operation, a designer locates the *Q* point at cutoff.
- Then, only the positive half-cycle of ac base voltage can produce collector current. This reduces the wasted heat in power transistors.

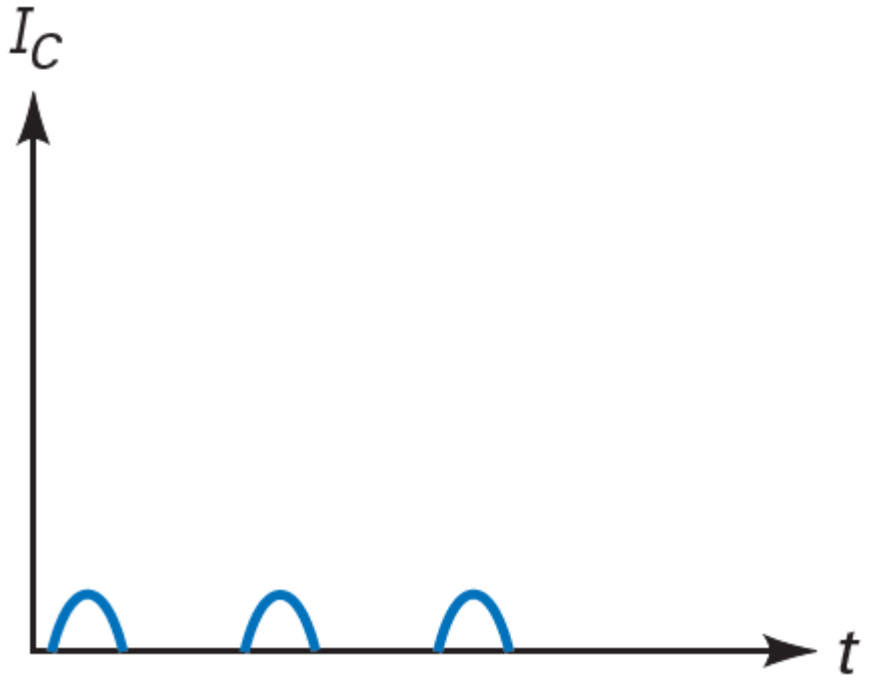




5. Amplifier types

- **Class-C operation** means that collector current flows for less than 180° of the ac cycle.
- With Class-C operation, only part of the positive half-cycle of ac base voltage produces collector current.



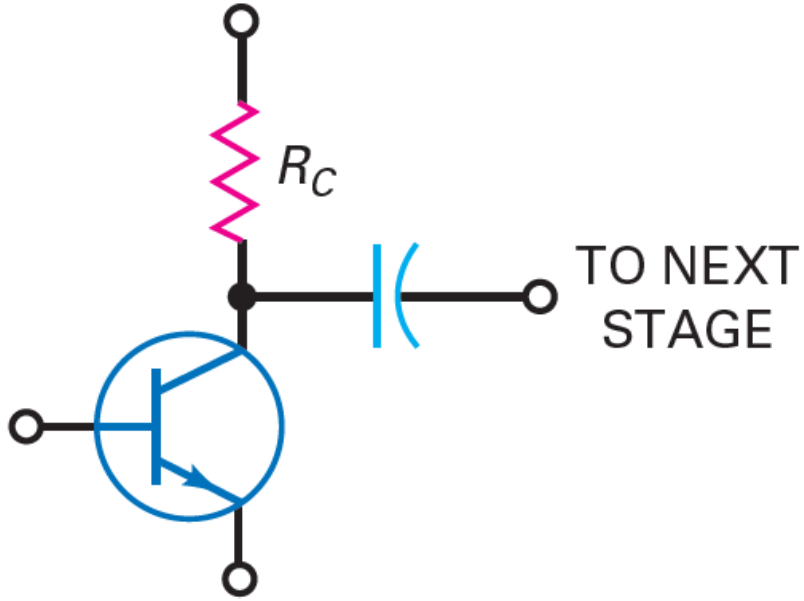


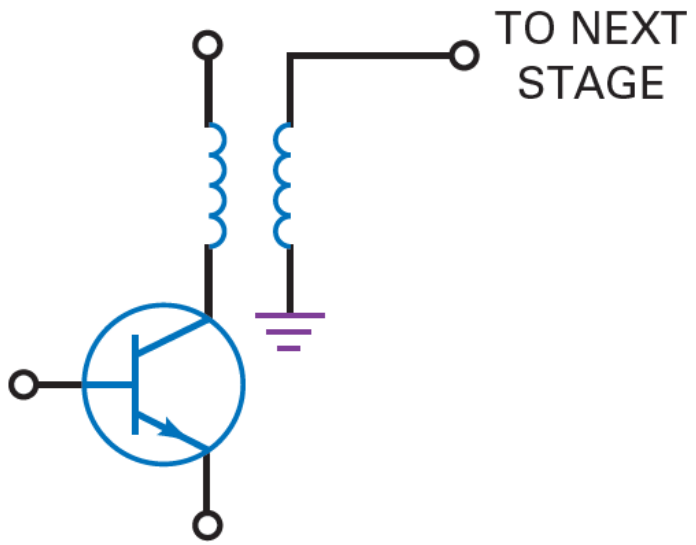
6. Types of Coupling

Transmits ac voltage to next stage

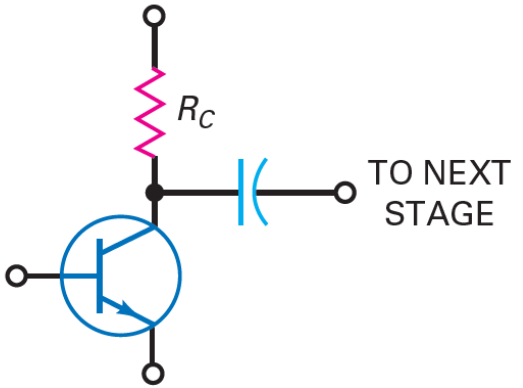
a) Capacitive coupling

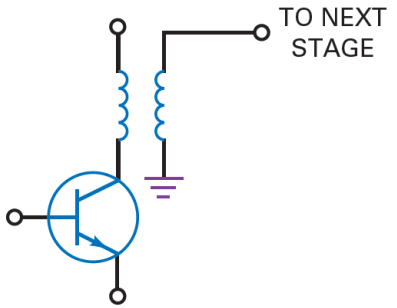
b) Inductive coupling





6. Types of Coupling





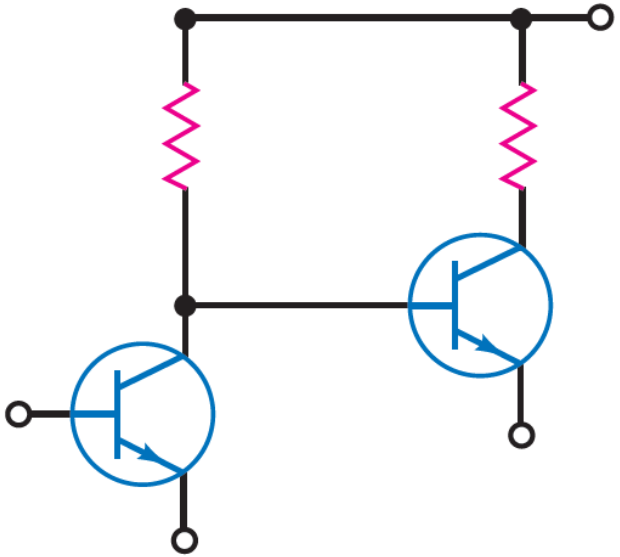
Transmits ac voltage to next stage

a) Capacitive coupling

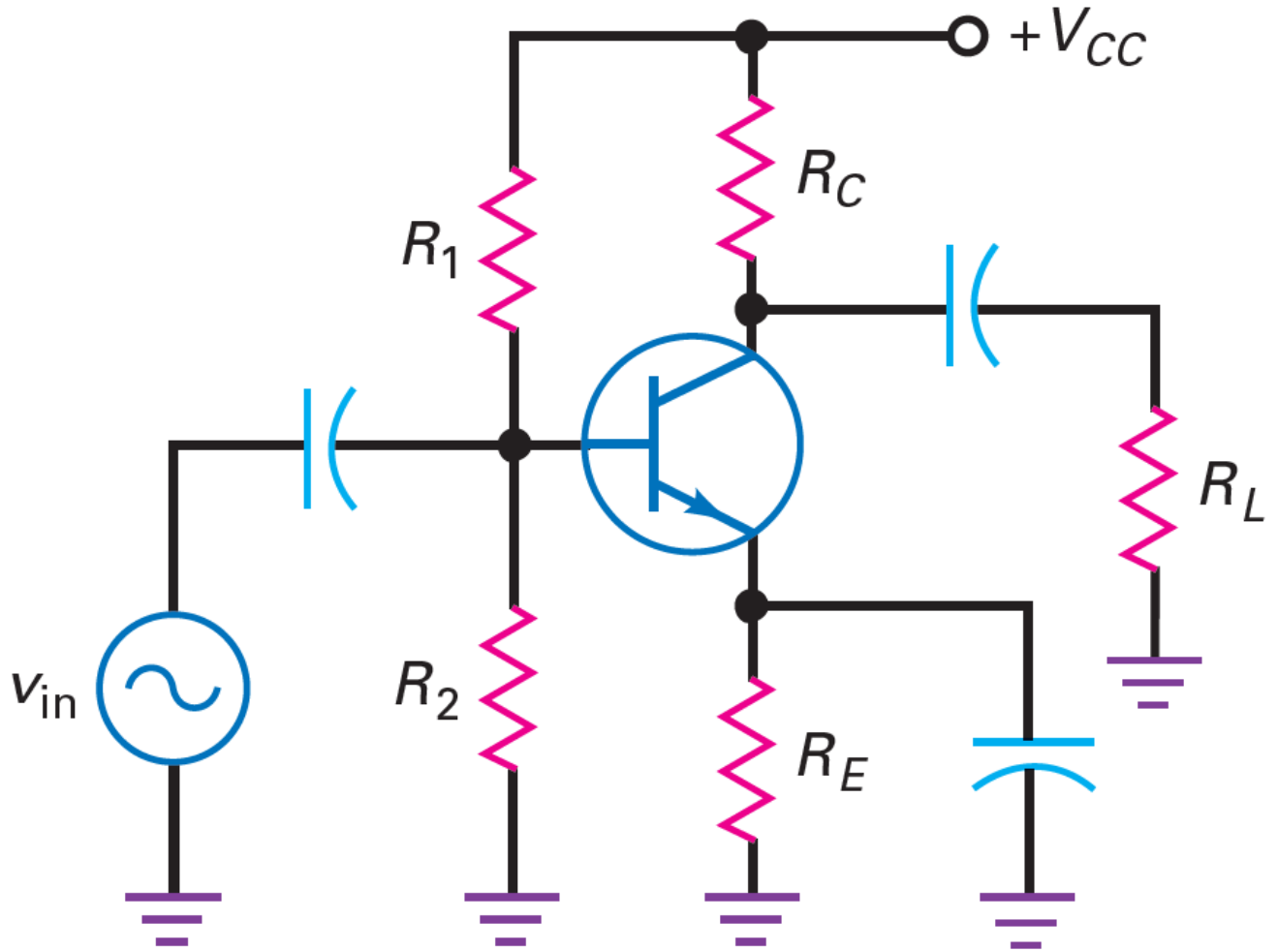
b) Inductive coupling

To transmit both ac and dc:

a) Direct coupling

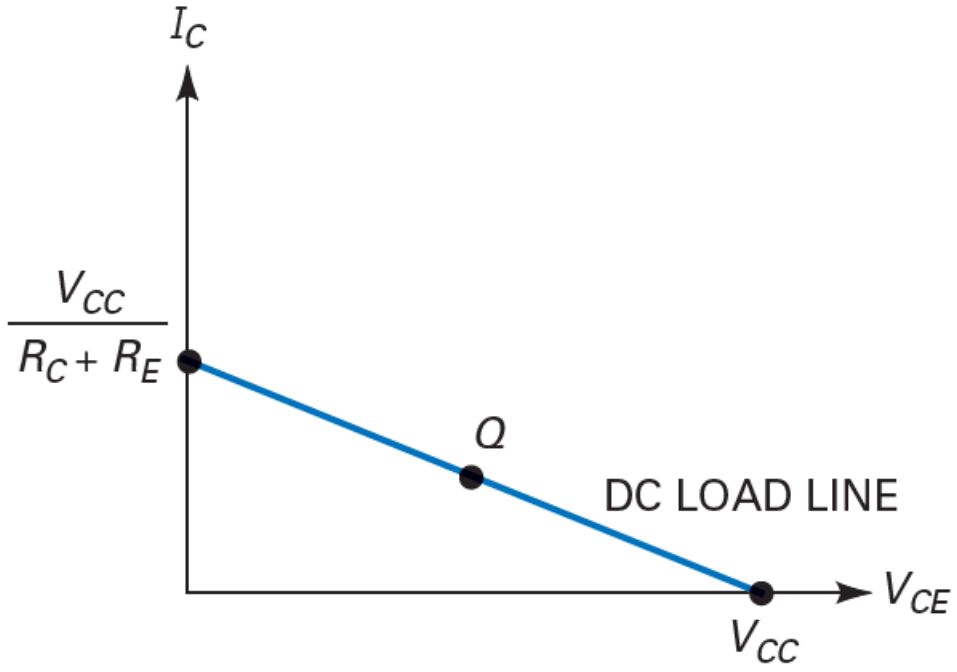


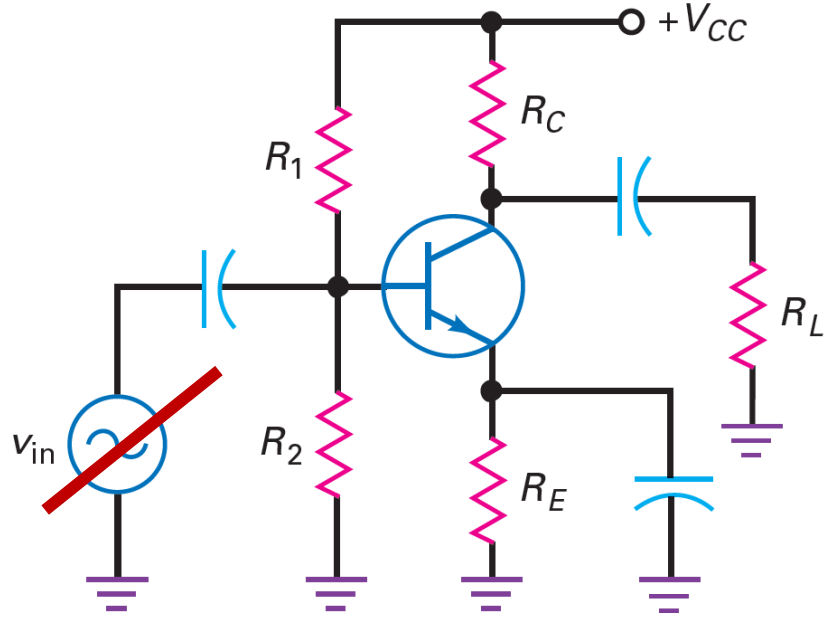
7. VDB amplifier



7. VDB amplifier: DC load line

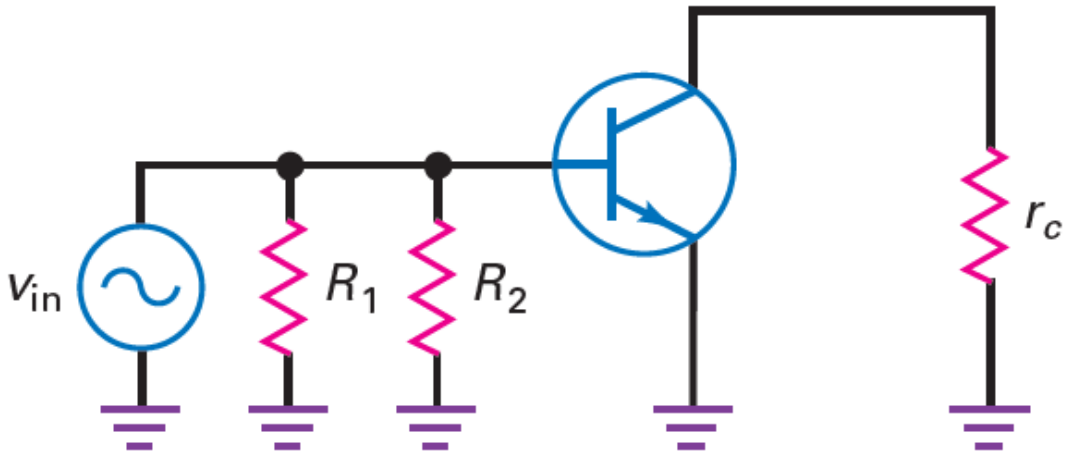
- **DC Load line**: When **no ac input**:
  Connect points $V_{CE} = V_{CC}$ (Cutoff – Open transistor)
  and
  $I_C = \frac{V_{CC}}{R_C + R_E}$ (Saturation – Short transistor)

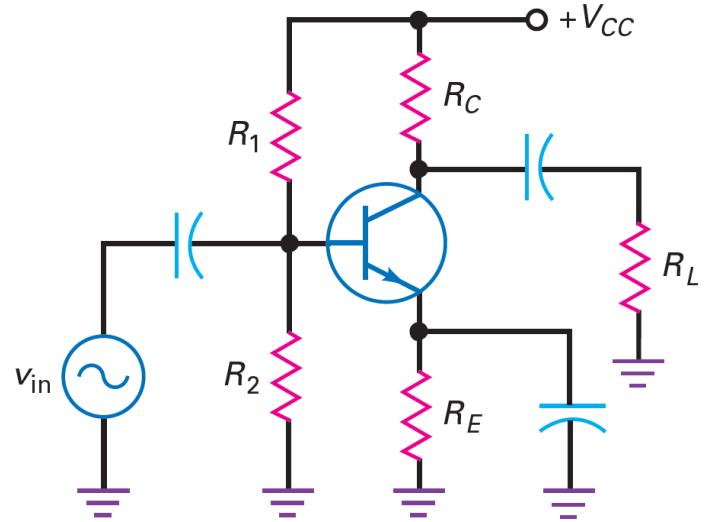


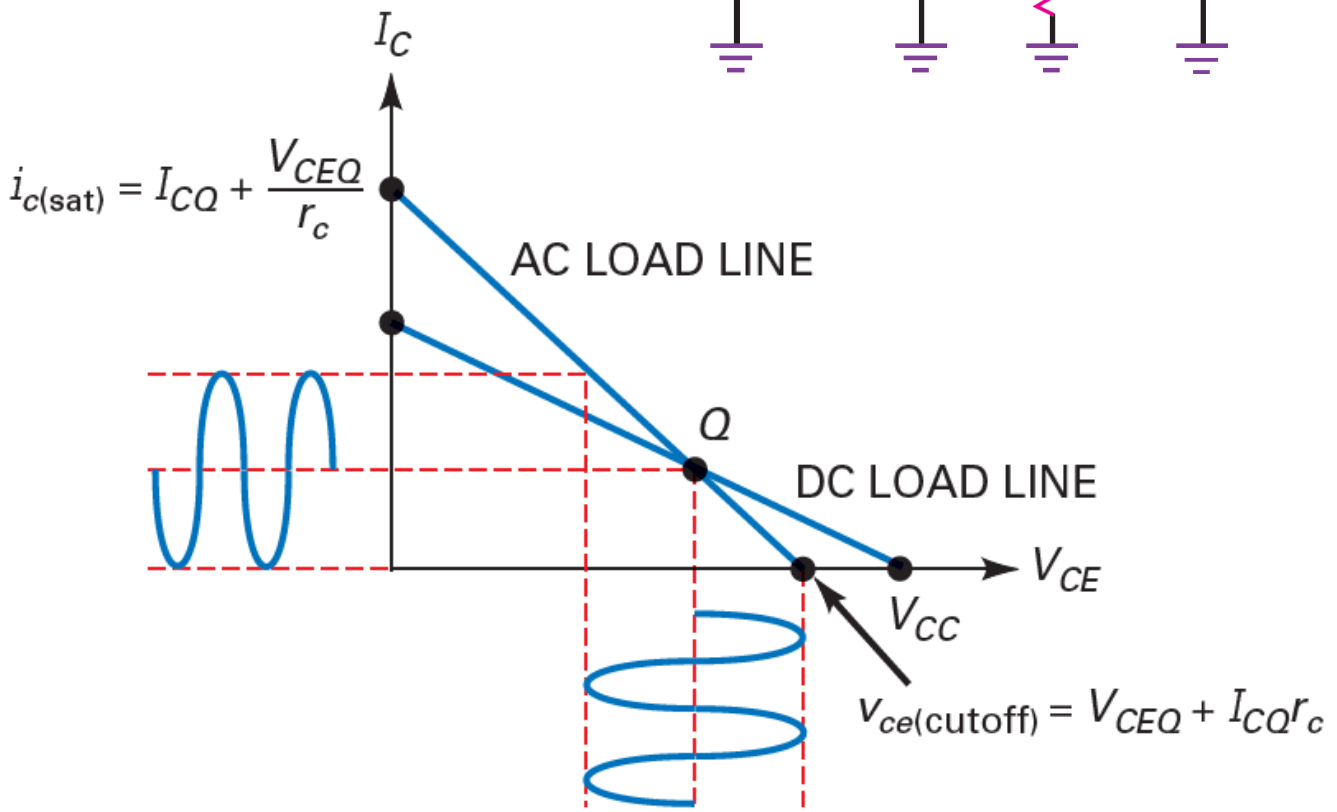


7. VDB amplifier: AC load line

- AC equivalent and AC Load line:
  In the presence of ac.

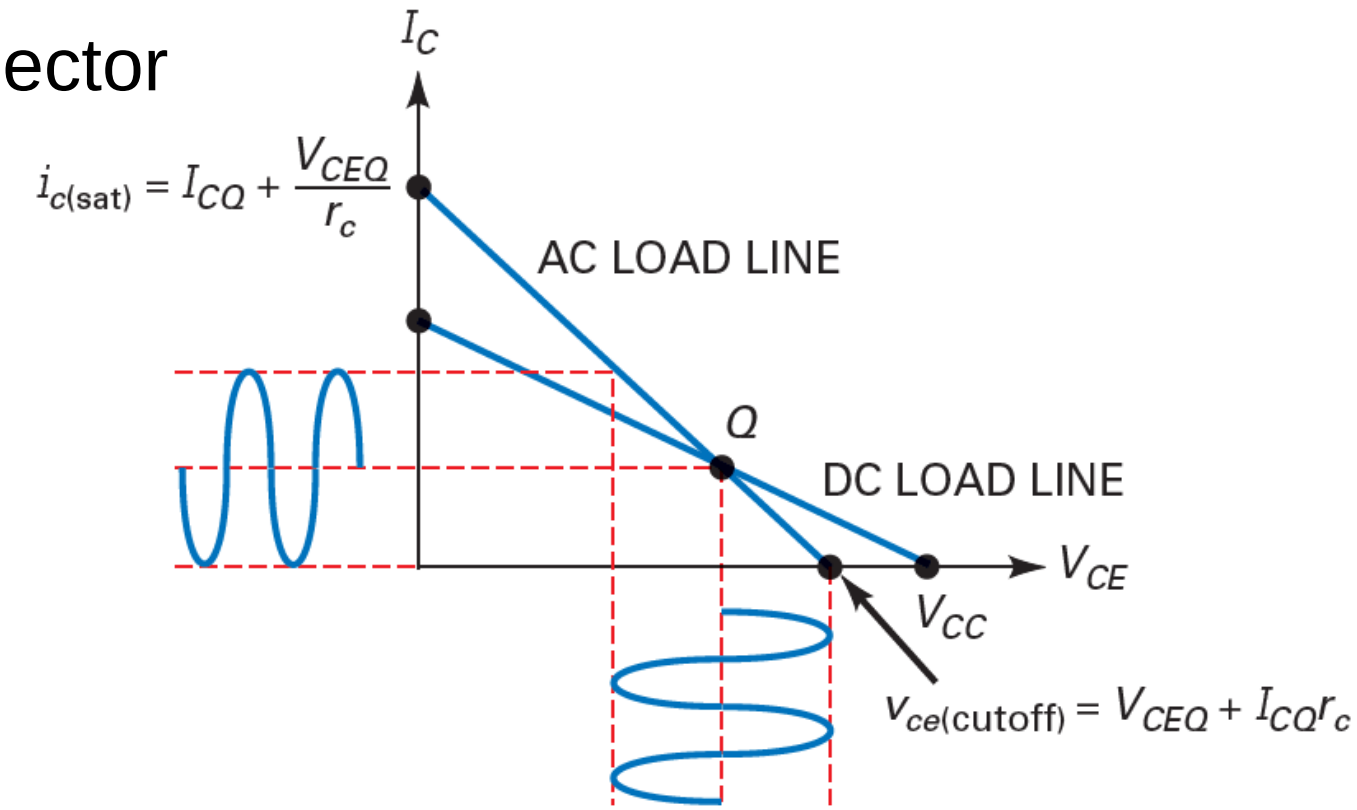






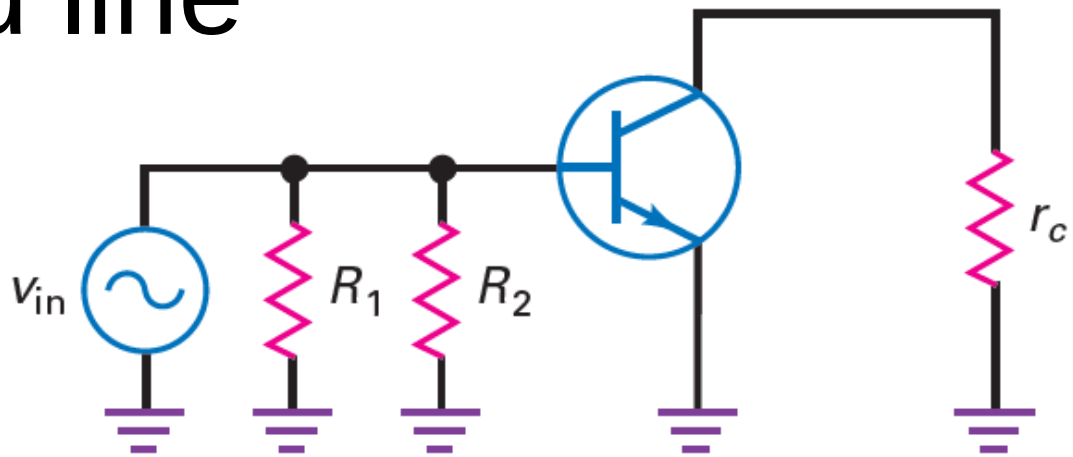
7. VDB amplifier: AC load line

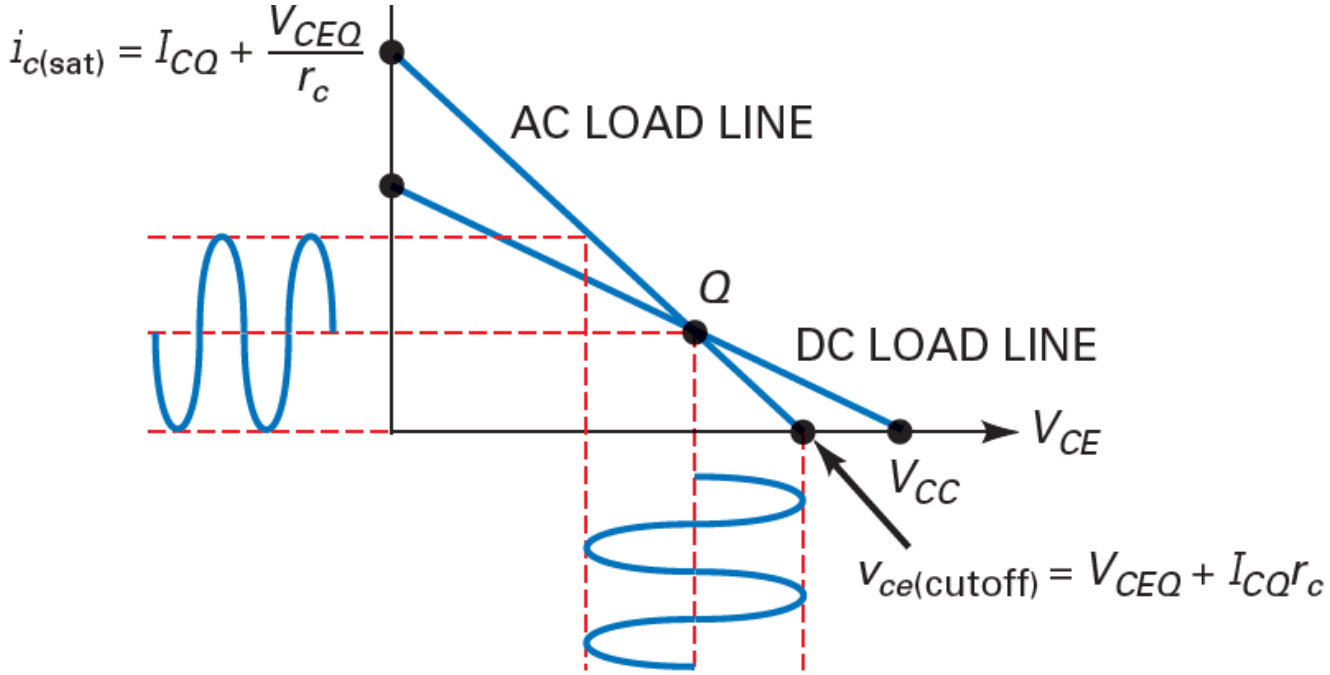
- I_{CQ} =dc collector current
- V_{CEQ} = dc collector-emitter voltage
- r_c =ac resistance seen by collector



7. VDB amplifier: AC load line

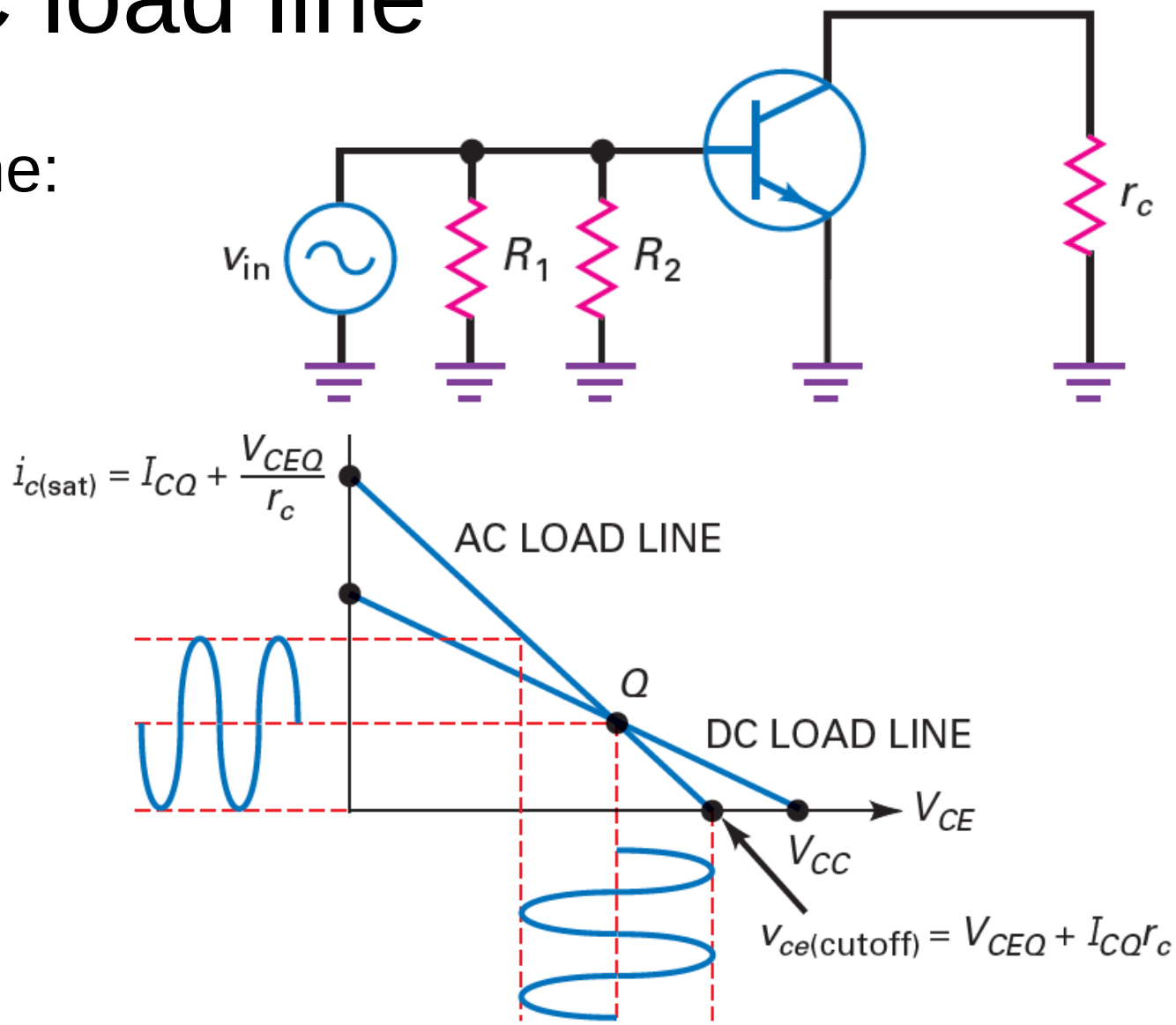
- AC equivalent and AC Load line:
  In the presence of ac.
-





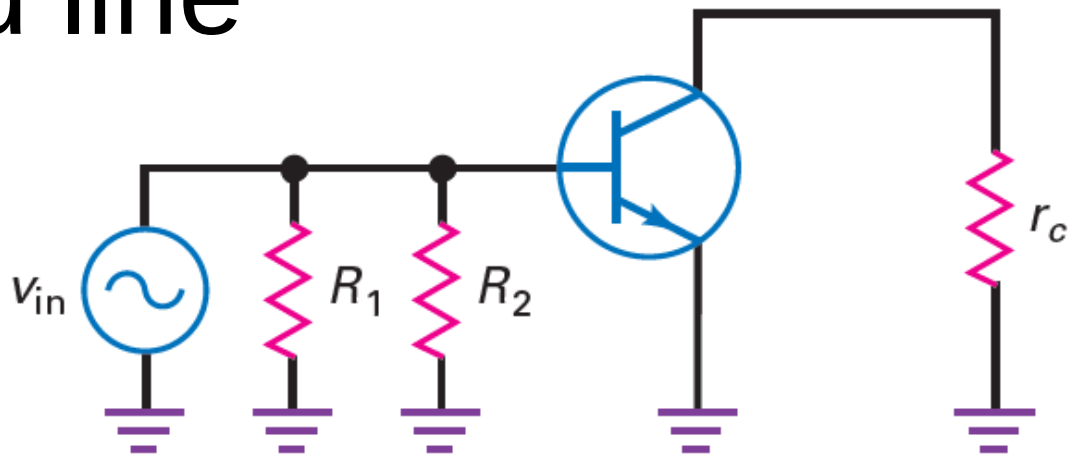
7. VDB amplifier: AC load line

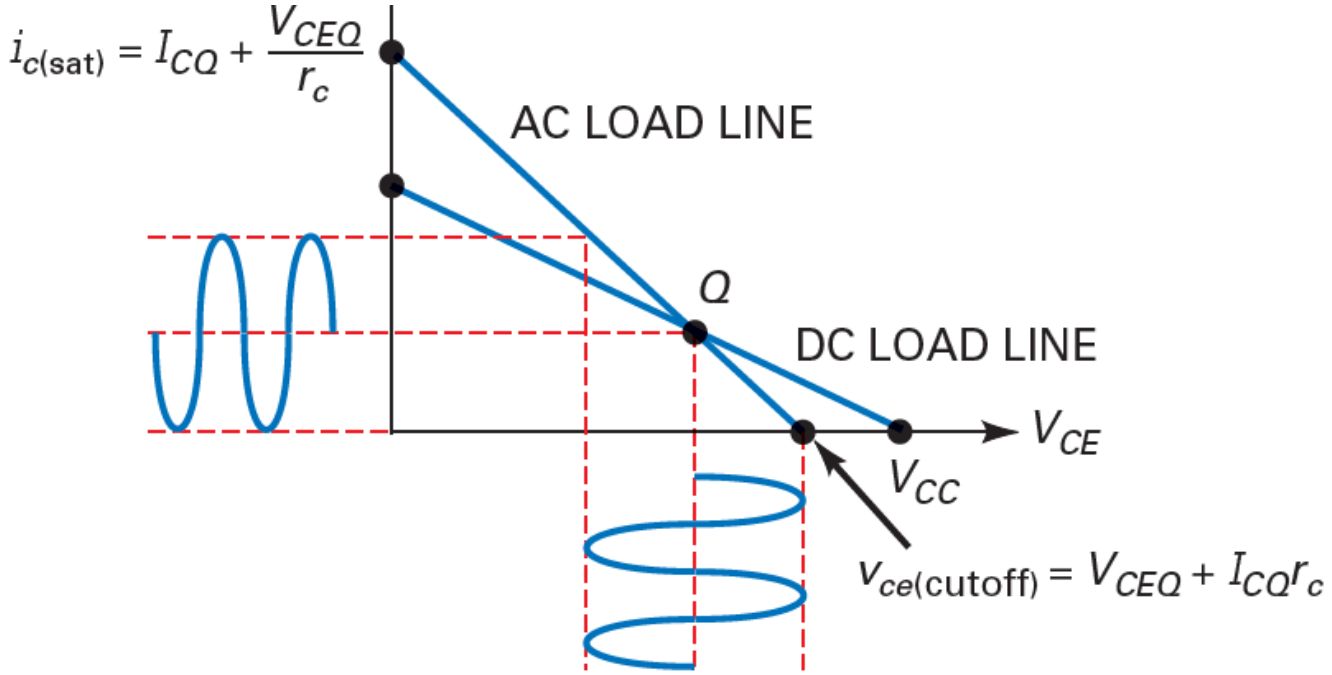
- AC equivalent and AC Load line:
  In the presence of ac.
- Ac Collector current
  $i_c = \Delta I_C = I_C - I_{CQ}$
- Ac Collector voltage:
  $v_{ce} = \Delta V_{CE} = V_{CE} - V_{CEQ}$



7. VDB amplifier: AC load line

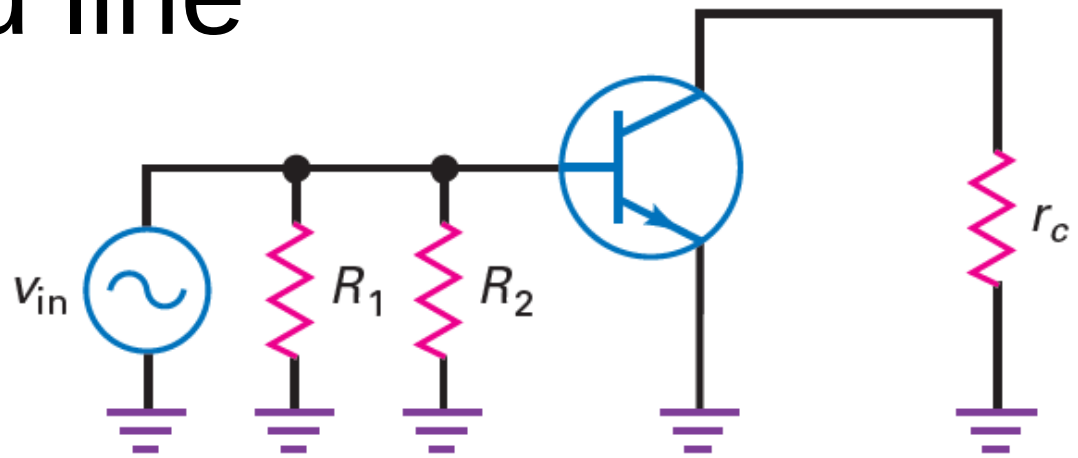
- AC equivalent and AC Load line:
  In the presence of ac.
- Ac Collector current
  $i_c = \Delta I_C = I_C - I_{CQ}$
- Ac Collector voltage:
  $v_{ce} = \Delta V_{CE} = V_{CE} - V_{CEQ}$
- $v_{ce} + i_C r_c = 0$
  $i_c = -v_{ce}/r_c$

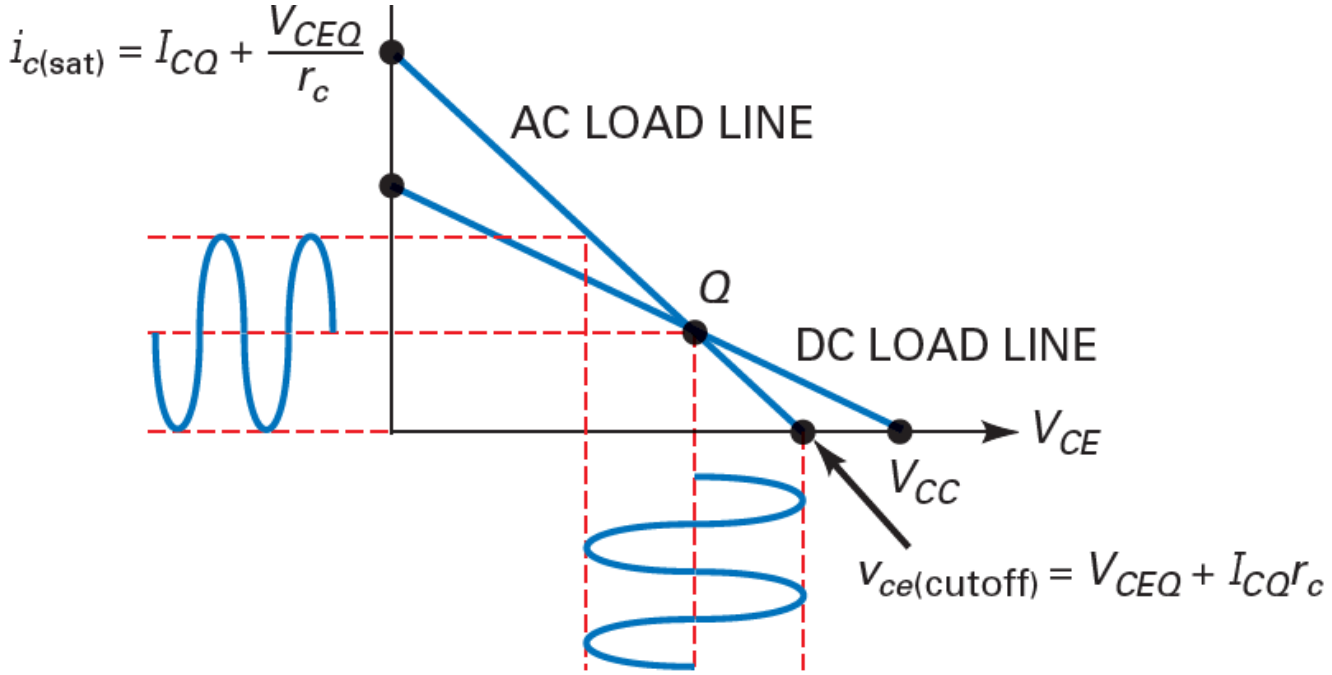




7. VDB amplifier: AC load line

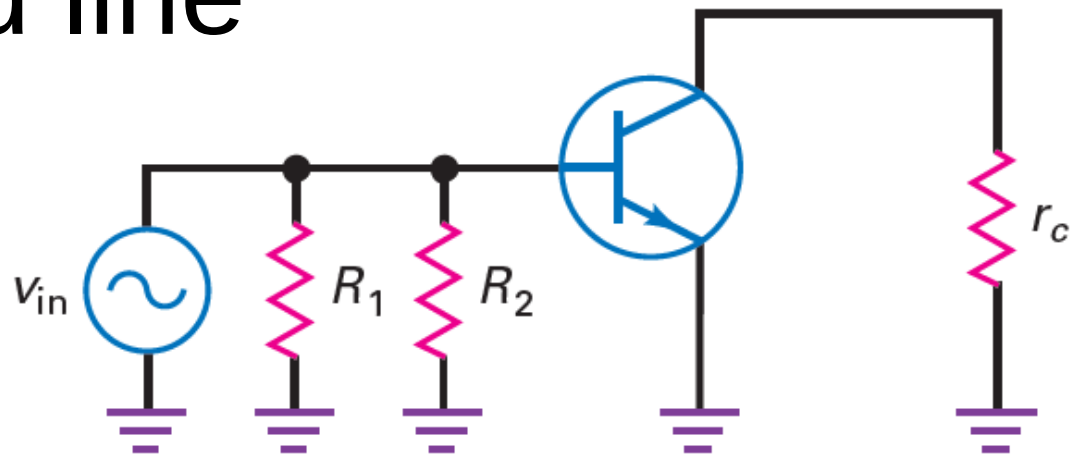
- AC equivalent and AC Load line:
  In the presence of ac.
- Ac Collector current
  $i_c = \Delta I_C = I_C - I_{CQ}$
- Ac Collector voltage:
  $v_{ce} = \Delta V_{CE} = V_{CE} - V_{CEQ}$
- $v_{ce} + i_C r_c = 0$
  $i_c = -v_{ce}/r_c$
- $I_C = I_{CQ} - \frac{V_{CE}}{r_c} + \frac{V_{CEQ}}{r_C}$

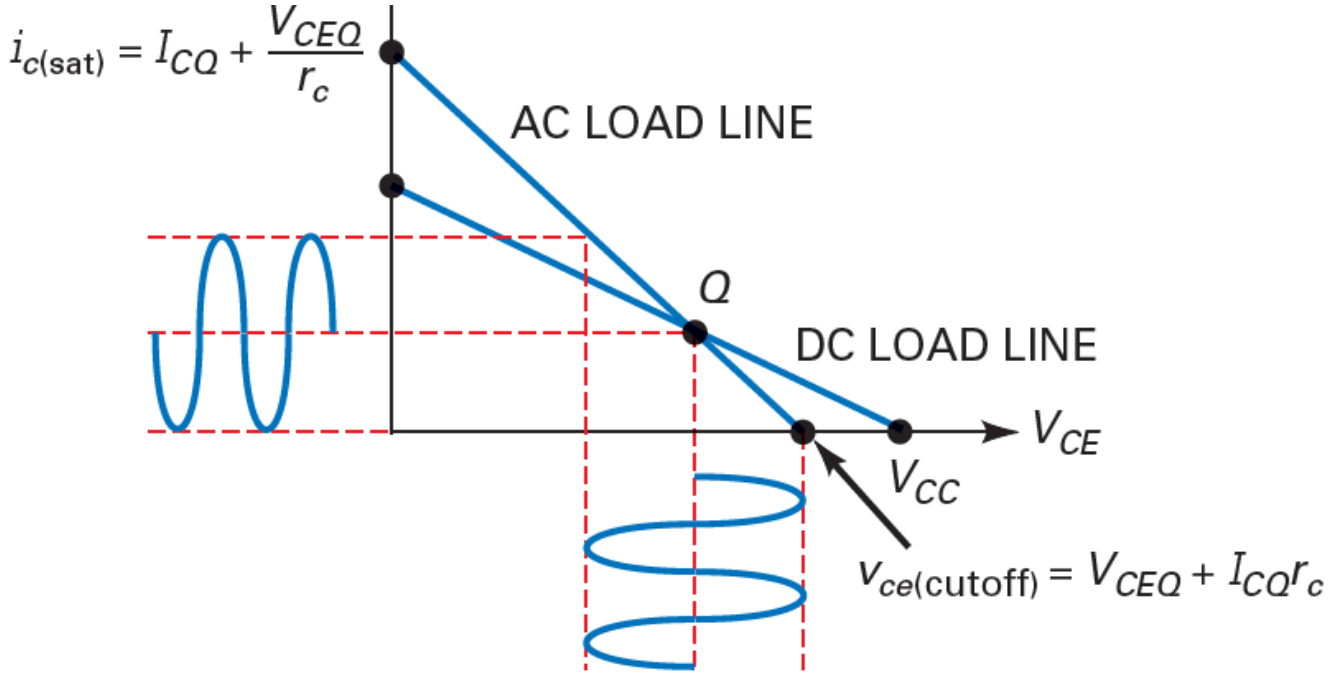




7. VDB amplifier: AC load line

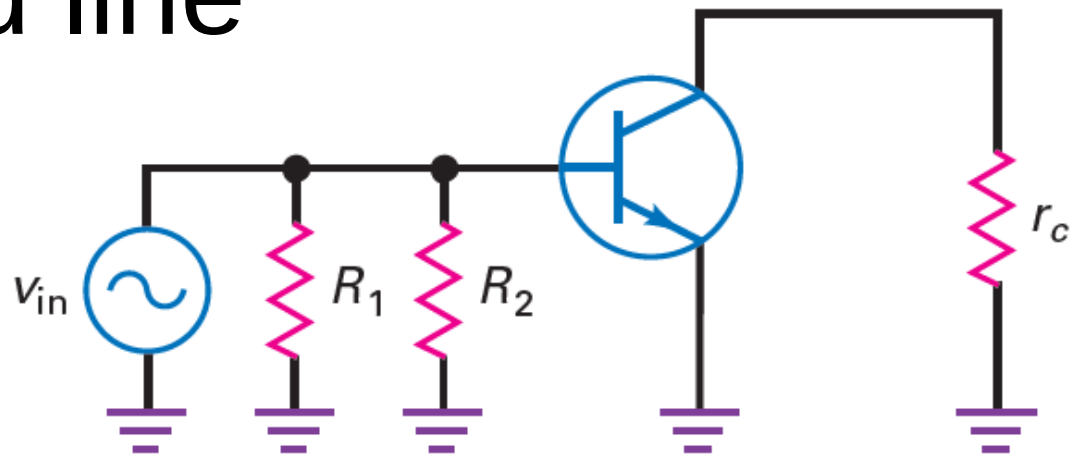
- AC equivalent and AC Load line:
  In the presence of ac.
- $I_C = I_{CQ} - \frac{V_{CE}}{r_c} + \frac{V_{CEQ}}{r_C}$
- At saturation, $V_{CE} = 0$
  $i_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$

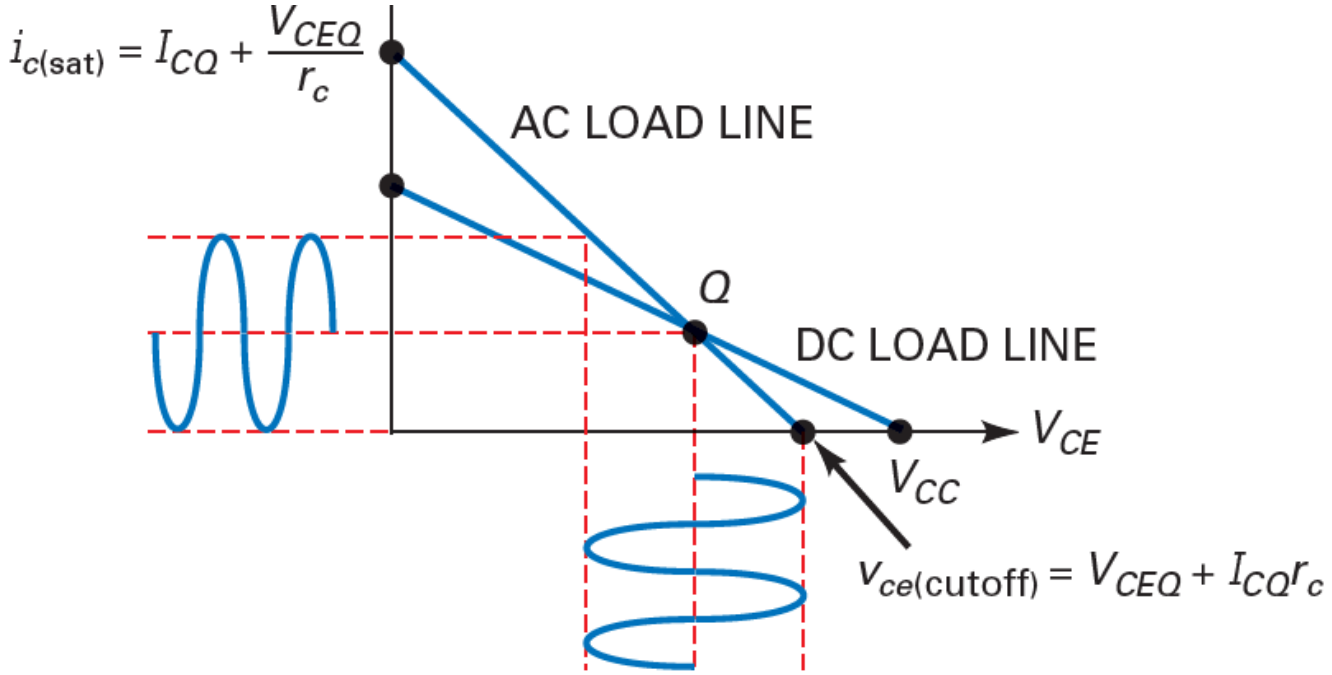




7. VDB amplifier: AC load line

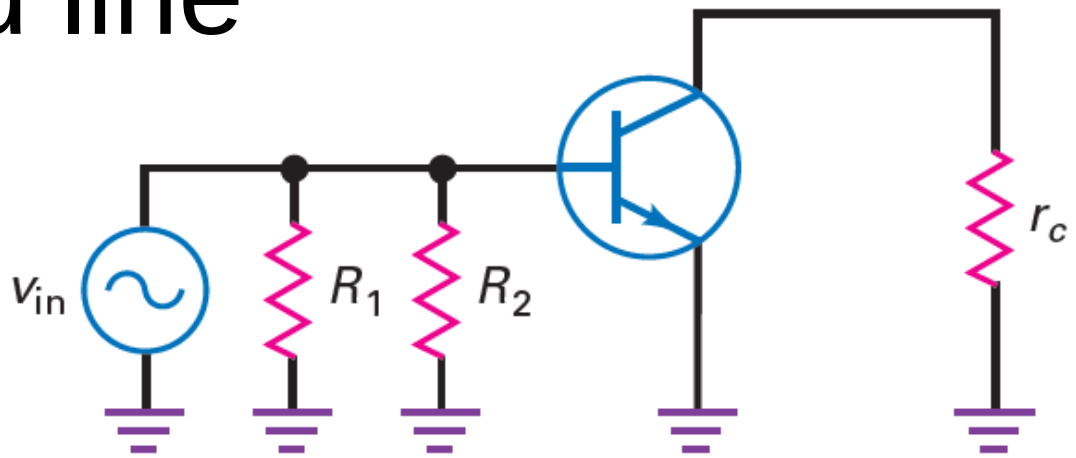
- AC equivalent and AC Load line:
  In the presence of ac.
- $I_C = I_{CQ} - \frac{V_{CE}}{r_c} + \frac{V_{CEQ}}{r_C}$
- At saturation, $V_{CE} = 0$
  $i_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$
- At cutoff, $I_C = 0$
  $v_{ce(cutoff)} = I_{CQ}r_c + V_{CEQ}$

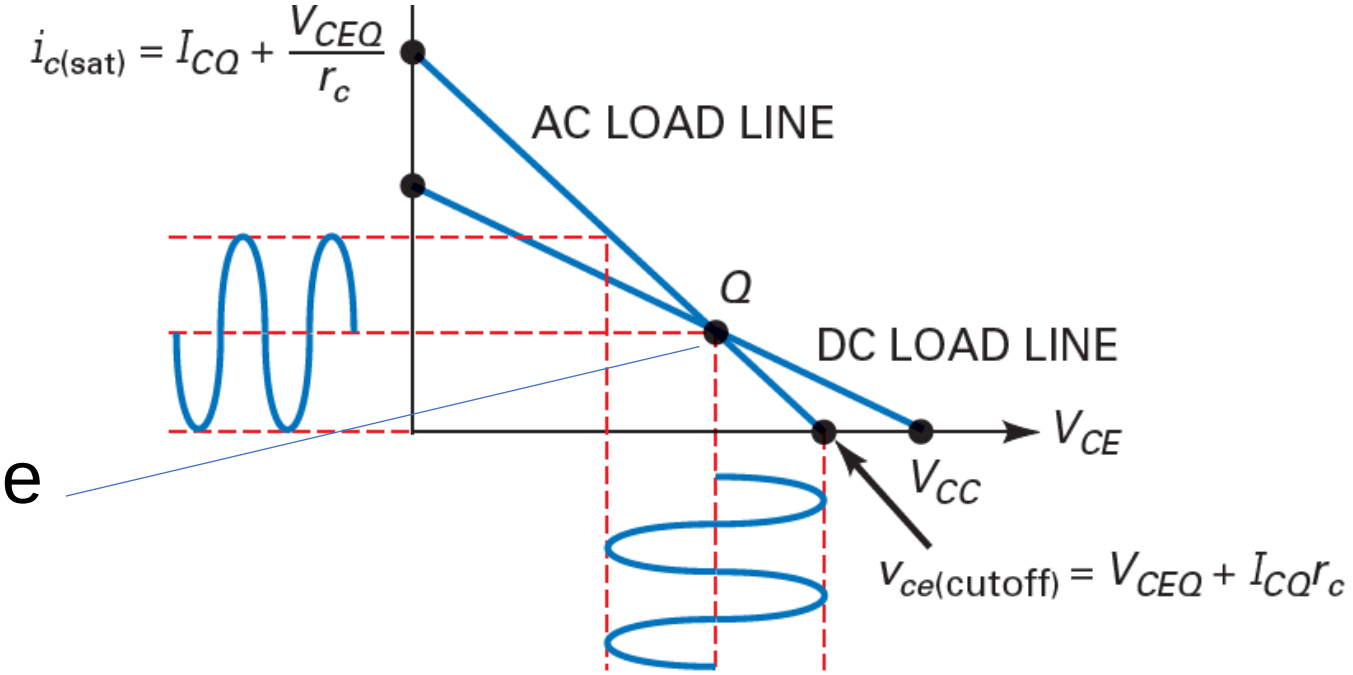




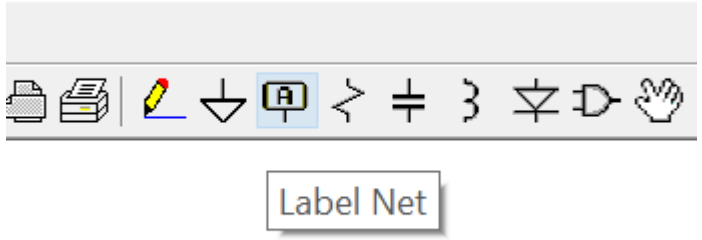
7. VDB amplifier: AC load line

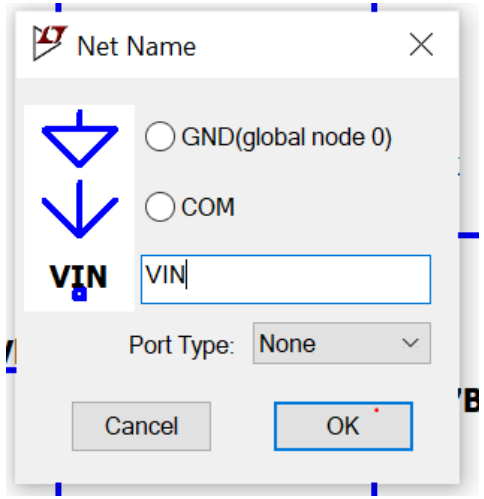
- AC equivalent and AC Load line:
  In the presence of ac.
- $I_C = I_{CQ} - \frac{V_{CE}}{r_c} + \frac{V_{CEQ}}{r_C}$
- At saturation, $V_{CE} = 0$
  $i_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$
- At cutoff, $I_C = 0$
  $v_{ce(cutoff)} = I_{CQ} r_c + V_{CEQ}$
- Maximum peak to peak voltage
  $MPP < V_{CC}$

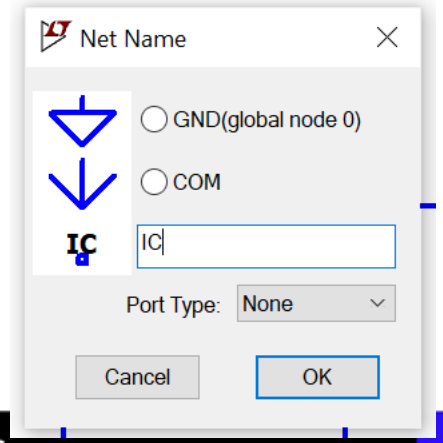


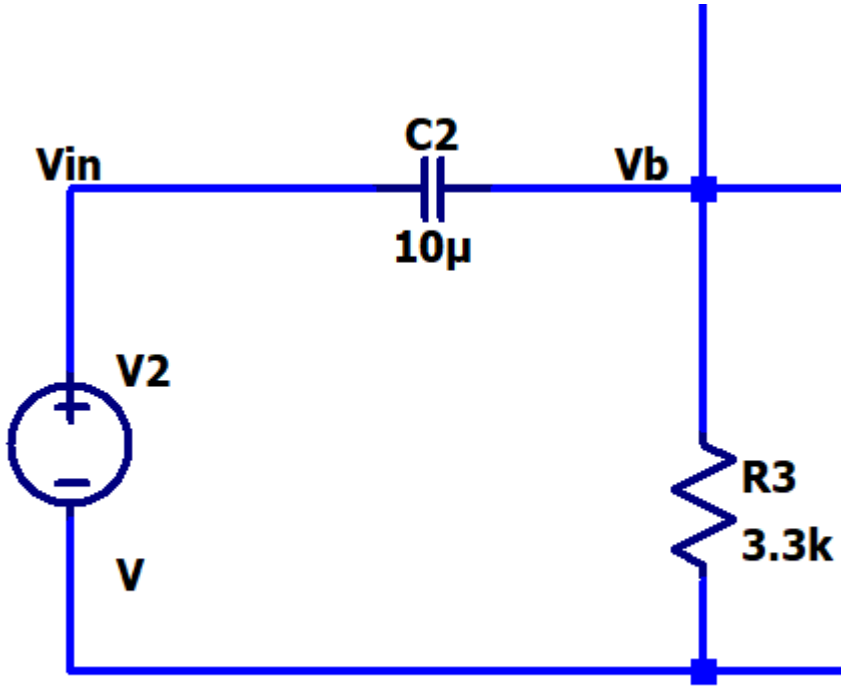


8. Task 2: Operating point of the amplifier







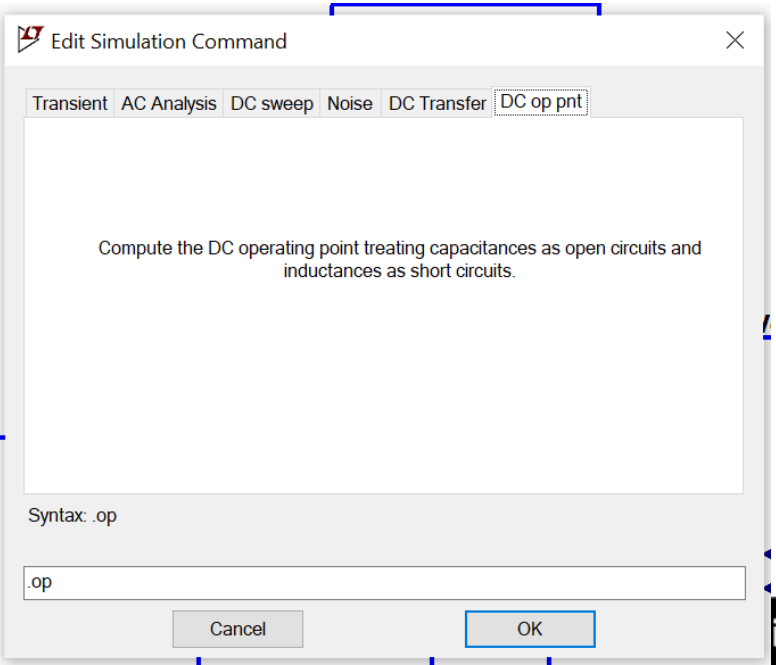


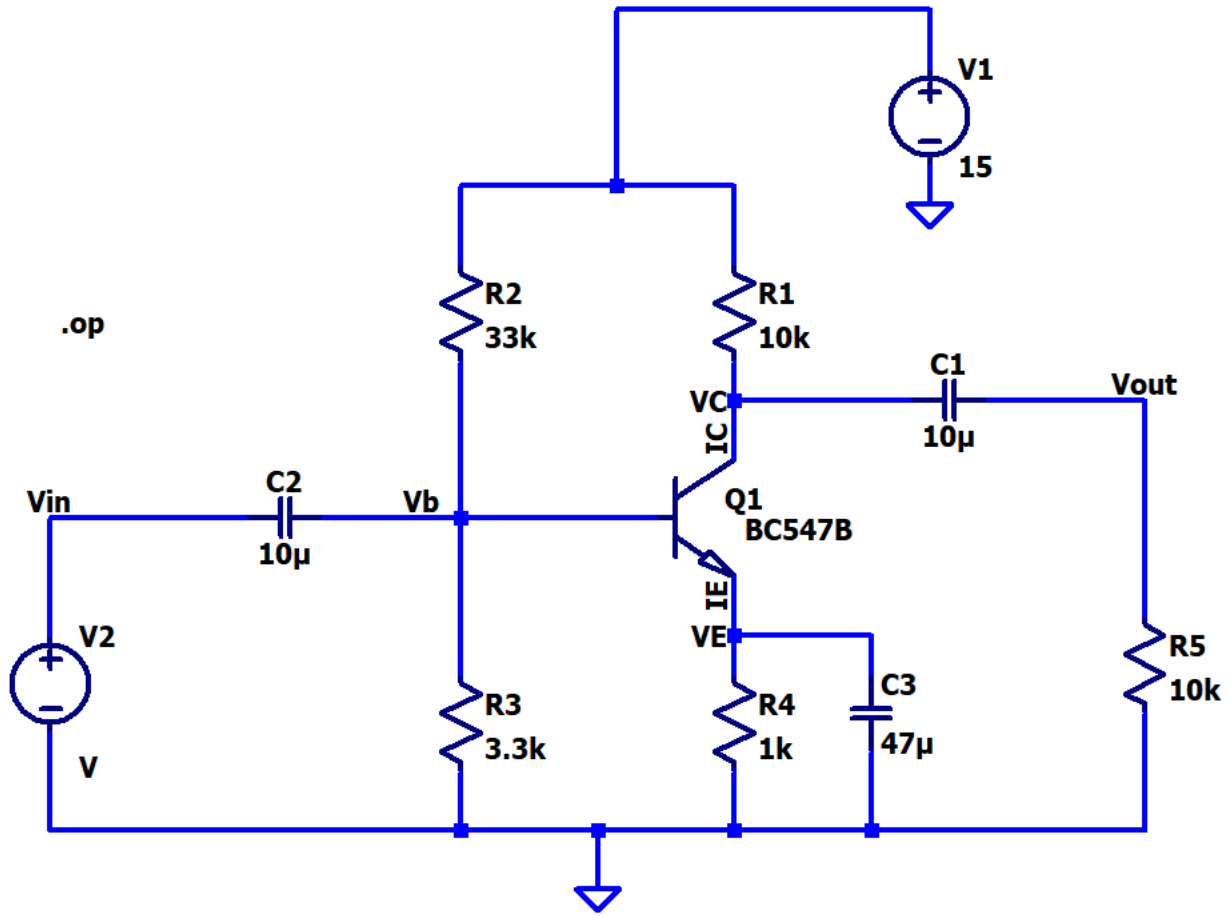
8. Task 2: Operating point of the amplifier

p_analysis]

View Simulate Tools Window Help

Run
Pause Ctrl+P
Halt Ctrl+H
Clear Waveforms '0'
Efficiency Calculation
Control Panel
Edit Simulation Cmd





8. Task 2: Operating point of the amplifier

- Click RUN,
- You will find right operating point values

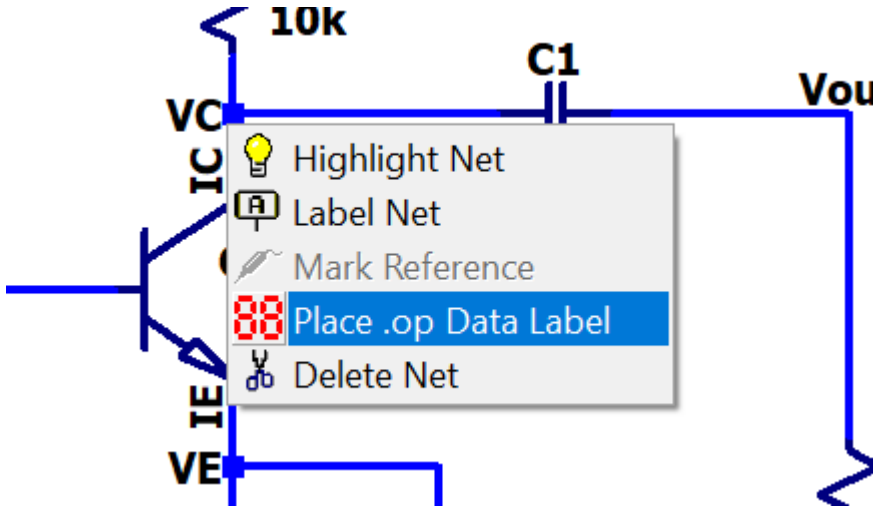
* E:\VIT Data\Academics\2021-22 FALL\ECE1008 EHT\Exp 05\01_dc_op_analysis.asc

```
       --- Operating Point ---

V(ic):          7.73536         voltage
V(vb):          1.35665         voltage
V(ve):          0.728793        voltage
V(n001):        15              voltage
V(vout):        7.73536e-013    voltage
V(vin):         0               voltage
Ic(Q1):         0.000726464     device_current
Ib(Q1):         2.3284e-006     device_current
Ie(Q1):         -0.000728793    device_current
I(C3):          3.42533e-017    device_current
I(C2):          1.35665e-017    device_current
I(C1):          -7.73536e-017   device_current
I(R5):          7.73536e-017    device_current
I(R4):          0.000728793     device_current
I(R3):          0.000411106     device_current
I(R2):          0.000413435     device_current
I(R1):          0.000726464     device_current
I(V2):          1.35665e-017    device_current
I(V1):          -0.0011399      device_current
```

8. Task 2: Operating point of the amplifier

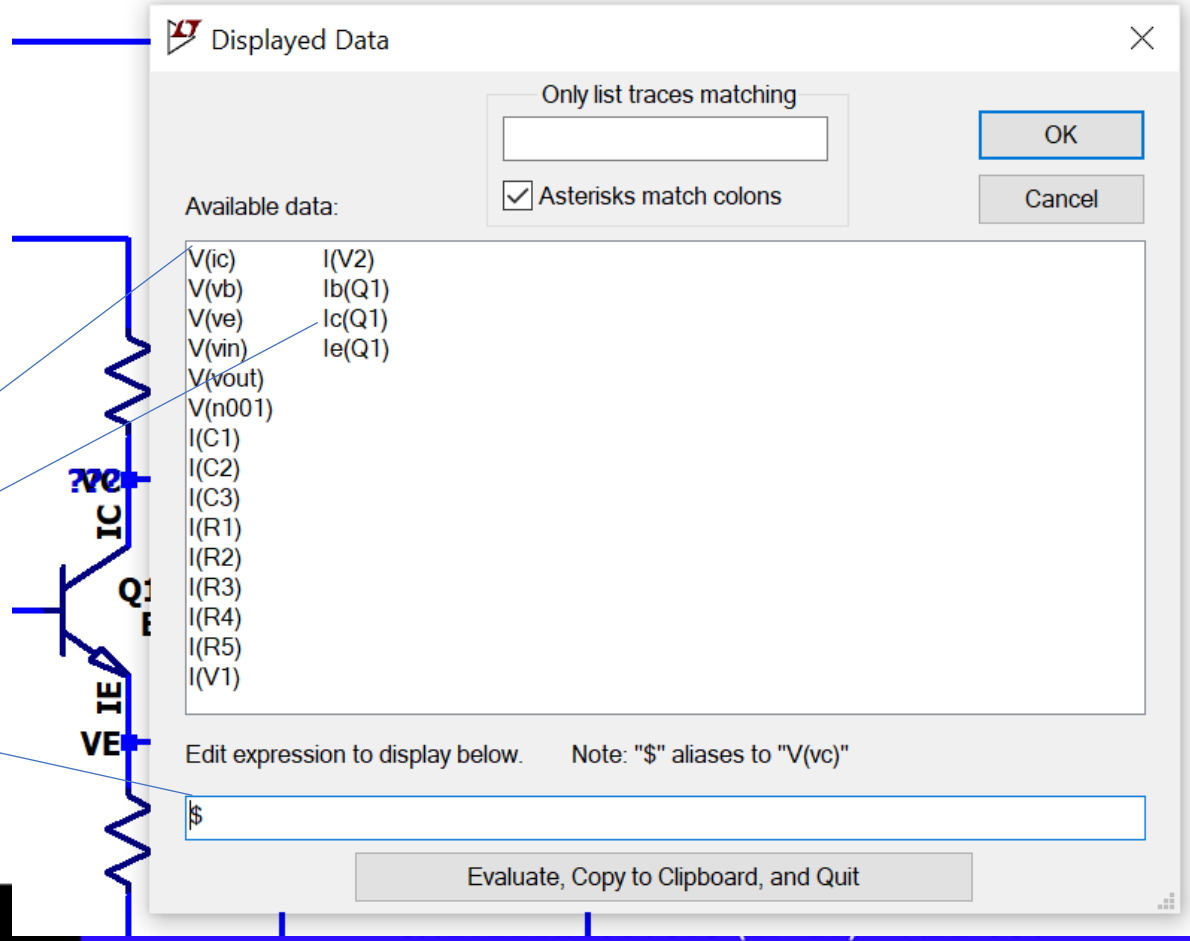
- After clicking RUN, right click at Collector wire,



- Right click at question marks, Remove "$"

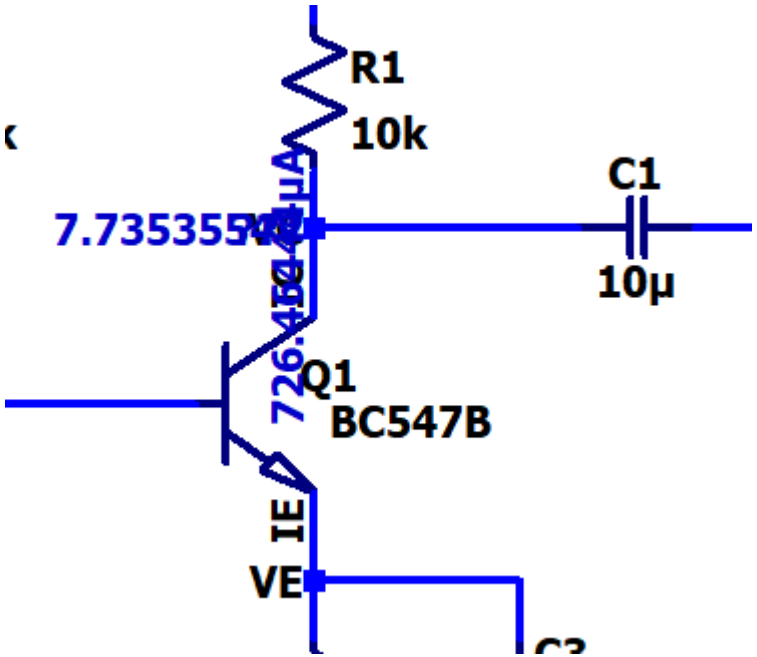
  and replace with "V(ic)"

  or "Ic(Q1)"

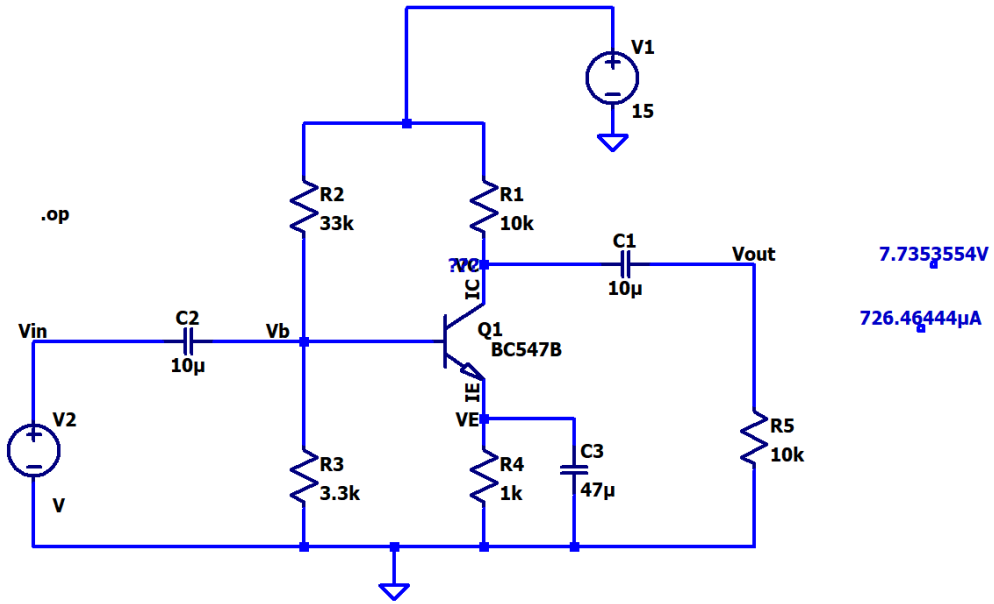


8. Task 2: DC Operating point of the amplifier

- Place the values nearby

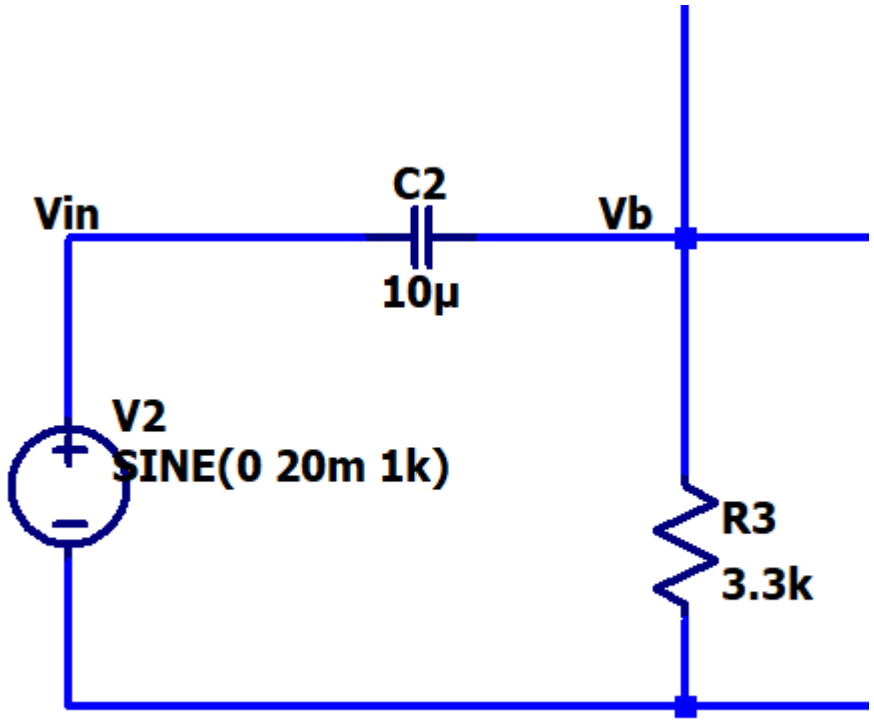


- Or move separately the DC operating point

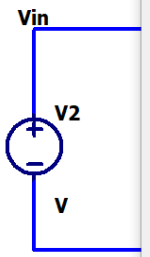


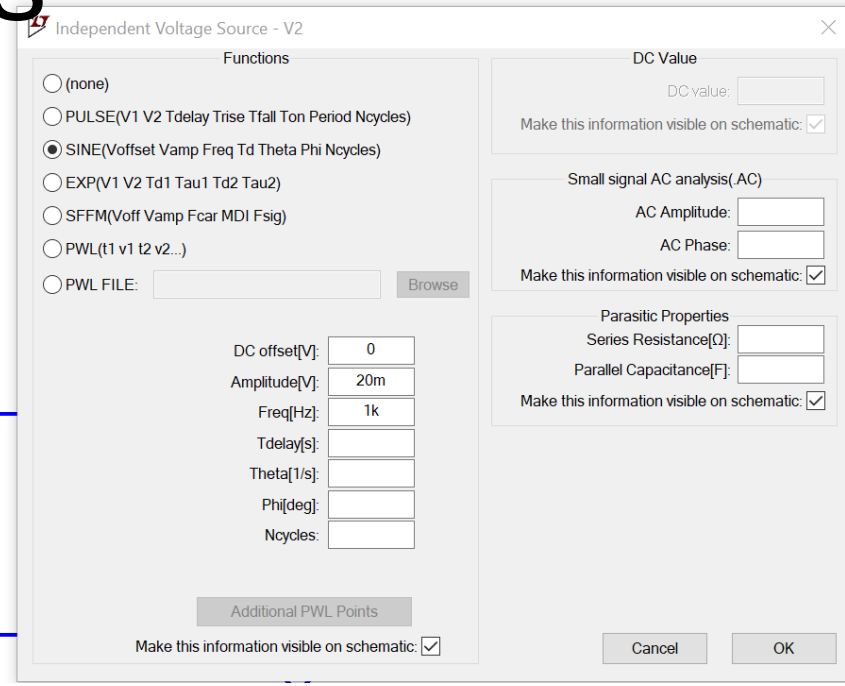
9. Task 3: AC transient analysis

- Select input voltage source and advanced -> sine wave -> 20mV and 1kHz



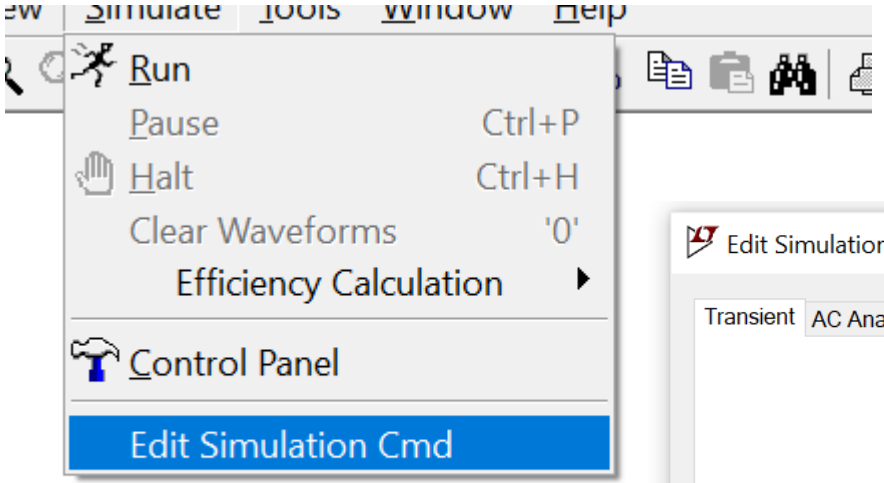
.op



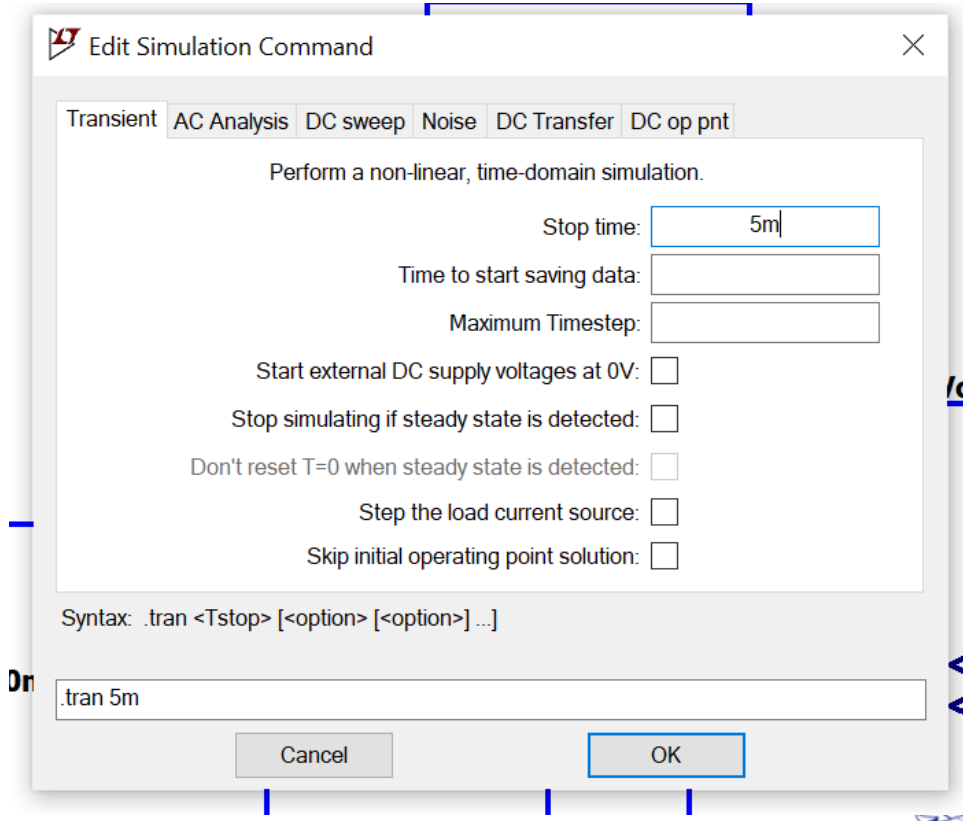


9. Task 3: AC transient analysis

- For the circuit,

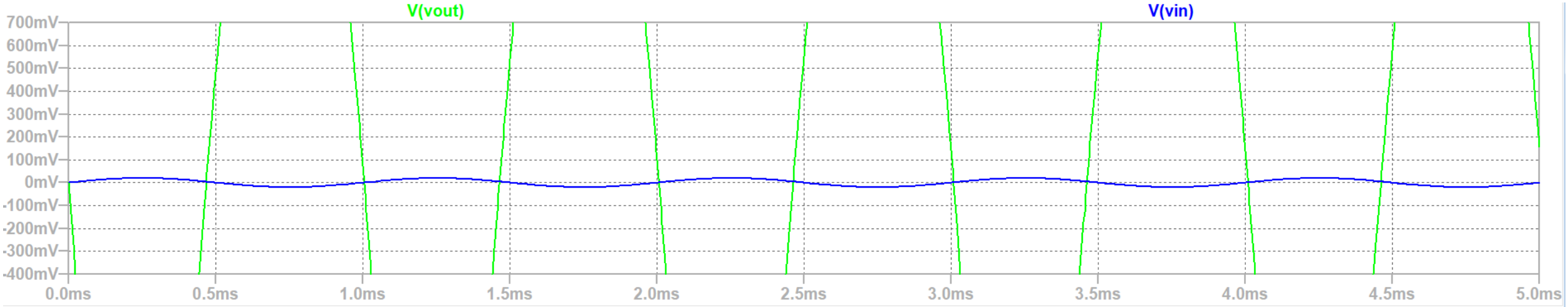


- Delete the .op command



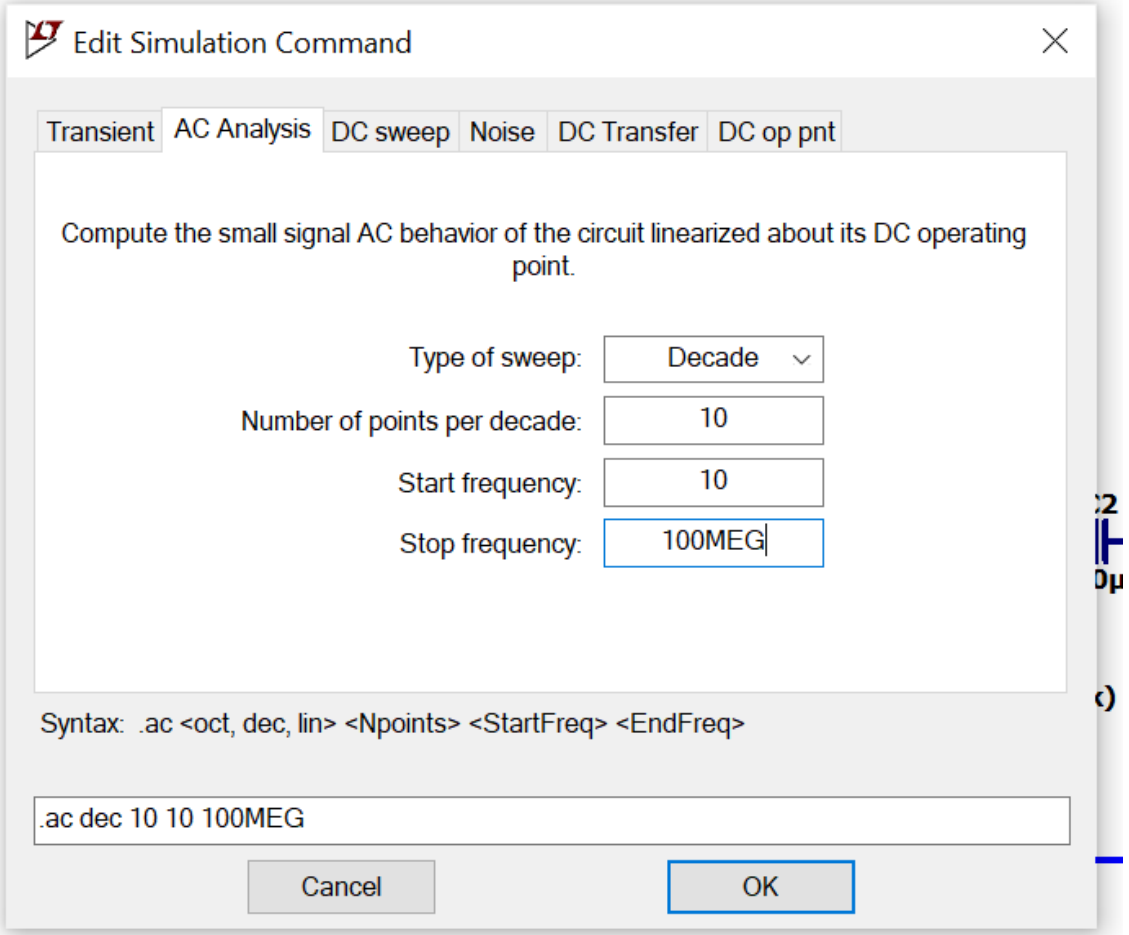
9. Task 3: AC transient analysis

- Plot input and output:



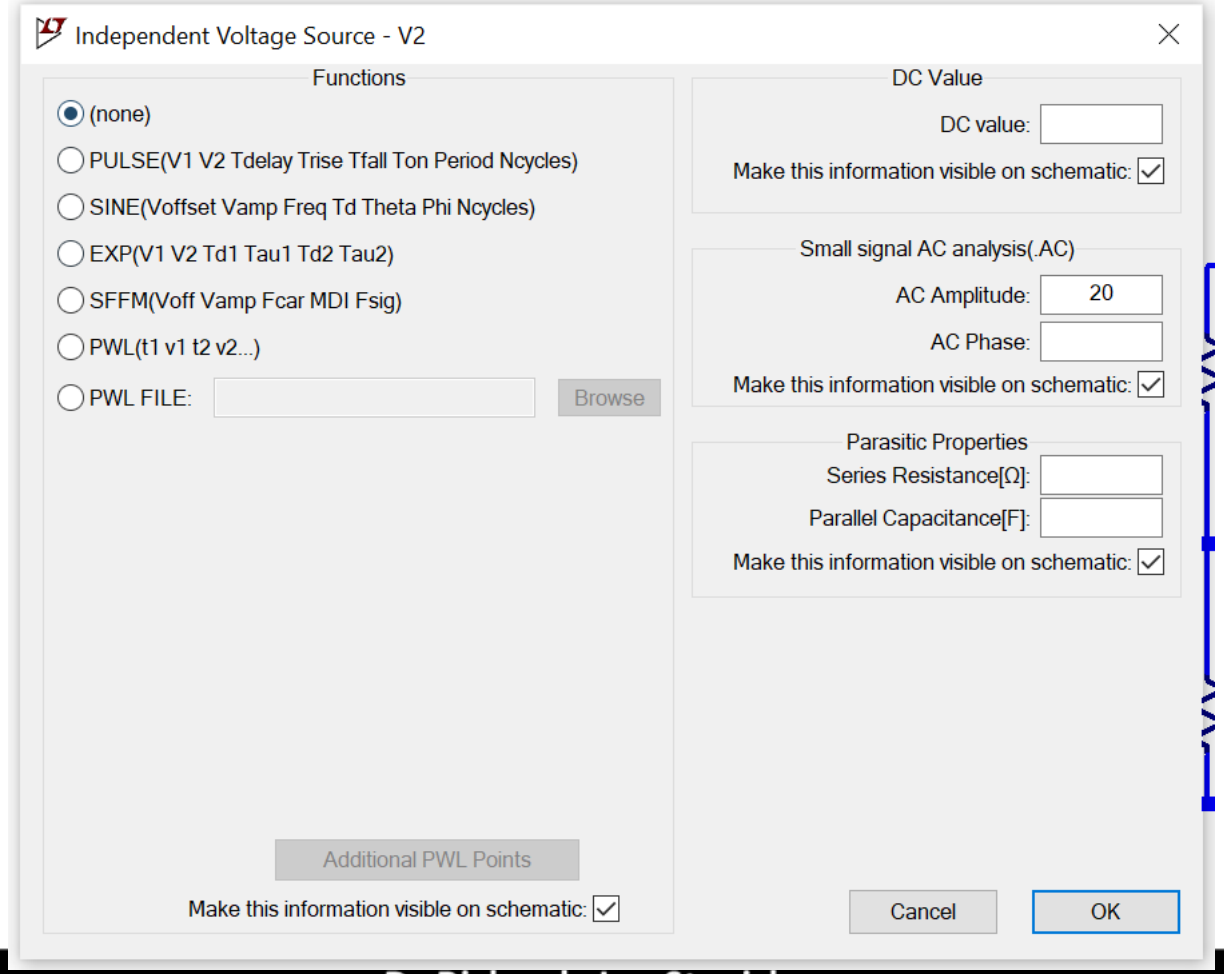
10. Task 4: AC Analysis – Frequency sweep

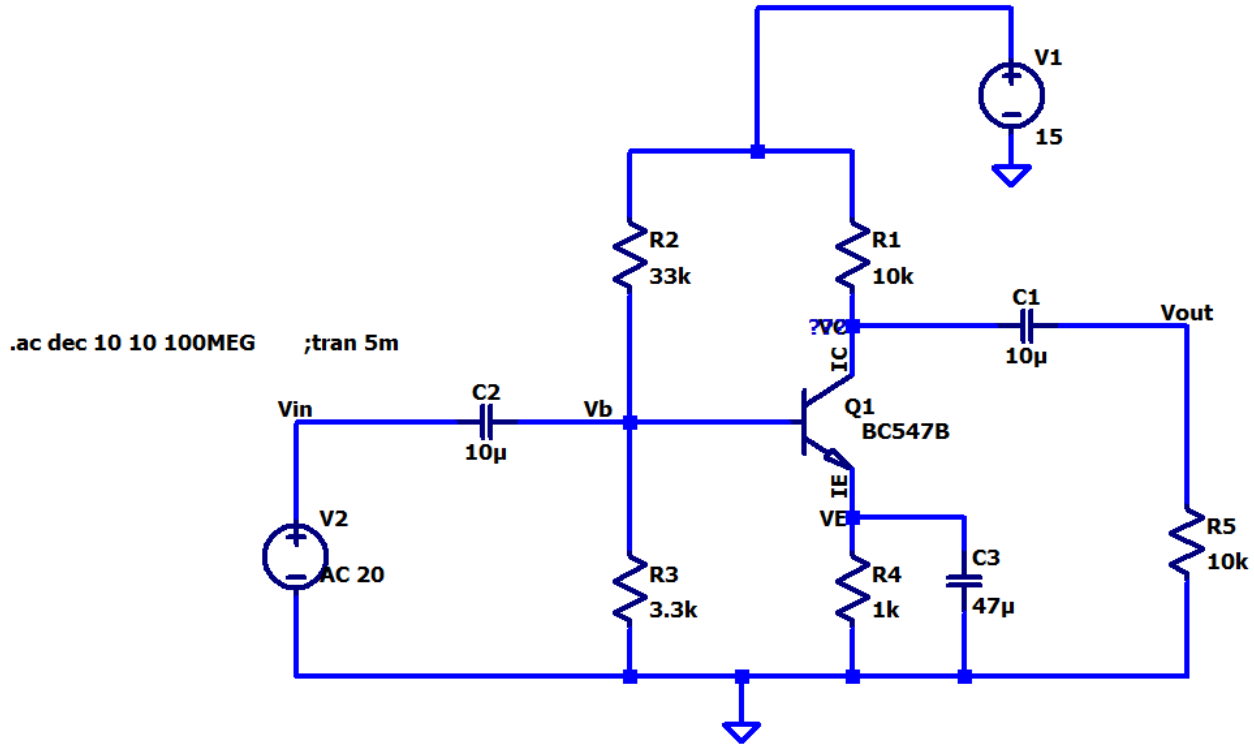
- For the circuit, obtain Bode plot.



10. Task 4: AC Analysis – Frequency sweep

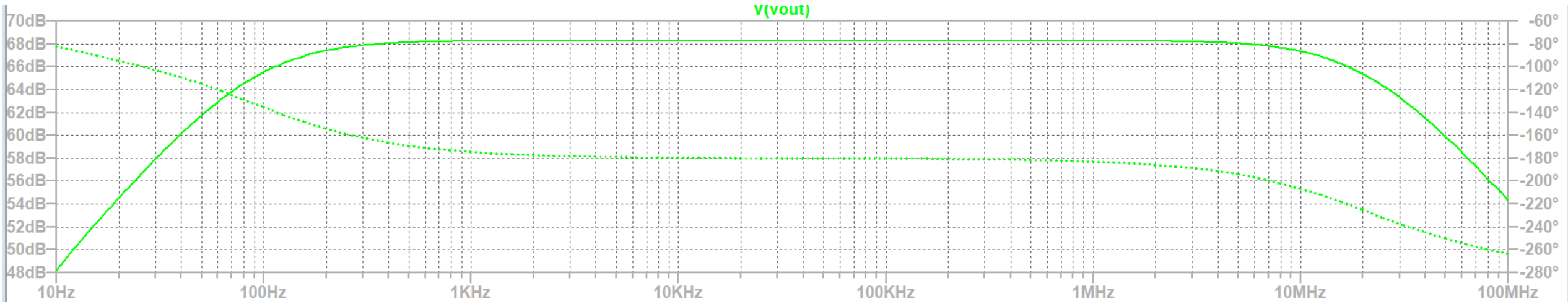
- Change input voltage source to





10. Task 4: AC Analysis – Frequency sweep

- Run and select output
- Left: Magnitude
  Right: Phase response.



Important NOTE

- Enter your **registration number** and **Full Name** next to

  all your circuits and
  the output plots.
- Keep the background of circuit and plot as white.

LAB record instructions:

For the lab experiment,

- Write the **Aim**.
- Complete the **Software/Hardware components used**.
- **Obtain the expression for the outputs.**
- Place the respective **circuits in LT Spice**.
- Connect the inputs and outputs. Name them and **write the same in the lab copy(inputs and outputs section)**.
- Use probe in LT spice to plot all possible combinations.
- Write a **concluding statement for each circuit**.
- **Submit** the document's soft copy **on time** in lms.vit.ac.in when available.