10. Design and analysis of Buck converter with realistic capacitance

Course: ECE1008 – Electronic Hardware Troubleshooting LAB

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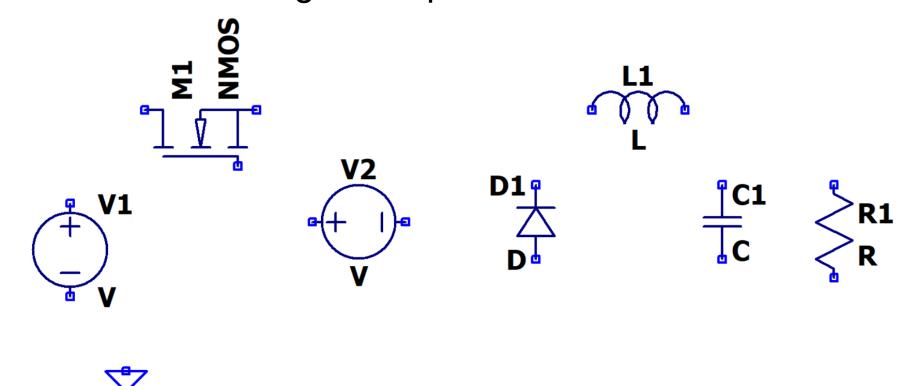


Introduction

- Buck converter is used to provide
 Stable Stepped down dc voltage from a source of higher DC voltage.
- In this experiment, we will design a 12V DC to 5.7V DC signal using NMOS,
 Schottky diode (reverse biased)
 - Schottky diode (reverse biased) LC filter and a resistor.

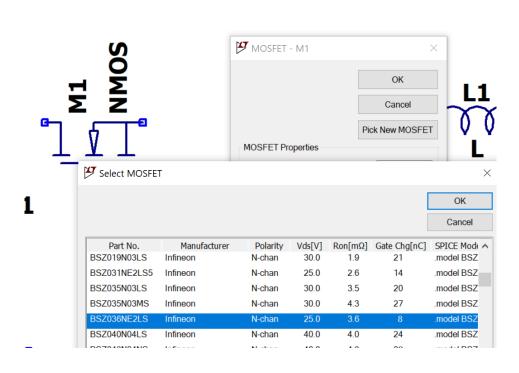


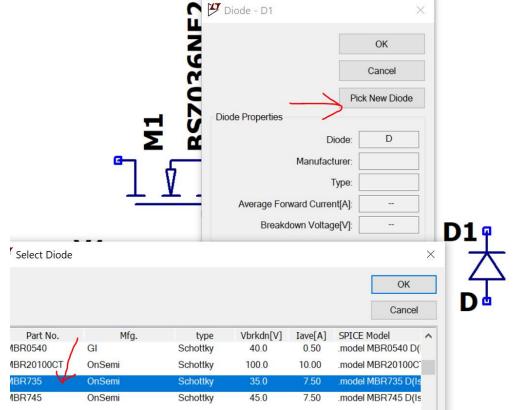
1a) Place all the components as shown below: Note: Use CTRL+R for rotating a component.



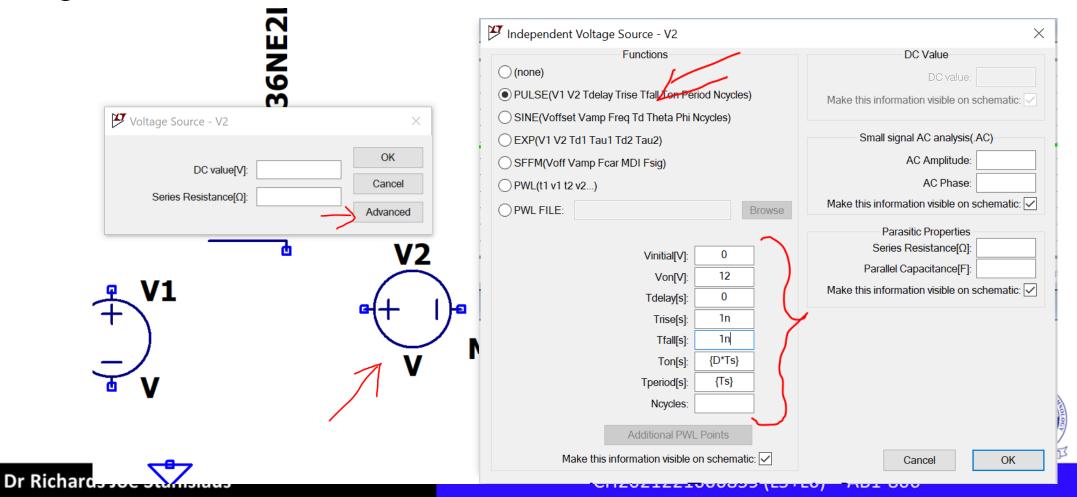


1b) Right click at NMOS and select BSZ036NE2LS Right click at diode, and pick new diode: MBR735





2. Set input DC voltage V1 as 12V and second Voltage source V2as Pulse source.

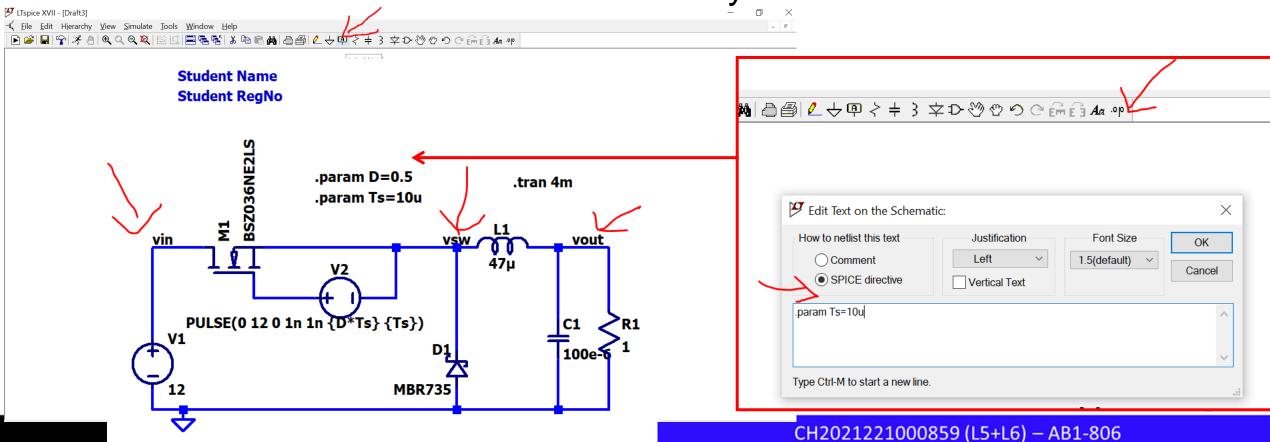


Add labelnets Vin, VSW, Vout.

EditText on schematic -> Spice directive

Include parameters D and Ts (pulse source's duty cycle time duration.)

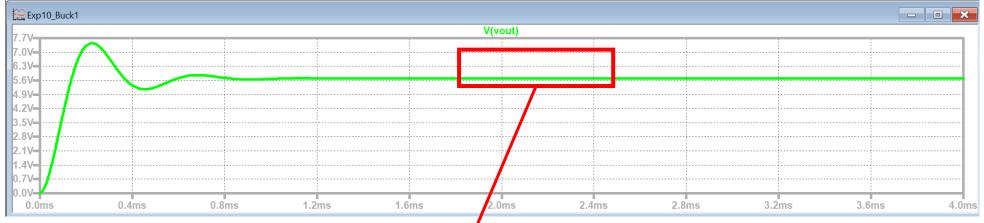
Edit Simulation command -> Transient analysis -> 4m

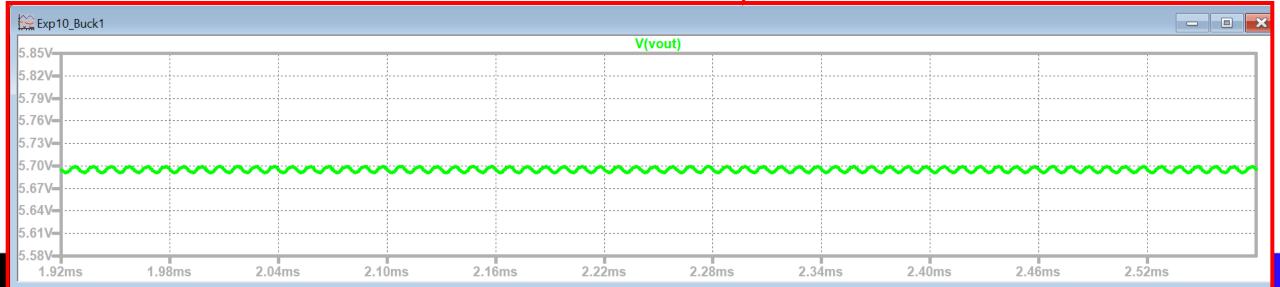


Task 1a: Measure the output (vout) fluctuations in steady state

• Simulation > Edit simulation command .tran 4m

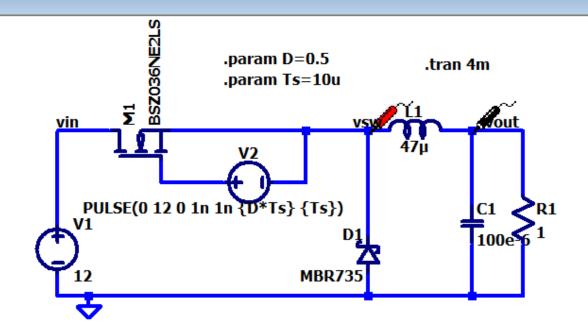
• Run

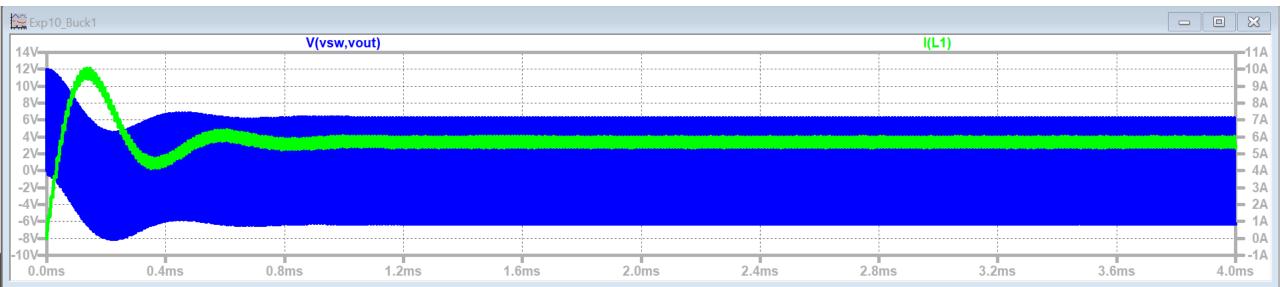




Task 1b: Measure the voltage, current across inductor in steady state

- Click at Inductor's vsw end, hold the mouse and move to vout and release the mouse click This will measure voltage across the inductor.
- Measure the inductor current too.

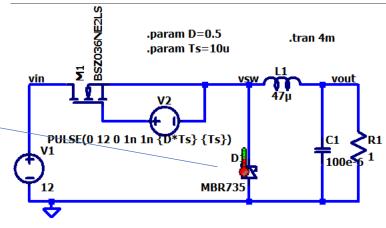


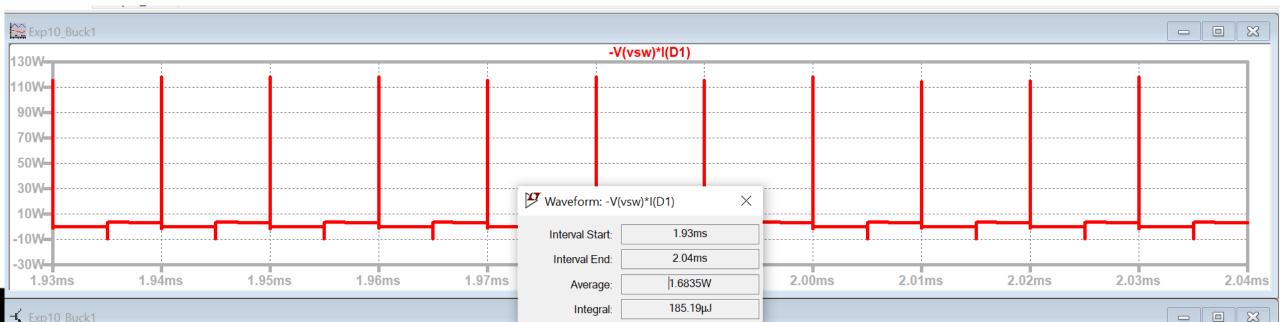


Task 1c: Measure the instantaneous power and average power at components

- Press alt key and click on Diode
- Zoom in the plot and Hold CTRL key and click on the variable in plot (power)

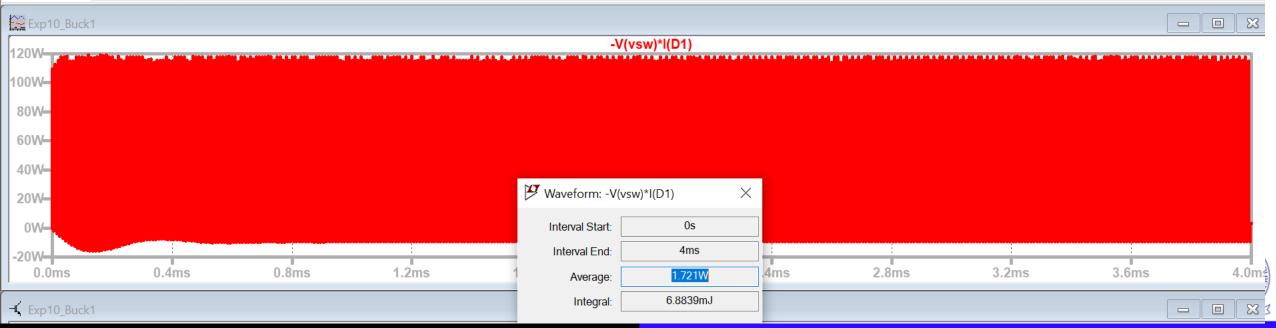
The pop-up window will display average power.





Task 1c: Measure the instantaneous power and average power at components

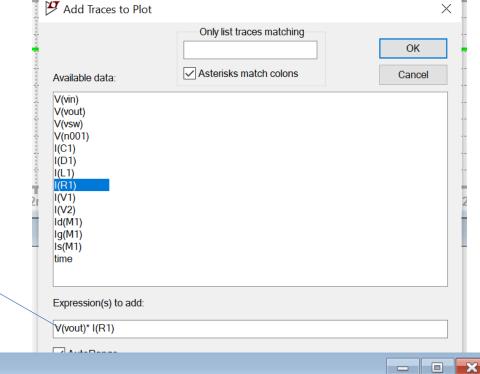
• To calculate average for whole period: Zoom to fit the plot and find average:

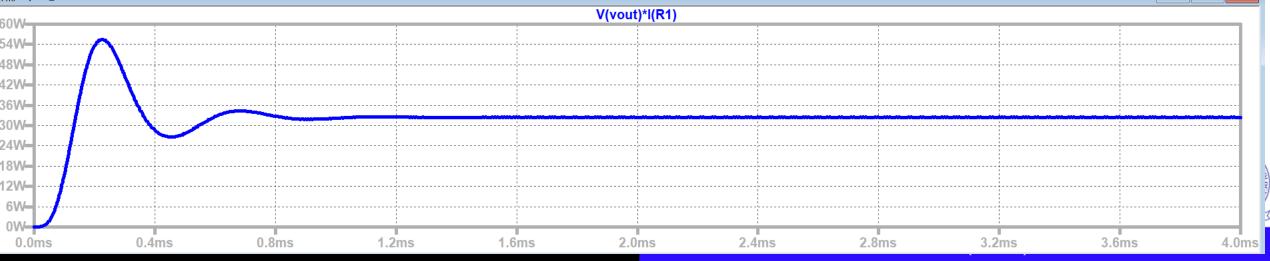


Exp10 Buck1

Task 1d: Measure the instantaneous power and average power at output

 Alternatively, for instantaneous power at load resistor, Right click at plot -> Add trace-> In expression: Type V(vout)*I(R1)

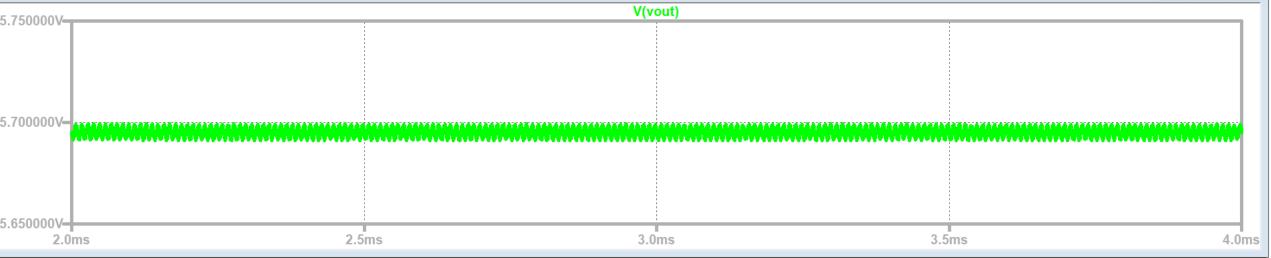




Task 2a: Select FFT of the signal (output voltage)

 Select the region on the plot by clicking on y-tick marks and x tick marks

x: 2ms to 3ms and y: 5.6V to 5.7V





View Plot Settings

€ Zoom Area

💐 Zoom to Fit

Q Pan

<u>S</u>imulation

Ctrl+Z

Ctrl+B

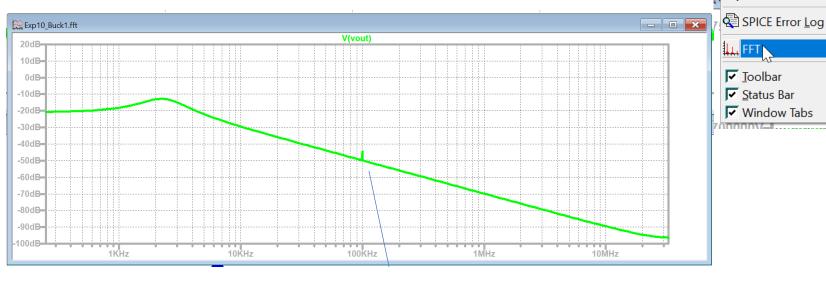
Ctrl+E

CH202122100

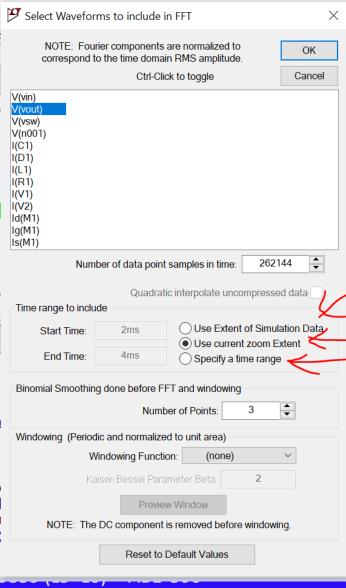
Task 2a: Select FFT of the signal (output voltage)

Select the plot window, and View-> FFT

Select extent of simulation data



Switching frequency

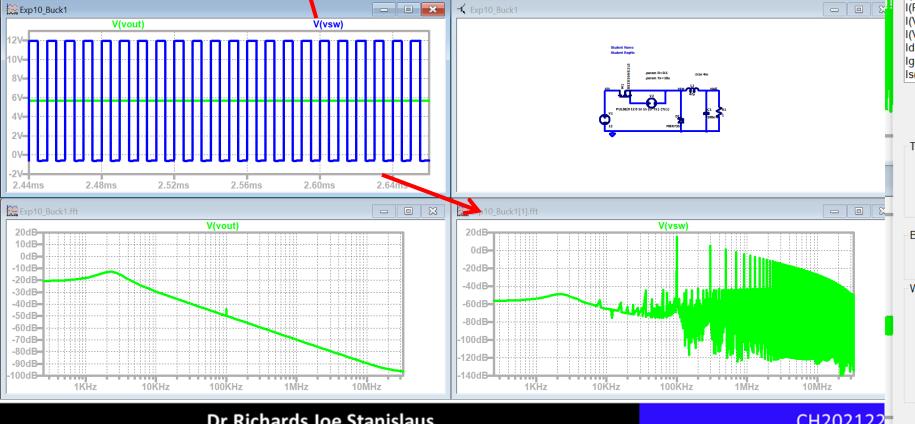


Select Waveforms to include in FFT

Task 2b: Select FFT of the signal (Switch

voltage)

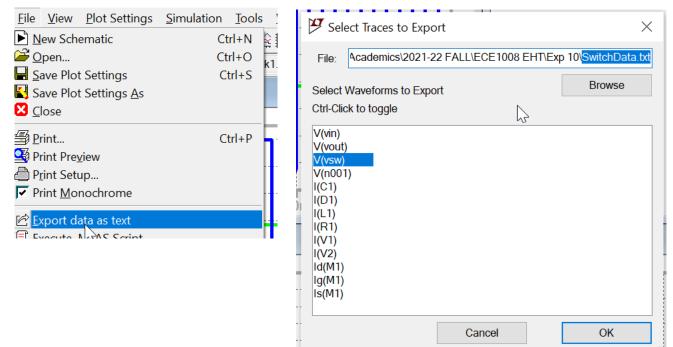
 Select the vsw in FFT and plot for entire range Notice the frequency and its harmonics.

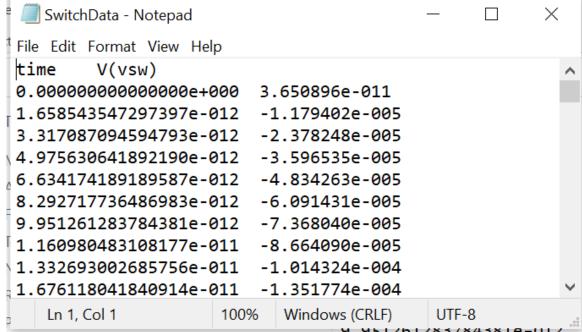


NOTE: Fourier components are normalized to OK correspond to the time domain RMS amplitude. Ctrl-Click to toggle Cancel V(vin) V(vout) V(n001) I(D1) I(V1) I(V2) Id(M1) Ig(M1) Is(M1) 262144 Number of data point samples in time: Quadratic interpolate uncompressed data Time range to include Use Extent of Simulation Data Start Time: Use current zoom Extent 4ms End Time: Specify a time range Binomial Smoothing done before FFT and windowing Number of Points: Windowing (Periodic and normalized to unit area) Windowing Function: Preview Window NOTE: The DC component is removed before windowing. Reset to Default Values

Task 2c: Export switch voltage plot data

File -> Export -> Select vsw(switch voltage)







Task 3: Import txt file as source

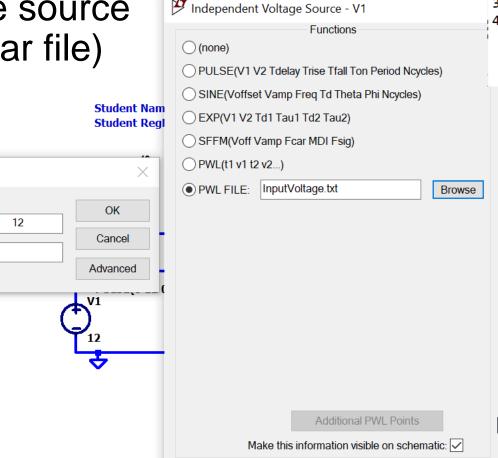
• Save a new text file with extension .txt with the data:

 Right click at input voltage source Select pwl(piece wise linear file)

Voltage Source - V1

DC value[V]:

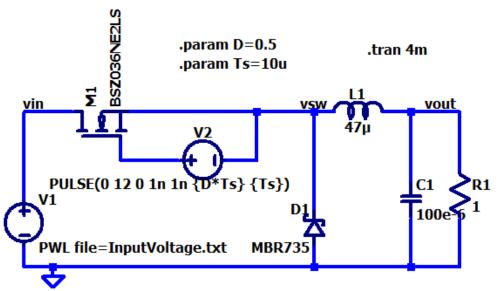
Series Resistance[Ω]:

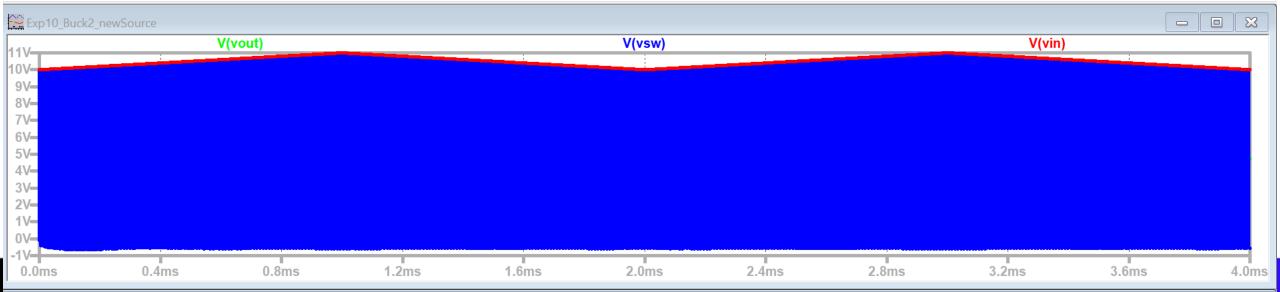


InputVoltage - Notepad File Edit Format View Help 0 10 1m 11 2m 10 3m 11 4m 10 12 hematic: Small signal AC analysis(.AC) AC Amplitude: AC Phase: Make this information visible on schematic: Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: Cancel OK

Task 3: Import txt file as source RegNo

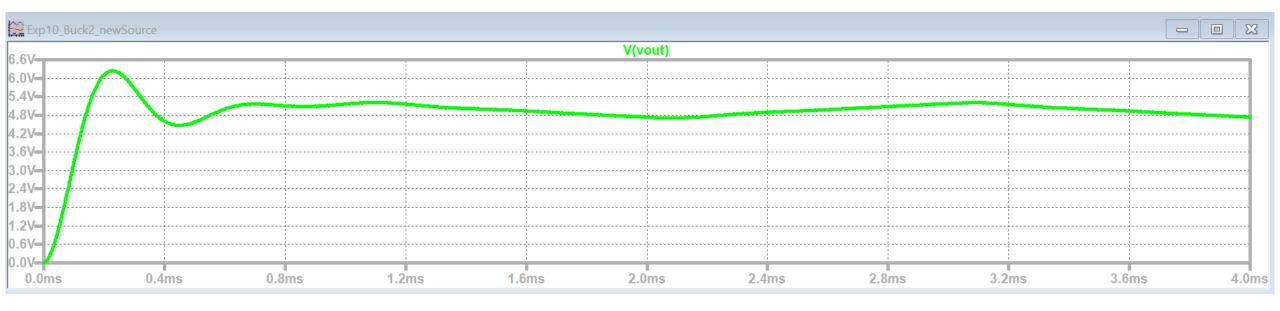
- Input voltage source is in RED
- Blue represents the switching voltage





Task 3: Import txt file as source

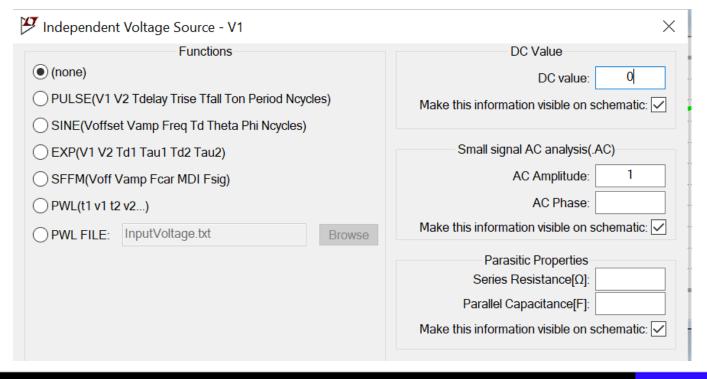
Vout

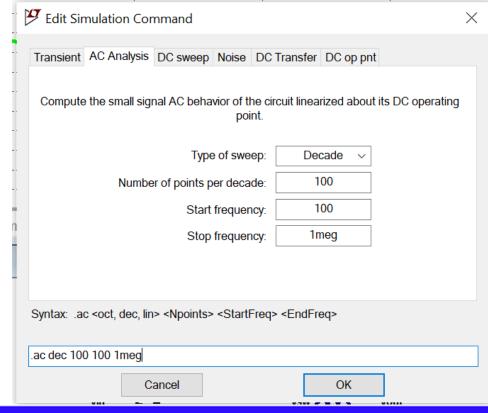




Task 4: AC analysis

- Replace V2 pulse source to DC (12V)
- Replace V1 input voltage to DC (0V) with an ac amplitude of 1V
- Set simulation as ac analysis:

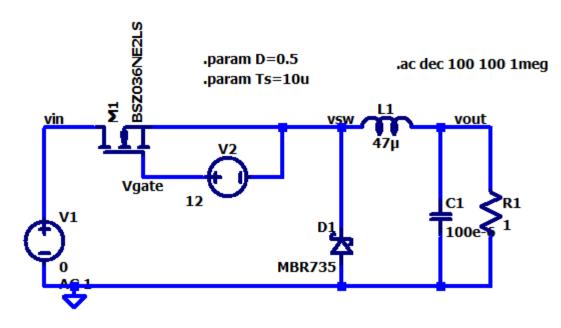


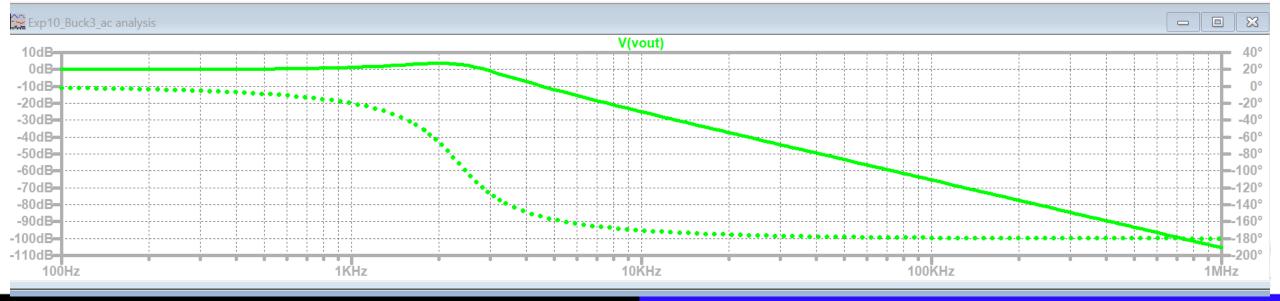


Student Name Student RegNo

Task 4: AC analysis

- Close to DC: unity gain
 After resonance: the drop in gain
- After DC: notice the Phase shift





Hierarchy View Simulate Tools

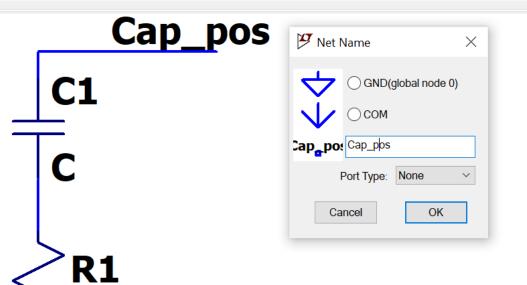
D- Open this Sheet's Symbol

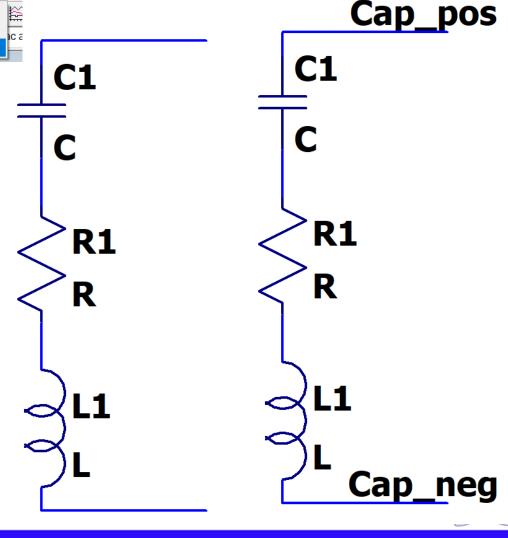
Create a New Symbol

Create a New Sheet

• Delete the 100uF capacitor.

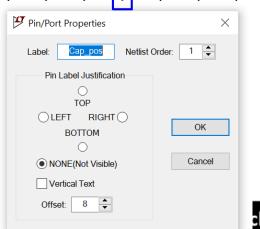
Go to Hierarchy -> New sheet
 Place the three passive components (C, L and R) in series.
 Add labelnets to end terminals.

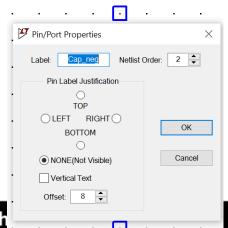


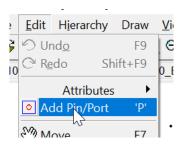


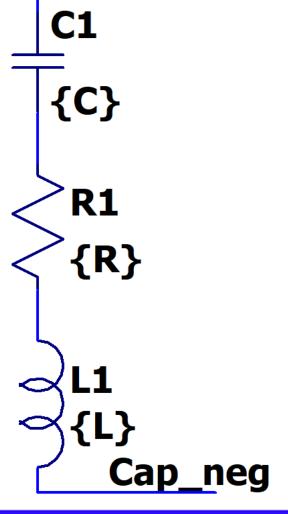
Change the values as parameters:
 {C}, {R} and {L}

- Save as "my_cap.asc"
- Once sub-circuit is complete Hierarchy->Create New symbol
- Edit-> Add Pins/ports
 Use same labelnet names



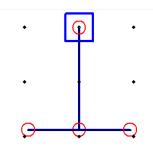


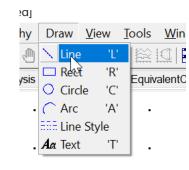




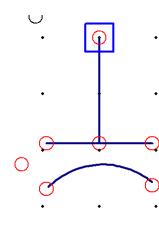


- Remember the netlist order
- To draw between the pins,
 Draw -> line or arc

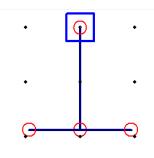


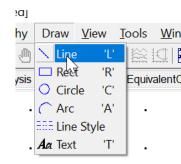




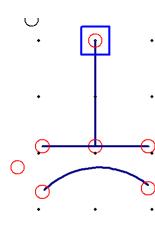


- Remember the netlist order
- To draw between the pins,
 Draw -> line or arc

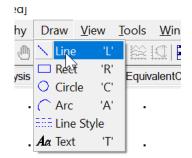




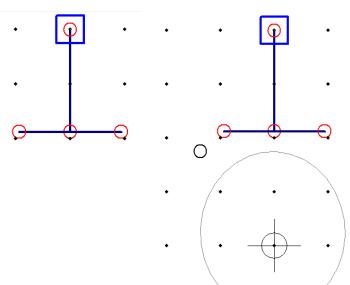
To draw arc: select arc->

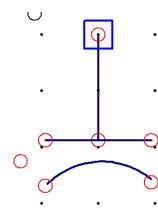


- Remember the netlist order
- To draw between the pins,
 Draw -> line or arc

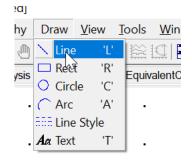


To draw arc: select arc->
 Draw an ellipse,

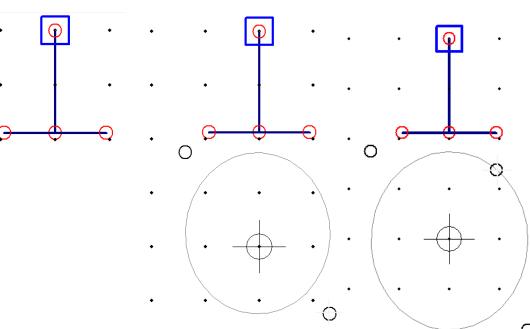


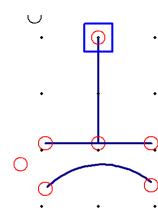


- Remember the netlist order
- To draw between the pins,
 Draw -> line or arc

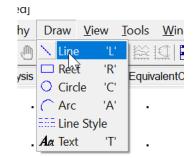


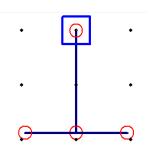
To draw arc: select arc->
 Draw an ellipse,
 Select the right end of arc

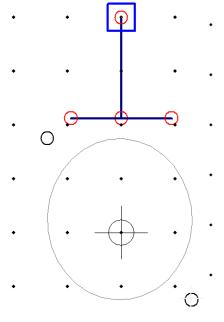


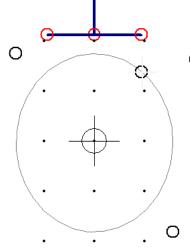


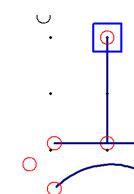
- Remember the netlist order
- To draw between the pins,
 Draw -> line or arc





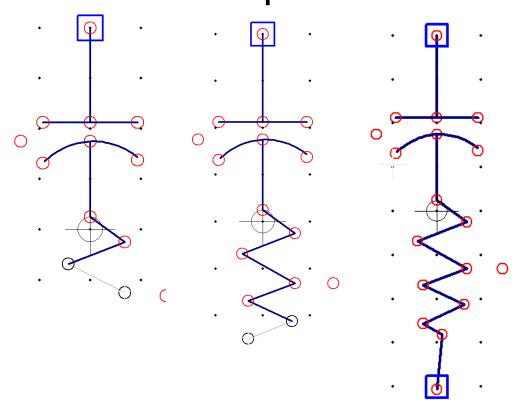






To draw arc: select arc->
 Draw an ellipse,
 Select the right end of arc
 Then select location of left end and then click.

- Using Draw -> Line Complete the custom symbol as Capacitor with series resistor
- File-> Save-> my_cap.asy
 (same name with .asy for symbol)

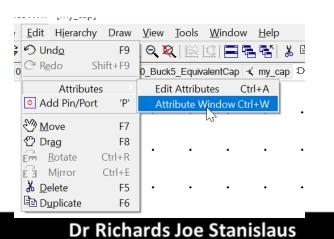


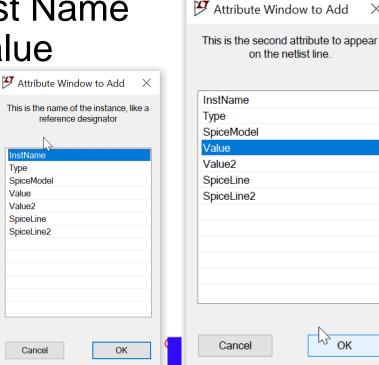


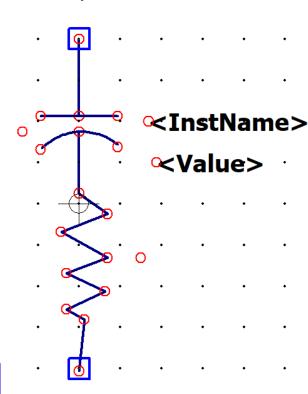
0859

Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

- Using Draw -> Line
 Complete the custom symbol as Capacitor with series resistor
- File-> Save-> my_cap.asy (same name with .asy for symbol)
- Edit-> Attribute window-> Inst Name
 -> Value
- Close the symbol.







21000859 (L5+L6) - AB1-806

Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

Edit Hierarchy View Select Component Symbol Open circuit of Buck converter: Undo Undo E:\VIT Data\Academics\2021-22 FALL\ECE1008 EHT\Exp 10 >> Redo Shift+F9 Edit-> component -> **A**a Text OP SPICE Directive 'S' Search the folder where you had SPICE Analysis Resistor saved the my_cap symbol. Capacitor Inductor Place the my_cap symbol 文 Diode E:\VIT Data\Academics\2021-22 FALL\ECE1008 EHT\Exp 10 instead of Capacitor **Student Name Student RegNo** in the initial circuit of 4m transient simulaiton. .param D=0.5 .tran 4m .param Ts=10u OK Cancel vin VSW / vout **/+** \ 47µ Vgate PULSE(0 12 0 1n 1n $\{D^*TS\}$ $\{Ts\}$)

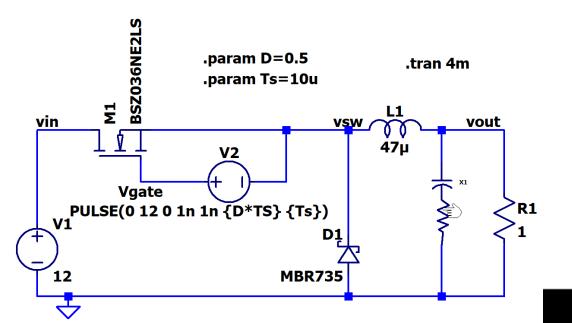
MBR735

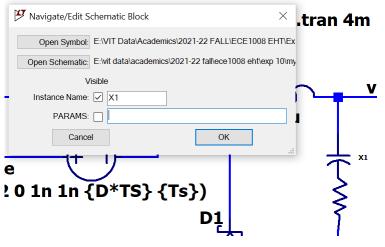
12

5a) Right click at the my_cap symbol and add values as C=100u R=1m L=1p

Simulation -> RUN

Student Name Student RegNo

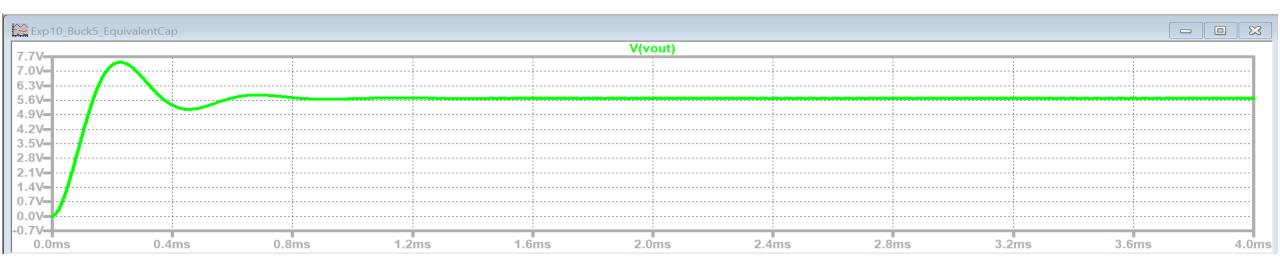




| Navigate/Edit Schematic Block | × |
|--|-------|
| Open Symbol: E:\VIT Data\Academics\2021-22 FALL\ECE1008 EI | HT\Ex |
| Open Schematic: E:\vit data\academics\2021-22 fall\ece1008 eht\exp | 10\my |
| Visible | |
| ■ Instance Name: ✓ X1 | |
| PARAMS: C=100u R=1m L=1p | ı |
| Cancel | |
| | .:: |



5a) C=100u R=1m L=1p (Similar to earlier circuit)

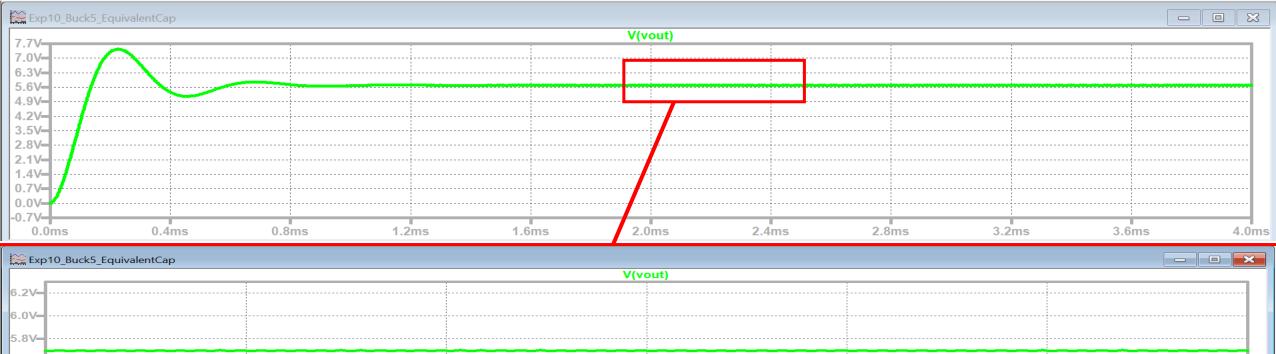




5a) C=100u R=1m L=1p (Similar to earlier circuit) Less ripples as before.

2.1ms

2.0ms



2.2ms

2.3ms

2.4ms

Change the resistance to 100 (unrealistic) to check if symbol works

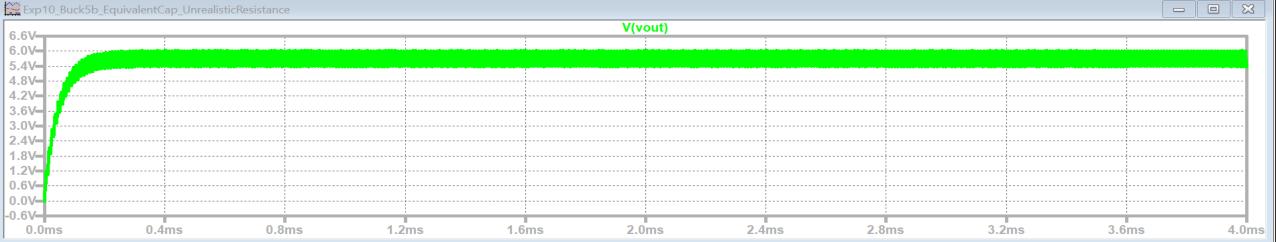
5b) C=100u **R=100** L=1p :

| Navigate/Edit Schen | matic Block × | |
|--|--|--|
| Open Symbol: E:\V | /IT Data\Academics\2021-22 FALL\ECE1008 EHT\Ex | |
| Open Schematic: E:\vit data\academics\2021-22 fall\ece1008 eht\exp 10\my | | |
| Visible | | |
| Instance Name: 🗸 | X1 | |
| PARAMS: | C=100u R=100 L=1p | |
| Cancel | ОК | |
| | ii. | |



Change the resistance to 100 (unrealistic) to check if symbol works

5b) C=100u **R=100** L=1p :





0.4 ms

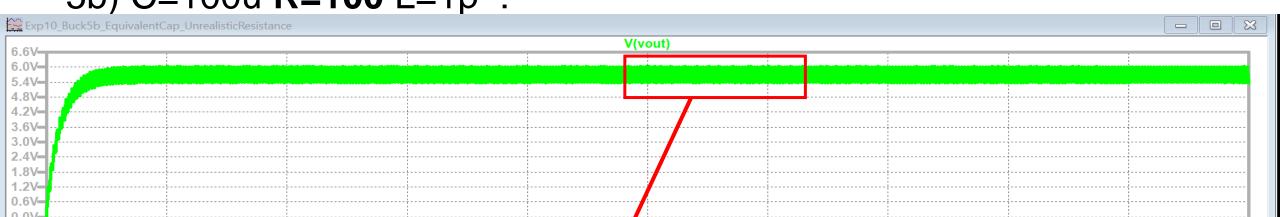
0.8ms

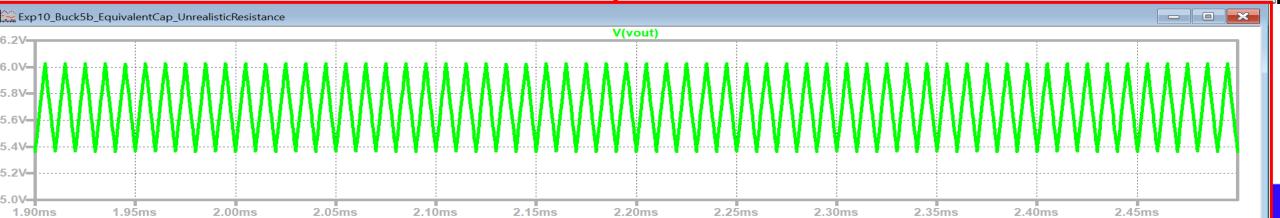
1.2ms

1.6ms

Task 5: To replace the ideal capacitor with model consisting of equivalent series resistance, inductance and capacitance

Change the resistance to 100 (unrealistic) to check if symbol works 5b) C=100u **R=100** L=1p:





2.0ms

2.4ms

2.8ms

3.2ms

3.6ms

4.0ms

Important NOTE

 Enter your registration number and Full Name next to

all your circuits and the output plots.

•Keep the background of circuit and plot as white.



LAB record instructions:

For the lab experiment,

- Write the Aim.
- Complete the Software/Hardware components used.
- Obtain the expression for the outputs.
- Place the respective circuits in LT Spice.
- Connect the inputs and outputs. Name them and write the same in the lab copy(inputs and outputs section).
- Use probe in LT spice to plot all possible combinations.
- Write a concluding statement for each circuit.
- Submit the document's soft copy on time in Ims.vit.ac.in when available.