ARYAMAN MISHRA
19BCE1027

<div align="center">
EXPERIMENT NO: 7
Design of Logic gates using NMOS, PMOS and Resistor
</div>

Aim: To design Logic gates using NMOS, PMOS and Resistor in LTSpice.
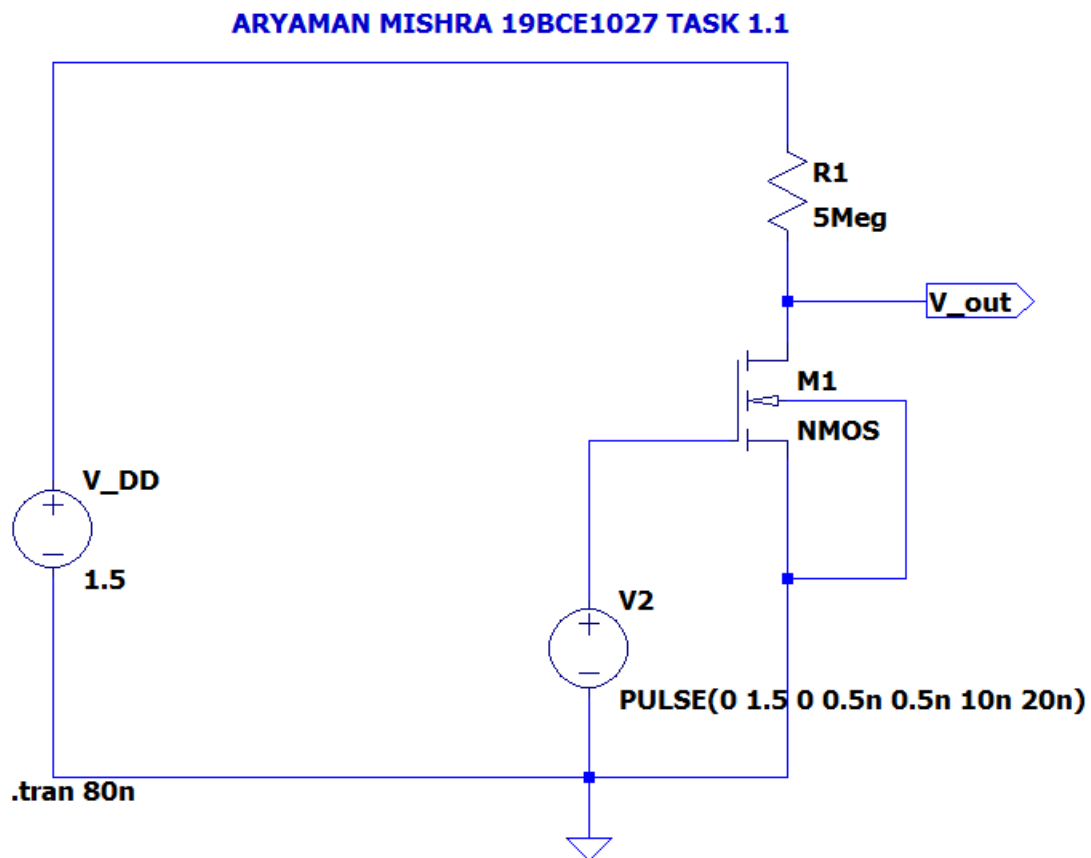
Software used: LTSpice

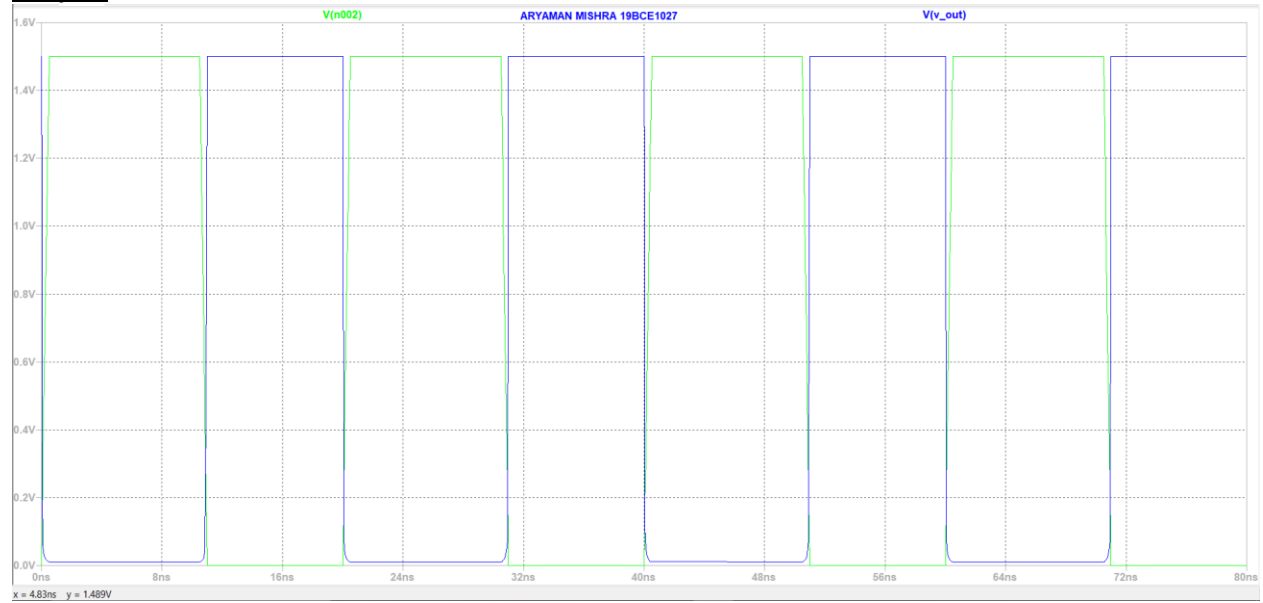**Components required:** Resistors, voltage source, NMOS, PMOS.

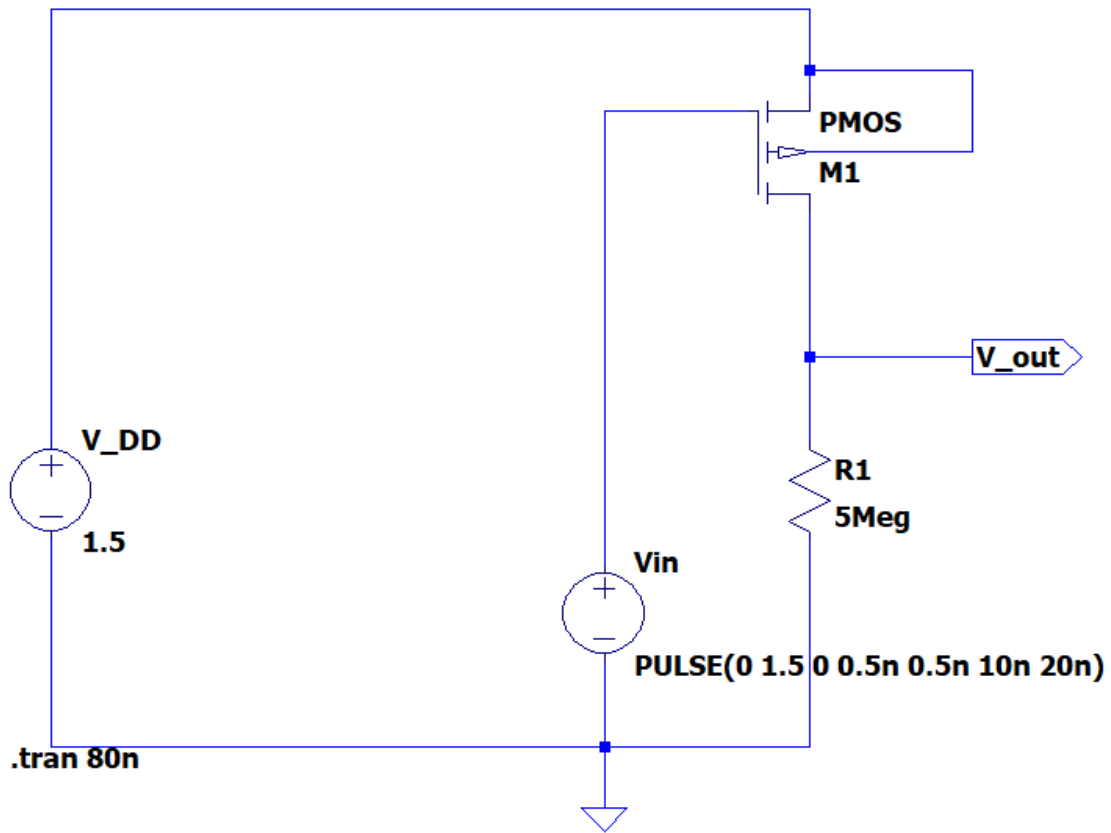**Task 1:**

1.1: **NOT GATE with NMOS**
Circuit:

ARYAMAN MISHRA 19BCE1027 TASK 1.1

R1
5Meg

V_out

M1
NMOS

V_DD

1.5

V2

PULSE(0 1.5 0 0.5n 0.5n 10n 20n)

.tran 80n

Output:

Truth Table:

Vin	Vout
1	0
0	1

1.2: NOT GATE with NMOS
Circuit:

ARYAMAN MISHRA 19BCE1027 TASK 1.2

V_DD

+

−

1.5

.tran 80n

PMOS

M1

V_out

R1

5Meg

Vin

+

−

PULSE(0 1.5 0 0.5n 0.5n 10n 20n)

Output:

V(n002)   ARYAMAN MISHRA 19BCE1027   V(v_out)

1.6V

1.4V

1.2V

1.0V

0.8V

0.6V

0.4V

0.2V

0.0V

0ns   8ns   16ns   24ns   32ns   40ns   48ns   56ns   64ns   72ns   80ns

x = 0.04ns   y = 1.627V
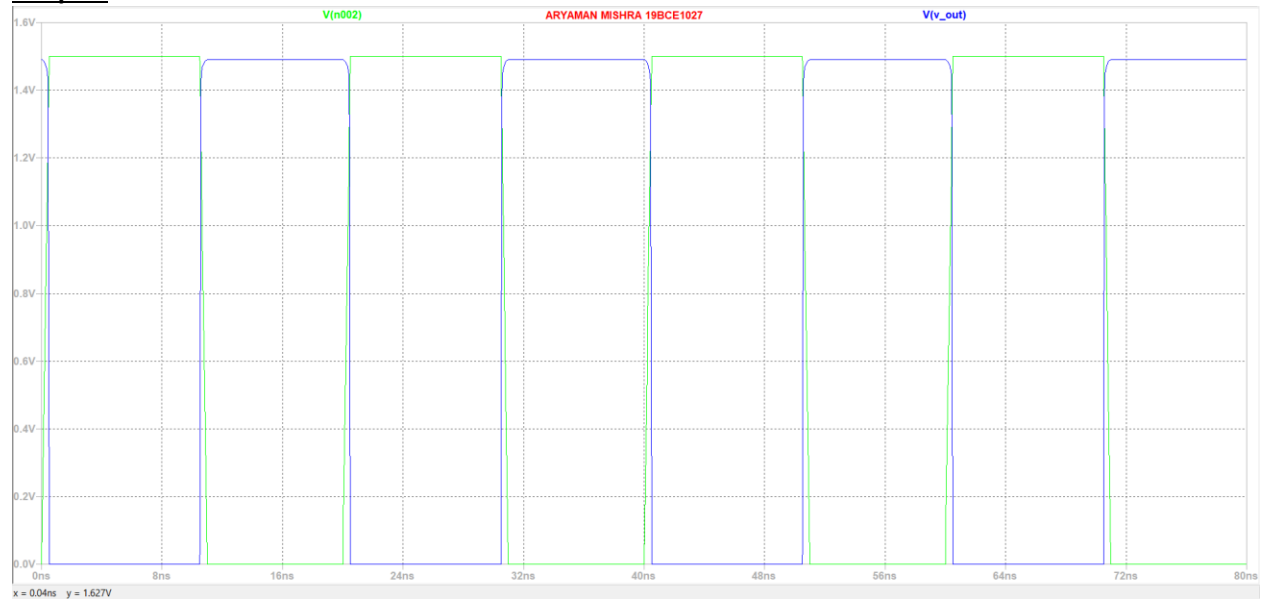
Truth Table:

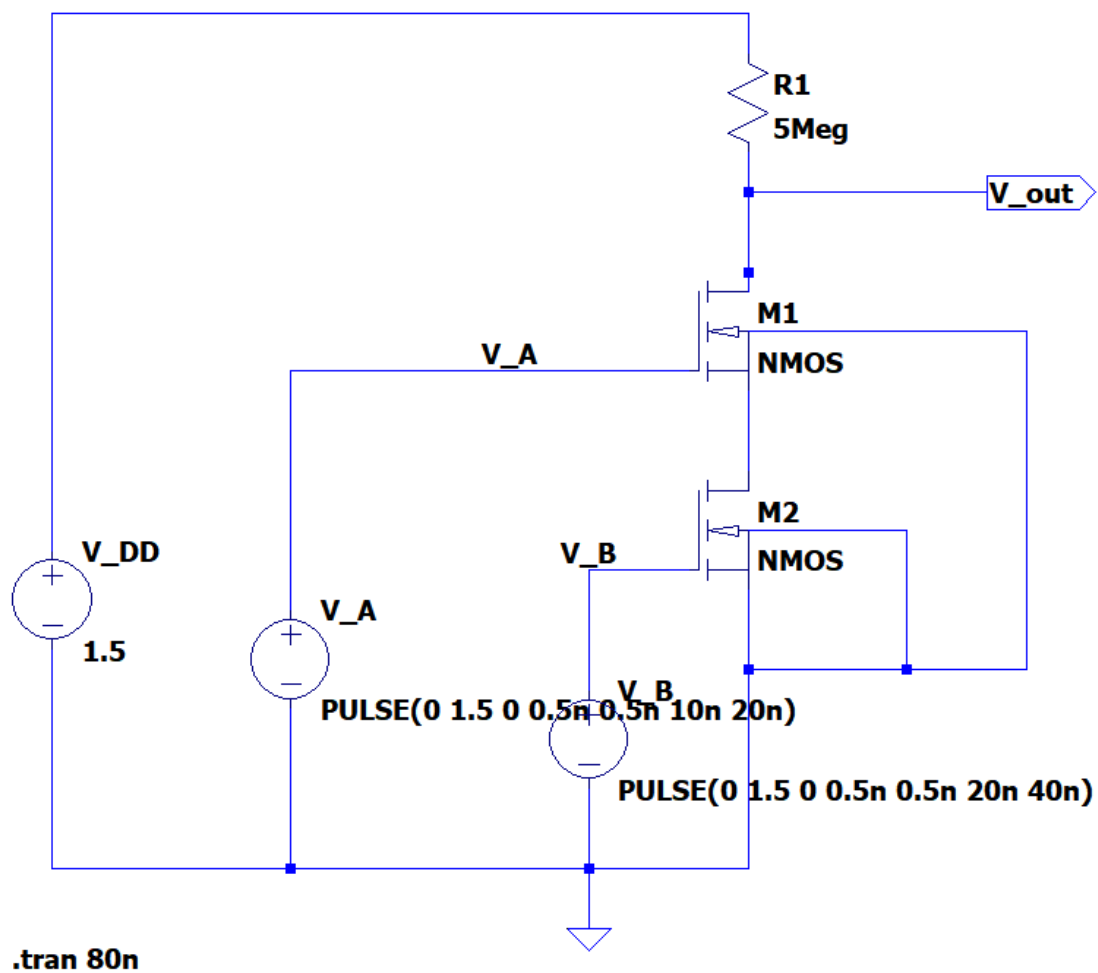| Vin	Vout
1	0
0	1

Conclusion:

From the graphs of task 1.1 and 1.2 we can observe that when input is low, output is high and when output is low input is high, this shows the functionality of NOT gate and satisfies the truth table.
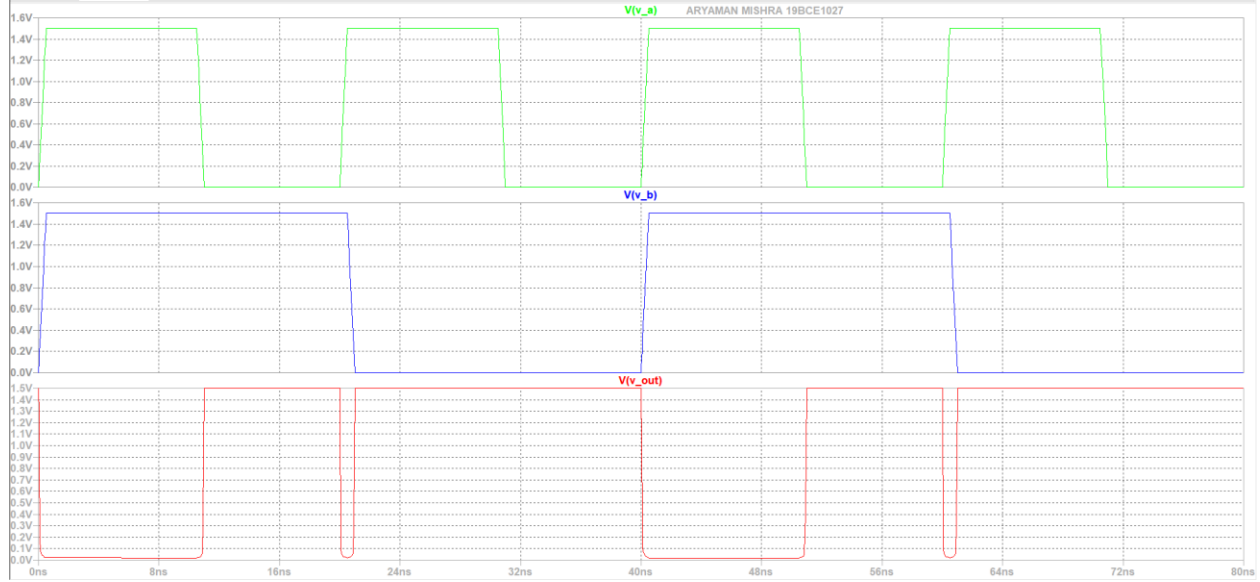
Task 2:

2.1: NAND GATE Using NMOS(NMOS4 symbol)
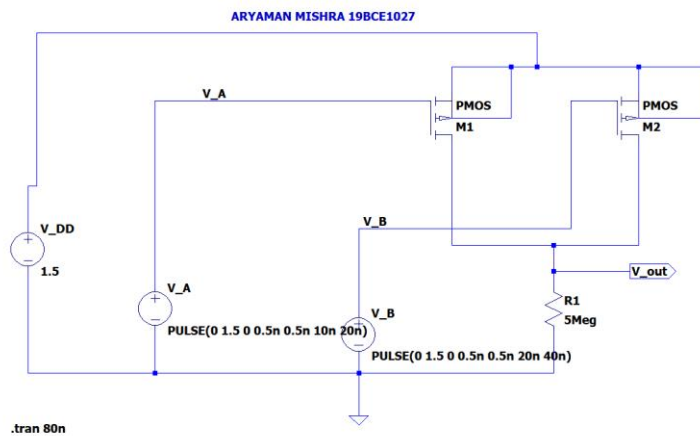
Circuit:

ARYAMAN MISHRA 19BCE1027

R1
5Meg

V_out

M1
V_A
NMOS
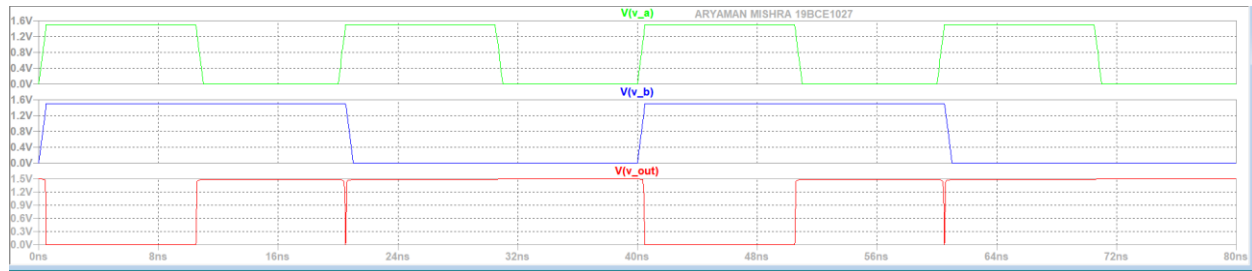
M2
V_DD   V_B   NMOS

V_A

1.5

V_B
PULSE(0 1.5 0 0.5n 0.5n 10n 20n)

PULSE(0 1.5 0 0.5n 0.5n 20n 40n)

.tran 80n

Output:

Truth Table:

V_A	V_B	V_out
0	0	1
0	1	1
1	0	1
1	1	0

2.2: NAND GATE Using PMOS (PMOS4 symbol)
Circuit:

Output:

Truth Table:

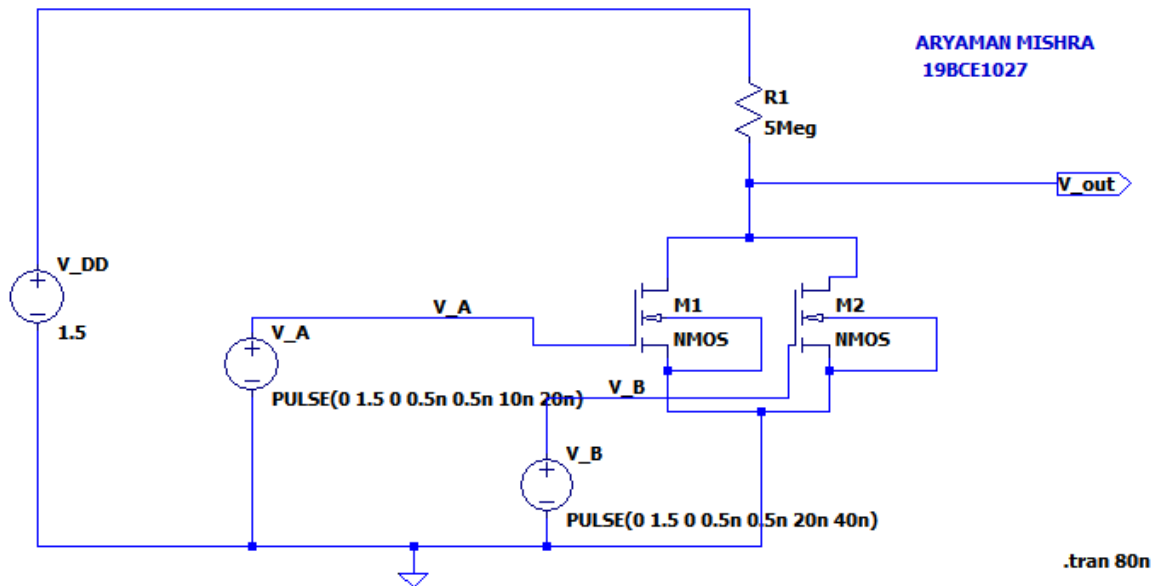| V_A	V_B	V_out
0	0	1
0	1	1
1	0	1
1	1	0

Conclusion:
From the graphs of task 2.1 and 2.2 we can observe that when both inputs are high, output is low while in all other cases it is high, this shows the functionality of NAND gate and satisfies the truth table.
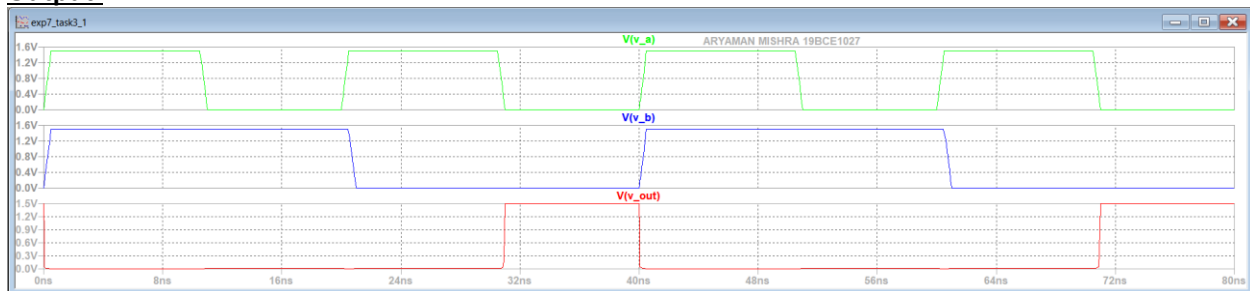
Task 3:
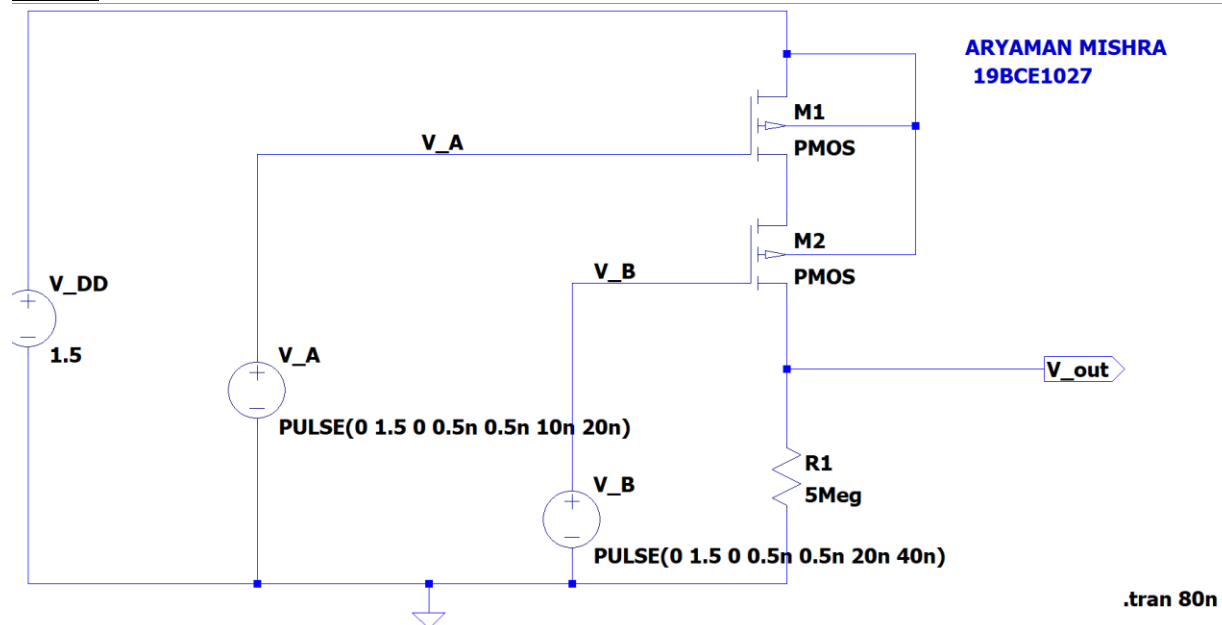**3.1: NOR GATE Using NMOS(NMOS4 symbol)**
Circuit:

Output:

Truth Table:

V_A	V_B	V_out
0	0	1
0	1	0
1	0	0
1	1	0

3.2: NOR GATE Using NMOS (NMOS4 symbol)
Circuit:

ARYAMAN MISHRA
19BCE1027

M1
PMOS

V_A

M2
PMOS

V_B

V_DD

1.5

V_A

PULSE(0 1.5 0 0.5n 0.5n 10n 20n)

V_B

V_out

R1
5Meg

V_B

PULSE(0 1.5 0 0.5n 0.5n 20n 40n)

.tran 80n
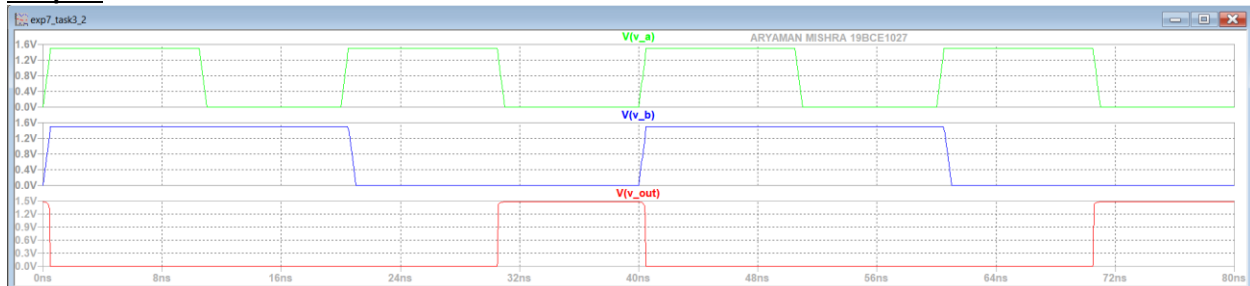
Output:

Truth Table:

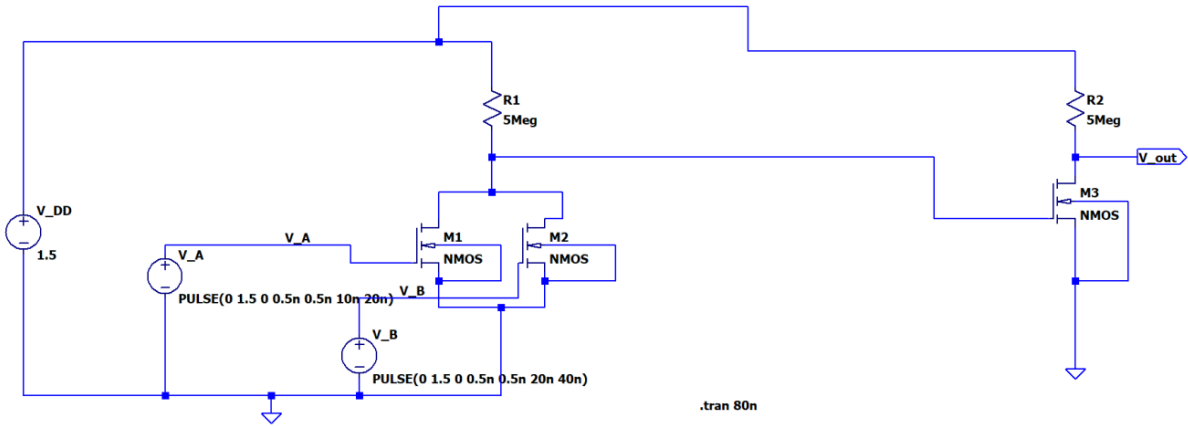| V_A	V_B	V_out
0	0	1
0	1	0
1	0	0
1	1	0

Conclusion:
From the graphs of task 3.1 and 3.2 we can observe that when both inputs are low, output is high while in all other cases it is low, this shows the functionality of NOR gate and satisfies the truth table.
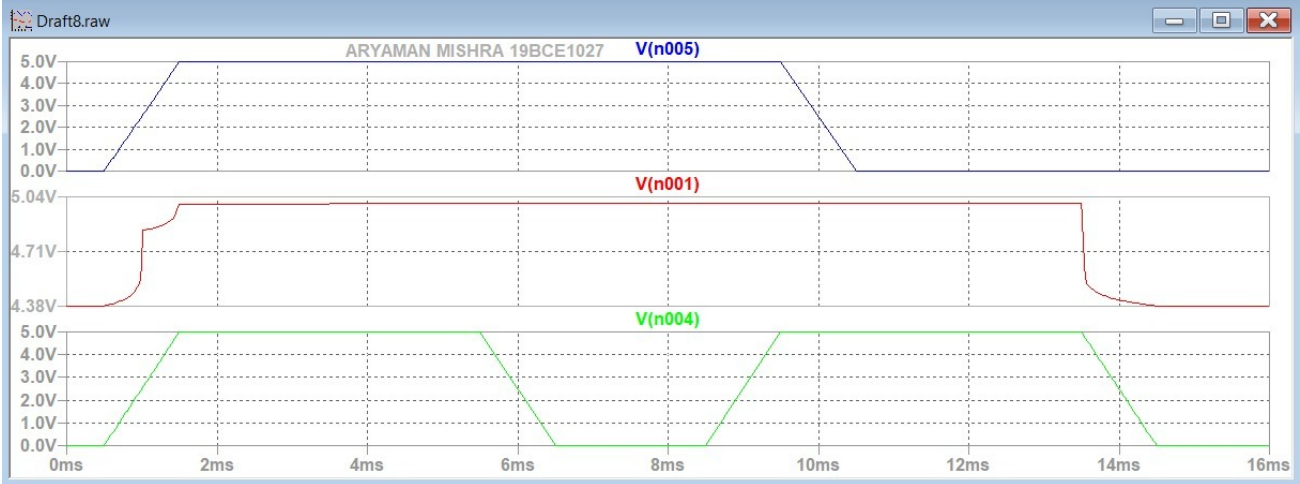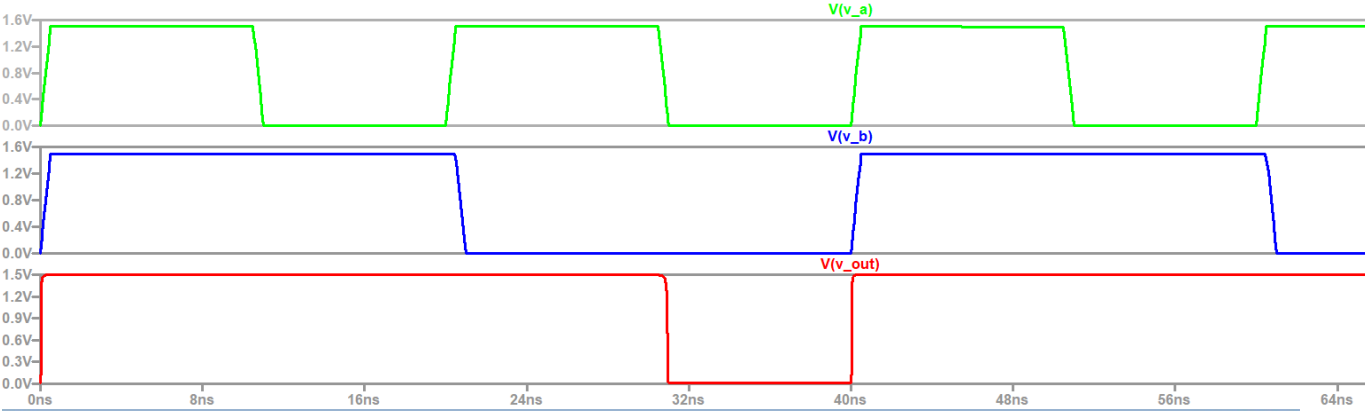
Task 4: OR GATE using NMOS (NMOS4 symbol)
Circuit :

R1
5Meg

R2
5Meg

V_out

M3
NMOS

V_DD

1.5

V_A

M1
NMOS

M2
NMOS

V_A

PULSE(0 1.5 0 0.5n 0.5n 10n 20n)

V_B

V_B

PULSE(0 1.5 0 0.5n 0.5n 20n 40n)

.tran 80n

Output:

V(v_a)

V(v_b)

V(v_out)

0ns   8ns   16ns   24ns   32ns   40ns   48ns   56ns   64ns

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V(n005)

V(n001)

V(n004)

0ms   2ms   4ms   6ms   8ms   10ms   12ms   14ms   16ms

Truth Table:

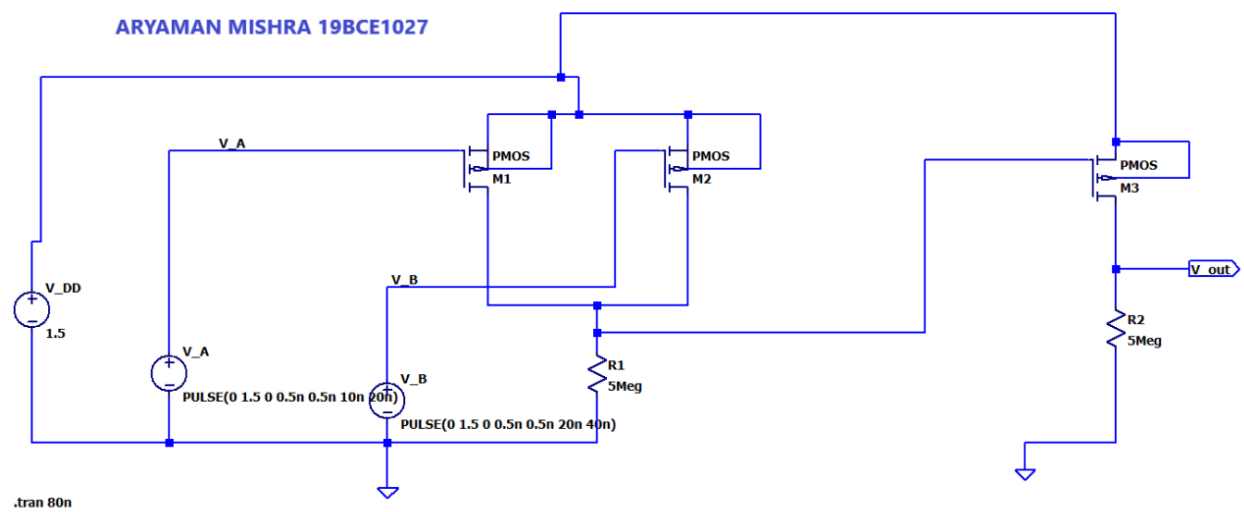| V_A	V_B	V_out
0	0	0

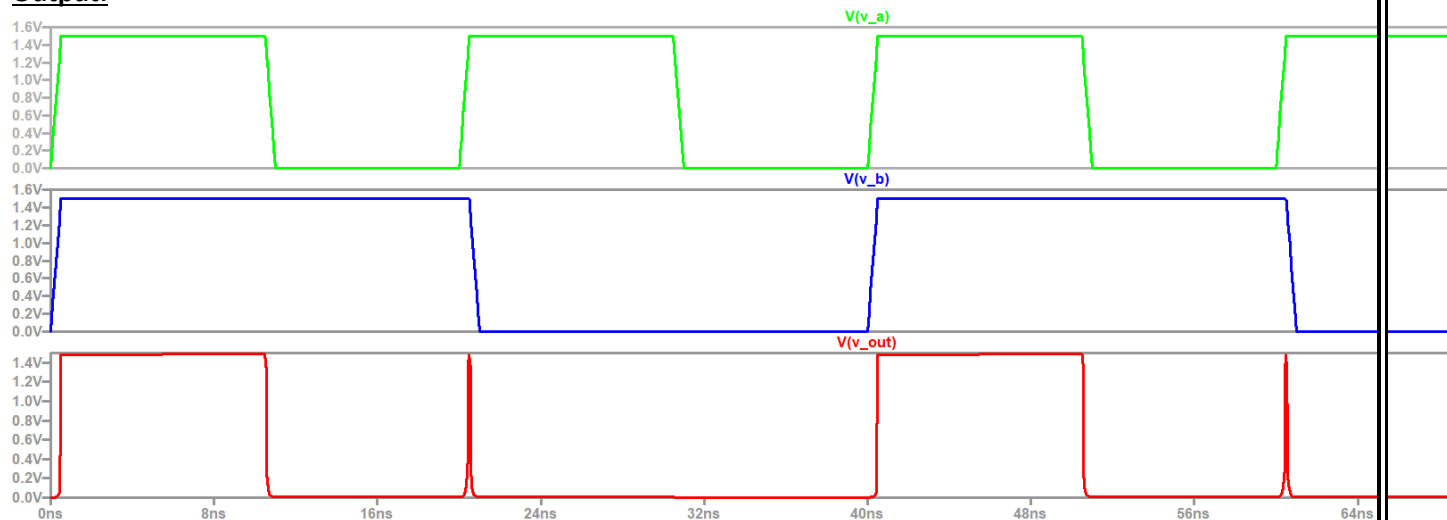|		
0	1	1
1	0	1
1	1	1

Conclusion:

From the graphs of we can observe that when both inputs are low, output is high while in all other cases it is high, this shows the functionality of OR gate and satisfies the truth table.

Task 5: AND GATE using PMOS(PMOS4 symbol)
Circuit:

ARYAMAN MISHRA 19BCE1027

Output:

Truth Table:

V_A	V_B	V_out

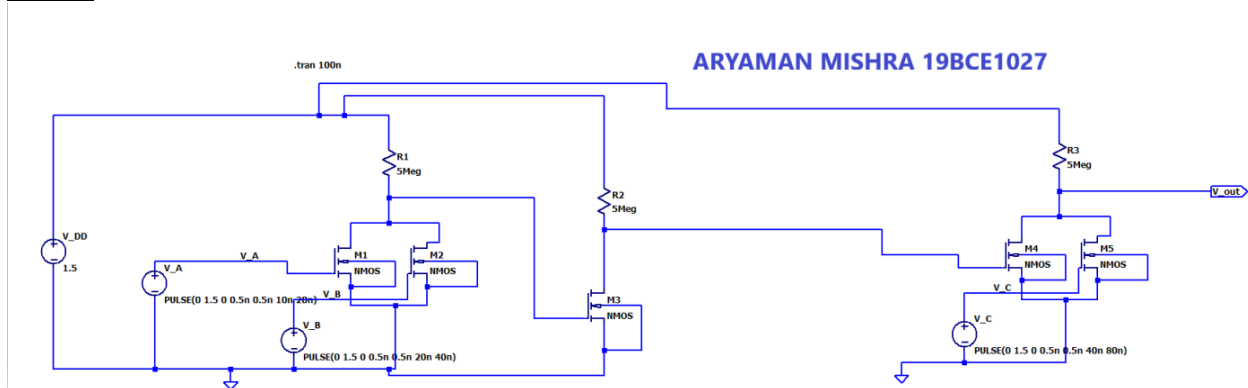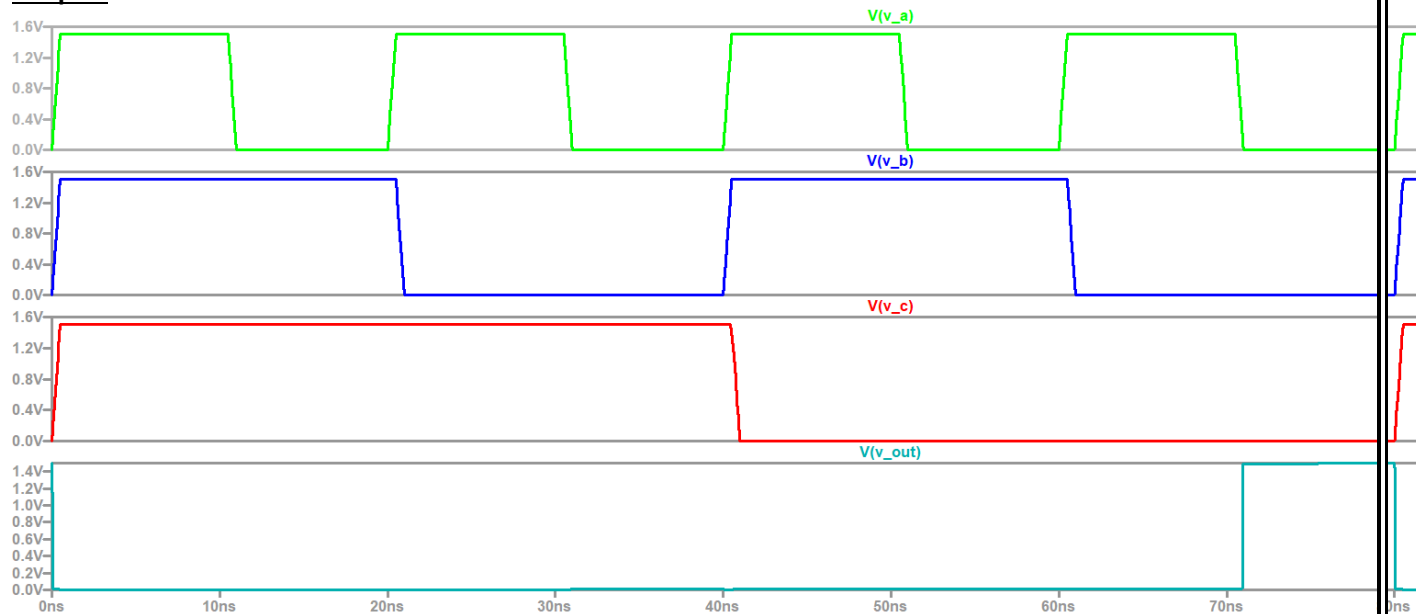| 0	0	0
0	1	0
1	0	0
1	1	1

Conclusion:

From the graphs of we can observe that when both inputs are high, output is high while in all other cases it is low, this shows the functionality of AND gate and satisfies the truth table.

Task 6: LOGIC using NMOS(NMOS4 symbol)
Circuit:

ARYAMAN MISHRA 19BCE1027

Output:

Truth Table:

V_A	V_B	V_C	V_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Conclusion:

From the graphs of we can observe that when all three inputs are high, output is high while in all other cases it is low, this shows the functionality of the given Boolean function $Y = A + B \cdot C$ and satisfies the truth table.