6. Design of Logic gates using Complementary MOSFET (CMOS)

Course: ECE1008 – Electronic Hardware Troubleshooting LAB

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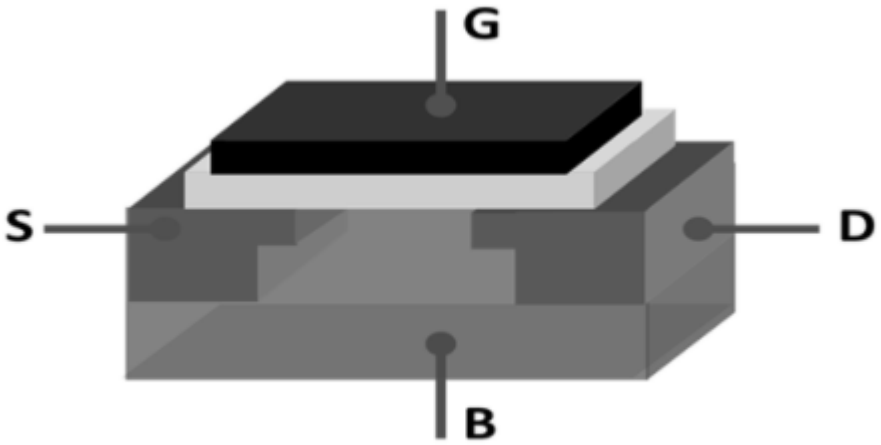
CHENNAI

1. MOSFET

- Metal Oxide Semiconductor Field Effect Transistor
- MOSFET is a semiconductor device used for
  - switching purposes
  - Amplification of electronic signals in electronic devices
- Since MOSFETs are available in very small sizes, they are used in integrated circuits.

1. MOSFET

- Four terminal device –> (3 terminal device)
- Source (S)
- Drain (D)
- Gate (G)
- Body (B) which is in connection with source

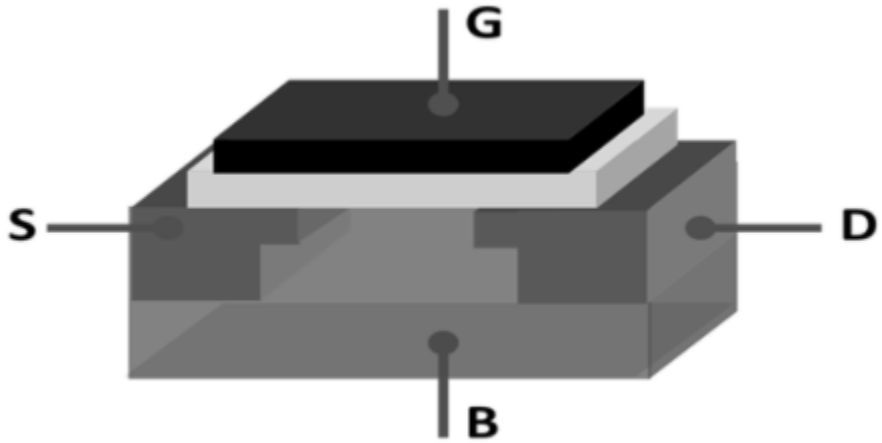


MOSFET

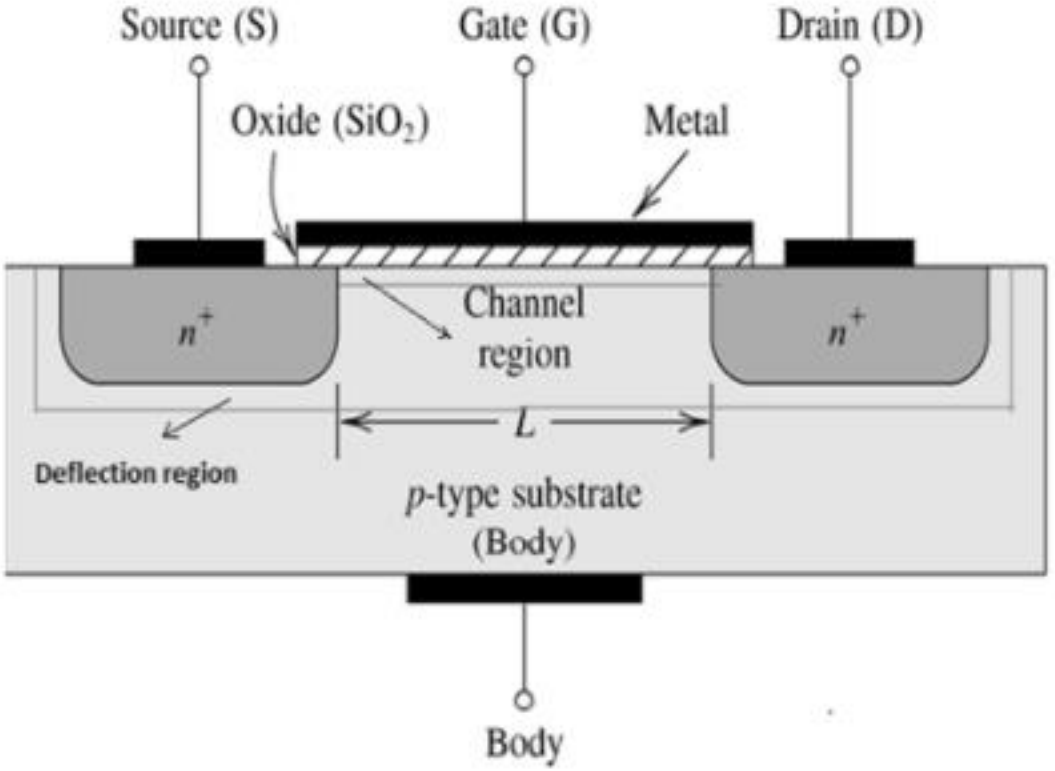
- Functionality depends on
  the electrical variations in the channel width along with
  the flow of carriers (either holes or electrons)
- The charge carriers enter into the channel through the source terminal and exit via the drain.

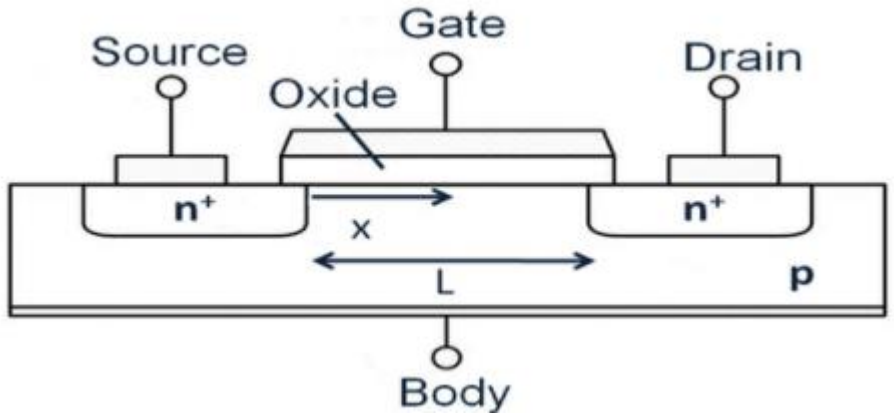
1. MOSFET

- Width of channel
  (controlled by voltage at Gate – which is between source and drain)
- Metal oxide layer (extremely thin and insulated)



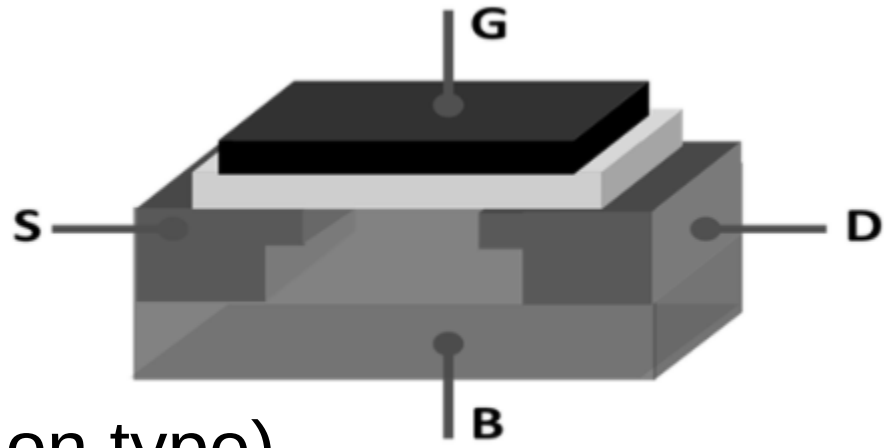
MOSFET



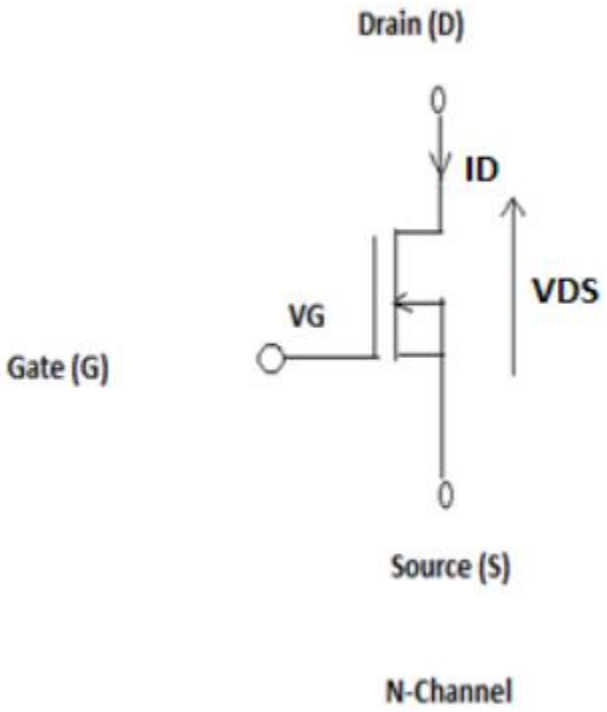


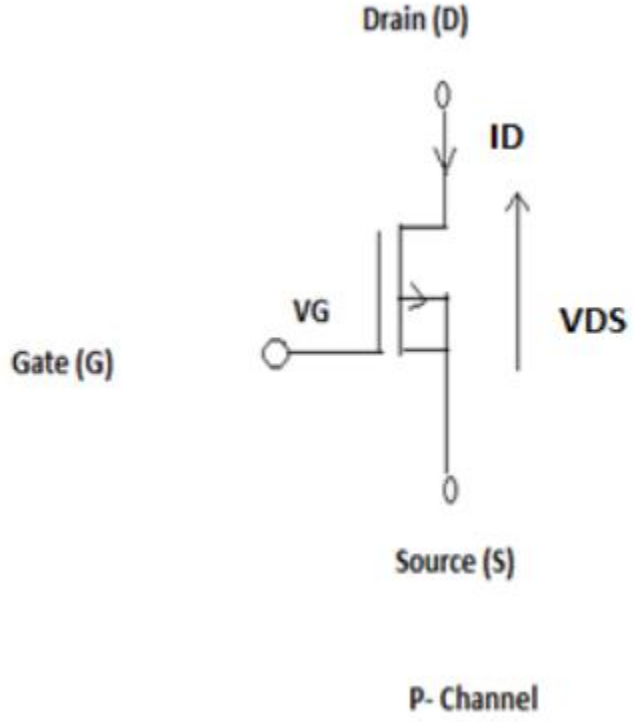
1.1 MOSFET functionality

- Depletion mode
  a) No voltage across gate terminal
  Channel – Maximum conductance
  b) If gate voltage is positive/negative (based on type)
  Channel conductivity decreases

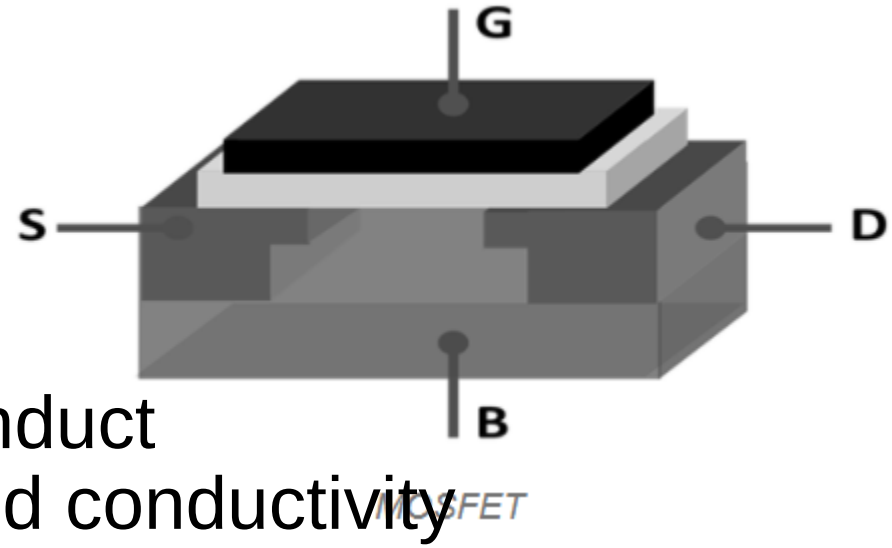


MOSFET

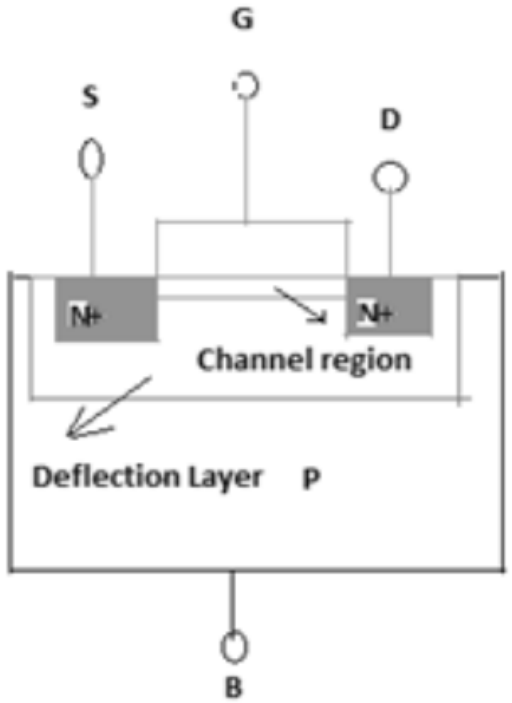


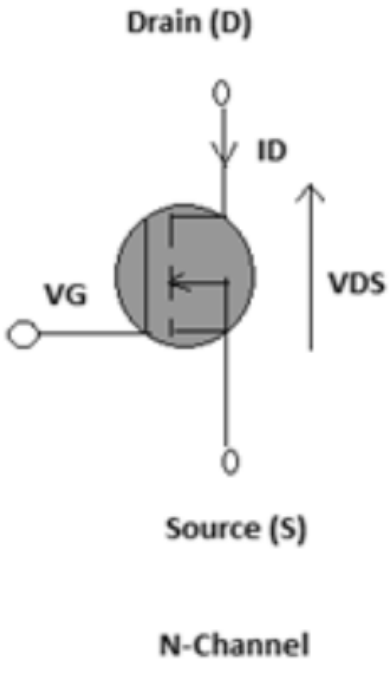


1.1 MOSFET functionality



- Depletion mode
- Enhancement mode
  No voltage across gate: Device does not conduct
  Maximum gate voltage: Device has enhanced conductivity



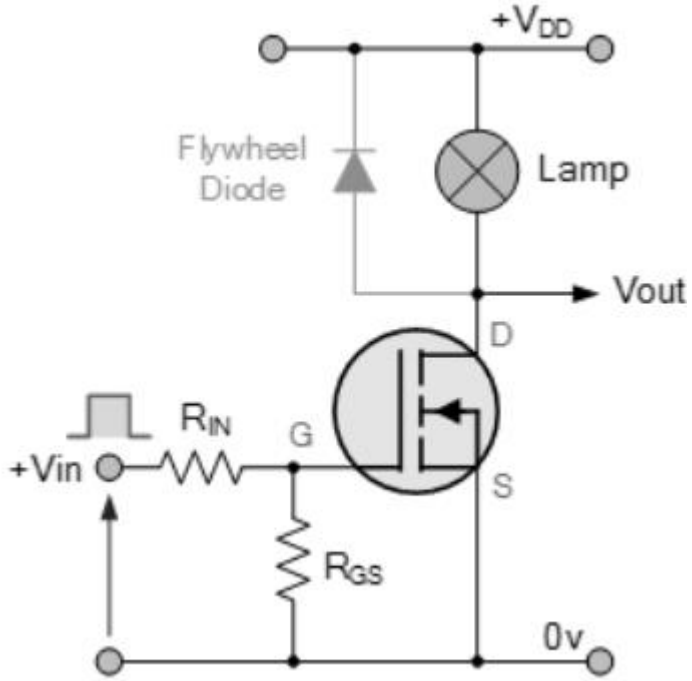


2.1 Practical switch characteristics

- ON condition: Power management abilities should be limited (flow of conduction current has to be restricted)
- OFF state: Blocking voltage levels should not be limited
- Turning ON and OFF with finite times – restricts limiting speed of device and limits function frequency
- ON: Minimal resistance values (Voltage drop in forward bias)
- OFF: Finite off resistance delivering reverse leakage current
- Loses power in ON and OFF states

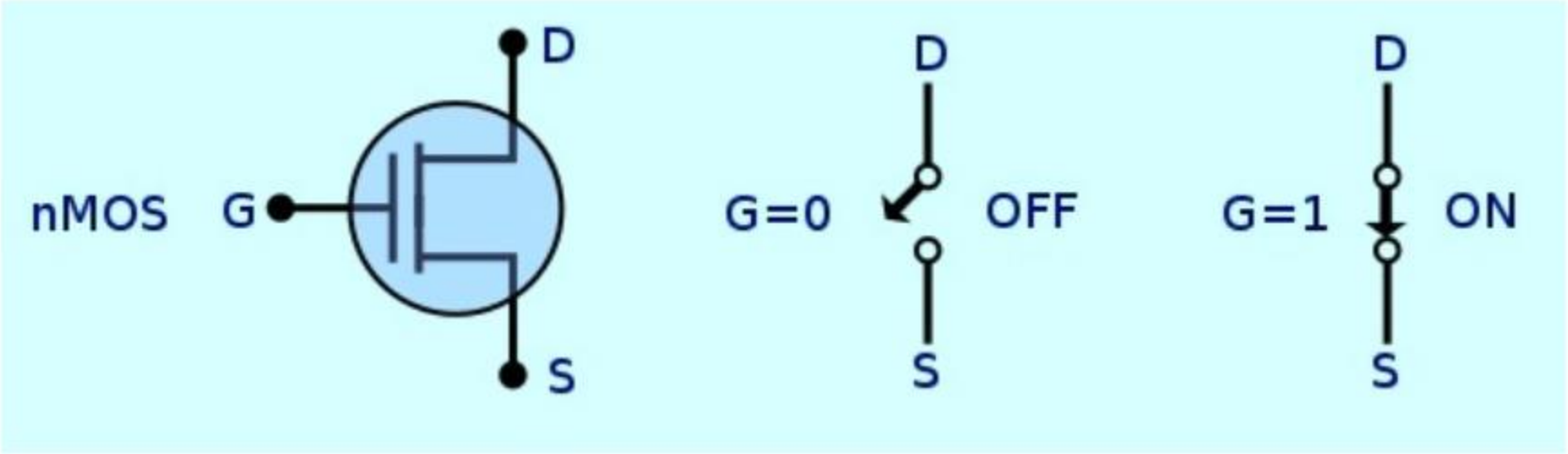
2.2 Example of MOSFET as switch

- Enhancement mode and N Channel MOSFET for switch operation
- Positive input voltage -> Gate terminal positive
  -> Lamp moves to ON condition
- Zero input voltage -> Gate terminal at zero volts
  -> Device turns OFF

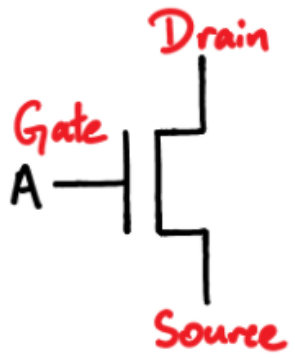


3.1 NMOS (n-type source and drain)

- n-type source and drain
- P-type substrate(body)
- When voltage is applied to gate: Holes in body are driven away from gate
- n-type channel is formed between source and drain



3.1 NMOS (n-type source and drain)

MOSFET Type	Logic Circuit Symbol	$A = 0$ Approximation	$A = 1$ Approximation
NMOS			

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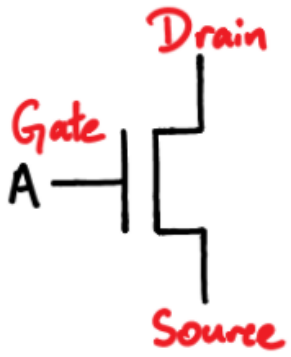
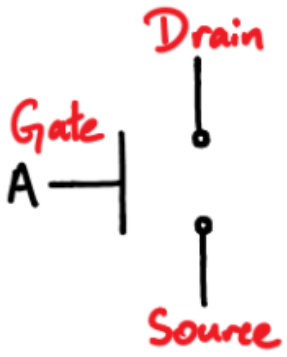
NMOS			

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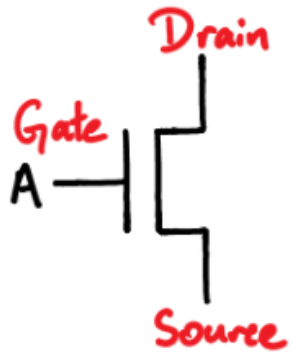
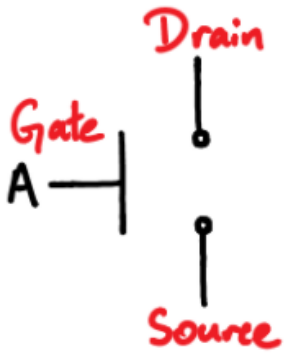
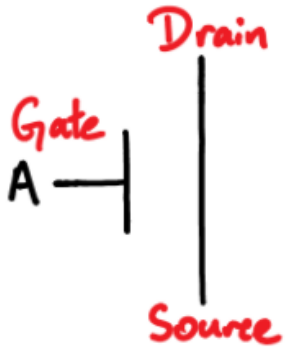
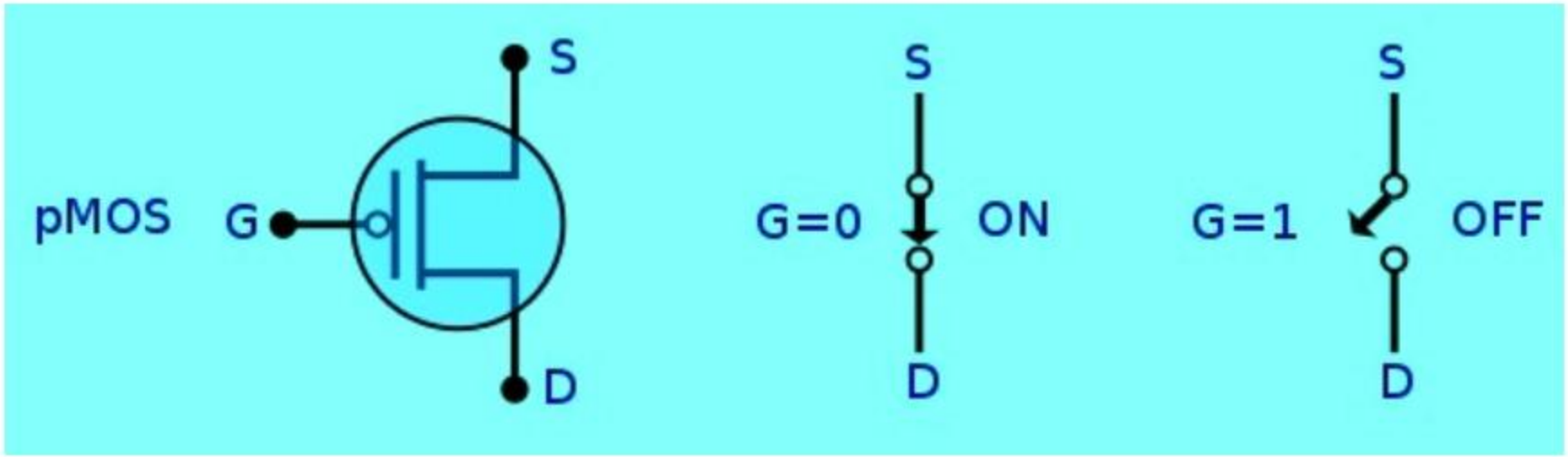
NMOS			

3.2 PMOS (p-type source and drain)

- p-type source and drain
- P-type substrate(body)
- When voltage is applied to gate: (Negative voltage between G and S) Electrons in body are driven away from gate
- p-type channel is formed between source and drain



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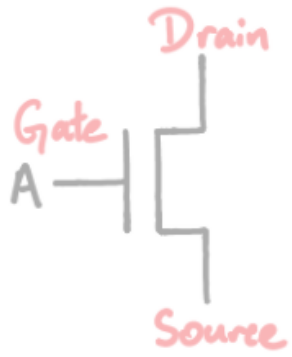
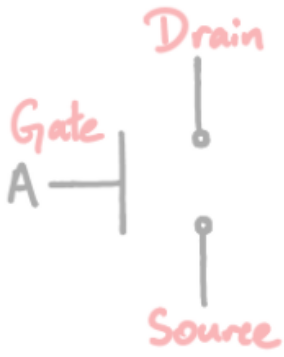
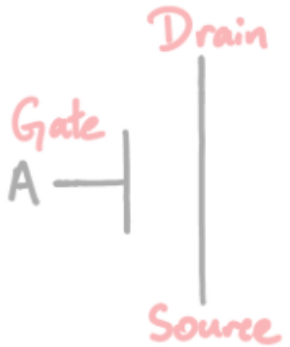
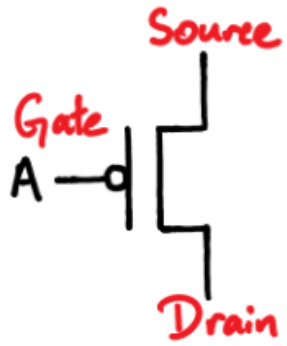
NMOS			
PMOS			

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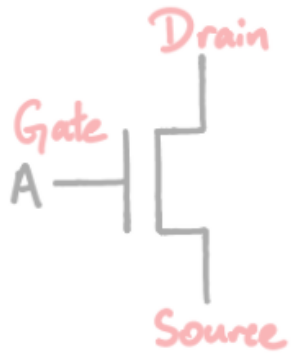
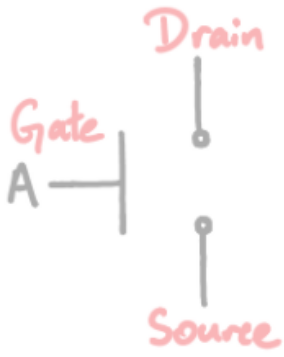
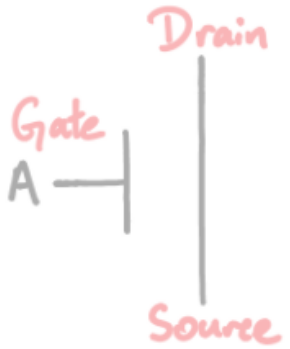
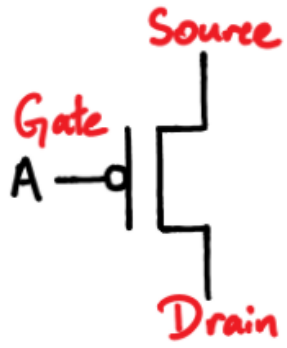
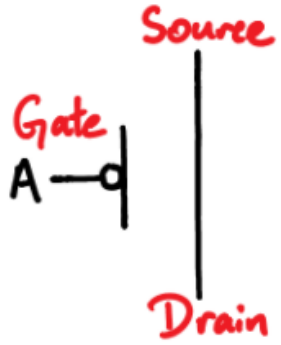
NMOS			
PMOS			

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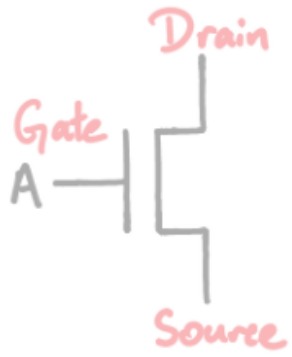
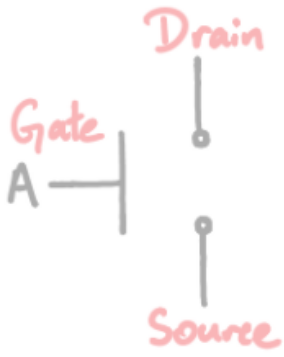
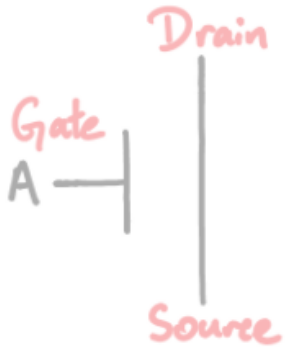
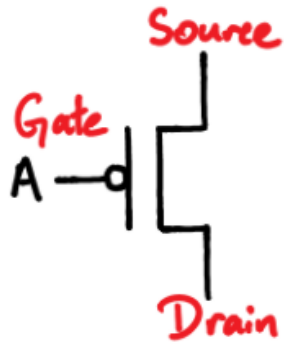
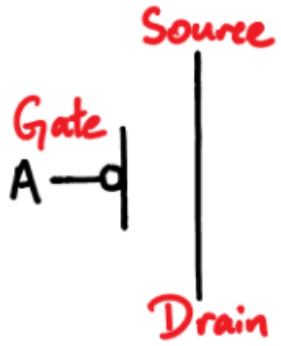
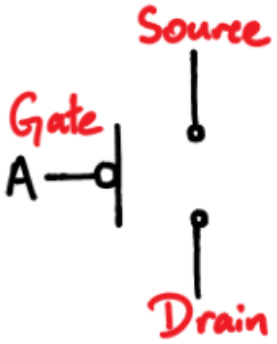
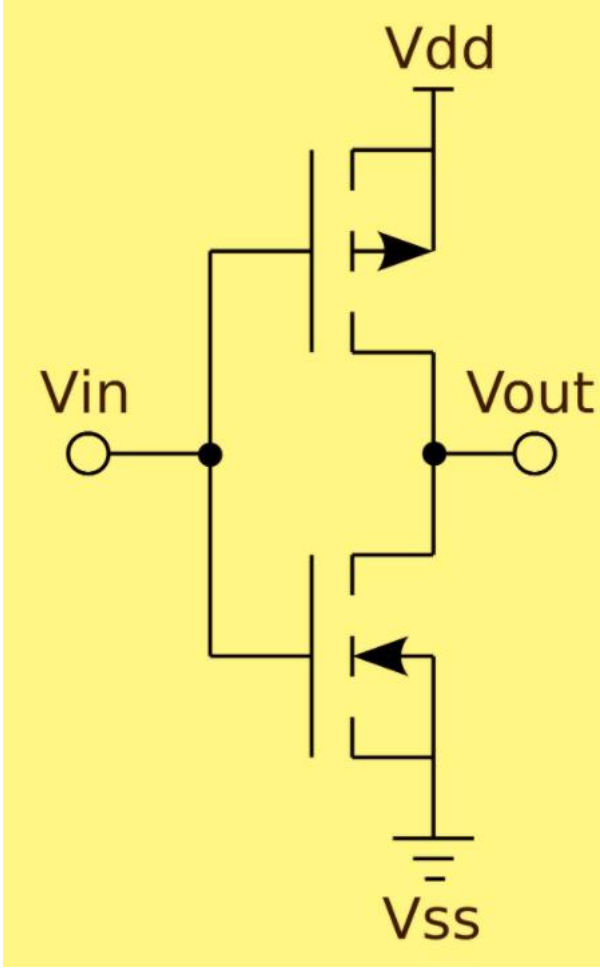
NMOS			
PMOS			

3.3 CMOS

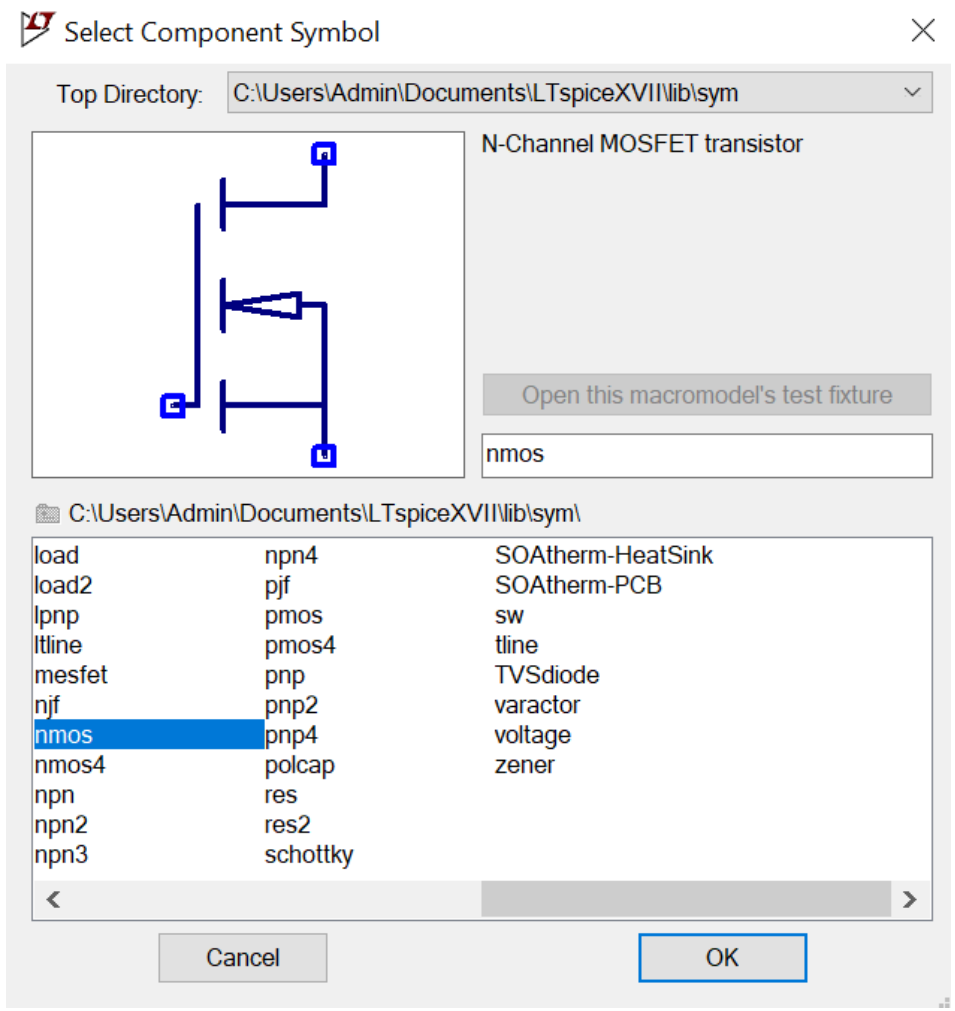
- Complementary Metal Oxide Semiconductor (CMOS) is an integrated circuit technology (process technology)
- Applications: Microprocessors, microcontrollers, static RAM, other digital circuits
- Analog circuits: Image sensors (CMOS sensor), data converters, highly integrated transceivers
- Uses PMOS and NMOS

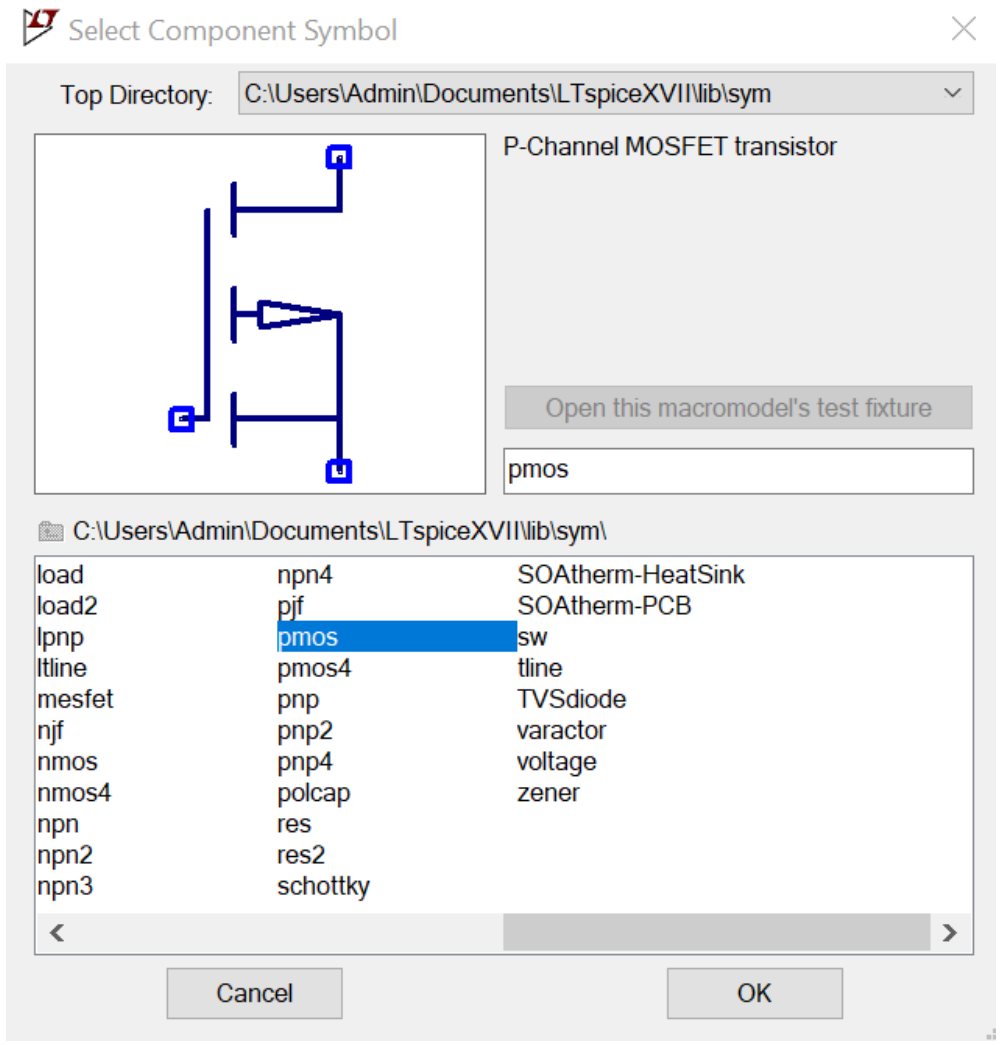


3.3 CMOS: Advantages

- Both low to high and high to low transitions are fast
- Output signal oscillates the full voltage between low and high rail

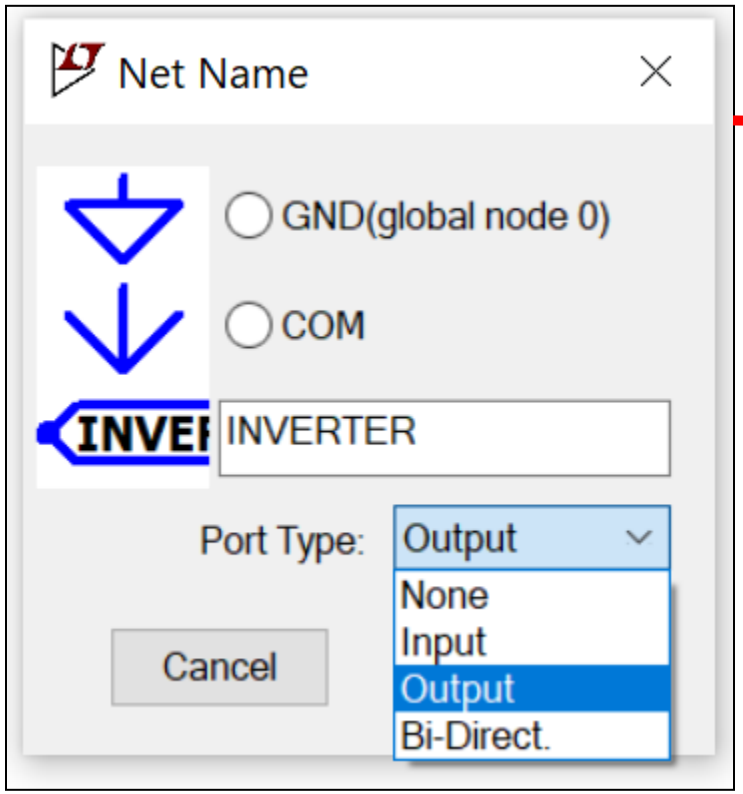
Task 1: Implementation of Inverter

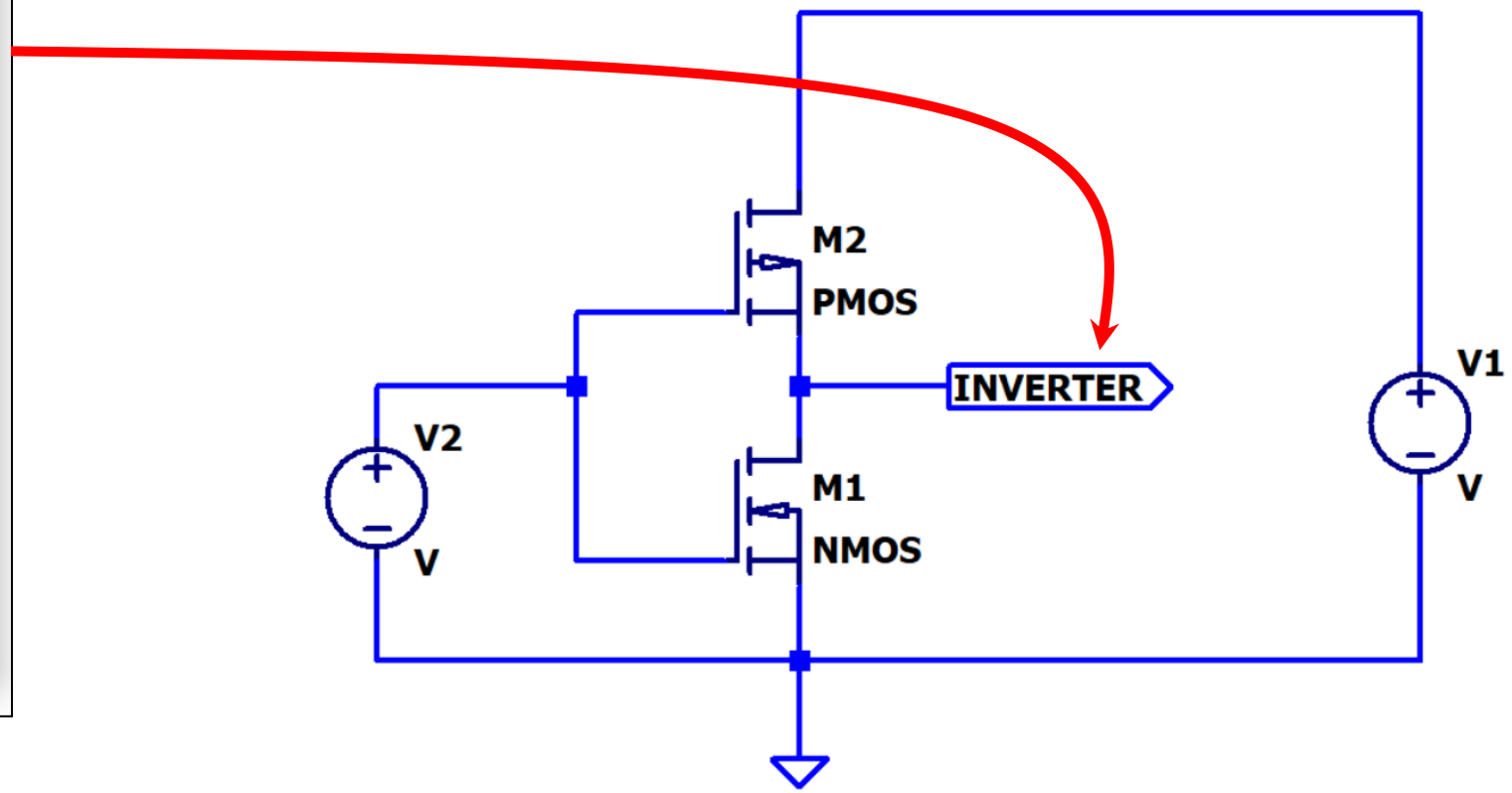




Task 1: Implementation of Inverter

- Edit-> Label net





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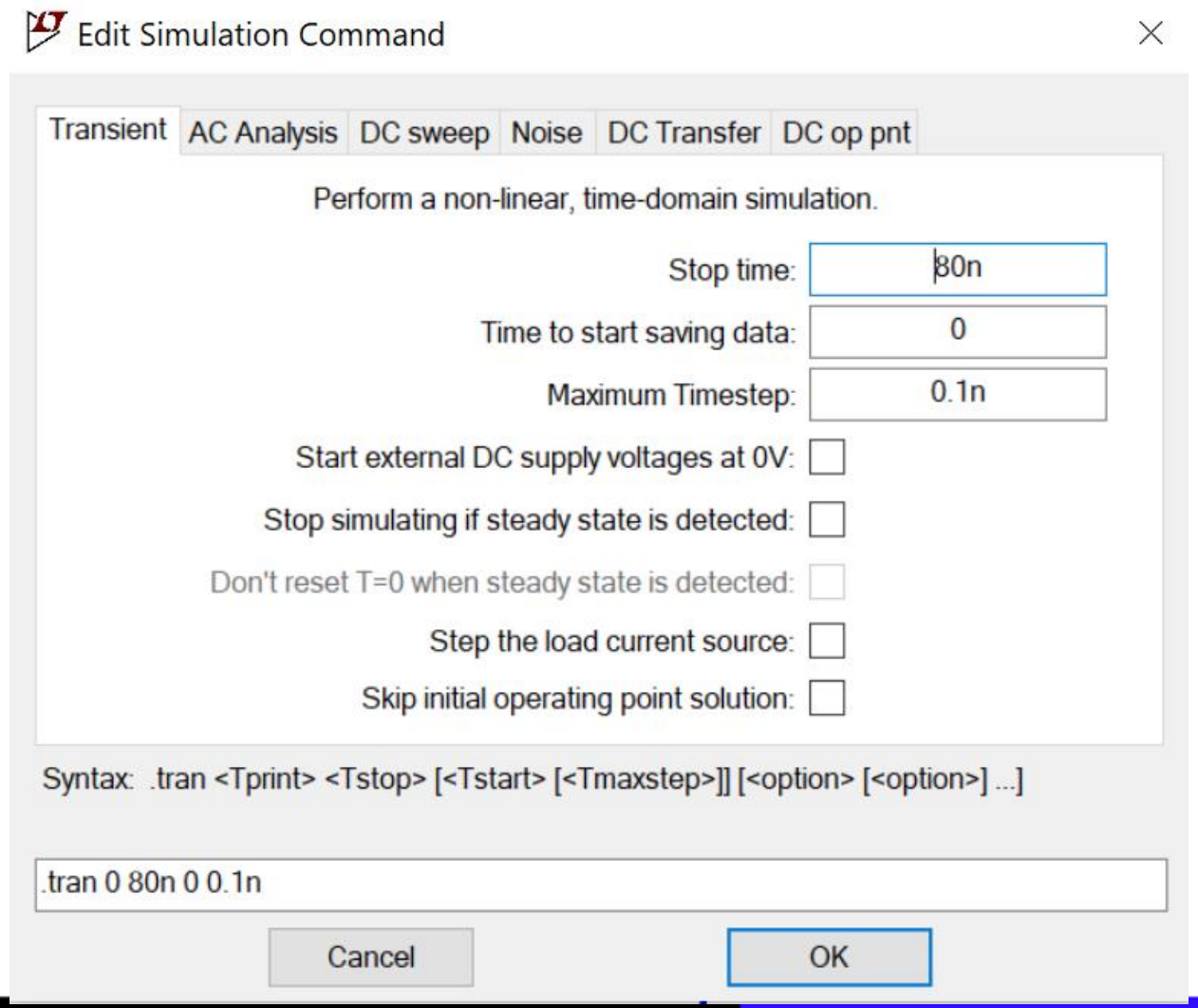
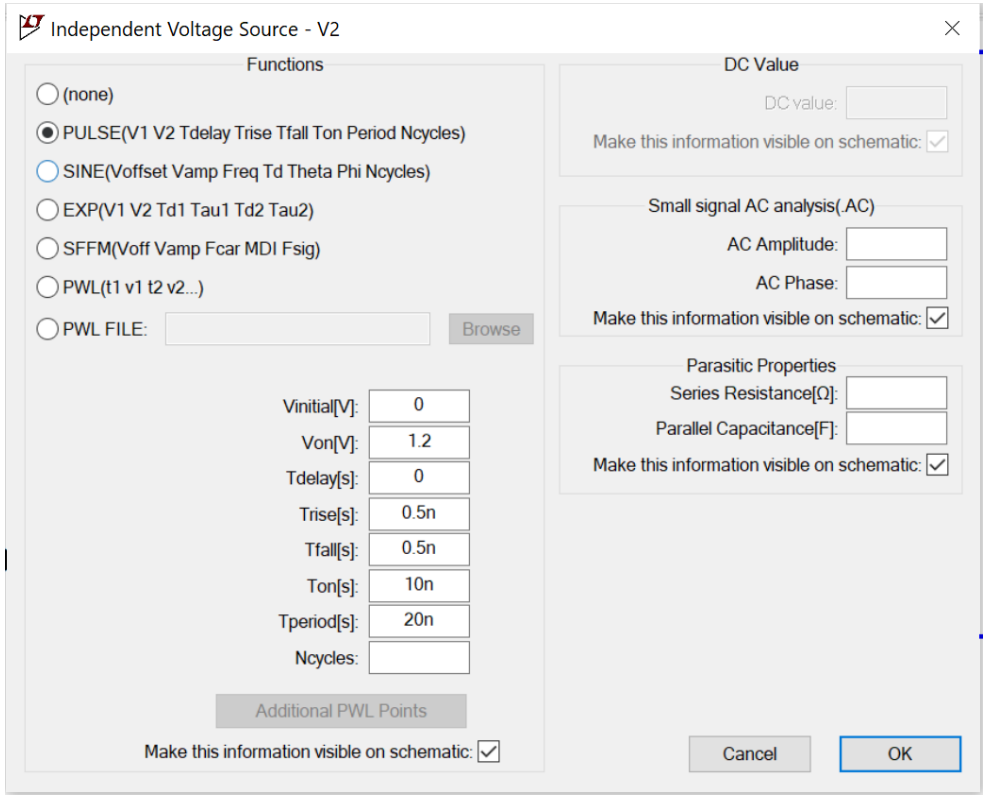
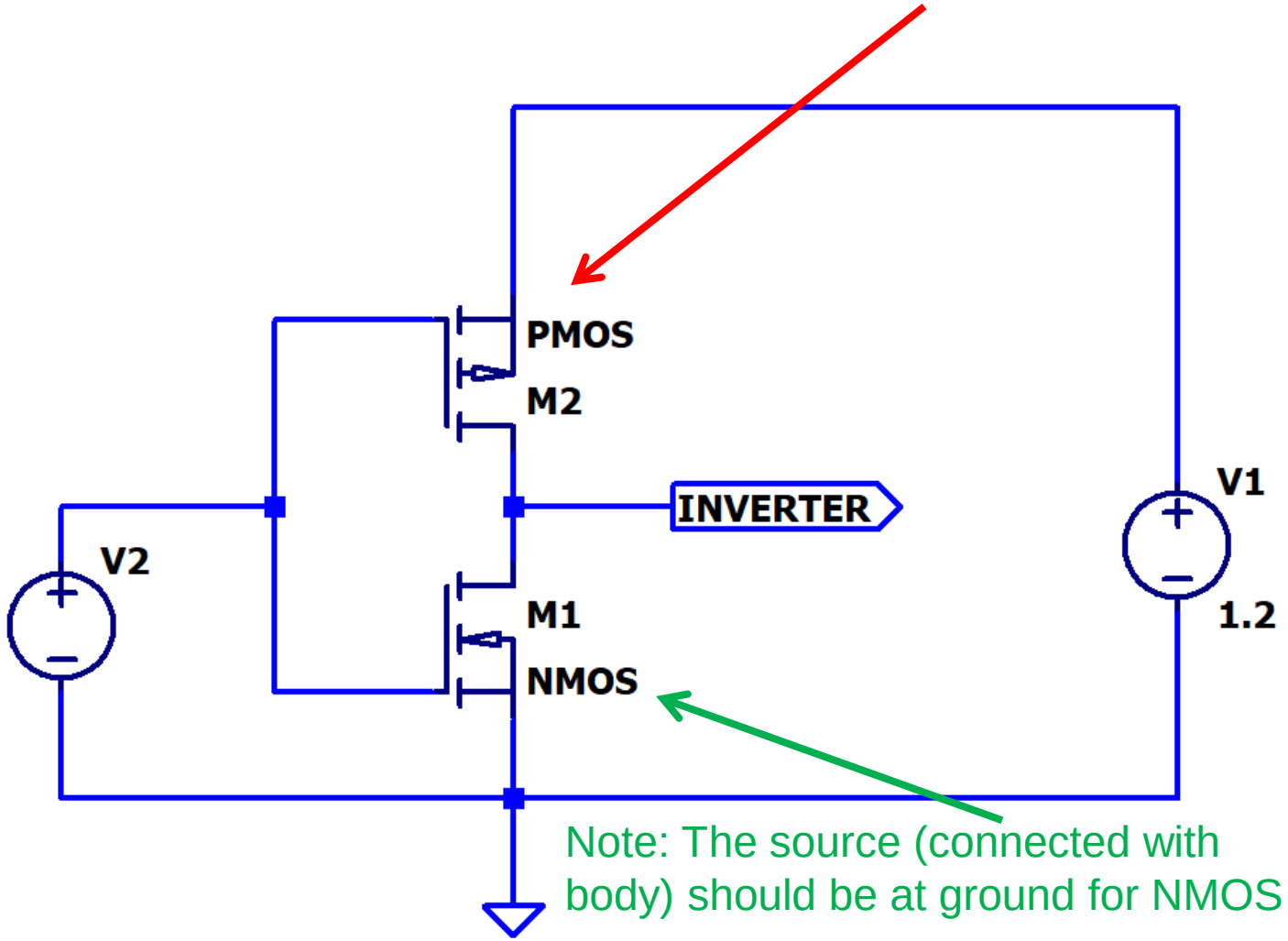


Task 1: Implementation of Inverter

Note: The source (connected with body) should be at supply for PMOS





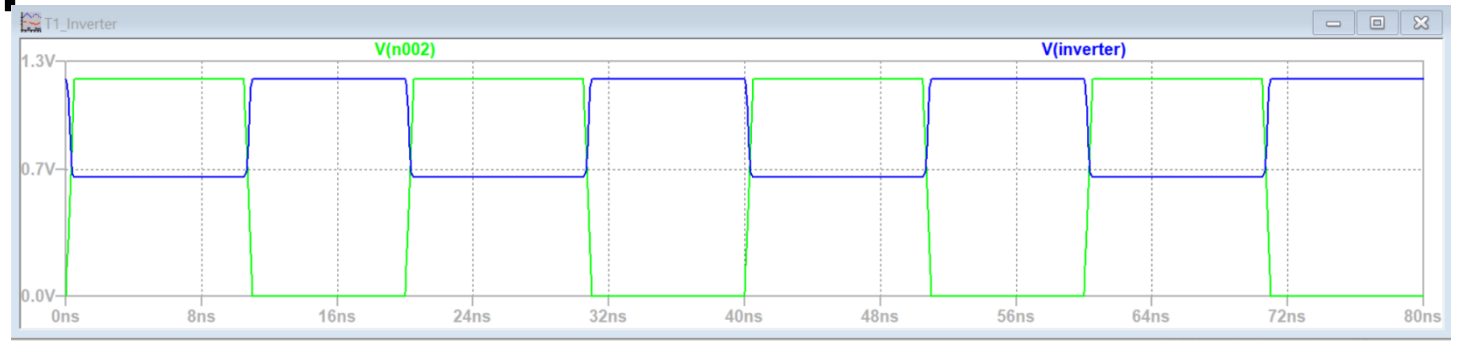
PULSE(0 1.2 0 0.5n 0.5n 10n 20n)

Note: The source (connected with body) should be at ground for NMOS

.tran 0 80n 0 0.1n

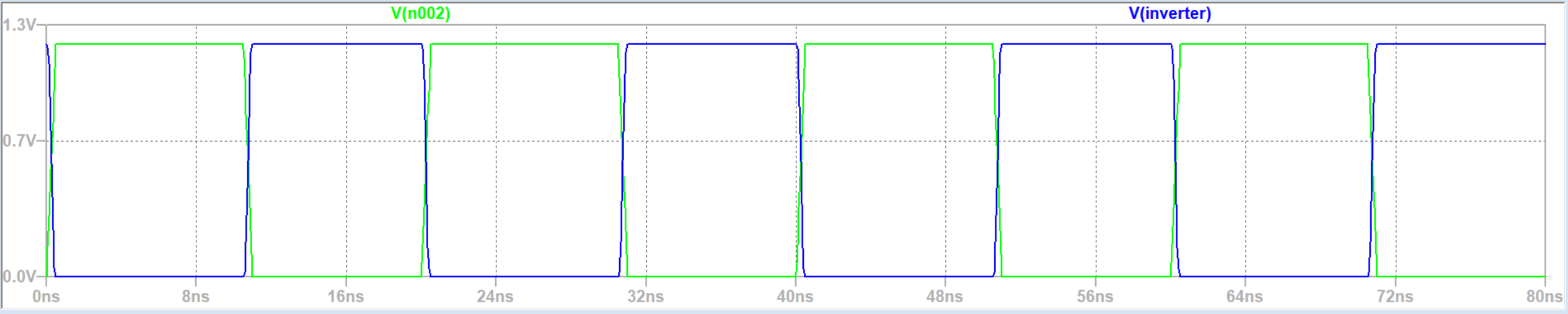
Task 1: Implementation of Inverter

- Wrong Output:



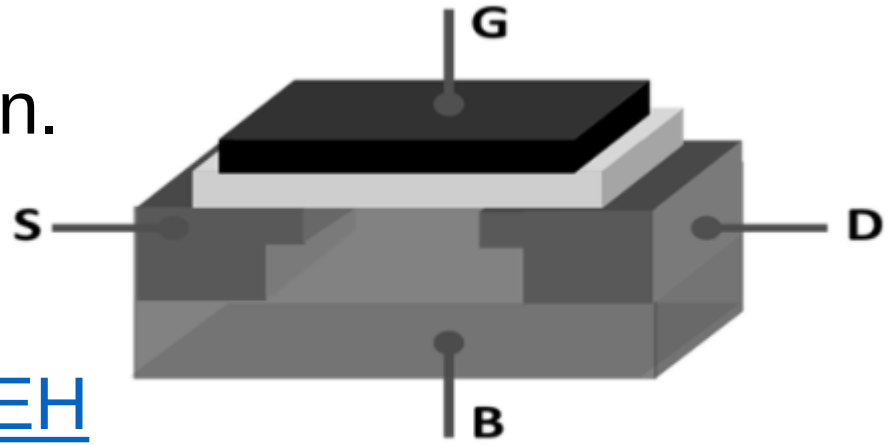
Does not contain true low
Check orientation of PMOS and NMOS in previous slide.

- **Correct output**:



This step is for all logic gates using CMOSP and CMOSN

- CMOS has CMOSN and CMOSP as PMOS and NMOS configuration with an additional option of selecting separate body connection.

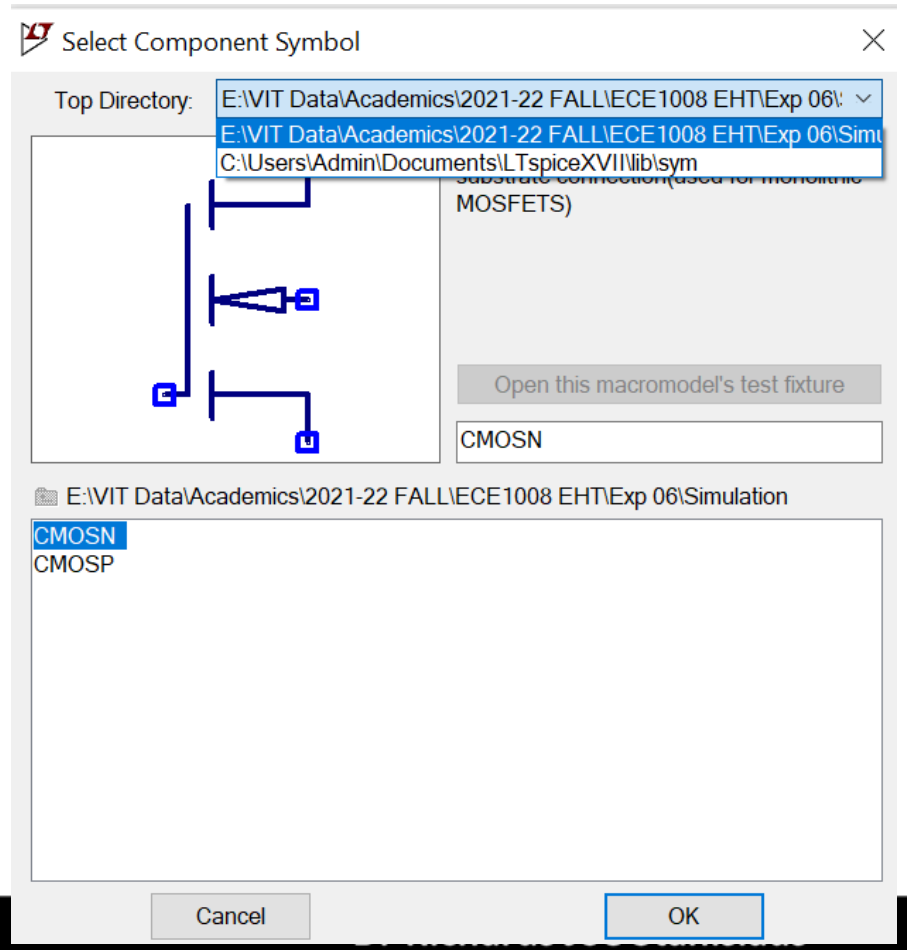


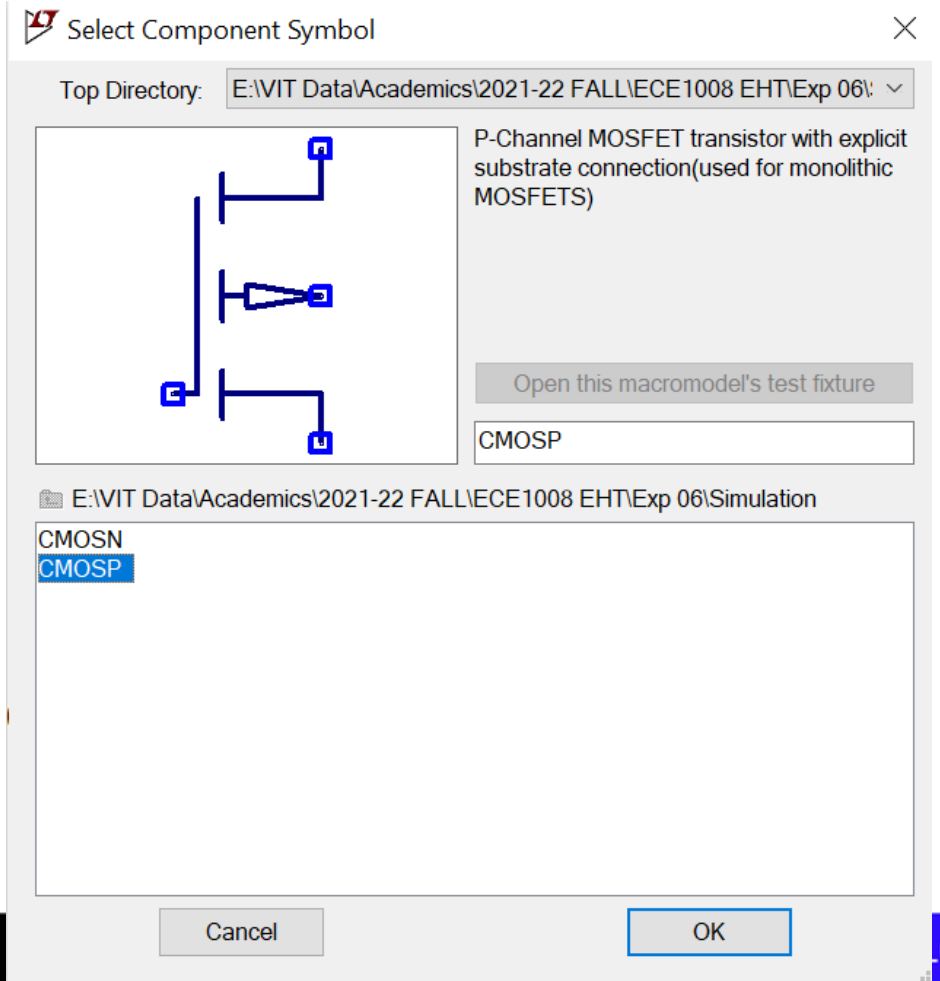
MOSFET

- Download the files from https://drive.google.com/drive/folders/1i2rQEHsiQ-Fp3v2wIlZP3EiMy_MBpy3l?usp=sharing
- Save all four files in same folder as the simulation file's folder

Task 2: Implementation of Inverter using CMOS

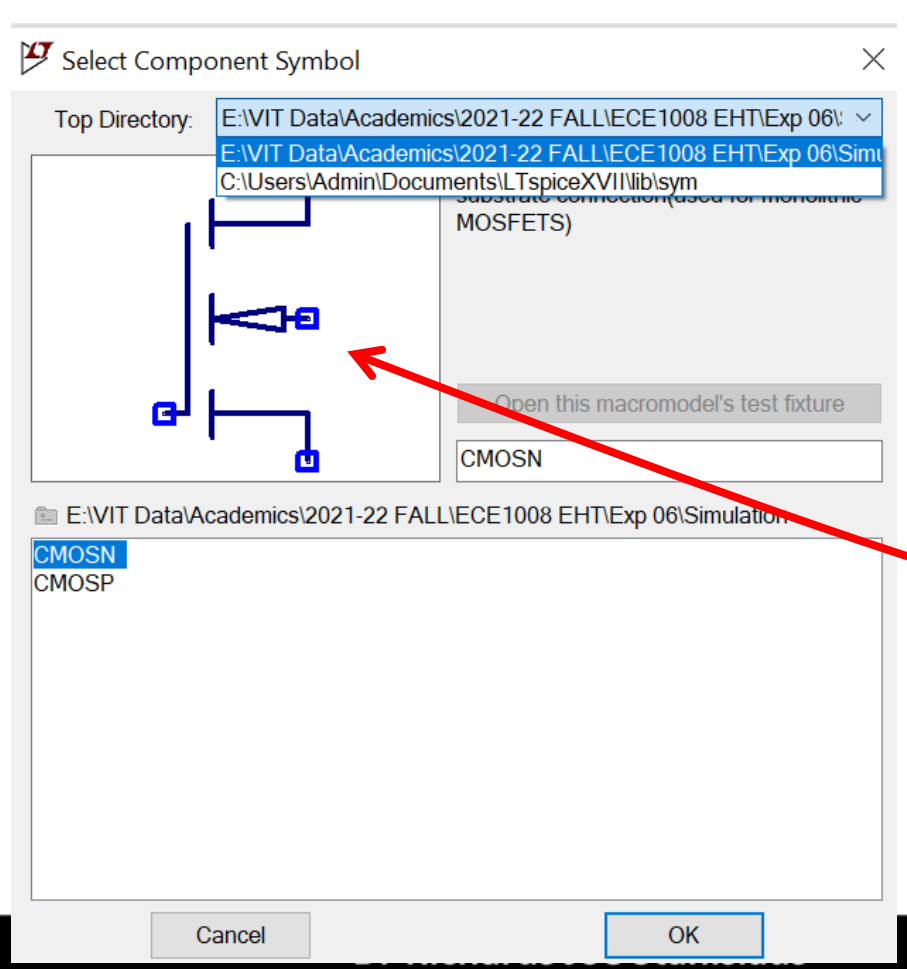
- Once the steps in previous slides are completed, select component and choose the current folder to select CMOSN and CMOSP.

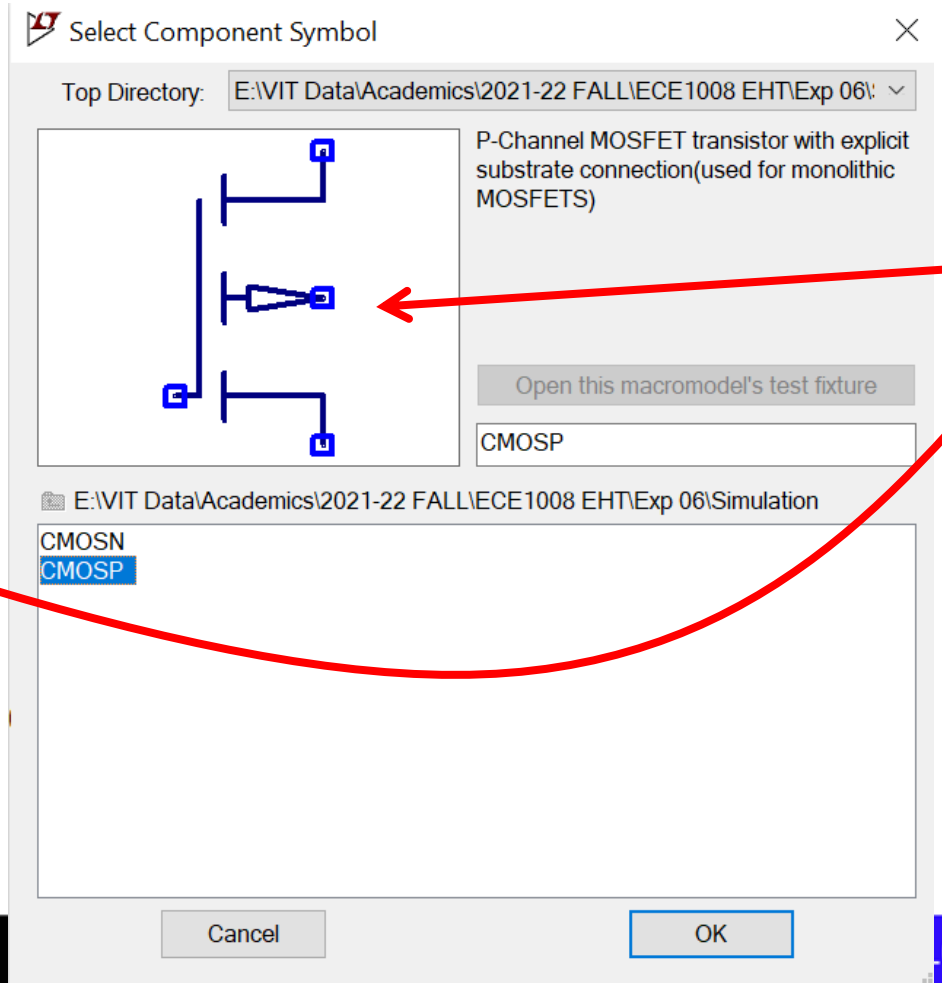




Task 2: Implementation of Inverter using CMOS

- Once the steps in previous slides are completed, select component and choose the current folder to select CMOSN and CMOSP.

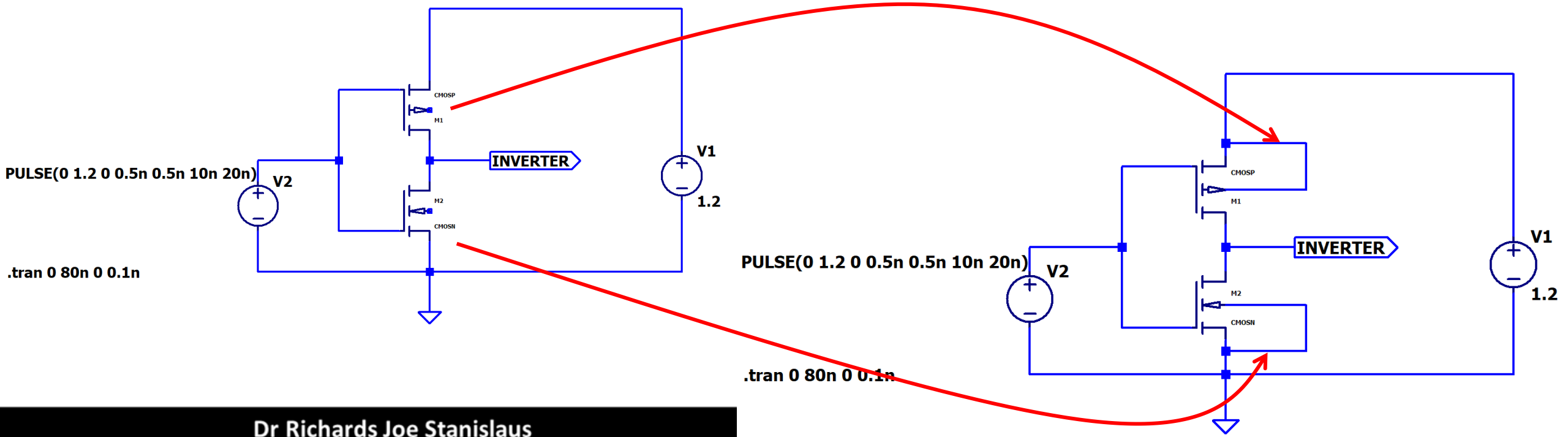




Separate body connection

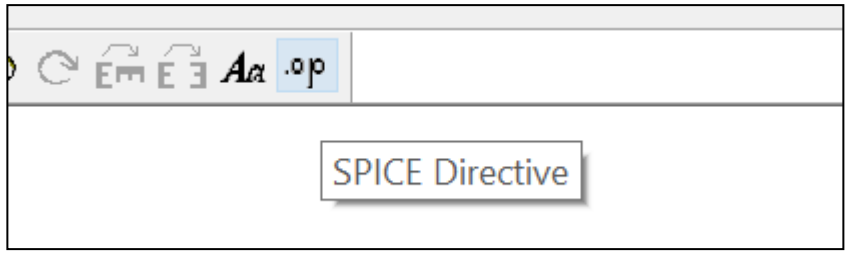
Task 2: Implementation of Inverter using CMOSP and CMOSN

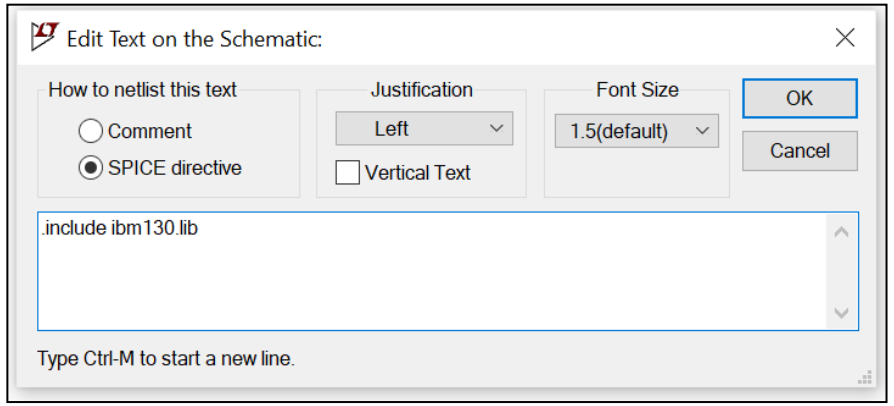
- Note: **in the symbol, Gate contact is close to source**. So, you may have to rotate and place the CMOSP using CTRL+E and CTRL+R.
- Remember to connect Body contact to source.

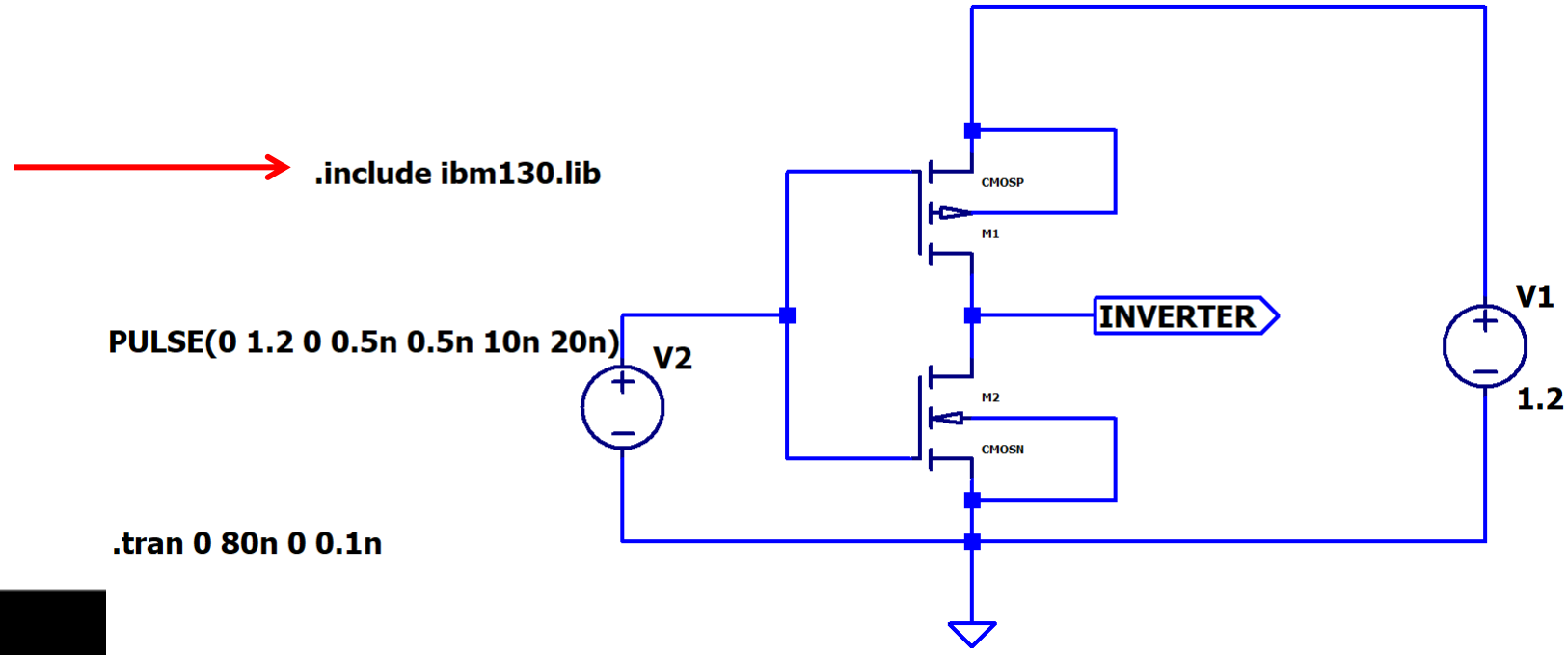


Task 2: Implementation of Inverter using CMOSP and CMOSN

- We need to specify which CMOS configuration we are going to use.



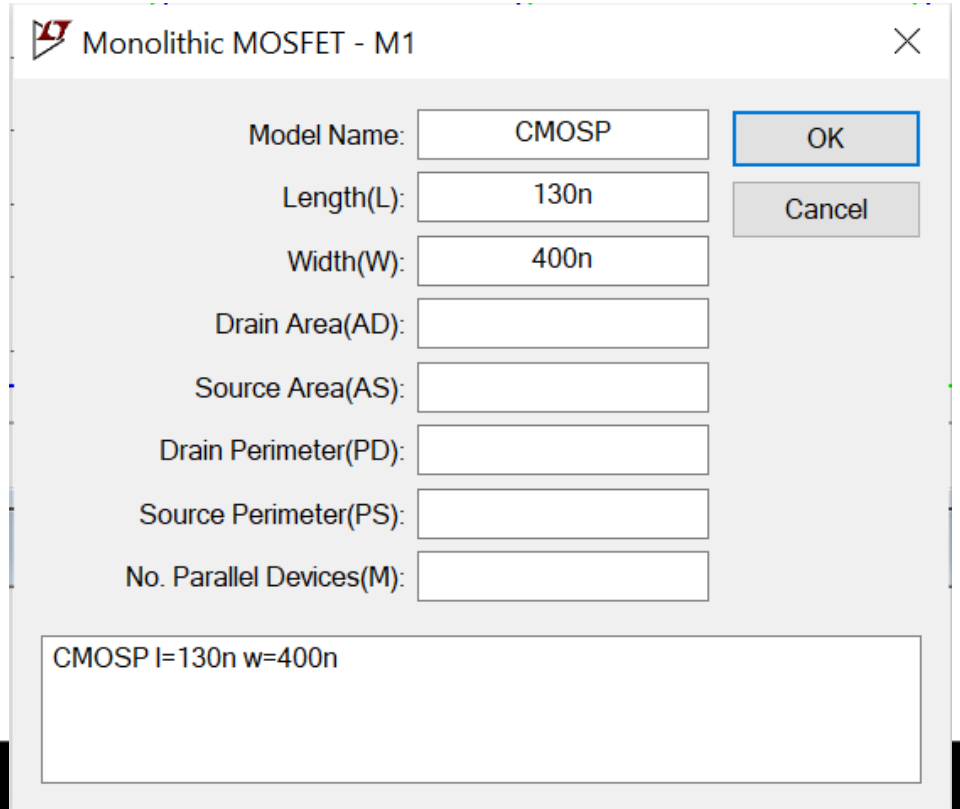


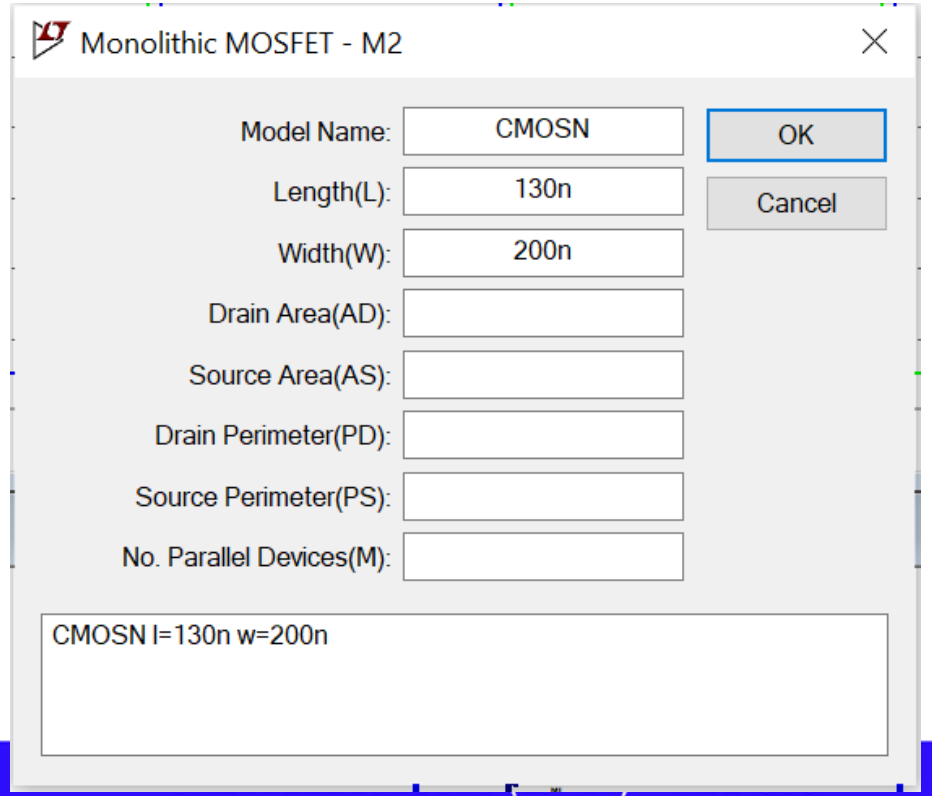


Task 2: Implementation of Inverter using CMOSP and CMOSN

Width 2:1 ratio

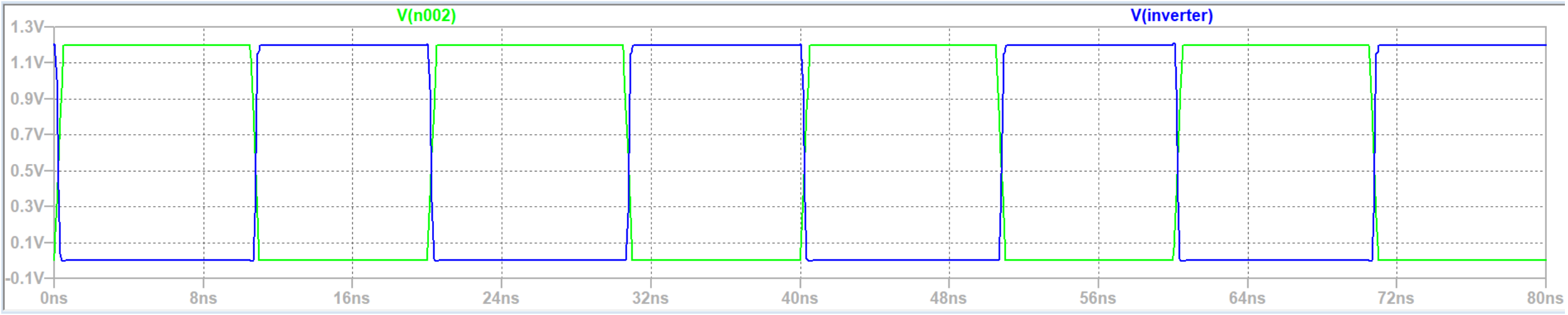
- Right click at CMOSP -> select length as 130nm and width as **400nm**.
- Right click at CMOSN -> select length as 130nm and width as **200nm**.





Task 2: Implementation of Inverter using CMOSP and CMOSN

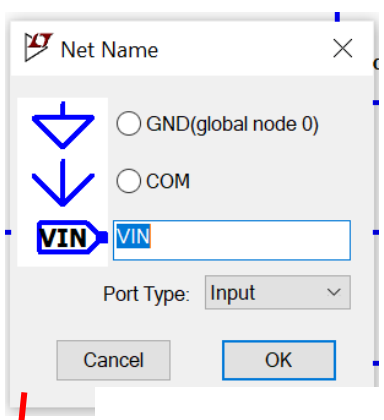
- Correct output:

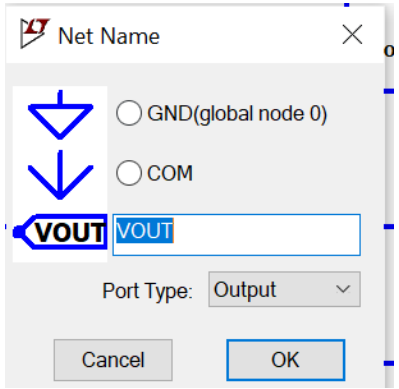


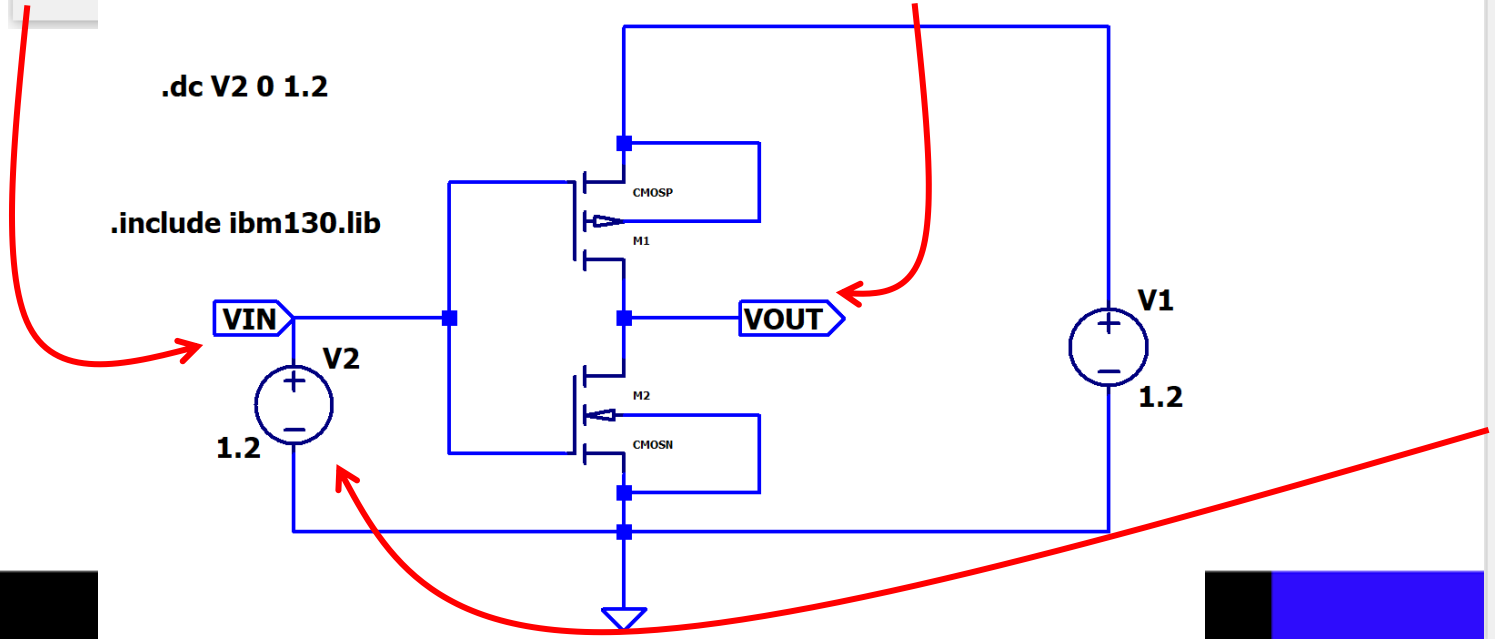
- If you get spikes, then you need to check previous slide for setting the length and width of the channel.

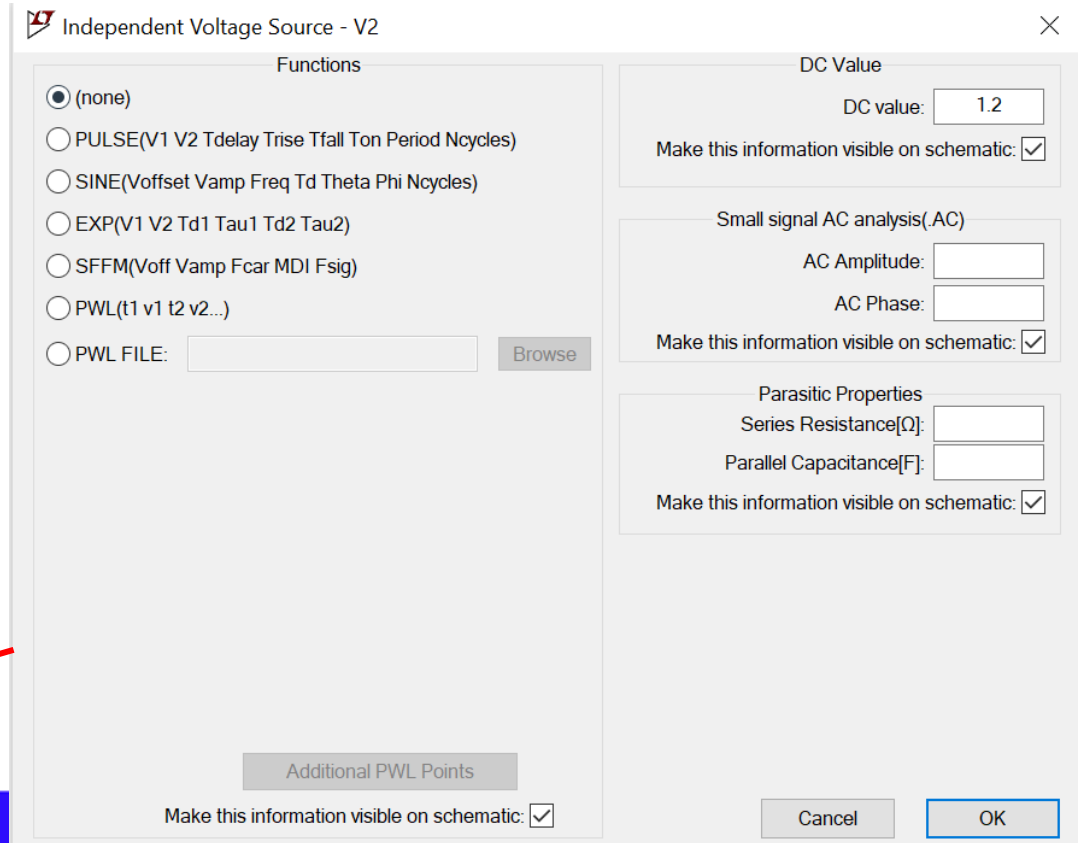
Task 3: To study transition characteristics of Invertor using 130nm technology

- With same 2:1 ratio (400nm for CMOSP and 200nm for CMOSN):



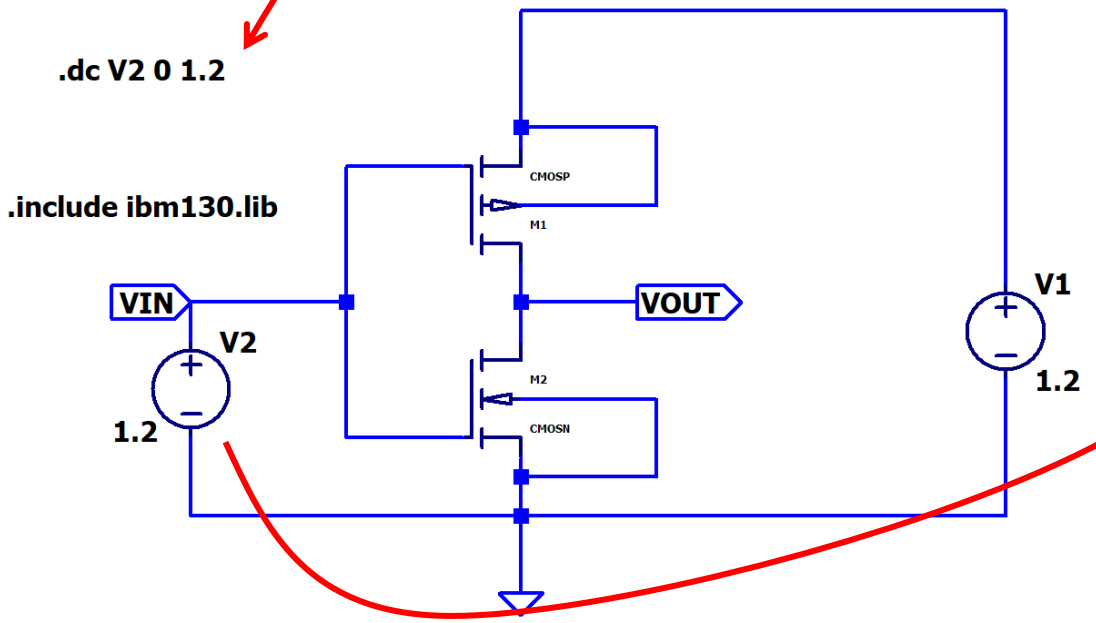


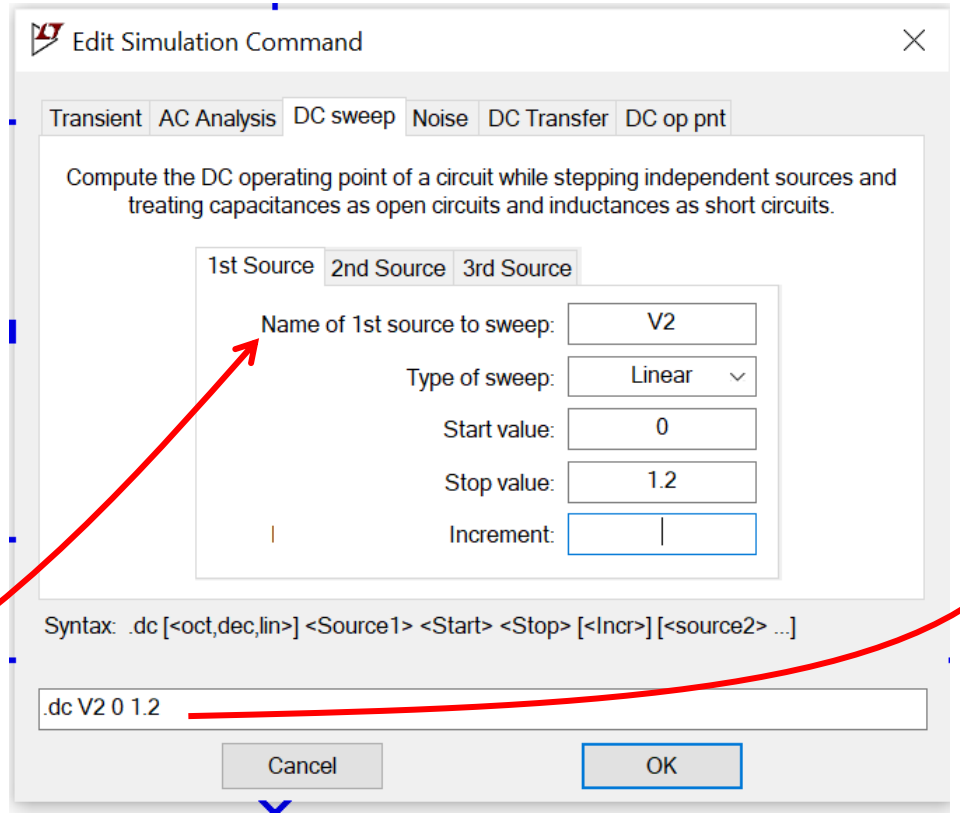




Task 3: To study transition characteristics of Invertor using 130nm technology

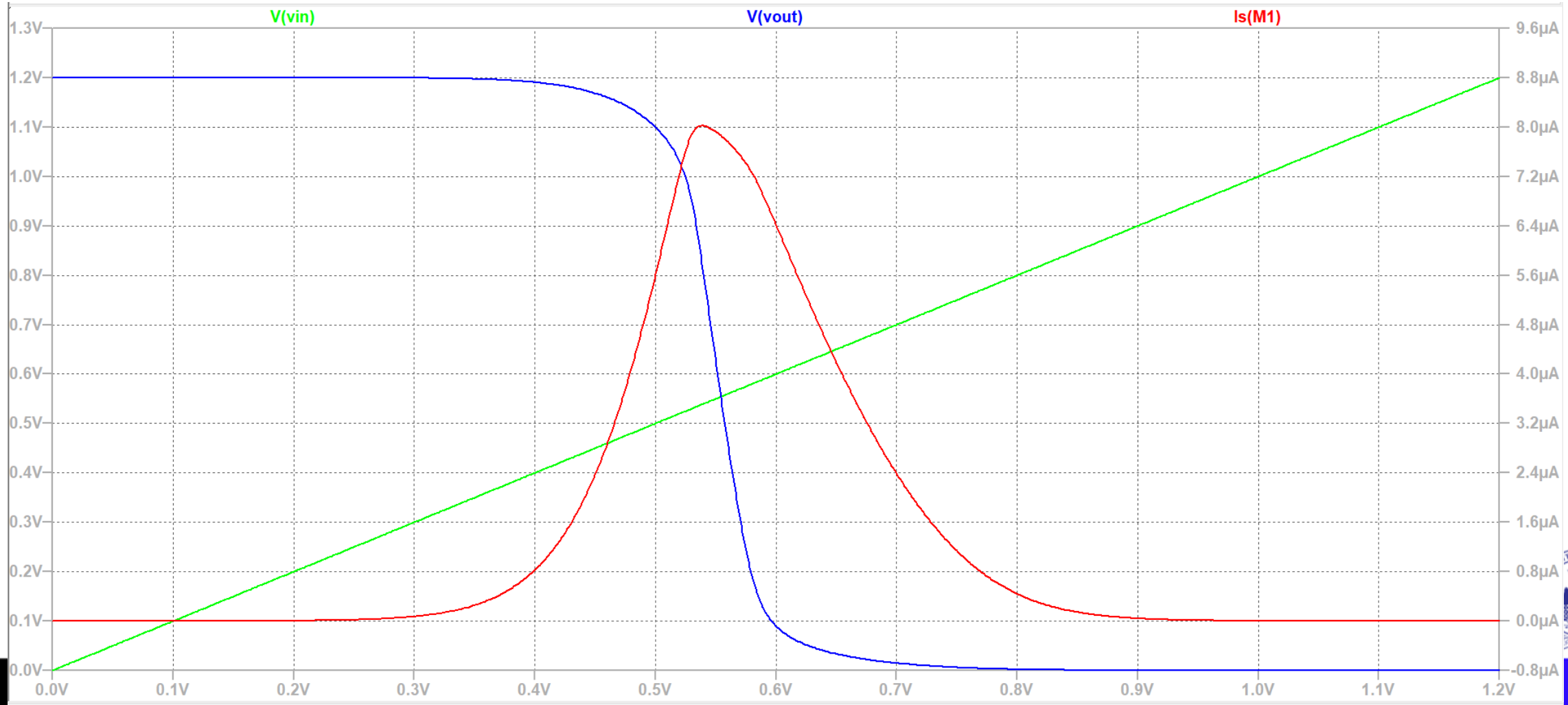
- With same 2:1 ratio (400nm for CMOSP and 200nm for CMOSN):





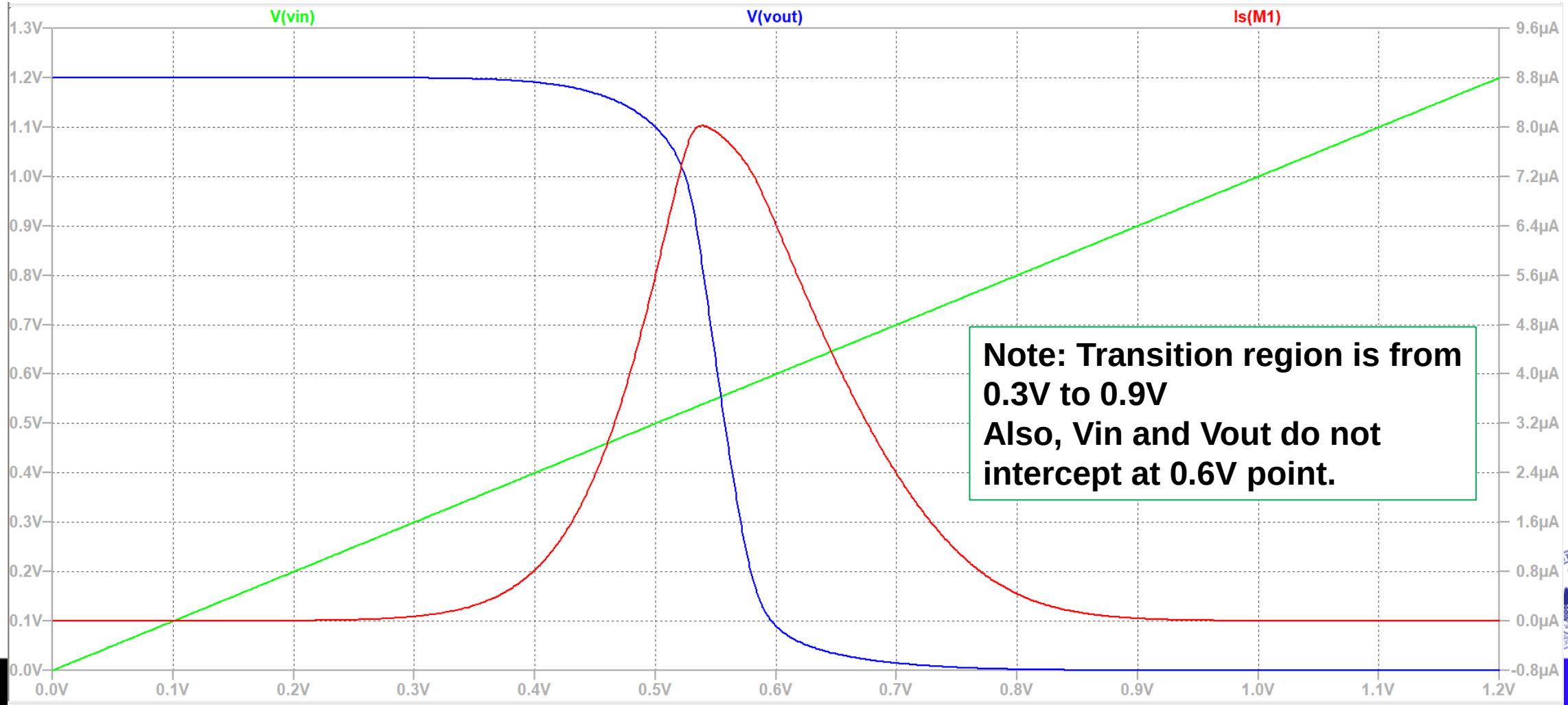
Task 3: To study transition characteristics of Invertor using 130nm technology

- Run and select Vin, Vout, current of source of PMOS.



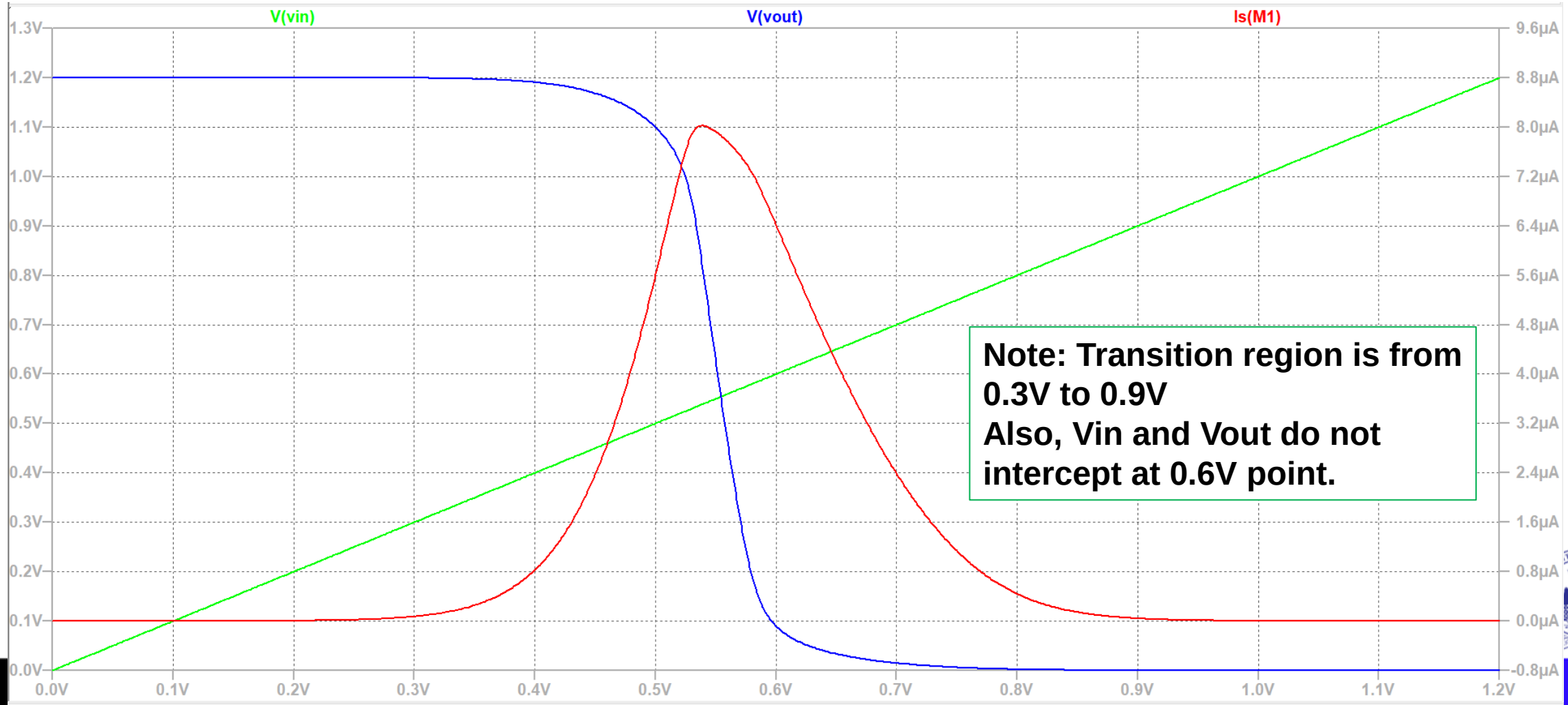
Task 3: To study transition characteristics of Invertor using 130nm technology

- Run and select Vin, Vout, current of source of PMOS.



Task 3: To study transition characteristics of Invertor using 130nm technology

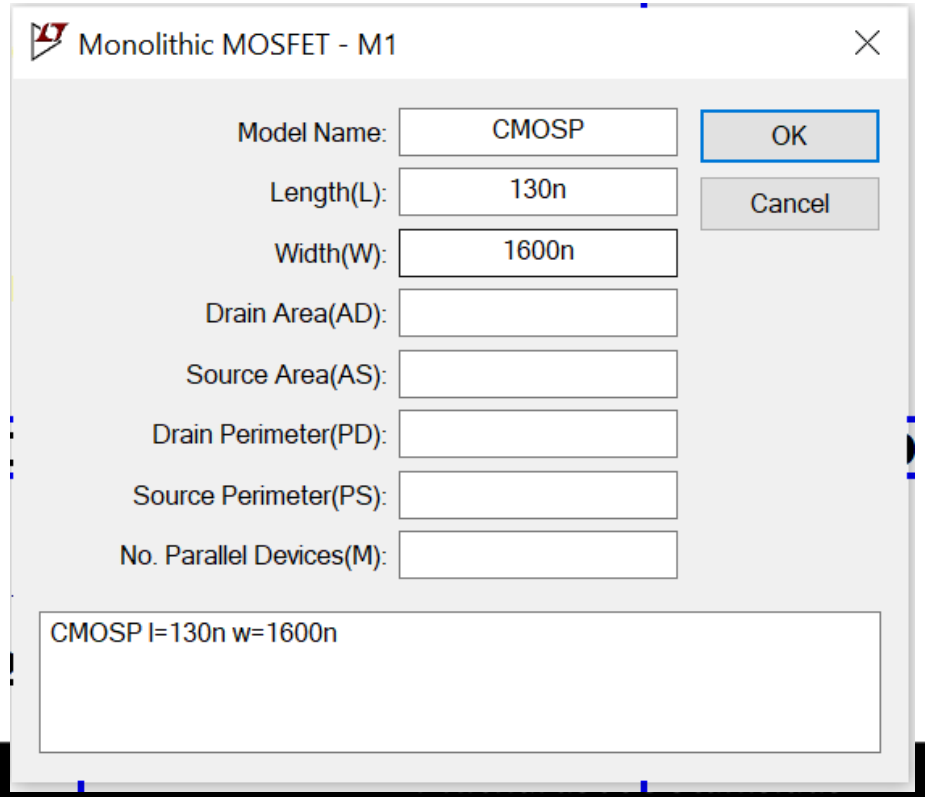
- Run and select Vin, Vout, current of source of PMOS.

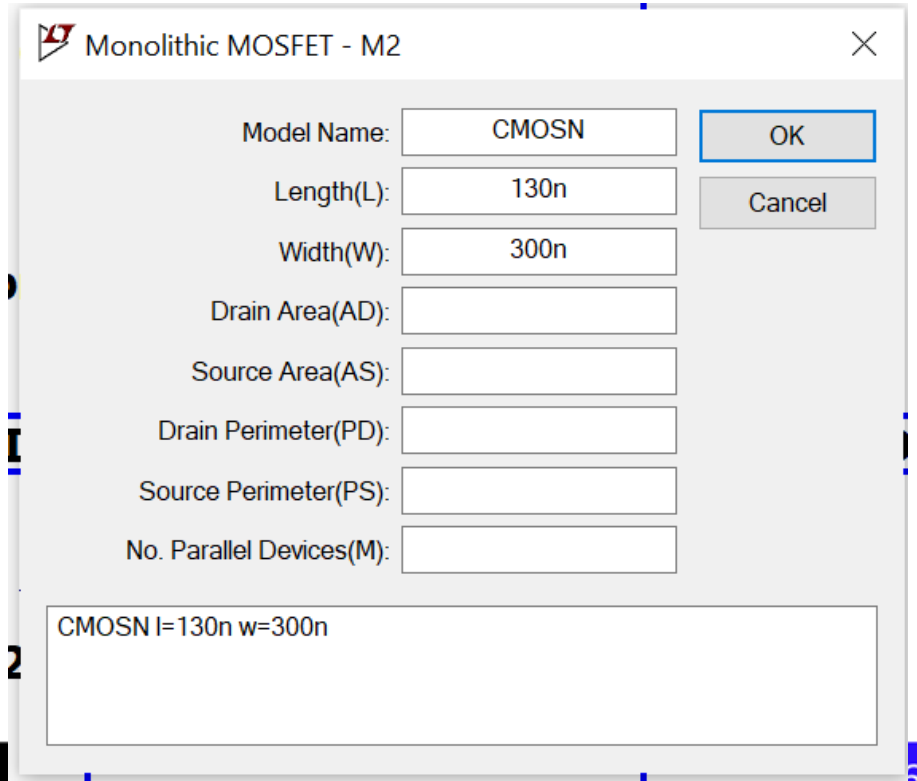


Task 4: To study transition characteristics of Invertor using 130nm technology: **Symmetric**

Change Width 5.3:1 ratio

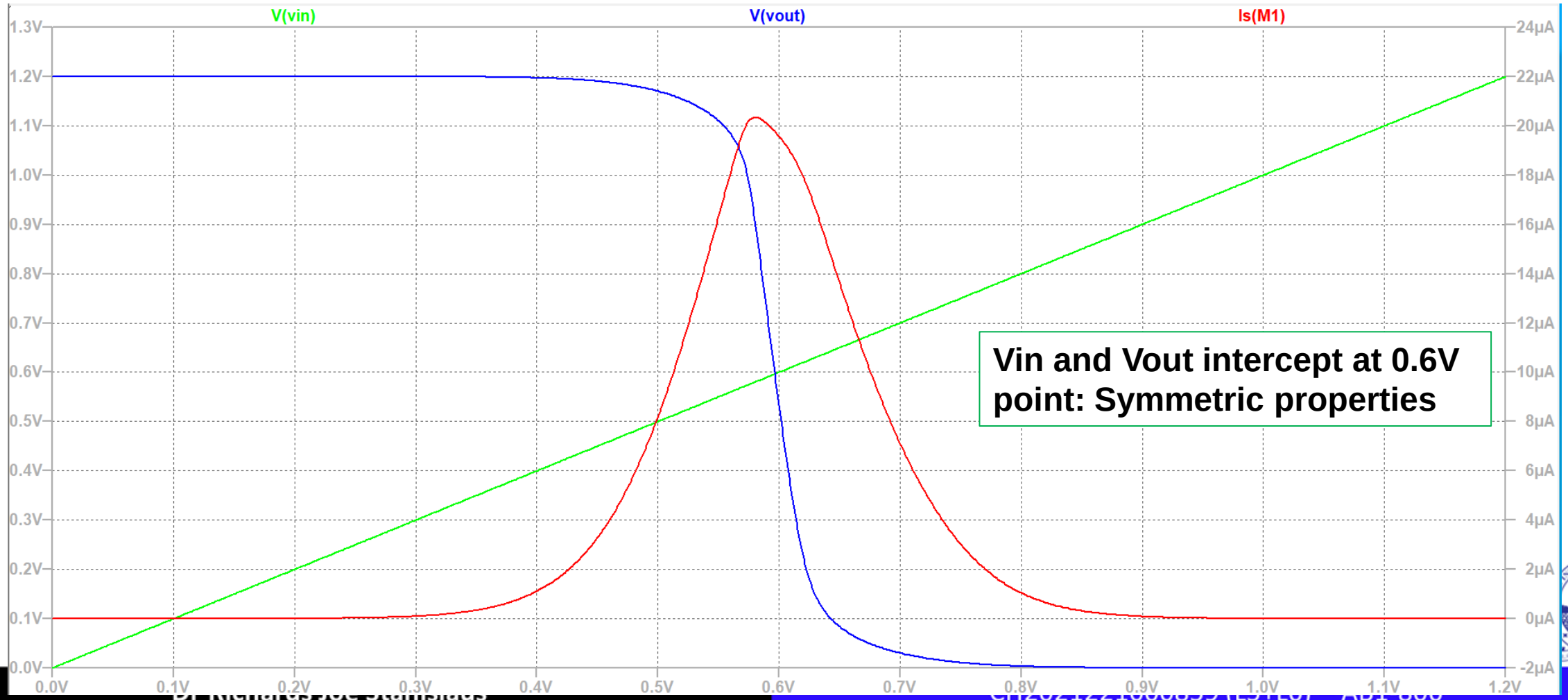
- Right click at CMOSP -> select length as 130nm and width as **1600nm**.
- Right click at CMOSN -> select length as 130nm and width as **300nm**.





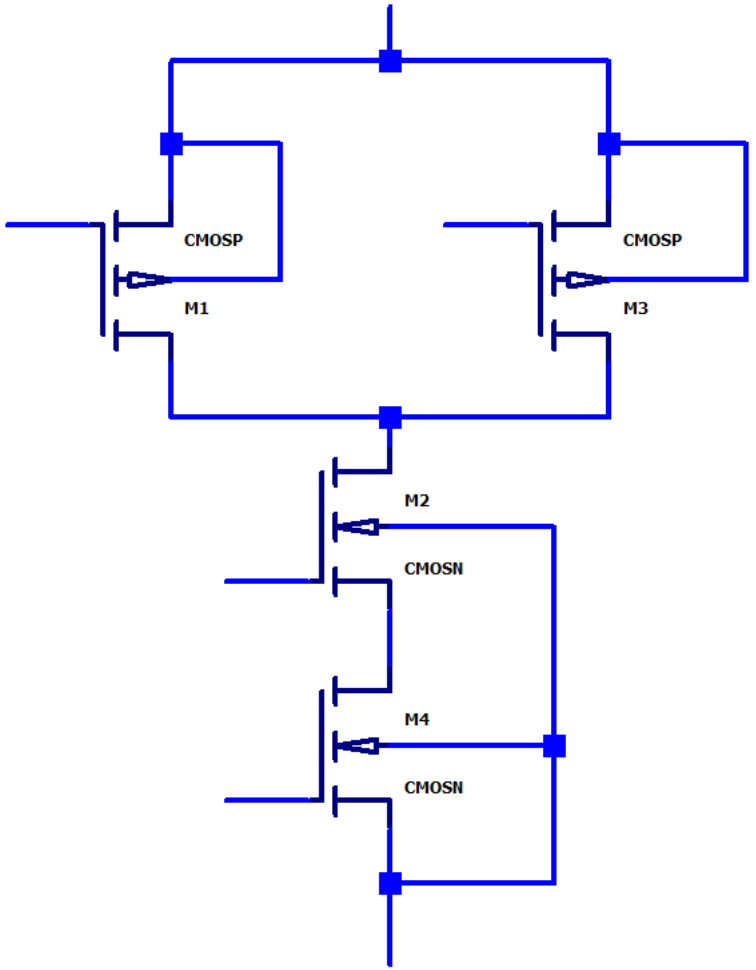
Task 4: To study transition characteristics of Invertor using 130nm technology: **Symmetric**

For the 5.3:1 ratio



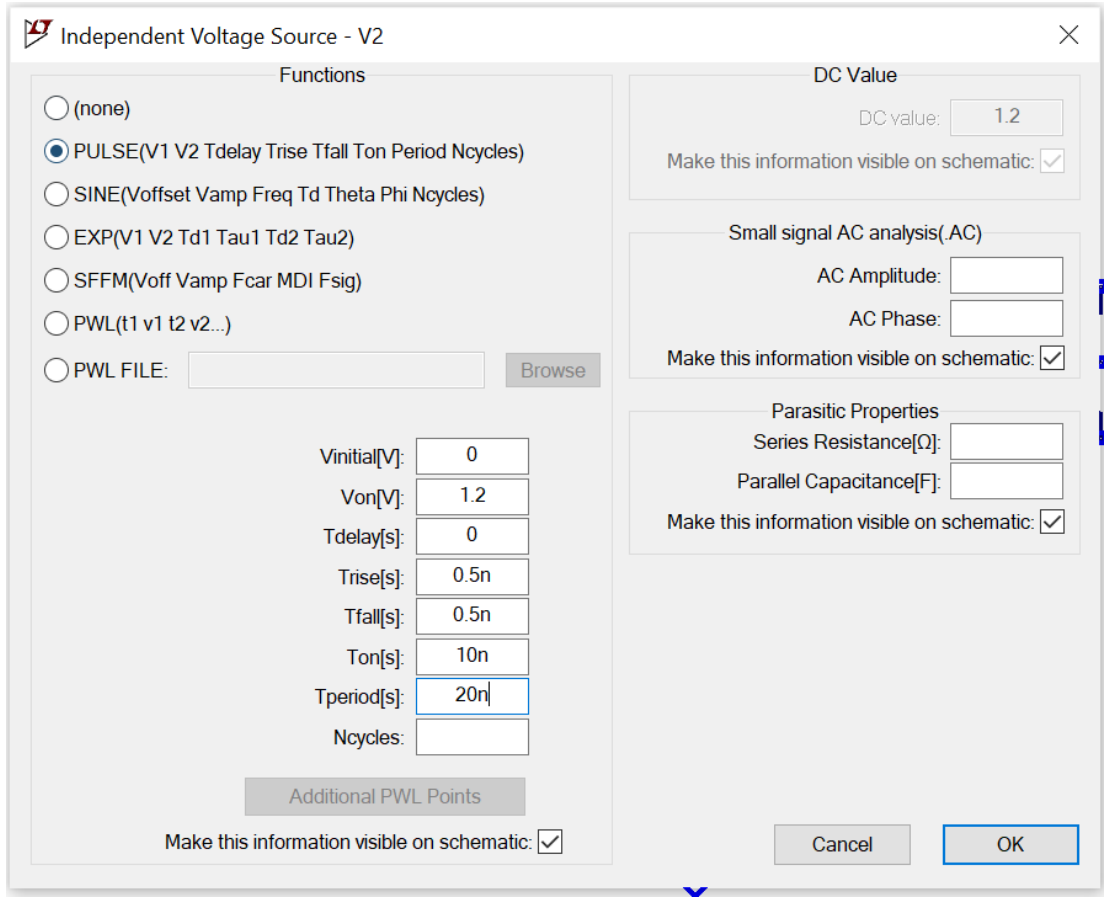
Task 5: To implement NAND gate using CMOS

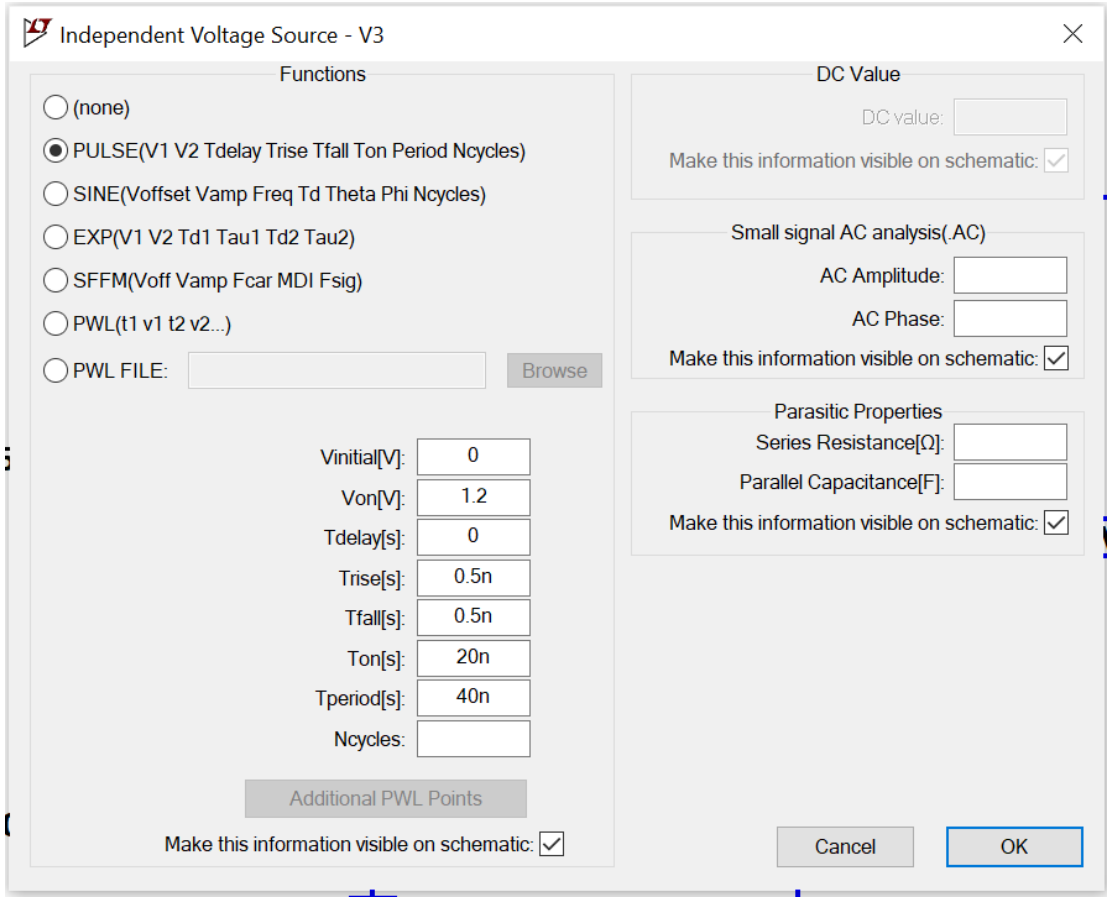
- Two PMOS are in parallel,
  Two NMOS are in series.
  The whole connection is in series



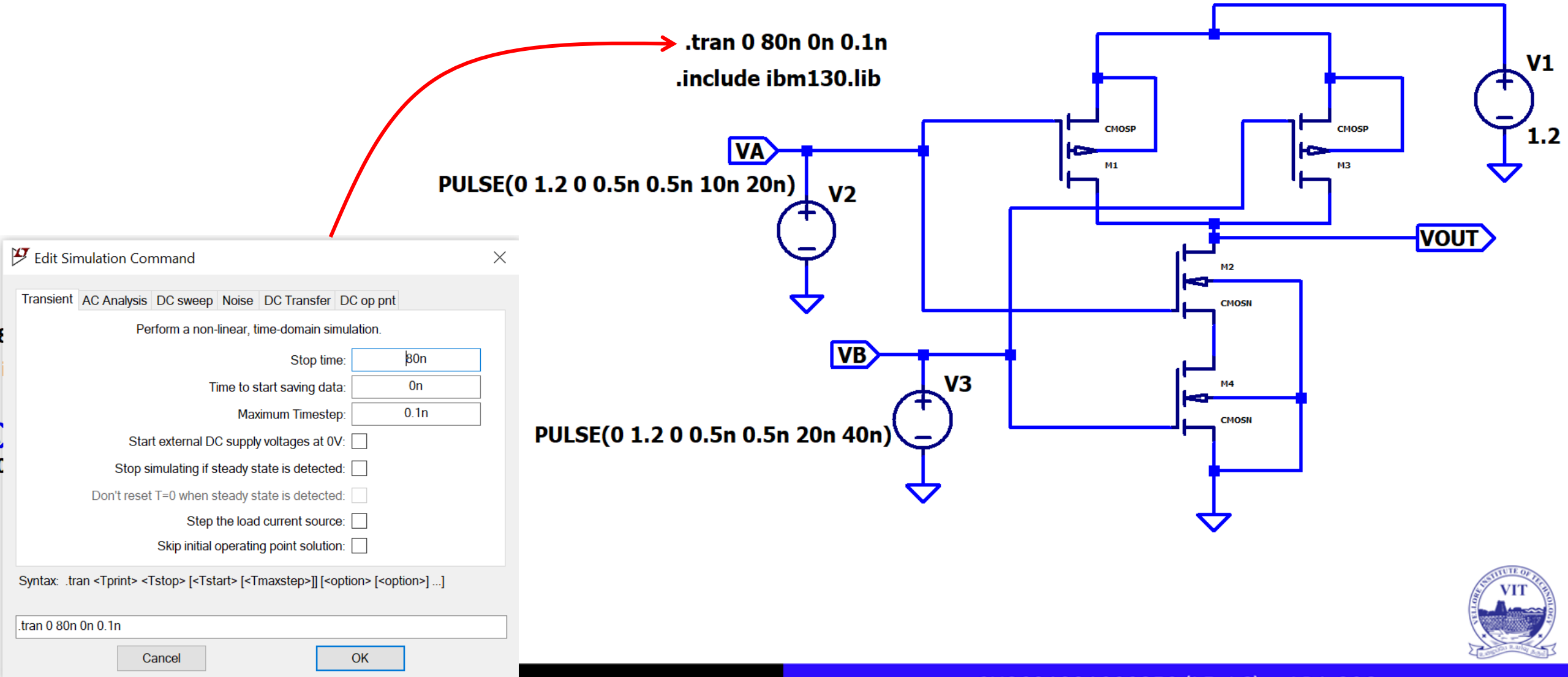
Task 5: To implement NAND gate using CMOS

- Adjust the sources V2 and V3 as below:



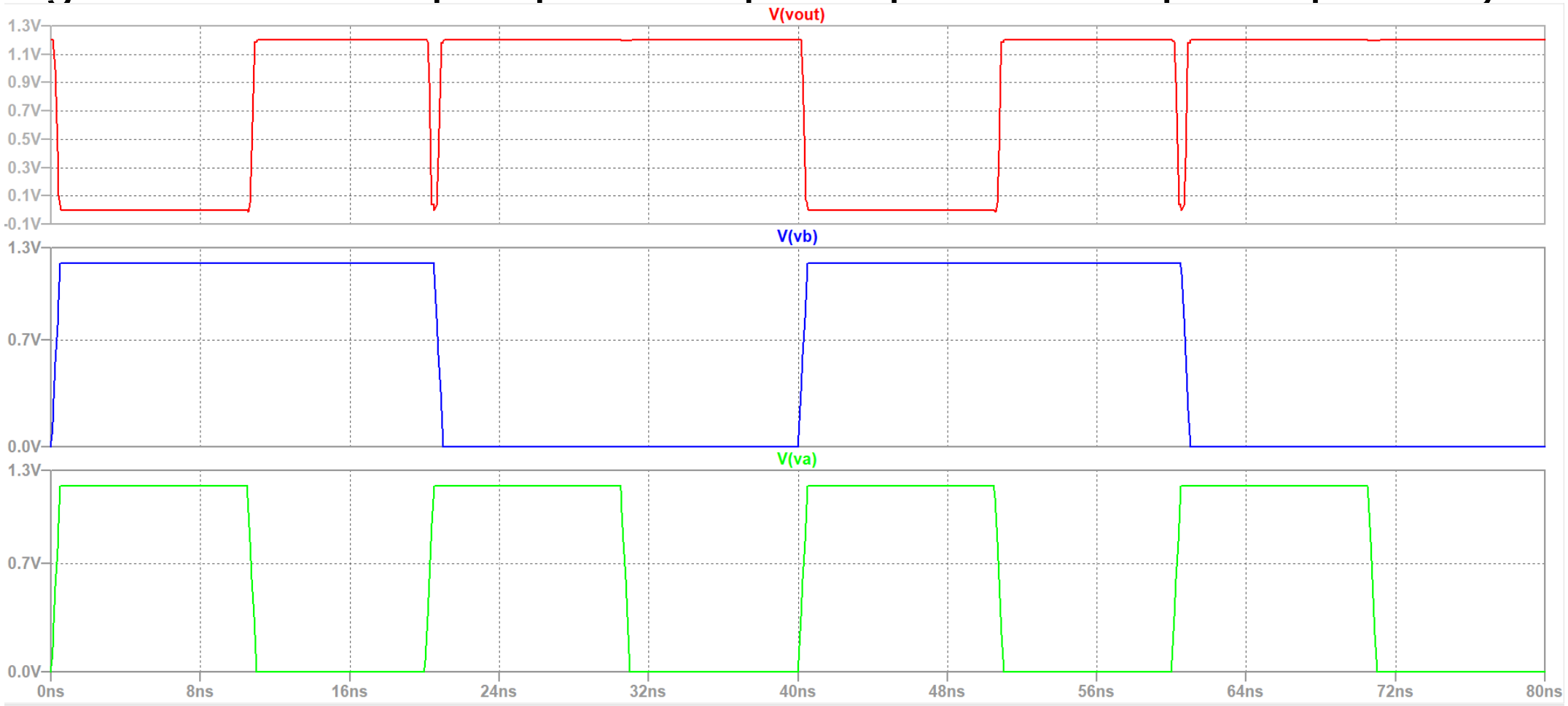


Task 5: To implement NAND gate using CMOS



Task 5: To implement NAND gate using CMOS

- Right click -> Add plot plane to plot input and output separately



Task 5: To implement NAND gate using CMOS

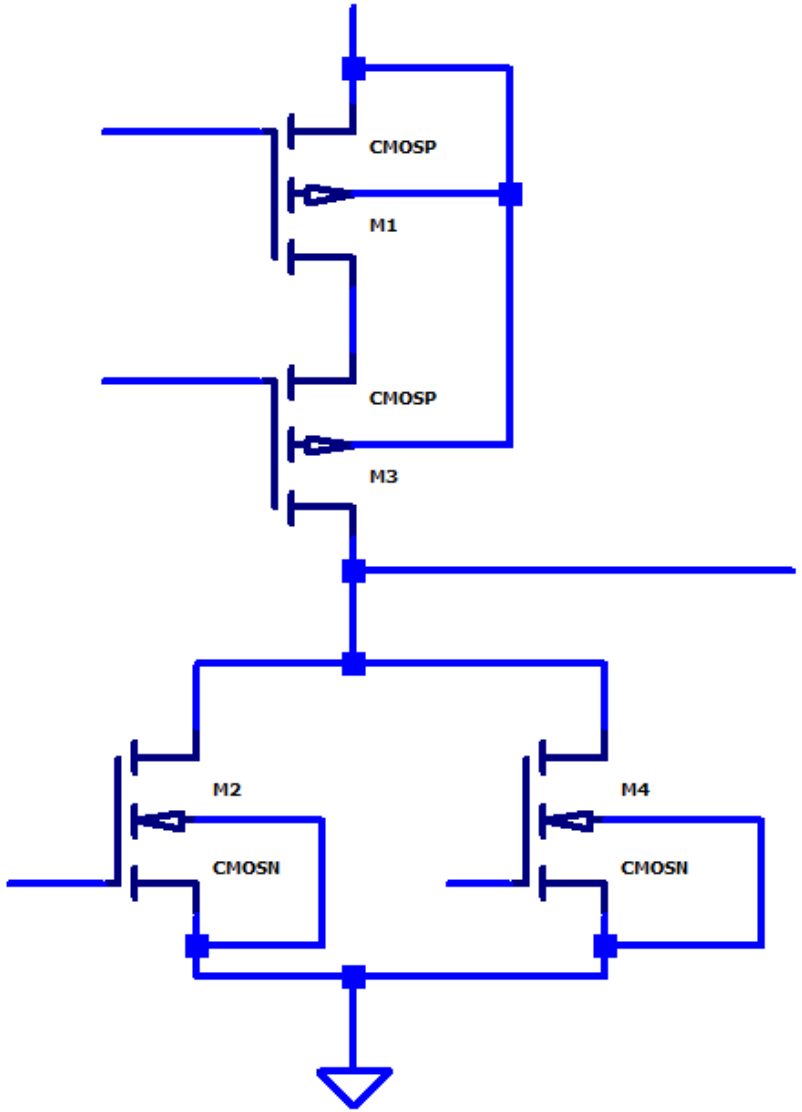
- Verify the truth table

A	B	Y=$\overline{A \cdot B} = \overline{A} + \overline{B}$
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

Task 6: To implement **NOR gate** using CMOS

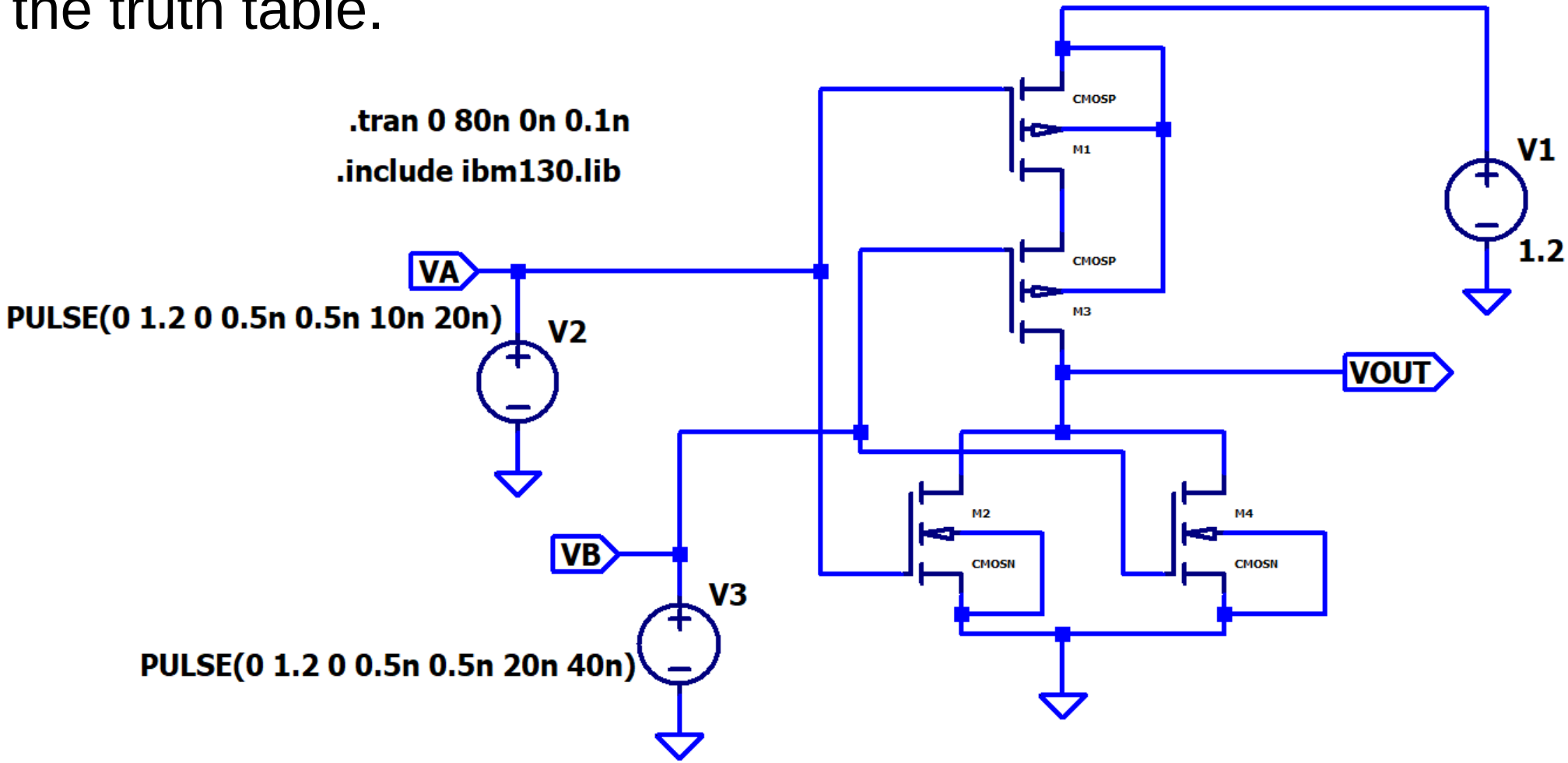
- Implement, plot the inputs and output and verify the truth table.

A	B	Y=$\overline{A+B}=\bar{A}\cdot\bar{B}$
0	0	**1**
0	1	**0**
1	0	**0**
1	1	**0**



Task 6: To implement NOR gate using CMOS

- Implement, plot the inputs and output and verify the truth table.



Important NOTE

- Enter your **registration number** and **Full Name** next to

  all your circuits and
  the output plots.
- Keep the background of circuit and plot as white.

LAB record instructions:

For the lab experiment,

- Write the **Aim**.
- Complete the **Software/Hardware components used**.
- **Obtain the expression for the outputs.**
- Place the respective **circuits in LT Spice**.
- Connect the inputs and outputs. Name them and **write the same in the lab copy(inputs and outputs section)**.
- Use probe in LT spice to plot all possible combinations.
- Write a **concluding statement for each circuit**.
- **Submit** the document's soft copy **on time** in lms.vit.ac.in when available.

Some sources

- https://www.elprocus.com/mosfet-as-a-switch-circuit-diagram-free-circuits/
- http://electrotopic.com/difference-between-nmos-pmos-and-cmos-transistors/
- https://courses.engr.illinois.edu/ece110/sp2021/content/courseNotes/files/?logicAndCMOS
- https://en.wikipedia.org/wiki/PMOS_logic
- https://www.youtube.com/watch?v=qhsleQAAj3g
- https://www.youtube.com/watch?v=Esnx3wd3hJ0