MIT - WORLD PEACE UNIVERSITY

B.Sc. (Computer Science)

Subject:

Exp. No.: 7

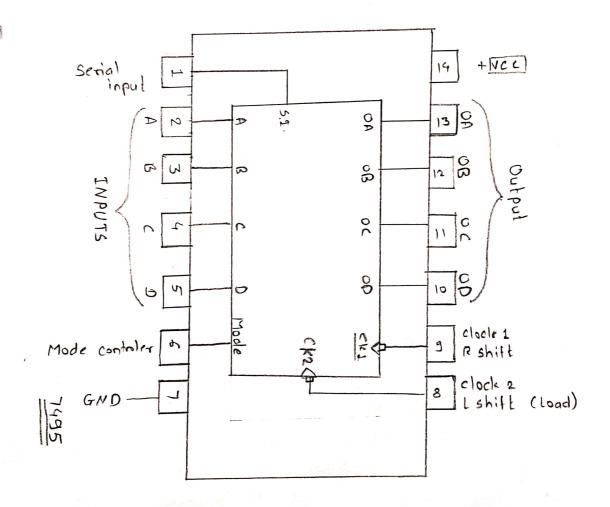
Class:

Batch:

Date:

Name: Veolant Adsor Remarks: Roll No.

Title: To study the operation of bi-operation Date: of shift regester and to observe is output



Incomplete for Diagram Observation Calculation / units **Graph Procedure Precautions** Results Late Submission

	DR. VISHWANATH KARAD MIT - WORLD PEACE UNIVERSITY						
	THE STATE ON VERSITY						
	Aim: To study the operation of bi-operation of shift						
	regester and to observe is output.						
	J STATULE 15 GALPUL.						
1	<u>Equipments:- Trainer kit and connecting wire</u>						
	The contracting wife.						
	Theory: - The IC 7495 shift register has 4-bit word						
	capacity and has provision for serial and						
	parallel output.						
	It can be loaded by serial as well as						
<u>)</u>	permollel data inputs and has the capacity						
	to provide the left shift and right shift						
	function.						
	The mode centrals and two clock determine						
	the function, which the shift register will						
1	perform. (shift right or shift left)						
	when made controls M = low; night shift operation						
	- With mode control 19 love one input of all						
* 1	AND goites No.2 and enable All AND gate No.1						
	- Register does not accept parallel data but						
	accept serial data and reaches to the input						
	to 1st flip flop						
	- Now output of each flip. flop is applied to						
	Il input of next flip flop through AND gates						
	No.1 and NOT gate NO.3 except IfA.						
	This senal shift regester arrangement in						
	which serial input is shifted too right after						
	application of every clock pulse and regester						
	works as right shift register.						
	When made controls M= high: left shift operation						
	- One input of all AND gotes No. 1 is low and						
	one input of all AND gate No. 2 is high This						
A second							

A :	disables all gate No.2.
	accepte spried data ===
	TE data 15
	to an in a the reaches the street
	() A (last (if) and it exertanally the
17	connected to Pc Qc connected to VB and UR
	is connected to Pa, then circuit arrangement
	Morks as left shif register
*	Serial input ordered Parailel output (SIPO) 03
	and rand Inout senal output
	- When Me low, data is applied at serial
	1
	- when clock pulses are applied than 4-bit
	data stored in Flop-Flop is available at the
- Called Street	outent of each Flip-flop.
<u> </u>	- so register work as serial input parallel
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	tail (STPA). It again 4 & clock pulse are
?/, >	applied and output is taken from last.
31	flip flop then data is axiilable senally and -
20	shift register mork as sIso shift register -
· e	
V - 1	Parallel input parallel output (PIPO) and
-	parallel input serial output (PISO)
	- When M= high and it parallel 4-bit data
	is connected at la to Po and clock pulse
, F	is applied, then 4 bit data is stored in
	4-bit flip flop, is available at each out
has to	of flip flop Hence it works as PISO shi
	register
	- when in is high and parallel date at Pd

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	to pp is applied						
Parker +	- when clock pulse is applied 4-bit parsallel						
	data gets stored in Flip-flop						
	- It M is made low and 4. clock pulses are						
	applied then senal data output at lost o						
	flip-flop.						
	- shift register works as PISO shift register.						
	Test Procedure:						
	PART (A): Serial in porallel out:						
	1. Connect the circuit as per circuit diagram.						
	2. Connect the +5v power supply between pin 14 to 7.						
	3. Apply series data at so input ic pin 1 and						
	ground to pin no.6.						
	4. Apply clock pulse one by one at clock input						
	i-e. pir no. 9.						
	5. connect pin nois la, 11, 12, 13 je (20 QCQBQA)						
	10 output LED's						
	6. Observe the output of COA DB. QC QD on LED						
	7. mite the output in the observation table.						
	PART (B): - serial in serial out						
	1. Connect the circuit as per the diagram.						
	2. Connect the +5V power supply between pin 14						
	and pin 7.						
	3. Apply the series data at sp input i.e. pin 1 and						
	ground to pin no.6.						
	4. Apply clock pulse one by one of clock input						
	i.e. pin no.g.						
1.4	5. Connect pins: nos 10, 11, 12, 13 i.e. (20, Qc, Qa, Qa, Qa) b						

	output LEO's.
	c. For senal out consider only an output
	7. Write the output in the observation table
1 2	
	Part (e): Parallel in parallel out
	1 Caret the circuit as per the circuit alog
	2. Connect the tov power supply between pin
	3- Apply permallel data ABCD at pin no. 234
	and 50 to pin no.6.
	4. Apply clock pulse one by one at clock input
111111111111111111111111111111111111111	i.e. pin no.8.
<u>-1 1</u>	5. Connect pin nois 10, 11, 12, 13 i.e. (QDQC, QBQr
3/3	to output LEP's
	7. Write the output in the observation table
and the same of the same of	7. write the output in the observa
,	
1 (20.7)	Part D:- parallel in senal out
1 Gas	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2 Connect the +5v power supply between pin 14t
Carlo	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2 Connect the top power supply between pin 14t pin 7.
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2. Connect the +5v power supply between pin 14th pin 7. 3. Apply series data at so input i.e. pin 1
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2. Connect the top power supply between pin 14th pin 7. 3. Apply series data at so input i.e. pin 1 and 5v to pin no.6.
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2. Connect the +5v power supply between pin 14th pin 7. 3. Apply series data at so input i.e. pin 1 and 5v to pin no.6. 4. Apply clock pulse one by one at clock input
	Part D:- parallel in senal out 1. Connect the circuit as per circuit diagram 2. Connect the top power supply between pin 14t pin 7. 3. Apply series data at so input i.e. pin 1 and sv to pin no 6. 4. Apply clock pulse one by one at clock input i.e. pin no 8.
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram. 2. Connect the +5v power supply between pin 14th pin 7. 3. Apply series data at sp input i.e. pin 1 and 5v to pin no.6 4. Apply clock pulse one by one at clock input i.e. pin no.8. 5. Connect pin no.e to pin no 12, pin no.3 to
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2. Connect the top power supply between pin 14th pin 7. 3. Apply series data at sp input i.e. pin 1 and 5x to pin no.6 4. Apply clock pulse one by one at clock input i.e. pin no.8. 5. Connect pin no.e to pin no. 12, pin no.3 to pin no.11, pin no.4 to pin no.10
	Part D:- parallel in serial out 1. Connect the circuit as per circuit diagram 2. Connect the top power supply between pin 1st pin 7. 3. Apply series data at so input i.e. pin 1 and sv to pin no. 6 4. Apply clock pulse one by one at clock input i.e. pin no. 8. 5. Connect pin no. e to pin no. 12, pin no. 3 to pin no. 11, pin no. 4 to pin no. 10 6. Connect pin no. 10, 11, 12, 13, i.e. (Do Oc. 20)
	Part D:- parallel in senal out 1. Connect the circuit as per circuit diagram 2. Connect the top power supply between pin 14th pin 7. 3. Apply series data at so input i.e. pin 1 and sv to pin no 6 4. Apply clock pulse one by one at clock input i.e. pin no 8. 5. Connect pin no e to pin nor 12, pin no 3 to pin no 11, pin no 4 to pin no 10 6. Connect pin no 10, 11, 12, 13. i.e. (Do De Sale to output IED's.
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Part (0) serial in parallel out (left shift)

Input		Output			
Sp.	Clock	QA	Q ₆	Qe	Qp
	Pulse				
in the second	0	~	~	×	1
O		Υ	×	l,	0
	2	~	(0	ľ
400	3	1	O	1	1
	4	0	1	1	1
	l		-		

Result: - All truth tables are successfully varified practically and theorotically!