Indian Institute of Technology Kharagpur

AUTUMN Semester, 2018
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-5: Verilog Design of Binary Multipliers

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench, and a report (in .pdf format) of the hardware resource requirement and time required to complete 8-bit multiplications. Name your submitted zipped folder as `Assgn_5_Grp_<Group_no>.zip` and (e.g. `Assgn_5__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Unsigned binary array multiplier**] Design (using Verilog), simulate and implement on FPGA an 8-bit unsigned binary array multiplier. Write a testbench to simulate it, and demonstrate its operation on the FPGA. Note its hardware requirement and critical path delay from the synthesis report. The interface of your design should be:
   ```
   module array_multiplier (input [7:0] a, input [7:0] b, output [15:0]
   product);
   ```
   (4 marks)

2. [**Two's complement combinational binary multiplier**] Design (using Verilog), simulate and implement on FPGA an 8-bit Two's complement combinational binary multiplier. **Your design should use the array multiplier designed in problem-1**. Write a testbench to simulate it, and demonstrate its operation on the FPGA. Note its hardware requirement and critical path delay from the synthesis report. The interface of your design should be:
   ```
   module combinational_multiplier (input [7:0] a, input [7:0] b, output [15:0]
   product);
   ```
   (6 marks)

3. [**Booth's multiplier**] Design (using Verilog), simulate and implement on FPGA a circuit for multiplication of two 6-bit two's complement integers, using the *Booth Multiplication Algorithm*. Write a testbench to simulate it, and demonstrate its operation on the FPGA. Note its hardware requirement and critical path delay from the synthesis report. The input-side operand registers used in the datpath of your multiplier should have "parallel load" capabilities such that the 6-bit operands can be loaded in each of them in one clock cycle. Come up with a proper interface of your design, which includes all input control signals and a clock signal. (8 marks)

4. Finally, submit a small 1-page report (in .pdf format) comparing the speed of operation and hardware requirements of the above three designs. (2 marks)