Indian Institute of Technology Kharagpur

AUTUMN Semester, 2018
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-3: Verilog Design of Combinational Circuit

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s), Verilog testbench, and a diagram of the architecture in PNG format on Moodle. Name your submitted zipped folder as `Assgn_3_Prob_1_Grp_<Group_no>.zip` and (e.g. `Assgn_3_Prob_1_Grp_25.zip`). The architectural diagrams must be drawn using a software, and should not be hand-drawn and scanned. Your code should have parity with the architectural diagram, otherwise marks would be deducted. Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Sign Magnitude Adder**] Design (using Verilog), simulate and implement on FPGA an 8-bit sign-magnitude adder circuit. Each of the two operands should have 7 magnitude bits and 1 sign bit (as the MSB). Write a testbench to simulate it, and use the provided ".ucf" file to demonstrate its operation on the FPGA. The interface of your design should be:
   `module sign_mag_adder (input [7:0] a, input [7:0] b, output [8:0] sum);` (10 marks)

2. [**Bidirectional Barrel Shifter**] Design (using Verilog), simulate and implement on FPGA an 8-bit bidirectional barrel shifter circuit to perform arbitrary circular right/left shift (when the input control signal "direction" is 1, it performs right shift, and otherwise it performs left shift). Write a testbench to simulate it, and use the provided ".ucf" file to demonstrate its operation on the FPGA. The interface of your design should be:
   `module bb_shifter (input [7:0] in, input [2:0] shift, input direction, output [7:0] out);` (10 marks)