

Summary Report on Adder

Comparison between the ripple carry adder, the hybrid adder, bit serial adder implemented using verilog.

The Ripple carry Adder

The ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

Delay : $O(n)$

Hardware Requirement - Minimum

Maximum Combinational Path Delay - 20.4ns

Macro Statistics

1 bit xor3 - 8 required

No. of 4 input LUTs used - 16

The Hybrid Adder

A 4 - bit Hybrid adder is designed by rippling the 3rd carry of the CLA through a full adder to produce the fourth carry and sum, by cascading this four bit block N-bit adder is realized. In general by rippling the last but one carry through a full adder the Hybrid adder can be designed.

Delay : $O(n)$

Hardware Requirement - More than Ripple Carry

Maximum Combinational Path Delay - 20.4ns

Macro Statistics

1 bit xor2- 16 required

No. of 4 input LUTs used - 16

The Bit Serial Adder

If speed is not of great importance, a cost-effective option is to use a serial adder. Bits are added a pair at a time (in one clock cycle) so this speed of this adder depends highly on the speed of the clock.

Delay : Depends on clock

Hardware Requirement - The hardware requirements are very different from the previous two adders since this is a sequential and not a combinational circuit

6 bit registers: 2 required

D flip-flop: 1 required.

Conclusion

We find that ripple carry adder and the hybrid adder have the same worst case delay, the hybrid adder is faster in general because the carry gets computed directly. In the case of the bit serial adder, the synthesis report does not show any maximum combinational path delay since it is a sequential circuit and not a combinational one. This is why the synthesis report of the bit serial adder looks very different from the other two adders.