Indian Institute of Technology Kharagpur

AUTUMN Semester, 2018
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-6: Verilog Design of Finite State Machines

Full Marks: 10

Time allowed: 3 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_6_Grp_<Group_no>.zip` and (e.g. `Assgn_6__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Two's Complement Converter FSM**] Design (using Verilog) and simulate (using an appropriate Verilog testbench) a simple finite state machine (FSM) that in every clock cycle reads an input bit, and outputs a bit such that the bitstring output till that point is the two's complement of the binary number read till that point, including the most recently read bit (the number is considered to be input from the LSB side). The FSM has one input control signals which resets it to the initial state. [Hint: consider a Mealy machine.] (5 marks)

2. [**Multiple-of-three Detector FSM**] Design (using Verilog) and simulate (using an appropriate Verilog testbench) a simple finite state machine (FSM) that in every clock cycle reads an input bit, and outputs a bit which indicates whether the binary number read till that point, including the most recently read bit (the number is considered to be input from the LSB side), is divisible by three. The input number is to be considered an unsigned integer. The FSM has one input control signals which resets it to the initial state. [Hint: again, consider a Mealy machine.] (5 marks)
