Single Cycle CPU

Instruction Format

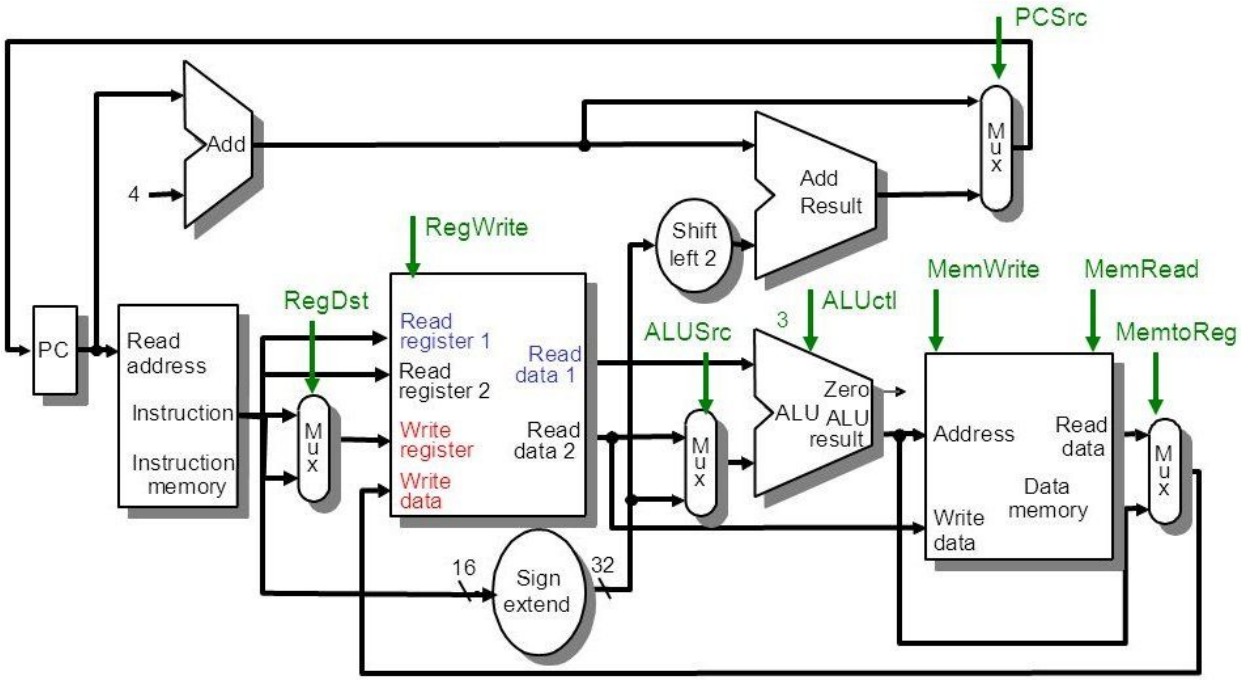
OP	rs	rt	Func	Offset
2	5	5	4	16

Decoding

Arithmetic	Add	00	0000
	Comp		0010
	Addi		0001
	Compi		0011
Logic	And	00	0100
	XOR		0101
Shift	SLL	00	0110
	SRL		0111
	SLLV		1000
	SRLV		1001
	SRA		1010
	SRAV		1011
Memory	LW	01	0000
	SW	10	0000
Branch	Unconditional Branch	11	0000
	Branch register		0001
	Branch on zero		0010
	Branch on not zero		0011

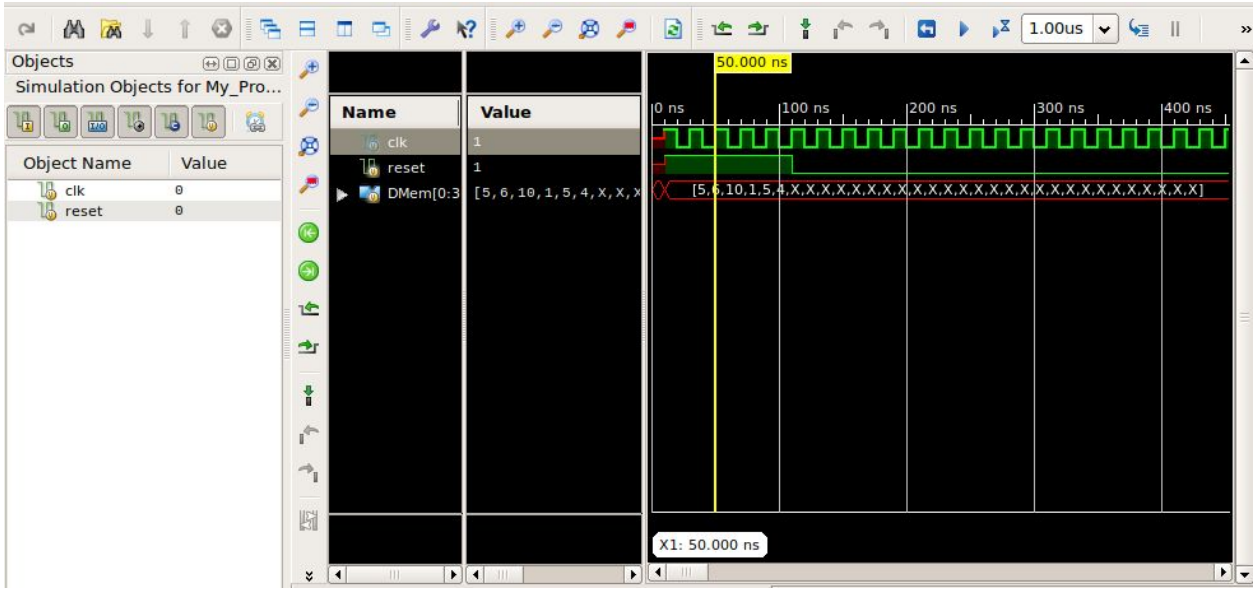
	Branch on carry		0100
	Branch on Not carry		0101
	Branch on sign		0110
	Branch on not sign		0111
	Branch on overflow		1000
	Branch on No overflow		1001
	Call		1010
	Return		1011

Architecture

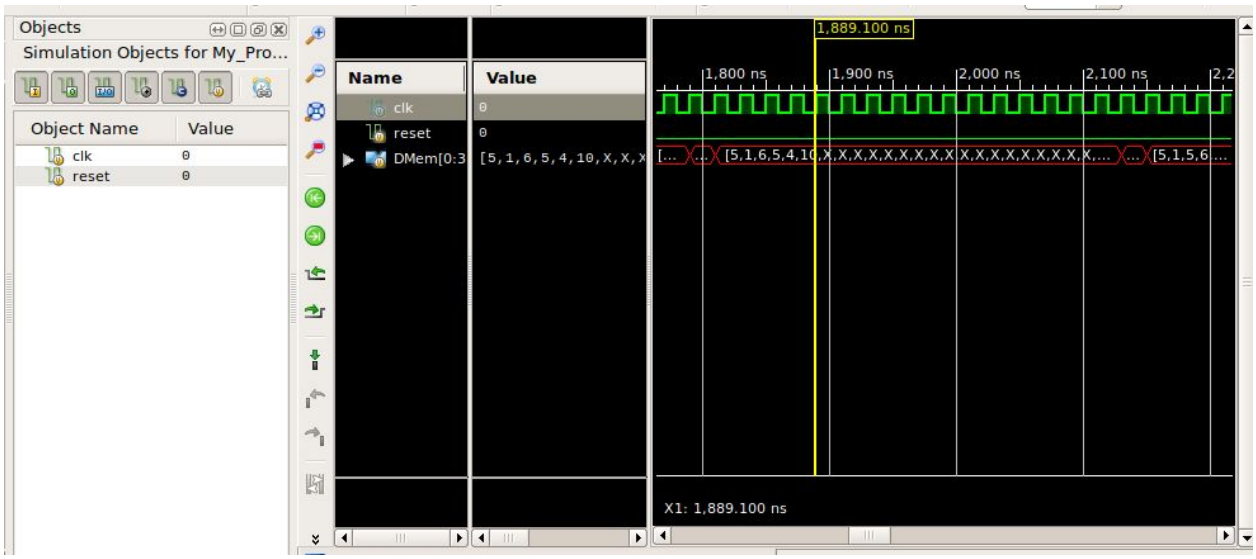


Sample Run and Output for Bubble Sort:

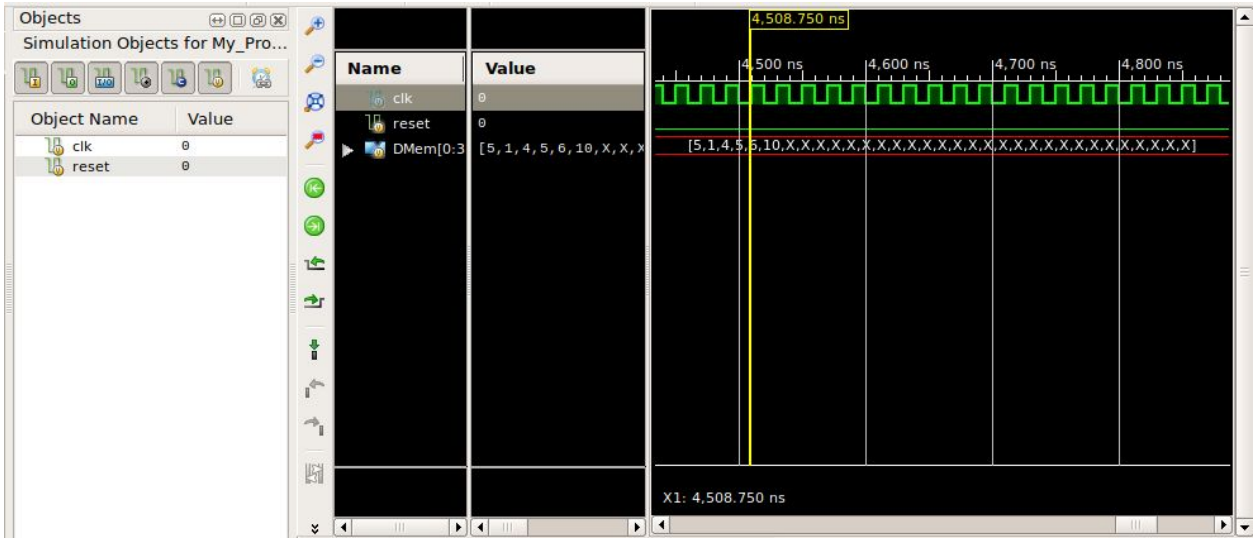
Initial Values



Intermediate Values



Final Output



Group 16:

Rahul Kumar (16CS10042)

Vedic Partap (16CS10053)