CodTech Internship - Task 1: ALU Design

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Language Used: Verilog

Simulation Tool: ModelSim / Vivado

ALU Verilog Code

```
module ALU (
    input [3:0] A,
    input [3:0] B,
    input [2:0] opcode,
    output reg [3:0] result
);

always @(*) begin
    case (opcode)
        3'b000: result = A + B;
        3'b001: result = A - B;
        3'b010: result = A & B;
        3'b011: result = A | B;
        3'b100: result = ~A;
        default: result = 4'b0000;
    endcase
end

endmodule
```

ALU Testbench Code

```
module ALU_tb;

    reg [3:0] A, B;
    reg [2:0] opcode;
    wire [3:0] result;

    ALU uut (
        .A(A),
        .B(B),
        .opcode(opcode),
        .result(result)
    );

    initial begin
        A = 4'b0011; B = 4'b0001; opcode = 3'b000; #10;
        A = 4'b0100; B = 4'b0001; opcode = 3'b001; #10;
        A = 4'b1100; B = 4'b1010; opcode = 3'b010; #10;
```

```
        A = 4'b1100; B = 4'b1010; opcode = 3'b011; #10;
        A = 4'b1010; opcode = 3'b100; #10;
        $finish;
    end

endmodule
```