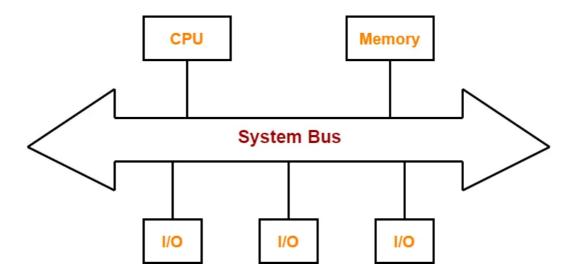
| System Bus in Computer Architecture Computer Organization and Architecture |
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| System Bus in Computer Architecture- |
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| What Is A System Bus? |
| |
| A bus is a set of electrical wires (lines) that connects the various hardware components of a computer system |
| It works as a communication pathway through which information flows from one hardware component to the other hardware component. |
| |
| A bus that connects major components (CPU, memory and I/O devices) of a computer system is called as a System Bus . |
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Tag: What are the types of buses in Computer Architecture

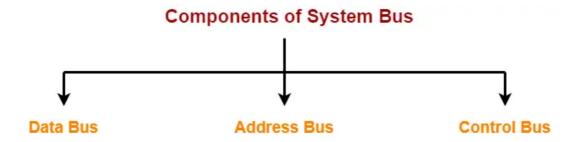


Why Do We Need Bus?

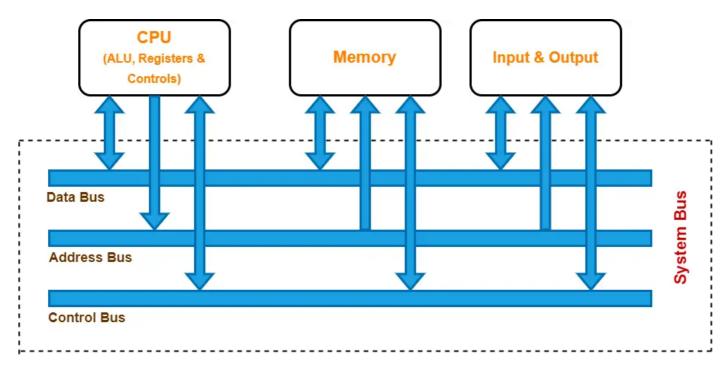
- A computer system is made of different components such as memory, ALU, registers etc.
- Each component should be able to communicate with other for proper execution of instructions and information flow.
- If we try to implement a mesh topology among different components, it would be really expensive.
- So, we use a common component to connect each necessary component i.e. BUS.

Components Of A System Bus-

The system bus consists of three major components-



- 1. Data Bus
- 2. Address Bus
- 3. Control Bus



Let us learn about each component one by one.

1) Data Bus-

- As the name suggests, data bus is used for transmitting the data / instruction from CPU to memory/IO and vice-versa.
- It is bi-directional.

Data Bus Width

- The width of a data bus refers to the number of bits (electrical wires) that the bus can carry at a time.
- Each line carries 1 bit at a time. So, the number of lines in data bus determine how many bits can be transferred parallely.
- The width of data bus is an important parameter because it determines how much data can be transmitted at one time.
- The wider the bus width, faster would be the data flow on the data bus and thus better would be the system performance.

Examples-

- A 32-bit bus has thirty two (32) wires and thus can transmit 32 bits of data at a time.
- A 64-bit bus has sixty four (64) wires and thus can transmit 64 bits of data at a time.

2) Control Bus-

- As the name suggests, control bus is used to transfer the control and timing signals from one component to the other component.
- The CPU uses control bus to communicate with the devices that are connected to the computer system.
- The CPU transmits different types of control signals to the system components.
- It is bi-directional.

What Are Control & Timing Signals?

Control signals are generated in the control unit of CPU.

Timing signals are used to synchronize the memory and I/O operations with a CPU clock.

| Typical | control | signals | hold | bv | control | bus- |
|---------|---------|---------|------|----|---------|------|

- Memory read Data from memory address location to be placed on data bus.
- **Memory write –** Data from data bus to be placed on memory address location.
- I/O Read Data from I/O address location to be placed on data bus.
- I/O Write Data from data bus to be placed on I/O address location.

Other control signals hold by control bus are interrupt, interrupt acknowledge, bus request, bus grant and several others.

Example-

When CPU wants to read or write data, it sends the memory read or memory write control signal on the control bus to perform the memory read or write operation from the main memory. Similarly, when the processor wants to read from an I/O device, it generates the I/O read signal.

3) Address Bus-

- As the name suggests, address bus is used to carry address from CPU to memory/IO devices.
- It is used to identify the particular location in memory.
- It carries the source or destination address of data i.e. where to store or from where to retrieve the data.
- It is uni-directional.

Example-

When CPU wants to read or write data, it sends the memory read or memory write control signal on the control bus to perform the memory read or write operation from the main memory and the address of the memory location is sent on the address bus.

If CPU wants to read data stored at the memory location (address) 4, the CPU send the value 4 in binary on the address bus.

Address Bus Width

• The addressing capacity of the system can be increased by adding more address lines.

Examples-

- An address bus that consists of 16 wires can convey 2¹⁶ (= 64K) different addresses.
- An address bus that consists of 32 wires can convey 2^{32} (= 4G) different addresses.

PRACTICE PROBLEMS BASED ON SYSTEM BUS-

Problem-01:

Which of the following system bus is used to designate the source or destination of the data on the bus itself?

- 1. Control bus
- 2. Data bus
- 3. Address bus
- 4. System bus

Solution-

The correct option is (C) Address bus.

Address bus carries the source or destination address of data i.e. where to store or from where to retrieve the data.

Problem-02:

| ised to transfer data | | |
|-----------------------|--|--|
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- 1. Data bus
- 2. Input bus
- 3. DMA bus
- 4. Output bus

Solution-

The correct option is (A) Data bus.

Data bus carries data / instruction from CPU to memory/IO and vice-versa.

Problem-03:

| How many memory locations a system with a 32-bit address bus can address | How many | memory locations | a system | with a 32-bit | address bus | can address? |
|--|----------|------------------|----------|---------------|-------------|--------------|
|--|----------|------------------|----------|---------------|-------------|--------------|

- 1. 2⁸
- 2. 2¹⁶
- 3. 2³²
- 4. 2⁶⁴

Solution-

The correct option is (C) 2^{32} .

 2^{32} memory locations can be addressed by a 32-bit address bus.

Problem-04:

How many bits can be transmitted at a time using a bus with 32 data lines?

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- 2. 16 bits
- 3. 32 bits
- 4. 1024 bits

Solution-

Each line carries one bit. So, a bus with 32 data lines can transmit 32 bits at a time.

Problem-05:

A microprocessor has a data bus with 64 lines and an address bus with 32 lines. The maximum number of bits that can be stored in memory is-

- 1. 32 x 2¹²
- 2. 32 x 2⁶⁴
- 3. 64 x 2³²
- 4. 64 x 2⁶⁴

Solution-

The correct option is (C) 64×2^{32} .

The amount of blocks that could be located is 2^{32} . Now, since data bus has 64 lines, so each block is 64 bits. Thus,

Problem-06:

| The | address | hus | with | a | ROM | Ωf | Size | 1024 | v | R | hite | ic_ |
|------|---------|-----|-------|---|------|----|------|------|---|---|------|-----|
| 1110 | auuless | บนจ | WILLI | а | LOIN | UΙ | SIZE | 1024 | _ | O | บแจ | 15- |

- 1. 8 bits
- 2. 10 bits
- 3. 12 bits
- 4. 16 bits

Solution-

The correct option is (B) 10 bits.

The size of the ROM is $1024 \times 8 = 2^{10} \times 8$. Here, 10 indicates the address bus and 8 indicates the data bus width.

Problem-07:

The data bus width of a ROM of size 2048 x 8 bits is-

- 1.8
- 2.10
- 3. 12
- 4. 16

Solution-

The correct option is (A) 8.

The size of the ROM is 2048 x 8 = 2^{11} x 8. Here, 11 indicates the address bus and 8 indicates the data bus width.

To gain better understanding about System Bus in Computer Architecture,

Watch this Video Lecture

Next Article- <u>Pipelining in Computer Architecture</u>