Certificate of Achievement

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Name of The Student Neeraj Singh

Roll no. ____________ Class B.TECH CS- Sec-24, P2

AFFIX YOUR PASSPORT SIZE PHOTO HERE

Examination Center ______________________________

Date of the Practical Examination ______________________________

Signature

Remarks: ______________________________

Index Of The Experiments Performed

S.no	Experiment Description	Page No.	Experiment Date	Submission Date	Remarks
1	To familiarize with Electrical and Electronic lab Equipment and basic electronics	2	20.1.22		
2	To verify (i) Kirchhoff's law (ii) Kirchoff's voltage law	4	20.1.22		
3	To verify the norton's theorem	6	20.1.22		
4	To verify the Thevenin's theorem	8	20.1.22		
5	observe the given waveform and calculate frequency, peak value, average value, RMS value and form factor.	10	20.1.22		
6	To plot the V-I characteristics of P-N junction Diode and calculate the forward and reverse resistance of the diode	12	20.1.22		
7	To plot the V-I characteristic and verify the functing of zener diode	14	20.1.22		
8	working of half/full wave rectifier	16	20.1.22		

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S.No	Resistor	Colour band	Calculated value of R(Ω)	Measured value of R(Ω) (design value)	Remark
1.	R1	Brown Red orange Silver	11.82 KΩ	$12 \times 10^3 \pm 10\%$ Ω	
2.	R2	Red Red orange Gold	21.80 KΩ	$22 \times 10^3 \pm 5\%$	
3.	R1 and R2		34 KΩ	34×10^3 KΩ	(Series)
4.	R1 and R2		7.66 KΩ	7.6×10^3 KΩ	(parallel)

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Experiment : 1

Date 20.1.22

Page No. 2

Experiment - 1

objective : To familiarize with measuring and testing equipments like multimeter, CRO, Function Generator, Power supply etc and also familize with bread board, resistor, capacitor etc calculate the Resistance value according the colour.

CLASSTIME

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Experiment : 2A

Date ______

Page No. 3

Aim: To verify the Kirchoff's current law (KCL)

objective: The objective of this lab activity is to verify Kirchoff's current law (KCL) using math and nodal analysis of the given circuit.

Theory: according to Kirchoff's current law, in any network of wires carrying current, the algebric sum of all current meeting at a junction is zero

apparatus required:- Regulated Power DC supply, PMMC ammeter, Resistance / Rheostats, connecting wire.

Observation

S.No.	Reading of ammeter A_1 (I_1)	Reading of ammeter A_2 (I_2)	Reading ammeter of A_3	$I_2 + I_3$

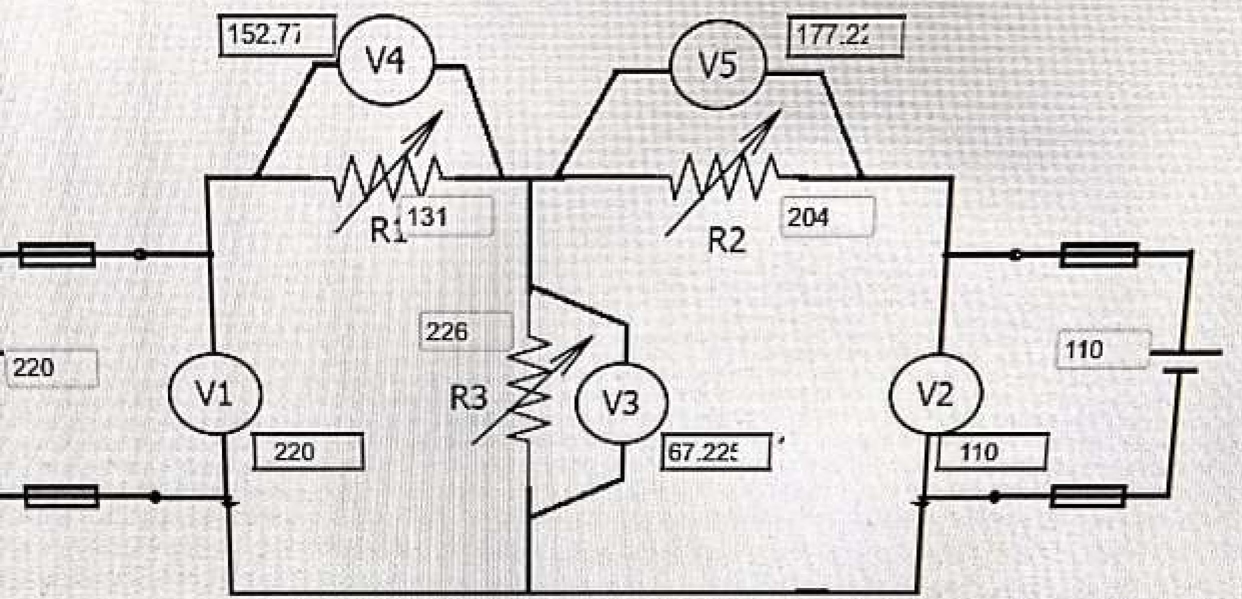
Working principle

The algebric sum of current in a network of conductors meeting a point is zero. Recalling that current is a signed quantity reflecting direction towards or away from node;

$$\sum_{k=1}^{N} I_k = 0$$

CLASSTIME

Experiment: Verification of Kirchoff's V



Input the val
Then click on

Observation Table

SL No.	Voltmeter Readings					Verification of KVL	
	V1	V2	V3	V4	V5	V2+V4	-V3+V4
1	220	152.30769	177.69230	67.692307	110	219.99999	110.00000
2	220	153.86525	176.13474	66.134741	110	219.99999	110.00000
3	220	161.55578	168.44421	58.444218	110	220	109.99999
4	220	157.71768	172.28231	62.282310	110	220.00000	109.99999
5	220	152.77407	177.22592	67.225921	110	220.00000	109.99999

Click here to print

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Experiment :

Date ___________

Page No. ___________

N is the total no. of branches.

Result

(i) calculate the ideal voltage and current for each element in the circuit and compare them to the measured values

(ii) compare the percentage error in the measurements and provide a brief explanation for the error.

precation :

- all connection should be tight
- all steps should be followed carefully.

CLASSTIME

Neeraj singh p2 bee lab

Experiment : 2B

Date ______
Page No. ______

Aim: to verify the Kirchoff voltage law (KVL)

objective: The objective of this lab activity is to verify Kirchoff' voltage (KVL) using mesh and nodal analysis of the circuit.

Theory:- according to Kirchoff's voltage law, in any closed or mesh, the algebric sum of emf acting on circuit is equal to the algebric sum of the product of the current and resistance of each part of the circuit

apparatus req: Regulated power DC supply, PMMC voltmeter, Resistance, connecting wire.

Observation

S.No.	Reading (V_1)	(V_2)	(V_3)	(V_4)	$V = V_1 + V_2$	$V_2 = V_3 + V_4$

principle:- The sum of the emf in any closed loop is equivalent to the sum of the potential drop in that loop.

$$\sum_{K=1}^{n} V_K = 0$$

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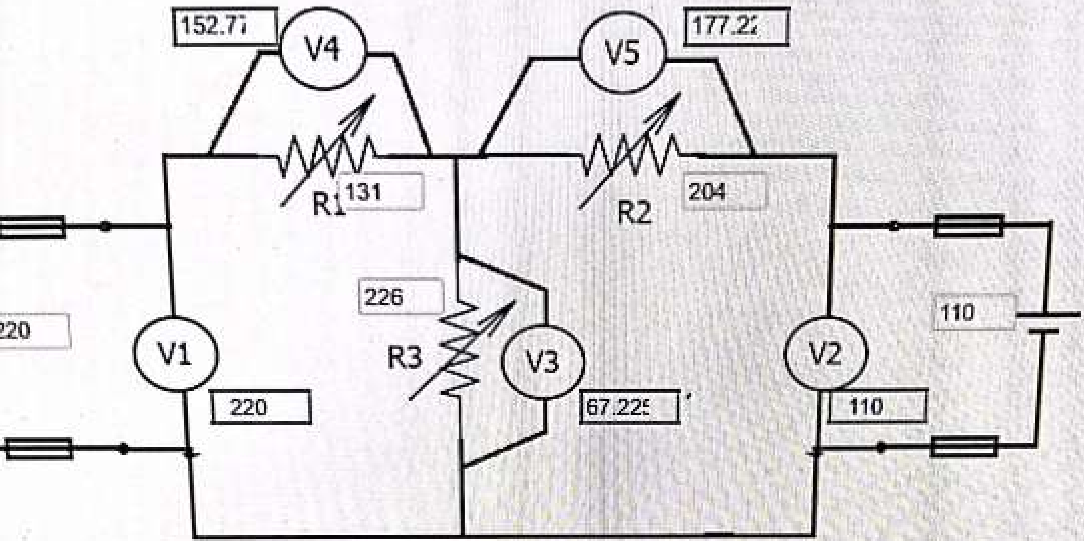
Experiment: Verification of Kirchoff's Voltage



Control

Input the values of Voltage
Then click on Run.

Run

Observation Table

SL No.	Voltmeter Readings					Verification of KVL	
	V1	V2	V3	V4	V5	V2+V4	-V3+V4
1	220	152.30769	177.69230	67.692307	110	219.99999	110.00000
2	220	153.86525	176.13474	66.134741	110	219.99999	110.00000
3	220	161.55578	168.44421	58.444218	110	220	109.99999
4	220	157.71768	172.28231	62.282310	110	220.00000	109.99999
5	220	152.77407	177.22592	67.225921	110	220.00000	109.99999

Click here to print

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Experiment : Date ______ Page No. ______

Result:

1) Calcalate the ideal voltage - and current for each element in the circuit and compare them to the measured values.

2) compare the percentage error in the two measurements and provide a brief explanation for the error.

precaution

→ all connection should be tight

→ all steps should be followed carefully.

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Experiment : 3

Date ________
Page No. ________

Aim : to verify the norton theorem

Apparatus req :- two regulated DC power, PMMC voltmeter, PMMC ammeter, resistance / rheostat, connecting wire.

theory :- according to theorem if a resistor of RL ohms be connected b/w any two terminals of a linear bilateral network, then the resulting current through load resistor will be equal to $\frac{R_{th} I_{sc}}{R_L + R_{th}}$.

Observation

S.No	Short circuit current load terminal (I_{sc})	Equivalent resistance across the load	load current $I = \frac{R_{th} I_{sc}}{R_L + R_{th}}$	Measured I_L

Calculation :- $I_L = \frac{R_{th} I_{sc}}{R_L + R_{th}}$

:

Script alerts in your browser.
resistances (R_1, R_2, R_3 & R_L) close to their
maximum values. Choose any arbitrary values of V_1

ent Part Select:

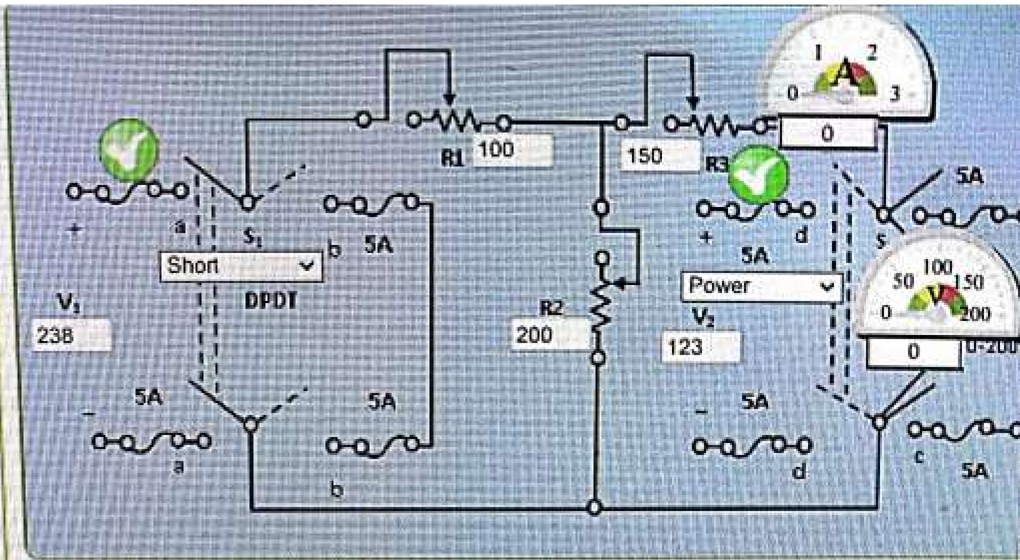
tch of S_1 to Power and S_2 to Load and Simulate the
rom Case 1 tab. Observe the result of load current.

Short circuit current analysis:
itch S_1 to power and S_2 to Short and Simulate the
and read Norton short circuit current (I_{sc}) from Case

n Resistance analysis:
witch S_1 to short and S_2 to power and Simulate the
n and read Norton resistance (Rn) from Case 2(b) tab.

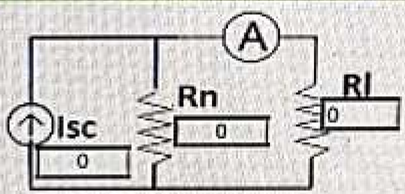
: Using I_{sc} and R_n determine Load Current
te the program and read Load current (I_L) from Case 3
ompare the load currents (I_L) obtained from Case 1 tab.
lick the button to fill the data to the observation table.

Moving Coil.
T- Double pole Double throw.
- All the resistances are in ohms.



Case 1 | Case 2(a) | Case 2(b) | Case 3

Click on simulate to get the Load Current(I_L) from the Thevenin equivalent parameter of the above ckt.



Load Current(I_L) : 0

Simul

Fill data to th

ervation Table:

Serial no. of Observation	Load Current(I_L) from case 1	Load Voltage(V_L)	Load Resistance (R_L)=V_L/I_L	Norton current(I_{sc}) from case 2(a)	2nd Voltage source(v) from case 2(b)	Ammeter Reading(I) from case 2(b)	Norton Resistance R_n=V/I	Load (I_L)=I_{sc}*I
1st	0.28387	85.161	300	0.67692	110	0.50769	216.67	0.2
2nd	0.29677	89.031	300	0.70769	115	0.53077	216.67	0.2
3rd	0.30710	92.130	300	0.73231	123	0.56769	216.67	0.3
4th	0.30710	92.130	300	0.73231	123	0.56769	216.67	0.3
5th								

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Experiment :

Date

Page No.

Result and Discussion

The value of short circuit I_{sc} is — Amp

The value of norton resistance is — Ω

It will be found that measured value of current through flowing through the load I_L is the same as determined by norton's theorem.

Precaution

- all connection should be tight
- all steps should be following carefully
- Reading and calculation should be taken carefully
- don't touch the live terminal

Neeraj singh p2 bee lab

Experiment : 4

Date ____________

Page No. ________

Aim: to verify the Thevin's Theorem

apparatus required : two regulated DC Supply, PMMC voltmeter, PMMC ammeter, Resistances, connecting wire.

theory: according to this theorem if a resistor of RL ohms be connected b/w any two terminals of a linear bilateral network, then the resulting current through load resistor will be equal to $\frac{V_{th}}{R_L + R_{th}}$ where V_{th} is pot. diff.

Observation

S.No	open circuit voltage RL	Rth	$I_L = \frac{V_{th}}{R_L + R_{th}}$	Measured IL

precaution

→ all connection should be tight

→ all steps should be followed carefully

→ Don't touch the live material

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Verification of Thevenin's Theorem

rocedure:

ep all the resistances (R_1, R_2, R_3, R_L) close to their pective maximum values. Choose any arbitrary values of and V_2.

periment Part Select:

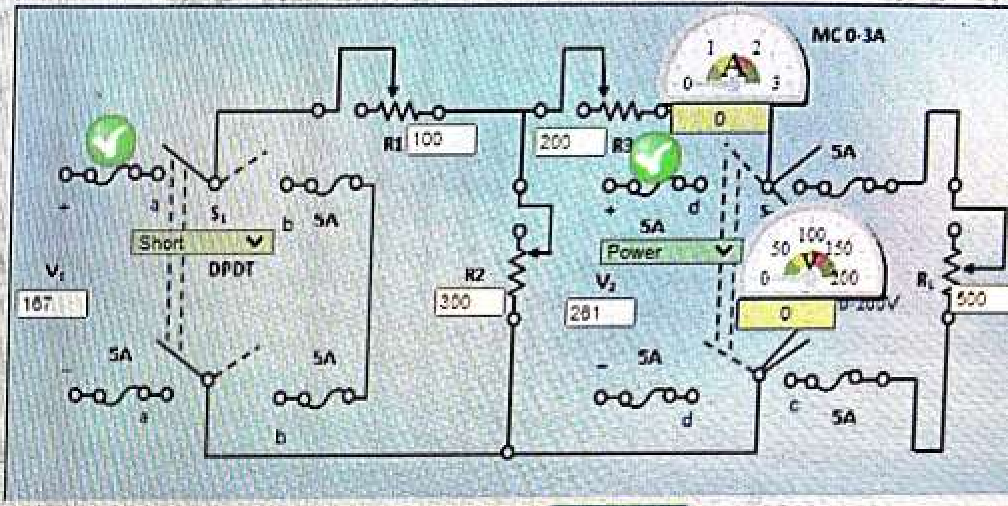
se 1:
ect switch of S_1 to Power and S_2 to load. Simulate the gram. Observe the result from Table 1.

se-2:
hevenin Voltage analysis:
ply switch S_1 to power and S_2 to intermediate. Simulate program.Read Thevenin voltage (V_{th}) from Case 2 tab.

hevenin Resistance analysis:
ply switch S_1 to short and S_2 to power. Simulate the gram. Read Thevenin resistance (R_{th}) from Case 2 tab.

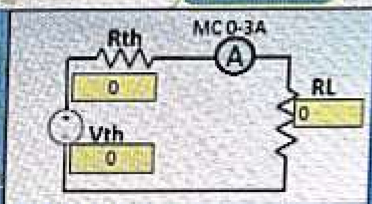
e-3: Using V_{th} and R_{th} determine Load Current:
cify the load resistance in case of the result table as the e load resistance entered in the main circuit. Simulate the gram. Read Load current (I_L) from Case 3 tab. Compare load currents (I_L) obtained from above two cases.

-Moving Coil.
DT- Double pole Double throw.
:- All the resistances are in ohms.



Case 1 | Case 2(a) | Case 2(b) | Case 3

Click on simulate to get the Load Current(I_L) from the Thevenin equivalent parameter of the above circuit



Simulate

Load Current(I_L) : 0

Fill data to the table

rvation Table:

l no. of rvation	Load Current(I_L) from case 1	Load Voltage(V_L)	Load Resistance (R_L)=V_L/I_L	Thevenin Voltage(V_{th}) from case 2(a)	2nd Voltage source(v) for case 2(b)	Ammeter Reading(I) from case 2(b)	Thevenin Resistance R_{th}=V/I	Load current (I_L)=$V_{th}/(R_{th}+R_L)$
[illegible]	0.10645	53.225	500	82.500	220	0.80000	275.00	0.10645
[illegible]	0.11613	58.065	500	90.000	230	0.83636	275.00	0.11613
[illegible]	0.13452	67.26	500	104.25	239	0.86909	275.00	0.13452
[illegible]	0.15000	75	500	116.25	250	0.90909	275.00	0.15000
[illegible]	0.16161	80.805	500	125.25	261	0.94909	275.00	0.16161

...ximum values. Choose any arbitrary values of

t Part Select:

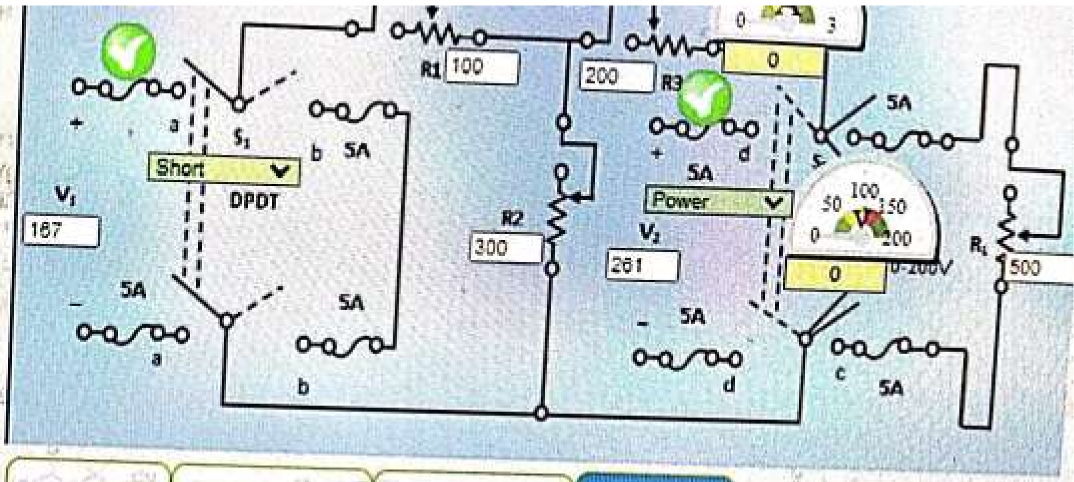
of S_1 to Power and S_2 to load. Simulate the
erve the result from Table 1.

oltage analysis:
$_1$ to power and S_2 to intermediate. Simulate
ead Thevenin voltage (V_{th}) from Case 2 tab.

esistance analysis:
$_1$ to short and S_2 to power. Simulate the
Thevenin resistance (R_{th}) from Case 2 tab.

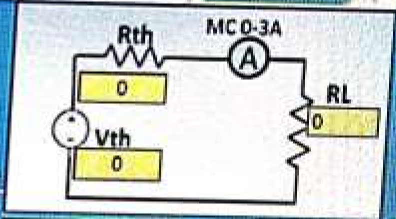
V_{th} and R_{th} determine Load Current:
l resistance in case of the result table as the
ance entered in the main circuit. Simulate the
Load current (I_L) from Case 3 tab. Compare
s (I_L) obtained from above two cases.

oil.
pole Double throw.
sistances are in ohms.



Case 1 | Case 2(a) | Case 2(b) | Case 3

Click on simulate to get the Load Current(I_L) from the Thevenin equivalent parameter of the above circuit.



Load Current(I_L) : 0

Simulate

Fill data to the table

ble:

Current(I_L) from case 1	Load Voltage(V_L)	Load Resistance (R_L)=V_L/I_L	Thevenin Voltage(V_{th}) from case 2(a)	2nd Voltage source(v) for case 2(b)	Ammeter Reading(I) from case 2(b)	Thevenin Resistance R_{th}=V/I	Load current (I_L)=V_{th}/(R_{th}+R_L)
0.10645	53.225	500	82.500	220	0.80000	275.00	0.10645
0.11613	58.065	500	90.000	230	0.83636	275.00	0.11613
0.13452	67.26	500	104.25	239	0.86909	275.00	0.13452
0.15000	75	500	116.25	250	0.90909	275.00	0.15000
0.16161	80.805	500	125.25	261	0.94909	275.00	0.16161

Experiment : 5

Date

Page No.

Aim: to observe the given waveform and calculate its frequency, Peak value, Average value, RMS value and form factor

Theory:- Peak value = V_P

Peak to peak value = $V_{PP} = 2V_P$

Period = T[s]

frequency $f = \frac{1}{T}$ (Hz)

ω (angular freq.) = $\omega = 2\pi f$ (rad/s)

phase = ϕ

Apparatus req: function generator, CRO

Observation:

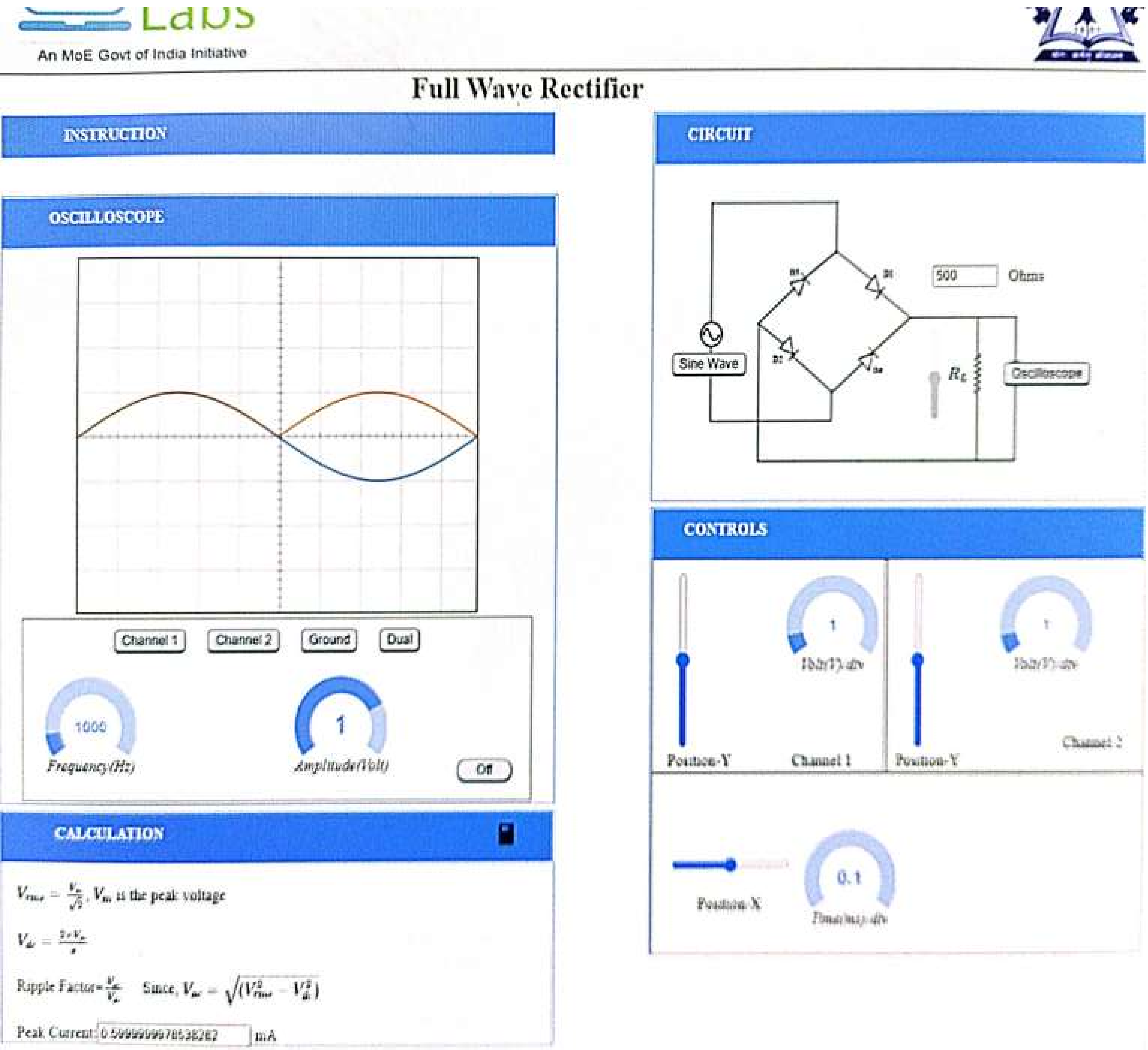
S.No.	Sine wave	triangular wave	square wave
Peak voltage			
Time period			

Calculation :- calculate the listed electrical parameter using formula

precaution:

all connection should be tight

all steps should be followed carefully.



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Experiment : 6 Neeraj singh p2 bee lab

Date ____________

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Aim: to verify the functionality of PN junction diode in forward bias and reverse bias.

Objective: To study volt-ampere characteristics of P-N diode and also find cut-in voltage for p-n junction diode

Theory: A PN junction diode is formed when a single crystal of semiconductor is doped with acceptor impurities on one side and donor impurities on the other side. It has two terminals called electrodes, one each from P-region and N-region. Due to two electrodes it is called Diode.

Biasing of PN junction diode.

applying external D.C. voltage to any electronic device is called biasing. There is no current in the unbiased PN junction at equilibrium. Depending upon the polarity of the D.C. voltage externally apply to diode, the biasing is classified as forward biasing and reverse biasing

forward bias operation: The P-N junction support uni-directional current flow. If +ive terminal of the input supply is connected to anode (P-side) and -ive terminal of the input supply is connected the cathode. The diode is said to be forward bias.

Reverse bias operation: If a negative terminal of the input supply is connected to ~~cathode~~ anode (p-side) and -ive terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased.

CLASSTIME

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Experiment : Neeraj singh p2 bee lab

Date ________

Page No. ________

Diode current equation :

$I = I_o(e^{V/\eta V_T} - 1)$

Observation

forward bias

RPS voltage (V_S)	forward voltage across diode (V_f)	forward current through diode I_f (mA)

Reverse Bias :

RPS Voltage (V_S)	Reverse voltage V_r	Reverse current I_f (μA)

CLASSTIME

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Zener Diode - LOAD Regulator

INSTRUCTION

CONTROLS

DC volt : Volt

Zener Diode(V_Z) : Volt

Resistance(R_S) : Ohms

Resistance(R_L) : Ohms

Print It

Take another sets of Output Volatge for another Zener value

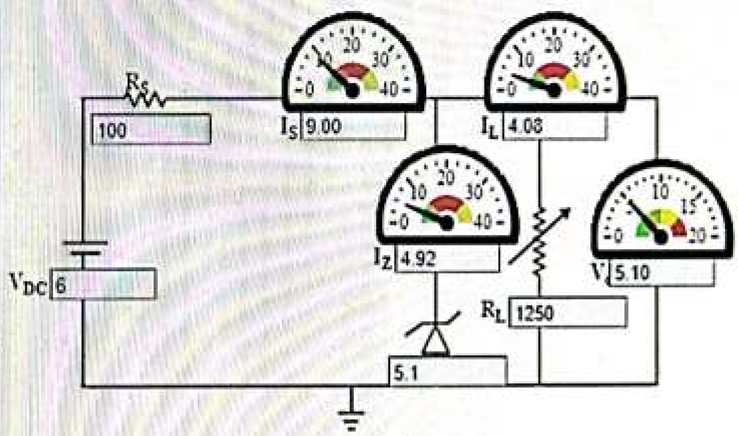
EXPERIMENTAL TABLE

DC Voltage (V_{DC}): 6 V Zener Voltage(V_Z): 5.1 V

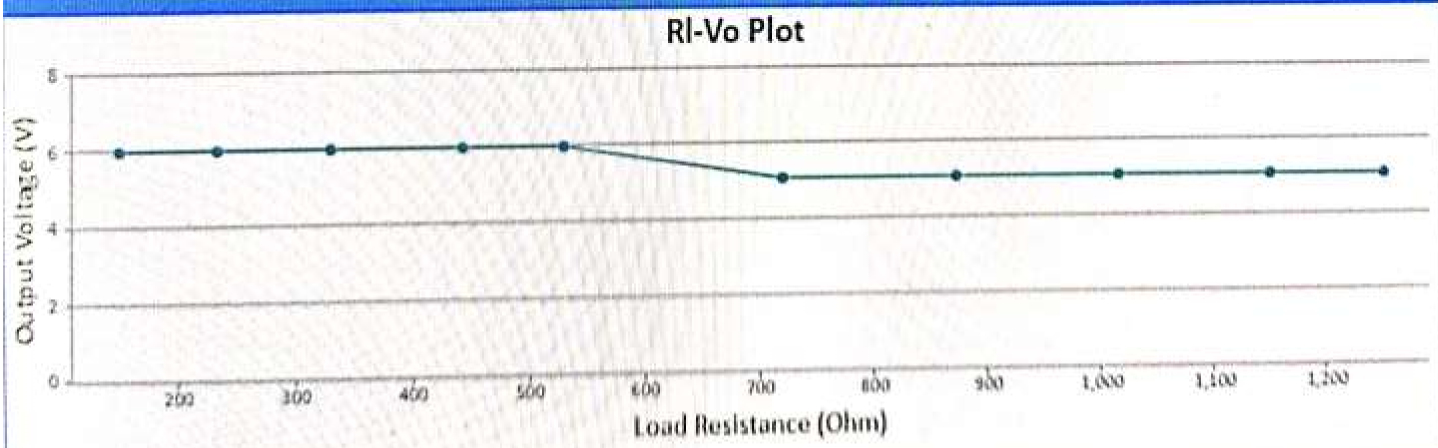
Series Resistance(R_S): 0.1 KΩ

Serial No.	Load Resistance(R_L) Ohm	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_O) V	% Voltag Regulatio
1	150	34.0	0	6	40.0
2	232	22.0	0	6	30.1
3	328	15.5	0	6	23.4
4	442	11.5	0	6	18.5
5	528	9.66	0	6	15.9

Add to Table | Plot | Clear



GRAPH PLOT



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Zener Diode - LINE Regulator

INSTRUCTION

EXPERIMENTAL TABLE

Zener Voltage(V_Z): 5.1 V

Series Resistance(R_S): 1 KΩ

Load Resistance (R_L): 2 KΩ

Serial No.	Unregulated supply voltage(V_S) V	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_O) V	% Voltage Regulation
1	0	2.55	0	0	NaN
2	1.4	2.55	0	1.4	100
3	3.6	2.55	0	3.6	100
4	6.4	2.55	-1.250	5.10	83.3
5	8.6	2.55	0.950	5.10	62.5
6	11.6	2.55	3.950	5.10	45.5

CONTROLS

DC volt : Volt

Zener Diode(V_Z) : Volt

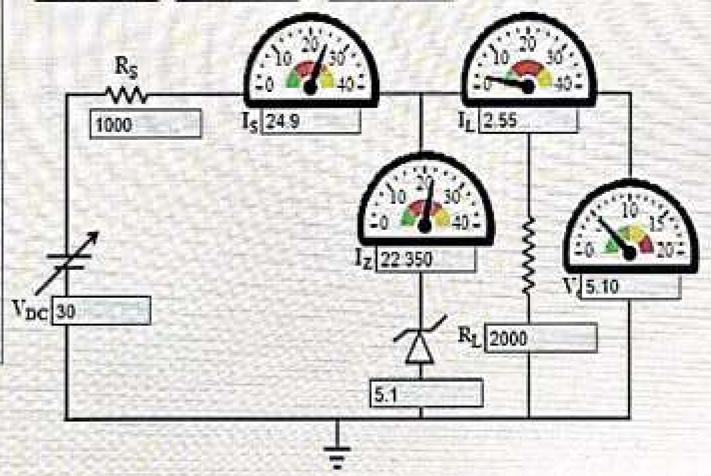
Resistance(R_S) : Ohms

Resistance(R_L) : Ohms

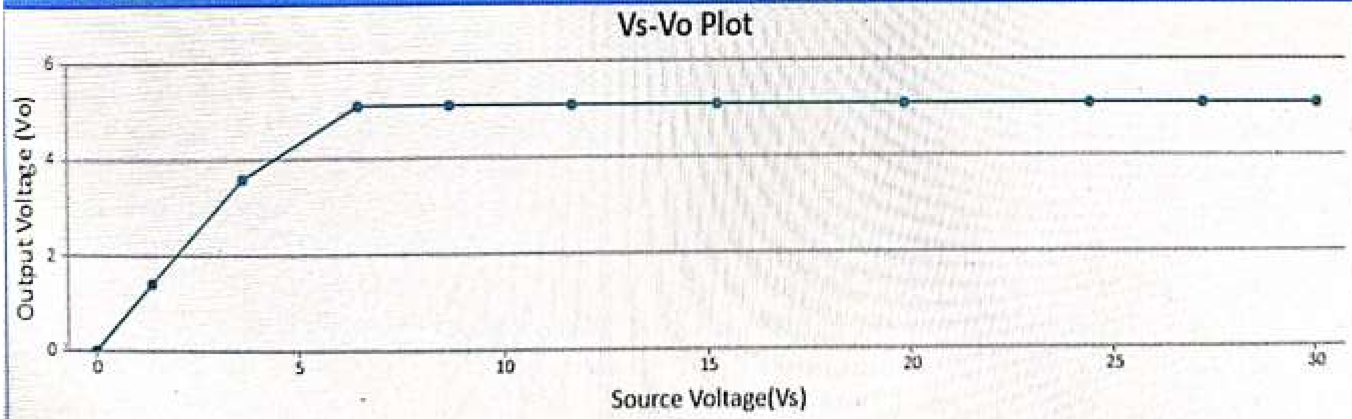
Print It

Take another sets of Output Volatge for another Zener value

Add to Table | Plot | Clear



GRAPH PLOT



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Experiment :

Date

Page No.

Result :

1) Calculate the ideal voltage and current for each element in the circuit and compare them to the measured value.

2) Compute the percentage error in the two measurement and provide a brief explanation.

precaution

- while doing the experiment do not exceed the reading of the diode. This may lead to damaging of the diode

- connector voltmeter and ammeter in correct polarity as shown.

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Experiment : 7
Date
Page No.

Exp-7

Aim: To plot V-I characteristics and verify the functionality the regulation action of zener diode

Objective: to plot the volt-ampere characteristic of zener diode and also find zener Breakdown voltage in reverse Biased

Theory:
Zener diode are a special kind of diode which permits current to flow in forward direction. What makes them different from other diodes is that zener diode will also allow current to flow in the reverse direction when the voltage is above a certain value. This break down voltage is called as the zener voltage.

avalanche breakdown
when the diode is in the reverse bias condition, the width of the depletion region is more. If both p-side and n-type side of the diode are lightly doped, depletion region at the junction widens.

zener breakdown
If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces compared to the width in normal doping. applying in reverse bias causes a strong electric field get applied across the devices. as the reverse bias is increased, the electric field become strong enough to rupture covalent band.

CLASSTIME

zenor diode as voltage regulator

The function of a regulator is to provide a const. output voltage to a load connected in parallel with it in spite of the ripple in the supply voltage or the variation in the load current and the zenor diode will continue to regulate permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value.

observation

Experiment :

Date

Page No.

Result

(1) Calculate the ideal voltages and current for each element in the circuit and compare them to the measured values.

(2) compute the percentage error in the two measurement and provide a brief explanation for the error.

precaution:

1) while doing the experiment do not exceed the reading of the diode

2) connect voltmeter and ammeter in correct polarities as shown in the circuit diagram

Experiment : 8

Date

Page No.

Aim: To study working of the half / full wave bridge rectifier and calculate its efficiency.

Objective: To verify the working of full wave rectifier circuit and calculate its efficiency

Apparatus req.: CRO, Multimeter, Trainer kit, Bread Board, connecting wire, diode, Power supply.

Working:- The full wave bridge rectifier circuit contains four diodes D1, D2, D3, D4 connected to form a bridge. The ac supply to be rectified is applied to the diagonally opp. ends of the bridge through the transformer. B/w other two ends of the bridge, the load resistance RL is connected

Calculation: Ripple factor of FWR = ac voltage o/p / dc =

Result:- The output dc voltage is little less than the theoritical value.

→ There is little diff. b/w theo. and measured value of ripple factor

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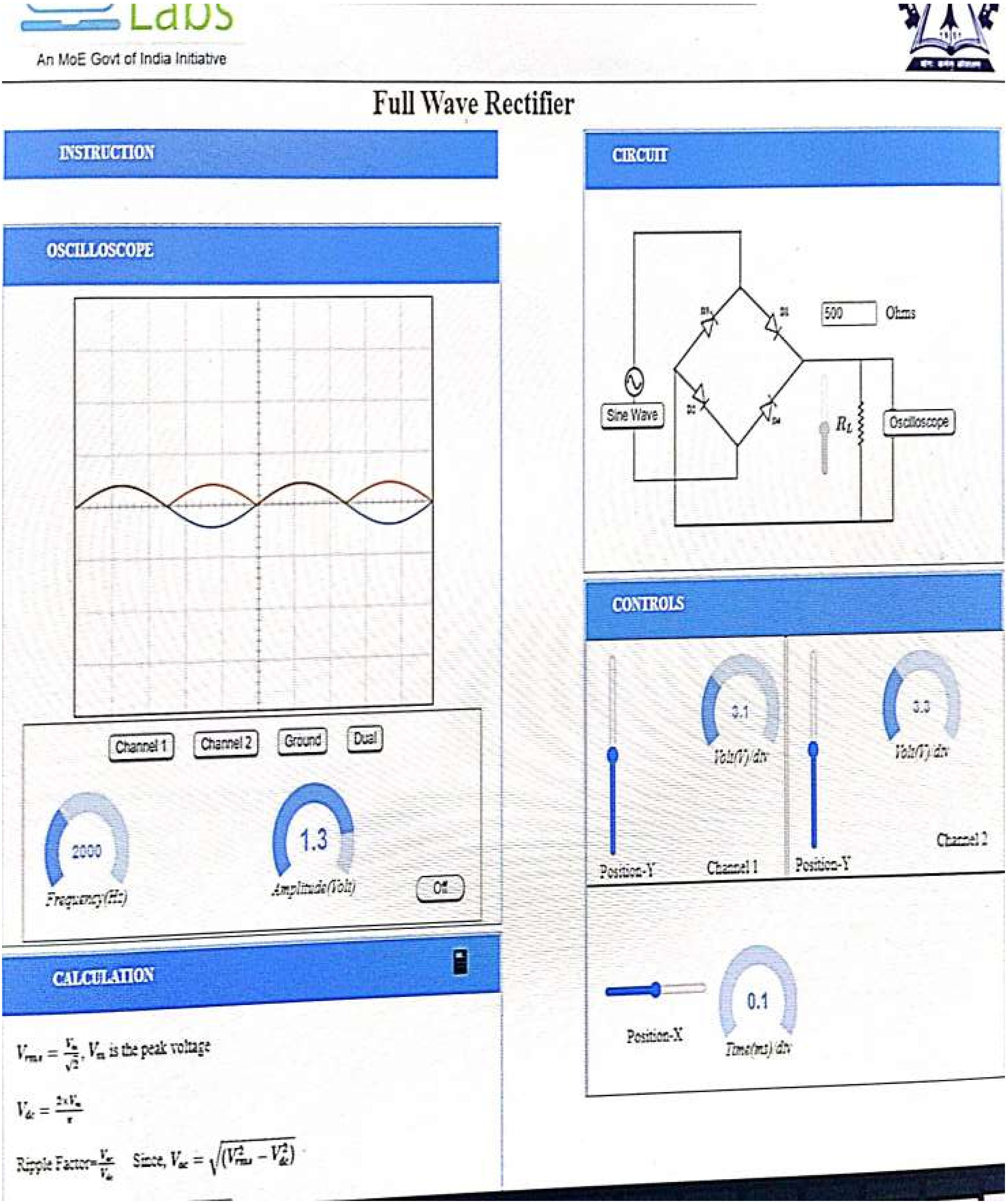

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