Sequential Logic Circuit Design
Module III (Lec-2)

SR Latch

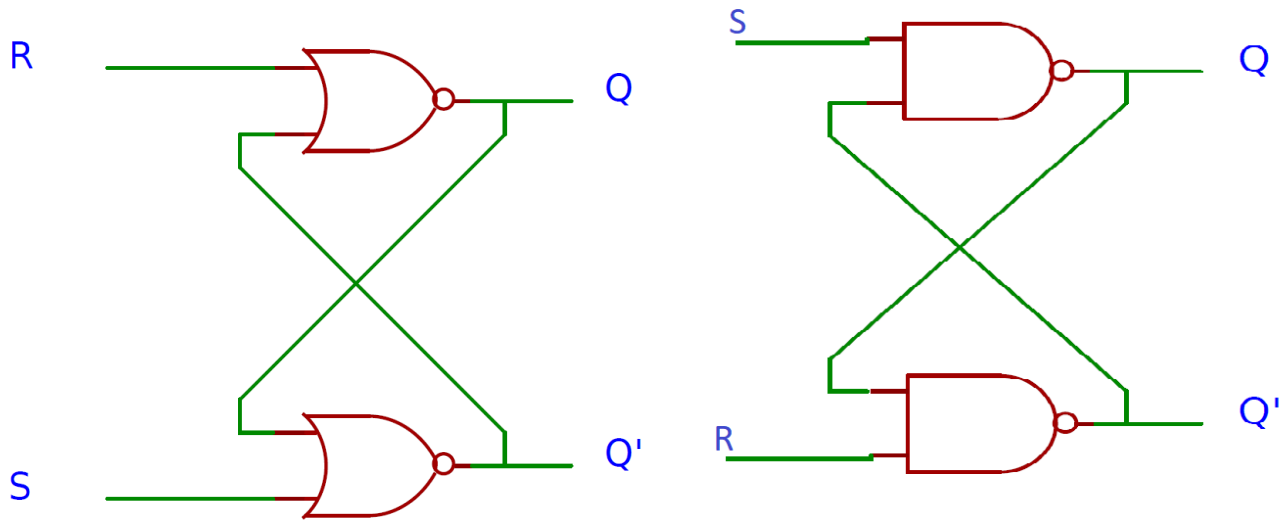
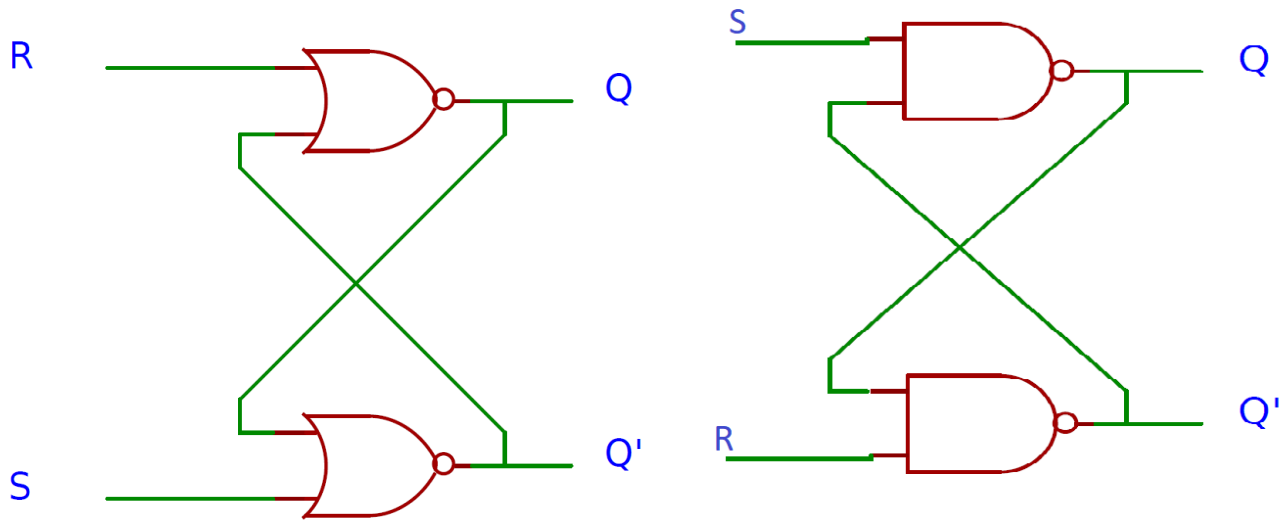


Figure: SR Latches using NOR and NAND Gates

SR Latch is a circuit with:

- Two cross-coupled NOR gate or 2 cross-coupled NAND gate.

SR Latch



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- Two inputs S for SET and R for RESET.

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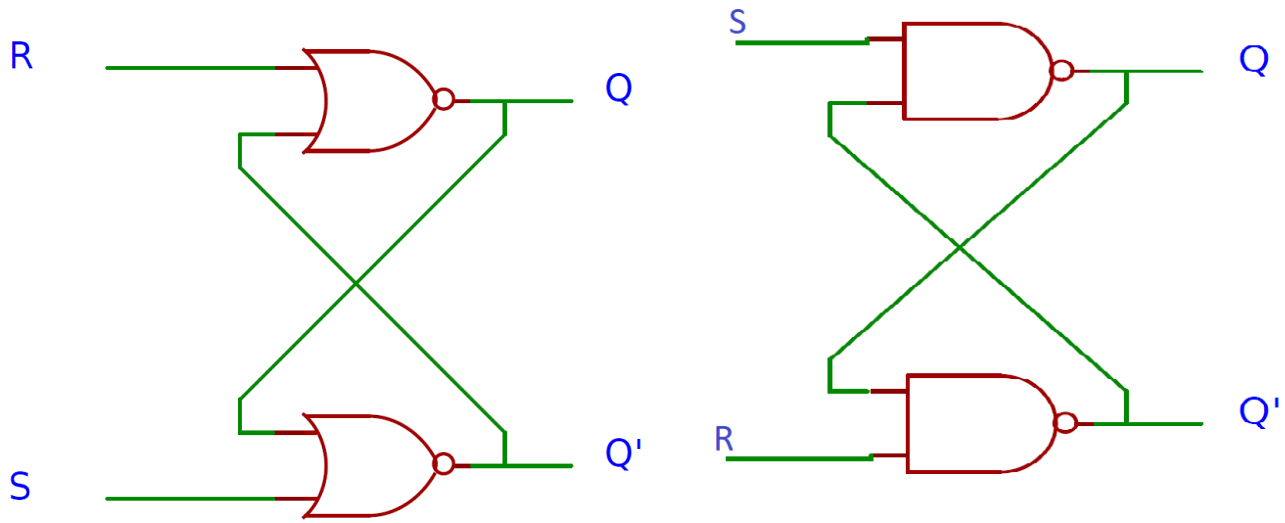

Figure: SR Latches using NOR and NAND Gates

SR Latch is a circuit with:

- Two cross-coupled NOR gate or 2 cross-coupled NAND gate.
- Two inputs S for SET and R for RESET.
- Two outputs Q, Q'. Both outputs are complement to each other.

SR Latch using NAND Gates

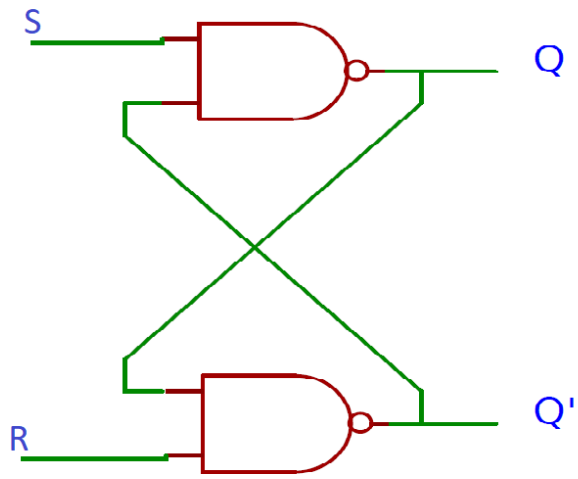

Figure: Logic Diagram of SR Latch

Table: Truth Table for SR Latch

S	R	Q
0	0	Invalid state
0	1	1
1	0	0
1	1	Previous state

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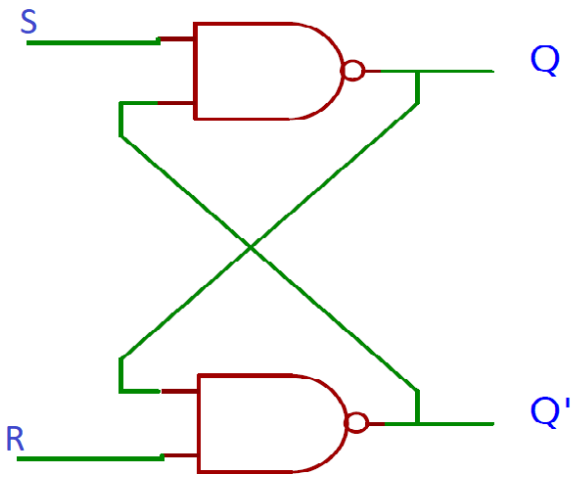

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- When both inputs S= R=0, the outputs Q and Q' =1.

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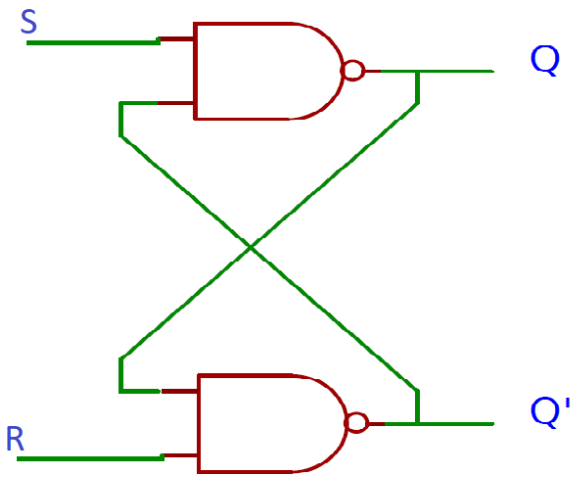

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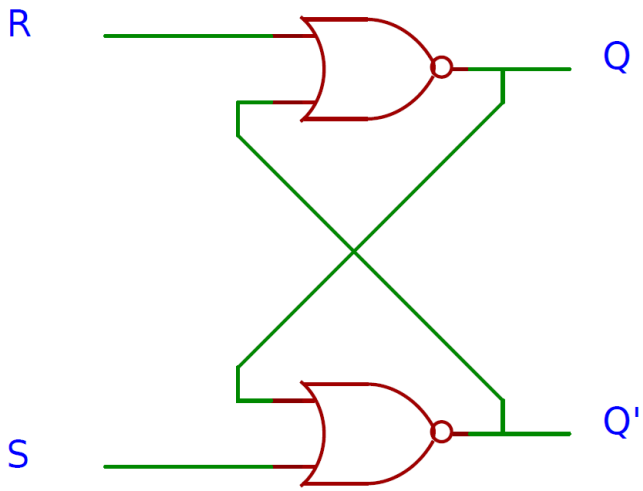
- When both inputs S= R=0, the outputs Q and Q' =1.
- The valid states only when (Q=0,and Q' =1) or (Q = 1, and Q'=0).

SR Latch using NOR Gates



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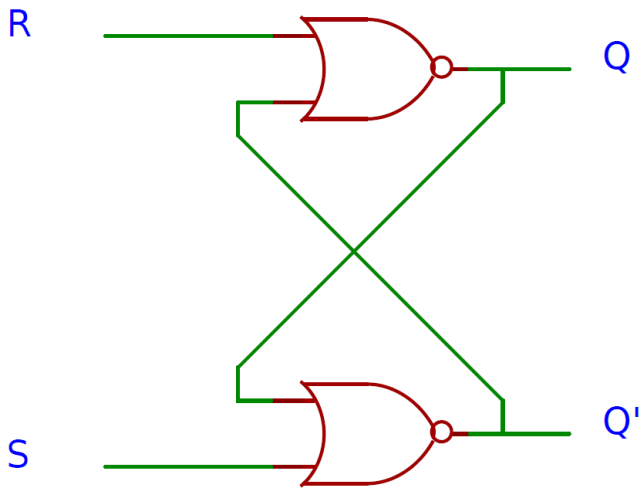
SR Latch using NOR Gates



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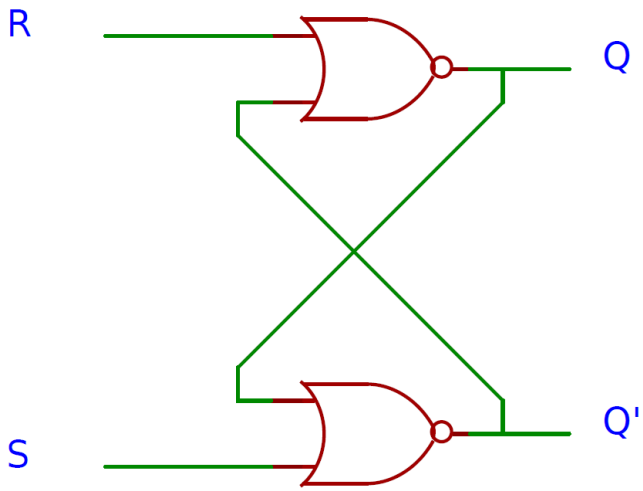
SR Latch using NOR Gates



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- When both inputs S= R=1, the outputs Q and Q' =0.
- The truth table of NOR latch is opposite to the NAND latch.

Flip Flop

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Flip Flops Classification

[1] SR Flip Flop
[2] JK Flip Flop
[3] D Flip Flop
[4] T Flip Flop

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Procedure for Designing of Flip Flops

[1] Truth Table
[2] Characteristic Table
[3] Characteristic Equation
[4] Excitation Table

SR Flip Flop

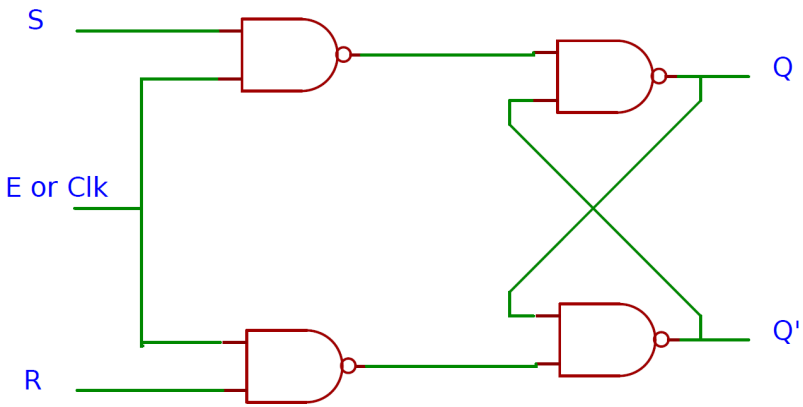
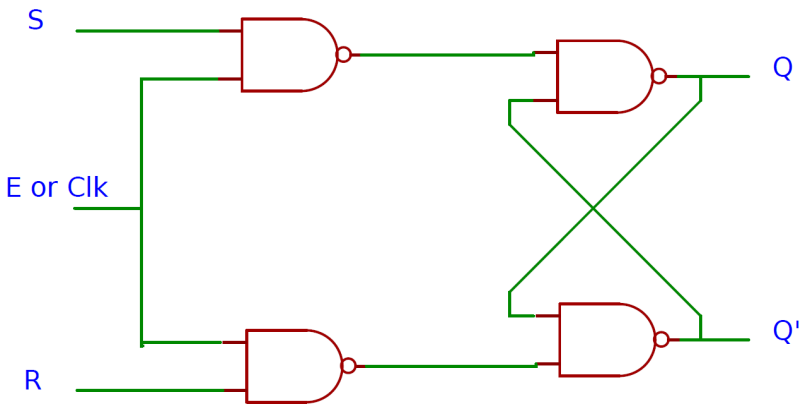


Table: Truth Table for SR Flip Flop

Clk	S	R	Q
0	×	×	Previous state
1	0	0	Previous state
1	0	1	0 (Reset State)
1	1	0	1 (Set State)
1	1	1	Invalid state

SR Flip Flop



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- The control input (E or Clk) acts as an enable signal or clocked pulse for the two inputs.

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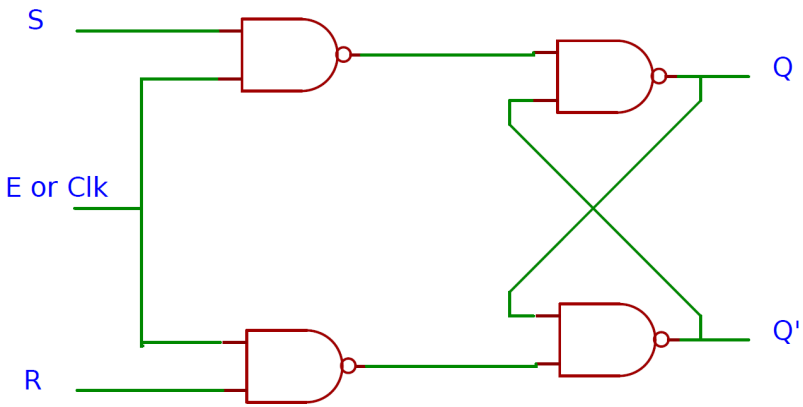

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Clk	S	R	Q
0	×	×	Previous state
1	0	0	Previous state
1	0	1	0 (Reset State)
1	1	0	1 (Set State)
1	1	1	Invalid state

- The control input (E or Clk) acts as an enable signal or clocked pulse for the two inputs.
- When **E=0**, the circuit remains in the previous state.
- When **E goes to 1**, information from the S or R input is allowed to get the output.

SR Flip Flop

Table: **Characteristic Table** for SR Flip Flop

S	**R**	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	$\times$
1	1	1	$\times$

SR Flip Flop

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S	**R**	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	$\times$
1	1	1	$\times$

Table: **Excitation Table** for SR Flip Flop

Q_n	Q_{n+1}	**S**	**R**
0	0	0	$\times$
0	1	1	0
1	0	0	1
1	1	$\times$	0

SR Flip Flop

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S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	$\times$
1	1	1	$\times$

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Q_n	Q_{n+1}	S	R
0	0	0	$\times$
0	1	1	0
1	0	0	1
1	1	$\times$	0

K Map

SR Flip Flop

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S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	$\times$
1	1	1	$\times$

Characteristic Equation

$$Q_{n+1} = S + \bar{R}Q_n$$

Table: **Excitation Table** for SR Flip Flop

Q_n	Q_{n+1}	S	R
0	0	0	$\times$
0	1	1	0
1	0	0	1
1	1	$\times$	0

K Map