Digital Logic Design
(ECE 1003)

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VIT®
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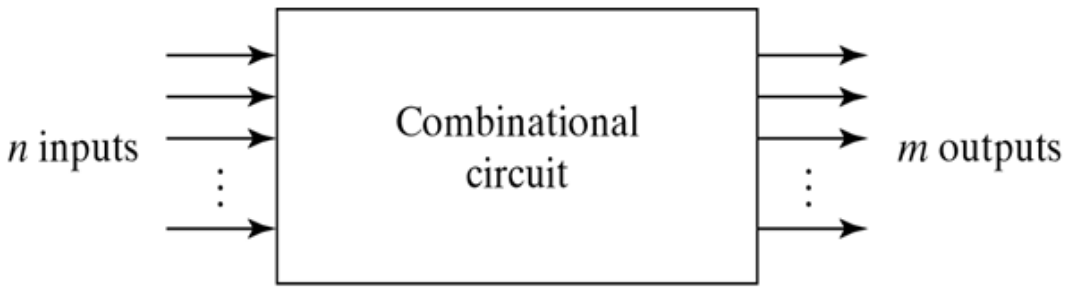
Sequential Logic Circuit Design
Module III

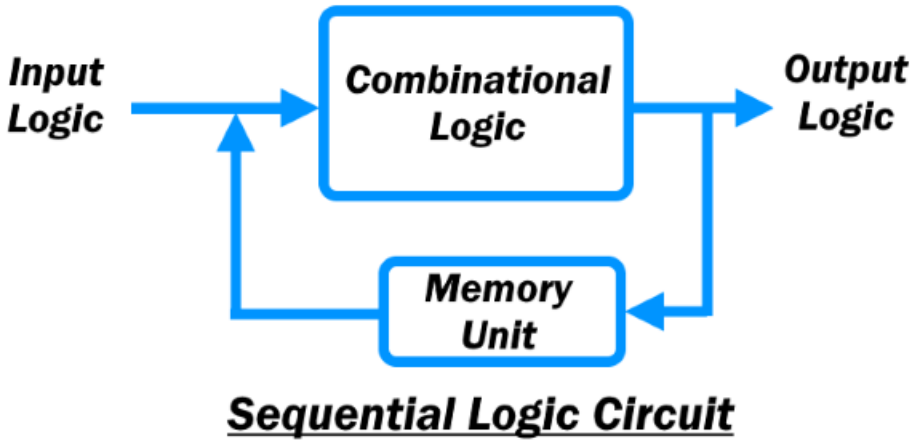
Combinational Circuits (Recall)

- Logic circuits for digital systems may be combinational or sequential.
- A combinational circuit consists of input variables, logic gates, and output variables.
- Present output depends only on the the present input.
- There is no memory and feedback in combinational circuits.



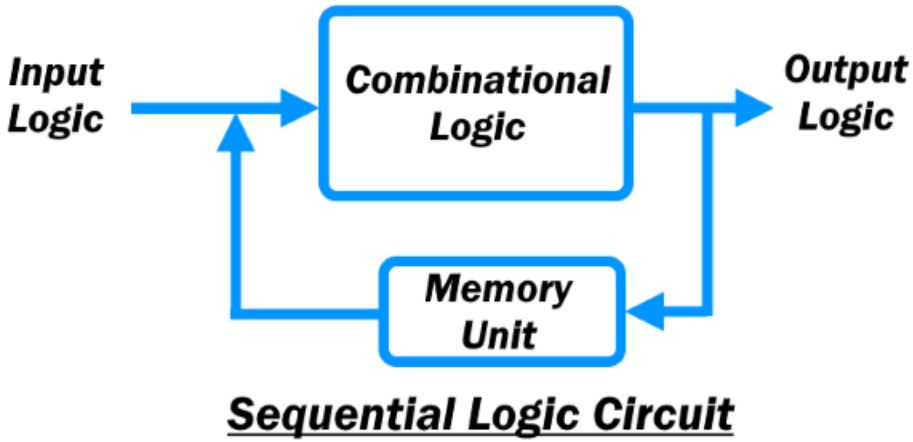
Block Diagram of Combinational Circuit

Sequential Circuits



- A sequential logic circuit consists of a combinational circuit and a memory element.

Sequential Circuits



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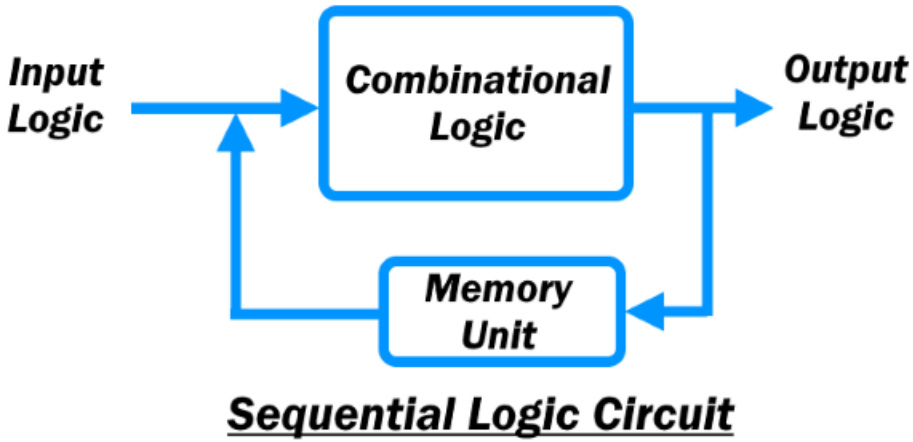

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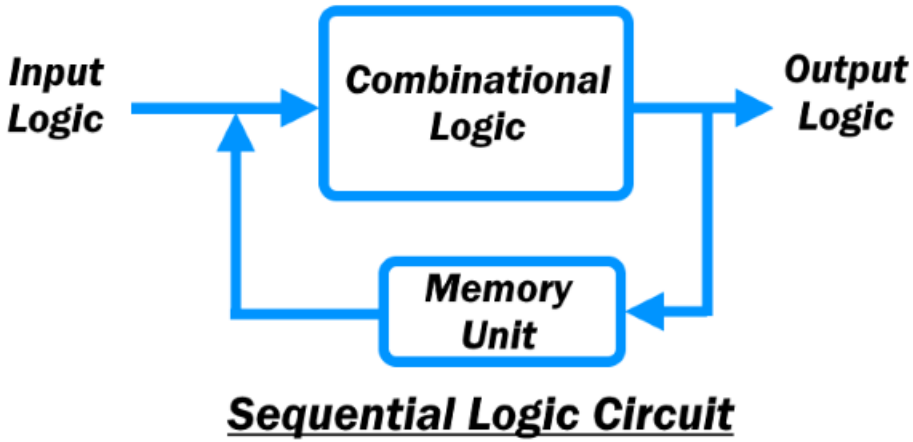

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- Present output depends on the the present input and past output.
- There is a memory and feedback path in the sequential circuits.
- The sequential circuit is capable to store the binary information.

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3. The output of the circuit is affected only at the active edge of clock.	4. The output of these circuits may change at any instant as soon as input is changed.
4. Flip flops are used in synchronous sequential circuits	5. Latches are used in the asynchronous sequential circuits.

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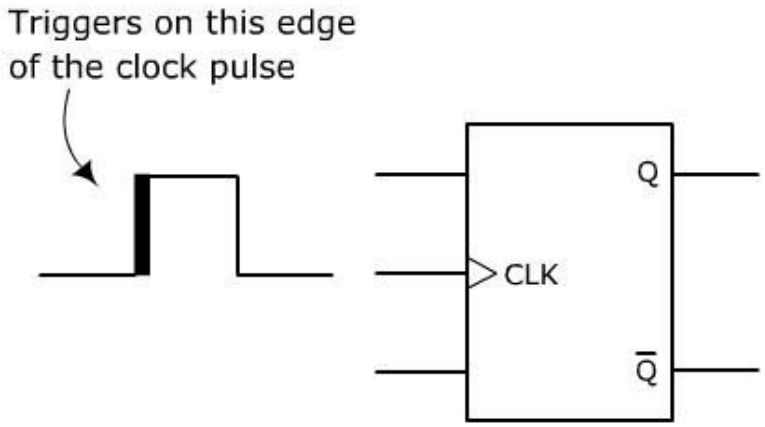
- Flip flop is edge triggered and the latch is the level triggered or untriggered.
- A latch checks input continuously and changes the output whenever there is a change in input.
- But, the flip flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock.

Edge Triggering



Positive Edge Triggering

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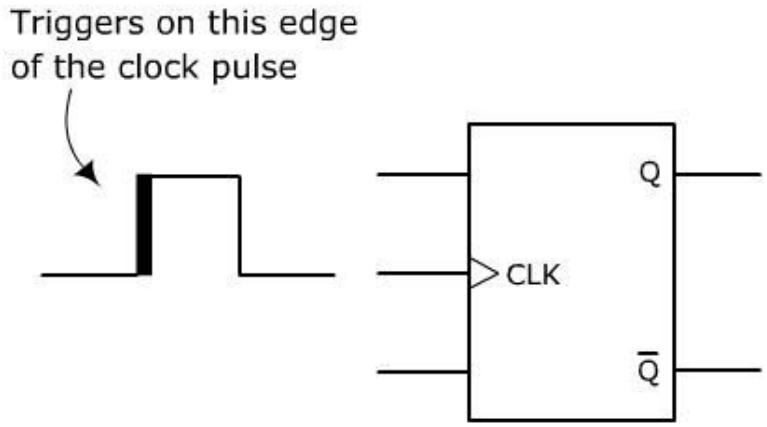

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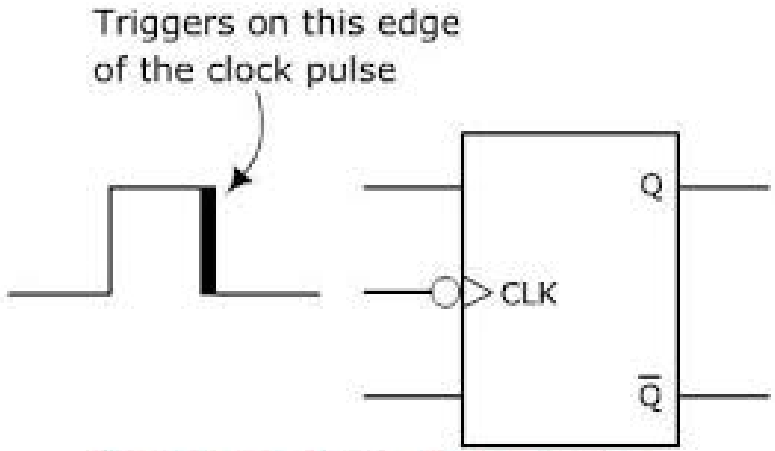
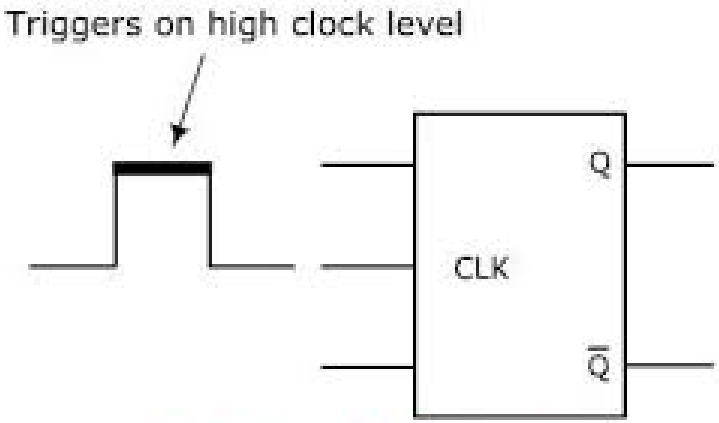


Negative Edge Triggering

Level Triggering



High Level Triggering

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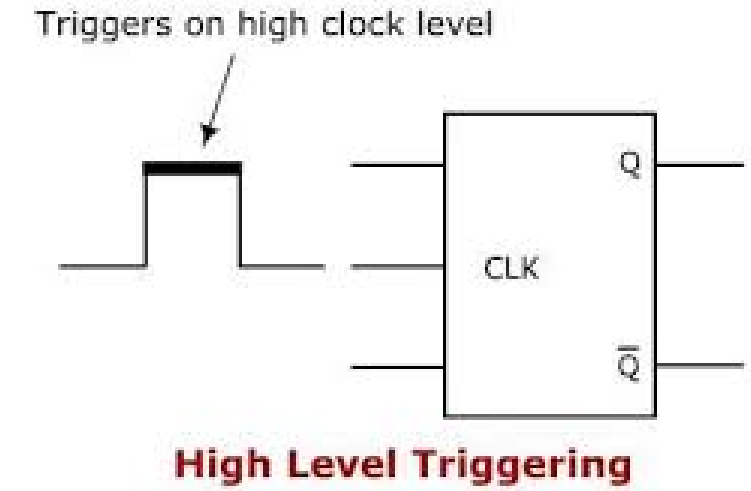

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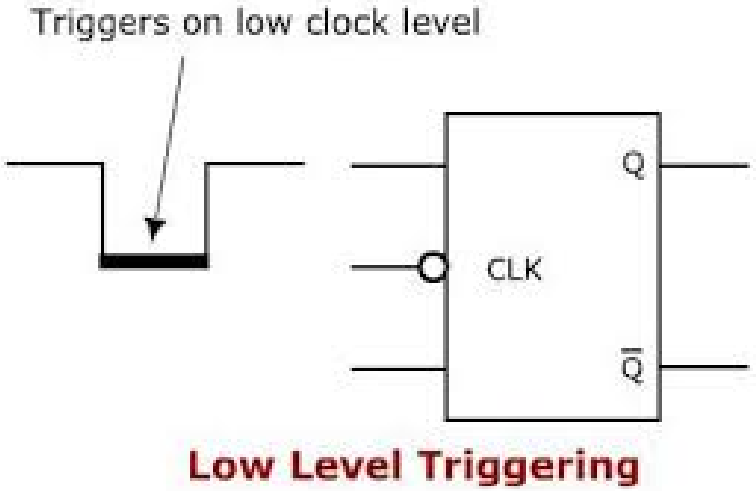

Low Level Triggering

Timing diagram of flip flop ($Q = D$)

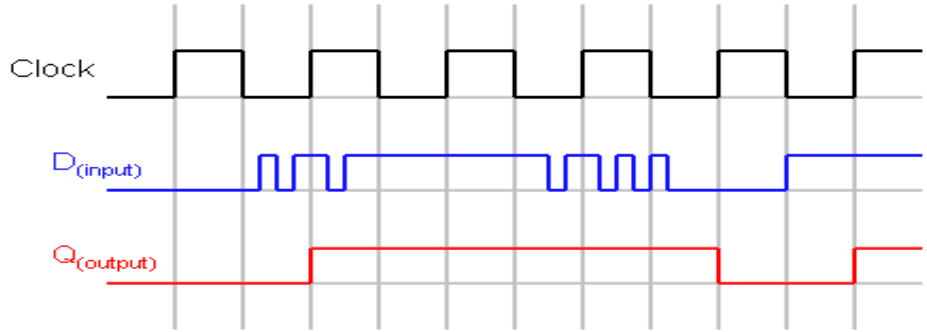

Figure: Timing diagram of Flip flop

- From the timing diagram it is clear that the output Q changes only at the positive edge of the clock.

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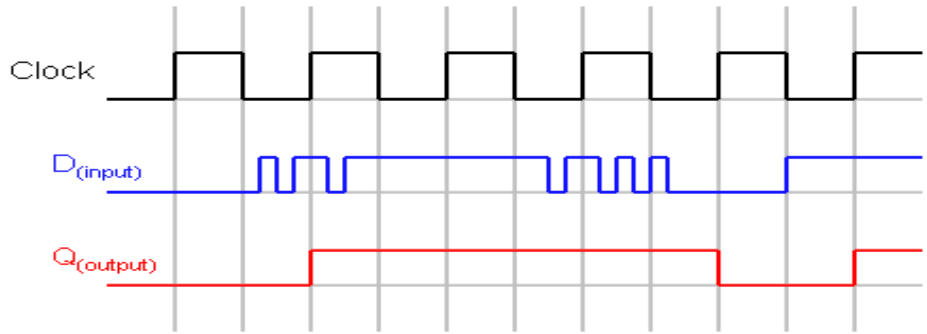

Figure: Timing diagram of Flip flop

- From the timing diagram it is clear that the output Q changes only at the positive edge of the clock.
- At each positive edge the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge

Timing diagram of Latch $(Q = D)$

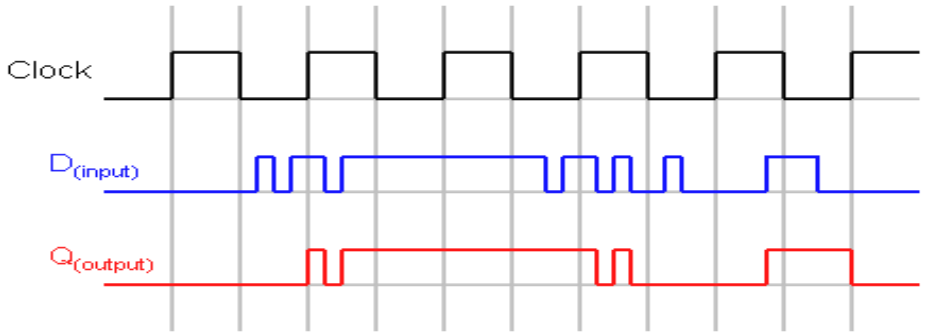

Figure: Timing diagram of Latch

- A latch checks input continuously and changes the output whenever there is a change in input (Untriggered latch) .

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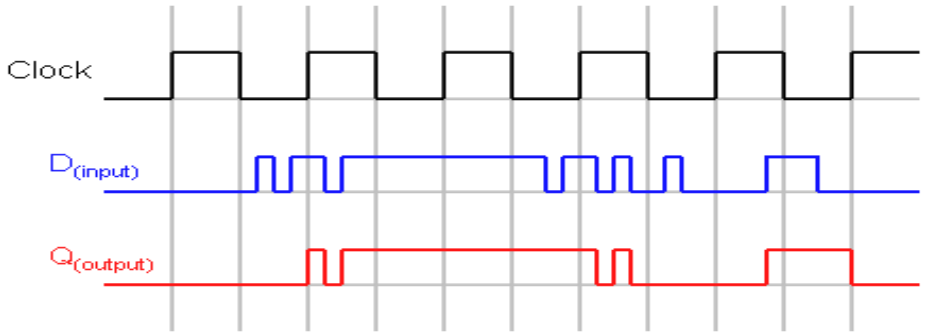

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- A latch checks input continuously and changes the output whenever there is a change in input (Untriggered latch) .
- From the timing diagram it is clear that the output Q changes at the positive level of the clock (Level triggered).

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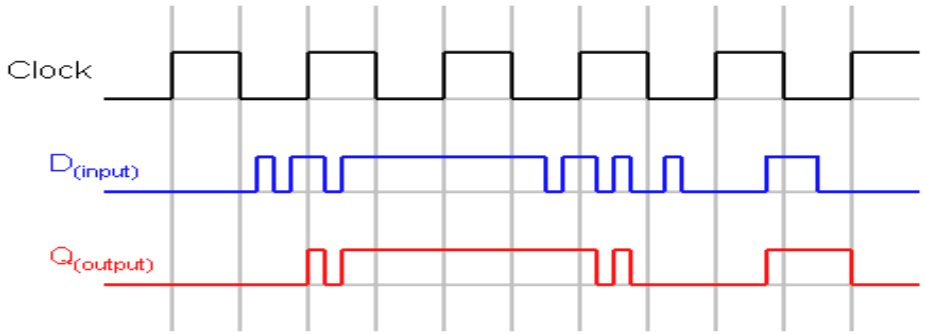

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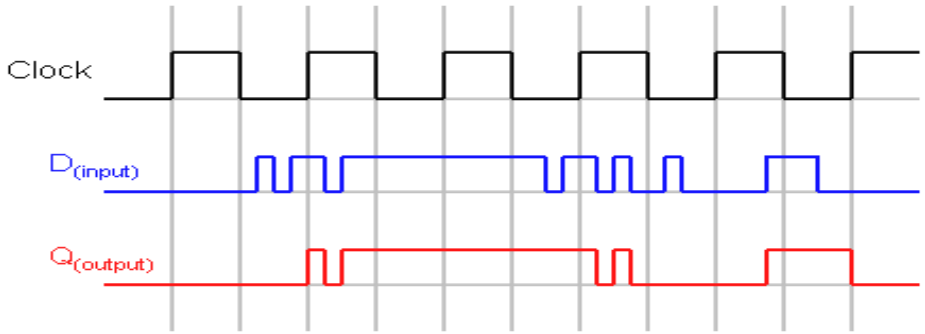

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- From the timing diagram it is clear that the output Q changes at the positive level of the clock (Level triggered).
- When clock is high, output Q will be equal to input D.
- When clock is low, the output Q will be the last value of the output till next positive clock.