Sequential Logic Circuit Design
Module III

Flip-Flop Conversion

The FF conversion is a process to design a new FF from the available FF.

Step-by-step procedure for FF conversion

[1] Identify available and required FFs.

[2] Make characteristic table for required FF.

[3] Make excitation table for available FF.

[4] Write boolean expression for available FF in terms of required FF.

[5] Draw the logic diagram.

SR FF to D FF Conversion

Step-1: Available FF : **SR**
Required FF : **D**

SR FF to D FF Conversion

Step-1: Available FF : **SR**
Required FF : **D**

Step-2-3: Characteristic (**D**) and excitation (**SR**) table

D	$\mathbf{Q_n}$	$\mathbf{Q_{n+1}}$	**S**	**R**
0	0	0	0	$\times$
0	1	0	0	1
1	0	1	1	0
1	1	1	$\times$	0

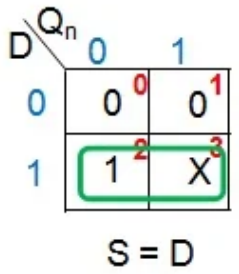
SR FF to D FF Conversion

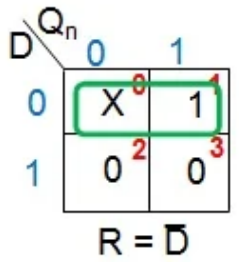
Step-1: Available FF : **SR**
Required FF : **D**

Step-2-3: Characteristic (**D**) and excitation (**SR**) table

D	Q_n	Q_{n+1}	S	R
0	0	0	0	×
0	1	0	0	1
1	0	1	1	0
1	1	1	×	0

Step-4: Boolean expression





SR FF to D FF Conversion

Step-1: Available FF : **SR**
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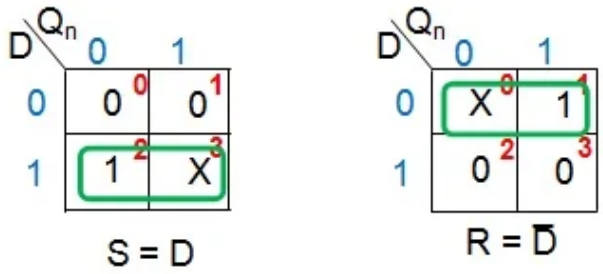
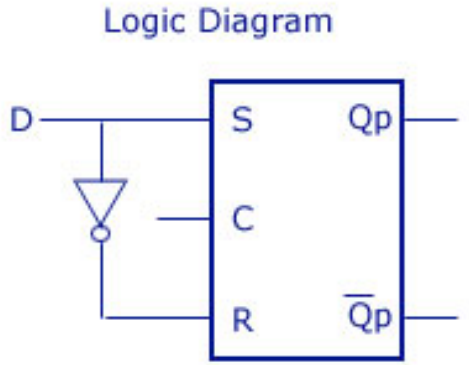
Step-2-3: Characteristic (**D**) and excitation (**SR**) table

D	$\mathbf{Q_n}$	$\mathbf{Q_{n+1}}$	**S**	**R**
0	0	0	0	×
0	1	0	0	1
1	0	1	1	0
1	1	1	×	0

Step-4: Boolean expression



Step-5: Circuit Diagram



SR FF to T FF Conversion

Step-1: Available FF : **SR** Required FF : **T**

SR FF to T FF Conversion

Step-1: Available FF : **SR** Required FF : **T**

Step-2-3: Characteristic (T) and excitation (SR) table

T	$\mathbf{Q_n}$	$\mathbf{Q_{n+1}}$	**S**	**R**
0	0	0	0	$\times$
0	1	1	$\times$	0
1	0	1	1	0
1	1	0	0	1

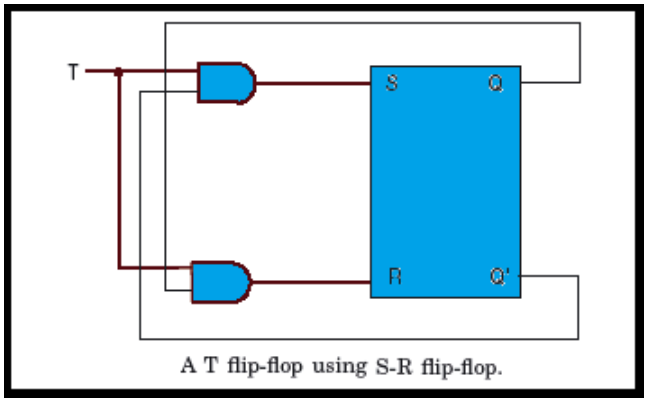
SR FF to T FF Conversion

Step-1: Available FF : **SR** Required FF : **T**

Step-2-3: Characteristic (T) and excitation (SR) table

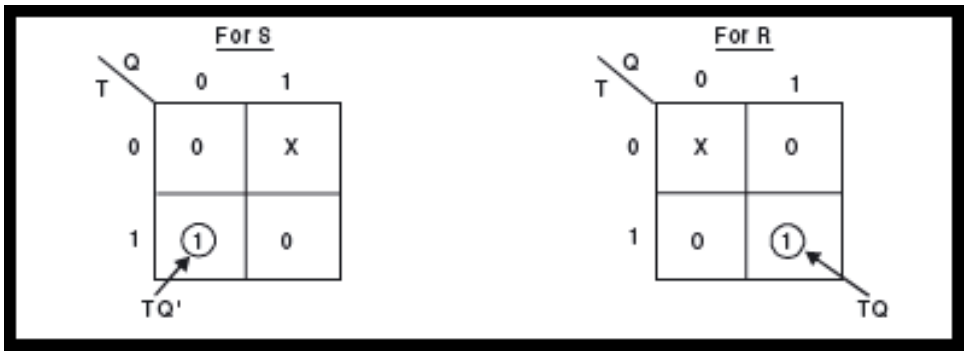
T	Q_n	Q_{n+1}	S	R
0	0	0	0	×
0	1	1	×	0
1	0	1	1	0
1	1	0	0	1

Step-5: Circuit Diagram



A T flip-flop using S-R flip-flop.

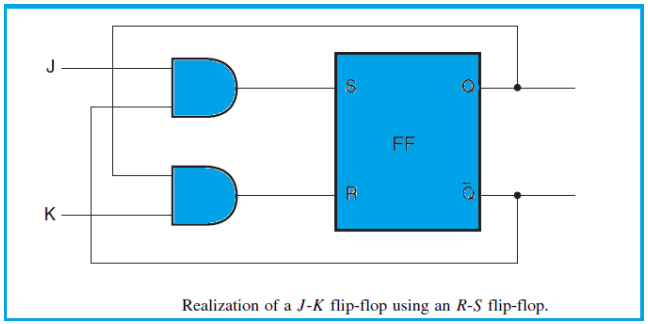
Step-4: Boolean expression



SR FF to JK FF

Step-1: Available FF : **SR**
Required FF : **JK**

Step-5: Circuit Diagram

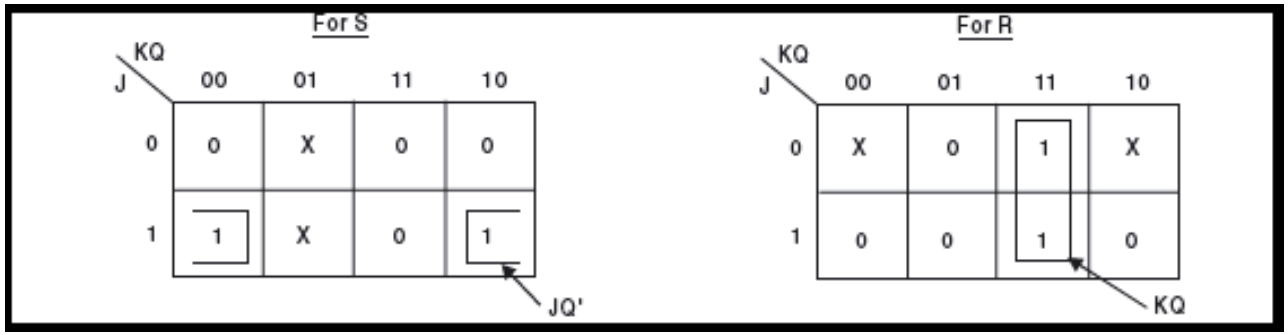


Realization of a *J-K* flip-flop using an *R-S* flip-flop.

Step-2-3: Characteristic and excitation table

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

Step-4: Boolean expression



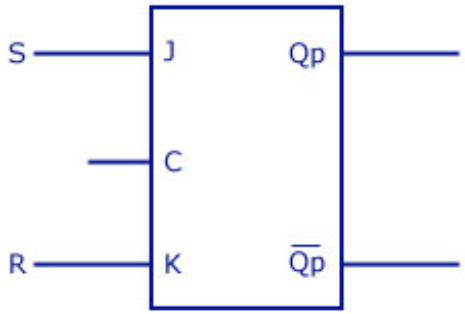
JK FF to SR FF Conversion

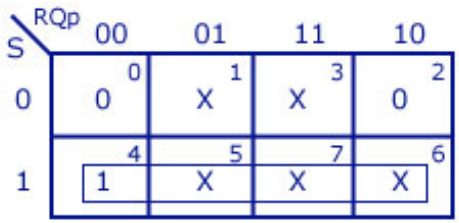
J-K Flip Flop to S-R Flip Flop

Conversion Table

S-R Inputs		Outputs		J-K Inputs	
S	R	Qp	Qp+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

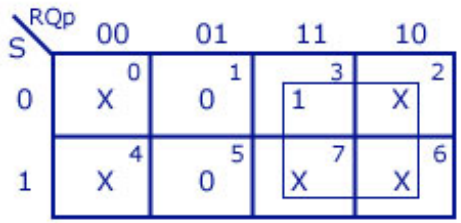
Logic Diagram





J=S

K-maps



K=R

Home Assignment on FF Conversion

- JK Flip Flop to D Flip Flop
- JK Flip Flop to T Flip Flop
- D Flip Flop to SR Flip Flop
- D Flip Flop to JK Flip Flop
- D Flip Flop to T Flip Flop
- T Flip Flop to SR Flip Flop
- T Flip Flop to JK Flip Flop
- T Flip Flop to D Flip Flop

Problem 1 on FF Conversion

A new clocked X-Y flip-flop is defined with two inputs, X and Y is in addition to the clock input. The flip flop functions as follows:

1. If XY = 00, the FF changes state with each clock pulse
2. If XY = 01, the FF state Q becomes '1' with the next clock pulse
3. If XY = 10, the FF state Q becomes '0' with the next clock pulse
4. If XY =11, the same state occurs with the clock pulse.

(a) Write the truth table for the XY FF.
(b) Write the excitation table for the XY FF.
(c) Convert JK FF into XY FF by adding some external gates.

Solution of problem 1

Table: (a) **Truth Table** for XY FF

X	**Y**	Q_{n+1}
0	0	Q'_n
0	1	1
1	0	0
1	1	Q_n

Table: (b) **Excitation Table** for XY Flip Flop

Q_n	Q_{n+1}	**J**	**K**
0	0	1	$\times$
0	1	0	$\times$
1	0	$\times$	0
1	1	$\times$	1

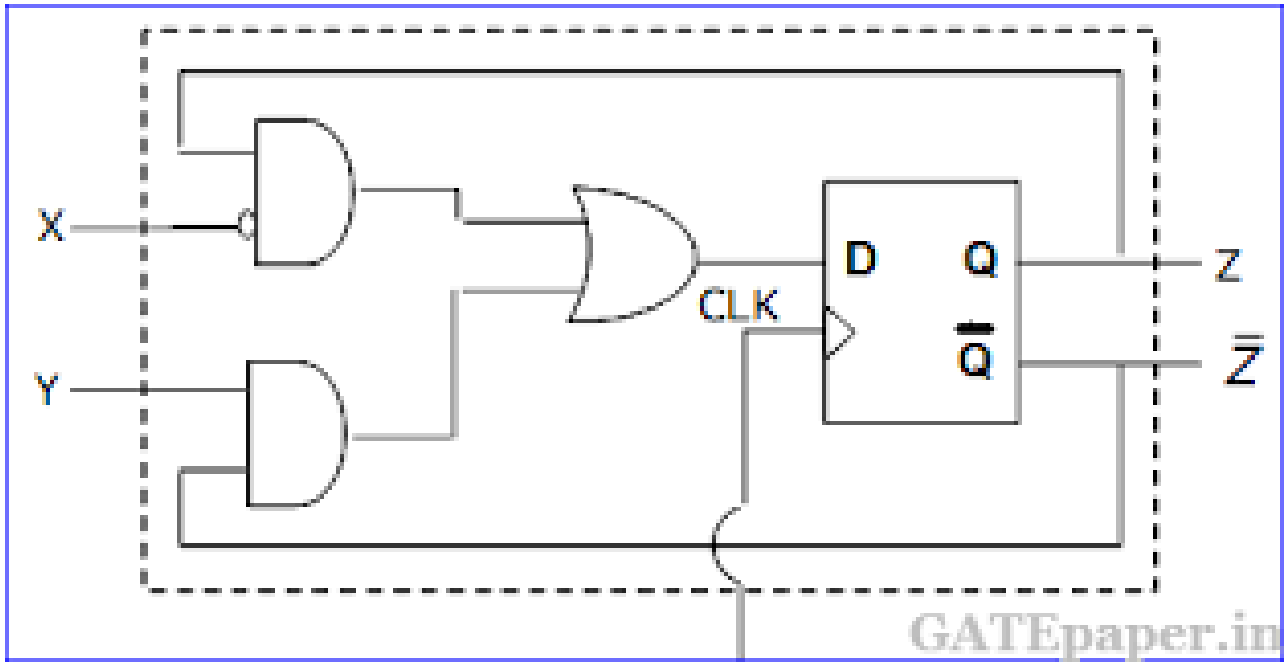
Table: **Characteristic Table** for XY Flip Flop

X	**Y**	Q_n	Q_{n+1}
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Now follow the same procedure that we did in the standard FF conversion

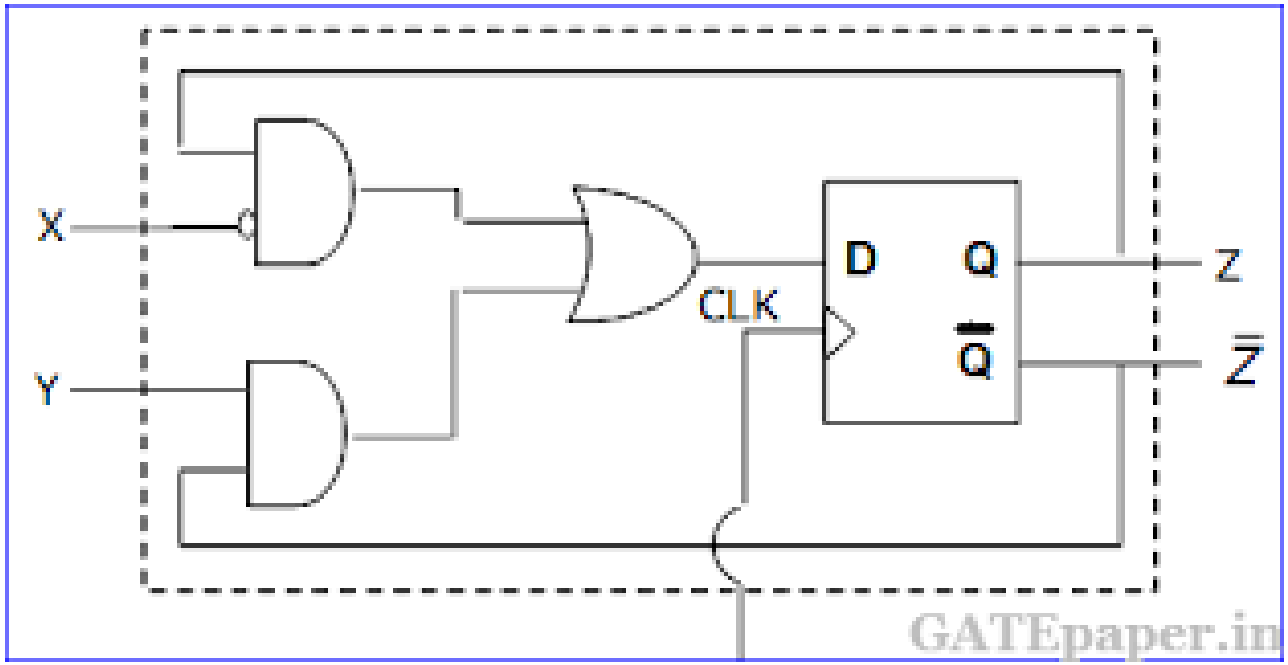
Problem 2 on FF Conversion

A sequential circuit using D FF and logic gates is shown in figure, where X and Y are the inputs and Z is output. The circuit is



Problem 2 on FF Conversion

A sequential circuit using D FF and logic gates is shown in figure, where X and Y are the inputs and Z is output. The circuit is



a. S-R FF with inputs X=R and Y =S
b. S-R FF with inputs X=S and Y=R
c. J-K FF with inputs X=J and Y=K
d. **J-K FF with inputs X=K and Y=J**

Solution of problem 2

From the Circuit: $D = X'Z + YZ'$
Output $Z = Q = D$
Inputs are X and Y

$\mathbf{X}$	$\mathbf{Y}$	$\mathbf{Q_n = Z}$	$\mathbf{Q_{n+1} = D}$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Solution of problem 2

From the Circuit: $D = X'Z + YZ'$
Output $Z = Q = D$
Inputs are X and Y

X	Y	$Q_n = Z$	$Q_{n+1} = D$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table: JK Flip Flop

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

The answer is [d] J-K FF with inputs X=K and Y=J