Sequential Logic Circuit Design
Module III

Question on Timing Diagram

Draw the timing diagram of output waveforms for given inputs and clock pulse using positive edge triggering.

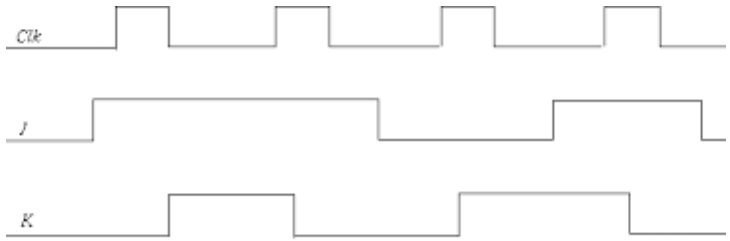


Figure: (1)

Question on Timing Diagram

Draw the timing diagram of output waveforms for given inputs and clock pulse using positive edge triggering.

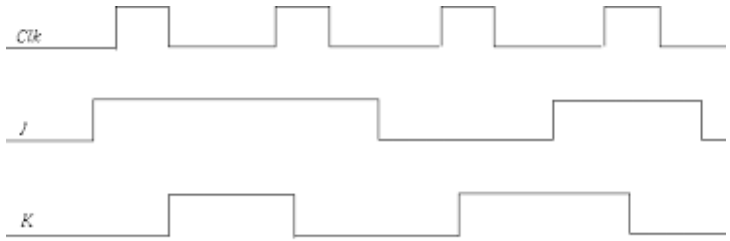


Figure: (1)

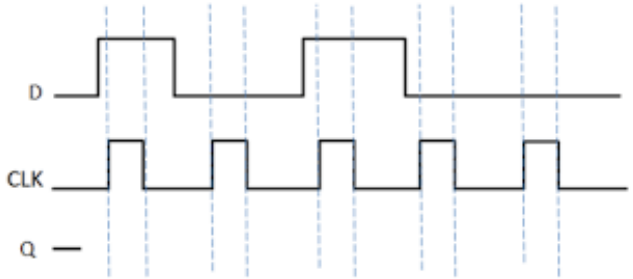
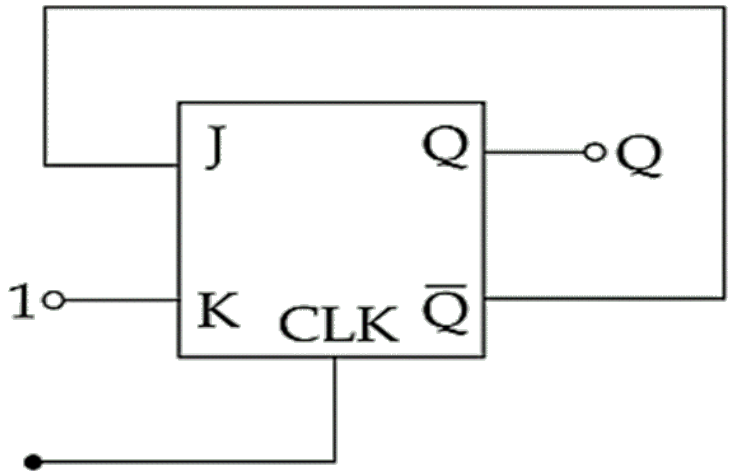


Figure: (2)

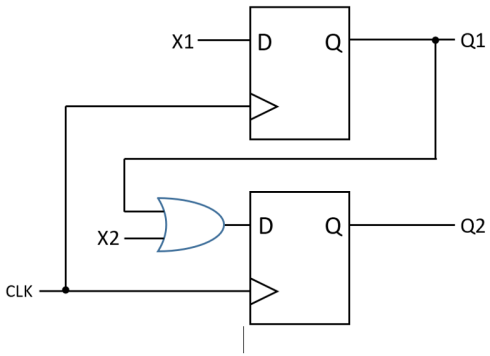
Question on JK Flip Flop

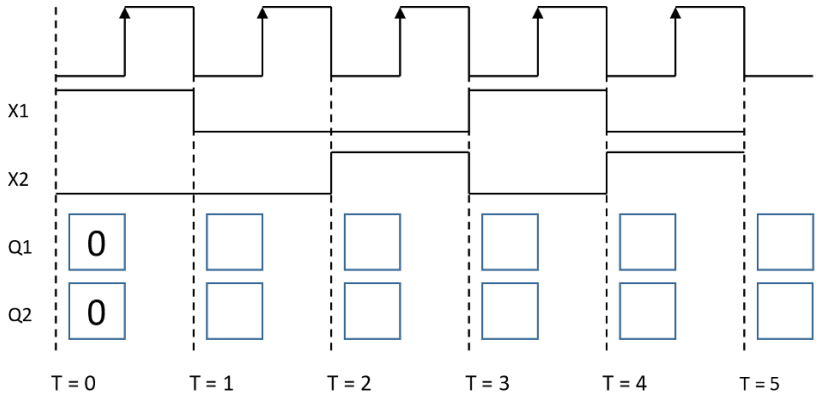
In a JK flip-fop, we have $J = \bar{Q}$ and K=1 shown in figure. Assuming the FF was initially cleared and clocked for 6 pulses, the sequence at the Q output will be:



Question on D Flip-Flop

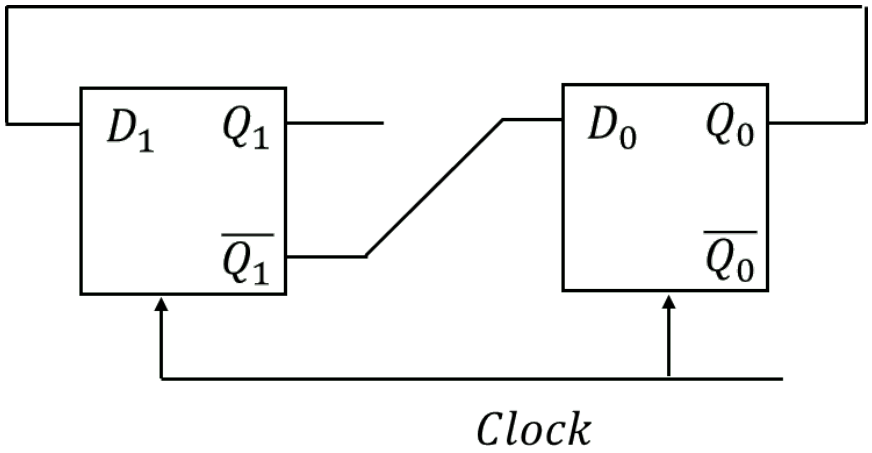
Analyze the circuit containing D flip-flops shown below by giving the value for $Q1$ and $Q2$ that result from each clock trigger. The flip-flops are positive-edge triggered so the question will ask about the values at the negative edges, by which time the flip-flop outputs should have settled. At time t $= 0$, $Q1 = 0$ and $Q2$ equal 0. Note that the flip-flops are commonly-clocked.





Question on D Flip Flop

The digital circuit shown below uses two positive edge triggered D flip-flops. Assuming initial condition of Q_1 and Q_0 as zero, the output sequence Q_1Q_0 of the circuit is



a 00,01,10,11,00...

b 00,01,11,11,00...

c **00,01,11,10,00...**

d 00,11,10,01,00....