



भारतीय सूचना प्रौद्योगिकी संस्थान, नागपुर
Indian Institute of Information Technology, Nagpur

Project Report

2-Stage Differential Op-Amp Simulation Using LTspice

CMOS Design- ECL 312

Submission Date: 25/04/2024

Submitted by:

1. ARYAN RANJAN BT21ECE048
2. HRITIK GUPTA BT21ECE049

Under the guidance of:
Dr.Paritosh D. Peshwe

Department of Electronics and Communication Engineering
IIIT NAGPUR

Table of Contents:

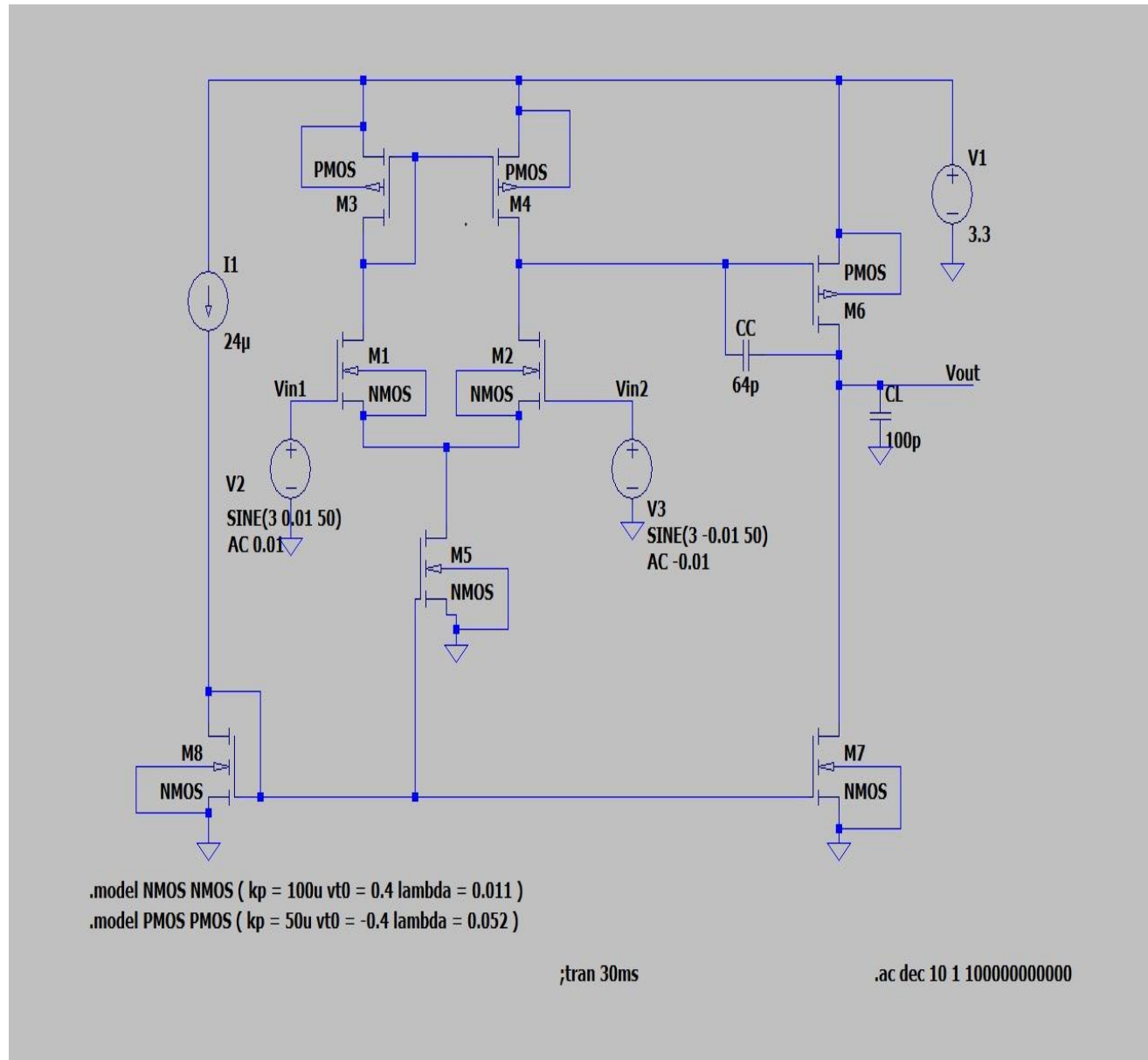
Chapter No.	Particular	Page No.
1	Introduction	2
2	Circuit Design	3
3	Simulation Results	4
4	Netlist	8
5	Conclusion	9

Chapter 1: Introduction

Operational amplifiers (Op-Amps) are widely used in various electronic circuits due to their versatility and efficiency. Differential amplifiers, a specific type of Op-Amp configuration, are particularly useful in applications where the difference between two input voltages needs to be amplified while rejecting common-mode signals.

In this project, we aim to simulate the behavior of a differential Op-Amp circuit using LTspice, a powerful simulation tool commonly employed for electronic circuit design and analysis. Through simulation, we will investigate the performance characteristics of the differential Op-Amp and validate its functionality.

Chapter 2: Circuit Design

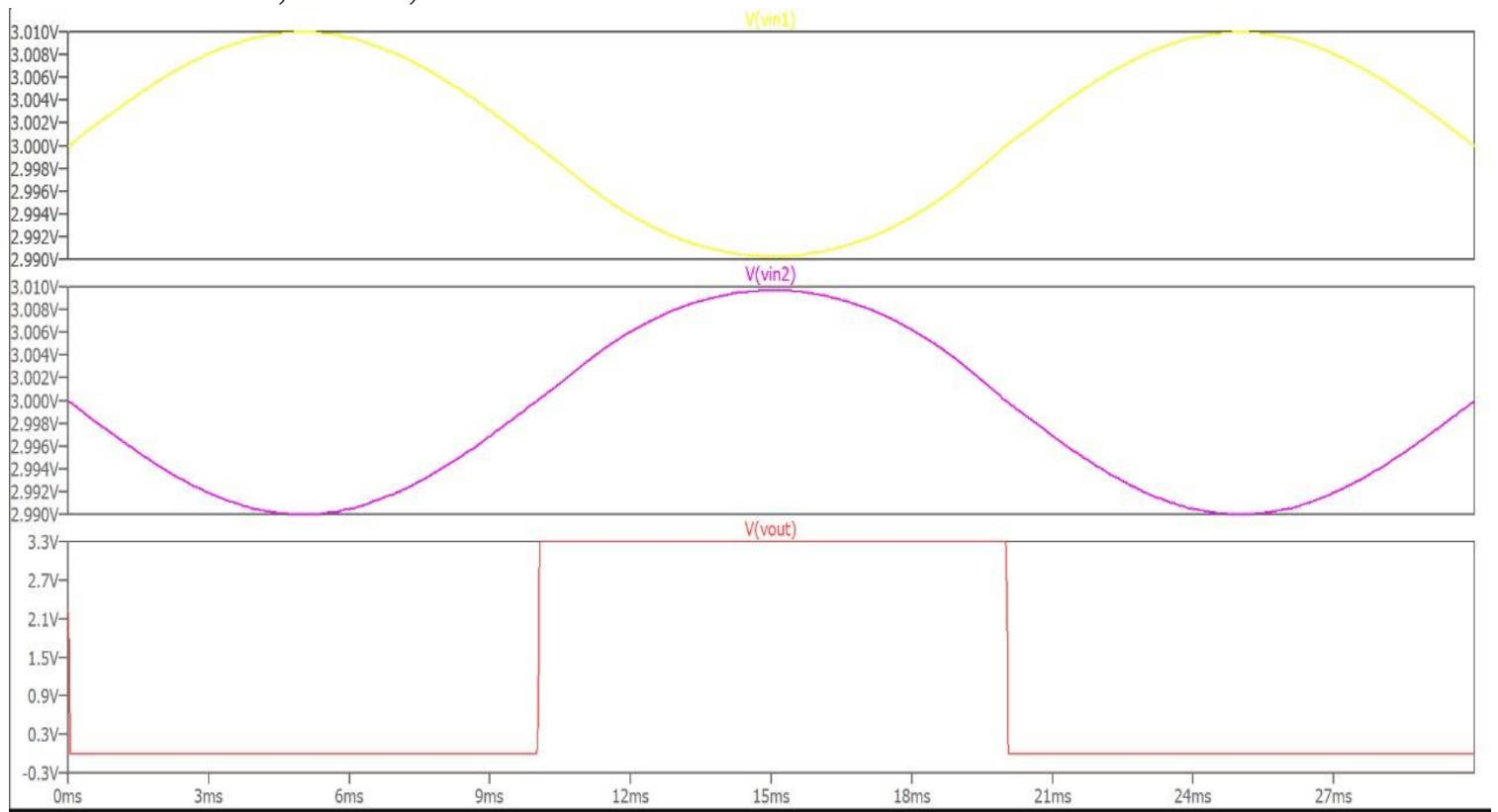


2 Stage OP Amps with specifications :

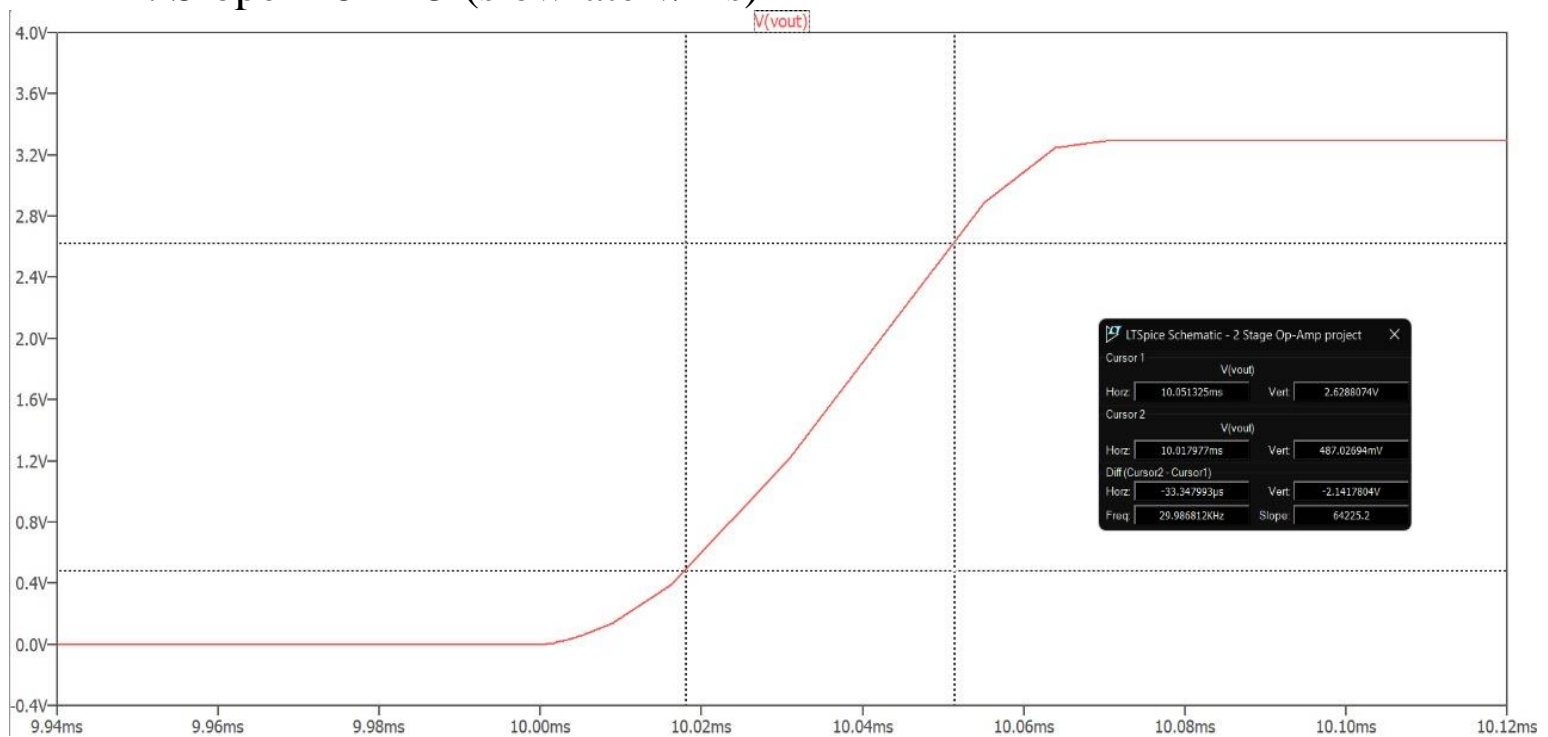
- Open loop gain = 115dB
- Bandwidth = 66.21 MHz
- Power Voltage Supply (Vdd) = 3.3 V
- Slope (V/ms) = 64225
- Power = 8 Mw

Chapter 3: Simulation Results

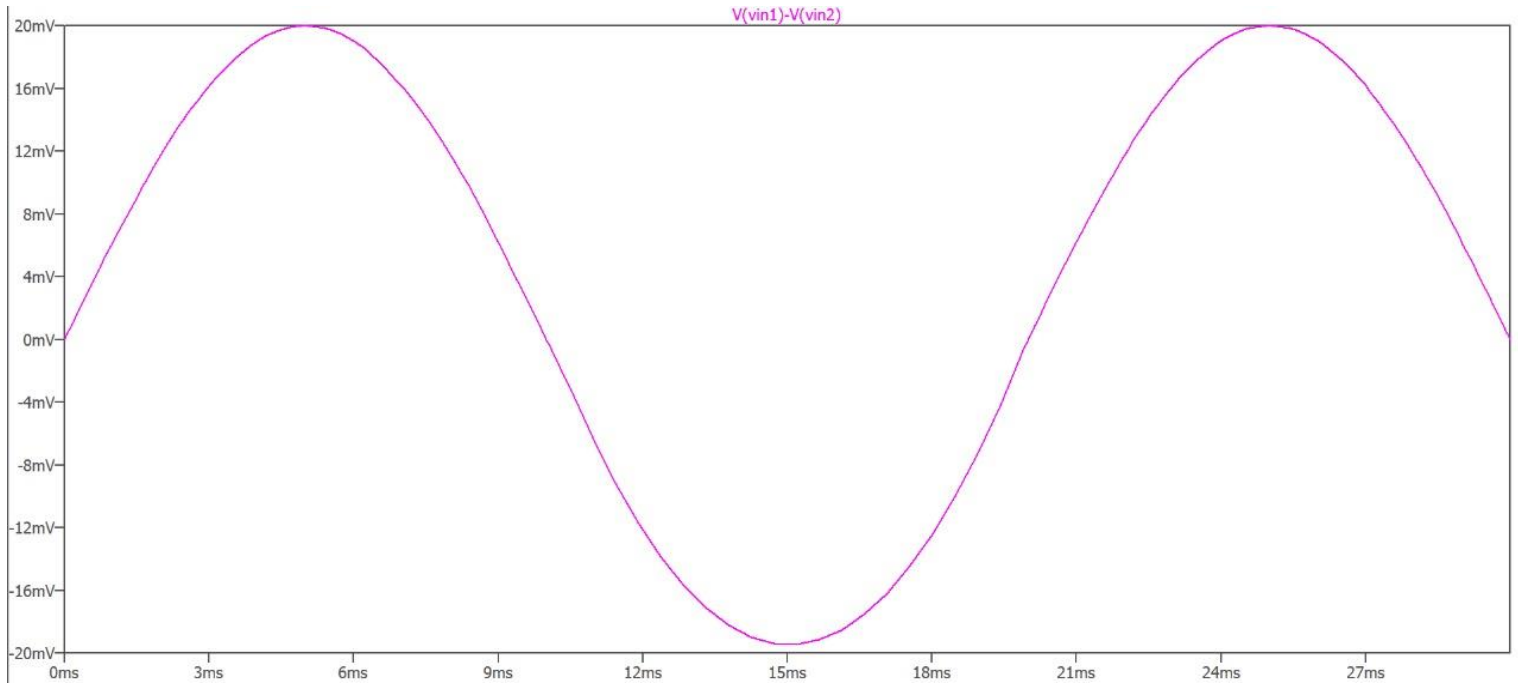
1. Vin1 , Vin2 , Vout



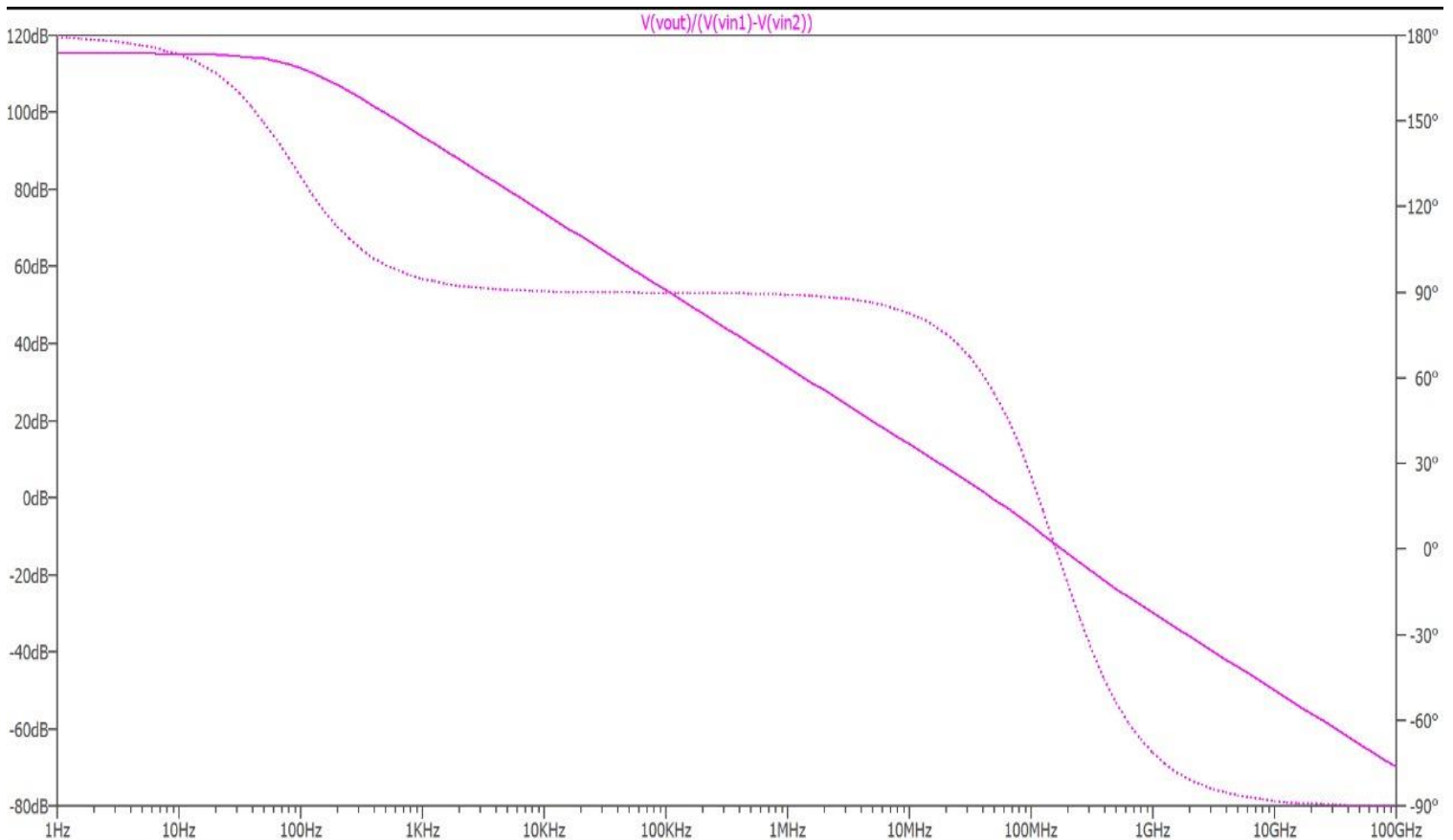
2. Slope = 64225 (slewrate v/ms)



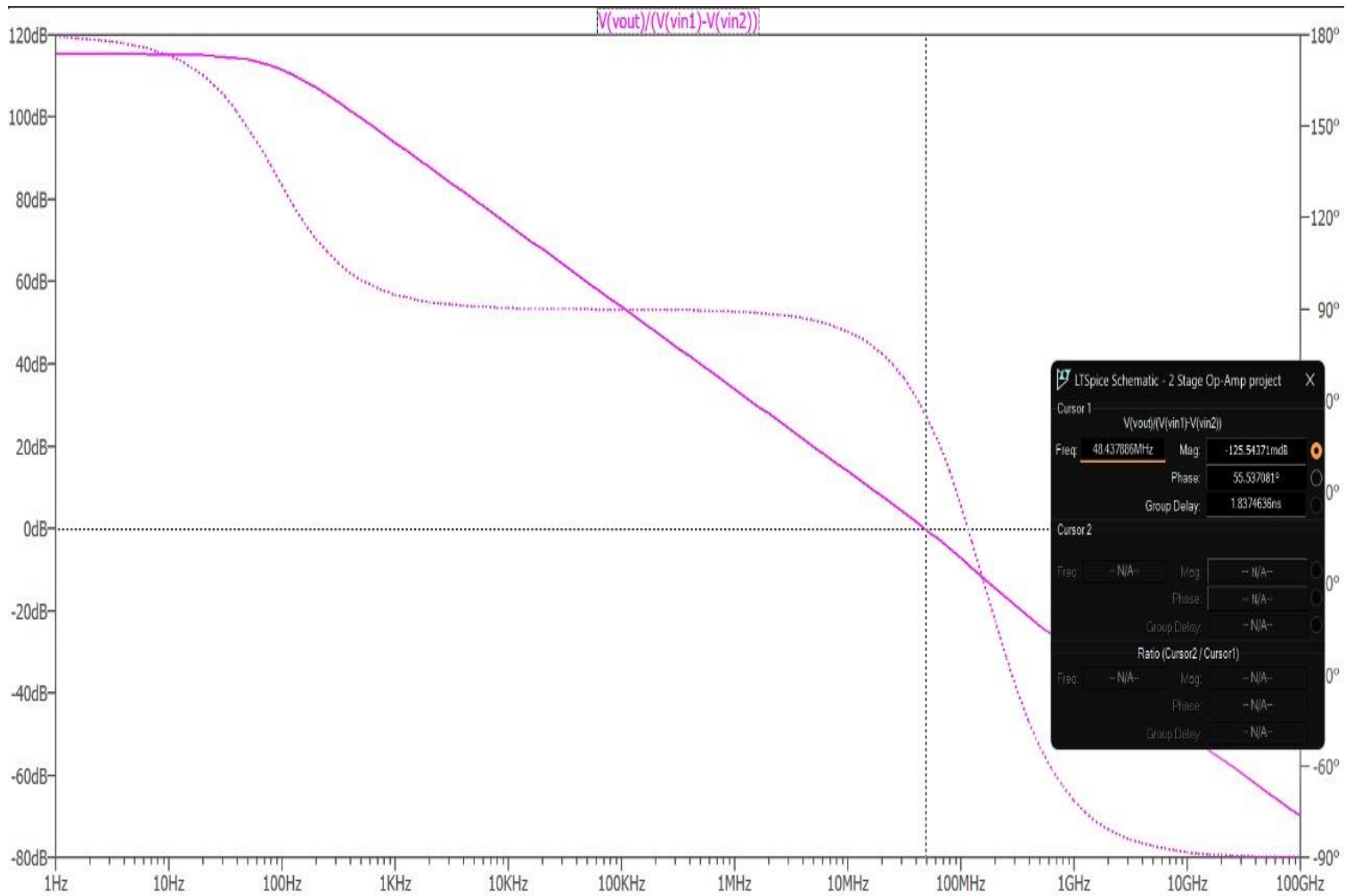
3. Vin1-Vin2



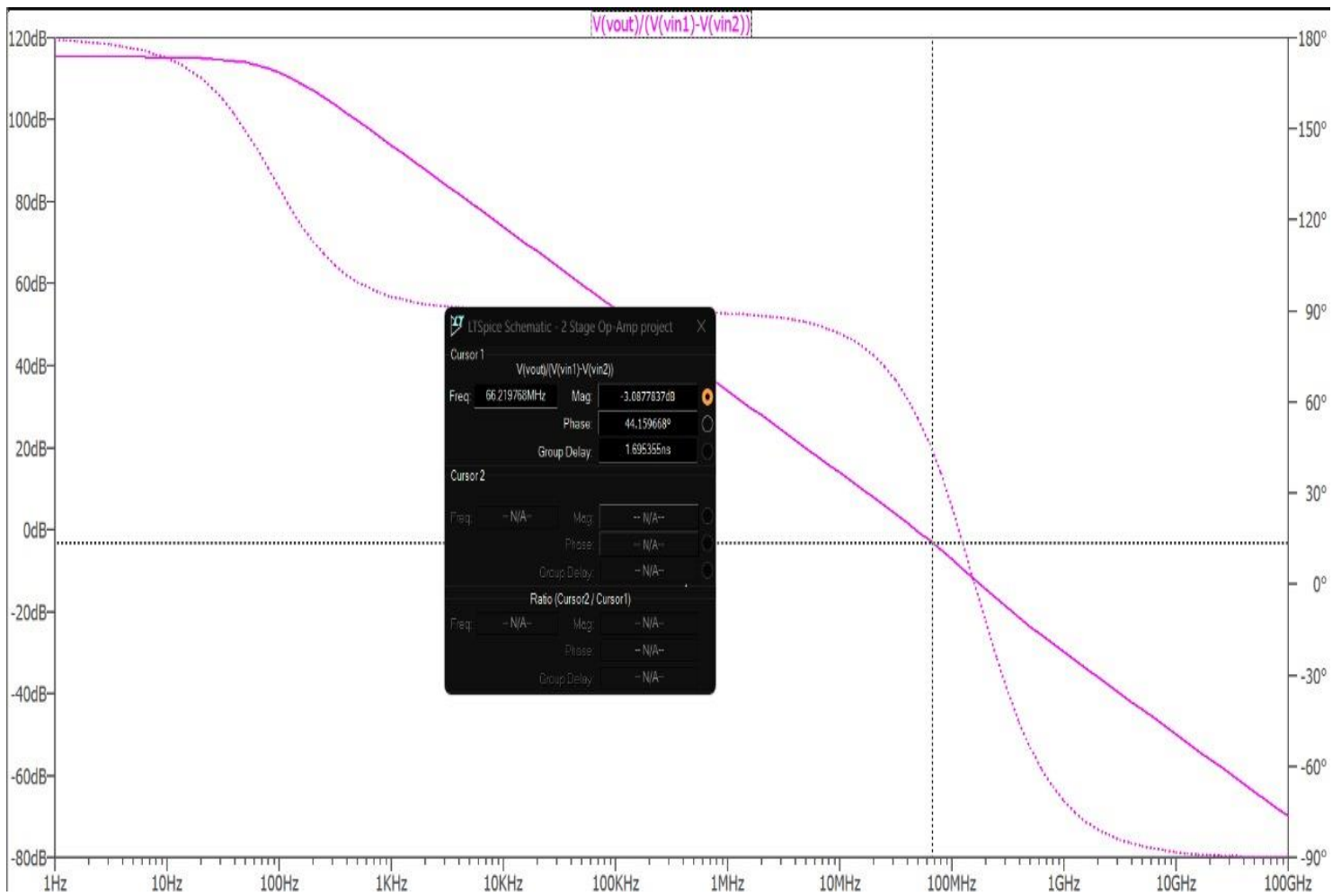
4. Vout / Vin (Gain)



5. Phase Margin : 55.53 deg & Freq : 48.43 MHZ at 0dB



6. Freq(B.W) : 66.21 MHz at -3dB



Chapter 4: Netlist

```
/* 2 Stage Op-Amp project.asc */
```

```
M1 N002 Vin1 N004 N004 NMOS l=1620n w=16m
```

```
M5 N004 N005 0 0 NMOS l=1620n w=2200n
```

```
M8 N005 N005 0 0 NMOS l=2430n w=198n
```

```
I1 N001 N005 24μ
```

```
M3 N002 N002 N001 N001 PMOS l=520n w=1662u
```

```
M4 N003 N002 N001 N001 PMOS l=520n w=1662u
```

```
V1 N001 0 3.3
```

```
V2 Vin1 0 SINE(3 0.01 50) AC 0.01
```

```
M2 N003 Vin2 N004 N004 NMOS l=1620n w=16m
```

```
V3 Vin2 0 SINE(3 -0.01 50) AC -0.01
```

```
M6 Vout N003 N001 N001 PMOS l=520n w=16m
```

```
M7 Vout N005 0 0 NMOS l=1620n w=11u
```

```
CL Vout 0 100p
```

```
CC Vout N003 64p
```

```
.model NMOS NMOS
```

```
.model PMOS PMOS
```

```
.lib C:\Users\Dell\AppData\Local\LTspice\lib\cmp\standard.mos
```

```
.model NMOS NMOS ( kp = 100u vt0 = 0.4 lambda = 0.011 )
```

```
.model PMOS PMOS ( kp = 50u vt0 = -0.4 lambda = 0.052 )
```

```
;ac dec 10 1 100000000000
```

```
.tran 30ms
```

```
.backanno
```

```
.end
```

Chapter 4: Conclusion

- The simulation of the differential Op-Amp circuit using LTspice has provided valuable insights into its behavior and performance.
- Through transient and Ac analyses, we have observed the circuit's response to differential input signals, determined its biasing conditions, and evaluated its frequency response characteristics.
- Key parameters such as gain, bandwidth, and linearity have been analyzed, demonstrating the circuit's suitability for various applications requiring precision signal amplification.
- Overall, this project has enhanced our understanding of differential Op-Amp circuits and their simulation using LTspice, contributing to the advancement of electronic circuit design and analysis methodologies.