

INVERTER DESIGN & LAYOUT

EECT / CE 6325 – VLSI DESIGN

Instructor

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Submitted by

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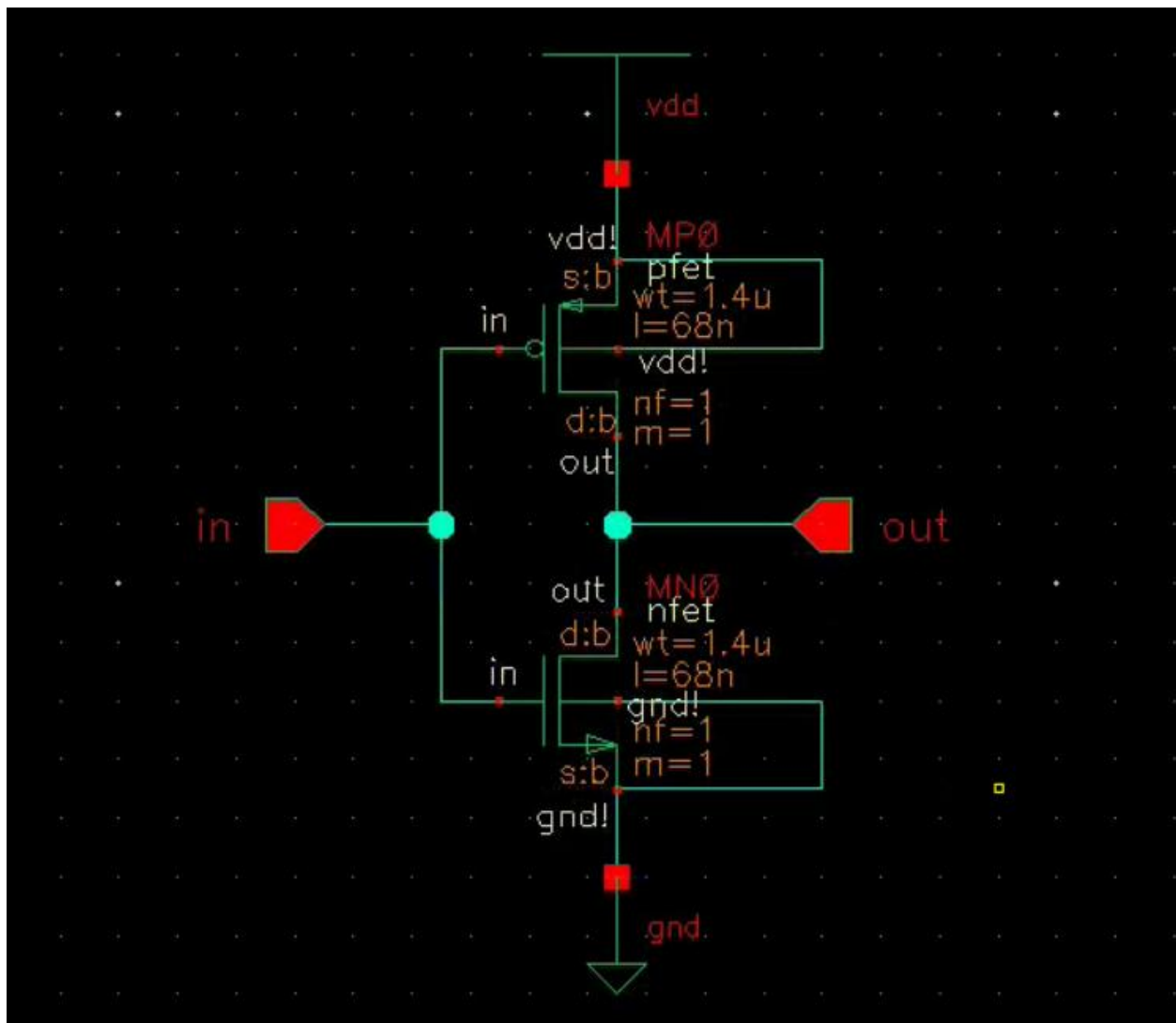
Date: 10/15/2025

Introduction:

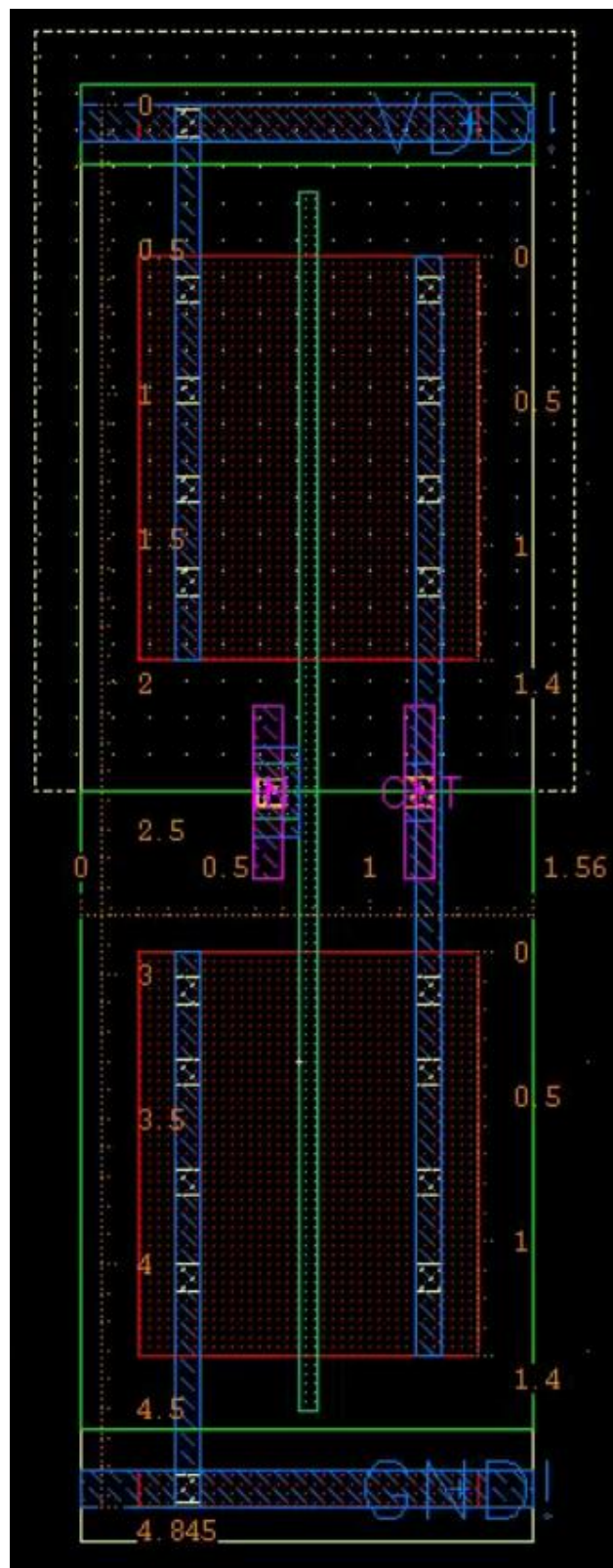
We have designed the inverter layout with $W_P = 1.4 \mu\text{m}$, $W_n = 1.4 \mu\text{m}$ and $C_{\text{load}} = 28 \text{ fF}$.
Summary of the design is:

Rise Delay (t _{LH})	79.9ps
Fall Delay (t _{HL})	44.5ps
Output Rise Edge Rate	90.6ps
Output Fall Edge Rate	40.3ps
Area	7.5582 μm^2

Schematic of the Inverter:



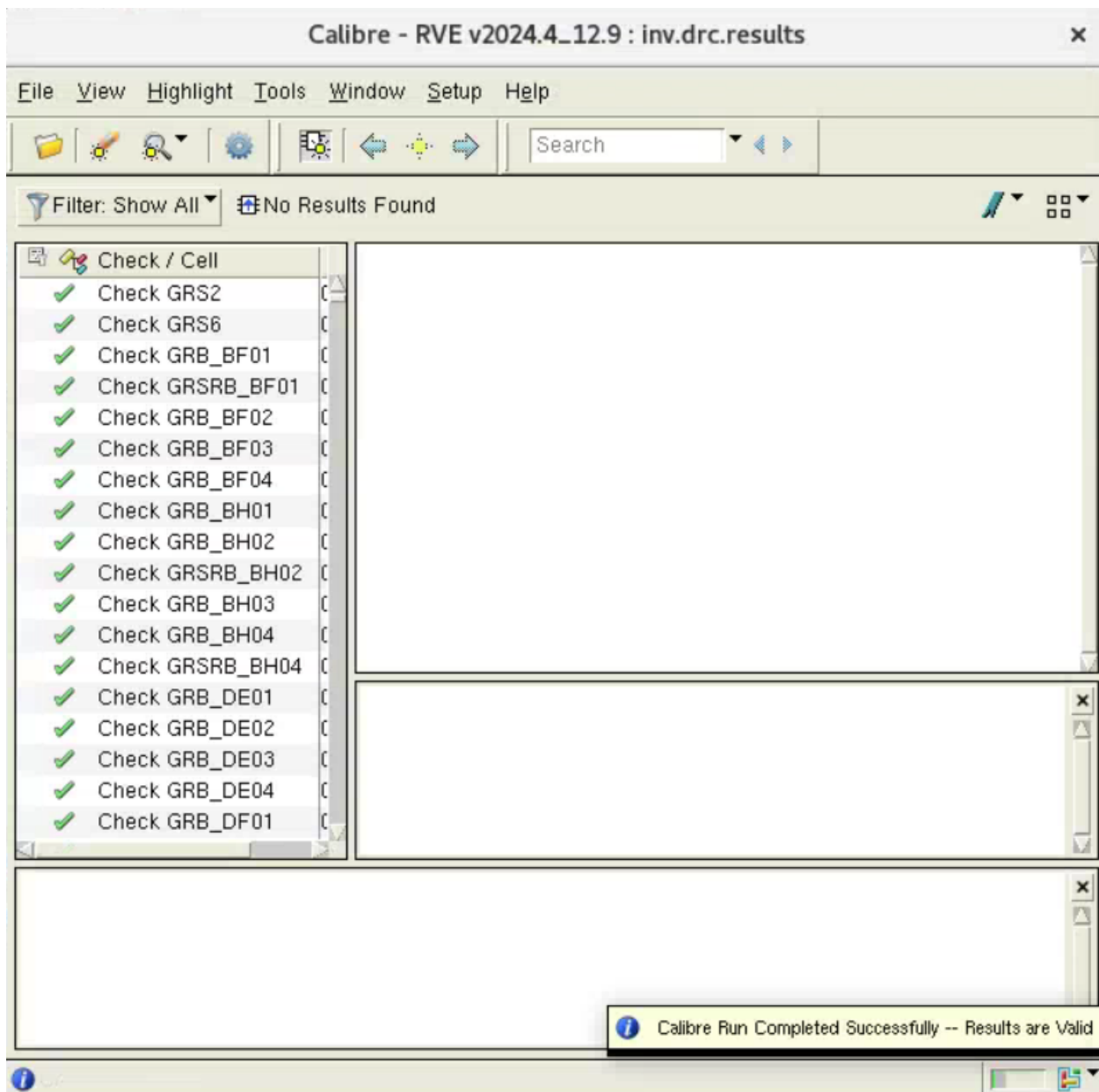
Layout of the inverter:



From the layout, we can see that the width of the pmos is 1.4 μm , the width of the nmos is 1.4 μm and the length of the transistor is 68 nm.

The area of the inverter is $= (1.56 * 4.845) \mu\text{m}^2 = 7.5582 \mu\text{m}^2$. The pin pitch is 0.52 μm . The offset on the left side is 0.65 μm and on the right side is 0.39 μm .

DRC Check:



Extracted Spice Netlist:

* File: inv.pex.sp

* Created: Tue Oct 14 22:42:20 2025

* Program "Calibre xRC"

* Version "v2024.4_12.9"

*

.include "inv.pex.sp.pex"

.subckt inv GND! OUT VDD! IN

*

* IN IN

* VDD! VDD!

* OUT OUT

* GND! GND!

XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=4.90308e-12

+ PERIM=8.988e-06

XMMN0 N_OUT_MMN0_d N_IN_MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6.8e-08

+ W=1.4e-06 AD=7.714e-13 AS=7.714e-13 PD=3.902e-06 PS=3.902e-06 NRD=0.272857

+ NRS=0.272857 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.51e-07

+ SB=5.51e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=3.604e-15

+ PANW7=1.36e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=3.7196e-14

XMMP0 N_OUT_MMP0_d N_IN_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6.8e-08

+ W=1.4e-06 AD=7.714e-13 AS=7.714e-13 PD=3.902e-06 PS=3.902e-06 NRD=0.272857

+ NRS=0.272857 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5.51e-07

+ SB=5.51e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=3.196e-15 PANW6=6.8e-15

+ PANW7=1.5232e-14 PANW8=2.176e-13 PANW9=5.44e-14 PANW10=7.1604e-14

*

.include "inv.pex.sp.INV.pxi"

*

.ends

*

*

Spice Test Setup File:

\$example HSPICE setup file

\$transistor model

.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "inv.pex.sp"

.option post runlv1=5

xi GND! OUT VDD! IN inv

vdd VDD! GND! 1.2v

vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.0585ns 0v 6ns 0v 6.0585ns 1.2v 12ns 1.2v)

cout OUT GND! 28f

\$transient analysis

.tr 100ps 12ns

\$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp

\$.tr 100ps 12ns sweep WP 1.4u 9u 0.5u

.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 \$measure tih at
0.6v

.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 \$measure tpi at
0.6v

.measure tavg param = '(trise+tfall)/2' \$calculate average delay

.measure tdiff param='abs(trise-tfall)' \$calculate delay difference

.measure delay param='max(trise,tfall)' \$calculate worst case delay

\$ method 1

.measure tran iavg avg i(vdd) from=0 to=10n \$average current in one clock cycle

.measure energy param='1.2*iavg*10n' \$calculate energy in one clock cycle

.measure edp1 param='abs(delay*energy)'

\$ method 2

.measure tran t1 when v(IN)=1.19 fall=1

.measure tran t2 when v(OUT)=1.19 rise=1

.measure tran t3 when v(IN)=0.01 rise=1

.measure tran t4 when v(OUT)=0.01 fall=1

.measure tran i1 avg i(vdd) from=t1 to=t2 \$average current when output rise

.measure tran i2 avg i(vdd) from=t3 to=t4 \$average current when output fall

```
.measure energy1 param='1.2*i1*(t2-t1)' $calculate energy when output rise
```

```
.measure energy2 param='1.2*i2*(t4-t3)' $calculate energy when output fall
```

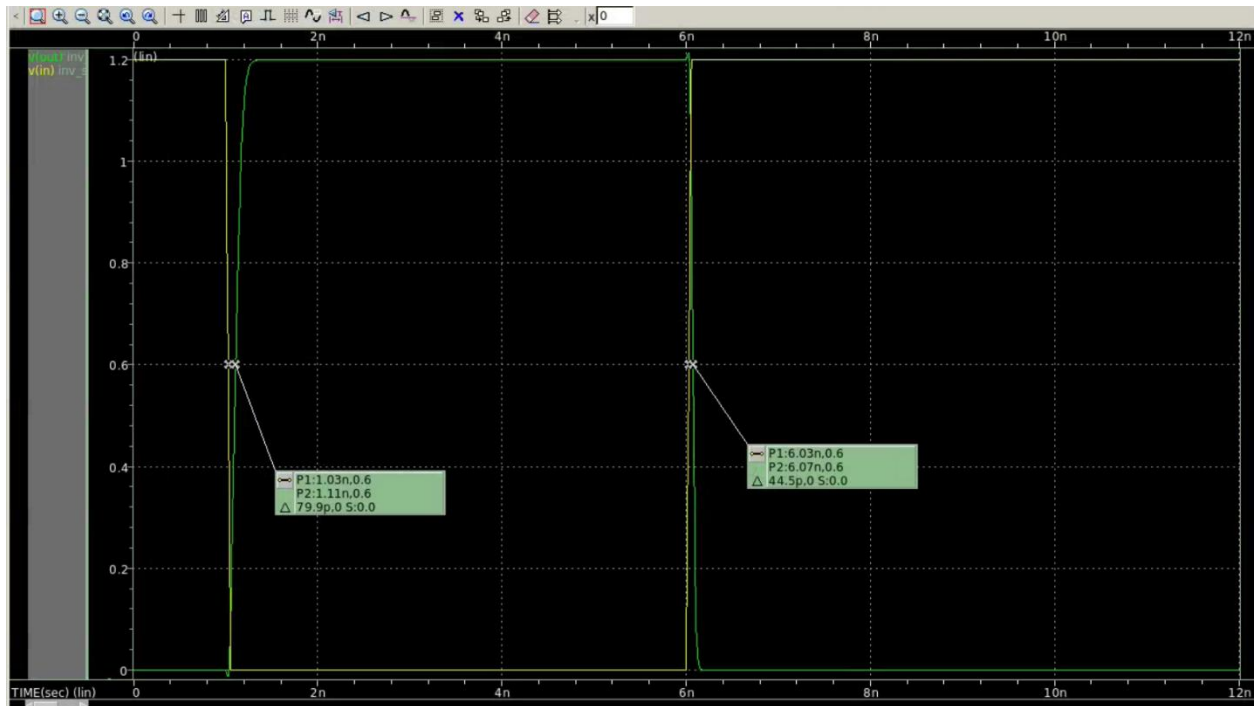
```
.measure energysum param='energy1+energy2'
```

```
.measure edp2 param='abs(delay*energysum)'
```

```
.end
```

Waveform –

Rise & Fall Delay-



Output rise & fall edge-

