



Erik Jonsson School of Engineering
and Computer Science

PROJECT 4 – CELL LIBRARY

EECT / CE 6325 – VLSI DESIGN FALL 2025

Instructor

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9. Layout of All Cells	

OBJECTIVE

The objective of this project is to design a cell library. We have designed a schematic, a layout, generated waveforms and an abstract view for each of the cells below in this project using Cadence Virtuoso and HSpice tools.

The cells are

1. INVERTER
2. NAND2
3. NOR2
4. XOR2
5. AOI22
6. OAI22
7. OAI21
8. NAND3

All the cells were designed and optimized with the minimum possible height with reference to the INVERTER cell which has a maximum cell height of 5.660um. The height of all the other cells was scaled up to 5.660um to maintain uniform cell height when placed next to each other. All the other measurements between different layers were also brought to the least minimum possible as per the design rules mentioned in the technology file to ultimately reduce the total cell area.

The minimum pin-pitch and offset obtained are 0.52um and 0.39um respectively. There were no errors when DRC, LVS and PEX were run for individual cells. Also, when all the cells were placed next to each other, the DRC check passed successfully without any errors. As mentioned in the project requirements, all the inputs of all the cells are maintained with a slew rate of 35ps, 45 fF load capacitance and the same has been depicted for both rising and falling edges in the HSpice waveform simulations.

INVERTER

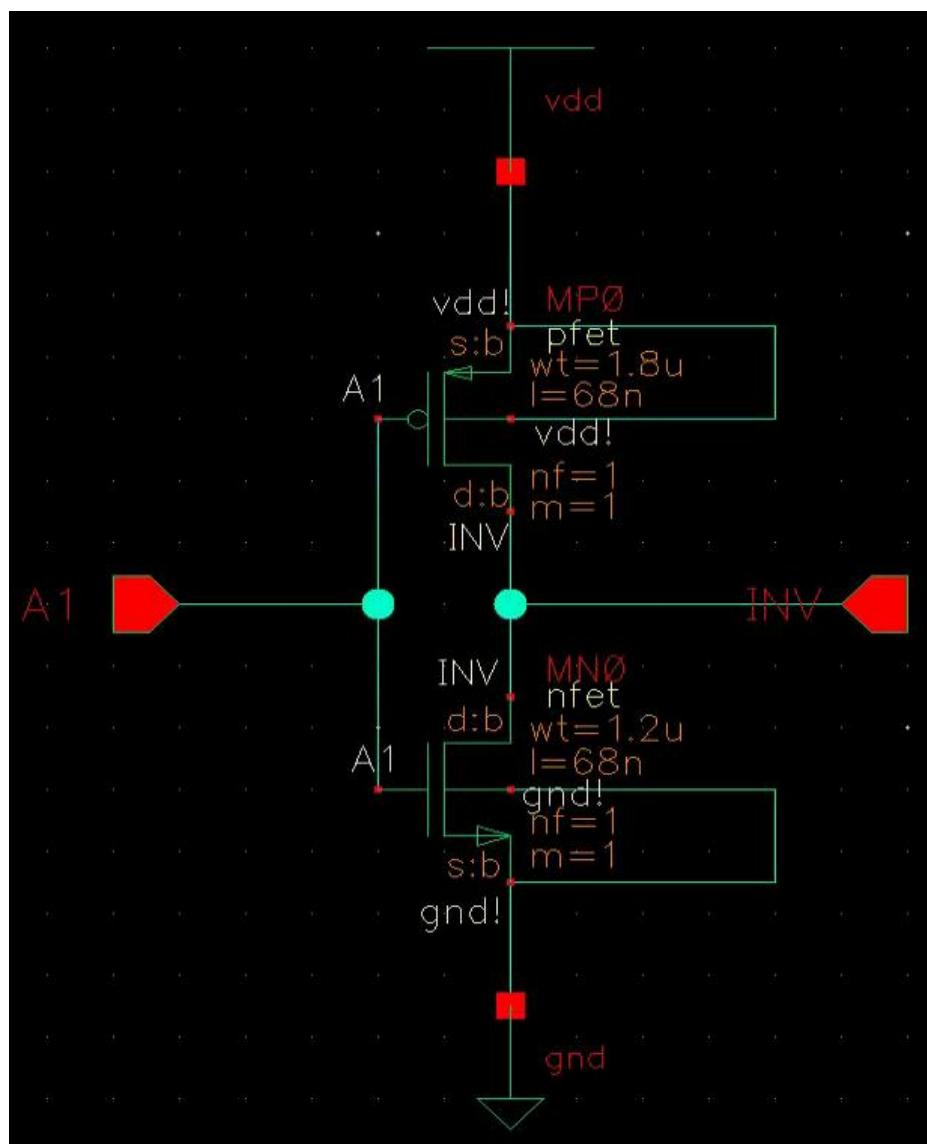
Function

$$\text{OUT} = \text{NOT } (\text{A})$$

Truth Table

INPUT (A1)	OUTPUT (INV)
1	0
0	1

Schematic

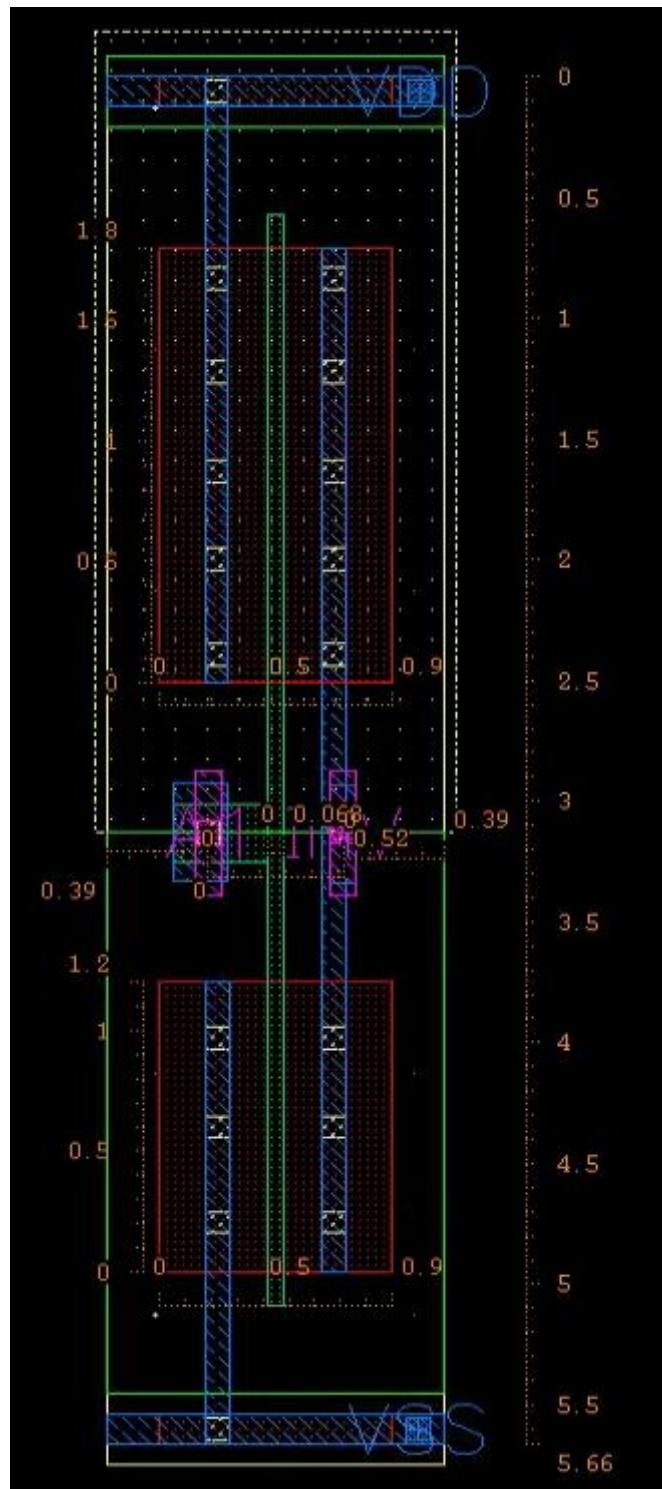


Layout

Cell Height = 5.660 μm

Cell Width = 0.900 μm

Total Cell Area = 5.094 μm^2



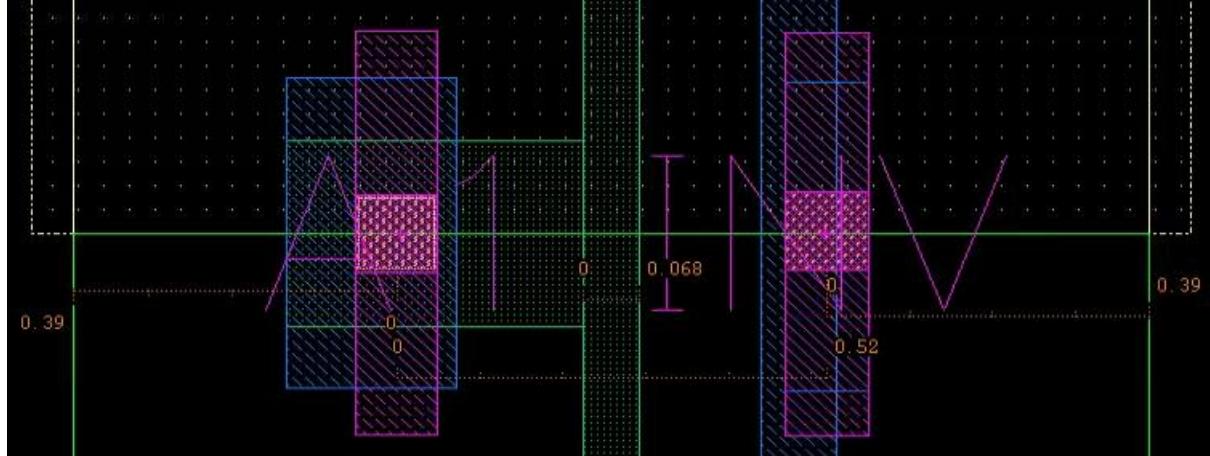
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

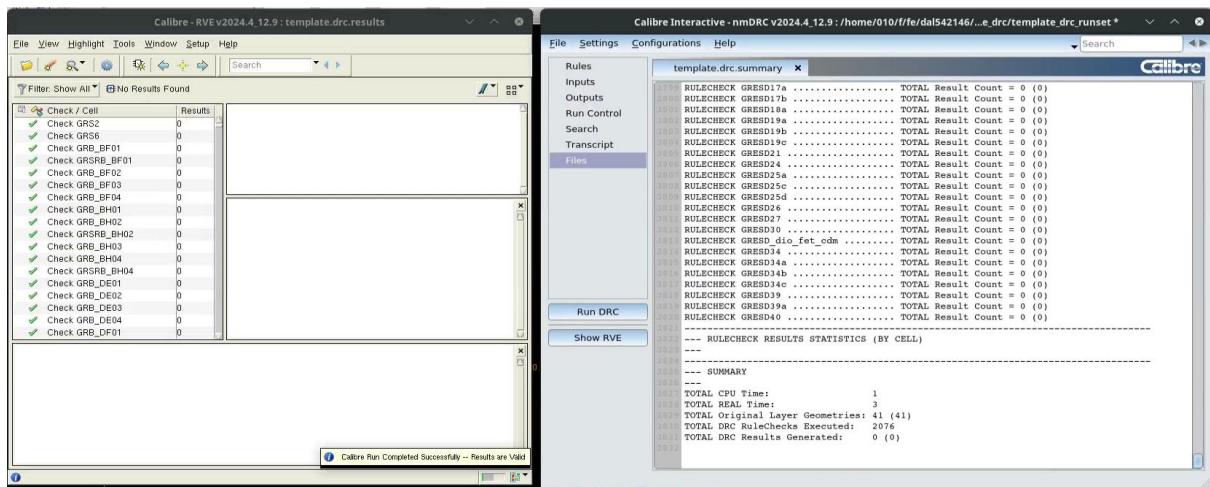
Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

Offset (right side) = 0.39 um



DRC Result



LVS Result

Calibre - RVE v2024.4.12.9 : svdb template

Calibre Interactive - nmLVS v2024.4_12.9 : /home/010/f/fe/dal542146/c...te_lvs/template_lvs.runset *

template.lvs.report

REPORT FILE NAME: template.lvs.report
 SOURCE NAME: template.scp.net ('template')
 SOURCE FILE: _Calibre_LVS.rules
 CURRENT TIME: Tue Nov 4 20:49:53 2025
 CURRENT DIRECTORY: /home/010/f/fe/dal542146/od/gf65/tmc65_stdcell_lib/template/
 template_lvs
 UBER NAME: dal542146
 CALIBRE VERSION: v2024.4_12.9 Tue Oct 1 20:34:12 PDT 2024

OVERALL COMPARISON RESULTS

PEX Result

Calibre Interactive - PEX v2024.4_12.9 : /home/010/f/fe/dal542146/...e_lvs/template_pex_runset *

template_pex_runset

total nets = 4
 top-level nets = 4
 non-top-level nets = 0
 degenerate nets = 0
 merged nets = 0
 error nets = 0

=====

CALIBRE xRC WARNING / ERROR Summary

xRC Warnings = 1
 xRC Errors = 0

=====

--- CALIBRE xRC::FORMATTER COMPLETED - Tue Nov 4 20:49:53 2025
 --- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 50/54/638 MALLOC = 380/380/689 ELAPSED

*** xRC run finished with exit code 0 ***

54901

0 Errors, 4 Warnings, 1 Info

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51464	Warning	Please increase descriptors limit for best performance (8192)
53553	Warning	Please increase descriptors limit for best performance (8192)
54861	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

PEX Generated Netlist

```
* File: template.pex.sp
* Created: Wed Nov 5 20:35:44 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "template.pex.sp.pex"
.subckt template GND! INV VDD! A1
*
* A1     A1
* VDD    VDD
* INV    INV
* VSS    VSS
XD0_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=4.648e-12
+ PERIM=9.44e-06
XMMN0_N_INV_MMN0_d N_A1_MMN0_g N_GND! MMN0_s N_GND! D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=4.992e-13 AS=4.992e-13 PD=3.232e-06 PS=3.232e-06 NRD=0.16
+ NRS=0.160833 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=4.16e-07
+ SB=4.16e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMP0_N_INV_MMP0_d N_A1_MMP0_g N_VDD! MMP0_s N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=7.488e-13 AS=7.488e-13 PD=4.432e-06 PS=4.432e-06 NRD=0.106667
+ NRS=0.108333 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=4.16e-07
+ SB=4.16e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=2.5704e-13 PANW8=2.04e-14 PANW9=5.44e-14 PANW10=8.16e-14
*
.include "template.pex.sp.TEMPLATE.pxi"
*
.ends
*
*
```

HSpice Setup File

```
$example HSPICE setup file

$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "template.pex.sp"

.option post runlvl=5
xi VSS OUT VDD IN template
vdd VDD VSS 1.2v

$ Input waveform with 35 ps 10-90% slew
$ (equivalent 0-100% = 35ps / 0.8 = 43.75 ps)
vin IN VSS PWL(0ns 0v 1ns 0v 1.04375ns 1.2v 6ns 1.2v 6.04375ns 0v 12ns 0v)

COUT OUT VSS| 45f

$transient analysis
.tr 100ps 12ns

$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
*.tr 100ps 12ns sweep WP 1u 9u 0.5u

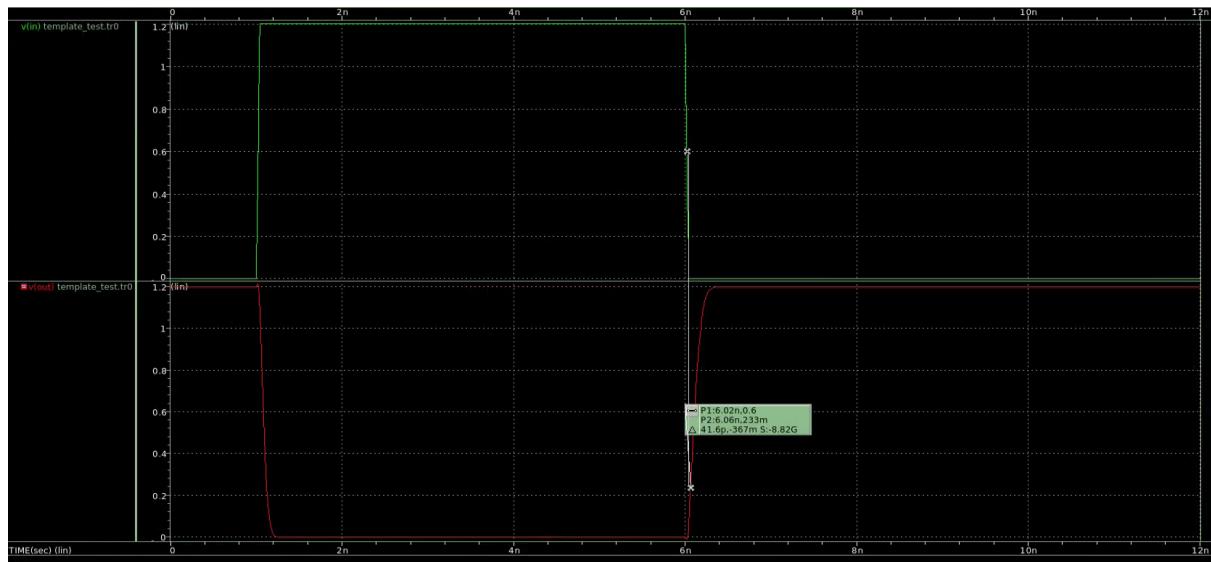
.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure tlh at
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure tpl at
.measure tavg param='(trise+tfall)/2' $calculate average delay
.measure tdiff param='abs(trise-tfall)' $calculate delay difference
.measure delay param='max(trise,tfall)' $calculate worst case delay

.measure tran iavg avg i(vdd) from=0ns to=1ns $average current in one clock cycle
.measure energy param='1.2*iavg*1ns' $calculate energy in one clock cycle
.measure edp param='abs(delay*energy)'

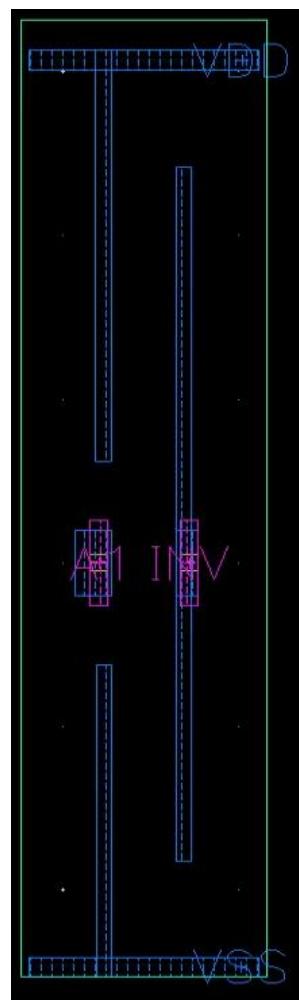
.measure tran t1 when v(IN)=1.19 fall=1
.measure tran t2 when v(OUT)=1.19 rise=1
.measure tran t3 when v(IN)=0.01 rise=1
.measure tran t4 when v(OUT)=0.01 fall=1
.measure tran ia avg i(vdd) from=t1 to=t2 $average current when output rise
.measure tran ib avg i(vdd) from=t3 to=t4 $average current when output fall
.measure energyl param='1.2*ia*(t2-t1)' $calculate energy when output rise
.measure energy2 param='1.2*ib*(t4-t3)' $calculate energy when output fall
.measure energysum param='energyl+energy2'
.measure edp2 param='abs(delay*energysum)'

.end
```

HSpice Simulation Waveform



Abstract View



NAND 2

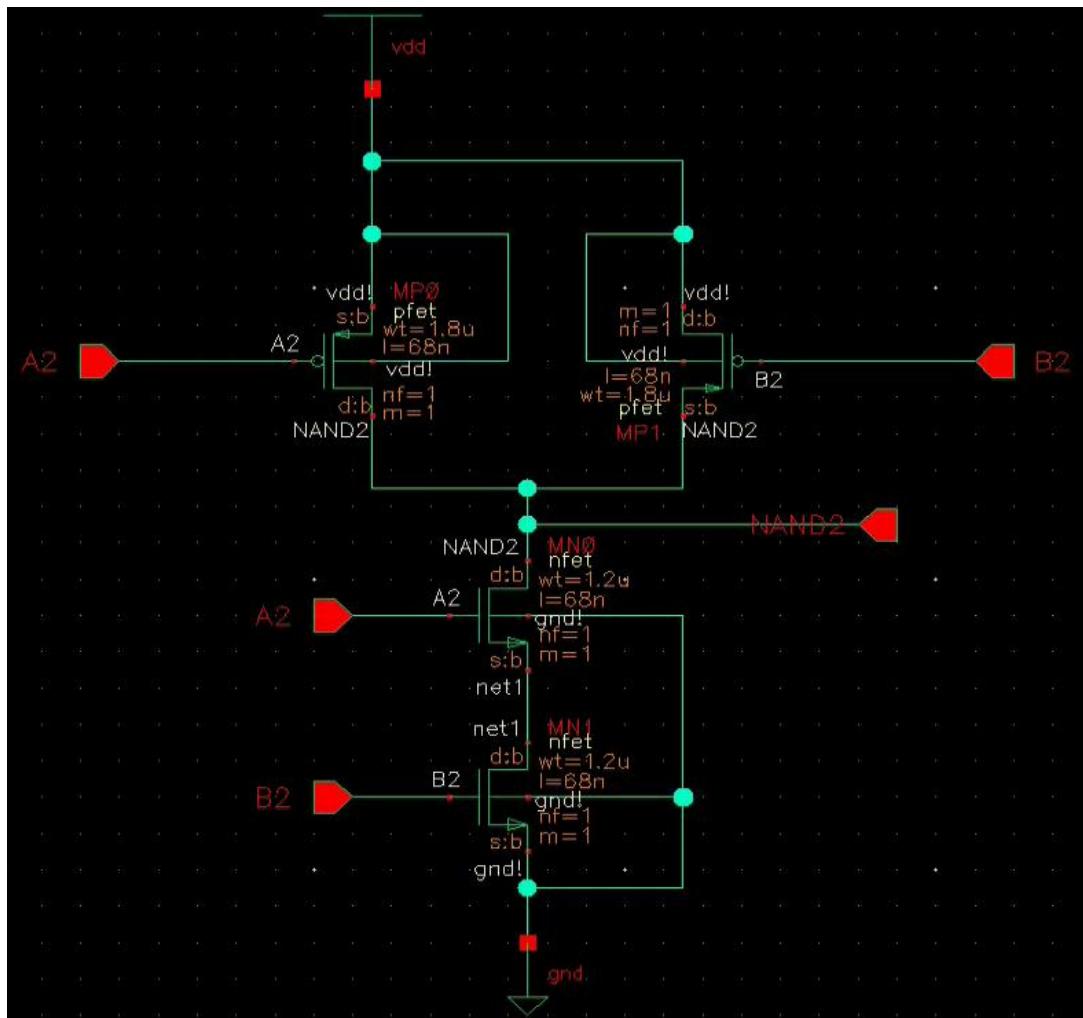
Function

$$\text{OUT} = \text{NOT } (\text{AB})$$

Truth Table

INPUT (A2)	INPUT (B2)	OUTPUT (NAND2)
0	0	1
0	1	1
1	0	1
1	1	0

Schematic

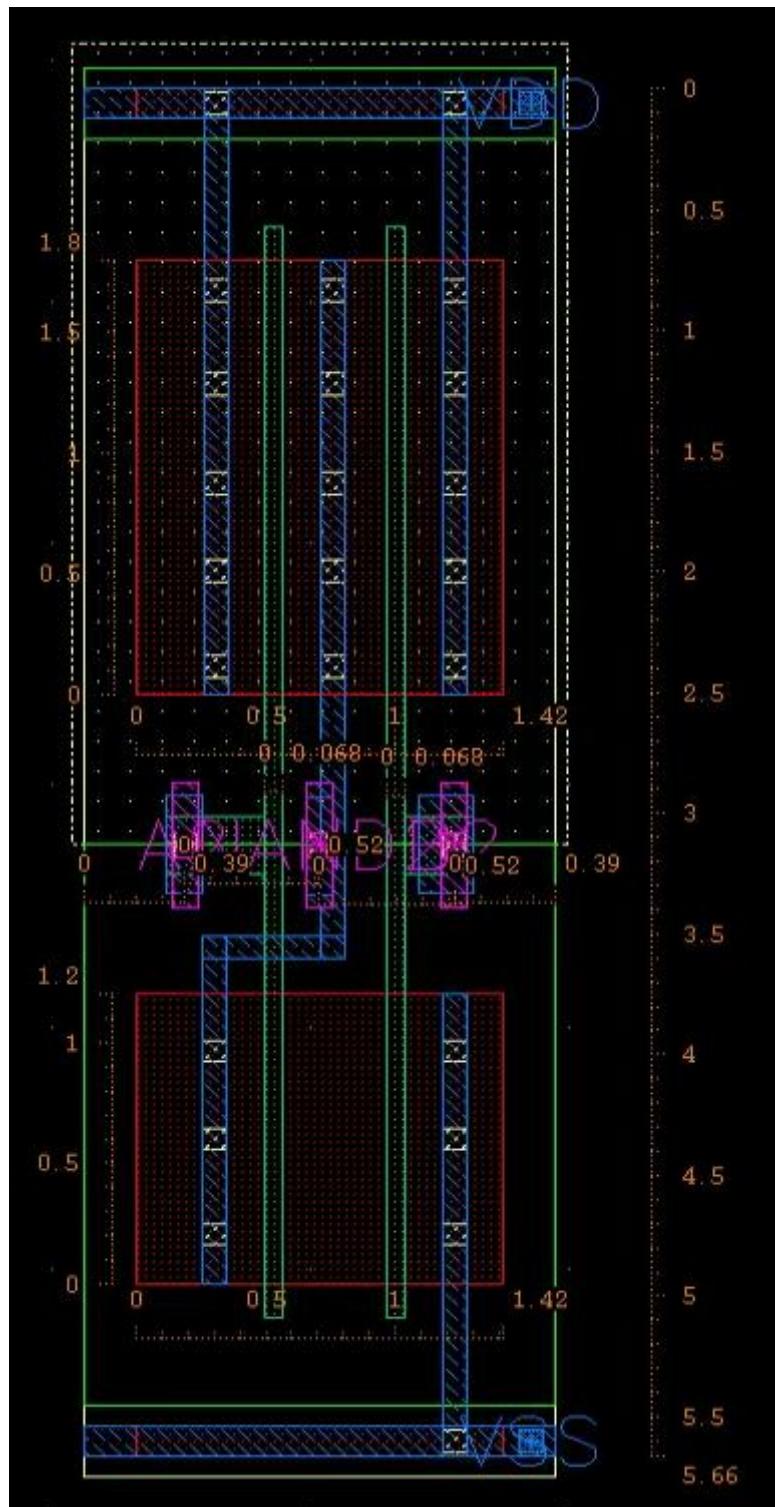


Layout

Cell Height = 5.660 μm

Cell Width = 1.420 μm

Total Cell Area = 8.0372 μm^2



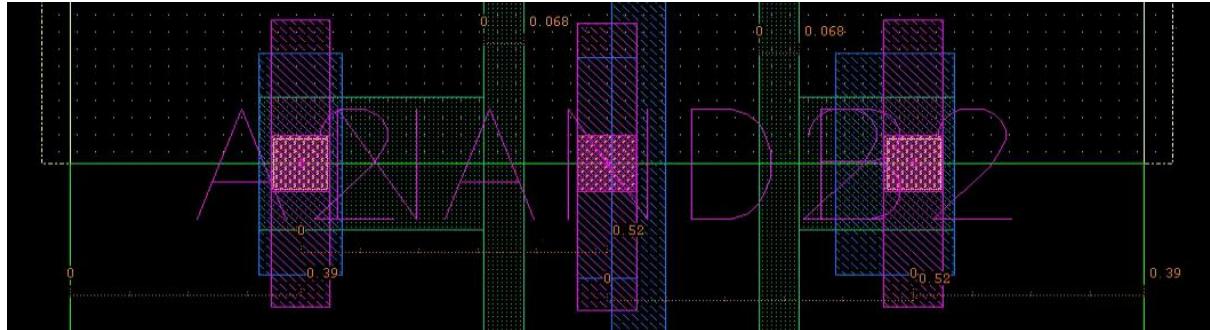
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

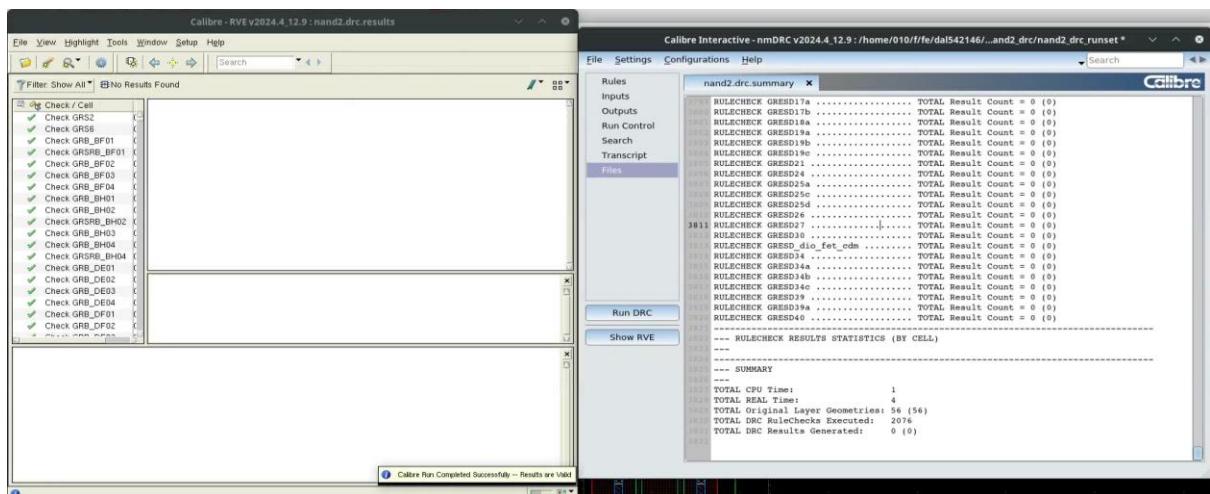
Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

Offset (right side) = 0.39 um



DRC Result



LVS Result

Calibre - RVE v2024.4_12.9 : svdb nand2

Calibre Interactive - nmLVS v2024.4_12.9 : /home/010/f/fe/dal542146/...and2_lvs/nand2_lvs.runset *

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
nand2	nand2	SL, SS	TL, TS	SL, SS

Cell nand2 Summary (Clear)

LAYOUT CELL NAME: nand2
SOURCE CELL NAME: nand2

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	5	
Nets:	6	6	
Instances:	2	2	IN (4 pins) NP (4 pins)
Total Inst:	4	4	

OVERALL COMPARISON RESULTS

PEX Result

Calibre Interactive - PEX v2024.4_12.9 : /home/010/f/fe/dal542146/...and2_lvs/nand2_pex_runset *

Transcript

```

total nets = 6
top-level nets = 6
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0
=====
CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 1
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Tue Nov 4 21:56:13 2025
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 50/54/638 MALLOC = 378/378/686 ELAPSED

*** xRC run finished with exit code 0 ***

```

0 Errors, 4 Warnings, 1 Info

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51466	Warning	Please increase descriptors limit for best performance (8192)
53555	Warning	Please increase descriptors limit for best performance (8192)
54863	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

PEX Generated Netlist

```
# File: nand2.pex.sp
# Created: Wed Nov 5 20:52:17 2025
# Program "Calibre xRC"
# Version "v2024.4_12.9"
#
.include "nand2.pex.sp.pex"
.subckt nand2 NAND2 GND! VDD! A2 B2
*
* B2 B2
* A2 A2
* VDD VDD
* VSS VSS
* NAND2 NAND2
D0_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=6.3744e-12
+ PERIM=1.048e-05
XMMN0 N NAND2 MMN0_d N A2 MMN0_g NET1 N GND! D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=6e-13 AS=2.4e-13 PD=3.4e-06 PS=1.6e-06 NRD=0.165 NRS=0.166667 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5e-07 SB=8.52e-07 SD=0 PANW1=0
+ PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14 PANW8=1.36e-14
+ PANW9=2.72e-14 PANW10=2.856e-14
XMMN1 NET1 N B2 MMN1_g N_GND! MMN1_s N_GND! D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.4e-13 AS=4.608e-13 PD=1.6e-06 PS=3.168e-06 NRD=0.166667
+ NRS=0.164167 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=9.68e-07
+ SB=3.84e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMP0 N NAND2 MMP0_d N A2 MMP0_g N_VDD! MMP0_s N_GND! D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=3.6e-13 AS=9e-13 PD=2.2e-06 PS=4.6e-06 NRD=0.108333
+ NRS=0.103889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5e-07
+ SB=8.52e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.0224e-13 PANW8=5.28e-14 PANW9=1.768e-13 PANW10=8.16e-14
XMMP1 N_VDD! MMP1_d N_B2 MMP1_g N NAND2 MMP0_d N_VDD! D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=6.912e-13 AS=3.6e-13 PD=4.368e-06 PS=2.2e-06
+ NRD=0.108889 NRS=0.113889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=9.68e-07 SB=3.84e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.3464e-13 PANW8=2.04e-14 PANW9=1.768e-13 PANW10=8.16e-14
*
.include "nand2.pex.sp.NAND2.pxi"
*
.ends
*
```

HSpice Setup File

```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "nand2.pex.sp" $ .subckt nand2 NAND2 VSS VDD A2 B2

.option post runlvl=5

$ DUT instance (pin order per PEX header: NAND2 VSS VDD A2 B2)
xi OUT VSS VDD INA INB nand2

$ VDD = 1.2 V
vdd VDD VSS 1.2v

$ ===== Stimulus =====
$ Input slew requirement: 10-90% = 35 ps ~ 0-100% = 43.75 ps
$ Sequence (2 ns per state): 00 → 01 → 11 → 10 → 00
vinA INA VSS PWL( 0ns 0v 4.04375ns 1.2v 8ns 1.2v 8.04375ns 0v 12ns 0v )
vinB INB VSS PWL( 0ns 0v 2ns 0v 2.04375ns 1.2v 6ns 1.2v 6.04375ns 0v 12ns 0v )

$ Output load = 45 fF
COUT OUT VSS 45f

$ ===== Analysis =====
.tr 100ps 12ns

$ ===== Measurements =====
$ Measure at 50% (0.6V) threshold
.measure tran t_in_r WHEN v(INA)=0.6 RISE=1
.measure tran t_out_f WHEN v(OUT)=0.6 FALL=1
.measure tran tphl PARAM='t_out_f - t_in_r'

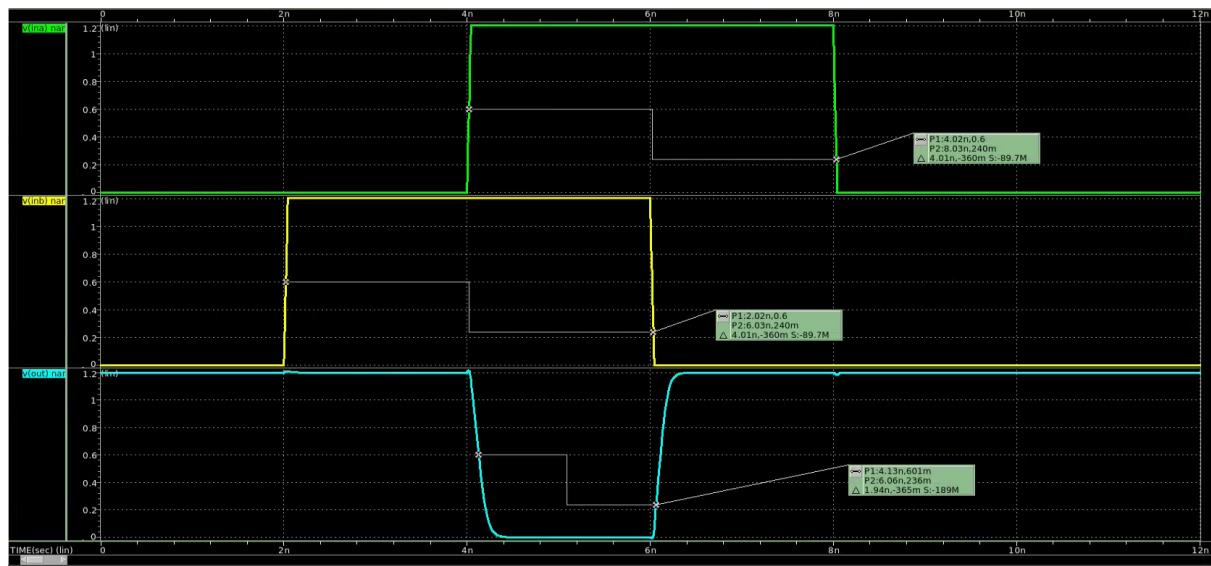
.measure tran t_in_f WHEN v(INA)=0.6 FALL=1
.measure tran t_out_r WHEN v(OUT)=0.6 RISE=1
.measure tran tphl PARAM='t_out_r - t_in_f'

.measure tavg PARAM='(tphl+tphl)/2'
.measure tdiff PARAM='abs(tphl-tphl)'
.measure delay PARAM='max(tphl,tphl)'

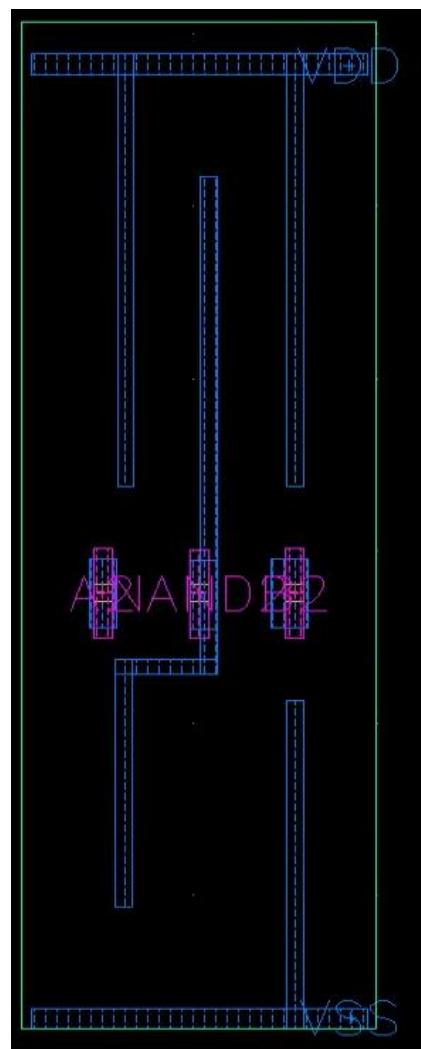
$ Average current & energy during a 1 ns window (switching period)
.measure tran iavg AVG I(vdd) FROM=4ns T0=5ns
.measure tran energy PARAM='1.2*iavg*1ns'
.measure tran edp PARAM='abs(delay*energy)'

.end
```

HSpice Simulation Waveform



Abstract View



NOR2

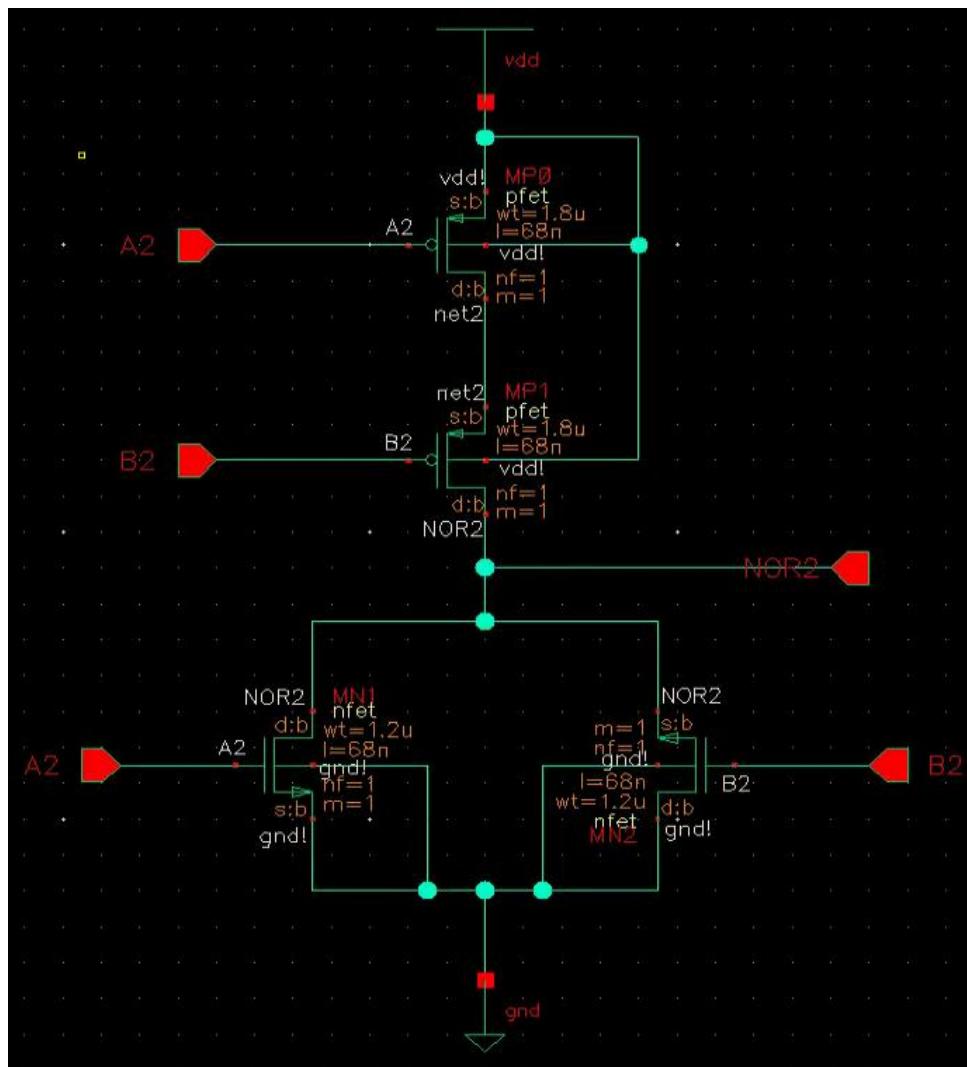
Function

$$\text{OUT} = \text{NOT } (\text{A} \mid \text{B})$$

Truth Table

INPUT (A3)	INPUT (B3)	OUTPUT (NOR2)
0	0	1
0	1	0
1	0	0
1	1	0

Schematic

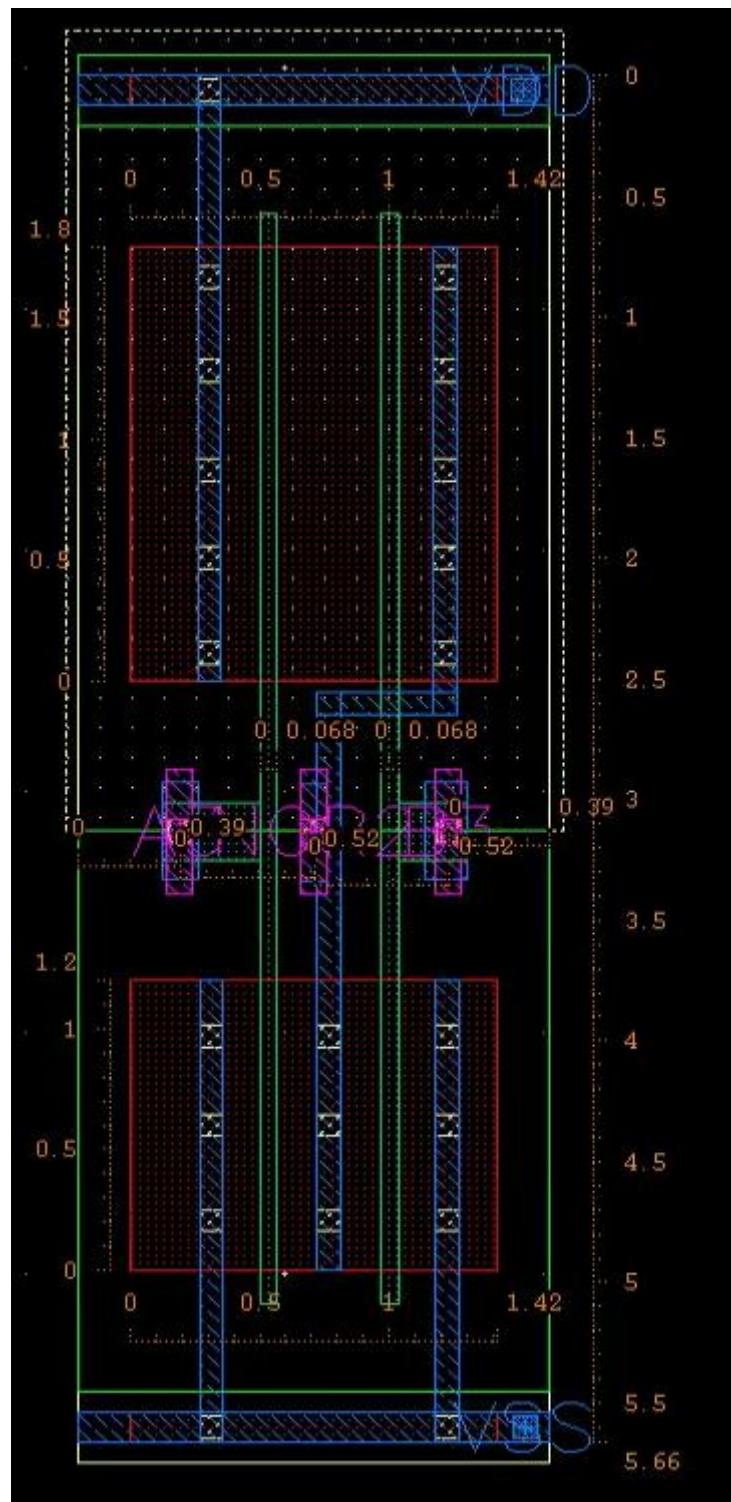


Layout

Cell Height = 5.660 μm

Cell Width = 1.420 μm

Total Cell Area = 8.0372 μm^2



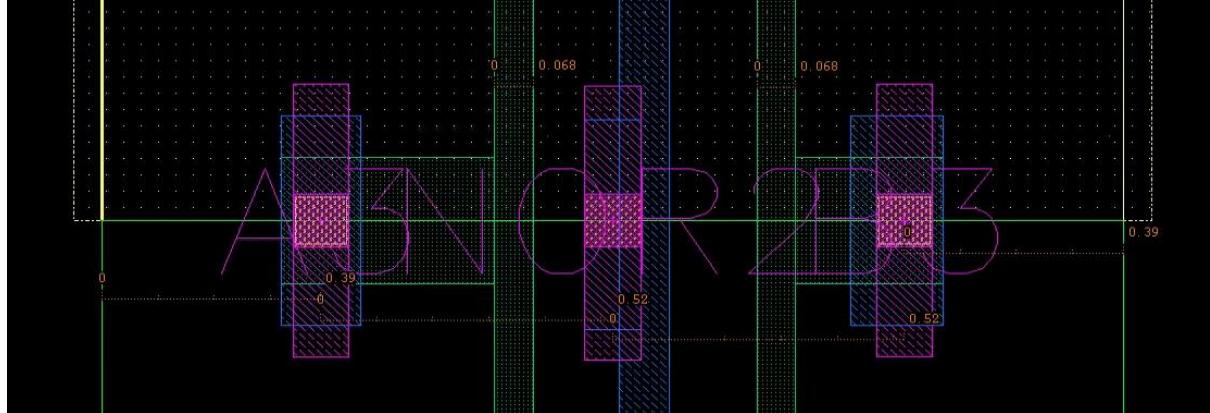
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

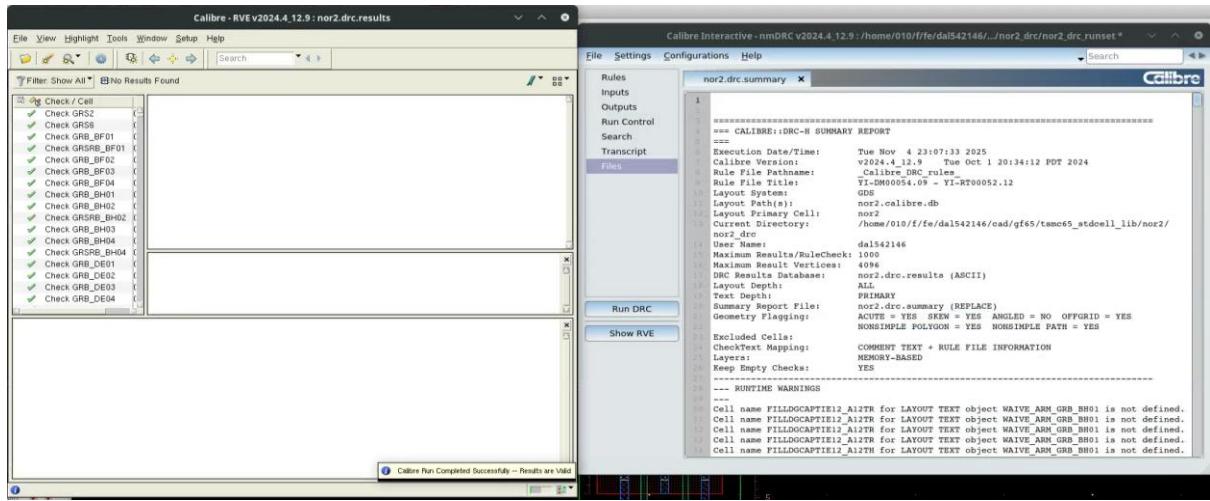
Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

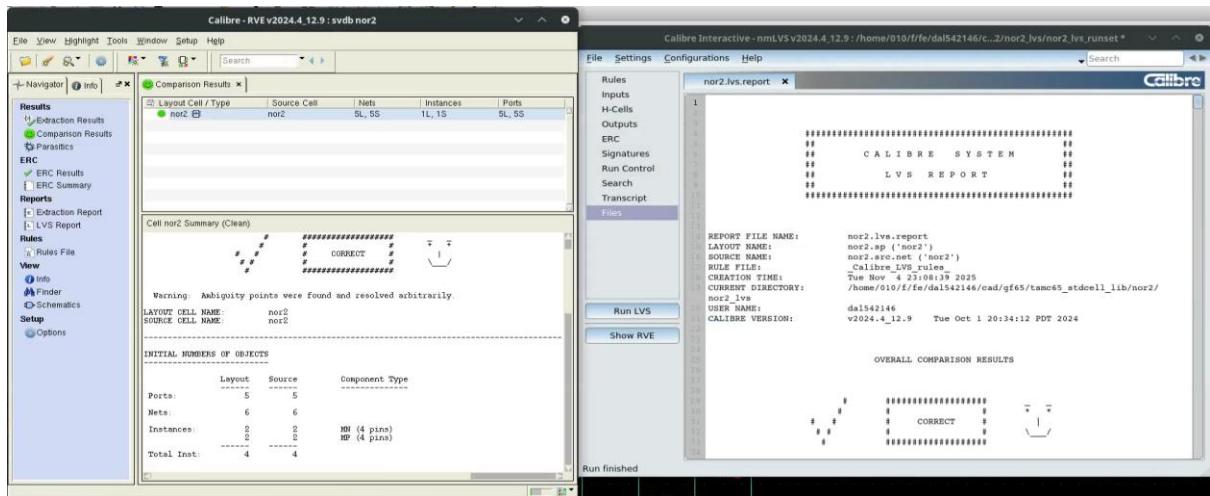
Offset (right side) = 0.39 um



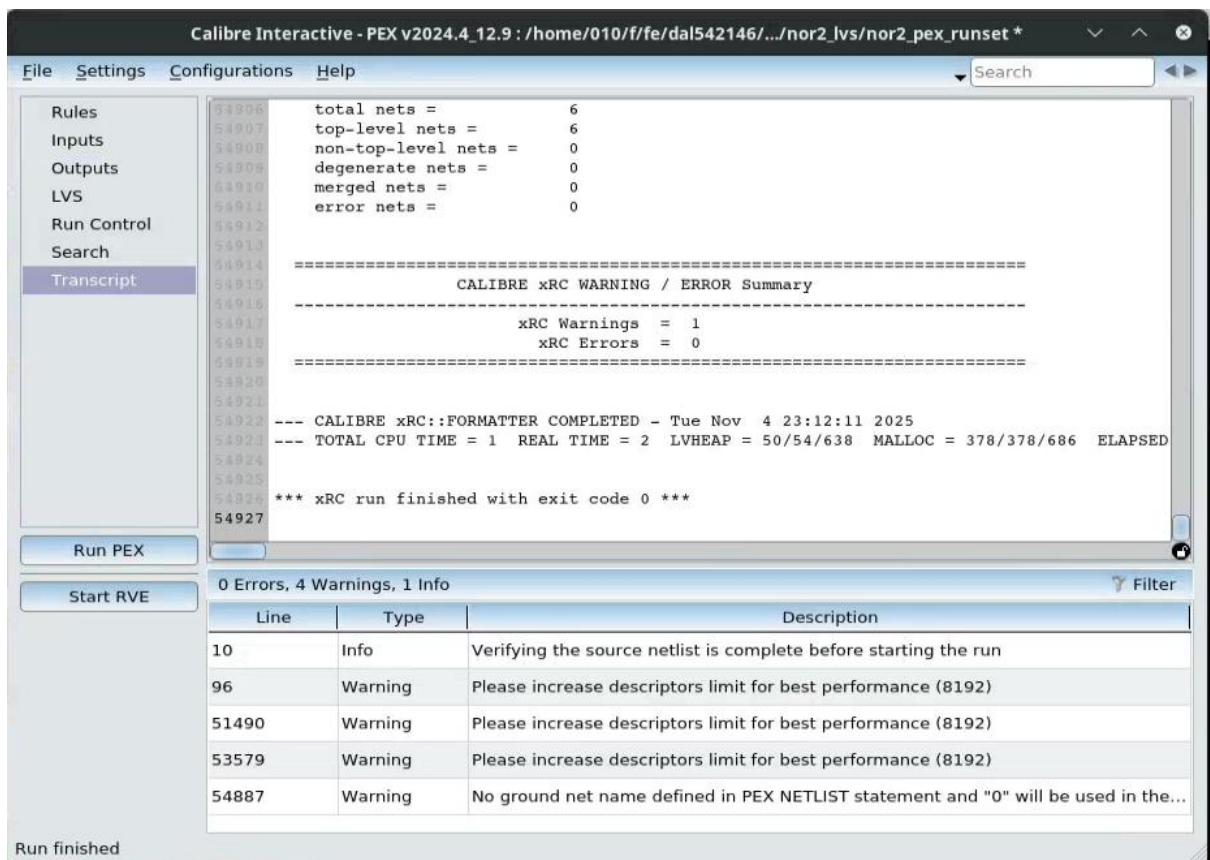
DRC Result



LVS Result



PEX Result



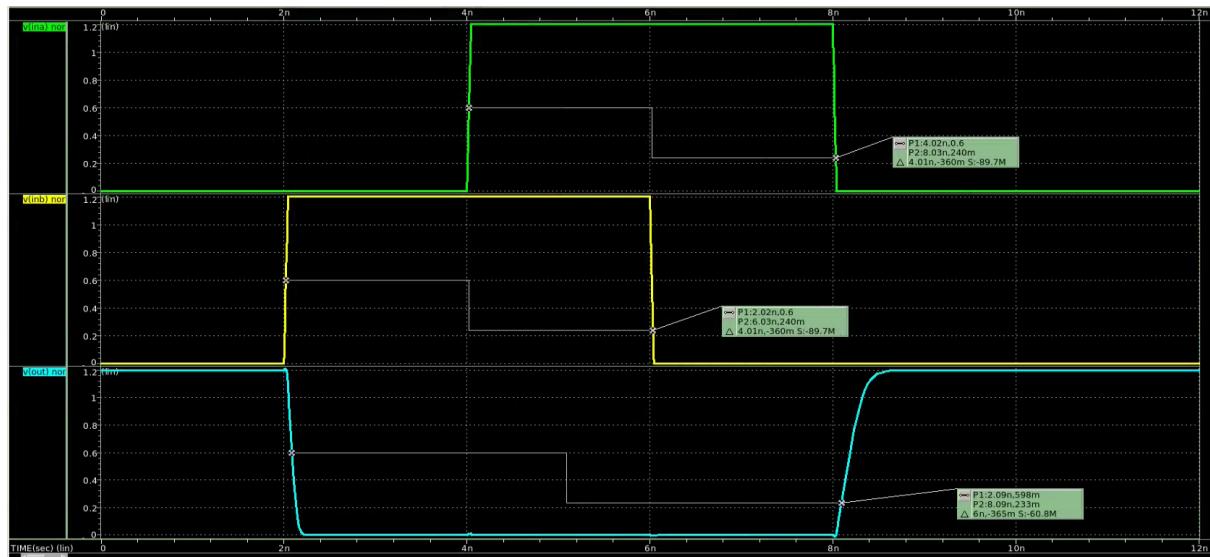
PEX Generated Netlist

```
* File: nor2.pex.sp
* Created: Wed Nov 5 21:01:58 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "nor2.pex.sp.pex"
.subckt nor2 GND! NOR2 VDD! B2 A2
*
* B3     B3
* A3     A3
* VDD    VDD
* NOR2   NOR2
* VSS    VSS
XD0_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=6.3744e-12
+ PERIM=1.048e-05
XMMN2_N_GND!_MMN2_d_N_B2_MMN2_g_N_NOR2_MMN2_s_N_GND!_D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=6e-13 AS=2.4e-13 PD=3.4e-06 PS=1.6e-06 NRD=0.155833
+ NRS=0.165 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5e-07 SB=8.52e-07
+ SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14
+ PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN1_N_NOR2_MMN2_S_N_A2_MMN1_g_N_GND!_MMN1_s_N_GND!_D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.4e-13 AS=4.608e-13 PD=1.6e-06 PS=3.168e-06
+ NRD=0.168333 NRS=0.156667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=9.68e-07 SB=3.84e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMPI1_NET2_N_B2_MMPI1_g_N_VDD!_MMPI1_s_N_VDD!_D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=3.6e-13 AS=9e-13 PD=2.2e-06 PS=4.6e-06 NRD=0.111111 NRS=0.108333
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5e-07 SB=8.52e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.0224e-13
+ PANW8=5.28e-14 PANW9=1.768e-13 PANW10=8.16e-14
XMMPO_N_NOR2_MMPO_d_N_A2_MMPO_g_NET2_N_VDD!_D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=6.912e-13 AS=3.6e-13 PD=4.368e-06 PS=2.2e-06 NRD=0.1 NRS=0.111111
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=9.68e-07 SB=3.84e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.3464e-13
+ PANW8=2.04e-14 PANW9=1.768e-13 PANW10=8.16e-14
*
.include "nor2.pex.sp.NOR2.pxi"
*
.ends
*
```

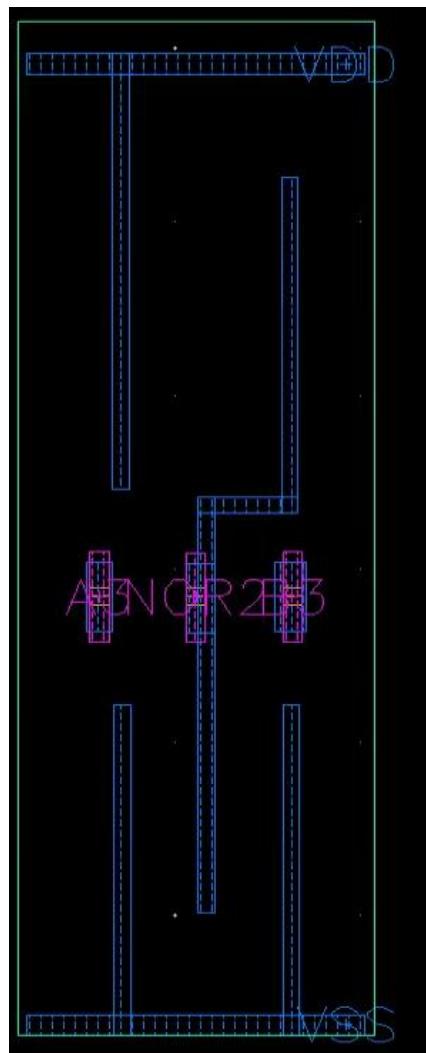
HSpice Setup File

```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "nor2.pex.sp" $ .subckt nor2 VSS NOR2 VDD B2 A2
.option post runlvl=5
$ DUT instance (pin order per PEX header: VSS NOR2 VDD B2 A2)
xi VSS OUT VDD INB INA nor2
$ VDD = 1.2 V
vdd VDD VSS 1.2v
$ ===== Stimulus =====
$ 10-90% slew = 35 ps -> 0-100% = 43.75 ps
$ Sequence (2 ns steps): 00 → 01 → 11 → 10 → 00
vinB INB VSS PWL( 0ns 0v 2ns 0v 2.04375ns 1.2v 6ns 1.2v 6.04375ns 0v 12ns 0v )
vinA INA VSS PWL( 0ns 0v 4ns 0v 4.04375ns 1.2v 8ns 1.2v 8.04375ns 0v 12ns 0v )
$ Output load = 45 fF
COUT OUT VSS 45f
$ ===== Analysis =====
.tr 100ps 12ns
$ ===== Measurements =====
.measure tran t_in_r WHEN v(INA)=0.6 RISE=1
.measure tran t_out_f WHEN v(OUT)=0.6 FALL=1
.measure tran tphl PARAM='t_out_f - t_in_r'
.measure tran t_in_f WHEN v(INA)=0.6 FALL=1
.measure tran t_out_r WHEN v(OUT)=0.6 RISE=1
.measure tran tphl PARAM='t_out_r - t_in_f'
.measure tavg PARAM='(tplh+tphl)/2'
.measure tdiff PARAM='abs(tplh-tphl)'
.measure delay PARAM='max(tplh,tphl)'
.measure tran iavg AVG I(vdd) FROM=4ns TO=5ns
.measure tran energy PARAM='1.2*iavg*ins'
.measure tran edp PARAM='abs(delay*energy)'
.end
```

HSpice Simulation Waveform



Abstract View



XOR2

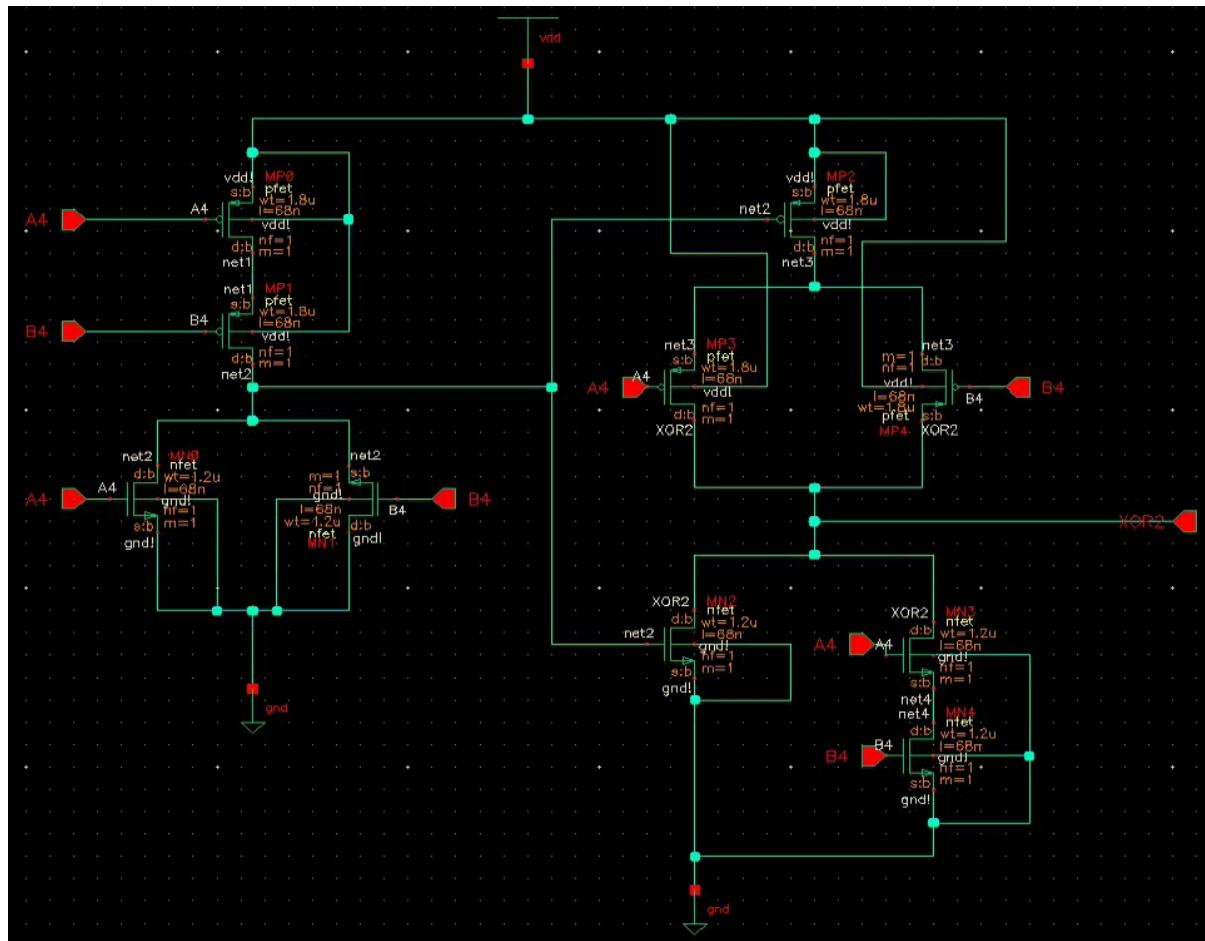
Function

$$\text{OUT} = ((\text{NOT}(A)) \& B) | ((\text{NOT}(B)) \& A)$$

Truth Table

INPUT (A4)	INPUT (B4)	OUTPUT (XOR2)
0	0	0
0	1	1
1	0	1
1	1	0

Schematic

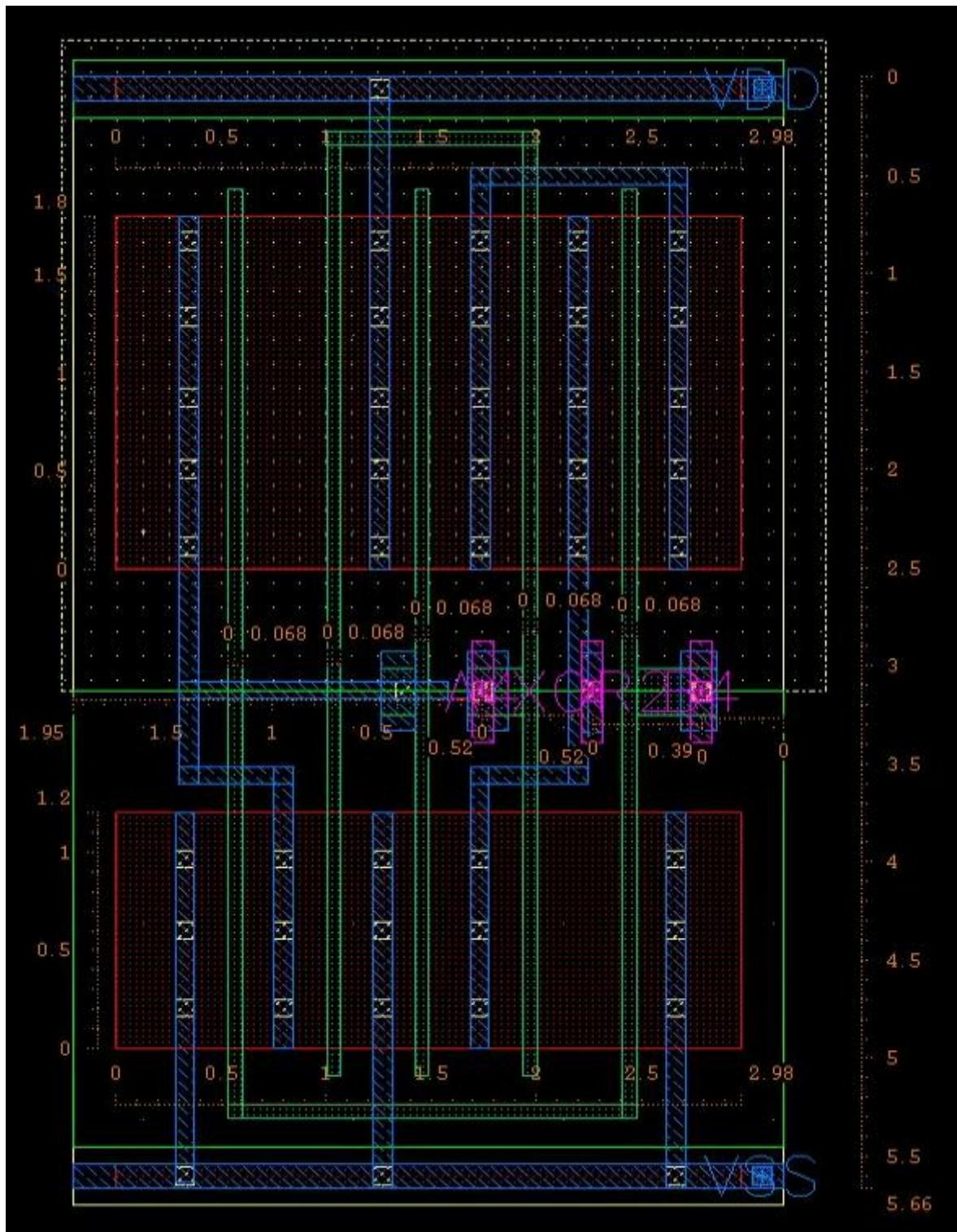


Layout

Cell Height = 5.660 μm

Cell Width = 2.980 μm

Total Cell Area = 16.8668 μm^2



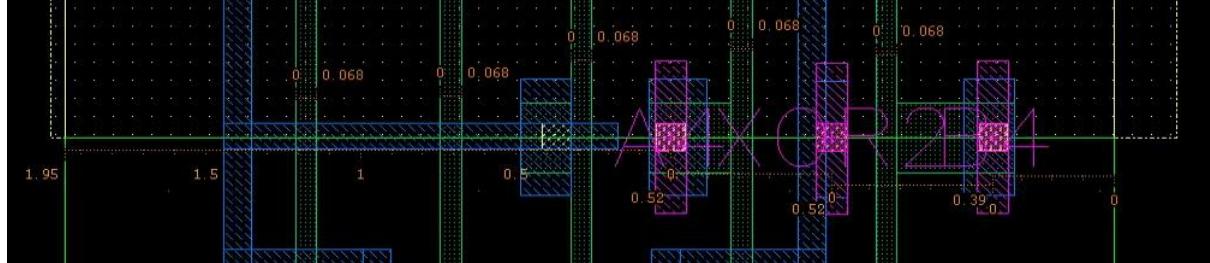
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

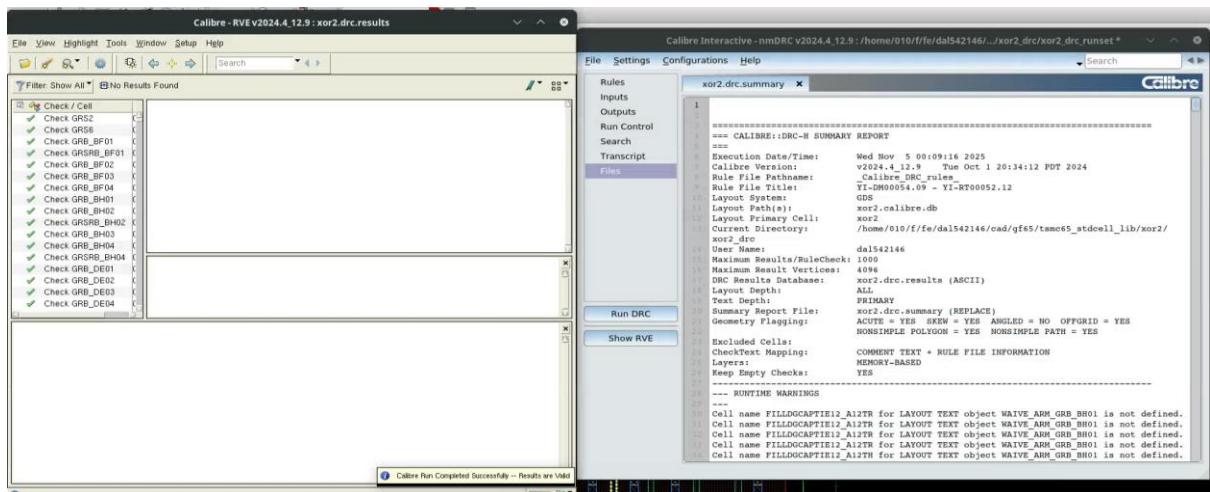
Pin Pitch = 0.52 um

Offset (left side) = 1.95 um

Offset (right side) = 0.39 um



DRC Result



LVS Result

Calibre - RVE v2024.4_12.9 : svdb xor2

Calibre Interactive - nmLVS v2024.4_12.9 : /home/010/f/fe/dal542146/c.../xor2_lvs/xor2_lvs_sunset *

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
xor2	xor2	6L, 6S	4L, 4S	5L, 5S

Cell xor2 Summary (Clean)

LAYOUT CELL NAME: xor2
SOURCE CELL NAME: xor2

INITIAL NUMBERS OF OBJECTS

Layout	Source	Component Type
Ports:	5	5
Nets:	9	9
Instances:	5	5
Total Inst:	10	10
	NP (4 pins)	NP (4 pins)

OVERALL COMPARISON RESULTS

Run finished

xor2.lvs.report

```

=====
## CALIBRE SYSTEM
## LVS REPORT
=====

REPORT FILE NAME: xor2.lvs.report
LAYOUT NAME: xor2.ap ('xor2')
SOURCE NAME: xor2.soc.net ('xor2')
RULE FILE: _Calibre_LVS.rules
DATE: Wed Nov 5 00:10:12 2025
CURRENT DIRECTORY: /home/010/f/fe/dal542146/cad/gf65/tmc65_stdcell_lib/xor2/
xor2_lvs
USER NAME: dal542146
CALIBRE VERSION: v2024.4_12.9 Tue Oct 1 20:34:12 PDT 2024

```

PEX Result

Calibre Interactive - PEX v2024.4_12.9 : /home/010/f/fe/dal542146/.../xor2_lvs/xor2_pex_sunset *

Transcript

```

54802 total nets = 9
54803 top-level nets = 8
54804 non-top-level nets = 0
54805 degenerate nets = 1
54806 merged nets = 0
54807 error nets = 0
=====
54808
54809                               CALIBRE xRC WARNING / ERROR Summary
54810 -----
54811           xRC Warnings = 1
54812           xRC Errors = 0
54813
54814
54815
54816
54817
54818
54819 --- CALIBRE xRC::FORMATTER COMPLETED - Wed Nov 5 00:12:07 2025
54820 --- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 50/54/638 MALLOC = 378/378/687 ELAPSED
54821
54822 *** xRC run finished with exit code 0 ***
54803

```

0 Errors, 4 Warnings, 1 Info

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51466	Warning	Please increase descriptors limit for best performance (8192)
53555	Warning	Please increase descriptors limit for best performance (8192)
54863	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

Run finished

PEX Generated Netlist

```

* File: xor2.pex.sp
* Created: Wed Nov  5 21:09:52 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "xor2.pex.sp.pex"
.subckt xor2 GND! XOR2 VDD! B4 A4
*
* A4      A4
* B4      B4
* VDD     VDD
* XOR2    XOR2
* VSS     VSS
X00_noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=1.20516e-11
+ PERIM=1.39e-05
XMMN1 N GND! MMN1_d N B4 MMN1_g N NET2_MMN1_s N GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=6.48e-13 AS=2.4e-13 PD=3.48e-06 PS=1.6e-06 NRD=0.173333
+ NR5=0.163333 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.4e-07
+ SB=2.372e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN0 N NET2_MMN1_s N A4 MMN0_g N GND! MMN0_s N GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.4e-13 AS=2.106e-13 PD=1.6e-06 PS=1.551e-06 NRD=0.17
+ NR5=0.164167 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.008e-06
+ SB=1.904e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN2 N XOR2_MMN2_d N NET2_MMN2_g N GND! MMN2_s N GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.694e-13 AS=2.106e-13 PD=1.649e-06 PS=1.551e-06
+ NRD=0.2 NR5=0.128333 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=1.427e-06 SB=1.485e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN3 N XOR2_MMN2_d N NET2_MMN3_g NET4_N GND! D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.694e-13 AS=2.4e-13 PD=1.649e-06 PS=1.6e-06 NRD=0.174167
+ NR5=0.166667 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.944e-06
+ SB=9.68e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN4 NET4_N B4 MMN4_g N GND! MMN4_s N GND! D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.694e-13 AS=2.106e-13 PD=1.6e-06 PS=3.4e-06 NRD=0.166667 NR5=0.155833
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=2.412e-06 SB=5e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14 PANW8=1.36e-14
+ PANW9=2.72e-14 PANW10=2.856e-14
XMMP1 N NET2_MMPL1_d N B4 MMP1_g NET1_N VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=9.72e-13 AS=3.6e-13 PD=4.68e-06 PS=2.2e-06 NRD=0.103889
+ NR5=0.111111 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5.4e-07
+ SB=2.372e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=3.024e-14 PANW8=1.248e-13 PANW9=5.44e-14 PANW10=8.16e-14
XMMP0 NET1_N A4 MMP0_g N VDD! MMP0_s N VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=3.6e-13 AS=3.159e-13 PD=2.2e-06 PS=2.151e-06 NRD=0.111111
+ NR5=0.101111 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.008e-06
+ SB=1.904e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.84e-14 PANW9=1.768e-13 PANW10=8.16e-14
XMMP2_N NET3_MMPL2_d N NET2_MMPL2_g N VDD! MMP2_s N VDD! D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.041e-13 AS=3.159e-13 PD=2.249e-06 PS=2.151e-06
+ NRD=0.136111 NR5=0.0938889 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.427e-06 SB=1.485e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0

```

HSpice Setup File

```

$example HSPICE setup file

$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lp_e_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "xor2.pex.sp" $ .subckt xor2 VSS XOR2 VDD B4 A4

.option post runlvl=5

$ DUT instance (pin order per PEX: VSS XOR2 VDD B4 A4)
xi VSS OUT VDD INB INA xor2

$ VDD
vdd VDD VSS 1.2v

$ ===== Stimulus =====
$ 10-90% slew = 35 ps → 0-100% = 43.75 ps
$ Sequence (2 ns steps): 00 → 01 → 11 → 10 → 00
|
vinA INA VSS PWL( 0ns 0v 4ns 0v 4.04375ns 1.2v 8ns 1.2v 8.04375ns 0v 12ns 0v )
vinB INB VSS PWL( 0ns 0v 2ns 0v 2.04375ns 1.2v 6ns 1.2v 6.04375ns 0v 12ns 0v )

$ Output load
COUT OUT VSS 45f

$ ===== Analysis =====
.tr 100ps 12ns

$ ===== Measurements =====
$ Measure vs A's edges (you can also add ones vs B if desired)
.measure tran t_in_rA WHEN v(INA)=0.6 RISE=1
.measure tran t_out_f WHEN v(OUT)=0.6 FALL=1
.measure tran tPHL PARAM='t_out_f - t_in_rA'

.measure tran t_in_fa WHEN v(INA)=0.6 FALL=1
.measure tran t_out_r WHEN v(OUT)=0.6 RISE=1
.measure tran tPLH PARAM='t_out_r - t_in_fa'

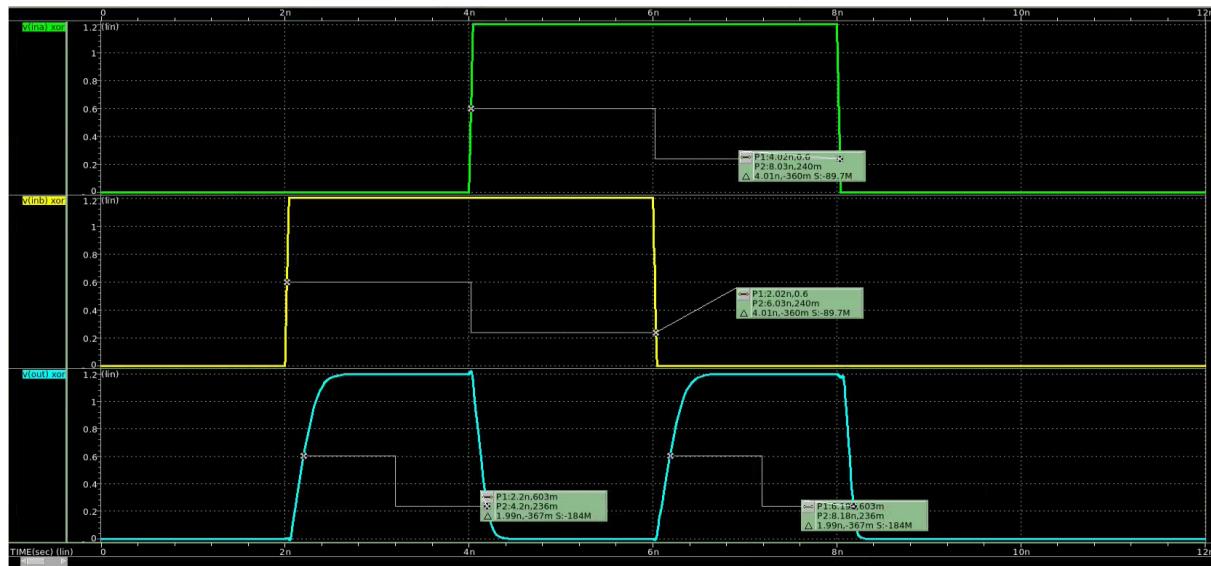
.measure tavg PARAM='(tPLH+tPHL)/2'
.measure tdiff PARAM='abs(tPLH-tPHL)'
.measure delay PARAM='max(tPLH,tPHL)'

$ Power window around a toggle
.measure tran iavg AVG I(vdd) FROm=4ns T0=5ns
.measure tran energy PARAM='1.2*iavg*ins'
.measure tran edp PARAM='abs(delay*energy)'

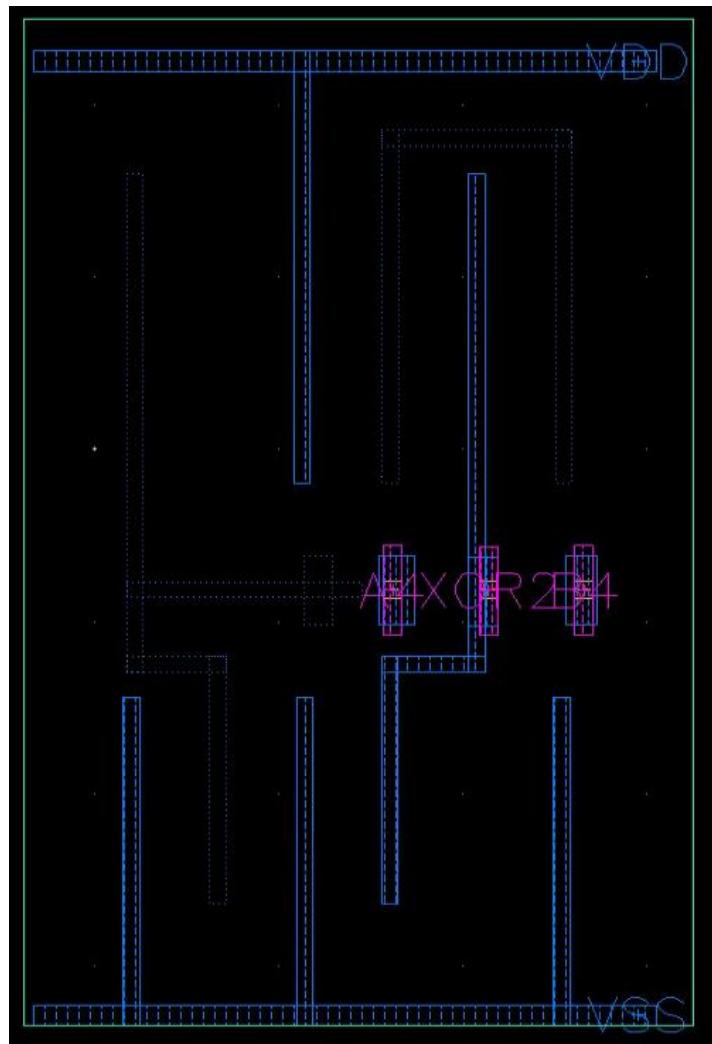
.end

```

HSpice Simulation Waveform



Abstract View



AOI22

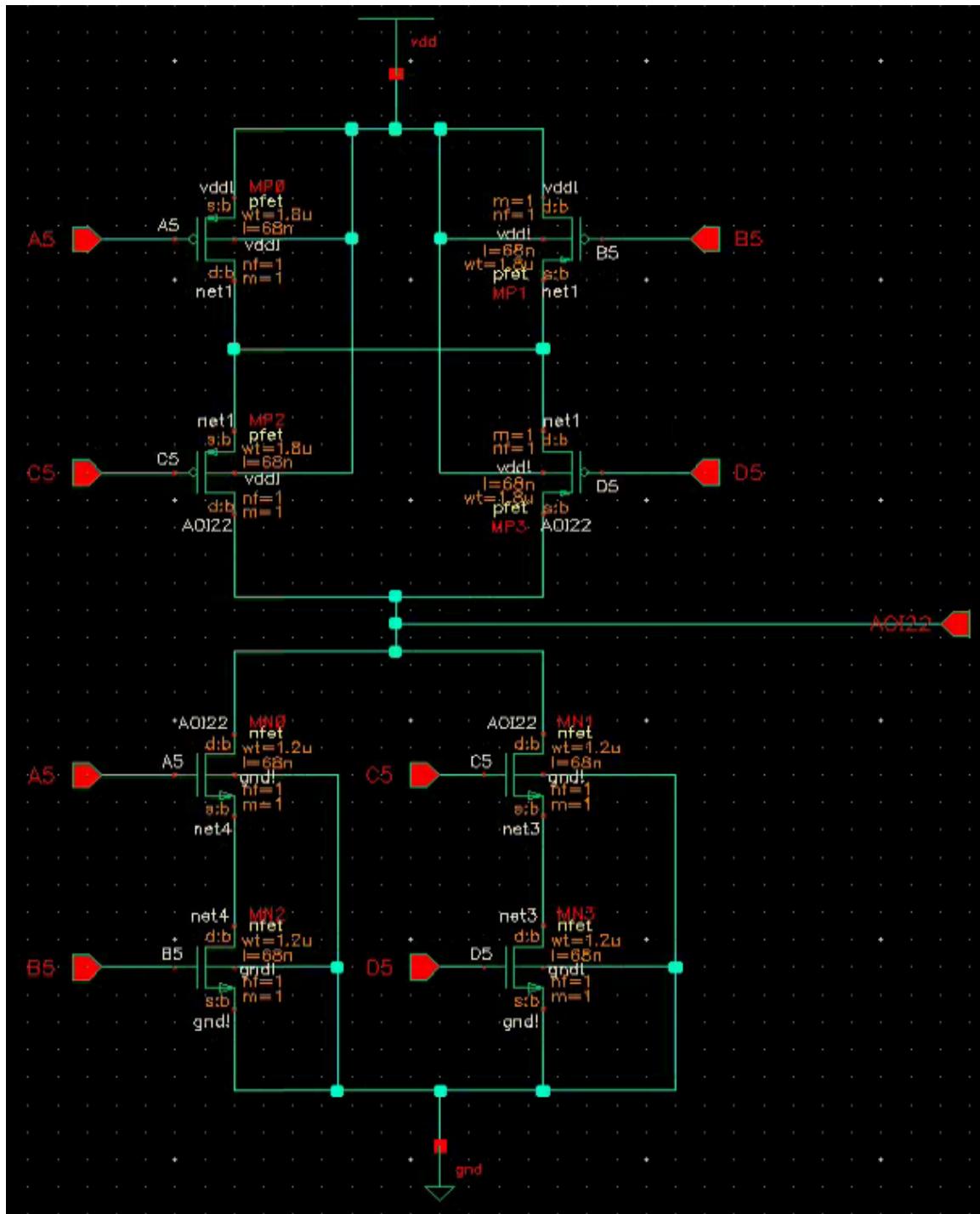
Function

$$\text{OUT} = \text{NOT } (\text{AB} \mid \text{CD})$$

Truth Table

INPUT (A5)	INPUT (B5)	INPUT (C5)	INPUT (D5)	OUTPUT (AOI22)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Schematic

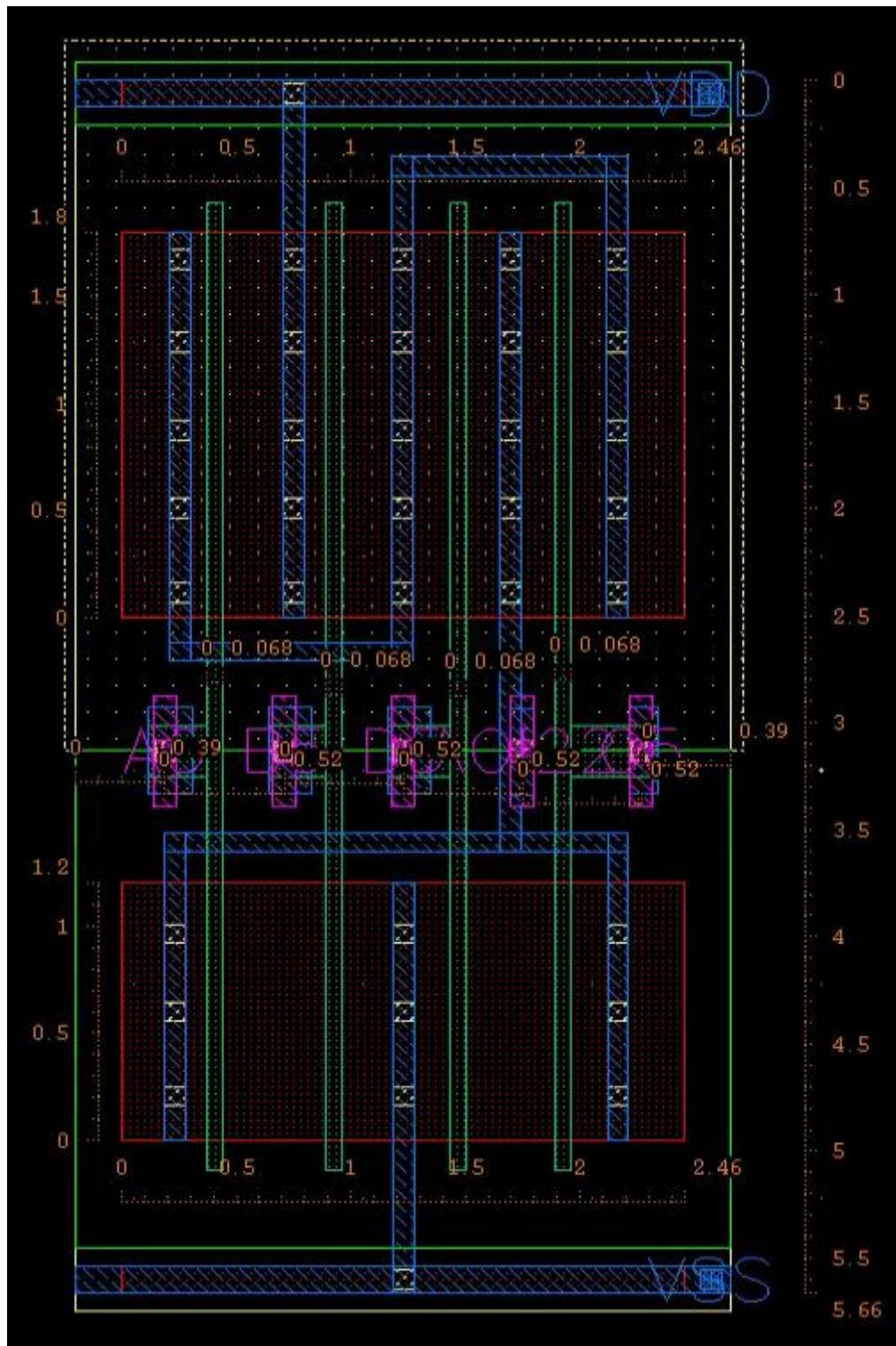


Layout

Cell Height = 5.660 μm

Cell Width = 2.460 μm

Total Cell Area = 13.9236 μm^2



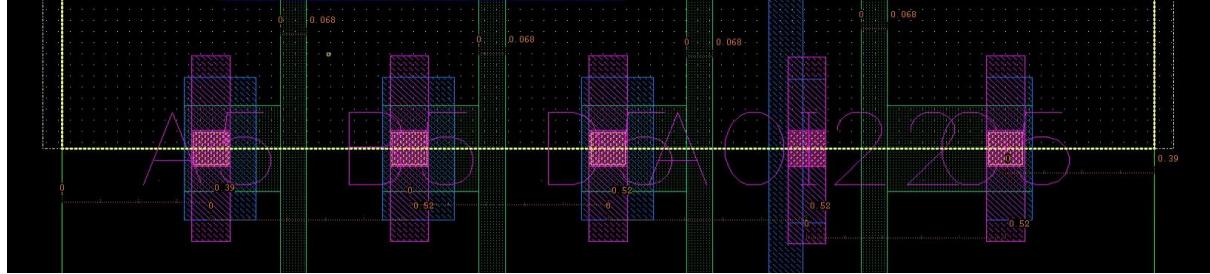
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

Offset (right side) = 0.39 um



DRC Result

The screenshot shows the Calibre interface with two main windows. The left window is titled 'Calibre - RVE v2024.4.12.9 : aoi22.drc.results' and displays a tree view of checked cells under the 'Check / Cell' category. The right window is titled 'Calibre Interactive - nmDRC v2024.4.12.9 : /home/010/f/fe/dal542146/.../aoi22_drc/aoi22.drc_runset*' and shows the 'aoi22.drc.summary' report. The report contains detailed configuration information and a log of DRC results, including sections for Rules, Inputs, Outputs, Run Control, Search, Transcript, and Files. The summary report also includes sections for RUNTIME:SUMMARY, RUNTIME:WARNINGS, and a list of errors related to undefined layout objects like 'FILLDGCAPIE12_A11TH' and 'FILLDGCAPIE12_A12TH'.

```
=====
CALIBRE:DRC-H SUMMARY REPORT
=====
Execution Date/Time: Wed Nov 5 00:47:27 2025
Calibre Version: v2024.4.12.9 Tue Oct 1 20:34:12 PDT 2024
Rule File Pathname: Calibre_DRC_rules
Rule File Title: VI-DMO0054.09 - YI-RK00052.12
Run ID: 00000000000000000000000000000000
Layout Path(s):
Layout Primary Cell: aoi22
Layout Directory: /home/010/f/fe/dal542146/cad/gf65/tmc65_stdcell_lib/aoi22/
aoi22.drc
User Name: dal542146
Maximum Results/MultiCheck: 1000
Number of Result Vertices: 66
DRC Results Database: aoi22.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Report Output File: aoi22.drc.summary (REPLACE)
Geometry Flagging: ACUTE = YES SKew = YES ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = YES NONSIMPLE PATH = YES
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
=====
RUNTIME:WARNINGS
===
30 Cell name FILLDGCAPIE12_A11TH for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
Cell name FILLDGCAPIE12_A11TP for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
Cell name FILLDGCAPIE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
Cell name FILLDGCAPIE12_A12TH for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
Cell name FILLDGCAPIE12_A12TP for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
```

LVS Result

The screenshot shows two windows from the Calibre LVS interface. The left window, titled 'Calibre - RVE v2024.4_12.9 : svdb ao122', displays the 'Comparison Results' tab with a table showing one entry for 'ao122'. The right window, titled 'Calibre Interactive - nmLVS v2024.4_12.9 : /home/010/f/fe/dal542146/c...ao122_lvs/ao122_lvs.runset *', shows the 'ao122.lvs.report' file content. The report header includes details like REPORT FILE NAME: ao122.lvs.report, LAYOUT NAME: ao122, and SOURCE NAME: ao122.scd.net ('ao122'). The log section shows the command 'Run LVS' was run at Wed Nov 5 00:41:50 2025. The overall comparison results section indicates the run was successful.

PEX Result

The screenshot shows the Calibre Interactive PEX interface. The left sidebar includes tabs for Rules, Inputs, Outputs, LVS, Run Control, Search, and Transcript. The Transcript tab is selected, displaying the PEX run log. Key log entries include:

```

total nets = 10
top-level nets = 10
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

=====
CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 1
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Wed Nov 5 00:51:37 2025
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 50/54/638 MALLOC = 378/378/684 ELAPSED

*** xRC run finished with exit code 0 ***

```

Below the transcript, a summary table shows '0 Errors, 4 Warnings, 1 Info'. The table has columns for Line, Type, and Description.

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51470	Warning	Please increase descriptors limit for best performance (8192)
53559	Warning	Please increase descriptors limit for best performance (8192)
54867	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

PEX Generated Netlist

```
* File: aoi22.pex.sp
* Created: Wed Nov 5 21:19:07 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "aoi22.pex.sp.pex"
.subckt aoi22 AOI22 GND! VDD! A5 B5 D5 C5
*
* C5 C5
* D5 D5
* B5 B5
* A5 A5
* VDD VDD
* VSS VSS
* A0I22 A0I22
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=9.8272e-12
+ PERIM=1.256e-05
XMMN0 N_AOI22 MMN0 d N_A5_MMN0_g NET4 N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=4.464e-13 AS=2.712e-13 PD=3.144e-06 PS=1.652e-06 NRD=0.116667
+ NRS=0.188333 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=3.72e-07
+ SB=2.02e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN2 NET4 N_B5_MMN2_g N_GND!_MMN2_s_N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.712e-13 AS=2.856e-13 PD=1.652e-06 PS=1.676e-06 NRD=0.188333
+ NRS=0.2275 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=8.92e-07
+ SB=1.5e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN3 NET3 N_D5_MMN3_g N_GND!_MMN2_s_N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.328e-13 AS=2.856e-13 PD=1.588e-06 PS=1.676e-06 NRD=0.161667
+ NRS=0.169167 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.436e-06
+ SB=9.56e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN1 N_AOI22 MMN1 d N_C5_MMN1_g NET3 N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=6e-13 AS=2.328e-13 PD=3.4e-06 PS=1.588e-06 NRD=0.170833
+ NRS=0.161667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.892e-06
+ SB=5e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14
+ PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMPO_N_NET1_MMP0_d N_A5_MMP0_g N_VDD!_MMP0_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=6.696e-13 AS=4.068e-13 PD=4.344e-06 PS=2.252e-06
+ NRD=0.0655556 NRS=0.172222 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=3.72e-07 SB=2.02e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.3464e-13 PANW8=2.04e-14 PANW9=5.44e-14 PANW10=8.16e-14
XMMPI_N_VDD!_MMP0_s_N_B5_MMPI_g N_NET1_MMPI_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.068e-13 AS=4.284e-13 PD=2.252e-06 PS=2.276e-06
+ NRD=0.0788889 NRS=0.146111 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=8.92e-07 SB=1.5e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=1.768e-13 PANW10=2.04e-13
XMMP3_N_NET1_MMPI_s_N_D5_MMMP3_g N_AOI22_MMMP3_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.284e-13 AS=3.492e-13 PD=2.276e-06 PS=2.188e-06
+ NRD=0.118333 NRS=0.106111 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.436e-06 SB=9.56e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=1.768e-13 PANW10=2.04e-13
XMMP2_N_AOI22_MMMP2_s_N_C5_MMMP2_g N_NET1_MMMP2_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=3.492e-13 AS=9e-13 PD=2.188e-06 PS=4.6e-06 NRD=0.109444
```

HSpice Setup File

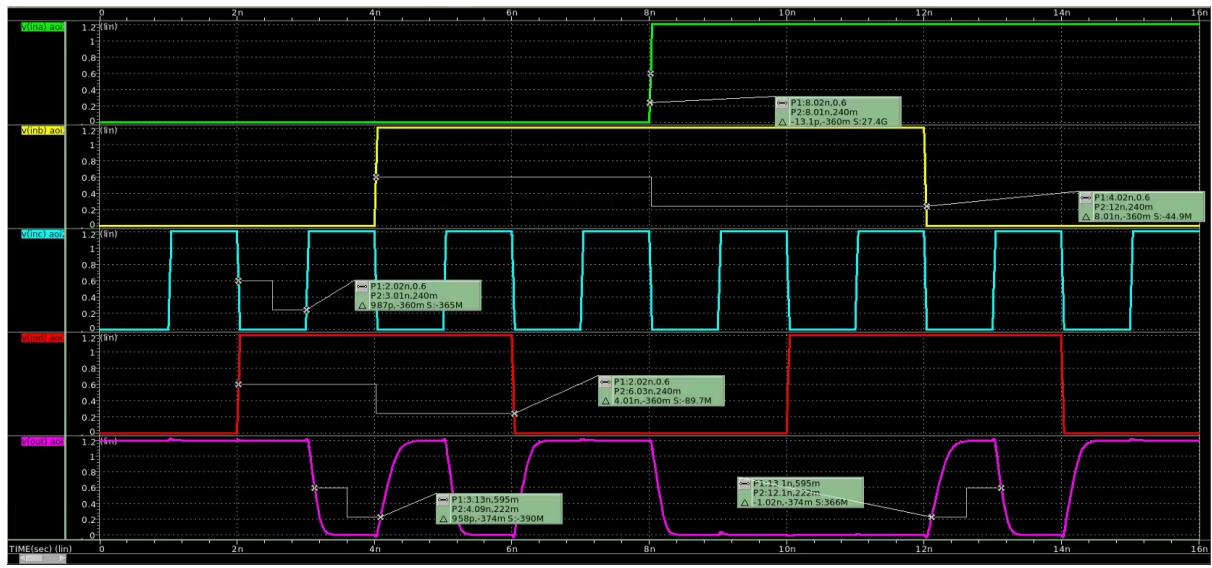
```
* Example HSPICE Testbench for Extracted A0I22
.include "/proj/cad/library/mosis/GF65_LPE/cmso10lpe.CDS_0a_dl064_11_20160415/models/YI-SM0030/Hspice/models/design.inc"
.include "aoi22.pex.sp"

.param VDD=1.2v
.vdd VDD GND !VDD

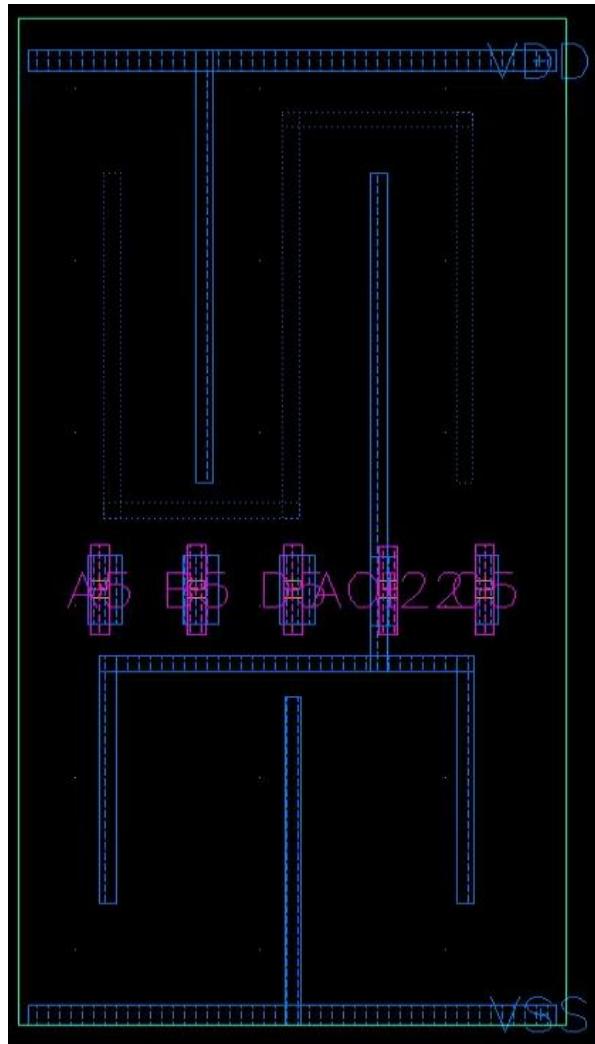
* transient analysis
.tran lps 16ns
.options post nomod

.measure tran t_in_f WHEN V(A5)=0.6 RISE=1
.measure tran t_out_f WHEN V(A5)=1.0 FLOOR=0.6 RISE=1
.measure tran t_PHL PARAM='t_out_f-t_in_f'
.measure tran t_in_fB WHEN V(B5)=0.6 FALSE=1
.measure tran t_out_f WHEN V(A0I22)=0.6 RISE=1
.measure tran t_PHL PARAM='t_out_f-t_in_f'
.measure tran tdiff PARAM='abs(t_PHL-t_PHL)'
.measure tran delay PARAM=max(t_PHL, t_PHL)
.measure tran javg AVG I(vdd) FROM=0ns TO=16ns
.measure tran javg AVG I(vdd) PROPER FROM=0ns TO=16ns
.measure tran energy PARAM='abs(pd*16ns)'
```

HSpice Simulation Waveform



Abstract View



OAI22

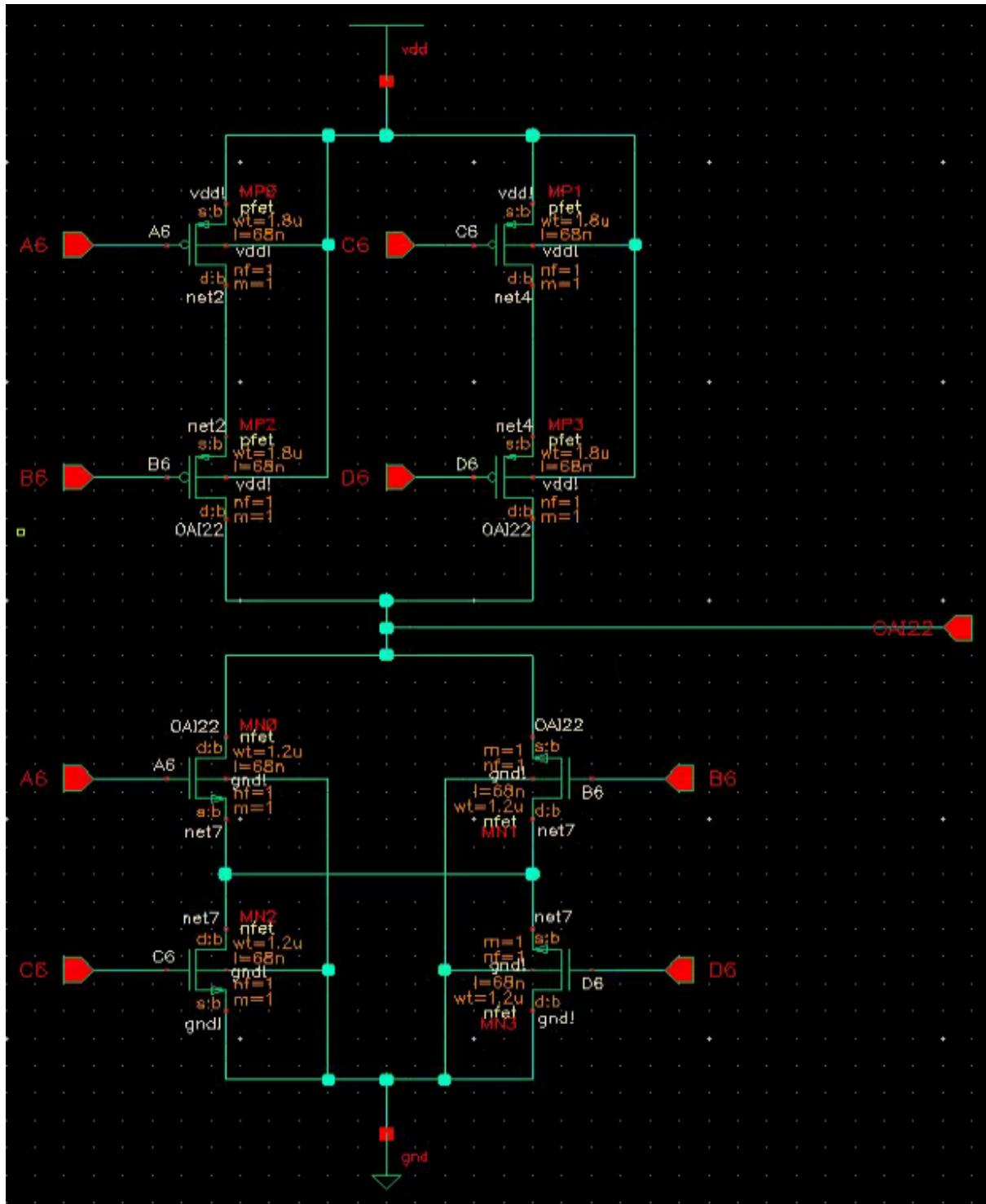
Function

$$\text{OUT} = \text{NOT}((A|B) \& (C|D))$$

Truth Table

INPUT (A6)	INPUT (B6)	INPUT (C6)	INPUT (D6)	OUTPUT (OAI22)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Schematic

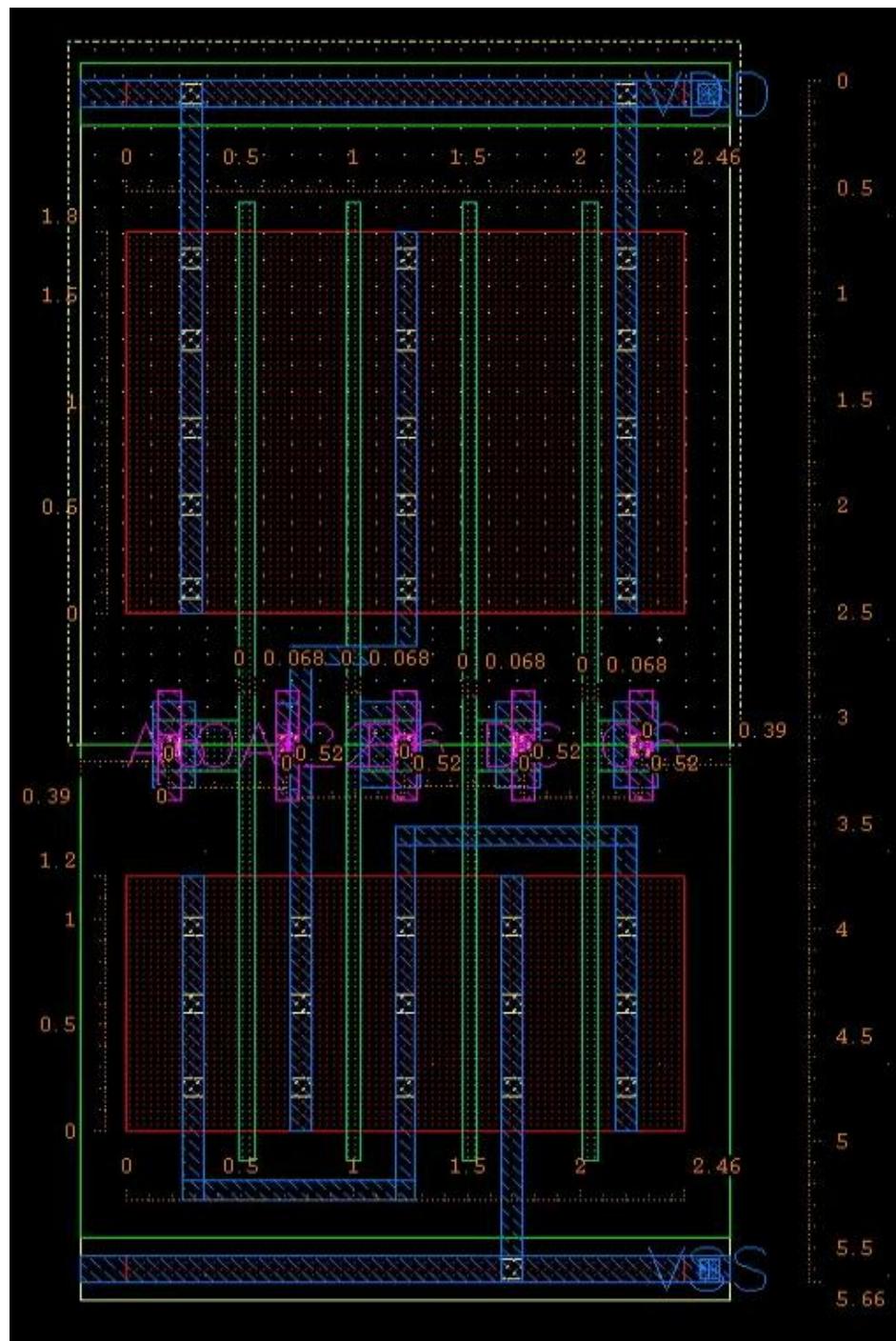


Layout

Cell Height = 5.660 um

Cell Width = 2.460 um

Total Cell Area = 13.9236 um²



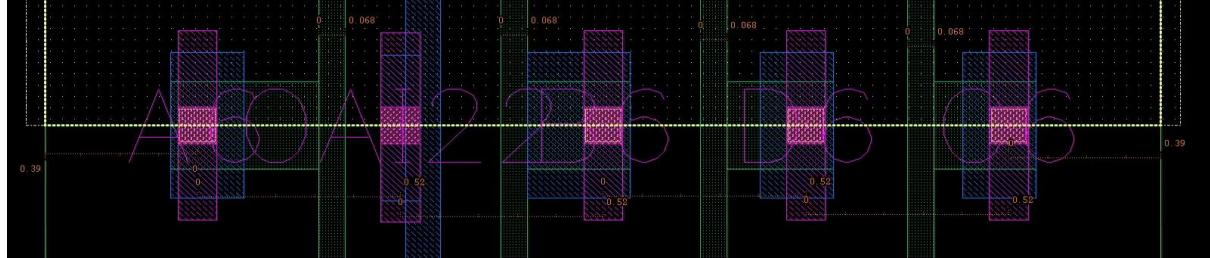
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

Offset (right side) = 0.39 um



DRC Result

Calibre - RVE v2024.4.12.9 : oai22.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All No Results Found

Check / Cell

- ✓ Check_GRSZ
- ✓ Check_GRF4
- ✓ Check_GRB_BF01
- ✓ Check_GRSB_BF01
- ✓ Check_GRB_BF02
- ✓ Check_GRB_BF03
- ✓ Check_GRB_BF04
- ✓ Check_GRB_BF05
- ✓ Check_GRB_BH01
- ✓ Check_GRB_BH02
- ✓ Check_GRSB_BH02
- ✓ Check_GRB_BH03
- ✓ Check_GRB_BH04
- ✓ Check_GRB_BH05
- ✓ Check_GRB_DE01
- ✓ Check_GRB_DE02
- ✓ Check_GRB_DE03
- ✓ Check_GRB_DF01
- ✓ Check_GRB_DF02

Run DRC

Show RVE

Calibre Interactive - nmDRC v2024.4.12.9 : /home/010/tfe/dal542146/_oai22_drc/oai22.drc.runset *

File Settings Configurations Help

oai22.drc.summary

```
=====
1 == CALIBRE:DRC-S SUMMARY REPORT
2
3 Execution Date/Time: Wed Nov 5 01:20:59 2025
4 Calibre Version: v2024.4_12.9 Tue Oct 1 20:34:12 PDT 2024
5 Rule File Pathname: Calibre_DRC_rules_
6 Rule File Title: YI-DM90054.09 - YI-R700052.12
7 Output System: GDS
8 Layout Path(s): oai22.calibre.db
9 Layout Primary Cells: oai22
10 Layout Directory: /home/010/tfe/dal542146/cad/gf65/tmc65_stdcell_lib/oai22/
11 User Name: dal542146
12 Maximum Vertices/RuleCheck: 1000
13 Maximum Result Vertices: 1000
14 DB Results Database: oai22.drc.results (ASCII)
15 Layout Depth: ALL
16 Text Depth: PRIMARY
17 Text Report File: oai22.drc.summary (REPLACE)
18 Geometry Flagging: ACUTE = YES SKew = YES ANGLED = NO OFFGRID = YES
19 NonSimple Polygon = YES NonSimple Path = YES
20 Excluded Cells: COMMENT TEXT + RULE FILE INFORMATION
21 CheckText Mapping: MEMORY-BASED
22 Layers: MEMORY-BASED
23 Keep Empty Checks: YES
24 =====
25 ===== RUNTIME WARNINGS =====
26
27 Cell name FILLDGCAPTE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
28 Cell name FILLDGCAPTE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
29 Cell name FILLDGCAPTE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
30 Cell name FILLDGCAPTE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
31 Cell name FILLDGCAPTE12_A12TR for LAYOUT TEXT object WAIVE_ARM_GRB_BH01 is not defined.
```

Calibre Run Completed Successfully - Results are Valid

LVS Result

PEX Result

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51470	Warning	Please increase descriptors limit for best performance (8192)
53559	Warning	Please increase descriptors limit for best performance (8192)
54867	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

PEX Generated Netlist

```
* File: oai22.pex.sp
* Created: Wed Nov 5 21:32:25 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "oai22.pex.sp.pex"
.subckt oai22 OAI22 GND! VDD! A6 B6 D6 C6
*
* C6 C6
* D6 D6
* B6 B6
* A6 A6
* VDD VDD
* VSS VSS
* OAI22 OAI22
XDO_noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=9.8272e-12
+ PERIM=1.256e-05
XMMN0 N OAI22_MMN0_d N_A6_MMN0_g N_NET7_MMN0_s N_GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.4e-13 AS=6e-13 PD=1.6e-06 PS=3.4e-06 NRD=0.166667
+ NRS=0.170833 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5e-07
+ SB=1.892e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN1 N NET7_MMN1_d N_B6_MMN1_g N_OAI22_MMN0_d N_GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.664e-13 AS=2.4e-13 PD=1.644e-06 PS=1.6e-06
+ NRD=0.163333 NRS=0.166667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=9.68e-07 SB=1.424e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN3 N GND! MMN3_d N_D6_MMN3_g N_NET7_MMN1_d N_GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.772e-13 AS=2.664e-13 PD=1.662e-06 PS=1.644e-06
+ NRD=0.125 NRS=0.206667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=1.48e-06 SD=9.12e-13 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN2 N NET7_MMN2_d N_C6_MMN2_g N_GND! MMN3_d N_GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.772e-13 AS=2.664e-13 PD=3.164e-06 PS=1.662e-06
+ NRD=0.104167 NRS=0.26 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=2.01e-06 SB=3.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMP0 NET2_N_A6_MMP0_g N_VDD! MMP0_s N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=3.6e-13 AS=9e-13 PD=2.2e-06 PS=4.6e-06 NRD=0.111111 NRS=0.116111
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5e-07 SB=1.892e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.0224e-13
+ PANW8=5.28e-14 PANW9=5.44e-14 PANW10=8.16e-14
XMMP2_N_OAI22_MMP2_d N_B6_MMP2_g NET2_N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=3.996e-13 AS=3.6e-13 PD=2.244e-06 PS=2.2e-06 NRD=0.111111
+ NRS=0.111111 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=9.68e-07
+ SB=1.424e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=1.768e-13 PANW10=2.04e-13
XMMP3_N_OAI22_MMP2_d N_D6_MMP3_g NET4_N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=3.996e-13 AS=4.158e-13 PD=2.244e-06 PS=2.262e-06 NRD=0.135556
+ NRS=0.128333 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.48e-06
+ SB=9.12e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=1.768e-13 PANW10=2.04e-13
XMMP1_NET4_N_C6_MMP1_g N_VDD! MMP1_s N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.8e-06 AD=4.158e-13 AS=6.876e-13 PD=2.262e-06 PS=4.364e-06 NRD=0.128333
```

HSpice Setup File

```
* Example HSPICE Testbench for Extracted OAI22
.include "/proj/cad/library/mosis/GF65_LPe_cmos18lp_e_CDS_oa_d1864_11_20160415/models/YI-SM0080/Hspice/models/design.inc"
.include "oai22.pex.sp"

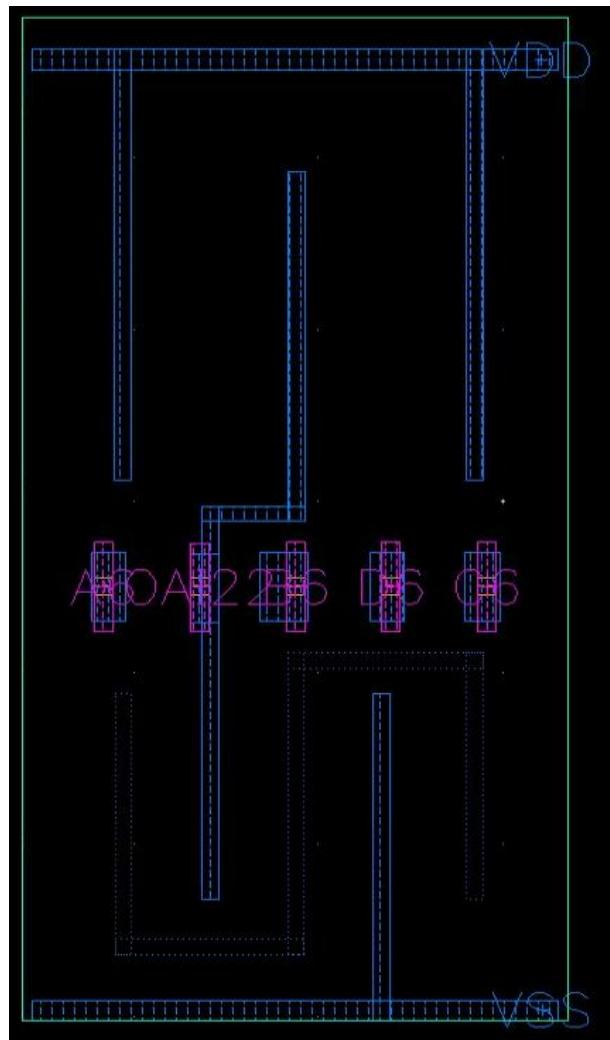
.param VDD=1.2v
vdd VDD! GND! VDD!
*via A6 GND! PML_0ns_0v_Bns_0v_8.04375ns_1.2v_16ns_1.2v_
via B6 GND! PML_0ns_0v_4ns_0v_4.04375ns_1.2v_12ns_1.2v_12.04375ns_0v_16ns_0v_
via D6 GND! PML_0ns_0v_2ns_0v_2.04375ns_1.2v_6ns_1.2v_6.04375ns_0v_18ns_0v_1.04375ns_1.2v_14ns_1.2v_14.04375ns_0v_16ns_0v_
via C6 GND! PML_0ns_0v_1ns_0v_1.04375ns_1.2v_2ns_1.2v_2.04375ns_0v_3ns_0v_3.04375ns_1.2v_4ns_1.2v_4.04375ns_0v_5ns_0v_5.04375ns_1.2v_6ns_1.2v_6.04375ns_0v_7ns_0v_7.04375ns_1.2v_8ns_1.2v_8.04375ns_0v_9ns_0v_9.04375ns_1.2v_10ns_1.2v_10.04375ns_0v_11ns_0v_11.04375ns_1.2v_12ns_1.2v_12.04375ns_0v_13ns_0v_13.04375ns_1.2v_14ns_1.2v_14.04375ns_0v_15ns_0v_15.04375ns_1.2v_16ns_1.2v

COUT OAI22_GND! 45f
Xi OAI22_GND! VDD! A6 B6 D6 C6 oai22
* transient analysis
.tran ips 10ns
.options post nomod
.measure tran t_in_rA WHEN V(A6)=0.6 RISE=1
.measure tran t_out_rA WHEN V(OAI22)=0.6 FALL=1
.measure tran t_in_rB WHEN V(B6)=0.6 RISE=1
.measure tran t_in_rB WHEN V(B6)=0.6 FALL=1
.measure tran t_out_r WHEN V(OAI22)=0.6 RISE=1
.measure tran tPLH PARAM='t_out_r - t_in_rA'
.measure tran tPHL PARAM='t_in_rB - t_out_r'
.measure tran tdiff PARAM='tPLH - tPHL'
.measure tran delay PARAM='max(tPLH, tPHL)'
.measure tran avg II(vdd) FROM=0ns TO=10ns
.measure tran pd AVG power FROM=0ns TO=10ns
.measure tran energy PARAM='abs(pd@10ns)'
```

HSpice Simulation Waveform



Abstract View



OAI21

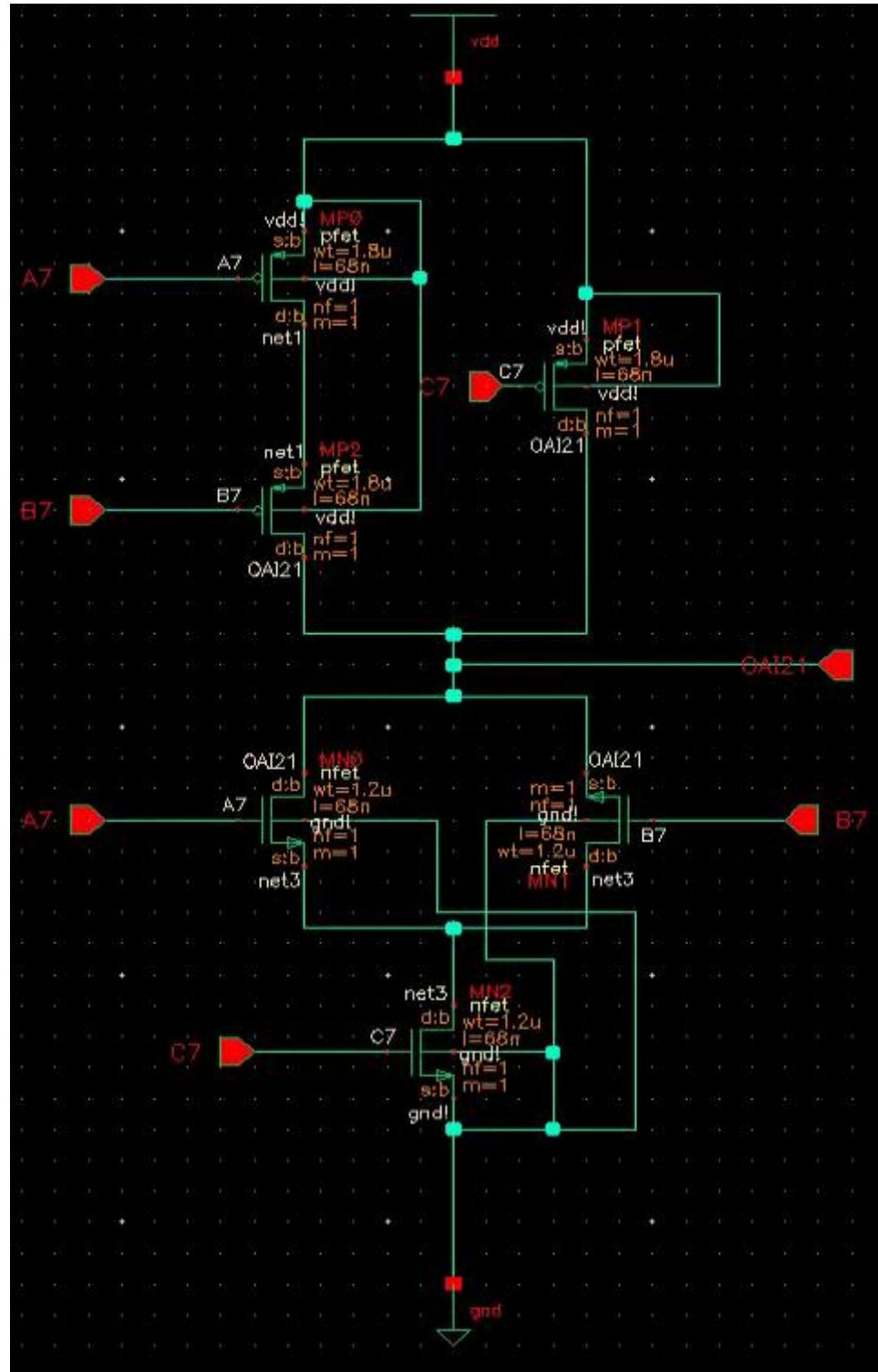
Function

$$\text{OUT} = \text{NOT}((A \mid B) \ \& \ (C))$$

Truth Table

INPUT (A7)	INPUT (B7)	INPUT (C7)	OUTPUT (OAI21)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Schematic

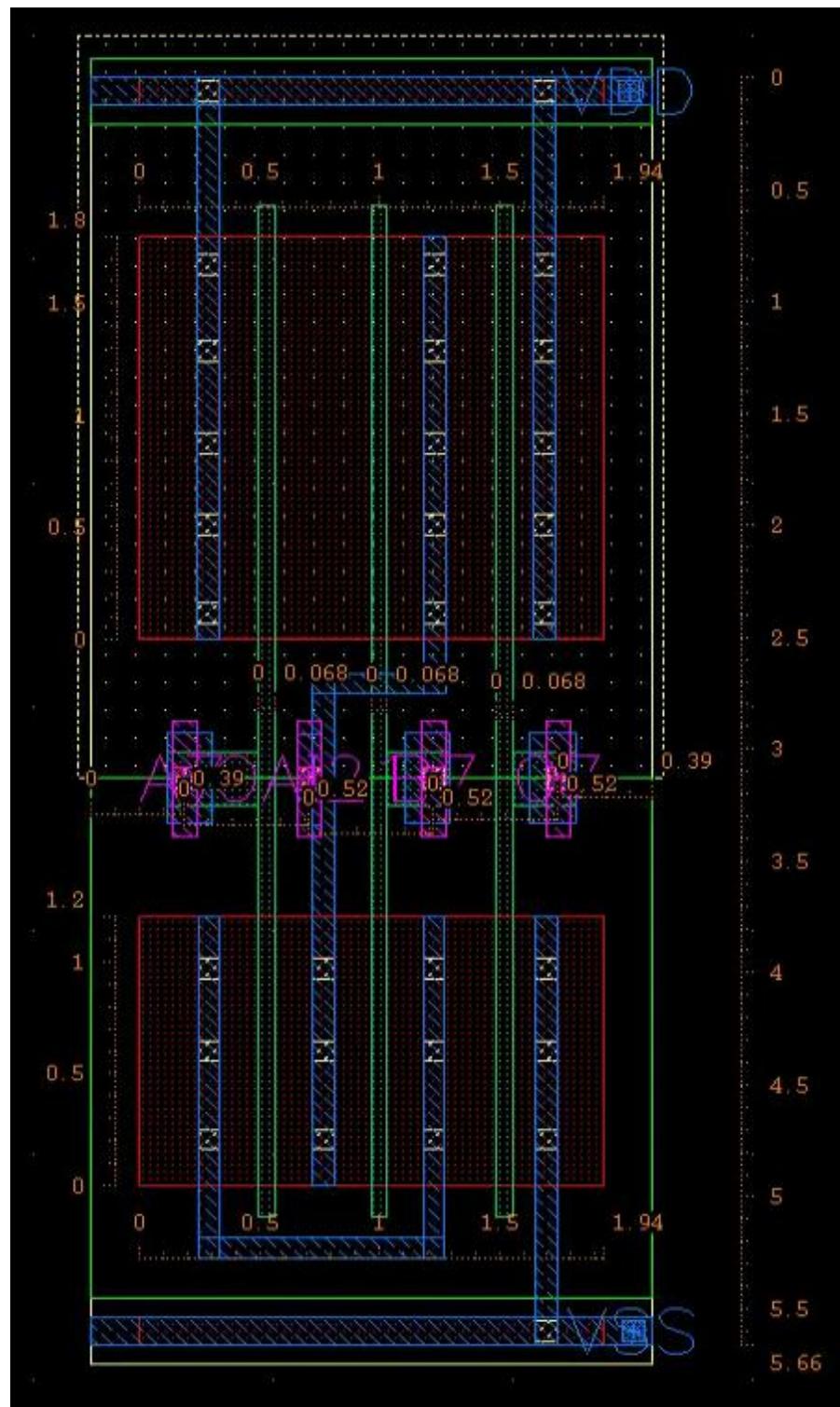


Layout

Cell Height = 5.660 um

Cell Width = 1.940 um

Total Cell Area = 10.9804 um²



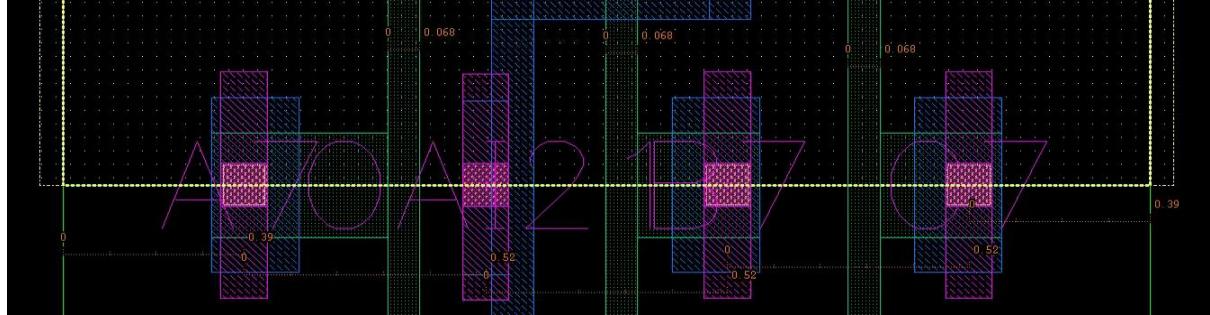
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

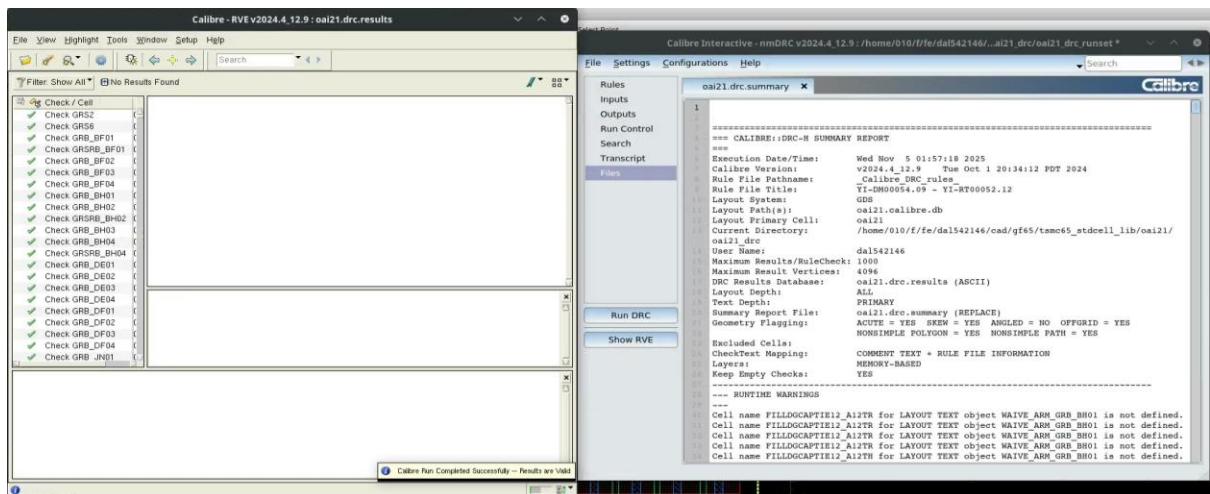
Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

Offset (right side) = 0.39 um



DRC Result



LVS Result

Calibre - RVE v2024.4_12.9 : svdb oai21

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
oai21	oai21	6L, 6S	3L, 3S	6L, 6S

Cell oai21 Summary (Clean)

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	8	8	
Instances:	3	3	RN (4 pins) RP (4 pins)
Total Inst:	6	6	

REPORT FILE NAME: oai21.lvs.report
LAYOUT NAME: oai21.ap ('oai21')
SOURCE NAME: oai21.sch ('oai21')
RULE FILE: _Calibre_LVS.rules
CREATION TIME: Wed Nov 5 01:58:24 2025
CURRENT DIRECTORY: /home/010/f/fe/dal542146/cad/gf65/tmc65_stdcell/lib/oai21/
USER NAME: dal542146
CALIBRE VERSION: v2024.4_12.9 Tue Oct 1 20:34:12 PDT 2024

OVERALL COMPARISON RESULTS

PEX Result

Calibre Interactive - PEX v2024.4_12.9 : /home/010/f/fe/dal542146/...ai21_lvs/oai21_pex_runset *

Transcript

```

total nets = 8
top-level nets = 8
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

=====
CALIBRE xRC WARNING / ERROR Summary
=====
xRC Warnings = 1
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Wed Nov 5 02:00:01 2025
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 50/54/638 MALLOC = 378/378/684 ELAPSED

*** xRC run finished with exit code 0 ***

```

0 Errors, 4 Warnings, 1 Info

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (8192)
51468	Warning	Please increase descriptors limit for best performance (8192)
53557	Warning	Please increase descriptors limit for best performance (8192)
54865	Warning	No ground net name defined in PEX NETLIST statement and "0" will be used in the...

PEX Generated Netlist

```

* File: oai21.pex.sp
* Created: Wed Nov  5 21:41:44 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
*.include "oai21.pex.sp.pex"
.subckt oai21  OAI21 GND! VDD! A7 B7 C7
*
* C7    C7
* B7    B7
* A7    A7
* VDD  VDD
* VSS  VSS
* OAI21 OAI21
XD0_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=8.1008e-12
+ PERIM=1.152e-05
XMMN0 N_OAI21 MMN0 d N A7 MMN0_g N NET3 MMN0_s N GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.4e-13 AS=6e-13 PD=1.6e-06 PS=3.4e-06 NRD=0.166667
+ NRS=0.170833 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5e-07
+ SB=1.372e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN1 N_NET3 MMN1_d N B7 MMN1_g N_OAI21 MMN0_d N_GND! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.724e-13 AS=2.4e-13 PD=1.654e-06 PS=1.e-06
+ NRD=0.163333 NRS=0.166667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=9.68e-07 SB=9.04e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMN2 N_NET3 MMN1_d N_C7 MMN2_g N_GND! MMN2_s N_VDD! D0_noxref_pos NFET
+ L=6.8e-08 W=1.2e-06 AD=2.724e-13 AS=4.584e-13 PD=1.654e-06 PS=3.164e-06
+ NRD=0.215 NRS=0.116667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=1.49e-06 SB=3.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMP0 NET1_N_A7 MMP0_g N_VDD! MMP0_s N_GND! D0_noxref_neg PFET L=6.8e-08
+ W=1.e-01 AD=3.6e-13 AS=9e-13 PD=2.2e-06 PS=4.e-06 NRD=0.111111 NRS=0.111111
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5e-07 SB=1.372e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.0224e-13
+ PANW8=5.28e-14 PANW9=5.44e-14 PANW10=2.04e-13
XMMP2 N_OAI21 MMP2_d N_B7 MMP2_g NET1_N_VDD! D0_noxref_neg PFET L=6.8e-08
+ W=1.e-06 AD=4.086e-13 AS=3.6e-13 PD=2.254e-06 PS=2.2e-06 NRD=0.111111
+ NRS=0.111111 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=9.68e-07
+ SB=9.04e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=2.992e-13 PANW10=8.16e-14
XMMP1 N_OAI21 MMP2_d_N_C7 MMP1_g_N_VDD! MMP1_s_N_GND! D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.086e-13 AS=6.876e-13 PD=2.254e-06 PS=4.364e-06
+ NRD=0.141111 NRS=0.0733333 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.49e-06 SB=3.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.3464e-13 PANW8=2.04e-14 PANW9=5.44e-14 PANW10=2.04e-13
*
*.include "oai21.pex.sp.OAI21.pxi"
*
.ends
*
*

```

HSpice Setup File

```

Open ▾  ↗
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe.CDS oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "oai21.pex.sp" $ .subckt oai21  OAI21 GND! VDD! A7 B7 C7

.option post runlvl=5

$===== DUT (pin order EXACTLY as PEX) =====
$ OAI21 logic: Y = ( (A + B) * C )
X1 OUT GND! VDD! INA INB INC oai21

$===== Supplies =====
vdd VDD! GND! 1.2V

$===== Stimulus (10-90% = 35 ps ~ 0-100% = 43.75 ps) =====
$ Visit all 8 input combinations in 8 ns (Gray-like counting):
$ A toggles at 4 ns, B at 2 ns, C at 1 ns
vinA INA GND! PWL( 0ns 0v 4.04375ns 1.2v 8ns 1.2v )
vinB INB GND! PWL( 0ns 0v 2ns 0v 2.04375ns 1.2v 4ns 1.2v 4.04375ns 0v 6ns 0v 6.04375ns 1.2v 8ns 1.2v )
vinC INC GND! PWL( 0ns 0v 1ns 0v 1.04375ns 1.2v 2ns 1.2v 2.04375ns 0v 3ns 0v 3.04375ns 1.2v
+ 4ns 1.2v 4.04375ns 0v 5ns 0v 5.04375ns 1.2v 6ns 1.2v 6.04375ns 0v
+ 7ns 0v 7.04375ns 1.2v 8ns 1.2v )

$===== Load =====
COUT OUT GND! 45f

$===== Analysis =====
.tr 100ps 8ns

$===== Measurements (VDD/2 = 0.6 V) =====
$ Representative delays (referenced to A's edges; add B/C-based ones if needed)
.measure tran t_in_rA WHEN v(INA)=0.6 RISE=1
.measure tran t_out_f WHEN v(OUT)=0.6 FALL=1
.measure tran tPHL PARAM='t_out_f - t_in_rA'

.measure tran t_in_fa WHEN v(INA)=0.6 FALL=1
.measure tran t_out_r WHEN v(OUT)=0.6 RISE=1
.measure tran tPLH PARAM='t_out_r - t_in_fa'

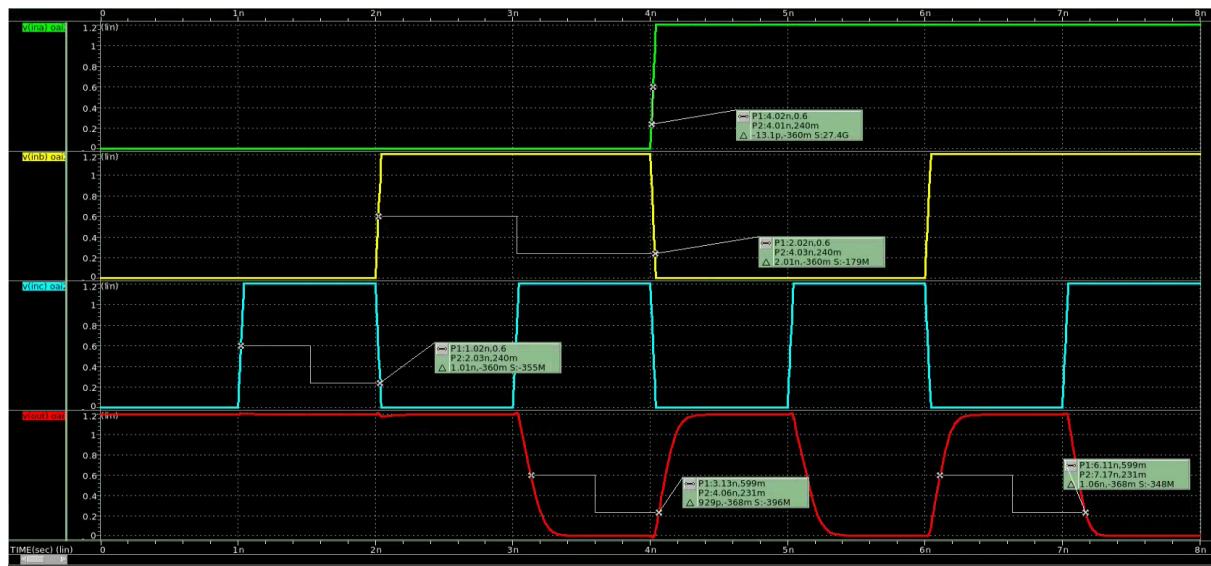
.measure tavg PARAM=(tPHL + tPLH)/2'
.measure tdiff PARAM=abs(tPHL - tPLH)'
.measure delay PARAM='max(tPHL, tPLH)'

$ Power around a representative 1 ns switching window
.measure tran iavg AVG I(vdd) FROM=4ns TO=5ns
.measure tran energy PARAM='1.2*iavg*1ns'
.measure tran edp PARAM='abs(delay*energy)'

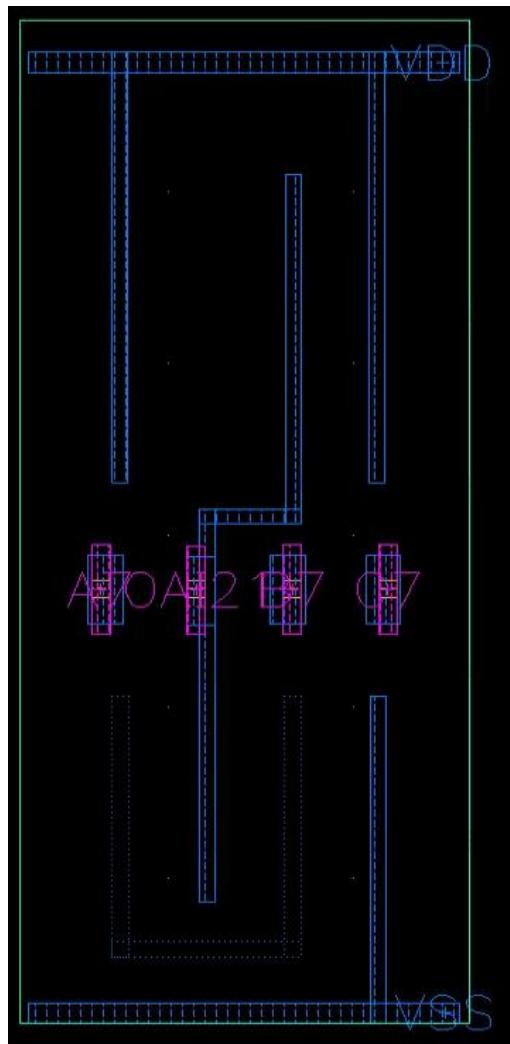
.end

```

HSpice Simulation Waveform



Abstract View



NAND 3

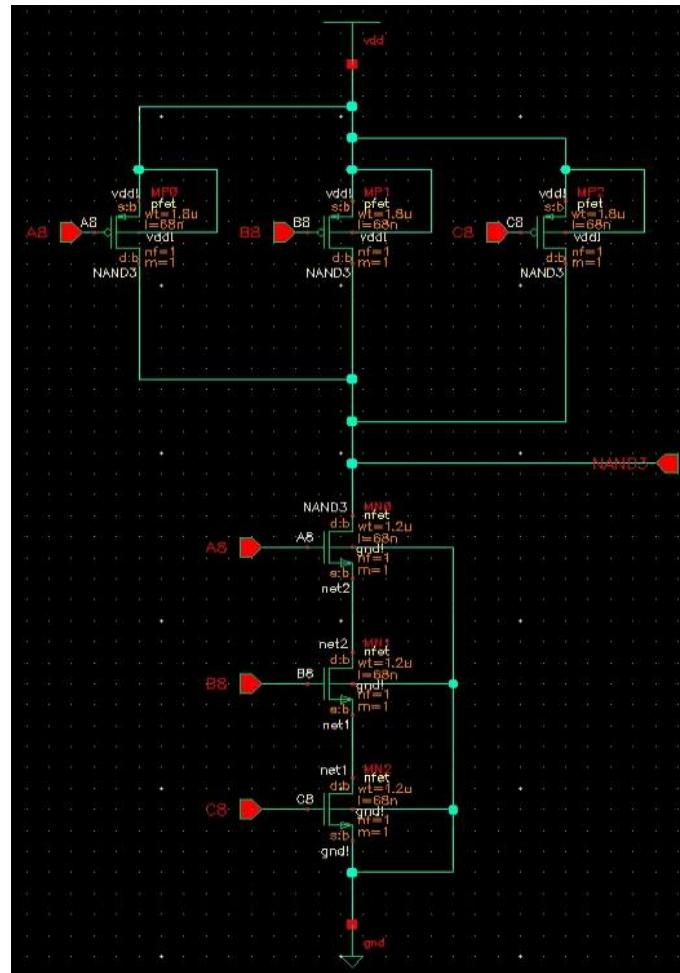
Function

$$\text{OUT} = (\text{NOT}(A \& B \& C))$$

Truth Table

INPUT (A8)	INPUT (B8)	INPUT (C8)	OUTPUT (NAND3)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Schematic

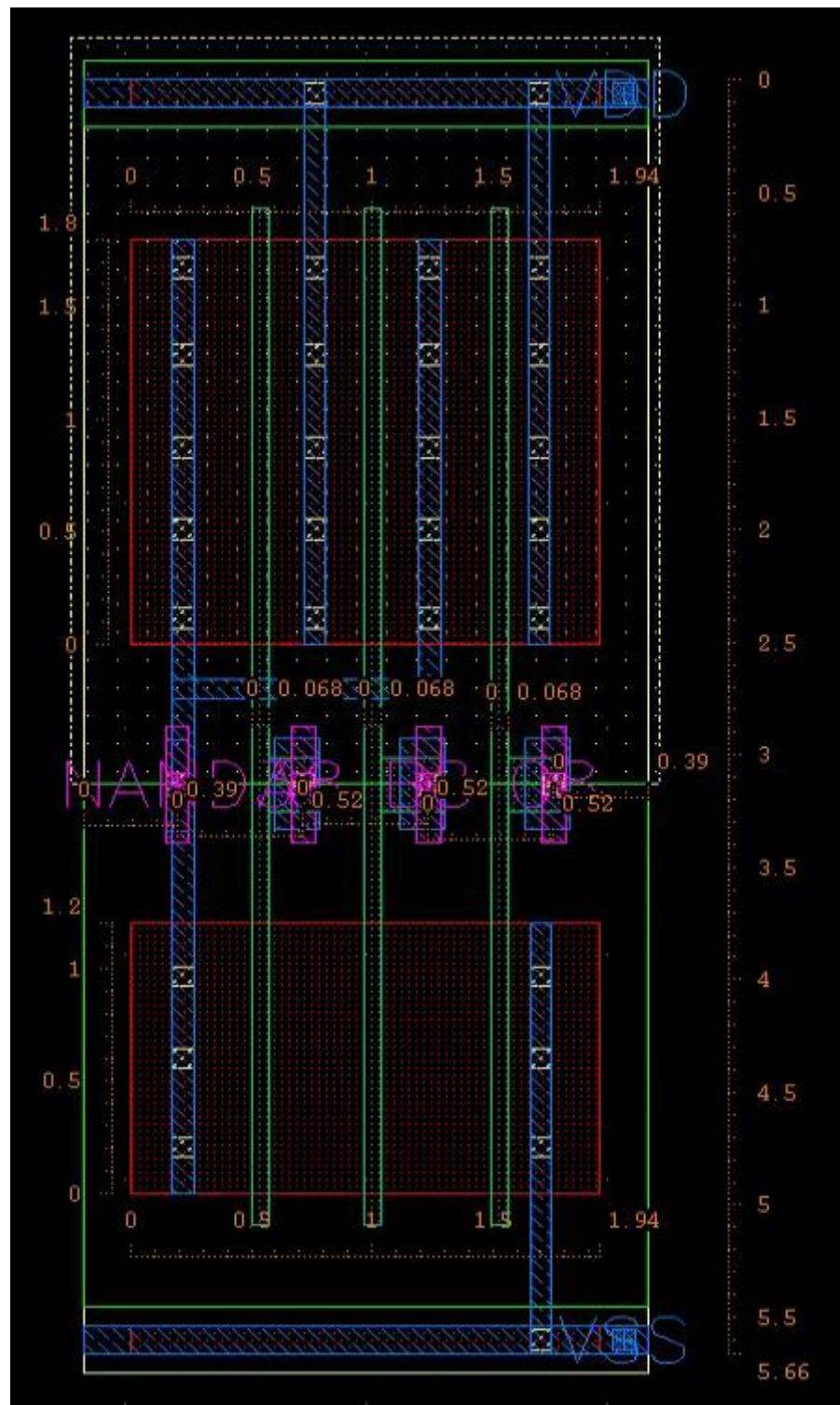


Layout

Cell Height = 5.660 um

Cell Width = 1.940 um

Total Cell Area = 10.9804 um²



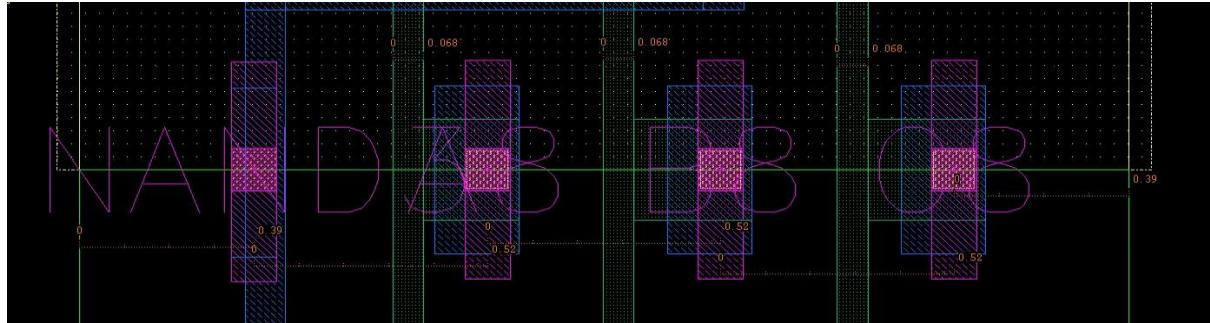
Offset, Pin Pitch and Channel Length

Channel Length = 0.068 um

Pin Pitch = 0.52 um

Offset (left side) = 0.39 um

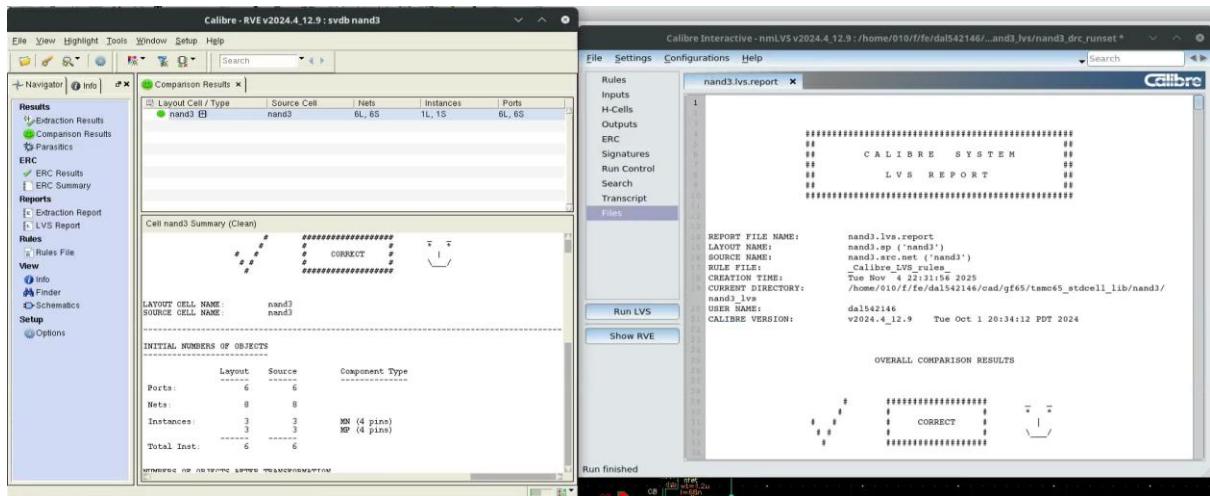
Offset (right side) = 0.39 um



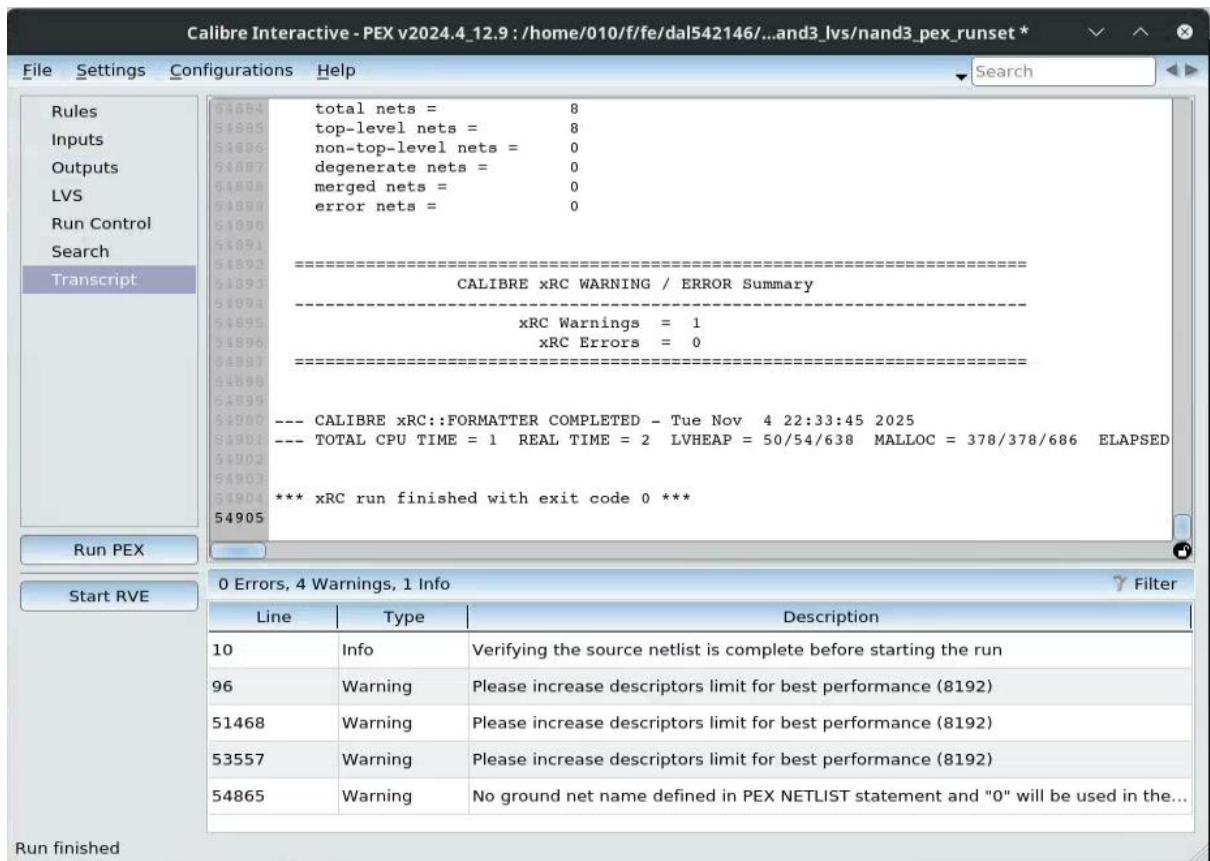
DRC Result

```
== CALIBRE:DRC-II SUMMARY REPORT
Tue Nov  4 22:13:05 2023
v2024.4.12.9 Tue Oct 1 20:34:12 PDT 2024
Calibre Version:          v2024.4.12.9
Rule File Pathname:       Calibre_DRC_rules_
Rule File Title:         YI-RM00054.09 - YI-RM00052.12
Run Type:                GDS
Layout Path(s):          nand3.calibre.db
Layout Primary Cell:    nand3
Layout Secondary Directory: /home/010/t/fe/dal542146/cad/gf65/tmc65_stdcell_lib/nand3/
User Name:               dal542146
Maximum Results/RuleCheck: 10000
Maximum Vertices:        10000
DBS Results Database(s): nand3.drc.results (ASCII)
DBS Results Database(s): nand3.drc.results (ASCII)
Layout Depth:             ALL
Text Depth:               PRIMARY
Report File:              nand3.drc.summary (REPLACE)
Geometry Flagging:        ACUTE = YES SKew = YES ANGLED = NO OFFGRID = YES
                           NONSIMPLE POLYGON = YES NONSIMPLE PATH = YES
Excluded Cells:          None
CheckText Mapping:        COMMENT TEXT + RULE FILE INFORMATION
Layers:                   MEMORY-BASED
Keep Empty Checks:        YES
--- RUNTIME WARNINGS
1 Cell name FILLOOCAPTEI2_A1TR for LAYOUT TEXT object WAIVE_ANH_GRB_BH01 is not defined.
2 Cell name FILLOOCAPTEI2_A1TR for LAYOUT TEXT object WAIVE_ANH_GRB_BH01 is not defined.
3 Cell name FILLOOCAPTEI2_A1TR for LAYOUT TEXT object WAIVE_ANH_GRB_BH01 is not defined.
4 Cell name FILLOOCAPTEI2_A1TR for LAYOUT TEXT object WAIVE_ANH_GRB_BH01 is not defined.
5 Cell name FILLOOCAPTEI2_A1TR for LAYOUT TEXT object WAIVE_ANH_GRB_BH01 is not defined.
```

LVS Result



PEX Result



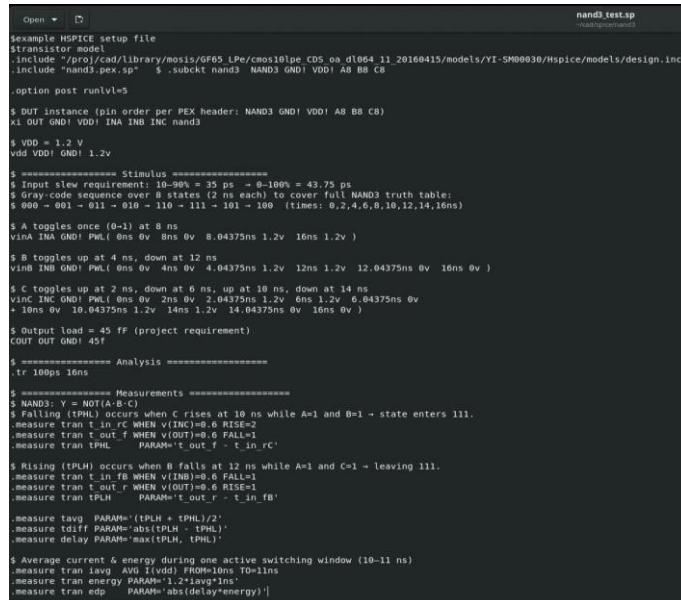
PEX Generated Netlist

```

* File: nand3.pex.sp
* Created: Wed Nov 5 21:48:04 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "nand3.pex.sp.pex"
.subckt nand3 NAND3 GND! VDD! A8 B8 C8
*
* C8     C8
* B8     B8
* A8     A8
* VDD   VDD
* VSS   VSS
* NAND3 NAND3
X00_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=8.1008e-12
+ PERIM=1.152e-05
XMMN0_N_NAND3_MMN0_d_N_A8_MMN0_g NET2_N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=6e-13 AS=2.4e-13 PD=3.4e-06 PS=1.6e-06 NRD=0.2375 NRS=0.166667
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5e-07 SB=1.372e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14 PANW8=1.36e-14
+ PANW9=2.72e-14 PANW10=2.856e-14
XMMN1_NET2_N_B8_MMN1_g NET1_N_GND!_D0_noxref_pos NFET L=6.8e-08 W=1.2e-06
+ AD=2.4e-13 AS=2.724e-13 PD=1.6e-06 PS=1.654e-06 NRD=0.166667 NRS=0.189167 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=9.68e-07 SB=9.04e-07 SD=0 PANW1=0
+ PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.224e-14 PANW8=1.36e-14
+ PANW9=2.72e-14 PANW10=2.856e-14
XMMN2_NET1_N_C8_MMN2_g_N_GND!_MMN2_s_N_GND!_D0_noxref_pos NFET L=6.8e-08
+ W=1.2e-06 AD=2.724e-13 AS=4.584e-13 PD=1.654e-06 PS=3.164e-06 NRD=0.189167
+ NRS=0.116667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.49e-06
+ SB=3.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=1.36e-14 PANW9=2.72e-14 PANW10=2.856e-14
XMMP0_N_NAND3_MMPO_d_N_A8_MMPO_g_N_VDD!_MMPO_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=9e-13 AS=3.6e-13 PD=4.6e-06 PS=2.2e-06 NRD=0.158333
+ NRS=0.107222 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5e-07
+ SB=1.372e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.0224e-13 PANW8=5.28e-14 PANW9=5.44e-14 PANW10=2.04e-13
XMMP1_N_NAND3_MMPI_d_N_B8_MMPI_g_N_VDD!_MMPO_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.086e-13 AS=3.6e-13 PD=2.254e-06 PS=2.2e-06
+ NRD=0.111111 NRS=0.115 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=9.68e-07 SB=9.04e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.224e-14 PANW8=2.04e-14 PANW9=2.992e-13 PANW10=8.16e-14
XMMP2_N_NAND3_MMPI_d_N_C8_MMPI_g_N_VDD!_MMPI_s_N_VDD!_D0_noxref_neg PFET
+ L=6.8e-08 W=1.8e-06 AD=4.086e-13 AS=6.876e-13 PD=2.254e-06 PS=4.364e-06
+ NRD=0.141111 NRS=0.0733333 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.49e-06 SB=3.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.3464e-13 PANW8=2.04e-14 PANW9=5.44e-14 PANW10=2.04e-13
*
.include "nand3.pex.sp.NAND3.pxi"
*
.ends
*
*

```

HSpice Setup File

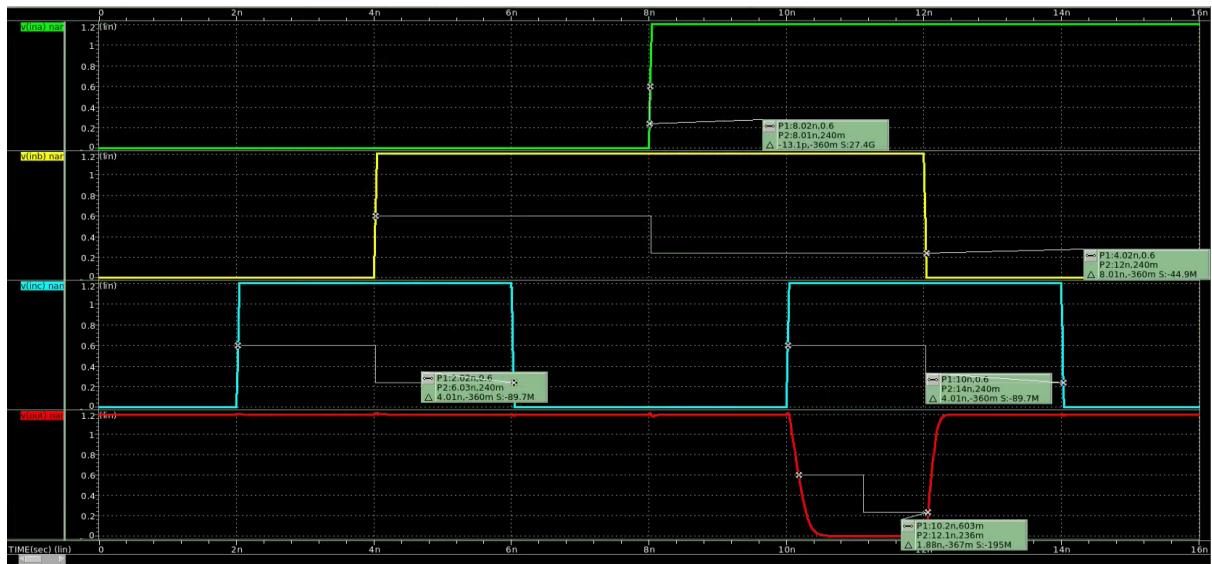


```

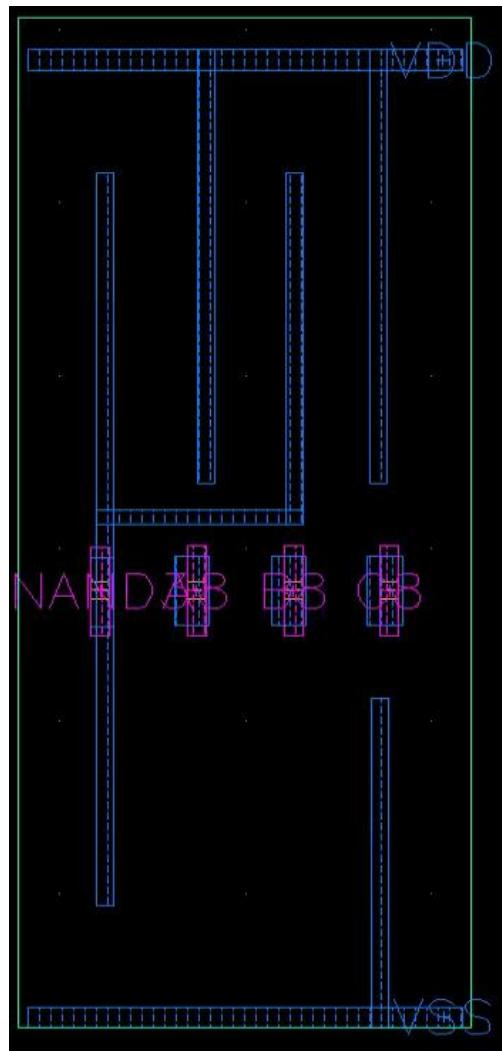
Open -> nand3.test.sp
example HSPICE setup file
transistor model
:include "<pro>/cad/library/mosis/GF65_LPe/cmso10lpe.LDS" on d1064_11_20160415/models/YI-SM0030/Hspice/models/design.lnc"
:include "nand3.pex.sp" $ .subckt nand3 NAND3 GND! VDD! A8 B8 C8
.option post runlvl=5
$ DUT instance (pin order per PEX header: NAND3 GND! VDD! A8 B8 C8)
xi OUT GND! VDD! INA INB INC nand3
$ VDD = 1.2 V
vdd VDD! GND! 1.2v
$ ===== Stimulus =====
$ Input Step requirement: 10-99% == 35 ps == 100% = 43.75 ps
$ Input-Clock setup requirement: 10 ns (10 ns each) to cover full NAND3 truth table:
$ 000 = 001 - 011 - 010 - 110 - 111 - 101 - 100 (times: 0, 2, 4, 6, 8, 10, 12, 14, 16ns)
$ A toggles once (0-1) at 8 ns
vinA INA GND! PWL(0ns 0v 8ns 0v 0.04375ns 1.2v 16ns 1.2v )
$ B toggles up at 4 ns, down at 12 ns
vinB INB GND! PWL(0ns 0v 4ns 0v 8ns 0v 0.04375ns 1.2v 12ns 1.2v 12ns 0v 16ns 0v )
$ C toggles up at 2 ns, down at 6 ns, up at 10 ns, down at 14 ns
vinc INC GND! PWL(0ns 0v 2ns 0v 6ns 0v 0.04375ns 1.2v 6ns 1.2v 6ns 0v 10ns 0v 10.04375ns 1.2v 14ns 1.2v 14.04375ns 0v 16ns 0v )
$ Output load = 45 fF (project requirement)
COUT OUT GND! 45f
$ ===== Analysis =====
.tr 10bps 16ns
$ ===== Measurements =====
$ NAND3: Y = NOT(A-B-C)
$ Falling (tPHL) occurs when C rises at 10 ns while A=1 and B=1 - state enters 111.
.measure tran t_in_rc WHEN v(INC)=0.6 RISE=2
.measure tran t_out_f WHEN v(OUT)=0.6 FALL=1
.measure tran t_in_f WHEN v(INC)=0.6 RISE=1
.measure tran t_out_rc WHEN v(OUT)=0.6 RISE=1
.measure tPHL PARAM=abs(tPLH - t_in_rc)
.measure tPLH PARAM=(tPLH + tPHL)/2
.measure tdiff PARAM=abs(tPLH - tPHL)
.measure delay PARAM=max(tPLH, tPHL)
$ Average current & energy during one active switching window (10-11 ns)
.measure tran iavg AVG I(vdd) FROM=10ns TO=11ns
.measure tran energy PARAM=1.2*iavg*1ns
.measure tran edp PARAM=abs(delay*energy)

```

HSpice Simulation Waveform



Abstract View

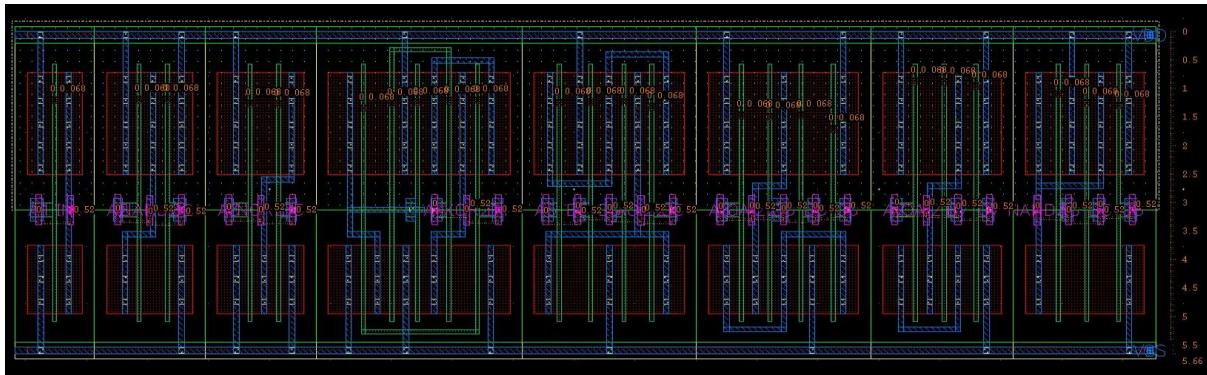


Layout of All Cells Together

Cell Height = 5.660 um

Channel Length = 0.068 um

Pin Pitch = 0.52 um



DRC Result

Calibre - RVE v2024.4.12.9 : all_cell.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All | No Results Found

Rules

- Check_GRS*
- Check_GRS*
- Check_GRS*
- Check_GRS_BF01
- Check_GRSB_BF01
- Check_GRB_BF02
- Check_GRB_BF02
- Check_GRB_BF04
- Check_GRB_BH01
- Check_GRB_BH02
- Check_GRSB_BH02
- Check_GRB_BH03
- Check_GRB_BH04
- Check_GRB_BH04
- Check_GRB_D001
- Check_GRB_D002
- Check_GRB_D003
- Check_GRB_D003
- Check_GRB_D004
- Check_GRB_D004
- Check_GRB_JN01
- Check_GRB_JN02

Inputs

Outputs

Run Control

Search

Transcript

Files

Run DRC

Show RVE

Calibre Interactive - nmDRC v2024.4.12.9 : /home/010/f/fe/dal542146/ca...ell_drc/all_cell.drc.runset *

File Settings Configurations Help

all_cell.drc.summary

```
RULECHECK GRESD17 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD17b .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD18 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD19a .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD19b .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD19c .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD20 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD21 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD22 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD23 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD24 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD25 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD26 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD27 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD28 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD29 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD30 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD31 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD32 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD33 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD34 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD35 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD36 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD37 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD38 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD39 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD40 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD41 .....
```

```
TOTAL Result Count = 0 (0)
```

```
RULECHECK GRESD42 .....
```

```
TOTAL Result Count = 0 (0)
```

```
-- RULECHECK RESULTS STATISTICS (BY CELL)
```

```
-----
```

```
-- SUMMARY
```

```
-----
```

```
TOTAL CPU Time: 1
```

```
TOTAL REAL Time: 4
```

```
TOTAL Original Layer Geometries: 513 (513)
```

```
TOTAL DRC RuleChecks Executed: 2076
```

```
TOTAL DRC Results Generated: 0 (0)
```