

JEDEC STANDARD

**Low Power Double Data Rate 4
(LPDDR4)**

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LOW POWER DOUBLE DATA RATE 4 (LPDDR4)

(From JEDEC Board Ballot JCB-14-41, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for JEDEC compliant 4 Gb through 32 Gb for x16x2channel SDRAM devices. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR4 standard.

2 Package Ballout & Pin Definition

2.1 Pad Order

Ch. A Top		Ch. B Top	
1	VDD2	41	VDD2
2	VSS	42	CKE_A
3	VDD1	43	CS_A
4	VDD2	44	VSS
5	VSS	45	CA1_A
6	VSSQ	46	CA0_A
7	DQ8_A	47	VDD2
8	VDDQ	48	ODT(ca)_A
9	DQ9_A	49	VSS
10	VSSQ	50	VDD1
11	DQ10_A	51	VSSQ
12	VDDQ	52	DQ7_A
13	DQ11_A	53	VDDQ
14	VSSQ	54	DQ6_A
15	DQS1_t_A	55	VSSQ
16	DQS1_c_A	56	DQ5_A
17	VDDQ	57	VDDQ
18	DMI1_A	58	DQ4_A
19	VSSQ	59	VSSQ
20	DQ12_A	60	DMI0_A
21	VDDQ	61	VDDQ
22	DQ13_A	62	DQS0_c_A
23	VSSQ	63	DQS0_t_A
24	DQ14_A	64	VSSQ
25	VDDQ	65	DQ3_A
26	DQ15_A	66	VDDQ
27	VSSQ	67	DQ2_A
28	ZQ	68	VSSQ
29	VDDQ	69	DQ1_A
30	VDD2	70	VDDQ
31	VDD1	71	DQ0_A
32	VSS	72	VSSQ
33	CA5_A	73	VSS
34	CA4_A	74	VDD2
35	VDD2	75	VDD1
36	CA3_A	76	VSS
37	CA2_A	77	VDD2
38	VSS		Ch. A Bottom
39	CK_c_A		
40	CK_t_A		
			Ch. B Bottom
			141 VDD2
			142 CKE_B
			143 CS_B
			144 VSS
			145 CA1_B
			146 CA0_B
			147 VDD2
			148 ODT(ca)_B
			149 VSS
			150 VDD1
			151 VSSQ
			152 DQ7_B
			153 VDDQ
			154 DQ6_B
			155 VSSQ
			156 DQ5_B
			157 VDDQ
			158 DQ4_B
			159 VSSQ
			160 DMI0_B
			161 VDDQ
			162 DQS0_c_B
			163 DQS0_t_B
			164 VSSQ
			165 DQ3_B
			166 VDDQ
			167 DQ2_B
			168 VSSQ
			169 DQ1_B
			170 VDDQ
			171 DQ0_B
			172 VSSQ
			173 VSS
			174 VDD2
			175 VDD1
			176 VSS
			177 VDD2
			178 Ch. B Bottom

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

2.2.2 200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_T_B	CK_C_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_N	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_C_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_T_B	VSS	VDDQ			VDDQ	VSS	DQS1_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

	0.65mm Pitch				
N	VDD2	VSS	VDD2	VSS	CS2_B
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2
V	VSS	DQ2_B	DQS0_C_B	DQ5_B	VSS
W	VDDQ	VSS	DQS0_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ
AB	DNU	DNU	VSS	VDD2	VSS
	CKE2_B	VSS	VDD2	VSS	VDD2
	CK_T_B	CK_C_B	VSS	CA5_B	VSS
	VDD2	CA2_B	CA3_B	CA4_B	VDD2
	VSS	VDD1	VSS	RESET_N	VSS
	VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
	VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
	VDDQ	VSS	DQS1_T_B	VSS	VDDQ
	VSS	DQ14_B	DMI1_B	DQ9_B	VSS
	VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
	VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad VSS and VSSQ signals are combined to VSS package balls.

2.3 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to Table 63 — Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V _{DDQ} through a 240Ω ± 1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2}	Supply	Power Supplies: Isolated on the die for improved noise immunity.
V _{SS} , V _{SSQ}	GND	Ground Reference: Power supply ground reference
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets both channels of the die.

3 Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured as 2-channel and 8-bank per channel memory that is up to 16Gb density. The configuration for the device density that is greater than 16Gb is still TBD¹.

These devices contain the following number of bits:

4Gb has 4,294,967,296 bits
6Gb has 6,442,450,944 bits
8Gb has 8,589,934,592 bits
12Gb has 12,884,901,888 bits
16Gb has 17,179,869,184 bits
24Gb has 25,769,803,776 bits
32Gb has 34,359,738,368 bits

LPDDR4 devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information.

Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See Table 63 — Command Truth Table, for details.

These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following provides detailed information covering device initialization, register definition, command description and device operation.

1. As of publication of this document, under discussion by the formulating committee.

3.1 LPDDR4 SDRAM Addressing

Table 2 — LPDDR4 SDRAM Addressing

Memory Density (per Die)	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Memory Density (per channel)	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Configuration	16Mb x 16DQ x 8 banks x 2 channels	24Mb x 16DQ x 8 banks x 2 channels	32Mb x 16DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64Mb x 16DQ x 8 banks x 2 channels	TBD x 16DQ x TBD banks x 2 channels	TBD x 16DQ x TBD banks x 2 channels
Number of Channels (per die)	2	2	2	2	2	2	2
Number of Banks (per channel)	8	8	8	8	8	TBD	TBD
Array Pre-Fetch (bits, per channel)	256	256	256	256	256	256	256
Number of Rows (per channel)	16,384	24,576	32,768	49,152	65,536	TBD	TBD
Number of Columns (fetch boundaries)	64	64	64	64	64	TBD	TBD
Page Size (Bytes)	2048	2048	2048	2048	2048	TBD	TBD
Channel Density (Bits per channel)	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total Density (Bits per die)	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA2	TBD	TBD				
x16	Row Addresses	R0 - R13 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	TBD	TBD
	Column Addresses	C0 - C9	C0 - C9	C0 - C9	C0 - C9	TBD	TBD
Burst Starting Address Boundary	64 - bit	64 - bit					

NOTE 1 The lower two column addresses (C0 - C1) are assumed to be "zero" and are not transmitted on the CA bus.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.

NOTE 3 For non - binary memory densities,only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 TBD, as of publication of this document, under discussion by the formulating committee.

3.2 Simplified LPDDR4 State Diagram

LPDDR4-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see clause 4, Command Definition and Timing Diagram.

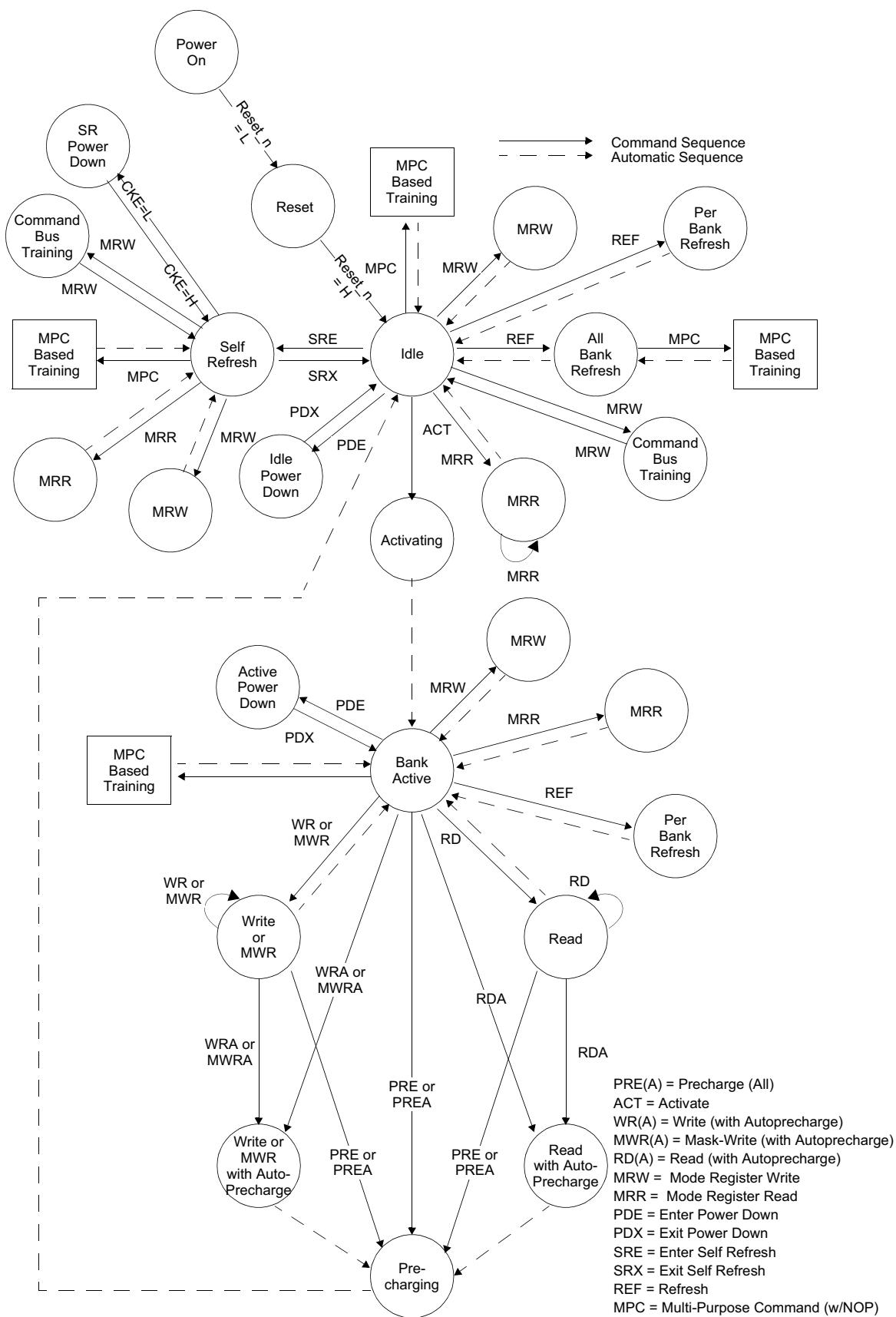
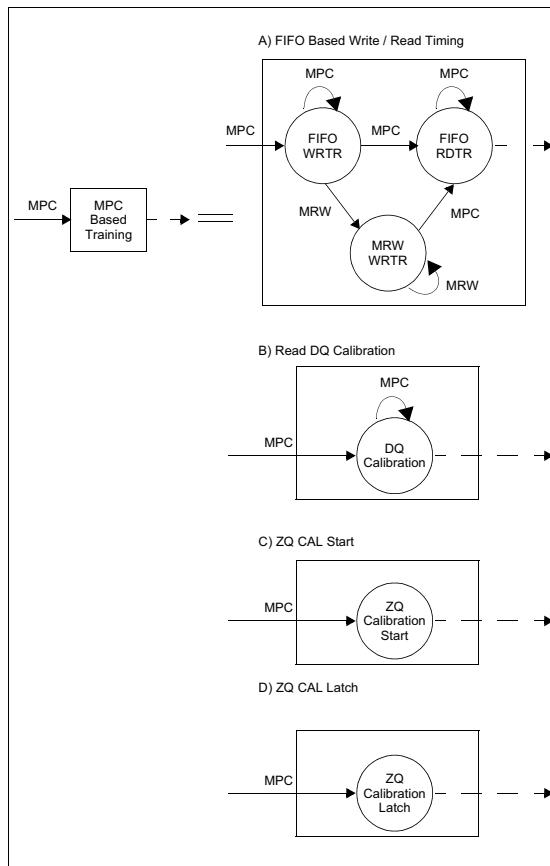


Figure 1 — LPDDR4: Simplified Bus Interface State Diagram-1



NOTE 1 From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See 4.13, on Self-Refresh for more information.

NOTE 2 In IDLE state, all banks are pre-charged.

NOTE 3 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See 4.17, on Mode Register Write (MRW) for more information.

NOTE 4 In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See 4.28, Multi-Purpose Command (MPC) for more information.

NOTE 5 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

NOTE 6 States that have an “automatic return” and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).

NOTE 7 The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

Figure 2 — LPDDR4: Simplified Bus Interface State Diagram-2

3.3 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 3.

Table 3 — MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00 _B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0 _B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000 _B	WL = 4
RL	MR2 OP[2:0]	000 _B	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000 _B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00 _B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000 _B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000 _B	DQ ODT is disabled
V _{REF} (CA) Setting	MR12 OP[6]	1 _B	V _{REF} (CA) Range[1] enabled
V _{REF} (CA) Value	MR12 OP[5:0]	001101 _B	Range1 : 27.2% of VDD2
V _{REF} (DQ) Setting	MR14 OP[6]	1 _B	V _{REF} (DQ) Range[1] enabled
V _{REF} (DQ) Value	MR14 OP[5:0]	001101 _B	Range1 : 27.2% of VDDQ

3.3.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 4. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table 4 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

NOTE 1 Ta is the point when any power supply first reaches 300mV.

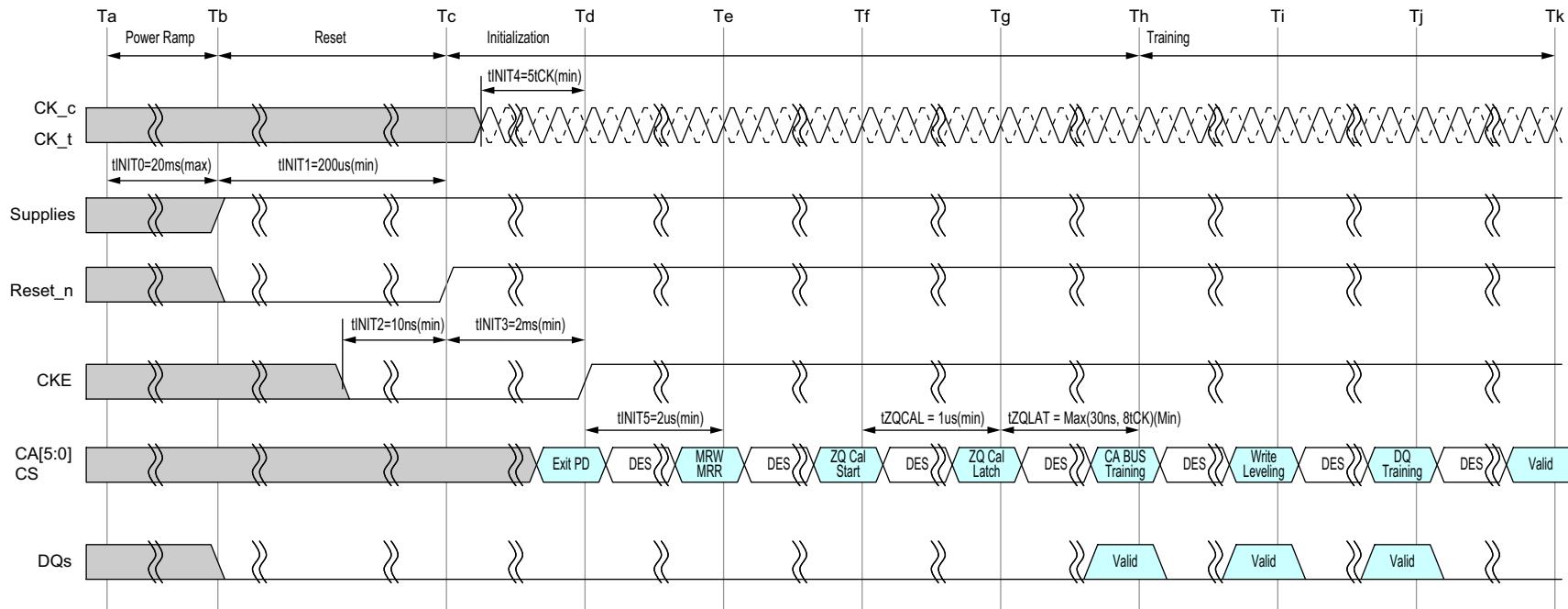
NOTE 2 Voltage ramp conditions in Table 4 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

NOTE 5 The voltage difference between any of Vss and Vssq pins must not exceed 100mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.
3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before RESET_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".



NOTES : 1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in Figure 1 is simplified recommendation and actual training sequence may vary depending on systems.

Figure 3 — Power Ramp and Initialization Sequence

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.
5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.
6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

3.3.1 Voltage Ramp and Device Initialization

7. After tZQLAT is satisfied (Th) the command bus (internal V_{REF}(ca), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and V_{REF}(ca) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

NOTE The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.21, (item 1.), MRW for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See 4.23, Mode Register Write-WR Leveling Mode, for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.
9. After write leveling, the DQ Bus (internal V_{REF}(dq), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust V_{REF}(dq)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and V_{REF}(dq) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.25, DQ Bus Training for detailed DQ Bus Training sequence.
10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 5 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage-ramp time
tINIT1	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE low time before RESET_n high
tINIT3	2	-	ms	Minimum CKE low time after RESET_n high
tINIT4	5	-	tCK	Minimum stable clock before first CKE high
tINIT5	2	-	us	Minimum idle time before first MRW/MRR command
tZQCAL	1	-	us	ZQ calibration time
tZQLAT	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time.
tCKb	Note * ^{1,2}	Note * ^{1,2}	ns	Clock cycle time during boot

NOTE 1 Min tCKb guaranteed by DRAM test is 18ns.

NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below $0.2 \times V_{DD2}$ anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.
2. Repeat steps 4 to 10 in 3.3.1, Voltage Ramp and Device Initialization.

Table 6 — Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low Time for Reset Initialization with stable power

3.3.3 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

Table 7 — Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2} V_{DD2} must be greater than $V_{DDQ} - 200\text{mV}$

The voltage difference between any of V_{SS}, V_{SSQ} pins must not exceed 100mV.

3.3.4 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5V/ μs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 8 — Timing Parameters Power Off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-off ramp item

3.4 Mode Register Definition

Table 9 shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 9 — Mode Register Assignment in LPDDR4 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CATR	RFU	RFU	RZQI		RFU	RFU	Refresh mode
1	RPST		nWR (for AP)		RD-PRE	WR-PRE		BL
2	WR Lev	WLS		WL			RL	
3	DBI-WR	DBI-RD		PDDS		PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort		Refresh Rate	
5				LPDDR4 Manufacturer ID				
6				Revision ID-1				
7				Revision ID-2				
8	IO Width			Density			Type	
9				Vendor Specific Test Register				
10				RFU			ZQ-Reset	
11	RFU		CA ODT		RFU		DQ ODT	
12	RFU	VR-CA			V _{REF} (ca)			
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(dq)			V _{REF} (dq)			
15				Lower-Byte Invert Register for DQ Calibration				
16				PASR Bank Mask				
17				PASR Segment Mask				
18				DQS Oscillator Count - LSB				
19				DQS Oscillator Count - MSB				
20				Upper-Byte Invert Register for DQ Calibration				
21				RFU				
22	RFU		ODTD-CA	ODTE-CS	ODTE-CK		CODT	
23				DQS interval timer run time setting				
24	TRR Mode		TRR Mode BAn		Unlimited MAC		MAC Value	
25				PPR Resource				
26				RFU				
27				RFU				
28				RFU				
29				RFU				
30				RFU				
31				RFU				
32				DQ Calibration Pattern "A" (default = 5AH)				
33				RFU				
34				RFU				
35				RFU				
36				RFU				
37				RFU				
38				RFU				
39				RFU				
40				DQ Calibration Pattern "B" (default = 3CH)				

3.4.1 MR0 Register Information (MA [7:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU	RFU		RZQI		RFU	Refresh mode

Function	Register Type	Operand	Data	Notes
Refresh mode	Read-only	OP[0]	0 _B : Both legacy & modified refresh mode supported 1 _B : Only modified refresh mode supported	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00 _B : RZQ Self-Test Not Supported 01 _B : ZQ pin may connect to V _{SSQ} or float 10 _B : ZQ-pin may short to V _{DDQ} 11 _B : ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V _{SSQ} or float, nor short to V _{DDQ})	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0 _B : CA for this rank is not terminated 1 _B : CA for this rank is terminated	5

NOTE 1 RZQI, if supported, will be set upon the completion of the MRW ZQ Initialization Calibration command.

NOTE 2 If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.

NOTE 4 If ZQ Self-Test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).

NOTE 5 OP[7] is set at power-up, according to the state of the CA-ODT pad on the die AND the state of MR11 OP[7]. If the CAODT pad is tied LOW, then the die will not terminate the CA bus and MR12 OP[7]=0_B, regardless of the state of ODTECA (MR11 OP[7]). If the CA-ODT pad is tied HIGH AND ODTE-CA is enabled (MR11 OP[7]=1_B), then this bit will be set (MR0 OP[7]=1_B) and the die will terminate the CA bus.

3.4.2 MR1 Register Information ($MA[7:0] = 01_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	nWR (for AP)			RD-PRE	WR-PRE		BL

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00 _B : BL=16 Sequential (default) 01 _B : BL=32 Sequential 10 _B : BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1,5,6
WR-PRE (WR Pre-amble Length)		OP[2]	0 _B : Reserved 1 _B : WR Pre-amble = 2*tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0 _B : RD Pre-amble = Static (default) 1 _B : RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Pre-charge commands)		OP[6:4]	000 _B : nWR = 6 (default) 001 _B : nWR = 10 010 _B : nWR = 16 011 _B : nWR = 20 100 _B : nWR = 24 101 _B : nWR = 30 110 _B : nWR = 34 111 _B : nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	0 _B : RD Post-amble = 0.5*tCK (default) 1 _B : RD Post-amble = 1.5*tCK	4,5,6

NOTE 1 Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See Table 63 — Command Truth Table.

NOTE 2 The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. (Ref. See Latency Code Frequency Table for allowable Frequency Ranges for RL/WL/nWR, available in next revision of this document)

NOTE 3 For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble. See 4.4, Read Preamble and Postamble, for a drawing of each type of pre-amble.

NOTE 4 OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 10 — Burst Sequence for READ

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32						
16	SEQ	V	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0	1	0	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1	0	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1	1	0	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	SEQ	0	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17				
		1	0	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

NOTE 1 C0-C1 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 64-bit (4n) boundaries.

NOTE 1 C0-C1 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 64-bit (4n) boundaries.

NOTE 3 C2-C3 shall be set to '0' for all Write operations.

Table 11 — Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32						
16	SEQ	V	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	SEQ	0	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

3.4.3 MR2 Register Information ($MA[7:0] = 02_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Lev	WLS		WL			RL	

Function	Register Type	Operand	Data	Notes
RL (Read latency)		OP[2:0]	RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0 _B) 000 _B : RL=6, nRTP = 8 (Default) 001 _B : RL=10, nRTP = 8 010 _B : RL=14, nRTP = 8 011 _B : RL=20, nRTP = 8 100 _B : RL=24, nRTP = 10 101 _B : RL=28, nRTP = 12 110 _B : RL=32, nRTP = 14 111 _B : RL=36, nRTP = 16 RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1 _B) 000 _B : RL=6, nRTP = 8 001 _B : RL=12, nRTP = 8 010 _B : RL=16, nRTP = 8 011 _B : RL=22, nRTP = 8 100 _B : RL=28, nRTP = 10 101 _B : RL=32, nRTP = 12 110 _B : RL=36, nRTP = 14 111 _B : RL=40, nRTP = 16	1,3,4
WL (Write latency)	Write-only	OP[5:3]	WL Set "A" (MR2 OP[6]=0 _B) 000 _B : WL=4 (Default) 001 _B : WL=6 010 _B : WL=8 011 _B : WL=10 100 _B : WL=12 101 _B : WL=14 110 _B : WL=16 111 _B : WL=18 WL Set "B" (MR2 OP[6]=1 _B) 000 _B : WL=4 001 _B : WL=8 010 _B : WL=12 011 _B : WL=18 100 _B : WL=22 101 _B : WL=26 110 _B : WL=30 111 _B : WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	0 _B : WL Set "A" (default) 1 _B : WL Set "B"	1,3,4
WR LEV (Write Leveling)		OP[7]	0 _B : Disabled (default) 1 _B : Enabled	2

NOTE 1 (Ref. See Latency Code Frequency Table for allowable Frequency Ranges for RL/WL/nWR/nRTP, available in next revision of this document)

NOTE 2 See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP. (The next revision of this document should contain a Table for "Latency Code Frequency")

NOTE 3 After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.

NOTE 4 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.4 MR3 Register Information (MA[7:0] = 03H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	0 _B : V _{DDQ} /2.5 1 _B : V _{DDQ} /3 (default)	1,4
WR PST(WR Post-Amble Length)		OP[1]	0 _B : WR Post-amble = 0.5*tCK (default) 1 _B : WR Post-amble = 1.5*tCK(Vendor specific function)	2,3,5
Post Package Repair Protection		OP[2]	0 _B : PPR protection disabled (default) 1 _B : PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000 _B : RFU 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 (default) 111 _B : Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0 _B : Disabled (default) 1 _B : Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0 _B : Disabled (default) 1 _B : Enabled	2,3

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.

NOTE 5 Refer to the supplier data sheet for vendor specific function. 1.5*tCK apply > 1.6GHz clock.

NOTE 6 If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset.

NOTE 7 MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

3.4.5 MR4 Register Information ($MA[7:0] = 04H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000 _B : SDRAM Low temperature operating limit exceeded 001 _B : 4x refresh 010 _B : 2x refresh 011 _B : 1x refresh (default) 100 _B : 0.5x refresh 101 _B : 0.25x refresh, no derating 110 _B : 0.25x refresh, with derating 111 _B : SDRAM High temperature operating limit exceeded	1,2,3,4 7,8,9
SR Abort (Self Refresh Abort)	Write	OP[3]	0 _B : Disable (default) 1 _B : Enable	9,11
PPRE (Post-package repair entry/exit)	Write	OP[4]	0 _B : Exit PPR mode (default) 1 _B : Enter PPR mode	5,9
Thermal Offset (Vendor Specific Function)	Write	OP[6:5]	00 _B : No offset, 0~5°C gradient (default) 01 _B : 5°C offset, 5~10°C gradient 10 _B : 10°C offset, 10~15°C gradient 11 _B : Reserved	10
TUF (Temperature Update Flag)	Read	OP[7]	0 _B : No change in OP[2:0] since last MR4 read (default) 1 _B : Change in OP[2:0] since last MR4 read	6,7,8

NOTE 1 The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011_B corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1_B, the device temperature is greater than 85 °C.

NOTE 2 At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR4-SDRAM will set OP[2:0]=110_B. See derating timing requirements in 10.3, Table 90.

NOTE 3 DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.

NOTE 4 The device may not operate properly when OP[2:0]=000_B or 111_B.

NOTE 5 Post-package repair can be entered or exited by writing to OP[4].

NOTE 6 When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.

NOTE 7 OP[7]=0 at power-up. OP[2:0] bits are undefined at power-up.

NOTE 8 See the 4.30, Temperature Sensor for information on the recommended frequency of reading MR4.

NOTE 9 OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.

NOTE 10 Refer to the supplier data sheet for vendor specific function.

NOTE 11 Self refresh abort feature is available for higher density devices starting with 12Gb device.

3.4.6 MR5 Register Information (MA[7:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4 Manufacturer ID							

Function	Register Type	Operand	Data	Notes
LPDDR4 Manufacturer ID	Read-only	OP[7:0]	See JEP166, LPDDR4 Manufacturer ID Codes	

3.4.7 MR6 Register Information (MA[7:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000 _B : A-version 00000001 _B : B-version	1

NOTE 1 MR6 is vendor specific.

3.4.8 MR7 Register Information (MA[7:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-2	Read-only	OP[7:0]	00000000 _B : A-version 00000001 _B : B-version	1

NOTE 1 MR7 is vendor specific.

3.4.9 MR8 Register Information (MA[7:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width	Density					Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00 _B : S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000 _B : 4Gb per die (2Gb per channel) 0001 _B : 6Gb per die (3Gb per channel) 0010 _B : 8Gb per die (4Gb per channel) 0011 _B : 12Gb per die (6Gb per channel) 0100 _B : 16Gb per die (8Gb per channel) 0101 _B : 24Gb per die (12Gb per channel) 0110 _B : 32Gb per die (16Gb per channel) All Others: Reserved	
IO Width		OP[7:6]	00 _B : x16 (per channel) All Others: Reserved	

3.4.10 MR9 Register Information (MA[7:0] = 09_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

NOTE 1 Only 00_H should be written to this register.

3.4.11 MR10 Register Information (MA[7:0] = 0A_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ-Reset

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	0 _B : Normal Operation (Default) 1 _B : ZQ Reset	1,2

NOTE 1 See Table 51, ZQCal Timing Parameters for calibration latency and timing.

NOTE 2 If the ZQ-pin is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

3.4.12 MR11 Register Information ($MA[7:0] = 0B_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA ODT			RFU	DQ ODT		

Function	Register Type	Operan d	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)		OP[2:0]	000_B : Disable (Default) 001_B : RZQ/1 010_B : RZQ/2 011_B : RZQ/3 100_B : RZQ/4 101_B : RZQ/5 110_B : RZQ/6 111_B : RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)	Write-only	OP[6:4]	000_B : Disable (Default) 001_B : RZQ/1 010_B : RZQ/2 011_B : RZQ/3 100_B : RZQ/4 101_B : RZQ/5 110_B : RZQ/6 111_B : RFU	1,2,3

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.13 MR12 Register Information (MA[7:0] = 0C_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA				V _{REF} (ca)		

Function	Register Type	Operand	Data	Notes
V _{REF} (ca) (V _{REF} (ca) Setting)	Read/ Write	OP[5:0]	000000 _B : -- Thru -- 110010 _B : See Table 12 All Others: Reserved	1,2,3, 5,6
VR-CA (V _{REF} (ca) Range)		OP[6]	0 _B : V _{REF} (ca) Range[0] enabled 1 _B : V _{REF} (ca) Range[1] enabled (default)	1,2,4, 5,6

NOTE 1 This register controls the V_{REF}(ca) levels for Frequency-Set-Point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting OP[6] appropriately.

NOTE 2 A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See 4.16, MRR Operation.

NOTE 3 A write to OP[5:0] sets the internal V_{REF}(ca) level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF}(ca) to reach the set level depends on the step size from the current level to the new level. See 4.19, V_{REF}(ca) training for more information.

NOTE 4 A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(ca) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(ca) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.13 MR12 Register Information (MA[7:0] = 0C_H) (cont'd)

Table 12 — V_{REF} Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of V _{DD2})	Range[1] Values (% of V _{DD2})	Notes
V _{REF} Settings for MR12	OP[5:0]	000000 _B : 10.0%	011010 _B : 20.4%	000000B: 22.0%
		000001 _B : 10.4%	011011 _B : 20.8%	000001B: 22.4%
		000010 _B : 10.8%	011100 _B : 21.2%	000010B: 22.8%
		000011 _B : 11.2%	011101 _B : 21.6%	000011B: 23.2%
		000100 _B : 11.6%	011110 _B : 22.0%	000100B: 23.6%
		000101 _B : 12.0%	011111 _B : 22.4%	000101B: 24.0%
		000110 _B : 12.4%	100000 _B : 22.8%	000110B: 24.4%
		000111 _B : 12.8%	100001 _B : 23.2%	000111B: 24.8%
		001000 _B : 13.2%	100010 _B : 23.6%	001000B: 25.2%
		001001 _B : 13.6%	100011 _B : 24.0%	001001B: 25.6%
		001010 _B : 14.0%	100100 _B : 24.4%	001010B: 26.0%
		001011 _B : 14.4%	100101 _B : 24.8%	001011B: 26.4%
		001100 _B : 14.8%	100110 _B : 25.2%	001100B: 26.8%
		001101 _B : 15.2%	100111 _B : 25.6%	001101B: 27.2% (Default)
		001110 _B : 15.6%	101000 _B : 26.0%	100111B: 37.6%
		001111 _B : 16.0%	101001 _B : 26.4%	101000B: 38.0%
		010000 _B : 16.4%	101010 _B : 26.8%	101001B: 38.4%
		010001 _B : 16.8%	101011 _B : 27.2%	101010B: 39.2%
		010010 _B : 17.2%	101100 _B : 27.6%	101011B: 39.6%
		010011 _B : 17.6%	101101 _B : 28.0%	101100B: 40.0%
		010100 _B : 18.0%	101110 _B : 28.4%	101101B: 40.4%
		010101 _B : 18.4%	101111 _B : 28.8%	101110B: 40.8%
		010110 _B : 18.8%	110000 _B : 29.2%	101111B: 41.2%
		010111 _B : 19.2%	110001 _B : 29.6%	110000B: 41.6%
		011000 _B : 19.6%	110010 _B : 30.0%	110001B: 42.0%
		011001 _B : 20.0%	All Others: Reserved	All Others: Reserved

NOTE 1 These values may be used for MR12 OP[5:0] to set the V_{REF}(ca) levels in the LPDDR4-SDRAM.

NOTE 2 The range may be selected in the MR12 register by setting OP[6] appropriately.

NOTE 3 The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

3.4.14 MR13 Register Information (MA [7:0] = 0D_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RFU	VRCG	VRO	RPT	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	0 _B : Normal Operation (default) 1 _B : Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	0 _B : Disable (default) 1 _B : Enable	
VRO (V _{REF} Output)		OP[2]	0 _B : Normal operation (default) 1 _B : Output the V _{REF} (ca) and V _{REF} (dq) values on DQ bits	2
VRCG (V _{REF} Current Generator)		OP[3]	0 _B : Normal Operation (default) 1 _B : V _{REF} Fast Response (high current) mode	3
RRO Refresh rate option		OP[4]	0 _B : Disable codes 001 and 010 in MR4 OP[2:0] 1 _B : Enable all codes in MR4 OP[2:0]	4, 5
DMD (Data Mask Disable)		OP[5]	0 _B : Data Mask Operation Enabled (default) 1 _B : Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write Enable)		OP[6]	0 _B : Frequency-Set-Point[0] (default) 1 _B : Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0 _B : Frequency-Set-Point[0] (default) 1 _B : Frequency-Set-Point [1]	8

NOTE 1 A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See 4.21, Command Bus Training, for more information.

NOTE 2 When set, the LPDDR4-SDRAM will output the V_{REF}(ca) and V_{REF}(dq) voltages on DQ pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor specific.

NOTE 3 When OP[3]=1, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.

NOTE 4 MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.

NOTE 5 When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.

NOTE 6 When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), masked write command is illegal. See 4.10, LPDDR4 Data Mask (DM) and Data Bus Inversion (DBIdc) Function.

NOTE 7 FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions: V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

NOTE 8 FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions: V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

3.4.15 MR14 Register Information (MA[7:0] = 0E_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(dq)				V _{REF} (dq)		

Function	Register Type	Operand	Data	Notes
V _{REF} (dq) (V _{REF} (dq) Setting)	Read/ Write	OP[5:0]	000000 _B : -- Thru -- 110010 _B : See Table 13 All Others: Reserved	1,2,3, 5,6
VR(dq) (V _{REF} (dq) Range)		OP[6]	0 _B : V _{REF} (dq) Range[0] enabled 1 _B : V _{REF} (dq) Range[1] enabled (default)	1,2,4, 5,6

NOTE 1 This register controls the V_{REF}(dq) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.

NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See 4.16, MRR Operation.

NOTE 3 A write to OP[5:0] sets the internal V_{REF}(dq) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for V_{REF}(dq) to reach the set level depends on the step size from the current level to the new level. See 4.20, V_{REF}(dq) training for more information.

NOTE 4 A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(dq) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(dq) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.15 MR14 Register Information ($MA[7:0] = 0E_H$)

Table 13 — V_{REF} Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of V_{DDQ})	Range[1] Values (% of V_{DDQ})	Notes
V_{REF} Settings for MR14	OP[5:0]	000000 _B : 10.0%	011010 _B : 20.4%	000000 _B : 22.0%
		000001 _B : 10.4%	011011 _B : 20.8%	000001 _B : 22.4%
		000010 _B : 10.8%	011100 _B : 21.2%	000010 _B : 22.8%
		000011 _B : 11.2%	011101 _B : 21.6%	000011 _B : 23.2%
		000100 _B : 11.6%	011110 _B : 22.0%	000100 _B : 23.6%
		000101 _B : 12.0%	011111 _B : 22.4%	000101 _B : 24.0%
		000110 _B : 12.4%	100000 _B : 22.8%	000110 _B : 24.4%
		000111 _B : 12.8%	100001 _B : 23.2%	000111 _B : 24.8%
		001000 _B : 13.2%	100010 _B : 23.6%	001000 _B : 25.2%
		001001 _B : 13.6%	100011 _B : 24.0%	001001 _B : 25.6%
		001010 _B : 14.0%	100100 _B : 24.4%	001010 _B : 26.0%
		001011 _B : 14.4%	100101 _B : 24.8%	001011 _B : 26.4%
		001100 _B : 14.8%	100110 _B : 25.2%	001100 _B : 26.8%
		001101 _B : 15.2%	100111 _B : 25.6%	001101 _B : 27.2% (Default)
		001110 _B : 15.6%	101000 _B : 26.0%	100111 _B : 37.6%
		001111 _B : 16.0%	101001 _B : 26.4%	101001 _B : 38.0%
		010000 _B : 16.4%	101010 _B : 26.8%	001111 _B : 38.4%
		010001 _B : 16.8%	101011 _B : 27.2%	010001 _B : 38.8%
		010010 _B : 17.2%	101100 _B : 27.6%	010001 _B : 39.2%
		010011 _B : 17.6%	101101 _B : 28.0%	010010 _B : 39.6%
		010100 _B : 18.0%	101110 _B : 28.4%	010011 _B : 40.0%
		010101 _B : 18.4%	101111 _B : 28.8%	010100 _B : 40.4%
		010110 _B : 18.8%	110000 _B : 29.2%	010101 _B : 40.8%
		010111 _B : 19.2%	110001 _B : 29.6%	010110 _B : 41.2%
		011000 _B : 19.6%	110001 _B : 30.0%	010111 _B : 41.6%
		011001 _B : 20.0%	All Others: Reserved	011000 _B : 42.0%
				All Others: Reserved

NOTE 1 These values may be used for MR14 OP[5:0] to set the $V_{REF}(dq)$ levels in the LPDDR4-SDRAM.

NOTE 2 The range may be selected in the MR14 register by setting OP[6] appropriately.

NOTE 3 The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

3.4.16 MR15 Register Information (MA[7:0] = 0F_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	<p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:</p> <p>0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55_H</p>	1,2,3

NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.

NOTE 2 DMI[0] is not inverted, and always transmits the “true” data contained in MR32/MR40.

NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 14 — MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

3.4.17 MR16 Register Information (MA[7:0] = 10_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0 _B : Bank Refresh enabled (default) : Unmasked 1 _B : Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxx1	Bank 0
1	xxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xx1xxxxx	Bank 4
5	x1xxxxxx	Bank 5
6	1xxxxxxx	Bank 6
7	1xxxxxxxx	Bank 7

NOTE 1 When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.

NOTE 2 PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking.

3.4.18 MR17 Register Information (MA[7:0] = 11_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	0 _B : Segment Refresh enabled (default) 1 _B : Segment Refresh disabled	

Segment	OP[n]	Segment Mask	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	TBD	TBD
0	0	xxxxxx1							000 _B
1	1	xxxxx1x							001 _B
2	2	xxxx1xx							010 _B
3	3	xxx1xxx							011 _B
4	4	xx1xxxx							100 _B
5	5	xx1xxxxx							101 _B
6	6	x1xxxxxx	110 _B	Not Allowed	110 _B	Not Allowed	110 _B	Not Allowed	110 _B
7	7	1xxxxxxx	111 _B		111 _B		111 _B		111 _B

NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.

NOTE 2 PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.

NOTE 3 For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00_B).

3.4.19 MR18 Register Information (MA[7:0] = 12_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	1,2,3

NOTE 1 MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.

NOTE 2 Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.

NOTE 3 A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.4.20 MR19 Register Information (MA[7:0] = 13_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

NOTE 1 MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.

NOTE 2 Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.

NOTE 3 A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.4.21 MR20 Register Information (MA[7:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0 _B : Do not invert 1 _B : Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55 _H	1,2

NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.

NOTE 2 DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.

NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 15 - MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

3.4.22 MR22 Register Information ($MA[7:0] = 16_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	ODTD-CA	ODTE-CS	ODTE-CK			CODT	

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000 _B : Disable (Default) 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,3
ODTE-CK (CK ODT enabled for nonterminating rank)			0 _B : ODT-CK Over-ride Disabled (Default) 1 _B : ODT-CK Over-ride Enabled	
ODTE-CS (CS ODT enable for non terminating rank)		OP[4]	0 _B : ODT-CS Over-ride Disabled (Default) 1 _B : ODT-CS Over-ride Enabled	2,3,5, 6,8
ODTD-CA (CA ODT termination disable)		OP[5]	0 _B : ODT-CAobeys ODT_CA bond pad (default) 1 _B : ODT-CA Disabled	2,3,6, 7,8

NOTE 1 All values are "typical".

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.

NOTE 5 When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.

NOTE 6 For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.

NOTE 7 When OP[5]=0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT_CA bond pad or MR11-OP[6:4].

NOTE 8 To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Precharge Power-down.

3.4.23 MR23 Register Information (MA[7:0] = 17_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS interval timer run time setting							

Function	Register Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	<p>00000000_B: DQS interval timer stop via MPC Command (Default)</p> <p>00000001_B: DQS timer stops automatically at 16th clocks after timer start</p> <p>00000010_B: DQS timer stops automatically at 32nd clocks after timer start</p> <p>00000011_B: DQS timer stops automatically at 48th clocks after timer start</p> <p>00000100_B: DQS timer stops automatically at 64th clocks after timer start</p> <p>----- Thru -----</p> <p>00111111_B: DQS timer stops automatically at (63X16)th clocks after timer start</p> <p>01XXXXXX_B: DQS timer stops automatically at 2048th clocks after timer start</p> <p>10XXXXXX_B: DQS timer stops automatically at 4096th clocks after timer start</p> <p>11XXXXXX_B: DQS timer stops automatically at 8192nd clocks after timer start</p>	1, 2

NOTE 1 MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000_B.

NOTE 2 MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

3.4.24 MR24 Register Information (MA[7:0] = 18_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode BAn			Unlimited	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000 _B : Unknown when bit OP3=0 (Note 1) Unlimited when bit OP3=1 (Note 2) 001 _B : 700K 010 _B : 600K 011 _B : 500K 100 _B : 400K 101 _B : 300K 110 _B : 200K 111 _B : Reserved	
			0 _B : OP[2:0] define MAC value 1 _B : Unlimited MAC value (Note 2, Note 3)	
TRR Mode BAn	Write-only	OP[6:4]	000 _B : Bank 0 001 _B : Bank 1 010 _B : Bank 2 011 _B : Bank 3 100 _B : Bank 4 101 _B : Bank 5 110 _B : Bank 6 111 _B : Bank 7	
			0 _B : Disabled (default) 1 _B : Enabled	

NOTE 1 Unknown means that the device is not tested for tMAC and pass/fail value in unknown.

NOTE 2 There is no restriction to number of activates.

NOTE 3 MR24 OP [2:0] is set to zero.

3.4.25 MR25 Register Information (MA[7:0] = 19_H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read-only	OP[7:0]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	

3.4.26 MR32 Register Information (MA[7:0] = 20_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "A" (default = 5A _H)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	X _B : An MPC command with OP[6:0]= 10000011 _B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5A _H " is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

3.4.27 MR40 Register Information (MA[7:0] = 28H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B" (default = 3C _H)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write only	OP[7:0]	X _B : A default pattern "3C _H " is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3

NOTE 1 The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.

NOTE 2 MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.

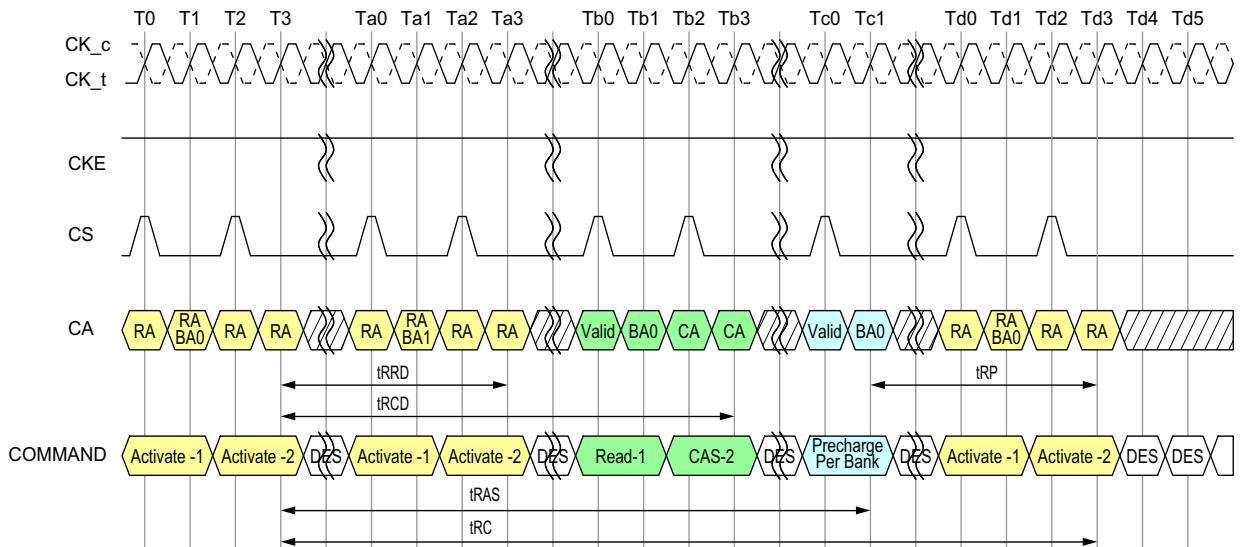
NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].

NOTE 4 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

4 Command Definitions and Timing Diagrams

4.1 Activate Command

The ACTIVATE command is composed of two consecutive commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the device(tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.



NOTES : 1. A PRECHARGE command uses tRPab timing for all-bank PRECHARGE and tRPpb timing for single-bank PRECHARGE.

In this figure, tRP is used to denote either all-bank PRECHARGE or a single-bank PRECHARGE.

/\ / \ DON'T CARE \ \ \ \ TIME BREAK

Figure 4 — ACTIVATE Command

4.2 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR4 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

8 bank device Sequential Bank Activation Restriction:

No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the tFAW time.

The 8-Bank Device Precharge-All Allowance:

tRP for a PRECHRGAE ALL command must equal tRPab, which is greater than tRPpb.

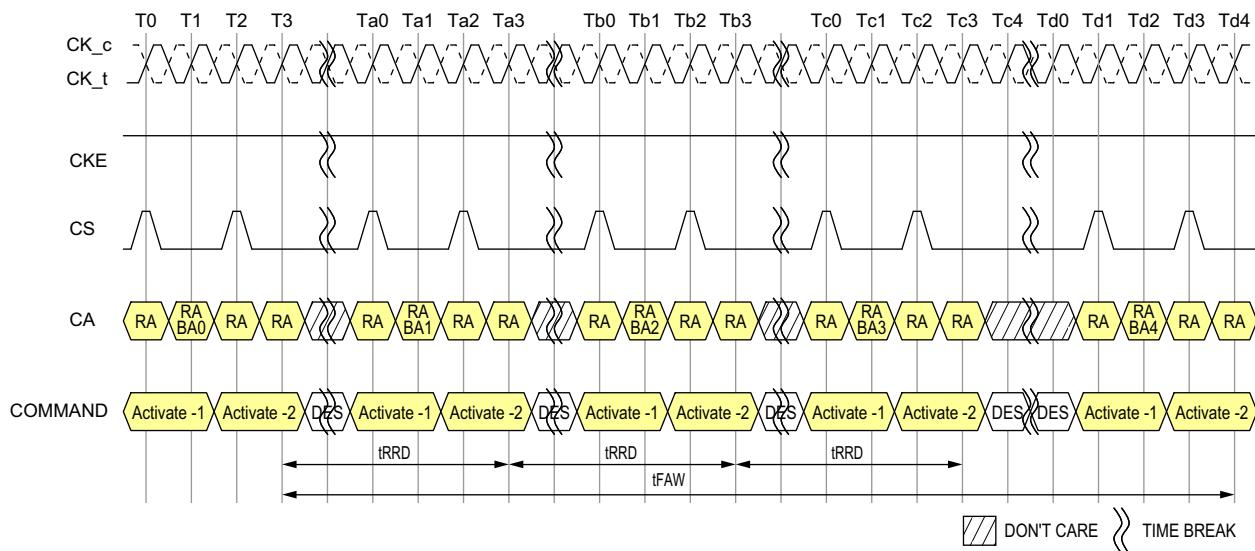


Figure 5 — tFAW Timing

4.3 Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Table 63 — Command Truth Table) at a rising edge of CK.

The LPDDR4-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see Table 63 — Command Truth Table).

4.4 Read Preamble and Postamble

The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS_t with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

For READ operations the pre-amble is $2*t_{CK}$, but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4 will have a DQS Read post-amble of $0.5*t_{CK}$ (or extended to $1.5*t_{CK}$). Standard DQS post-amble will be $0.5*t_{CK}$ driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. Figure 6 and Figure 7 show examples of DQS Read post-amble for both standard (t_{RPST}) and extended (t_{RPSTE}) post-amble operation.

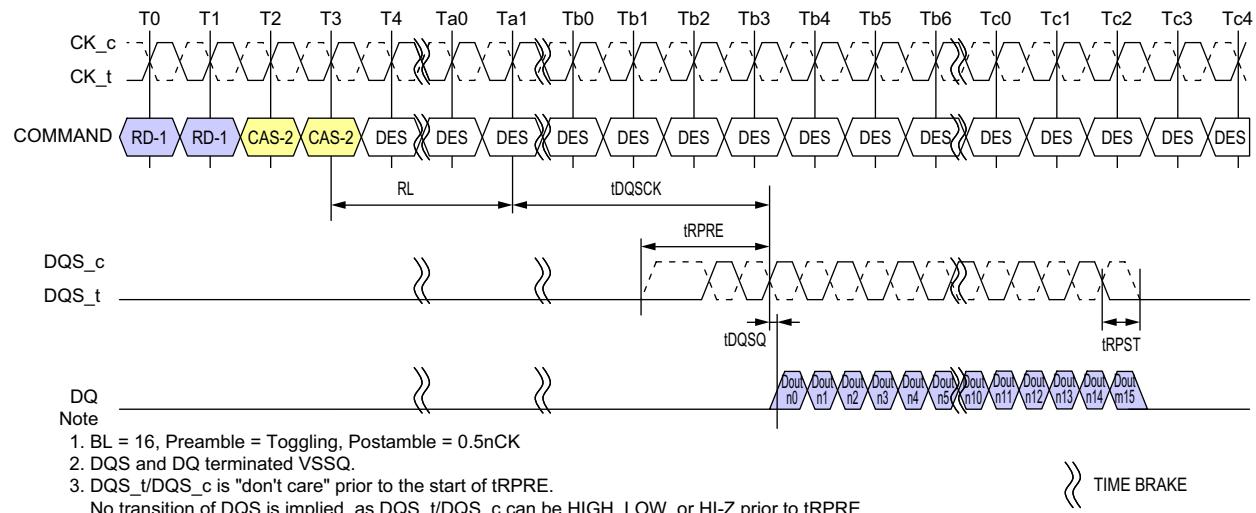


Figure 6 — DQS Read Preamble and Postamble: Toggling Preamble and 0.5nCK Postamble

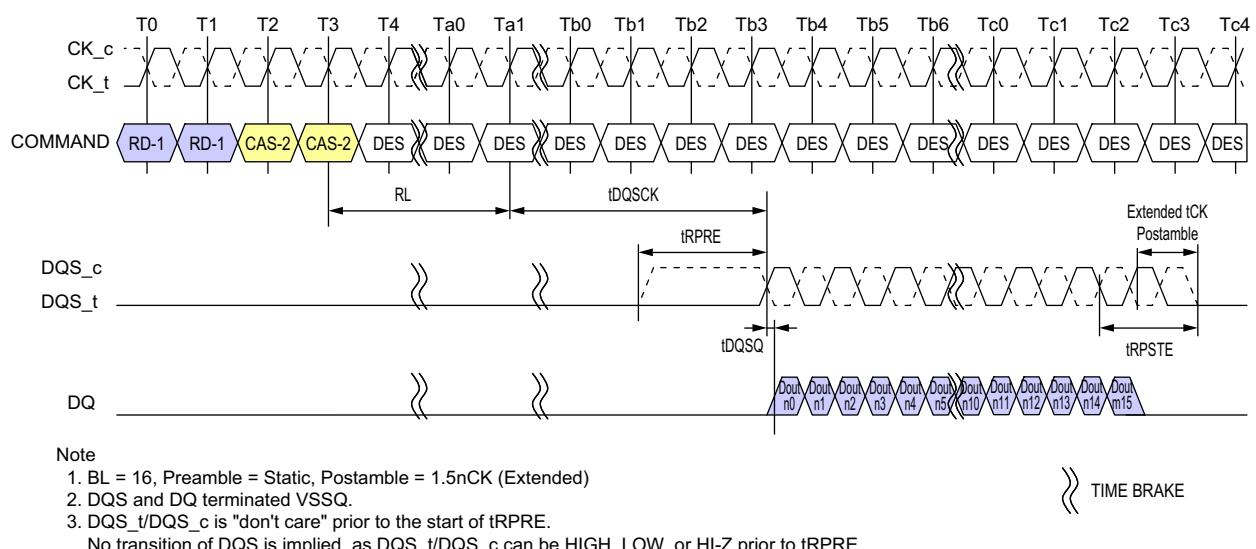


Figure 7 — DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble

4.5 Burst Read Operation

A burst Read command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by Table 63 — Command Truth Table.

The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be “0”, so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC).

The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available $RL * tCK + tDQSCK + tDQSQ$ after the rising edge of Clock that completes a read command.

The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent dataout appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register.

The RL is programmed in the mode registers.

Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c.

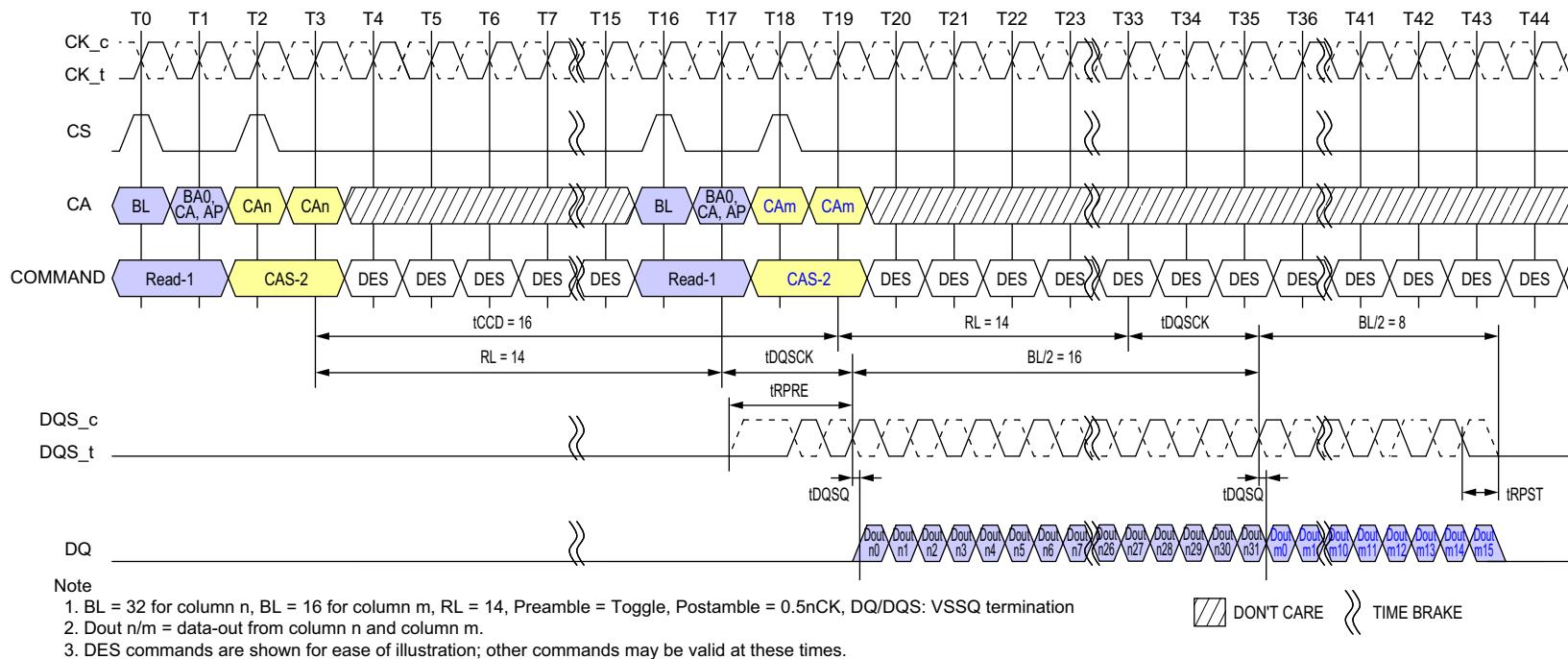
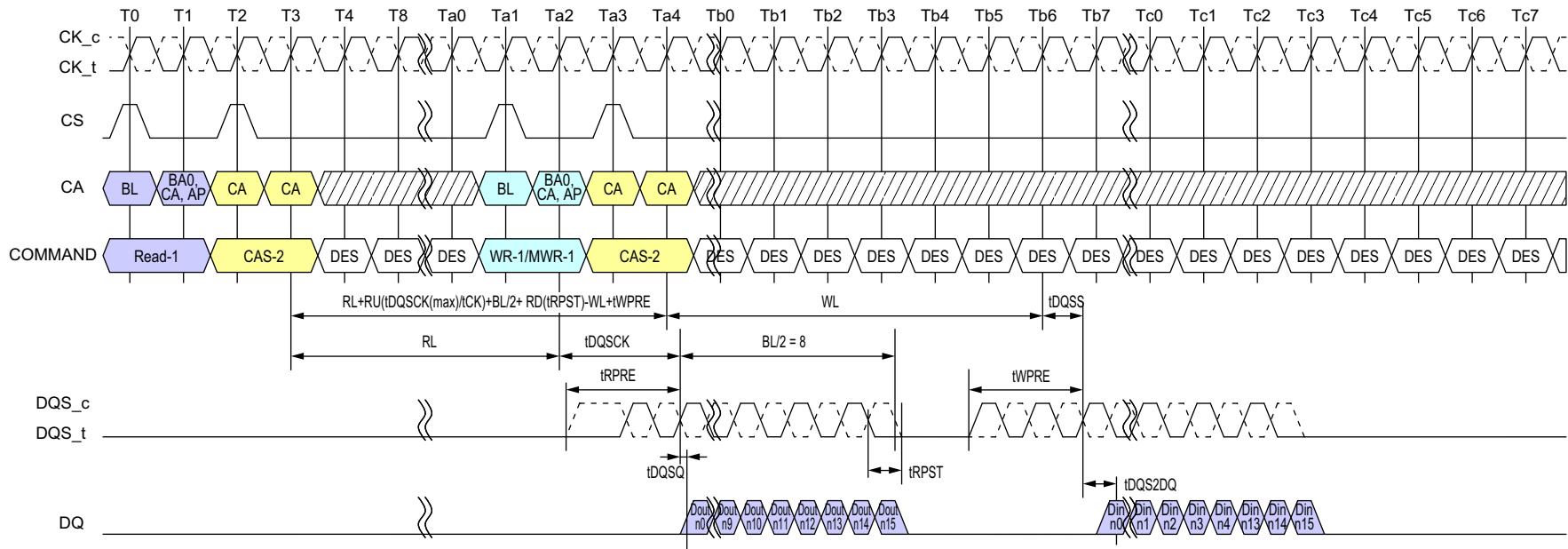


Figure 8 — Burst Read Timing



Note

1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure — 9 Burst Read followed by Burst Write or Burst Mask Write

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE or MASK WRITE latency is $RL+RU(tDQSK(max)/tCK)+BL/2+ RD(tRPST)-WL+tWPRE$.

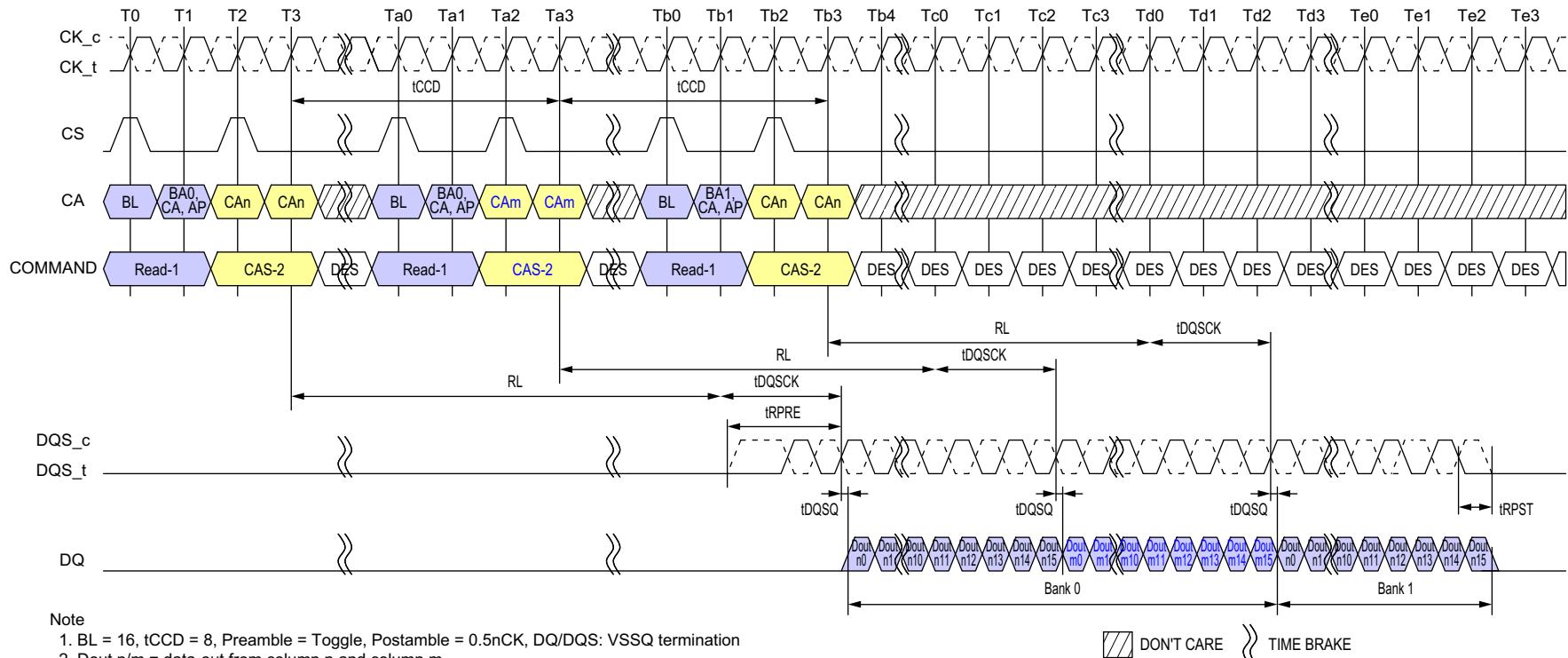


Figure 10 — Seamless Burst Read

The seamless Burst READ operation is supported by placing a READ command at every $t_{CCD}(\text{Min})$ interval for BL16 (or every $2 \times t_{CCD}(\text{Min})$ for BL32). The seamless Burst READ can access any open bank.

Note

1. BL = 16, $t_{CCD} = 8$, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

□ DON'T CARE ↗ TIME BRAKE

4.6 tDQSCK Timing Table

Table 16 — tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c - Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c - Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

NOTE 1 Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.

NOTE 2 tDQSCK_temp max delay variation as a function of Temperature.

NOTE 3 tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the $\text{Max}[\text{abs}\{tDQSCKmin@V1-tDQSCKmax@V2\}, \text{abs}\{tDQSCKmax@V1-tDQSCKmin@V2\}]/\text{abs}\{V1-V2\}$. For tester measurement VDDQ = VDD2 is assumed.

4.7 Write Preamble and Postamble

The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS_t with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

For WRITE operations, a 2^*tCK pre-amble is required at all operating frequencies.

LPDDR4 will have a DQS Write post-amble of 0.5^*tCK or extended to 1.5^*tCK . Standard DQS post-amble will be 0.5^*tCK driven by the memory controller for Writes. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Write post-amble. Figure 11 and Figure 12 show examples of DQS Write post-amble for both standard ($tWPST$) and extended ($tWPSTE$) post-amble operation.

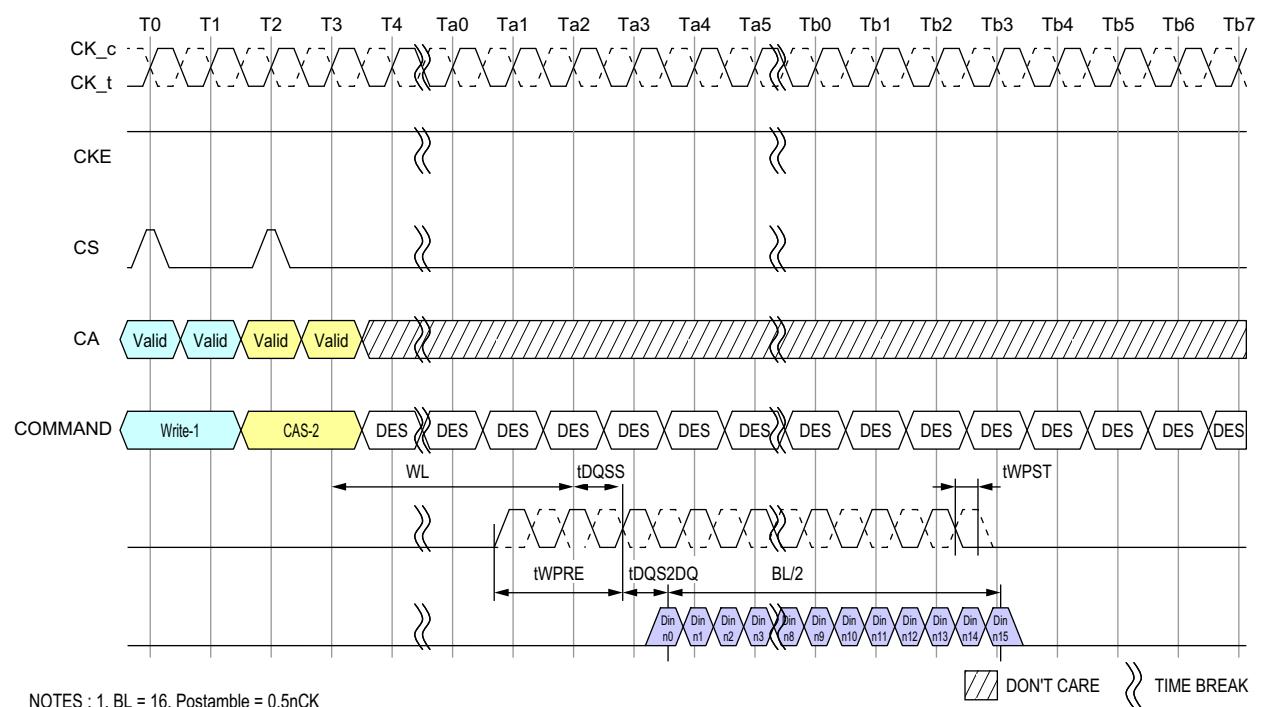


Figure 11 — DQS Write Preamble and Postamble: 0.5nCK Postamble

4.7 Write Preamble and Postamble (cont'd)

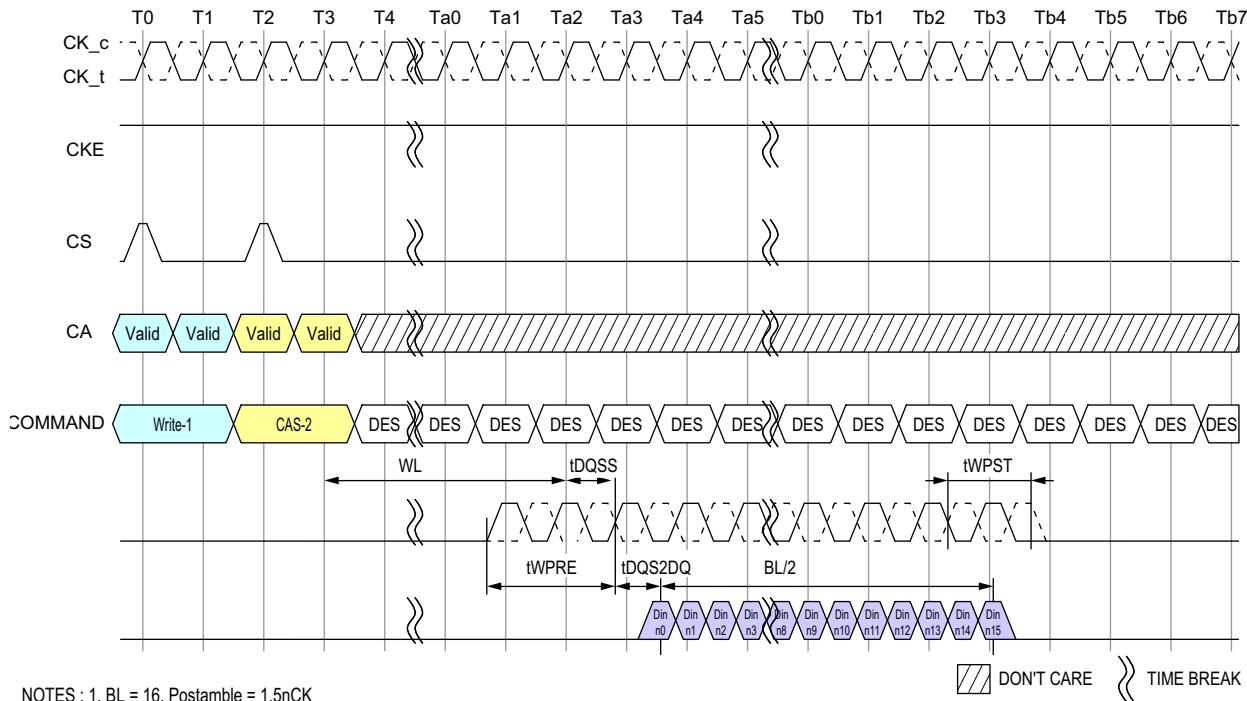


Figure 12 — DQS WriteRead Preamble and Postamble: 1.5nCK Postamble

4.8 Burst Write Operation

A burst WRITE command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by Table 63 — Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid “latching” edge of DQS must be driven $WL * tCK + tDQSS$ after the rising edge of Clock that completes a write command.

The LPDDR4-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE pre-amble is required to be $1 \times tCK$ at lower speeds, and $2 \times tCK$ at higher speeds (Frequency TBD¹). The DQS-strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (WRITE post-amble) after the completion of the burst WRITE. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and DQS_c.

1. As of publication of this document, under discussion by the formulating committee.

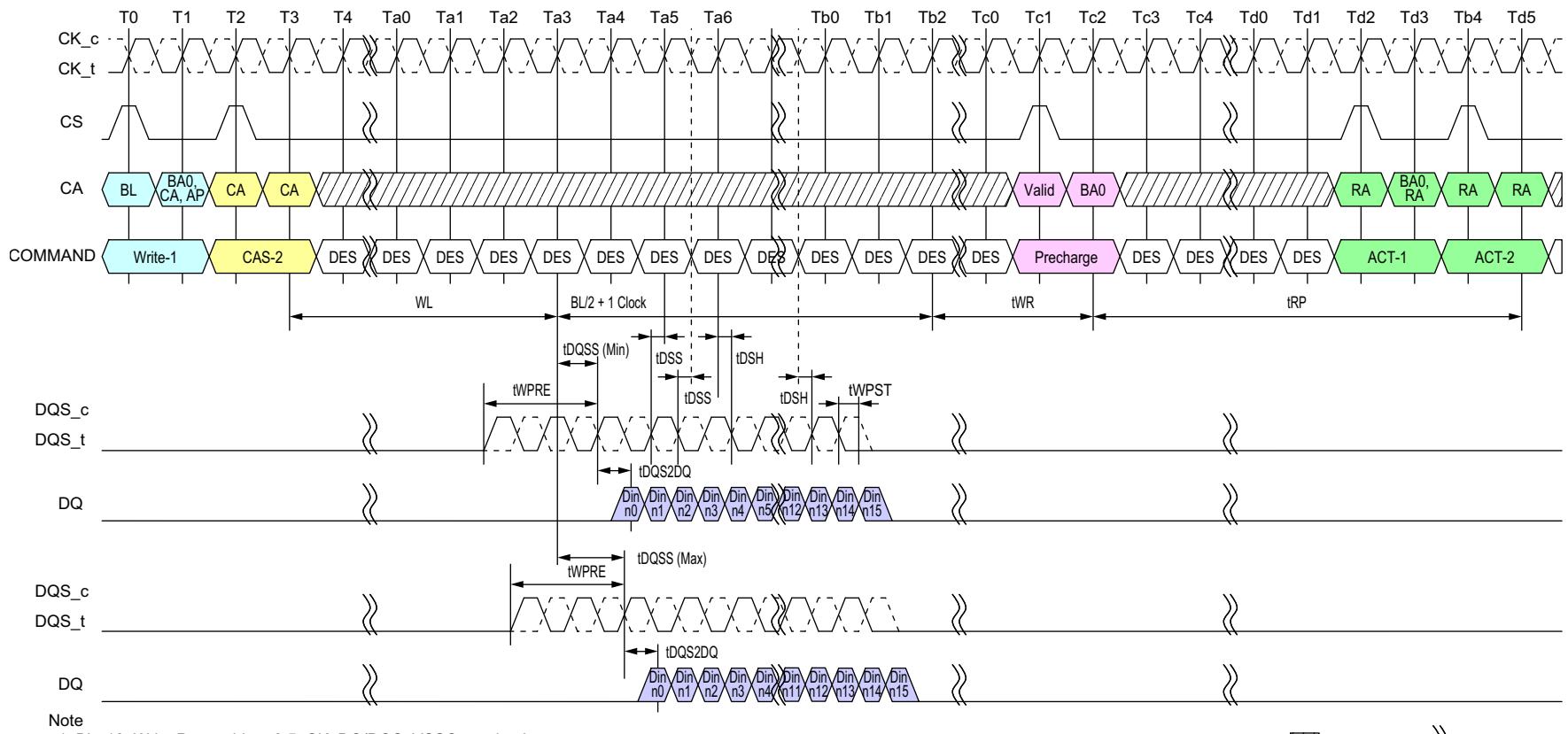
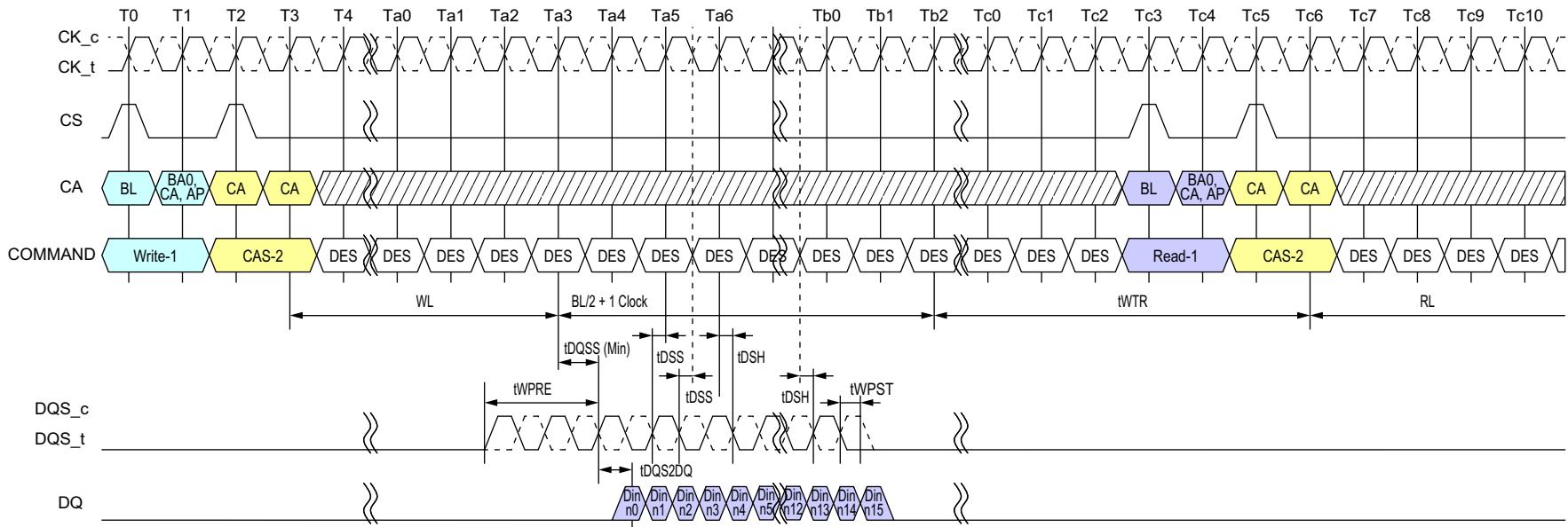


Figure 13 — Burst Write Operation



DON'T CARE TIME BREAK

Figure 14 — Burst Write Followed by Burst Read

4.9 Masked Write Operation

The LPDDR4-SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write-1 command is used to begin the operation, followed by a CAS-2 command. A Masked Write command to the same bank cannot be issued until tCCDMW later, to allow the LPDDR4-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See 4.10, Data Mask Inversion for more information on the use of the DMI signal.

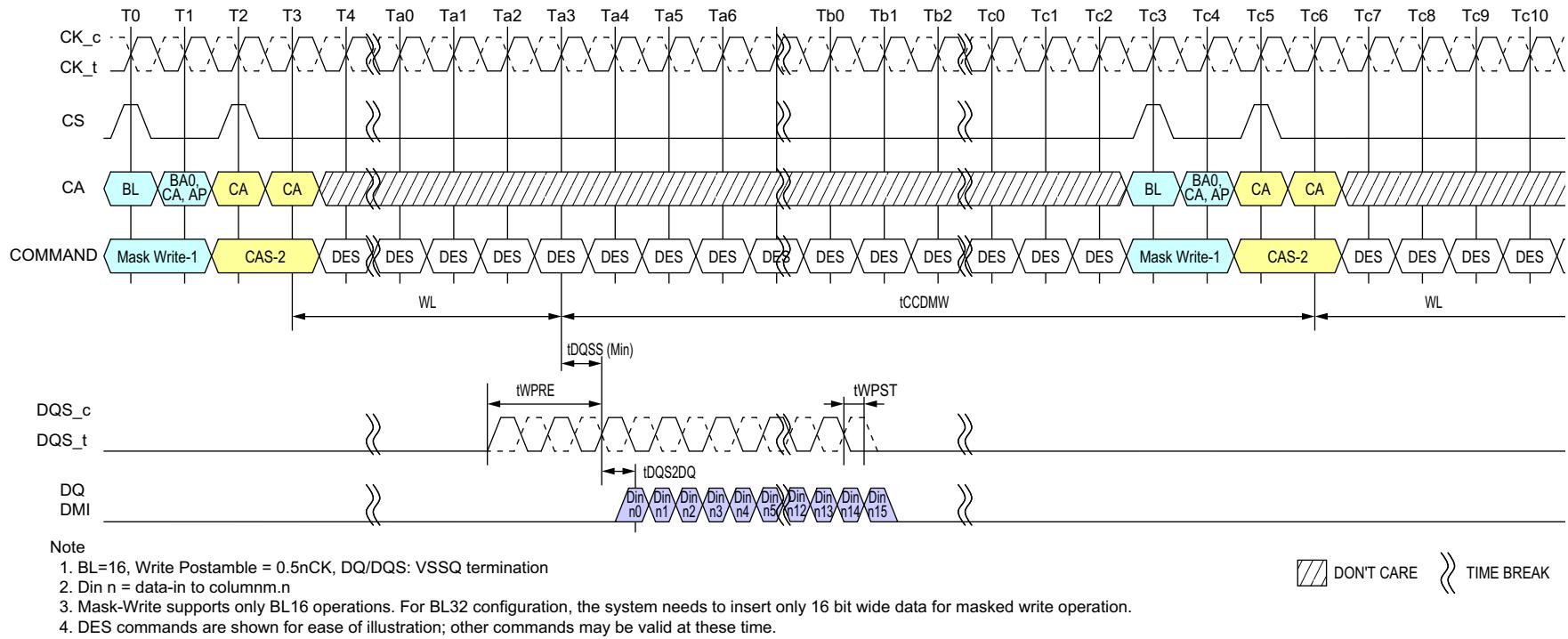


Figure 15 — Masked Write Command - Same Bank

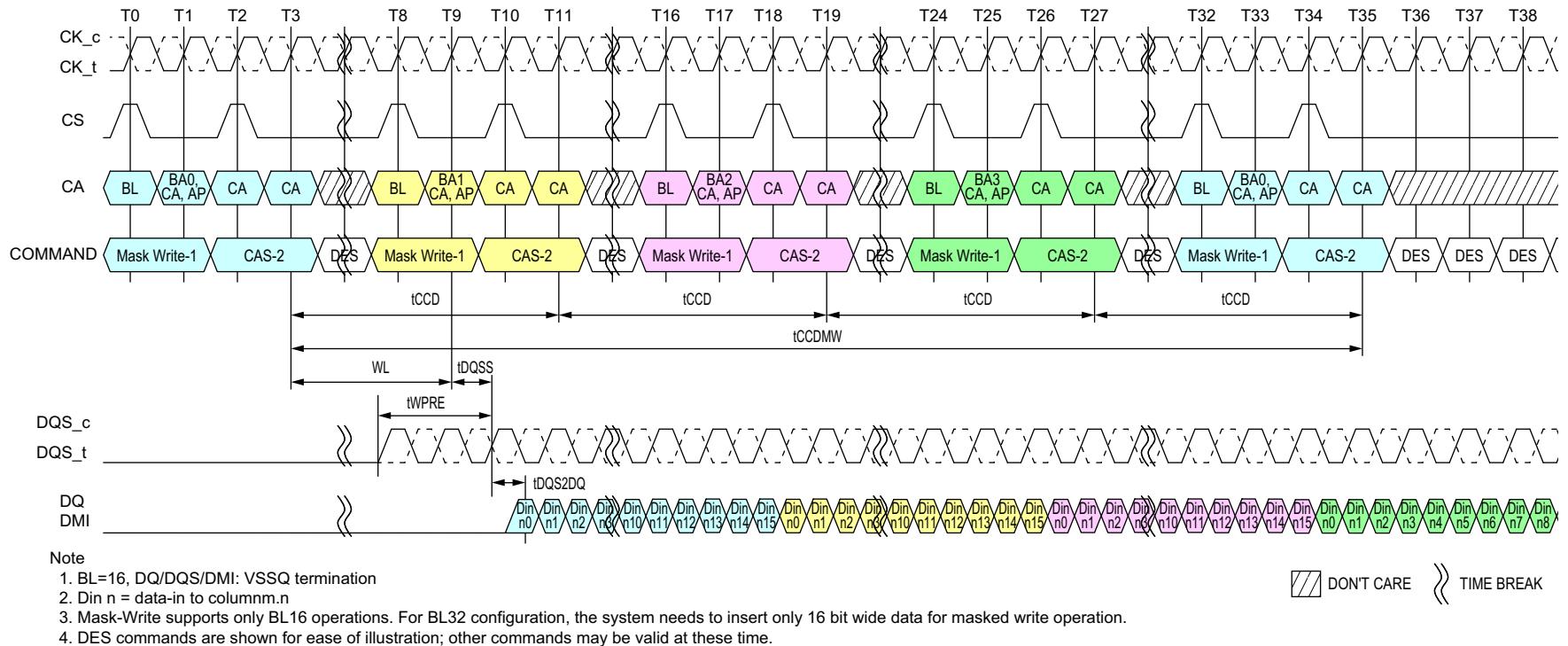


Figure 16 — Masked Write Command - Different Bank

4.9.1 Masked Write Timing constraints for BL16

Table 17 — Timing constraints for Same bank

Next CMD Current CMD	Active	Read (BL=16 or 32)	Write (BL=16 or 32)	Masked Write	Precharge
Active	illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
Read with BL = 16	illegal	8 ¹⁾	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	BL/2+max{(8,RU(tRTP/tCK)}-8
Read with BL = 32	illegal	16 ²⁾	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	BL/2+max{(8,RU(tRTP/tCK)}-8
Write with BL = 16	illegal	WL+1+BL/2 +RU(tWTR/tCK)	8 ¹⁾	tCCDMW ³⁾	WL+ 1 + BL/2+RU(tWR/tCK)
Write with BL = 32	illegal	WL+1+BL/2 +RU(tWTR/tCK)	16 ²⁾	tCCDMW +8 ⁴⁾	WL+ 1 + BL/2+RU(tWR/tCK)
Masked Write	illegal	WL+1+BL/2 +RU(tWTR/tCK)	tCCD	tCCDMW ³⁾	WL+ 1 + BL/2 +RU(tWR/tCK)
Precharge	RU(tRP/tCK), RU(tRPab/tCK)	illegal	illegal	illegal	4

NOTE 1 In the case of BL = 16, tCCD is 8*tCK.

NOTE 2 In the case of BL = 32, tCCD is 16*tCK.

NOTE 3 tCCDMW = 32*tCK (4*tCCD at BL=16)

NOTE 4 Write with BL=32 operation has 8*tCK longer than BL =16.

4.9.1 Masked Write Timing constraints for BL16 (cont'd)

Table 18 — Timing constraints for Different bank

Next CMD Current CMD	Active	Read (BL=16 or 32)	Write (BL=16 or 32)	Masked Write	Precharge
Active	RU(tRRD/tCK)	4	4	4	4
Read with BL = 16	4	8 ¹⁾	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	4
Read with BL = 32	4	16 ²⁾	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/tCK) +BL/2-WL+tWPRE+tRPST	4
Write with BL = 16	4	WL+1+BL/2 +RU(tWTR/tCK)	8 ¹⁾	8 ¹⁾	4
Write with BL = 32	4	WL+1+BL/2 +RU(tWTR/tCK)	16 ²⁾	16 ²⁾	4
Masked Write	4	WL+1+BL/2 +RU(tWTR/tCK)	8 ¹⁾	8 ¹⁾	4
Precharge	4	4	4	4	4

NOTE 1 In the case of BL = 16, tCCD is 8*tCK.

NOTE 2 In the case of BL = 32, tCCD is 16*tCK.

4.10 LPDDR4 Data Mask (DM) and Data Bus Inversion (DBI_{dc}) Function

LPDDR4 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are shown below.

- LPDDR4 device supports Data Mask (DM) function for Write operation.
- LPDDR4 device supports Data Bus Inversion (DBI_{dc}) function for Write and Read operation.
- LPDDR4 supports DM and DBI_{dc} function with a byte granularity.
- DBI_{dc} function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBI_{dc} function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR4 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

There are eight possible combinations for LPDDR4 device with DM and DBI_{dc} function. Table 19 describes the functional behavior for all combinations.

4.10 LPDDR4 Data Mask (DM) and Data Bus Inversion (DBIdc) Function (cont'd)

Table 19 — Function Behavior of DMI Signal During Write, Masked Write and Read Operation

DM Function	Write DBIdc Function	Read DBIdc Function	DMI Signal during Write Command	Signal during Masked Write Command	DMI Signal During Read	DMI Signal during MPC WR FIFO	DMI Signal during MPC RD FIFO	DMI Signal during MPC DQ Read Training	DMI Signal During MRR
Disable	Disable	Disable	Notes: 1	Notes: 1, 3	Notes: 2	Note: 1	Note: 2	Note: 2	Notes: 2
Disable	Enable	Disable	Notes: 4	Notes: 3	Notes: 2	Note: 9	Note: 10	Note: 11	Notes: 2
Disable	Disable	Enable	Notes: 1	Notes: 3	Notes: 5	Note: 9	Note: 10	Note: 11	Notes: 12
Disable	Enable	Enable	Notes: 4	Notes: 3	Notes: 5	Note: 9	Note: 10	Note: 11	Notes: 12
Enable	Disable	Disable	Notes: 6	Notes: 7	Notes: 2	Note: 9	Note: 10	Note: 11	Notes: 2
Enable	Enable	Disable	Notes: 4	Notes: 8	Notes: 2	Note: 9	Note: 10	Note: 11	Notes: 2
Enable	Disable	Enable	Notes: 6	Notes: 7	Notes: 5	Note: 9	Note: 10	Note: 11	Notes: 12
Enable	Enable	Enable	Notes: 4	Notes: 8	Notes: 5	Note: 9	Note: 10	Note: 11	Notes: 12

NOTE 1 DMI input signal is a don't care. DMI input receivers are turned OFF.

NOTE 2 DMI output drivers are turned OFF.

NOTE 3 Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.

NOTE 4 DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR4 device inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW.

NOTE 5 The LPDDR4 DRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.

NOTE 6 The LPDDR4 DRAM does not perform any mask operation when it receives Write command. During the Write burst associated with Write command, DMI signal must be driven LOW.

NOTE 7 The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR4 DRAM does not perform mask operation and data received on DQ input is written to the array.

NOTE 8 The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. The LPDDR4 device masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR4 DRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.

NOTE 9 DMI signal is treated as a training pattern. The LPDDR4 DRAM does not perform any mask operation and does not invert Write data received on the DQ inputs.

NOTE 10 DMI signal is treated as a training pattern. The LPDDR4 DRAM returns DMI pattern written in WR FIFO.

NOTE 11 DMI signal is treated as a training pattern. For more details, see 4.24, RD DQ Calibration.

NOTE 12 DBI may apply or may not apply during normal MRR. It's vendor specific.

If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.

If read DBI is enable with MRS and vendor can support the DBI during MRR, the LPDDR4 DRAM inverts Mode Register Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.

4.10 LPDDR4 Data Mask (DM) and Data Bus Inversion (DBI_{dc}) Function (cont'd)

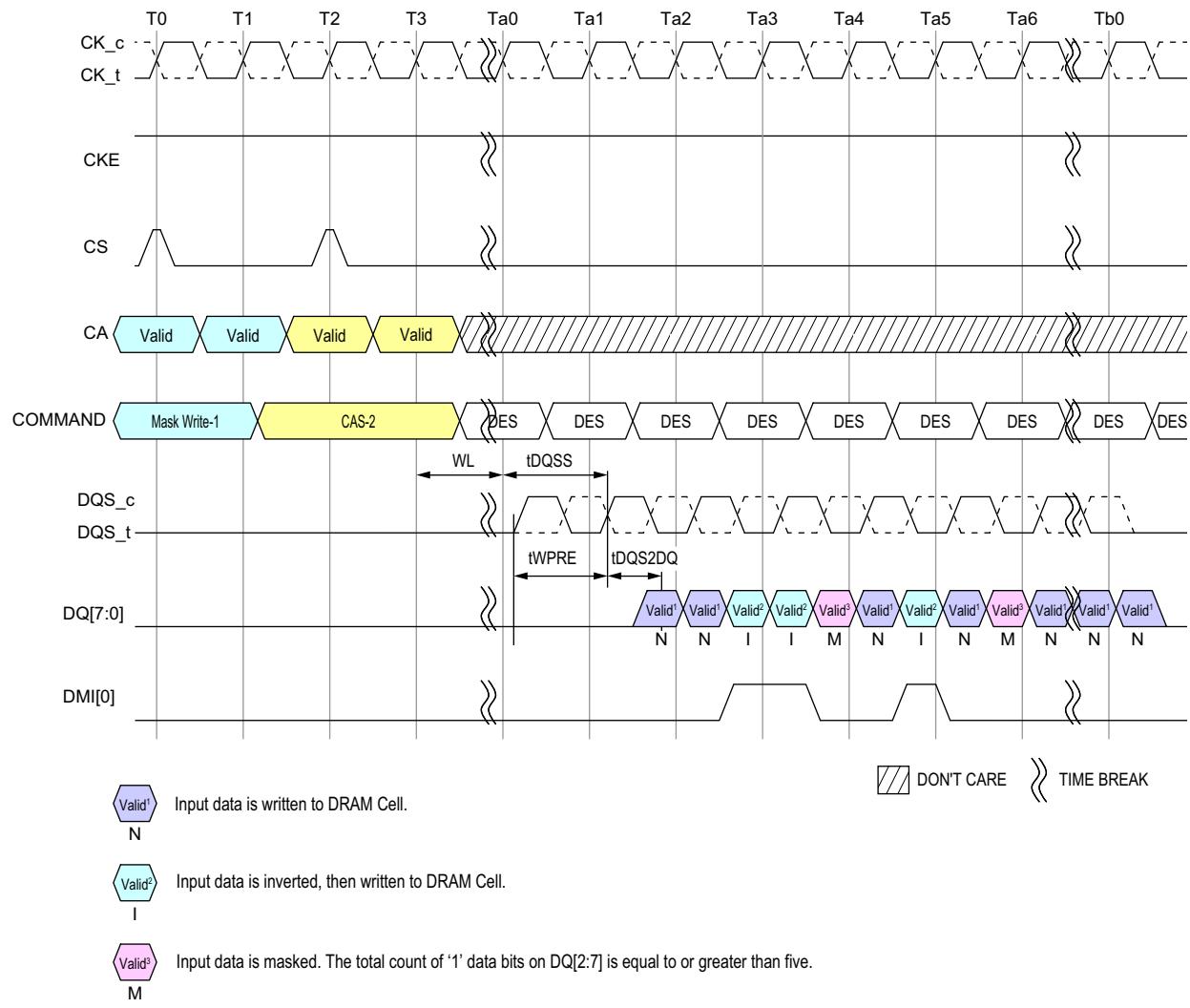
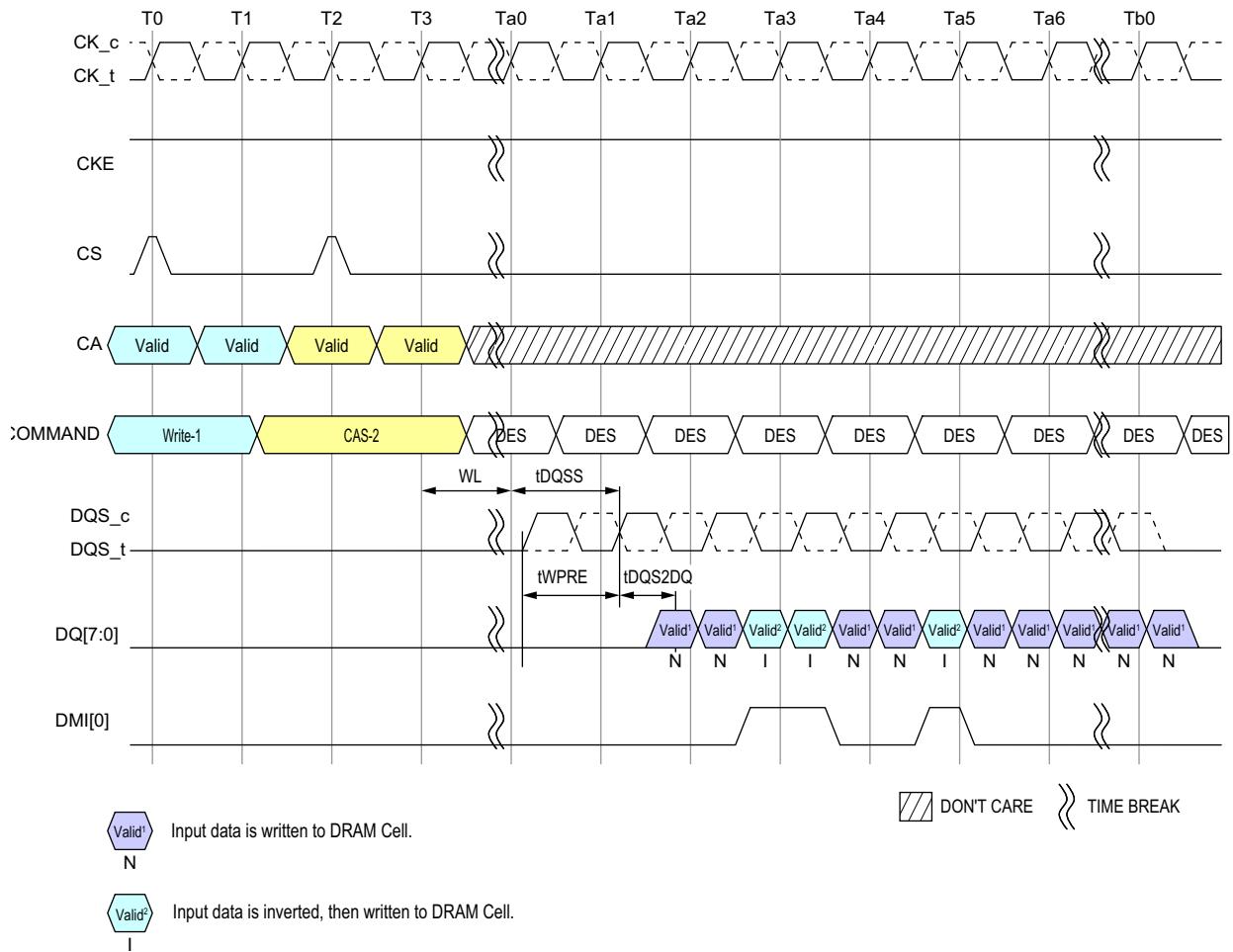


Figure 17 — Masked Write Command w/ Write DBI Enabled; DM Enabled

4.10 LPDDR4 Data Mask (DM) and Data Bus Inversion (DBIdc) Function (cont'd)



NOTES : 1. Data Mask (DM) is Disable: MR13 OP [5] = 0, Data BUS Inversion (DBI) Write is Enable: MR3 OP[7] = 1

Figure 18 — Write Command w/ Write DBI Enabled; DM Enabled

4.11 Pre-Charge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS, and CA[5:0] in the proper state as defined by Table 63 — Command Truth Table. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all-bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR4 devices can meet the instantaneous current demands, the row-precharge time for an all-bank PRECHARGE (tRPab) is longer than the perbank precharge time (tRPpb).

Table 20 — Precharge Bank Selection

AB (CA[5], R1)	BA2 (CA[2], R2)	BA1 (CA[1], R2)	BA0 (CA[0], R2)	Precharged Bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Valid	Valid	Valid	All Banks

4.11.1 Burst Read Operation Followed by a Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but PRECHARGE cannot be issued until after tRAS is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (tRP) has elapsed. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the 2nd rising clock edge of the CAS-2 command. tRTP begins BL/2 - 8 clock cycles after the READ command. For LPDDR4 READ-to-PRECHARGE timings see Table 21.

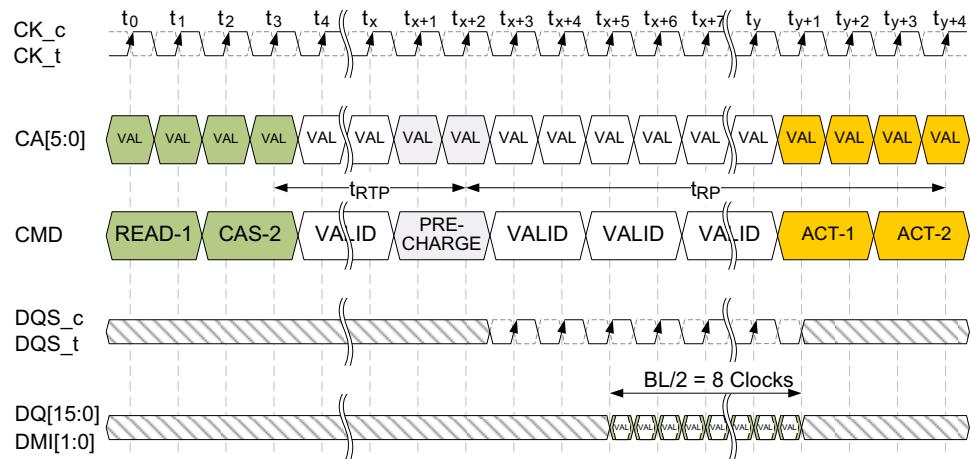


Figure 19 — Burst READ followed by PRECHARGE
(Shown with BL16, 2tCK pre-amble)

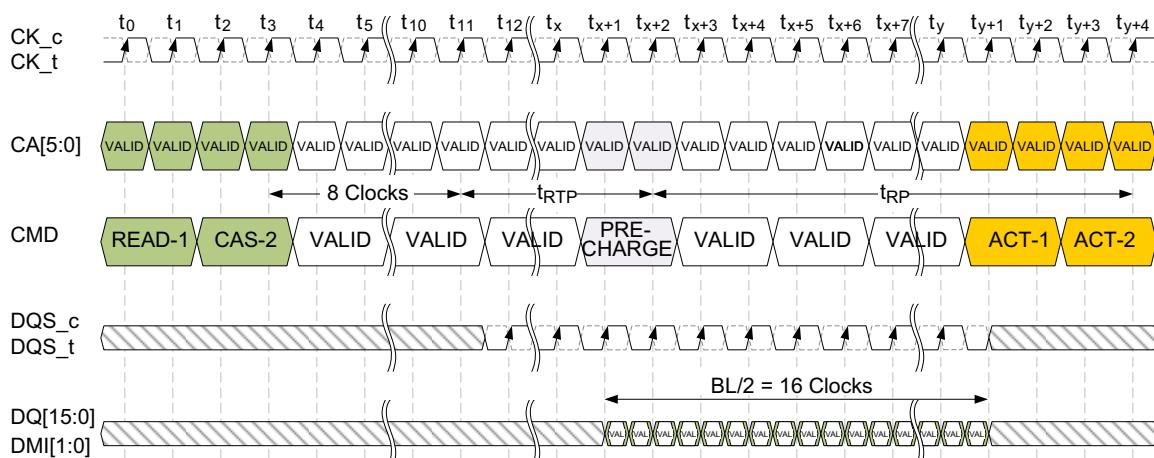
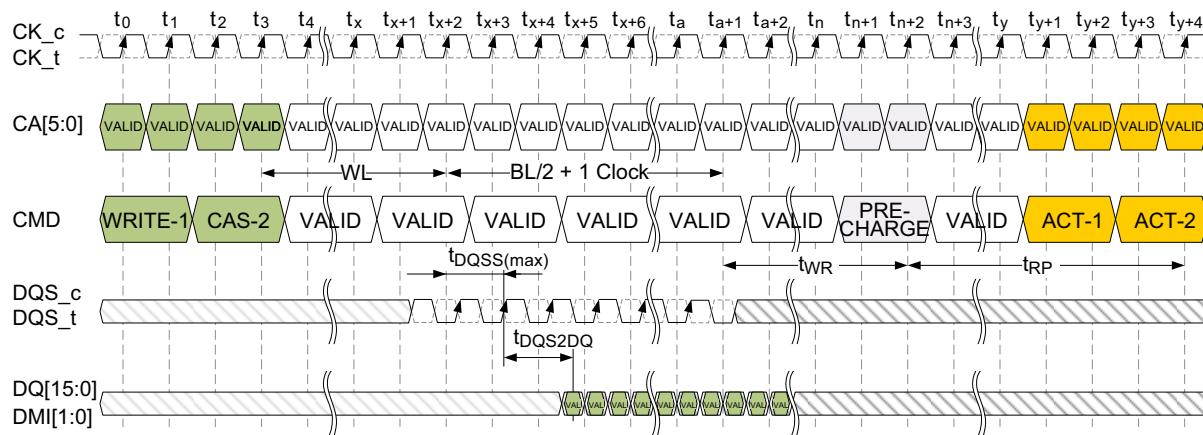


Figure 20 — Burst READ followed by PRECHARGE
(Shown with BL32, 2tCK pre-amble)

4.11.2 Burst WRITE Followed by PRECHARGE

A Write Recovery time (t_{WR}) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK_t after the last latching DQS clock of the burst.

LPDDR4-SDRAM devices write data to the memory array in prefetch multiples (prefetch=16). An internal WRITE operation can only begin after a prefetch group has been clocked, so t_{WR} starts at the prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is $WL + BL/2 + 1 + RU(t_{WR}/tCK)$ clock cycles.



**Figure 21 — Burst WRITE Followed by PRECHARGE
(Shown with BL16, 2tCK pre-amble)**

4.11.3 Auto-PRECHARGE Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-PRECHARGE function. When a READ, a WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

If AP is LOW when the READ or WRITE command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

4.11.4 Burst READ with Auto-PRECHARGE

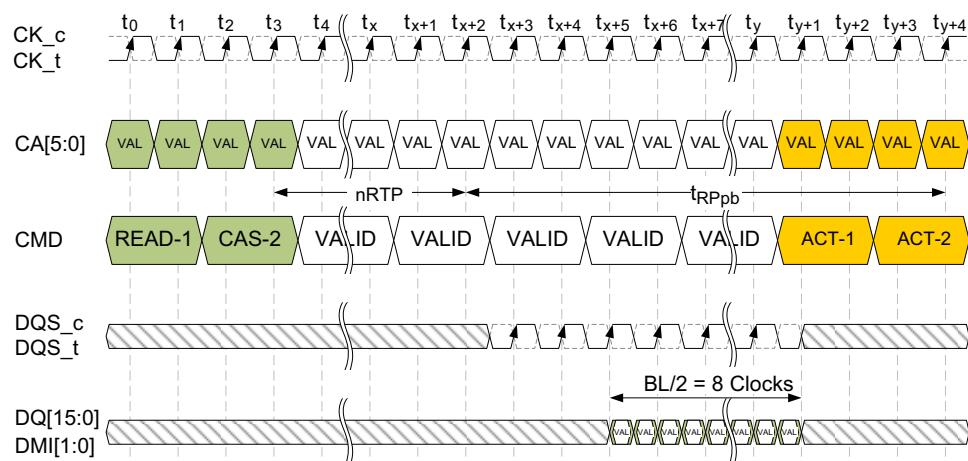
If AP is HIGH when a READ command is issued, the READ with Auto-PRECHARGE function is engaged. An internal precharge procedure starts a following delay time after the READ command. And this delay time depends on BL setting.

BL = 16: nRTP

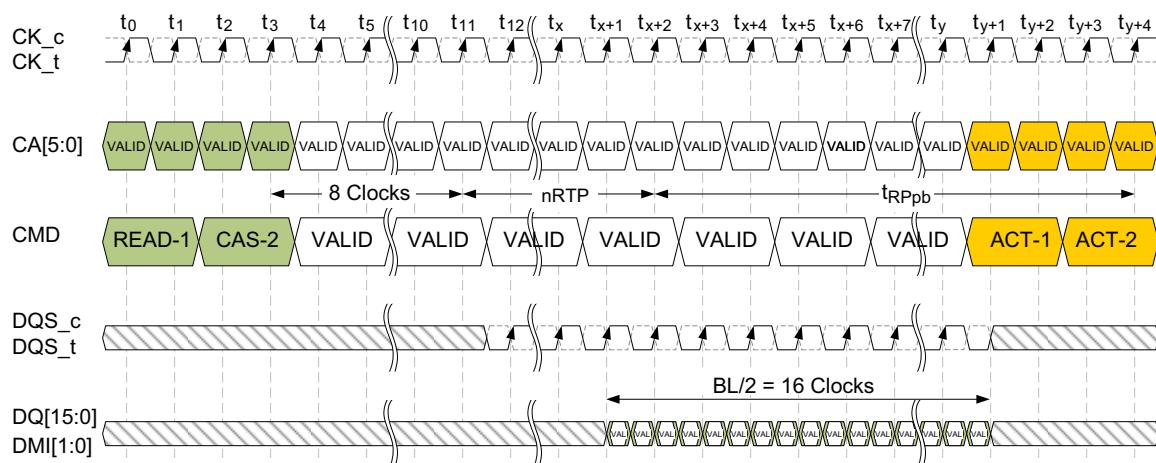
BL = 32: 8nCK + nRTP

For LPDDR4 Auto-PRECHARGE calculations, see Table 21. Following an Auto-PRECHARGE operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the Auto-PRECHARGE began, or
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



**Figure 22 — Burst READ with Auto-PRECHARGE
(Shown with BL16, 2tCK pre-amble)**



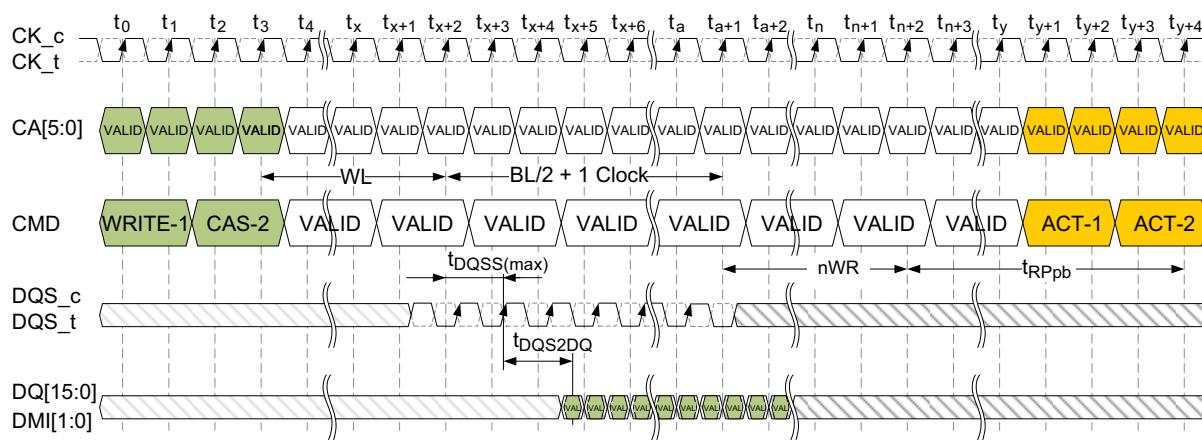
**Figure 23 — Burst READ with Auto-PRECHARGE
(Shown with BL32, 2tCK pre-amble)**

4.11.5 Burst WRITE with Auto-PRECHARGE

If AP is HIGH when a WRITE command is issued, the WRITE with Auto-PRECHARGE function is engaged. The device starts an Auto-PRECHARGE on the rising edge t_{WR} cycles after the completion of the Burst WRITE.

Following a WRITE with Auto-PRECHARGE, an ACTIVATE command can be issued to the same bank if the following conditions are met:

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the Auto-PRECHARGE began, and
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



**Figure 24 — Burst WRITE with Auto-PRECHARGE
(Shown with BL16, 2tCK pre-amble)**

4.11.5 Burst WRITE with Auto-PRECHARGE (cont'd)

Table 21 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE)(DQ ODT is Disable)

From Command	To Command	Minimum Delay between "From Command" and To Command"	Unit	Notes
READ BL=16	PRECHARGE (to same bank as Read)	tRTP	tCK	1,6
	PRECHARGE All	tRTP	tCK	1,6
READ BL=32	PRECHARGE (to same bank as Read)	8tCK + tRTP	tCK	1,6
	PRECHARGE All	8tCK + tRTP	tCK	1,6
READ w/AP BL=16	PRECHARGE (to same bank as READ w/AP)	nRTP	tCK	1,10
	PRECHARGE All	nRTP	tCK	1,10
	Activate (to same bank as READ w/AP)	nRTP + tRPpb	tCK	1,8,10
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	RL+RU(tDQSCK(max)/tCK) +BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	MASK-WR or MASK-WR w/AP (different bank)	RL+RU(tDQSCK(max)/tCK) +BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	READ or READ w/AP (same bank)	Illegal	-	
	READ or READ w/AP (different bank)	BL/2	tCK	3
READ w/AP BL=32	PRECHARGE (to same bank as READ w/AP)	8tCK + nRTP	tCK	1,10
	PRECHARGE All	8tCK + nRTP	tCK	1,10
	Activate (to same bank as READ w/AP)	8tCK + nRTP + tRPpb	tCK	1,8,10
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	RL+RU(tDQSCK(max)/tCK) +BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	MASK-WR or MASK-WR w/AP (different bank)	RL+RU(tDQSCK(max)/tCK) +BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	READ or READ w/AP (same bank)	Illegal	-	
	READ or READ w/AP (different bank)	BL/2	tCK	3
WRITE BL=16 & 32	PRECHARGE (to same bank as WRITE)	WL + BL/2 + tWR + 1	tCK	1,7
	PRECHARGE All	WL + BL/2 + tWR + 1	tCK	1,7

4.11.5 Burst WRITE with Auto-PRECHARGE (cont'd)**Table 21 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE)(DQ ODT is Disable)
(cont'd)**

From Command	To Command	Minimum Delay between "From Command" and To Command"	Unit	Notes
MASK-WR BL=16	PRECHARGE (to same bank as MASK-WR)	WL + BL/2 + tWR + 1	tCK	1,7
	PRECHARGE All	WL + BL/2 + tWR + 1	tCK	1,7
WRITE w/AP BL=16 & 32	PRECHARGE (to same bank as WRITE w/AP)	WL + BL/2 + nWR + 1	tCK	1,11
	PRECHARGE All	WL + BL/2 + nWR + 1	tCK	1,11
	ACTIVATE (to same bank as WRITE w/AP)	WL + BL/2 + nWR + 1 + tRPpb	tCK	1,8,11
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	READ or READ w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	BL/2	tCK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	tCK	3
	READ or READ w/AP (different bank)	WL + BL/2 + tWTR + 1	tCK	3,9
MASK-WR w/AP BL=16	PRECHARGE (to same bank as MASK-WR w/AP)	WL + BL/2 + nWR + 1	tCK	1,11
	PRECHARGE All	WL + BL/2 + nWR + 1	tCK	1,11
	ACTIVATE (to same bank as MASK-WR w/AP)	WL + BL/2 + nWR + 1 + tRPpb	tCK	1,8,11
	WRITE or WRITE w/AP (same bank)	Illegal	-	3
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	3
	WRITE or WRITE w/AP (different bank)	BL/2	tCK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	tCK	3
	READ or READ w/AP (same bank)	Illegal	-	3
PRECHARGE	READ or READ w/AP (different bank)	WL + BL/2 + tWTR + 1	tCK	3,9
	PRECHARGE (to same bank as PRECHARGE)	4	tCK	1
PRECHARGE All	PRECHARGE All	4	tCK	1
	PRECHARGE	4	tCK	1
	PRECHARGE All	4	tCK	1

4.11.5 Burst WRITE with Auto-PRECHARGE (cont'd)

Table 21 Notes.

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied tRP after that latest precharge command.

NOTE 2 Any command issued during the minimum delay time as specified in Table 21 is illegal.

NOTE 3 After READ w/AP, seamless read operations to different banks are supported. After WRITE w/AP or MASK-WR w/AP, seamless write operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.

NOTE 4 tRPST values depend on MR1-OP[7] respectively.

NOTE 5 tWPRE values depend on MR1-OP[2] respectively.

NOTE 6 Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRTP(ns) by tCK(ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRTP[ns] / tCK[ns])

NOTE 7 Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWR[ns] / tCK[ns])

NOTE 8 Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRPpb(ns) by tCK(ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRPpb[ns] / tCK[ns])

NOTE 9 Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWTR(ns) by tCK(ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWTR[ns] / tCK[ns])

NOTE 10 For Read w/AP the value is nRTP which is defined in Mode Register 2.

NOTE 11 For Write w/AP the value is nWR which is defined in Mode Register 1.

Table 22 - Timing Between Commands (PRECHARGE and Auto-PRECHARGE): DQ ODT is Enable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
READ w/AP BL=16	WRITE or WRITE w/AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD (tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD (tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2, 3
READ w/AP BL=32	WRITE or WRITE w/AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD (tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD (tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2, 3

NOTE 1 The rest of the timing about precharge and Auto-Precharge is same as DQ ODT is Disable case.

NOTE 2 After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.

NOTE 3 tRPST values depend on MR1-OP[7] respectively.

4.12 Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of the clock. Per-bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. All-bank REFRESH is initiated with CA5 HIGH at the first rising edge of the clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1 and CA2 at the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. e.g. REFpb commands are issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order: 7-1-3-5-0-4-2-6. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero the controller can issue per-bank REFRESH commands in any order as described in the previous paragraph.

An All Bank Refresh command issued when the bank counter is not zero will not increment the SDRAM's refresh counter. The required number of REFRESH Commands in a tREFW window must be satisfied excluding the above-mentioned All Bank Refresh Command.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- tRP has been satisfied after the prior PRECHARGE command to that bank.
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank.
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank.
- tRFCpb must be satisfied before issuing another REFpb command.

4.12 Refresh command (cont'd)

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.
- tRFCpb has been satisfied following the prior REFpb command.
- tRP has been satisfied following the prior PRECHARGE commands.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command.
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table 23 — REFRESH Command Scheduling Separation requirements

Symbol	Minimum Delay From	To	Notes
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb	1
		Activate command to different bank than prior Activate command	

NOTE 1 A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

4.12 Refresh command (cont'd)

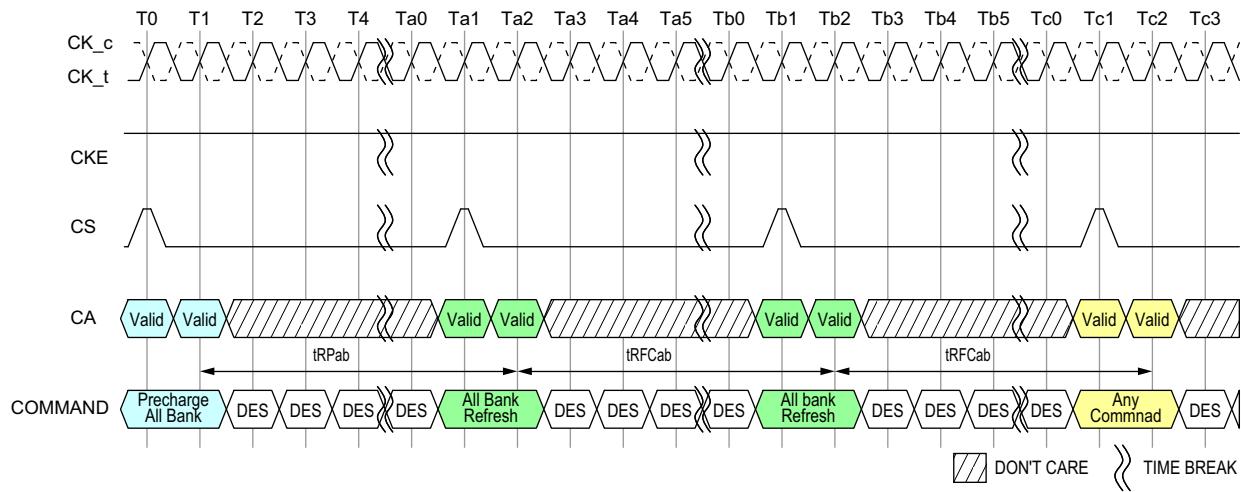


Figure 25 — All-Bank Refresh Operation

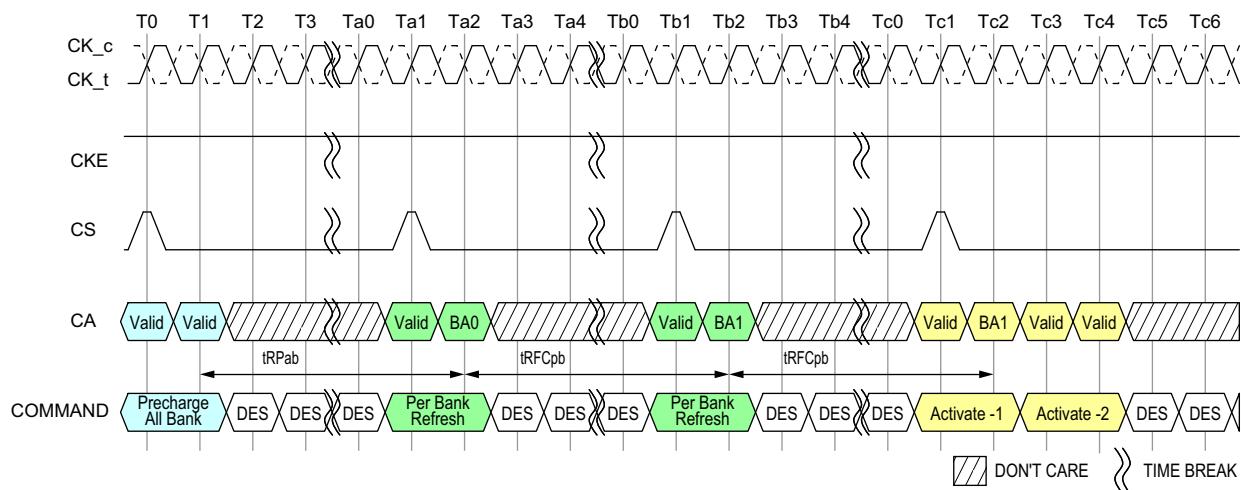


Figure 26 — Per-Bank Refresh Operation

In general, a Refresh command needs to be issued to the LPDDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in Table 24.

4.12 Refresh command (cont'd)

In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times tREFI$. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to $9 \times tREFI$. At any given time, a maximum of 16 REF commands can be issued within $2 \times tREFI$. Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REFcommands does not change.

Table 24 — Legacy Refresh Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab within max (2xtREFI x refresh rate multiplier, 16xtRFC)	Per-bank Refresh
000B	Low Temp. Limit	N/A	N/A	N/A	N/A
001B	4x tREFI	8	$9 \times 4 \times tREFI$	16	1/8 of REFab
010B	2x tREFI	8	$9 \times 2 \times tREFI$	16	1/8 of REFab
011B	1x tREFI	8	$9 \times tREFI$	16	1/8 of REFab
100B	0.5x tREFI	8	$9 \times 0.5 \times tREFI$	16	1/8 of REFab
101B	0.25x tREFI	8	$9 \times 0.25 \times tREFI$	16	1/8 of REFab
110B	0.25x tREFI	8	$9 \times 0.25 \times tREFI$	16	1/8 of REFab
111B	High Temp. Limit	N/A	N/A	N/A	N/A

Table 25 — Modified REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab within max (2xtREFI x refresh rate multiplier, 16xtRFC)	Per-bank Refresh
000B	Low Temp. Limit	N/A	N/A	N/A	N/A
001B	4x tREFI	2	$3 \times 4 \times tREFI$	4	1/8 of REFab
010B	2x tREFI	4	$5 \times 2 \times tREFI$	8	1/8 of REFab
011B	1x tREFI	8	$9 \times tREFI$	16	1/8 of REFab
100B	0.5x tREFI	8	$9 \times 0.5 \times tREFI$	16	1/8 of REFab
101B	0.25x tREFI	8	$9 \times 0.25 \times tREFI$	16	1/8 of REFab
110B	0.25x tREFI	8	$9 \times 0.25 \times tREFI$	16	1/8 of REFab
111B	High Temp. Limit	N/A	N/A	N/A	N/A

NOTE 1 For any thermal transition phase where Refresh mode is transitioned to either 2x tREFI or 4x tREFI, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.

NOTE 2 LPDDR4 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[2:0]. If shorter refresh period is applied, the corresponding requirements from Table apply. For example, when MR4 OP[2:0]=001B, controller can be in any refresh rate from 4xtREFI to 0.25x tREFI. When MR4 OP[2:0]=010B, the only prohibited refresh rate is 4x tREFI.

4.12 Refresh command (cont'd)

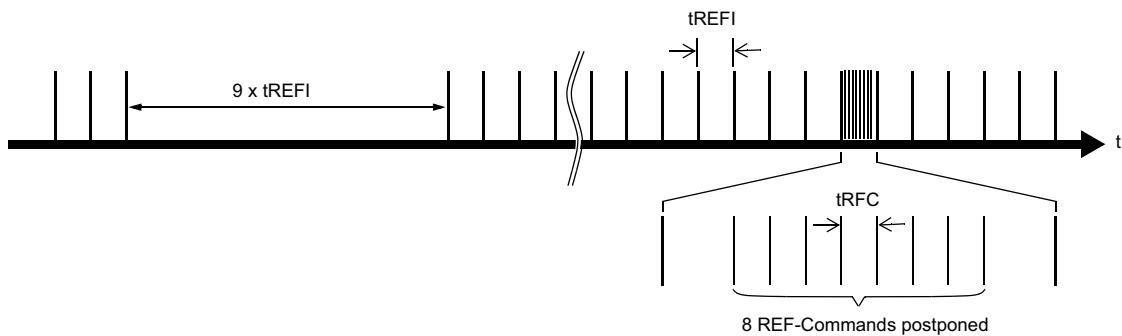


Figure 27 — Postponing Refresh Commands (Example)

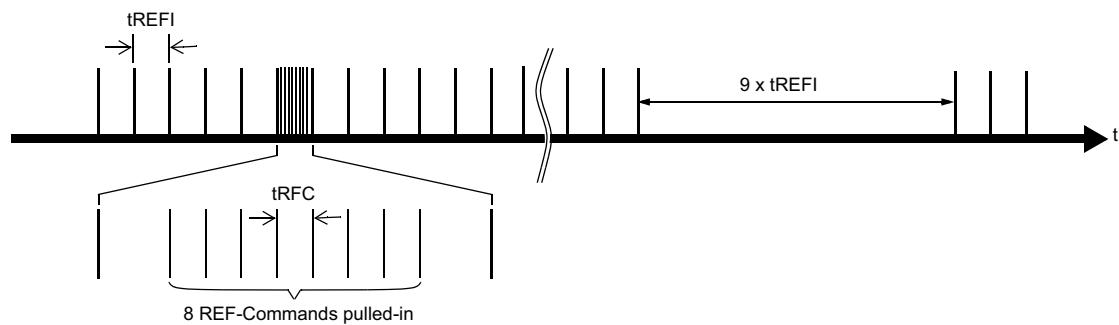


Figure 28 — Pulling-in Refresh Commands (Example)

4.12.1 Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Table 26 — Refresh Requirement Parameters per Die

Refresh Requirements		Symbol	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	Units
Density per Channel			2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	
Number of banks per channel			8			TBD	TBD	TBD	TBD	
Refresh Window (tREFW) (TCASE ≤ 85°C)		tREFW	32			TBD	TBD	TBD	TBD	ms
Refresh Window (tREFW) (1/2 Rate Refresh)		tREFW	16			TBD	TBD	TBD	TBD	ms
Refresh Window (tREFW) (1/4 Rate Refresh)		tREFW	8			TBD	TBD	TBD	TBD	ms
Required Number of REFRESH Commands in a tREFW window		R	8192			TBD	TBD	TBD	TBD	-
Average Refresh Interval (TCASE ≤ 85°C)	REFAB	tREFI	3.904			TBD	TBD	TBD	TBD	us
	REFPB	tREFIpb	488			TBD	TBD	TBD	TBD	ns
Average Refresh Interval (1/2 Rate Refresh)	REFAB	tREFI	1.953			TBD	TBD	TBD	TBD	us
	REFPB	tREFIpb	244			TBD	TBD	TBD	TBD	ns
Average Refresh Interval (1/4 Rate Refresh)	REFAB	tREFI	0.9765			TBD	TBD	TBD	TBD	us
	REFPB	tREFIpb	122			TBD	TBD	TBD	TBD	ns
Refresh Cycle Time (All Banks)		tRFCab	130	180	180	TBD		TBD	TBD	ns
Refresh Cycle Time (Per Bank)		tRFCpb	60	90	90	TBD		TBD	TBD	ns

NOTE 1 Refresh is defined with a 32ms window, which refreshes 1/2 of the channel (or die). The entire channel (or die) is refreshed every 64ms.

NOTE 2 Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

4.13 Self Refresh Operation

4.13.1 Self Refresh Entry and Exit

The Self Refresh command can be used to retain data in the LPDDR4 SDRAM, the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CKE High, CS High, CA0 Low, CA1 Low, CA2 Low; CA3 High; CA4 High, CA5 Valid (Valid that means it is Logic Level, High or Low) for the first rising edge and CKE High, CS Low, CA0 Valid, CA1 Valid, CA2 Valid, CA3 Valid, CA4 Valid, CA5 Valid at the second rising edge of the clock. Self Refresh command is only allowed when SDRAM is idle state.

During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated. SDRAM can accept the following commands, MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 except PASR Bank/Segment setting.

LPDDR4 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (V_{DD1} and V_{DD2}) must be at valid levels. V_{DDQ} may be turned off during Self-Refresh after t_{ESCKE} is satisfied (Refer to Figure 30 about t_{ESCKE}).

Prior to exiting Self-Refresh V_{DDQ} must be within specified limits. The minimum time that the SDRAM must remain in Self Refresh mode is $t_{SR,min}$.

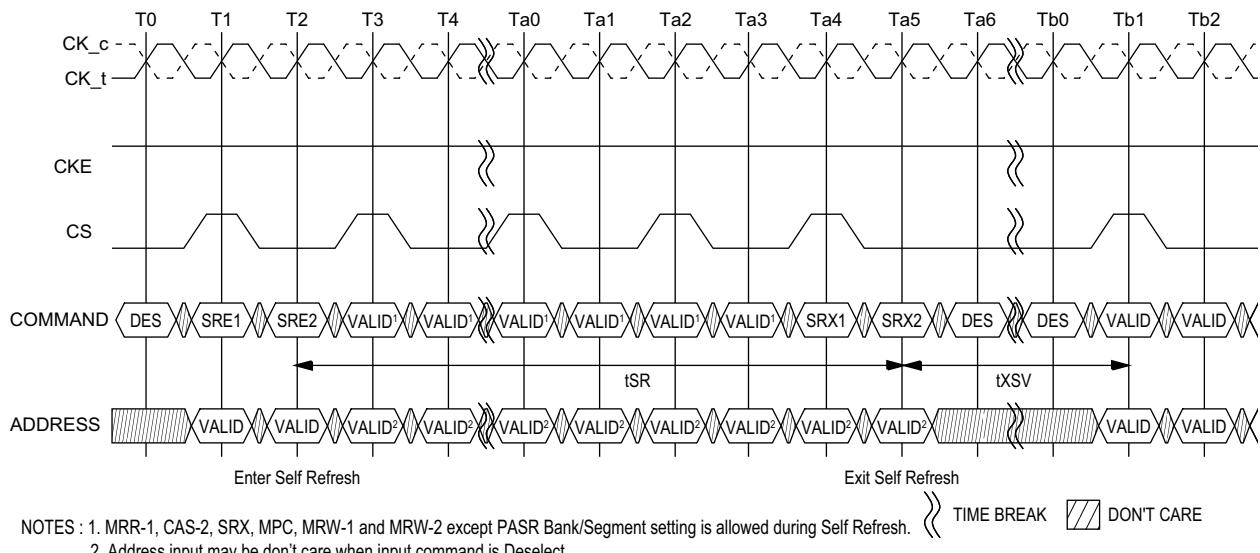
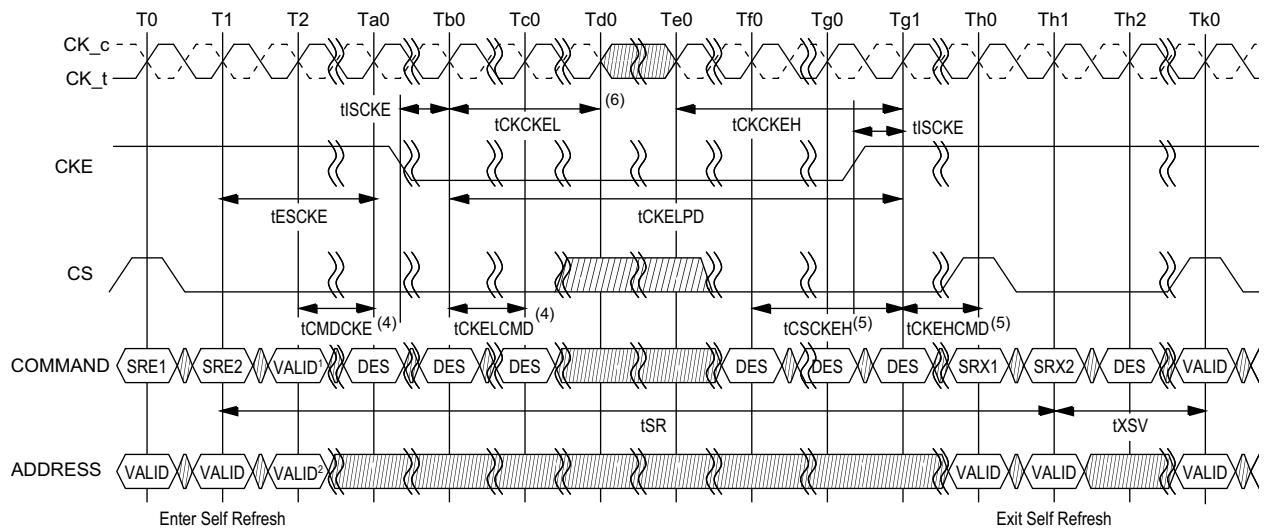


Figure 29 — Self Refresh Entry/Exit Timing

4.13.2 Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure 30.



NOTES : 1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Address input may be don't care when input command is Deselect.

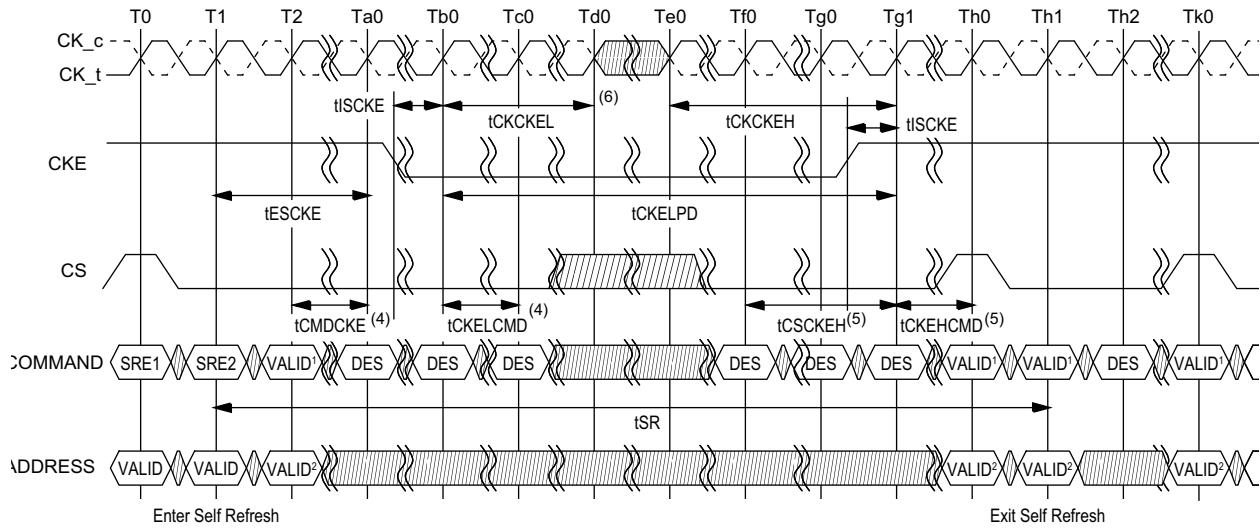
3. CS input must be low when input command is Deselect.
4. Deselect is only allowed during tCMDCKE(min) and tCKELCMD(min)
5. Deselect is only allowed during tCSCKEH(min) and tCKEHCMD(min)

6. The input clock frequency can be changed after tCKCKEL(min) satisfied.

Figure 30 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit

4.13.3 Command input Timing after Power Down Exit

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure 31.



- NOTES :
1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
 2. Address input may be don't care when input command is Deselect.
 3. CS input must be low when input command is Deselect.
 4. Deselect is only allowed during tCMDCKE(min) and tCKELCMD(min)
 5. Deselect is only allowed during tCSCKEH(min) and tCKEHCMD(min)
 6. The input clock frequency can be changed after tCKCKEL(min) satisfied.

}} TIME BREAK // DON'T CARE

Figure 31 — Command input timings after Power Down Exit during Self Refresh

4.13.4 Self Refresh AC Timing Table

Table 27 — Self Refresh AC Timing

Speed		LPDDR4-3200		DDR4-4266		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
CKE input setup time	tISCKE	TBD	-	TBD	-	nCK	
Valid Clock Requirement after CKE Input low	tCKCKEL	max(7.5ns, 3tCK)	-	max(7.5ns, 3tCK)	-	nCK	
Valid Clock Requirement before CKE Input High	tCKCCKEH	2tCK	-	2tCK	-	nCK	
Delay from SRE command to CKE Input low	tESCKE	2	-	2	-	nCK	
Delay from Valid command to CKE Input low	tCMDCKE	2	-	2	-	nCK	
CKE minimum pulse width	tCKELPD	max(7.5ns, 3tCK)	-	max(7.5ns, 3tCK)	-	nCK	
Valid Command Requirement after CKE Input low	tCKELCMD	max(7.5ns, 3tCK)	-	max(7.5ns, 3tCK)	-	nCK	
Valid Command Requirement after CKE Input High	tCKEHCMD	max(7.5ns, 3tCK)	-	max(7.5ns, 3tCK)	-	nCK	
Valid CS low Requirement before CKE Input High	tCSCCKEH	TBD	-	TBD	-	nCK	
Minimum Self Refresh Time	tSR	TBD	-	TBD	-	nCK	
Exit Self Refresh to Valid commands	tXSV	max(tRFCab + 7.5ns, 2nCK)	-	max(tRFCab + 7.5ns, 2nCK)	-	nCK	1

NOTE 1 MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.

4.14 Self Refresh Abort

If MR4 OP[3] is enabled then DRAM aborts any ongoing refresh during Self Refresh exit and does not increment the internal refresh counter. Controller can issue a valid command after a delay of tXSR_abort instead of tXSR.

The value of tXSR_abort(min) is defined as tRFCpb + TBD¹ns.

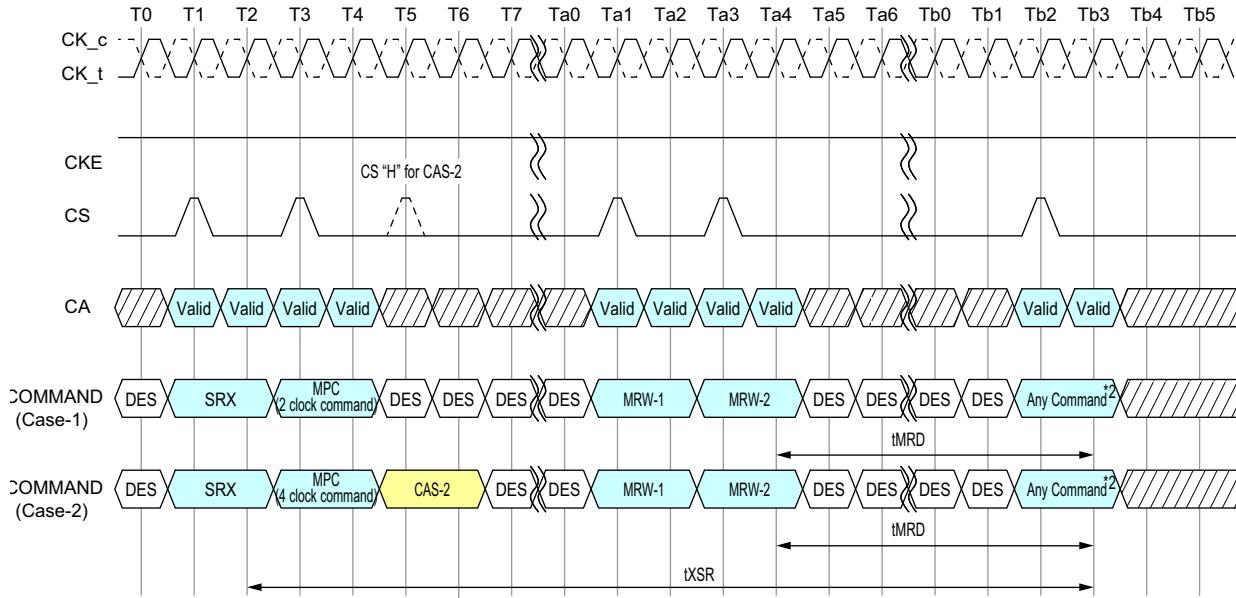
Upon exit from Self Refresh mode, the LPDDR4 SDRAM requires a minimum of one extra refresh (8 per bank or 1 all bank) before entry into a subsequent Self Refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

Self refresh abort feature is available for higher density devices starting with 12 Gb device.

1. As of publication of this document, under discussion by the formulating committee.

4.15 MRR, MRW, MPC Command during tXSR, tRFC

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tXSR period.



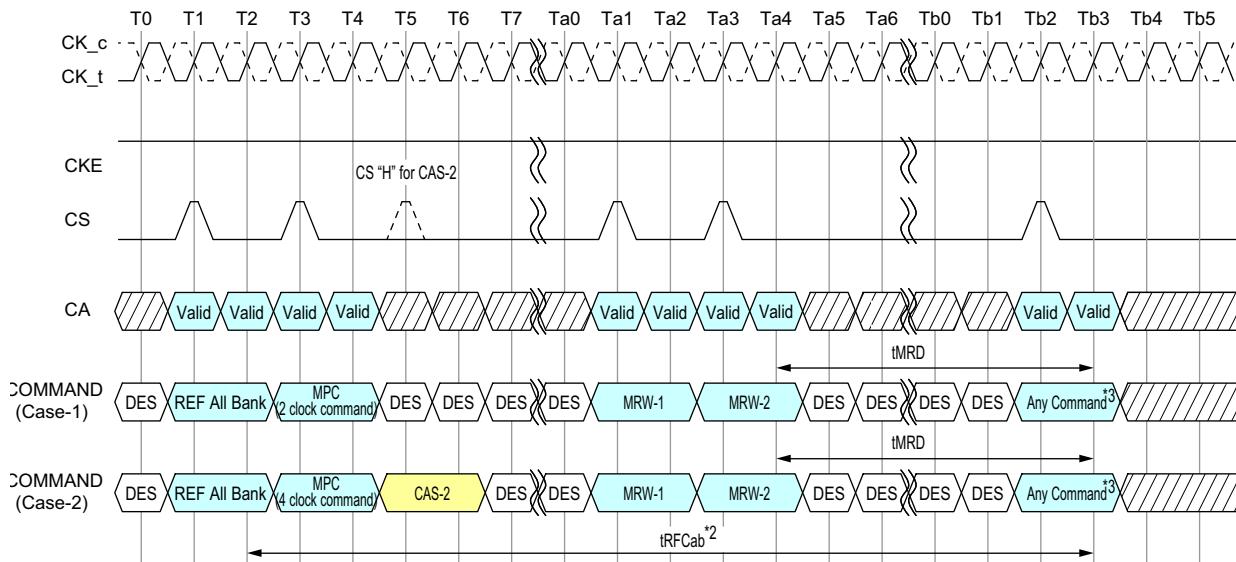
NOTES : 1. MPC and MRW command are shown in figure at this time, Any combination of MRR, MRW and MPC is allowed during tXSR period.

2. Any command also includes MRR, MRW and all MPC command.

DON'T CARE TIME BREAK

Figure 32 — MRR, MRW and MPC Commands Issuing Timing during tXSR

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tRFC period.



NOTES : 1. MPC and MRW command are shown in figure at this time, Any combination of MRR, MRW and MPC is allowed during tRFCab or tRFCpb period.

2. Refresh cycle time depends on Refresh command. In case of REF per Bank command issued, Refresh cycle time will be tRFCpb.

3. Any command also includes MRR, MRW and all MPC command.

DON'T CARE TIME BREAK

Figure 33 — MRR, MRW and MPC Commands Issuing Timing during tRFC

4.16 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4-SDRAM registers. The MRR command is initiated with CKE, CS and CA[5:0] in the proper state as defined by Table 63 — Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after RL + tCK + tDQSCK + tDQSQ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16.

MRR operation must not be interrupted.

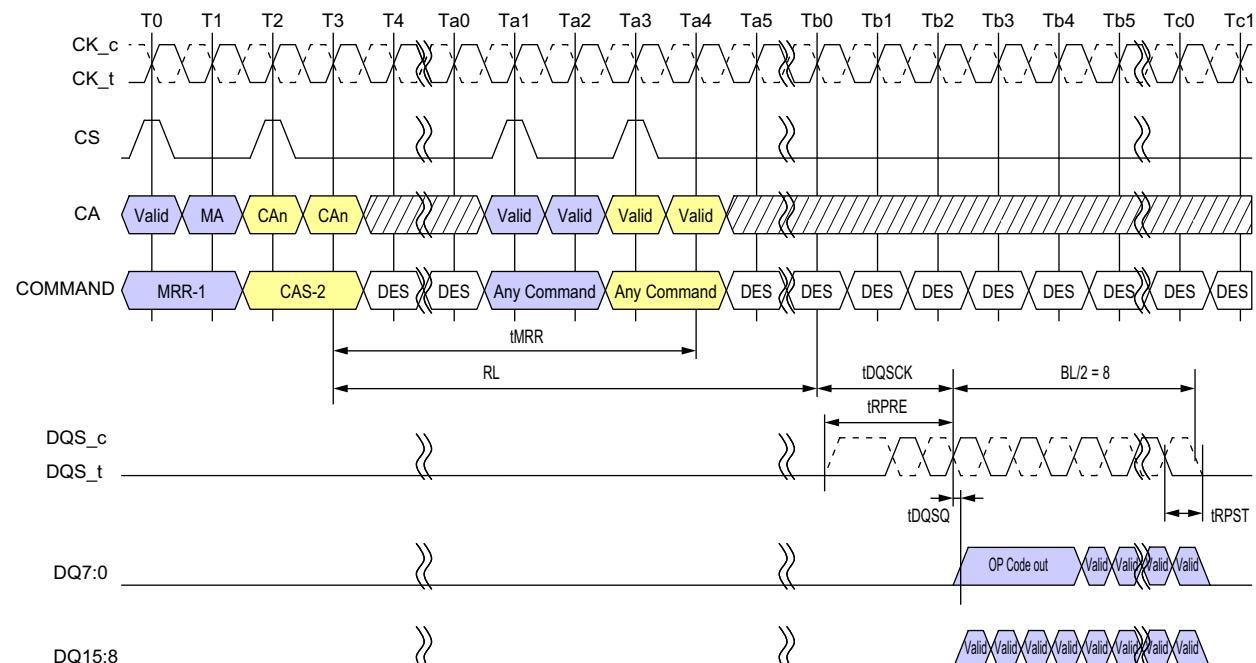
Table 28 — DQ output mapping

BL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0										V					
DQ1	OP1										V					
DQ2	OP2										V					
DQ3	OP3										V					
DQ4	OP4										V					
DQ5	OP5										V					
DQ6	OP6										V					
DQ7	OP7										V					
DBI0												V				

NOTE 1 MRR data are extended to first 4 UI's for DRAM controller to sample data easily.

NOTE 2 DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.

NOTE 3 The read pre-amble and post-amble of MRR are same as normal read.



Note

1. Only BL=16 is supported
2. Only DE-SELECT is allowed during tMRR period
3. DQ/DQS: VSSQ termination

DON'T CARE TIME BRAKE

Figure 34 — Mode Register Read Operation

4.17 Mode Register Write (MRW) Operation

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (see Table 63 — Command Truth Table). The mode register address and the data written to the mode registers is contained in CA[5:0] according to Table 63 — Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

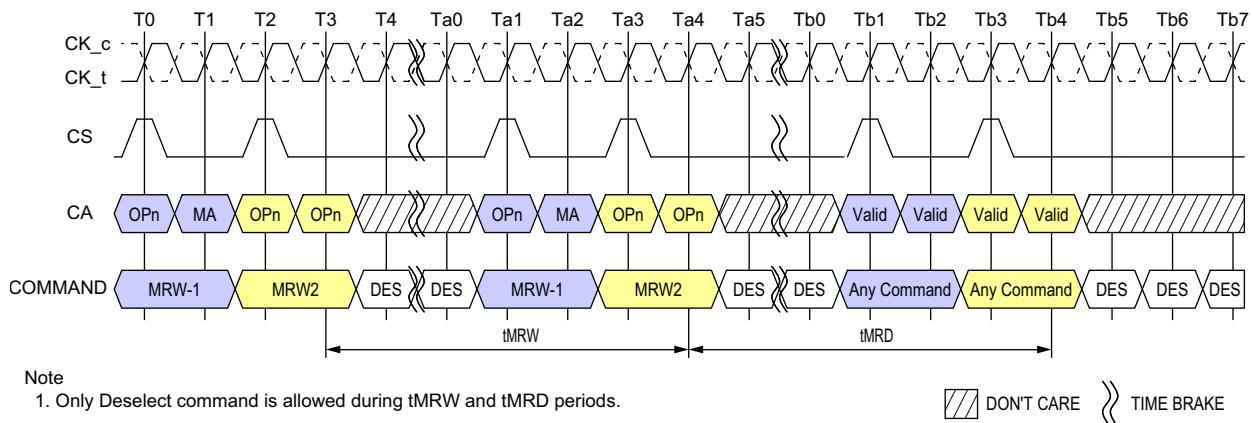


Figure 35 — Mode Register Write Timing

4.17.1 Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state.

Table 29 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State SDRAM	Command	Intermediate State	Next State SDRAM
		SDRAM	
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading	Bank(s) Active
	MRW	Mode Register Writing	Bank(s) Active

4.18 V_{REF} Current Generator (VRCG)

LPDDR4 SDRAM V_{REF} current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal V_{REF}(DQ) and V_{REF}(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown in Figure 36.

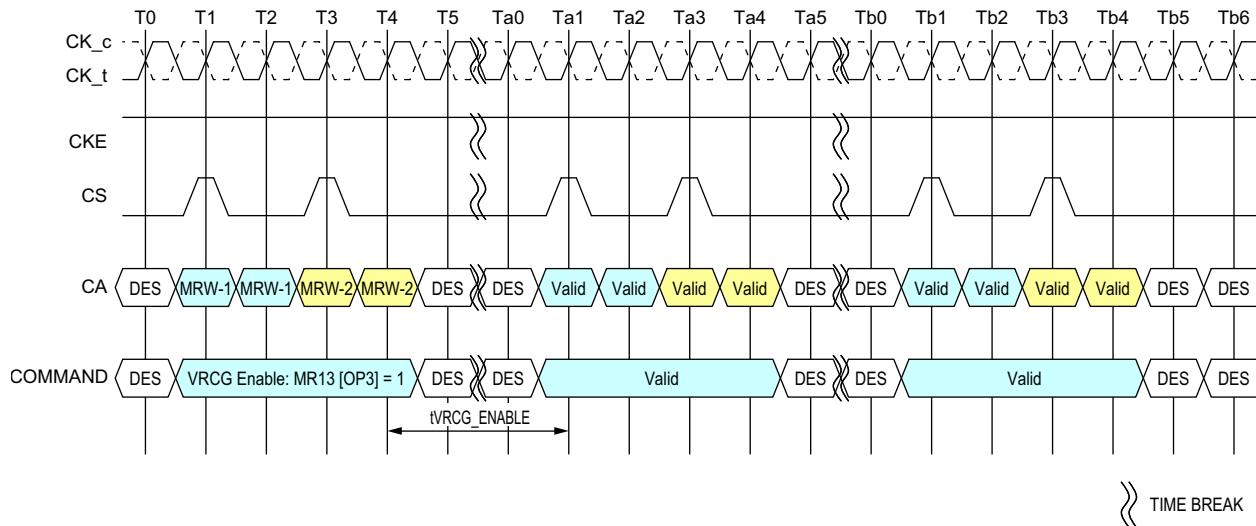


Figure 36 — VRCG Enable timing

VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown in Figure 37.

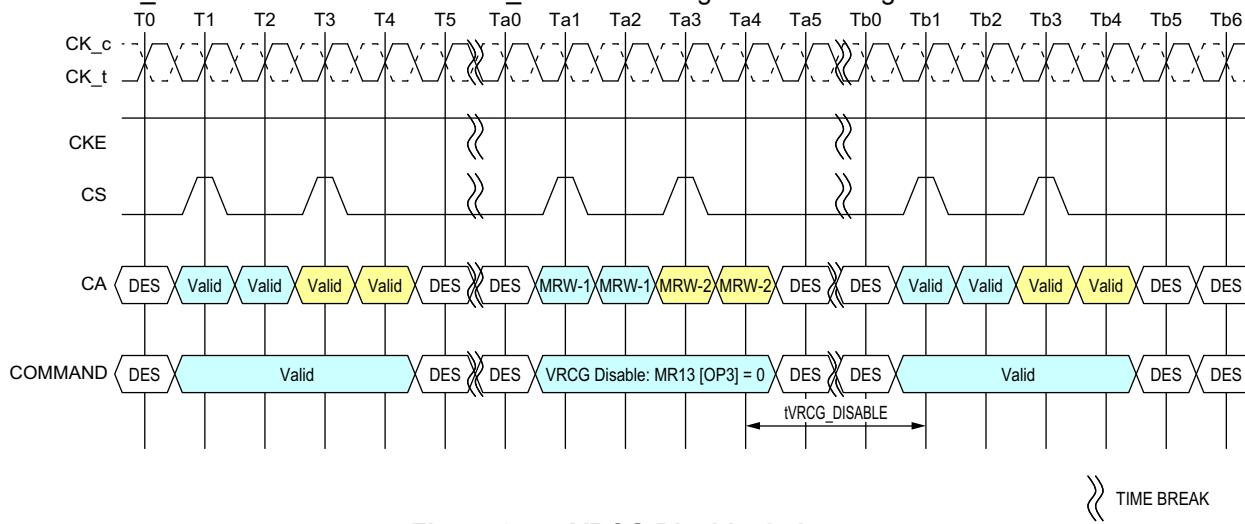


Figure 37 — VRCG Disable timing

Note that LPDDR4 SDRAM devices support V_{REF}(CA) and V_{REF}(DQ) range and value changes without enabling VRCG high current mode.

Table 30 — VRCG Enable/Disable Timing

Speed		533, 1066, 1600, 2133, 2667, 3200, 3733, 4267Mbps		Units	NOTE
Parameter	Symbol	MIN	MAX		
V _{REF} high current mode enable time	tVRCG_ENABLE	-	200	ns	
V _{REF} high current mode disable time	tVRCG_DISABLE	-	100	ns	

4.19 CA V_{REF} Training

The DRAM internal CA V_{REF} specification parameters are voltage operating range, stepsize, V_{REF} set tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 DRAM devices. The minimum range is defined by V_{REF}^{max} and V_{REF}^{min} as depicted in Figure 38.

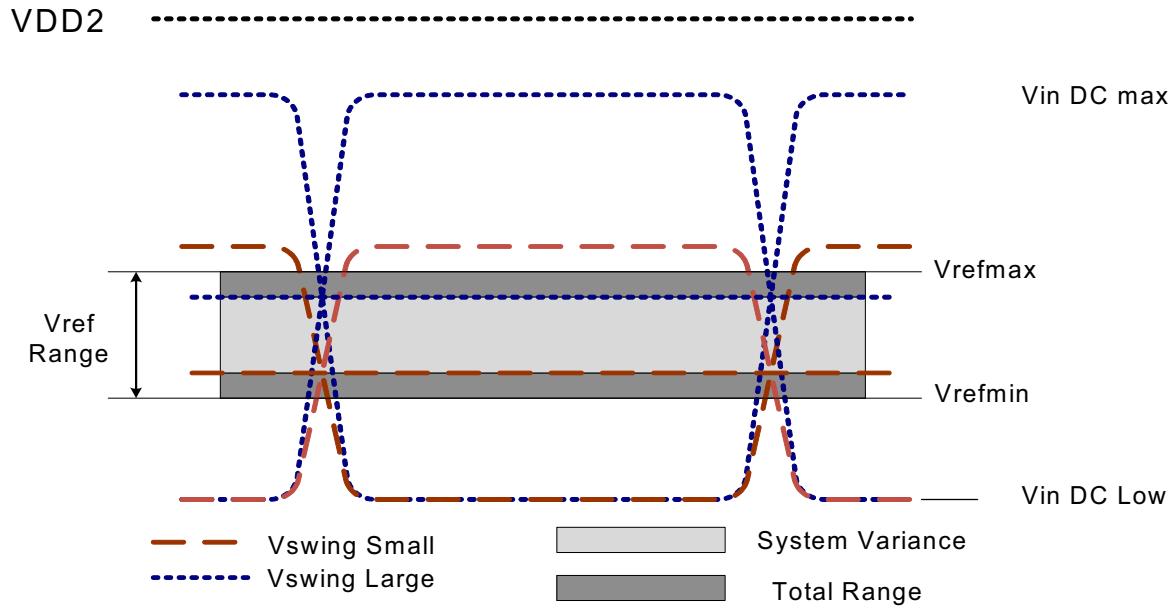


Figure 38 — V_{REF} operating range(V_{REF}^{min}, V_{REF}^{max})

4.19 CA V_{REF} Training (cont'd)

The V_{REF} stepsize is defined as the stepsize between adjacent steps. However, for a given design, DRAM has one value for V_{REF} step size that falls within the range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line which is based on the two endpoints.

Where the endpoints are at the min and max V_{REF} values for a specified range. An illustration depicting an example of the stepsize and V_{REF} set tolerance is shown in Figure 39.

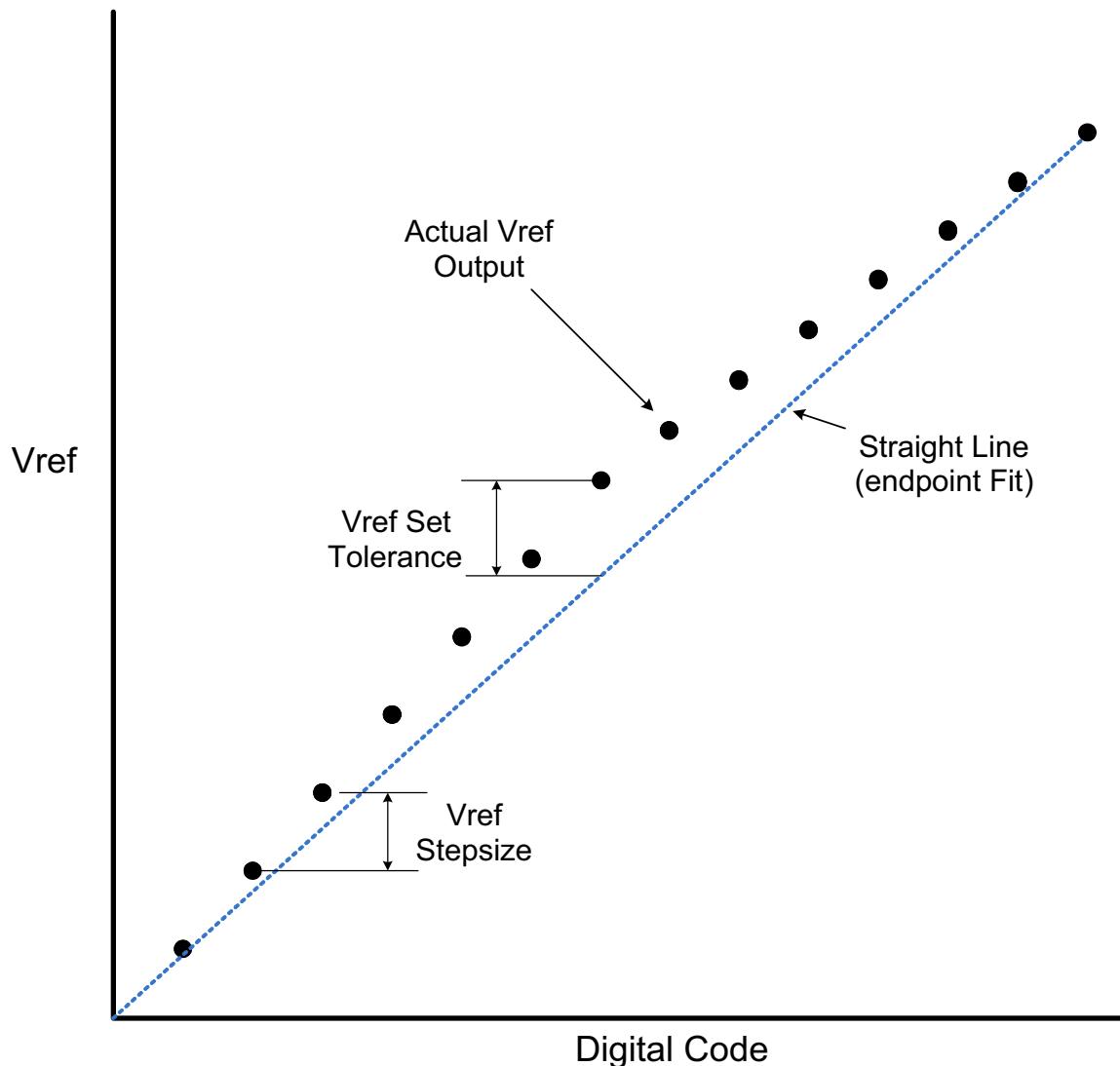


Figure 39 — Example of V_{REF} set tolerance(max case only shown) and stepsize

4.19 CA V_{REF} Training (cont'd)

The V_{REF} increment/decrement step times are defined by V_{REF_time-short}, V_{REF_time-Middle} and V_{REF_time-long}. The V_{REF_time-short}, V_{REF_time-Middle} and V_{REF_time-long} is defined from TS to TE as shown in Figure 40 where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance(V_{REF_val_tol}).

The V_{REF} valid level is defined by V_{REF_val} tolerance to qualify the step time TE as shown in Figure 40.

This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

V_{REF_time-Short} is for a single stepsize increment/decrement change in V_{REF} voltage.

V_{REF_time-Middle} is at least 2 stepsizes increment/decrement change within the same V_{REFCA} range in V_{REF} voltage.

V_{REF_time-Long} is the time including up to V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} change across the V_{REFCA} Range in V_{REF} voltage.

TS - is referenced to MRS command clock

TE - is referenced to the V_{REF_val_tol}

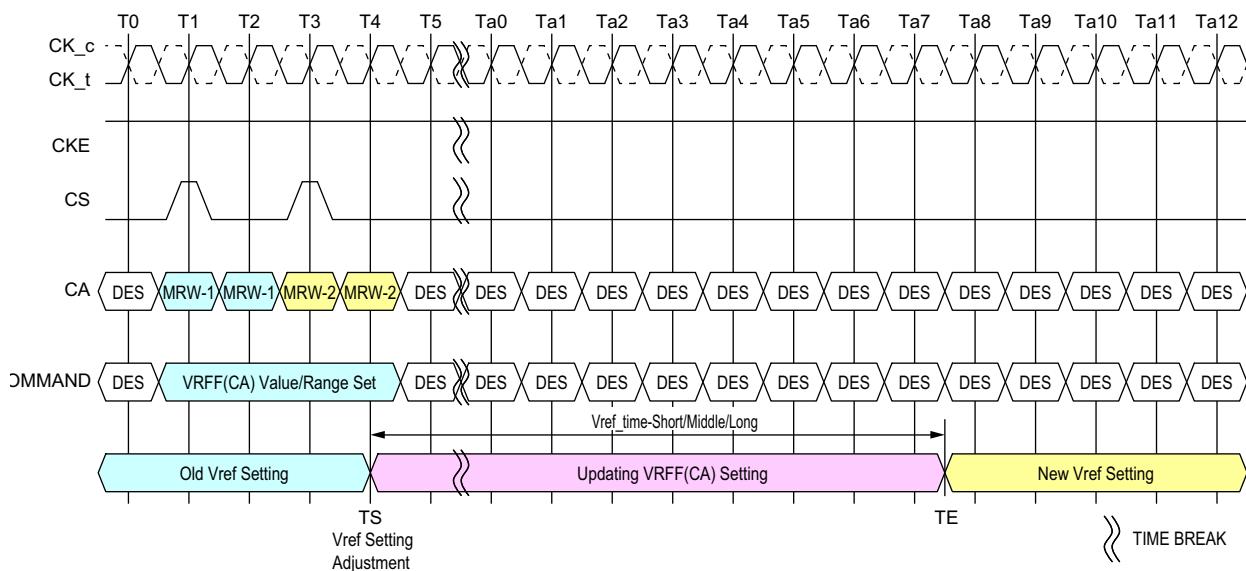


Figure 40 — V_{REF_time} for Short, Middle and Long Timing Diagram

The MRW command to the mode register bits are as follows.

MR12 OP[5:0] : V_{REF(CA)} Setting

MR12 OP[6] : V_{REF(CA)} Range

4.19 CA V_{REF} Training (cont'd)

The minimum time required between two V_{REF} MRS commands is V_{REF_time-short} for single step and V_{REF_time-Middle} for a full voltage range step.

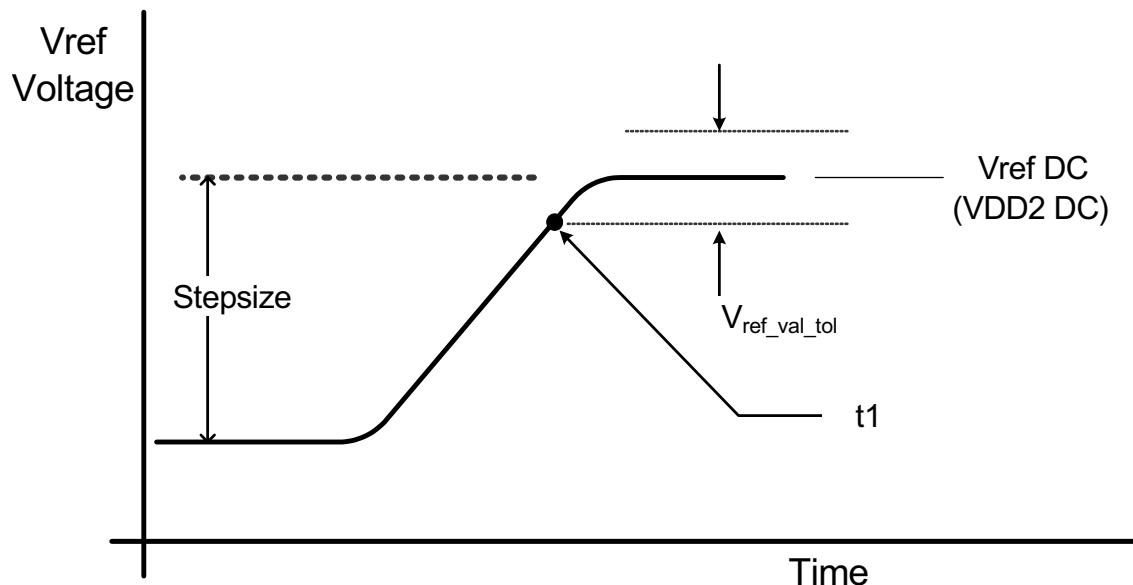


Figure 41 — V_{REF} step single stepsize increment case

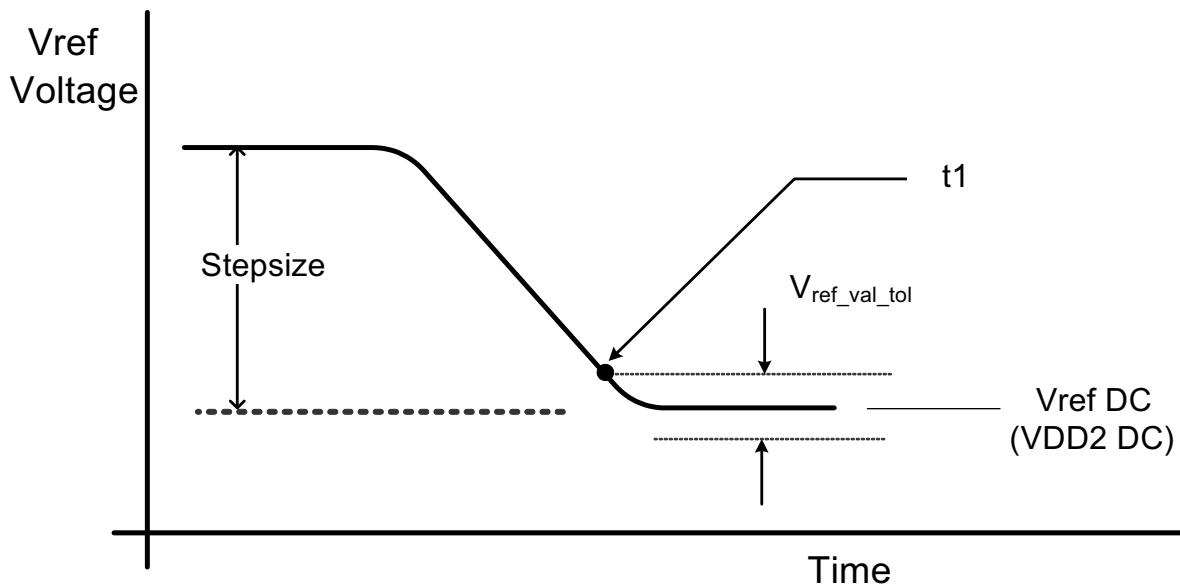


Figure 42 — V_{REF} step single stepsize decrement case

4.19 CA V_{REF} Training (cont'd)

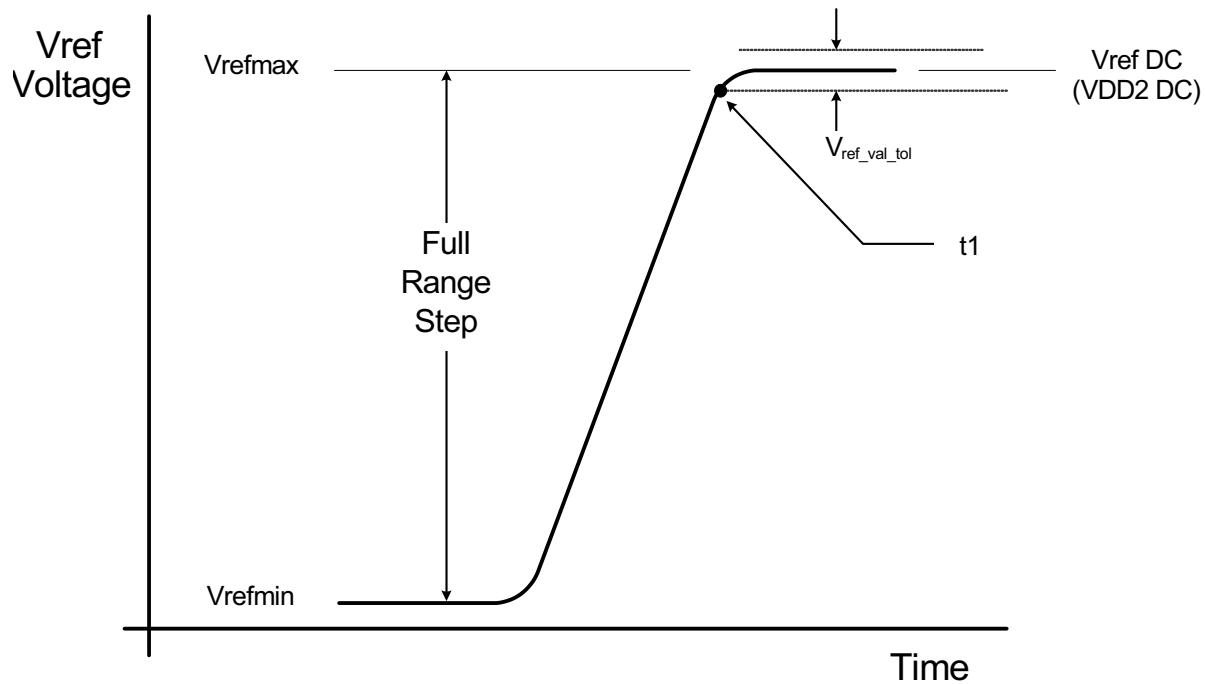


Figure 43 — V_{REF} full step from V_{REFmin} to V_{REFmax} case

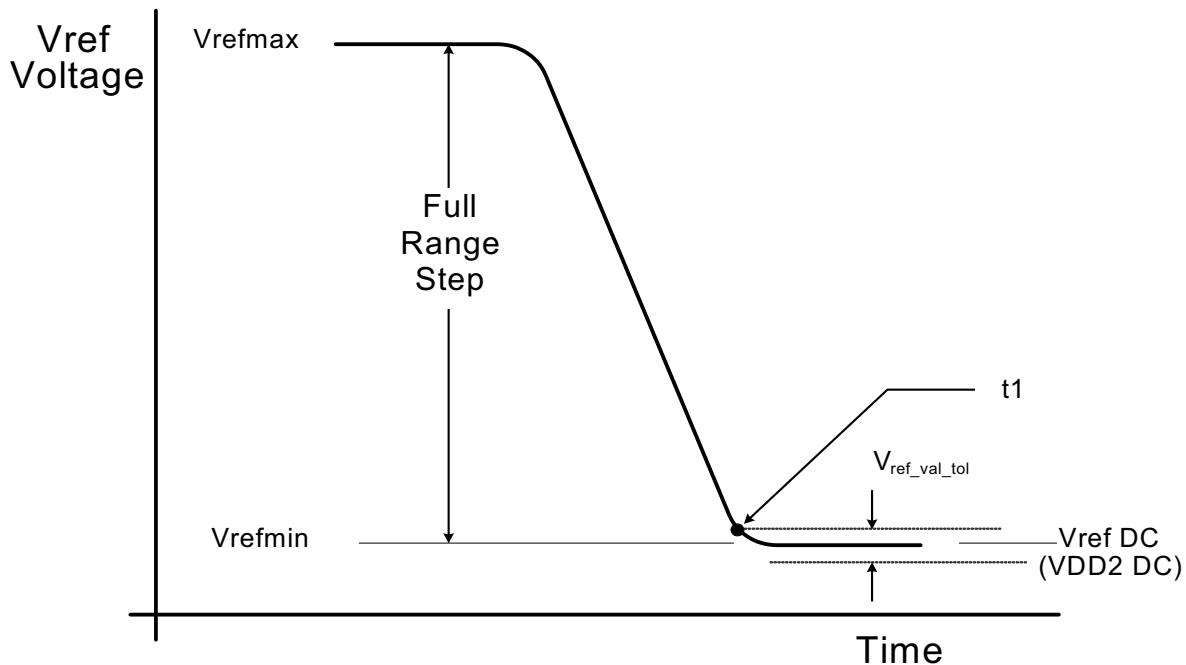


Figure 44 — V_{REF} full step from V_{REFmax} to V_{REFmin} case

4.19 CA V_{REF} Training (cont'd)

Table 31 contains the CA internal V_{REF} specifications that will be characterized at the component level for compliance. The component level characterization method is TBD¹.

Table 31 — CA Internal V_{REF} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
V _{REF} Max operating point Range0	V _{REF_max_R0}	30%	-	-	V _{DD2}	1,11
V _{REF} Min operating point Range0	V _{REF_min_R0}	-	-	10%	V _{DD2}	1,11
V _{REF} Max operating point Range1	V _{REF_max_R1}	42%	-	-	V _{DD2}	1,11
V _{REF} Min operating point Range1	V _{REF_min_R1}	-	-	22%	V _{DD2}	1,11
V _{REF} Stepsize	V _{REF_step}	0.30%	0.40%	0.50%	V _{DD2}	2
V _{REF} Set Tolerance	V _{REF_set_tol}	-1.00%	0.00%	1.00%	V _{DD2}	3,4,6
		-0.10%	0.00%	0.10%	V _{DD2}	3,5,7
V _{REF} Step Time	V _{REF_time-Short}	-	-	100	ns	8
	V _{REF_time_Middle}	-	-	200	ns	12
	V _{REF_time-Long}	-	-	250	ns	9
	V _{REF_time_weak}	-	-	1	ms	13,14
V _{REF} Valid tolerance	V _{REF_val_tol}	-0.10%	0.00%	0.10%	V _{DD2}	10

NOTE 1 V_{REF} DC voltage referenced to V_{DD2_DC}.

NOTE 2 V_{REF} stepsize increment/decrement range. V_{REF} at DC level.

NOTE 3 V_{REF_new} = V_{REF_old} + n*V_{REF_step}; n= number of steps; if increment use "+"; If decrement use "-".

NOTE 4 The minimum value of V_{REF} setting tolerance = V_{REF_new} - 1.0%*V_{DD2}. The maximum value of V_{REF} setting tolerance = V_{REF_new} + 1.0%*V_{DD2}. For n>4.

NOTE 5 The minimum value of V_{REF} setting tolerance = V_{REF_new} - 0.10%*V_{DD2}. The maximum value of V_{REF} setting tolerance = V_{REF_new} + 0.10%*V_{DD2}. For n≤ 4.

NOTE 6 Measured by recording the min and max values of the V_{REF} output over the range, drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 7 Measured by recording the min and max values of the V_{REF} output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for V_{REF}.

NOTE 9 Time from MRS command to increment or decrement V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} change across the V_{REF}CA Range in V_{REF} voltage.

NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.

NOTE 11 DRAM range 0 or 1 set by MR12 OP[6].

NOTE 12 Time from MRS command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same V_{REF}CA range.

NOTE 13 Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.

NOTE 14 V_{REF_time_weak} covers all V_{REF}(CA) Range and Value change conditions are applied to V_{REF_time_Short/Middle/Long}.

1. As of publication of this document, under discussion by the formulating committee.

4.20 DQ V_{REF} Training

The DRAM internal DQ V_{REF} specification parameters are voltage operating range, stepsize, V_{REF} set tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 DRAM devices. The minimum range is defined by V_{REF}max and V_{REF}min as depicted in Figure 45.

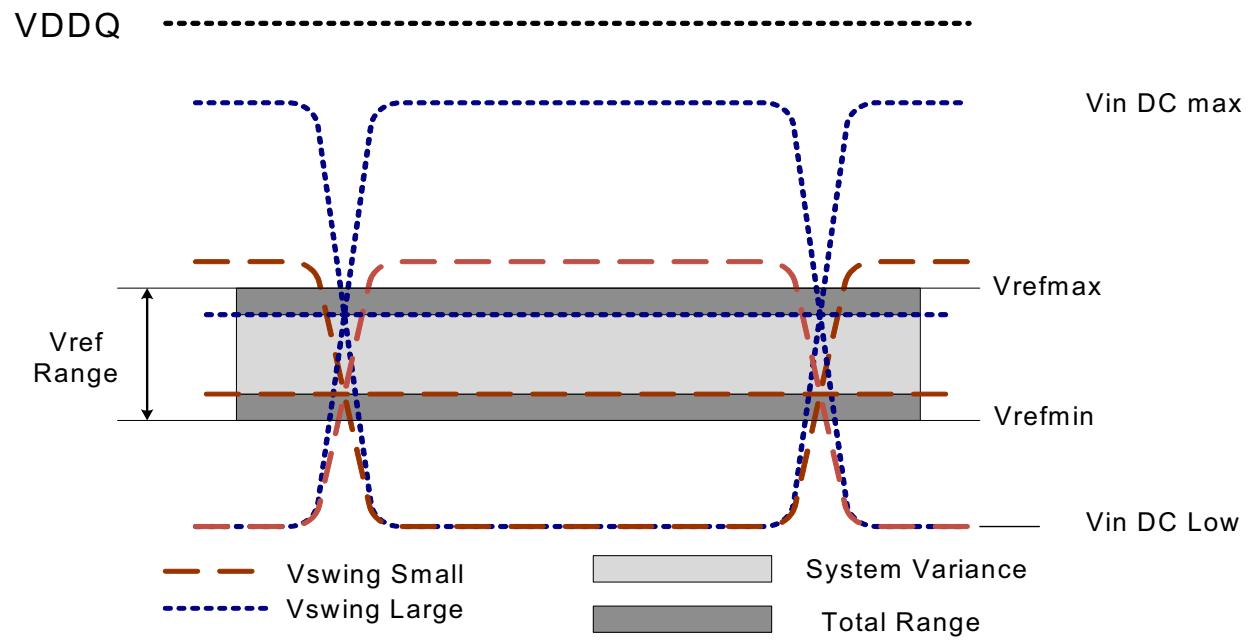


Figure 45 — V_{REF} operating range(V_{REF}min, V_{REF}max)

4.20 DQ V_{REF} Training (cont'd)

The V_{REF} stepsize is defined as the stepsize between adjacent steps. However, for a given design, DRAM has one value for V_{REF} step size that falls within the range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line which is based on the two endpoints.

Where the endpoints are at the min and max V_{REF} values for a specified range. An illustration depicting an example of the stepsize and V_{REF} set tolerance shown in Figure 46.

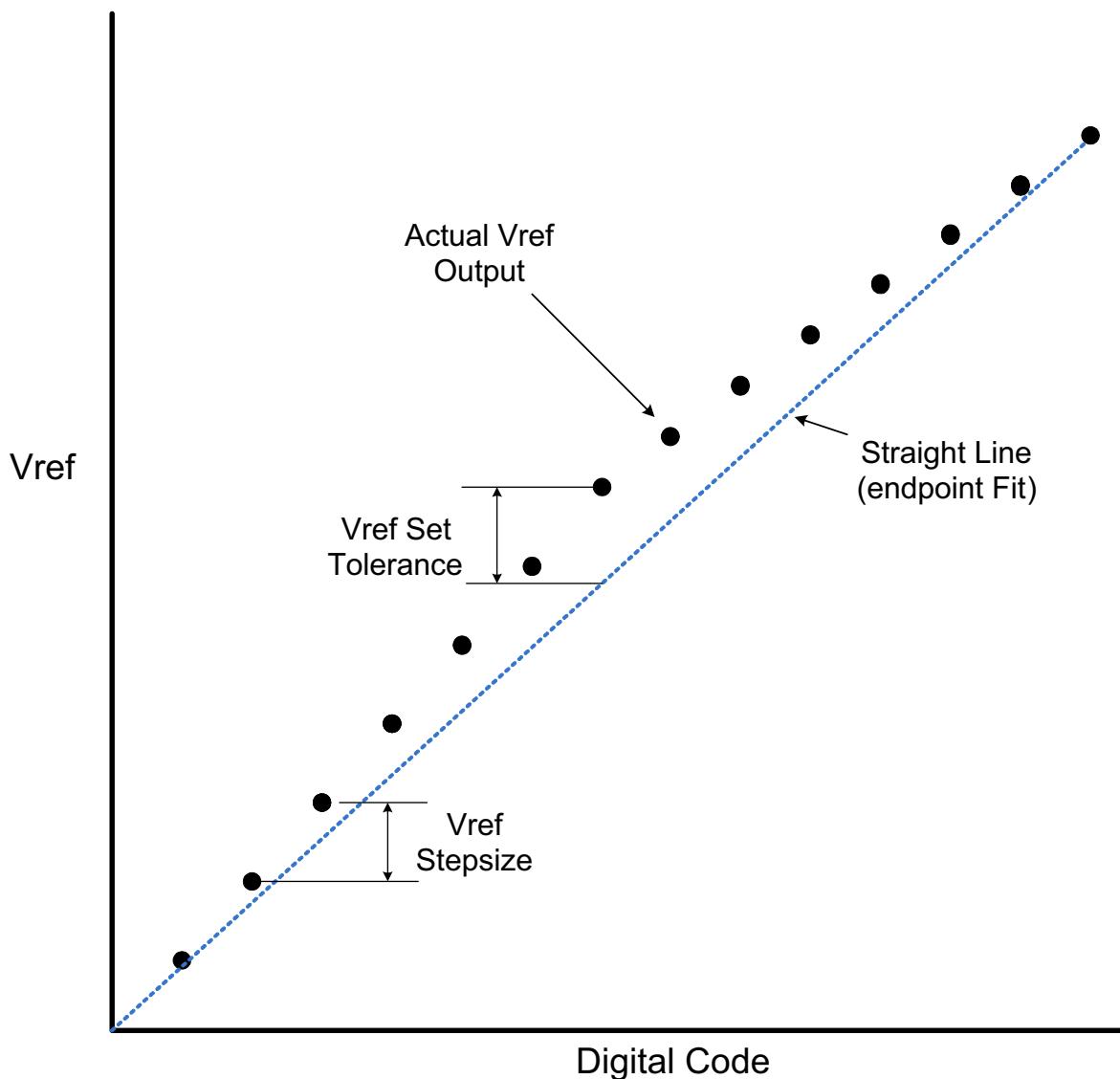


Figure 46 — Example of V_{REF} set tolerance(max case only shown) and stepsize

4.20 DQ V_{REF} Training (cont'd)

The V_{REF} increment/decrement step times are define by V_{REF_time-short}, Middle and long. The V_{REF_time-short}, V_{REF_time-Middle} and V_{REF_time-long} is defined from TS to TE as shown in Figure 47 where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance(V_{REF_val_tol}).

The V_{REF} valid level is defined by V_{REF_val} tolerance to qualify the step time TE as shown in Figure 47. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characerization.

V_{REF_time-Short} is for a single stepsize increment/decrement change in V_{REF} voltage.

V_{REF_time-Middle} is at least 2 stepsizes increment/decrement change within the same V_{REF}DQ range in V_{REF} voltage.

V_{REF_time-Long} is the time including up to V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} change across the V_{REF}DQ Range in Vref voltage.

TS - is referenced to MRS command clock

TE - is referenced to the V_{REF_val_tol}

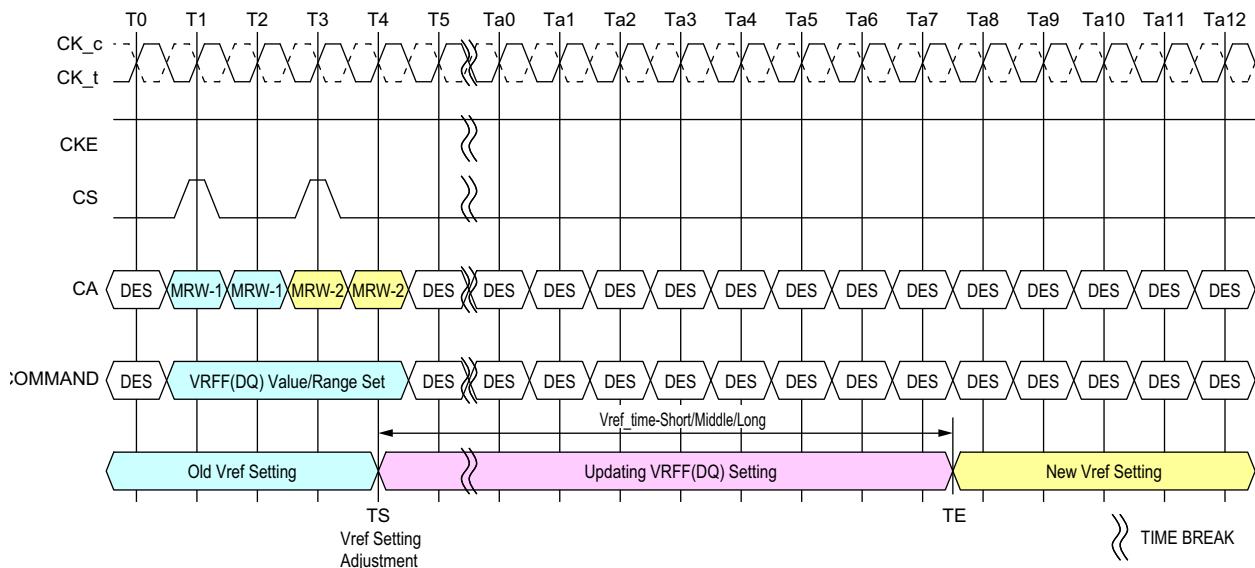


Figure 47 — V_{REF_time} for Short, Middle and Long Timing Diagram

The MRW command to the mode register bits are as follows.

MR14 OP[5:0] : V_{REF}(DQ) Setting

MR14 OP[6] : V_{REF}(DQ) Range

4.20 DQ V_{REF} Training (cont'd)

The minimum time required between two V_{REF} MRS commands is V_{REF_time-short} for single step and V_{REF_time-Middle} for a full voltage range step.

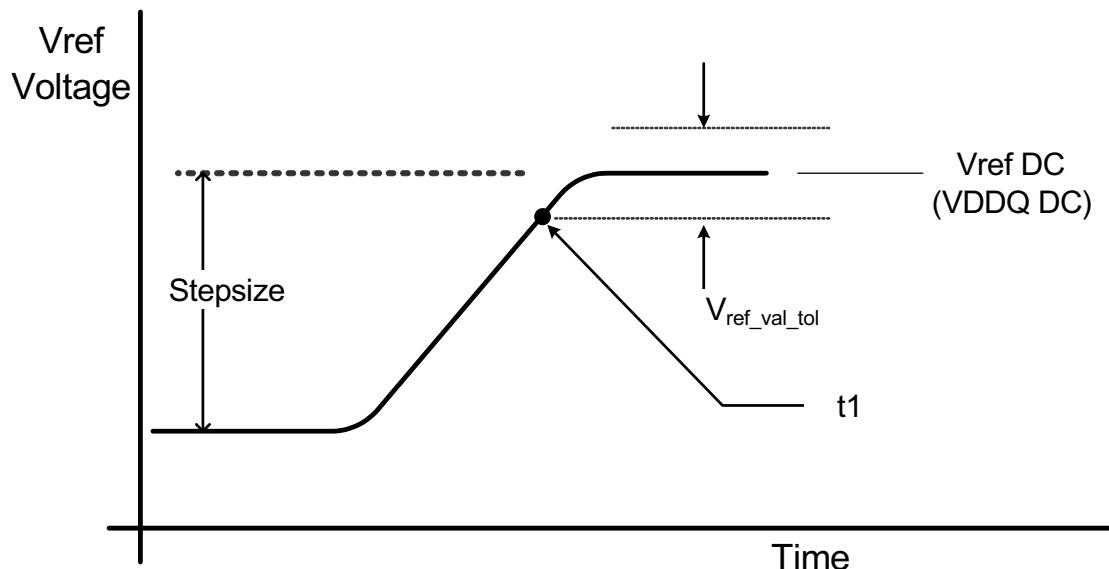


Figure 48 — V_{REF} step single stepsize increment case

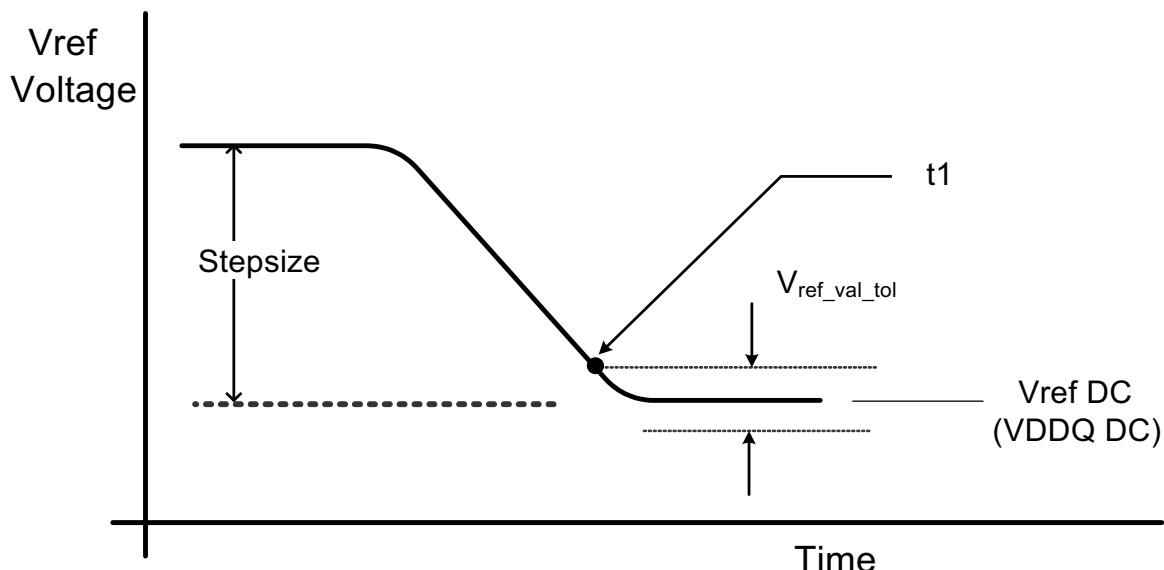


Figure 49 — V_{REF} step single stepsize decrement case

4.20 DQ V_{REF} Training (cont'd)

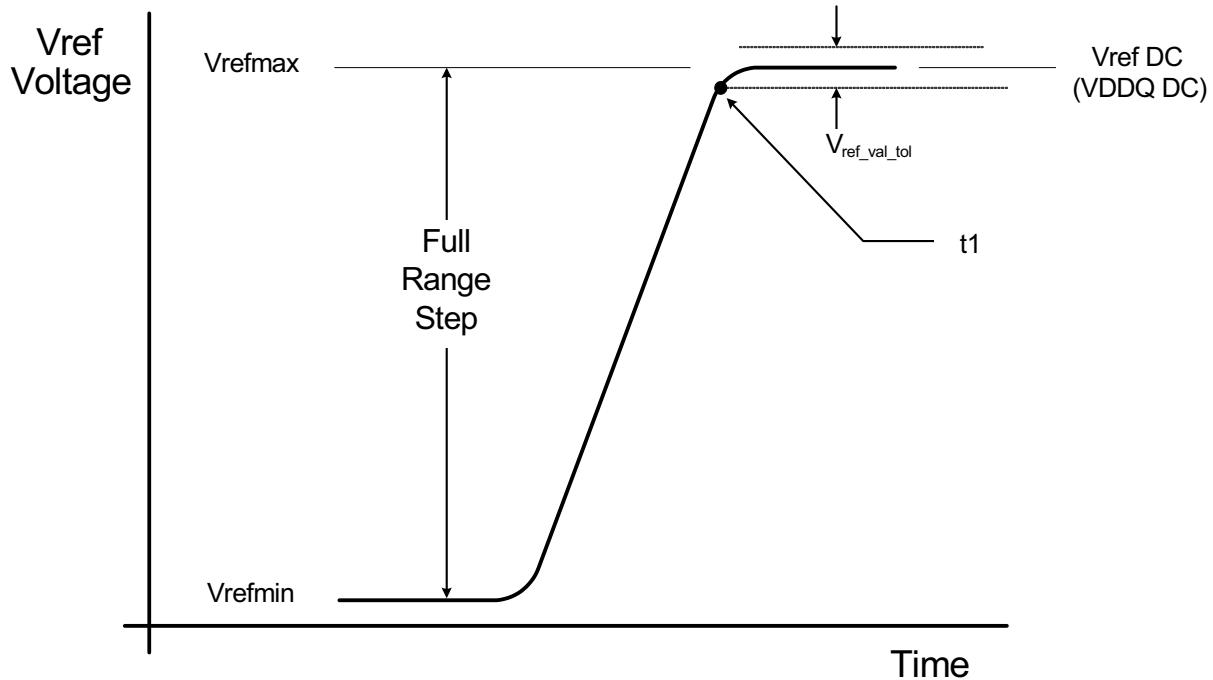


Figure 50 — V_{REF} full step from V_{REF}min to V_{REF}max case

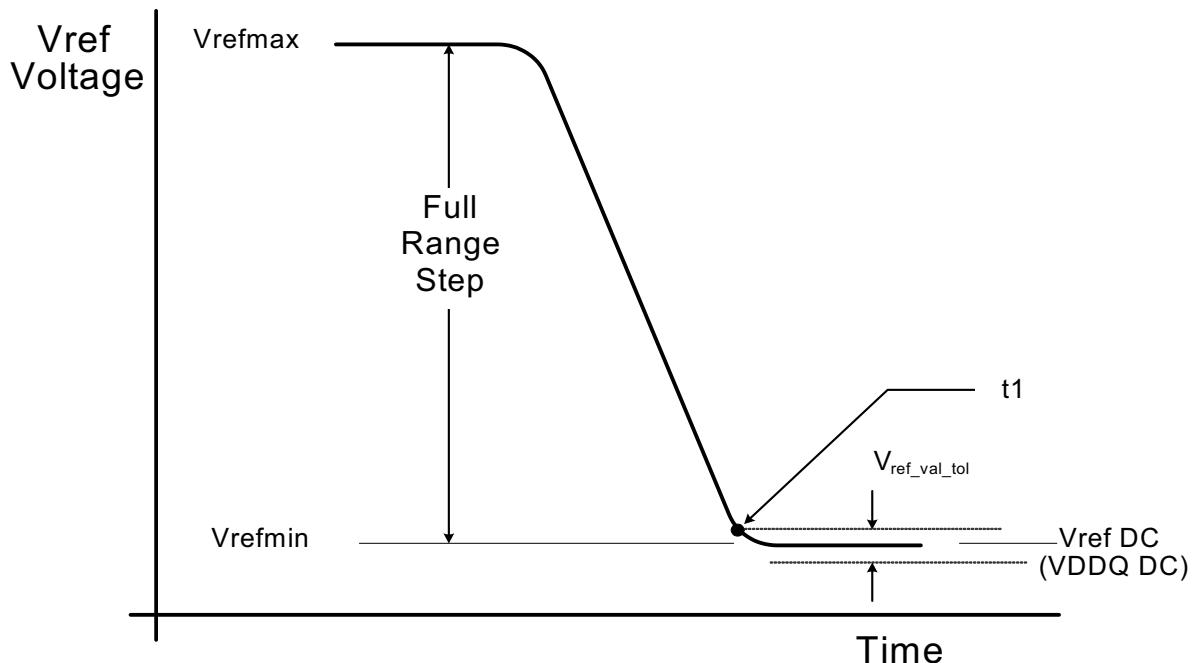


Figure 51 — V_{REF} full step from V_{REF}max to V_{REF}min case

4.20 DQ V_{REF} Training (cont'd)

Table 32 contains the DQ internal V_{REF} specifications that will be characterized at the component level for compliance. The component level characterization method is TBD¹.

Table 32 - DQ Internal V_{REF} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
V _{REF} Max operating point Range0	V _{REF_max_R0}	30%	-	-	V _{DDQ}	1,11
V _{REF} Min operating point Range0	V _{REF_min_R0}	-	-	10%	V _{DDQ}	1,11
V _{REF} Max operating point Range1	V _{REF_max_R1}	42%	-	-	V _{DDQ}	1,11
V _{REF} Min operating point Range1	V _{REF_min_R1}	-	-	22%	V _{DDQ}	1,11
V _{REF} Stepsize	V _{REF_step}	0.30%	0.40%	0.50%	V _{DDQ}	2
V _{REF} Set Tolerance	V _{REF_set_tol}	-1.00%	0.00%	1.00%	V _{DDQ}	3,4,6
		-0.10%	0.00%	0.10%	V _{DDQ}	3,5,7
V _{REF} Step Time	V _{REF_time-Short}	-	-	100	ns	8
	V _{REF_time_Middle}	-	-	200	ns	12
	V _{REF_time-Long}	-	-	250	ns	9
	V _{REF_time_weak}	-	-	1	ms	13,14
V _{REF} Valid tolerance	V _{REF_val_tol}	-0.10%	0.00%	0.10%	V _{DDQ}	10

NOTE 1 V_{REF} DC voltage referenced to V_{DDQ_DC}.

NOTE 2 V_{REF} stepsize increment/decrement range. V_{REF} at DC level.

NOTE 3 V_{REF_new} = V_{REF_old} + n*V_{REF_step}; n= number of steps; if increment use "+"; If decrement use "-".

NOTE 4 The minimum value of V_{REF} setting tolerance = V_{REF_new} - 1.0%*V_{DDQ}. The maximum value of V_{REF} setting tolerance = V_{REF_new} + 1.0%*V_{DDQ}. For n>4.

NOTE 5 The minimum value of V_{REF} setting tolerance = V_{REF_new} - 0.10%*V_{DDQ}. The maximum value of V_{REF} setting tolerance = V_{REF_new} + 0.10%*V_{DDQ}. For n< 4.

NOTE 6 Measured by recording the min and max values of the V_{REF} output over the range, drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 7 Measured by recording the min and max values of the V_{REF} output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for V_{REF}.

NOTE 9 Time from MRS command to increment or decrement V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} change across the V_{REFDQ} Range in V_{REF} voltage.

NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.

NOTE 11 DRAM range 0 or 1 set by MR14 OP[6].

NOTE 12 Time from MRS command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same V_{REFDQ} range.

NOTE 13 Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.

NOTE 14 V_{REF_time_weak} covers all V_{REF(DQ)} Range and Value change conditions are applied to V_{REF_time_Short/Middle/Long}.

1. As of publication of this document, under discussion by the formulating committee.

4.21 Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination for high-frequency operation. LPDDR4 provides an internal $V_{REF}(ca)$ that defaults to a level suitable for un-terminated, low-frequency operation, but the $V_{REF}(ca)$ must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal $V_{REF}(ca)$ in the CData eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

NOTE It is up to the system designer to determine what constitutes “low-frequency” and “high-frequency” based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the SDRAM before Command Bus Training is executed.

The LPDDR4-SDRAM die has a bond-pad (ODT-CA) for multi-rank operation. In a multi-rank system, the terminating rank should be trained first, followed by the nonterminating rank(s). See 4.33.1, ODT Mode Register, and Table 55 for more information.

The LPDDR4-SDRAM uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1B (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4-SDRAM will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See Figure 52, Note 6 for more information on FSP-OP register sets).

Upon training exit when CKE is driven HIGH, the LPDDR4-SDRAM will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the “known-good” state that was operating prior to training. The training values for $V_{REF}(ca)$ are not retained by the DRAM in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1B (Command Bus Training Mode Enabled).
2. After time tMRD, CKE may be set LOW, causing the LPDDR4-SDRAM to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode.

A status of DQS_t, DQS_c, DQ and DMI are as follows, and DQ ODT state will be followed Frequency Set Point function except output pins.

- DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by its toggling.
- DQ[5:0] become input pins for setting $V_{REF}(ca)$ Level.
- DQ[6] becomes a input pin for setting $V_{REF}(ca)$ Range.
- DQ[7] and DMI[0] become input pins and their input level is Valid level or floating, either way is fine.
- DQ[13:8] become output pins to feedback its capturing value via command bus by CS signal.
- DQS_t[1], DQS_c[1], DMI[1] and DQ[15:14] become output pins or disable, it means that SDRAM may drive to a valid level or left floating.

3. At time tCAENT later, LPDDR4 SDRAM can accept to change its VFREF(ca) Range and Value using input signals of DQS_t[0], DQS_c[0] and DQ[6:0] from existing value that's setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown in Table 33. At least one V_{REF} CA setting is required before proceeding to next training steps.

4.21 Command Bus Training (cont'd)

Table 33 — Mapping of MR12 OP Code and DQ Numbers

MR12 OP Code	Mapping							
	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	

4. The new $V_{REF}(ca)$ value must “settle” for time tV_{REF_LONG} before attempting to latch CA information.
5. To verify that the receiver has the correct $V_{REF}(ca)$ setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
6. To exit Command Bus Training mode, drive CKE HIGH, and after time tV_{REF_LONG} issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0B. After time $tMRW$ the LPDDR4-SDRAM is ready for normal operation. After training exit the LPDDR4-SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be executed from IDLE or Self Refresh states. When executing CBT within the Self Refresh state, the SDRAM must not be a power down state (i.e., CKE must be HIGH prior to training entry). Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

4.21.1 Training Sequence for single-rank systems

NOTE An example shown here is assuming an initial low-frequency, no-terminating operating point, training a high-frequency, terminating operating point. The **green text** is low-frequency, the **magenta text** is high-frequency. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point ‘y’ (FSP-WR[y]) (or FSP-OP[x], See note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
4. Drive CKE LOW, **and change CK frequency to the high-frequency operating point**.
5. Perform Command Bus Training ($V_{REF}ca$, CS, and CA).
6. **Exit training**, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
7. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, **and change CK frequency to the high frequency operating point**. At this point the Command Bus is trained and you may proceed to other training or normal operation.

4.21.2 Training Sequence for multi-rank systems

NOTE An example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The green text is low-frequency, the magenta text is high-frequency. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up high frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (V_{REFca} , CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (V_{REFca} , CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

4.21.3 Relation between CA input pin DQ output pin.

The relation between CA input pin DQ output pin is shown in Table 34.

Table 34 - Mapping of CA Input pin and DQ Output pin

	Mapping					
CA Number	CA5	CA4	CA3	CA2	CA1	CA0
DQ Number	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

4.21.4 Timing Diagram

The basic Timing diagrams of Command Bus Training are shown in Figure 52 through Figure 55.

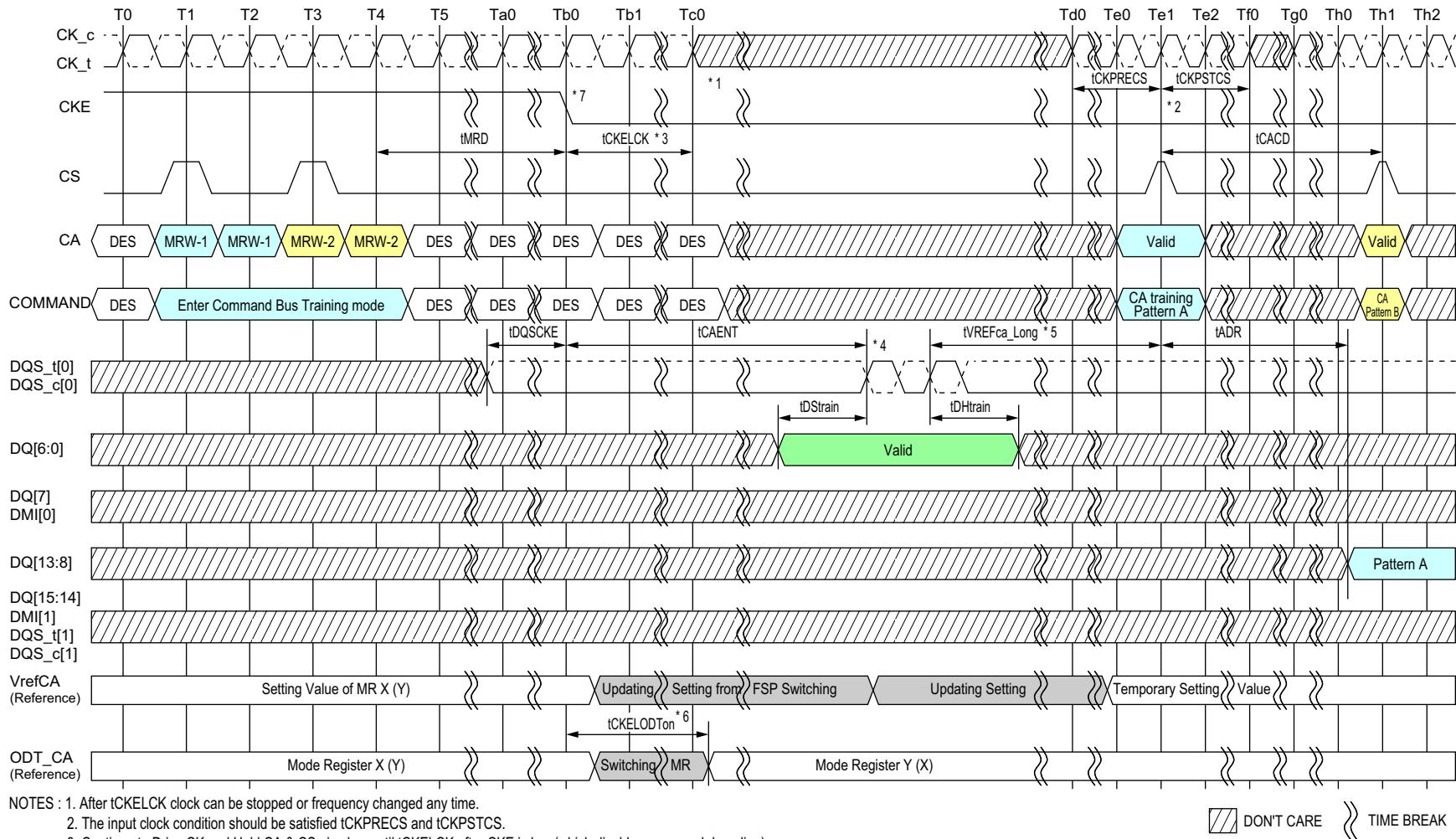
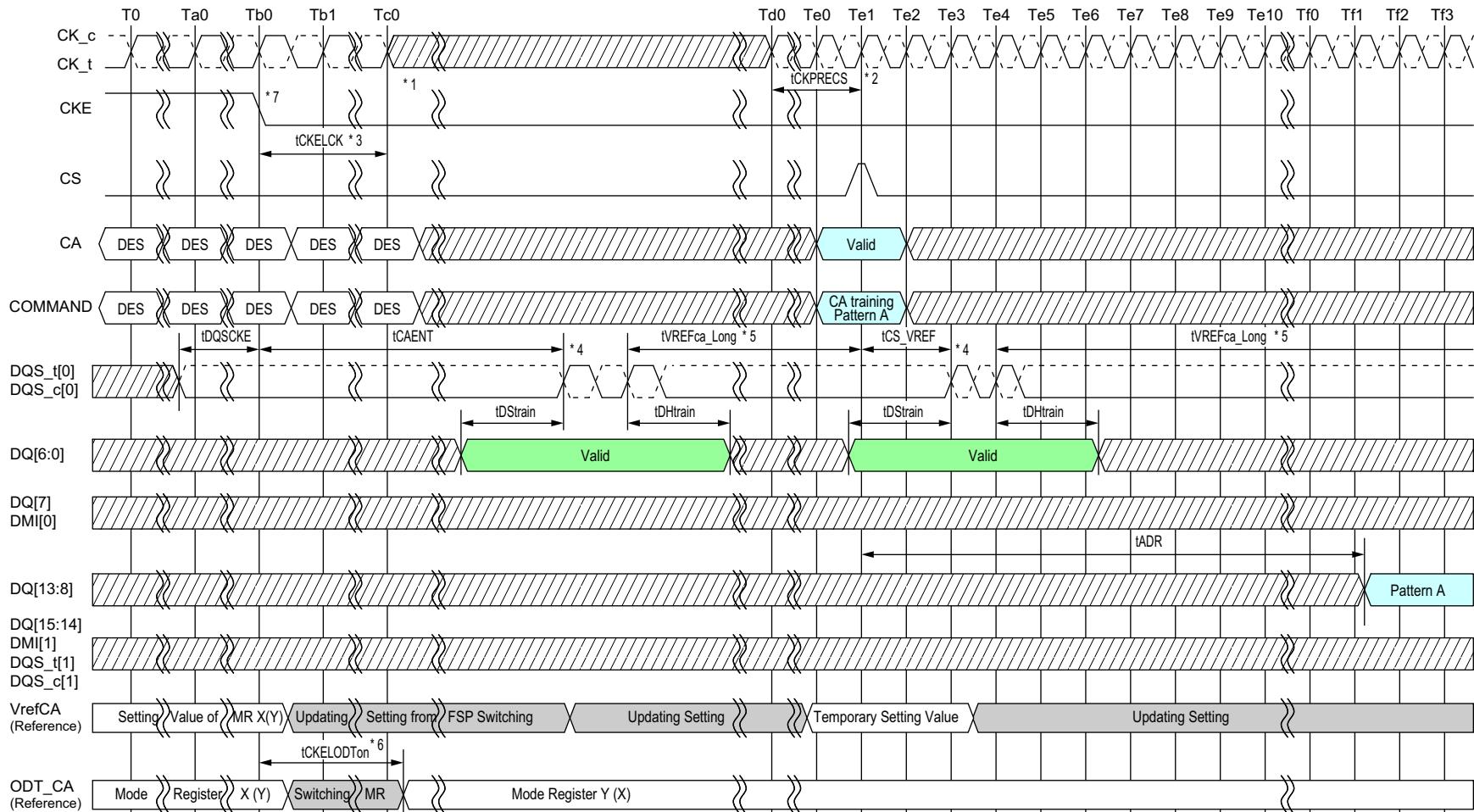


Figure 52 — Entering Command Bus Training Mode and CA Training Pattern Input and Output with V_{REFCA} Value Update



NOTES : 1. After tCKELCK clock can be stopped or frequency changed any time.

2. The input clock condition should be satisfied tCKPRECS.

3. Continue to Drive CK and Hold CA & CS pins low until tCKELCK after CKE is low (which disables command decoding).

4. DRAM may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals.

The captured value of DQ6:0 signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tVREFca_Long.

5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting,

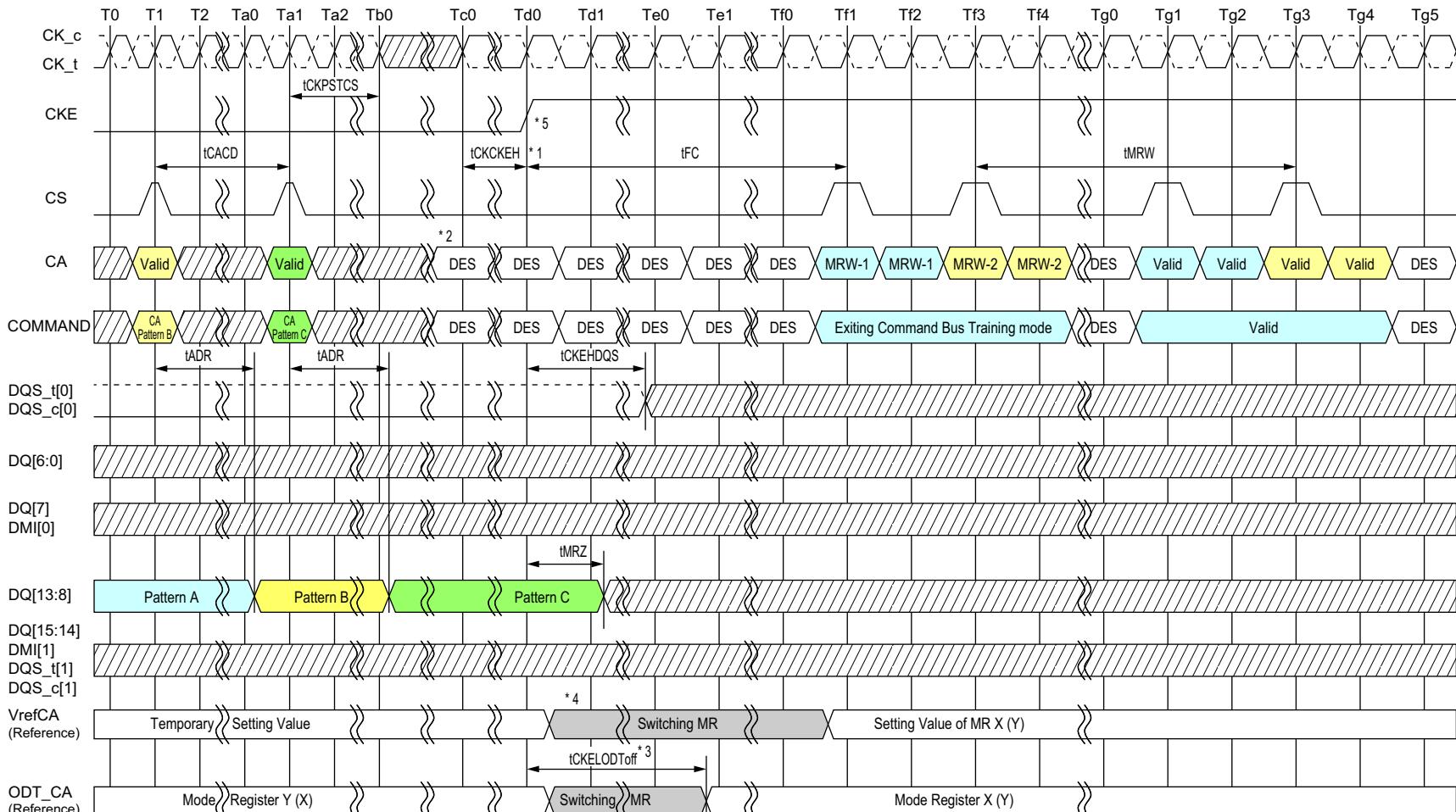
and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.

6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0],

then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode. If the ODT_CA pad is bonded to Vss or floating, ODT_CA termination will never enable for that die.

7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

Figure 53 — Consecutive V_{REFCA} Value Update



NOTES : 1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high.

When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)

2. CS and CA[5:0] must be Deselect (all low) tCKCKEH before CKE is driven high.

3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).

Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.

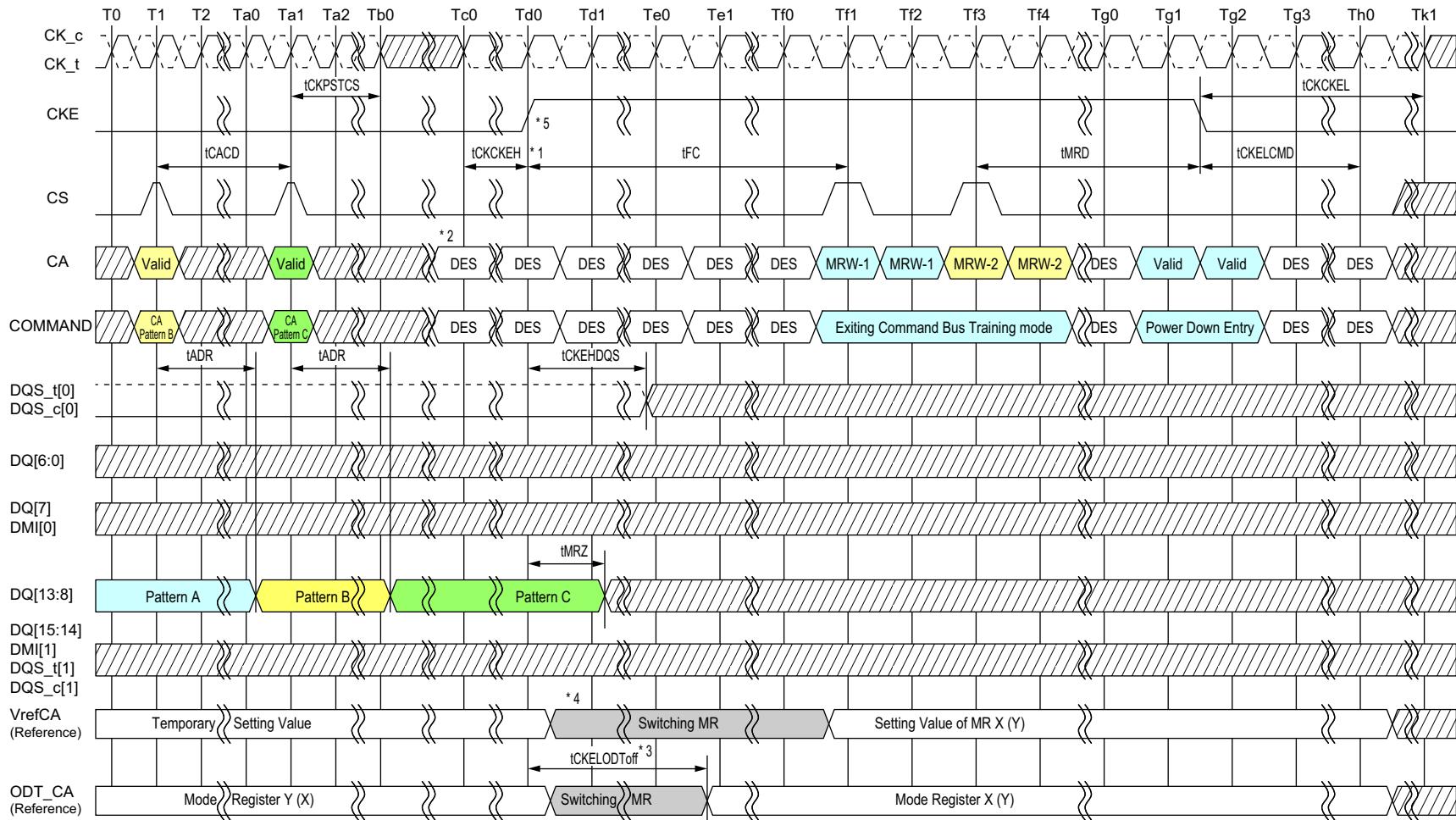
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.

Example: VREF(ca) will return to the value programmed in the original set point.

5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

DON'T CARE TIME BREAK

Figure 54 — Exiting Command Bus Training Mode with Valid Command



NOTES : 1. Clock can be stopped or frequency changed any time before tCKKEH. CK must meet tCKKEH before CKE is driven high.

When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)

2. CS and CA[5:0] must be Deselect (all low) tCKKEH before CKE is driven high.

3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).

Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.

4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.

Example: VREF(ca) will return to the value programmed in the original set point.

5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

DON'T CARE TIME BREAK

Figure 55 — Exiting Command Bus Training Mode with Power Down Entry

4.21.4 Timing Diagram (cont'd)

Table 35 — Command Bus Training AC Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Command Bus Training Timing												
Clock and Command Valid after CKE Low	tCKELCK	Min	max(7.5ns, 3nCK)						tCK			
Data Setup for V _{REF} Training Mode	tDStrain	Min	2						ns			
Data Hold for V _{REF} Training Mode	tDHtrain	Min	2						ns			
Asynchronous Data Read	tADR	Max	20						ns			
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)						tCK	2		
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10						ns	1		
First CA Bus Training Command Following CKE Low	tCAENT	Min	250						ns			
V _{REF} Step Time – multiple steps	tV _{REFca_LONG}	Max	250						ns			
V _{REF} Step Time – one step	tV _{REFca_SHORT}	Max	80						ns			
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 3nCK))						-			
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))						-			
Minimum delay from CS to DQS toggle in command bus training	tCS_V _{REF}	Min	2						tCK			
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS		10						ns			
Clock and Command Valid before CKE High	tCKCKEH	Min	2						tCK			
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5						ns			
ODT turn-on Latency from CKE	tCKELODTon	Min	20						ns			
ODT turn-off Latency from CKE	tCKELODToff	Min	20						ns			

NOTE 1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.

NOTE 2 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

4.22 Frequency Set Point

Frequency Set-Points allow the LPDDR4-SDRAM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an un-trained state which could result in a loss of communication to the DRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4-SDRAM's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include:

Table 36 — Mode Register Function with two physical registers

MR#	Operand	Function	Note
MR1	OP[2]	WR-PRE (WR Pre-amble Length)	
	OP[3]	RD-PRE (RD Pre-amble Type)	
	OP[6:4]	nWR (Write-Recovery for Auto-Pre-charge commands)	
	OP[7]	PST (RD Post-Amble Length)	
MR2	OP[2:0]	RL (Read latency)	
	OP[5:3]	WL (Write latency)	
	OP[6]	WLS (Write Latency Set)	
MR3	OP[0]	PU-Cal (Pull-up Calibration Point)	1
	OP[1]	WR PST(WR Post-Amble Length)	
	OP[5:3]	PDDS (Pull-Down Drive Strength)	
	OP[6]	DBI-RD (DBI-Read Enable)	
	OP[7]	DBI-WR (DBI-Write Enable)	
MR11	OP[2:0]	DQ ODT (DQ Bus Receiver On-Die-Termination)	
	OP[6:4]	CA ODT (CA Bus Receiver On-Die-Termination)	
MR12	OP[5:0]	$V_{REF}(ca)$ ($V_{REF}(ca)$ Setting)	
	OP[6]	$VR-CA$ ($V_{REF}(ca)$ Range)	
MR14	OP[5:0]	$V_{REF}(dq)$ ($V_{REF}(dq)$ Setting)	
	OP[6]	$VR(dq)$ ($V_{REF}(dq)$ Range)	
MR22	OP[2:0]	SoC ODT (Controller ODT Value for VOH calibration)	
	OP[3]	ODTE-CK (CK ODT enabled for nonterminating rank)	
	OP[4]	ODTE-CS (CS ODT enable for non terminating rank)	
	OP[5]	ODTD-CA (CA ODT termination disable)	

NOTE 1 PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command. See 3.4, Mode Register Definition, for more details.

4.22 Frequency Set Point (cont'd)

Table 37 shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

Table 37 — Relation between MR Setting and DRAM Operation

Function	MR# & Operand	Data	Operation	Note
FSP-WR	MR13 OP[6]	0 (Default)	Data write to Mode Register N for FSP-OP[0] by MRW Command	1
		1	Data write to Mode Register N for FSP-OP[1] by MRW Command	
FSP-OP	MR13 OP[7]	0 (Default)	DRAM operates with Mode Register N for FSP-OP[0] setting.	2
		1	DRAM operates with Mode Register N for FSP-OP[1] setting.	

NOTE 1 FSP-WR stands for Frequency Set Point Write/Read.

NOTE 2 FSP-OP stands for Frequency Set Point Operating Point.

4.22.1 Frequency set point update Timing

The Frequency set point update timing is shown in Figure 56. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into V_{REF} Fast Response (high current) mode at the same time. After Frequency change time(tFC) is satisfied. VRCG can be changed into Normal Operation mode via MR13 OP[3].

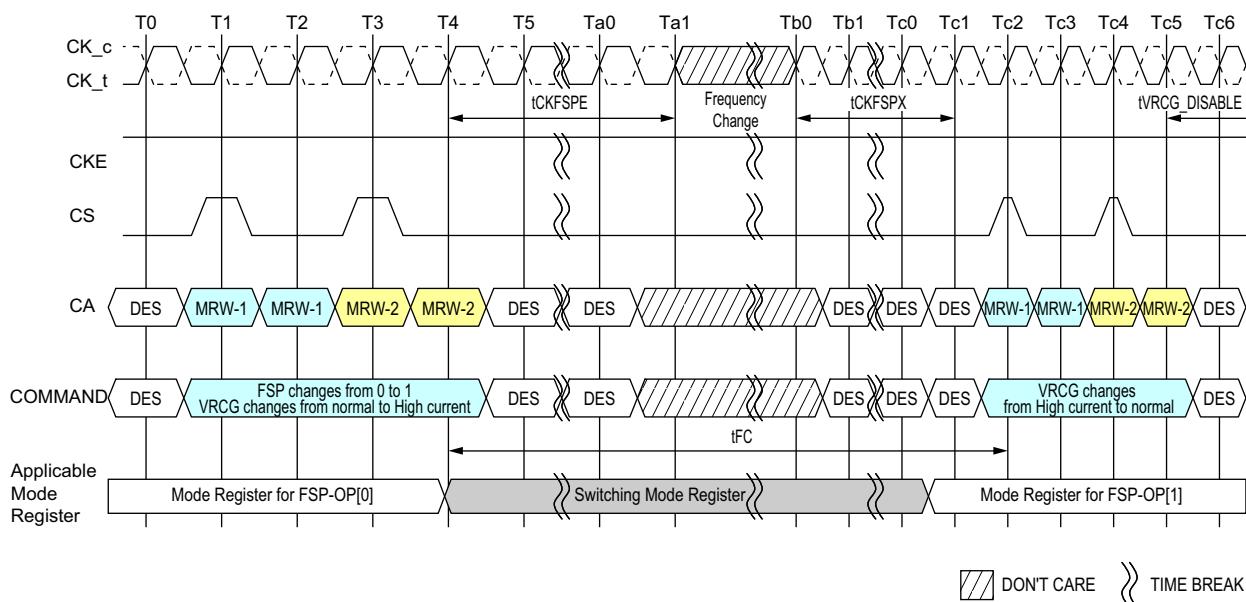


Figure 56 — Frequency Set Point Switching Timing

4.22.1 Frequency set point update Timing (cont'd)

Table 38 — Frequency Set Point AC Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note		
			533	1066	1600	2133	2667	3200	3733	4267				
Frequency Set Point parameters														
Frequency Set Point Switching Time	tFC_Short	MIN	TBD						ns		1			
	tFC_Middle	MIN	TBD						ns		1			
	tFC_Long	MIN	250						ns		1			
Valid Clock Requirement after Entering FSP Change	tCKFSPE	MIN	max(7.5ns, 4nCK)						-					
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	MIN	max(7.5ns, 4nCK)						-					

NOTE 1 Frequency Set Point Switching Time depends on value of $V_{REF}(ca)$ setting: MR12 OP[5:0] and $V_{REF}(ca)$ Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 39. Additionally change of Frequency Set Point may affect $V_{REF}(dq)$ setting. Settling time of $V_{REF}(dq)$ level is same as $V_{REF}(ca)$ level.

Table 39 — tFC value mapping

Application	Step Size		Range	
	From FSP -OP0	To FSP-OP1	From FSP -OP0	To FSP-OP1
tFC_Short	Base	A single step size increment/decrement	Base	No Change
tFC_Middle	Base	Two or more step size increment/decrement	Base	No Change
tFC_Long	-	-	Base	Change

NOTE 1 As well as change from FSP-OP1 to FSP-OP0.

4.22.1 Frequency set point update Timing (cont'd)

The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4-SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure 57). See 4.21, Command Bus Training, for more details on this training mode.

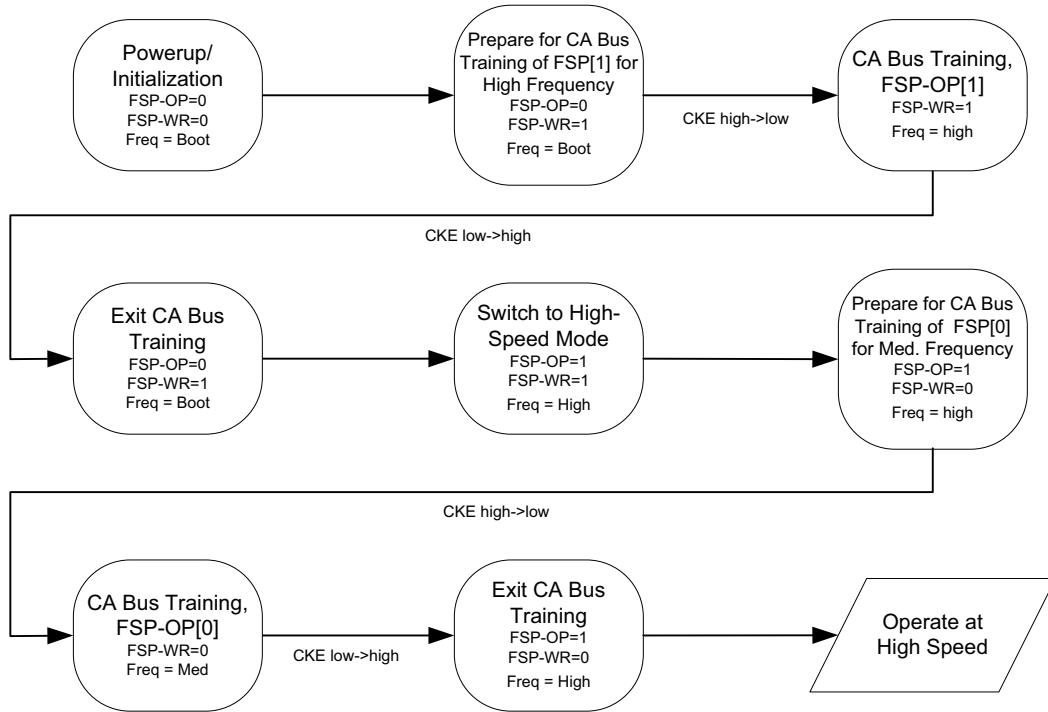


Figure 57 — Training Two Frequency Set-Points

Once both Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 58).

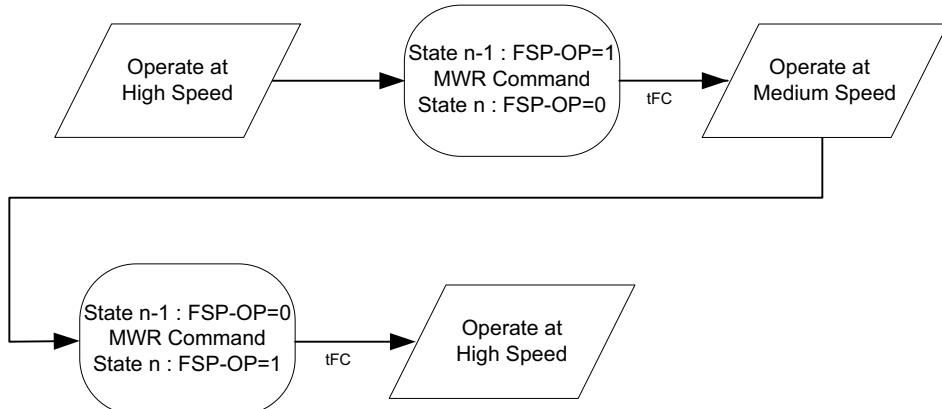


Figure 58 — Switching Between Two Trained Frequency Set-Points

4.22.1 Frequency set point update Timing (cont'd)

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the V_{REF} -CA calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 59).

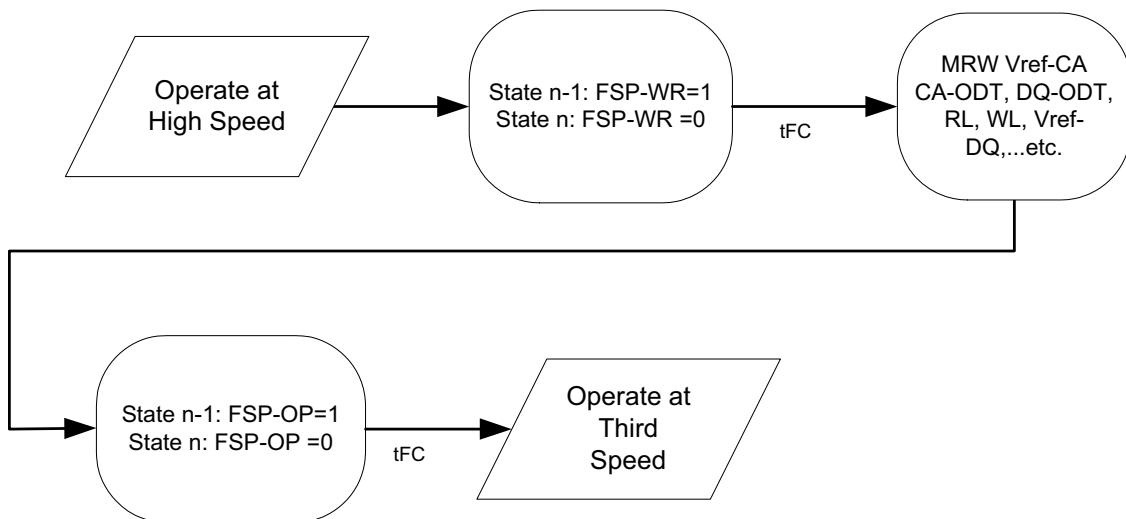


Figure 59 — Switching to a Third Trained Frequency Set-Point

4.23 Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS_t/DQS_c[0], and DQ[15:8] for DQS_t/DQS_c[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels.

The LPDDR4 SDRAM enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Depending on the absolute values of tDQSL and tDQSH in the application, the value of tDQSS may have to be better than the limits provided in the Write AC Timing Table¹ in order to satisfy the tDSS and tDSH specifications. Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2-OP[7] is reset LOW.

Write Leveling should be performed before Write Training (DQS2DQ Training).

4.23.1 Write Leveling Procedure

The following steps should be followed for Write Leveling:

1. Enter into Write-leveling mode by setting MR2-OP[7]=1.
2. Once entered into Write-leveling mode, DQS_t must be driven LOW and DQS_c HIGH after a delay of tWLQSEN.
3. Wait for a time tWLMRD before providing the first DQS signal input. The delay time tWLMRD(MAX) is controllerdependent.
4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode.
The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.
7. Exit from Write-leveling mode by setting MR2-OP[7]=0.

1. As of publication of this document, under discussion by the formulating committee.

4.23.1 Write Leveling Procedure (cont'd)

Write Leveling timing examples are shown in Figure 60 and Figure 61.

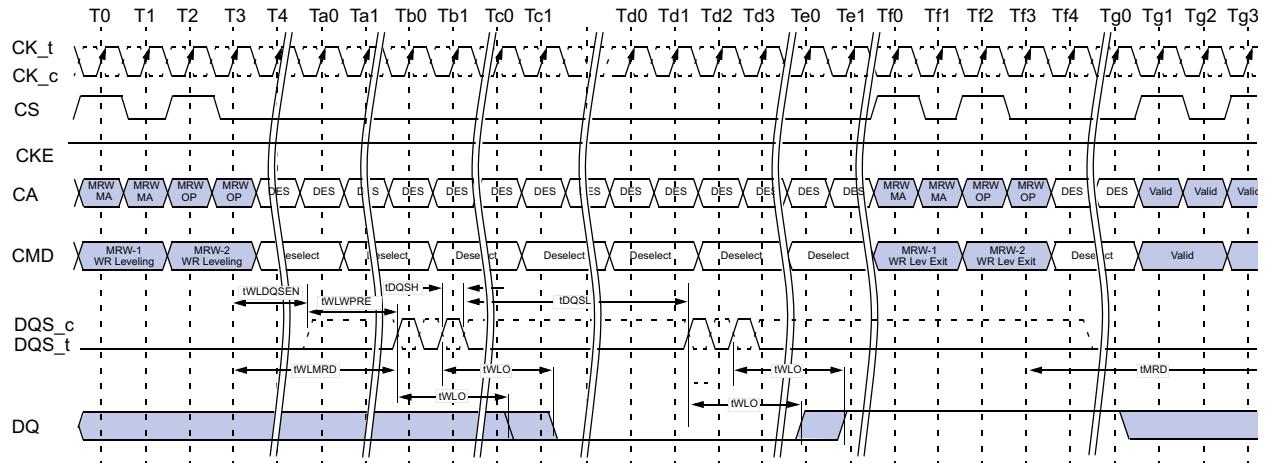


Figure 60 — Write Leveling Timing, tDQSL(max)

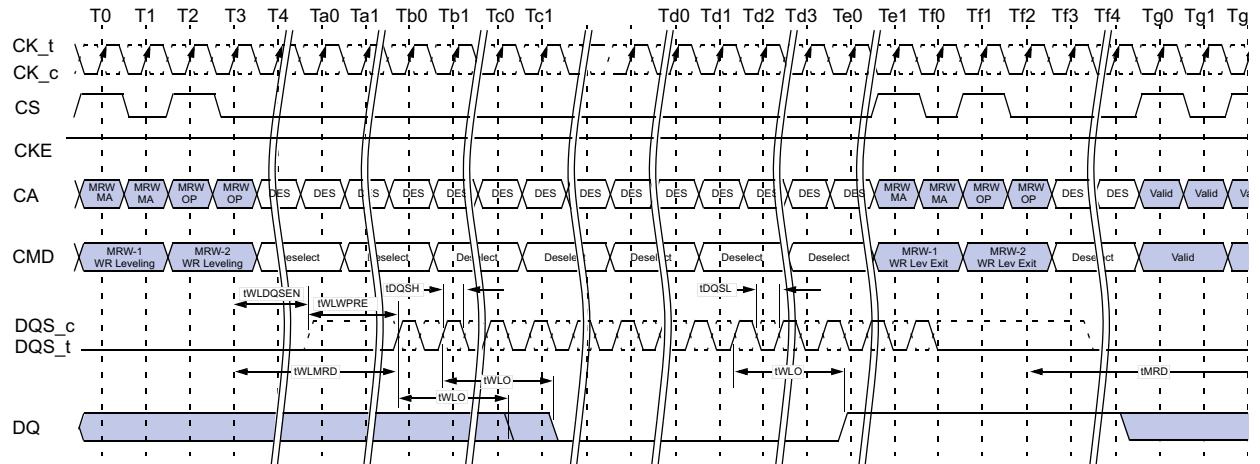
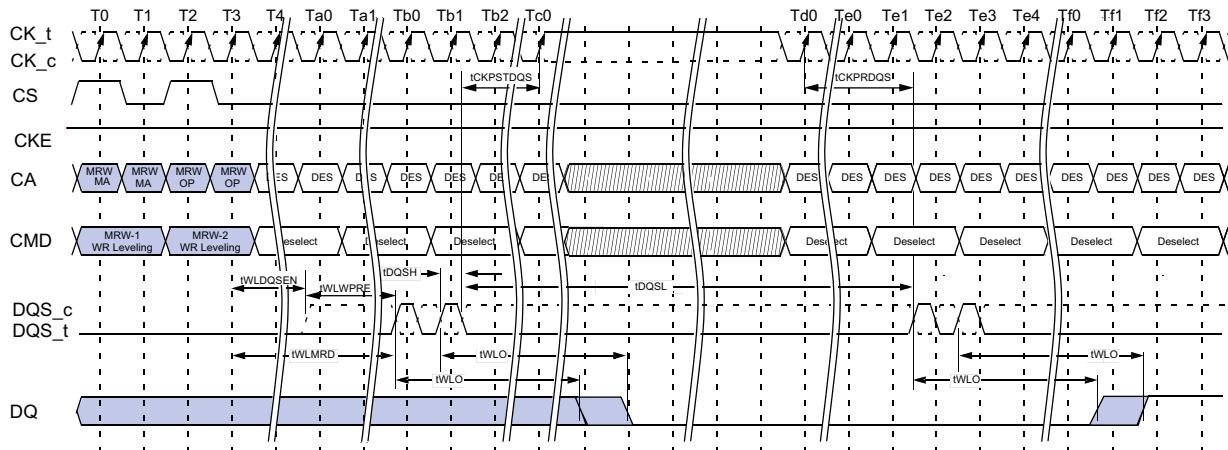


Figure 61 — Write Leveling Timing, tDQSL(min)

4.23.2 Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during Write Leveling mode.

The Frequency stop or change timing is shown in Figure 62.



NOTES : 1. CK_t is held LOW and CK_c is held HIGH during clock stop.

2. CS shall be held LOW during clock stop

Figure 62 — Clock Stop and Timing during Write Leveling

Table 40 — Write Leveling Timing Parameters

Parameter	Symbol	Min/Max	Value	Units	Notes
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	Min	20	tCK	
		Max	-		
Write preamble for Write Leveling	tWLWPRE	Min	20	tCK	
		Max	-		
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	Min	40	tCK	
		Max	-		
Write leveling output delay	tWLO	Min	0	ns	
		Max	20		
Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	ns	
		Max	-		
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	max(7.5ns, 4nCK)	-	
		Max	-		
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	Min	max(7.5ns, 4nCK)	-	
		Max	-		

4.23.3 Write Leveling Setup and Hold Time

Table 41 — Write Leveling Setup and Hold Time

Parameter	Symbol	Min/Max	Data Rate				Unit
			1600	2400	3200	4266	
Write Leveling Parameters							
Write leveling hold time	tWLH	MIN	150	100	75	50	ps
Write leveling setup time	tWLS	MIN	150	100	75	50	ps
Write leveling invalid window	tWLIVW_Total	MIN	240	160	120	90	ps

NOTE 1 In addition to the traditional setup and hold time specifications above, there is value in a invalid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.

NOTE 2 tWLIVW_Total is defined in a similar manner to tDIVW_Total, except that here it is a DQS invalid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

The DQS input mask for timing with respect to CK is shown in Figure 63. The "total" mask (TdiVW_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

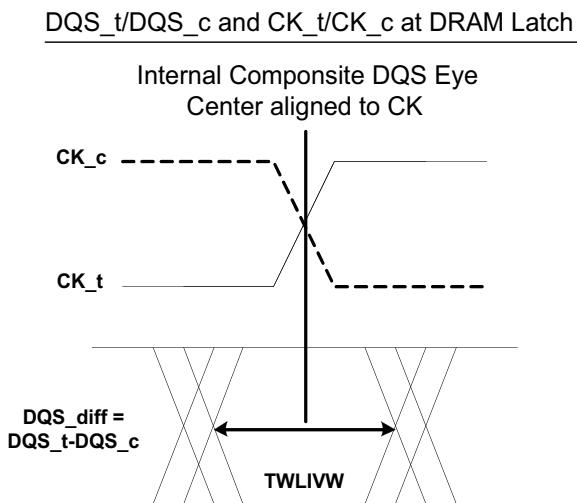


Figure 63 — DQS_t/DQS_c to CK_t/CK_t timings at the DRAM pins referenced from the internal latch

4.24 RD DQ Calibration

LPDDR4 devices feature a RD DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. RD DQ Calibration is initiated by issuing a MPC-1 [RD DQ Calibration] command followed by a CAS-2 command, cause the LPDDR4-SDRAM to drive the contents of MR32 followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

4.24.1 RD DQ Calibration Training Procedure

The procedure for executing RD DQ Calibration is:

- Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1).
- Optionally this step could be skipped to use the default patterns
 - MR32 default = 5Ah
 - MR40 default = 3Ch
 - MR15 default = 55h
 - MR20 default = 55h
- Issue an MPC-1 [RD DQ Calibration] command followed immediately by a CAS-2 command.
- Each time an MPC-1 [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit (see Table 42).
- Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
- This command can be issued every tCCD seamlessly, and can be issued seamlessly with array Read commands.
- The operands received with the CAS-2 command must be driven LOW.
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF with CKE high.

Table 42 — Invert Mask Assignments

DQ Pin	0	1	2	3	DMI0	4	5	6	7
MR15 bit	0	1	2	3	N/A	4	5	6	7

DQ Pin	8	9	10	11	DMI1	12	13	14	15
MR20 bit	0	1	2	3	N/A	4	5	6	7

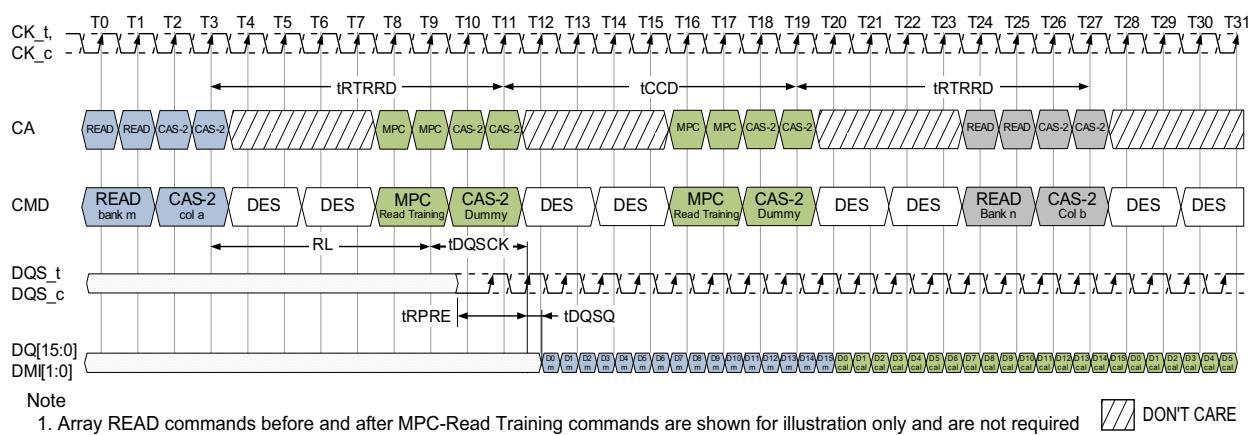


Figure 64 — DQ Read Training Timing

4.24.2 DQ Read Training Example

An example of DQ Read Training output is shown in Table 43. This shows the 16-bit data pattern that will be driven on each DQ in byte 0 when one DQ Read Training command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

Table 43 — DQ Read Calibration Bit Ordering and Inversion Example

Pin	Invert	Bit Sequence →															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ0	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ1	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ2	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ3	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI0	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ4	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ5	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ6	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ7	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ8	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ9	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ10	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ11	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI1	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ12	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ13	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ14	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ15	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

NOTE 1 The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when RD DQ Calibration is initiated via a MPC-1 [RD DQ Calibration] command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111 →.

NOTE 2 MR15 and MR22 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.

NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].

NOTE 4 No Data Bus Inversion (DBI) function is enacted during RD DQ Calibration, even if DBI is enabled in MR3-OP[6].

4.25 DQS-DQ Training

The LPDDR4-SDRAM uses an un-matched DQS-DQ path to enable high speed performance and save power in the DRAM. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad, and has a shorter internal delay in the SDRAM than does the DQS signal. The SDRAM DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the Data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available in LPDDR4:

- Command-based FIFO WR/RD with user patterns
- A internal DQS clock-tree oscillator, to determine the need for, and the magnitude of required training.

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if OP6 is set LOW then the DRAM will perform a NOP command. When OP6 is set HIGH, then OP5:0 enable training functions or are reserved for future use (RFU). MPC commands that initiate a Read FIFO, READ DQ Calibration or Write FIFO to the SDRAM must be followed immediately by a CAS-2 command. See 4.28, Multi Purpose Command (MPC) Definition" for more information.

To perform Write Training, the controller can issue a MPC [Write DQ FIFO] command with OP[6:0] set as described in 4.28, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a Write DQ FIFO. Timings for MPC [Write DQ FIFO] are identical to a Write command, with WL (Write Latency) timed from the 2nd rising clock edge of the CAS-2 command. Up to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command. Write/Read FIFO Pointer operation is described in 4.25.1.

After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed. MPC [Read DQ FIFO] is initiated by issuing a MPC command with OP[6:0] set as described in 4.28, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC [Read DQ FIFO] command are identical to a Read command, with RL (Read Latency) timed from the 2nd rising clock edge of the CAS-2 command.

Read DQ FIFO is non-destructive to the data captured in the FIFO, so data may be read continuously until it is either overwritten by a Write DQ FIFO command or disturbed by CKE LOW or any of the following commands; Write, Masked Write, Read, Read DQ Calibration and a MRR. If fewer than 5 Write DQ FIFO commands were executed, then unwritten registers will have un-defined (but valid) data when read back.

The following command about MRW is only allowed from MPC [Write DQ FIFO] command to MPC [Read DQ FIFO].

Allowing MRW command is for OP[7]:FSP-OP, OP[6]:FSP-WR and OP[3]:VRCG of MR13 and MR14. And the rest of MRW command is prohibited.

For example: If 5 Write DQ FIFO commands are executed sequentially, then a series of Read DQ FIFO commands will read valid data from FIFO[0], FIFO[1]....FIFO[4], and will then wrap back to FIFO[0] on the next Read DQ FIFO.

On the other hand, if fewer than 5 Write DQ FIFO commands are executed sequentially (example=3), then a series of Read DQ FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two Read DQ FIFO commands will return un-defined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

4.25.1 FIFO Pointer Reset and Synchronism

The Read and Write DQ FIFO pointers are reset under the following conditions:

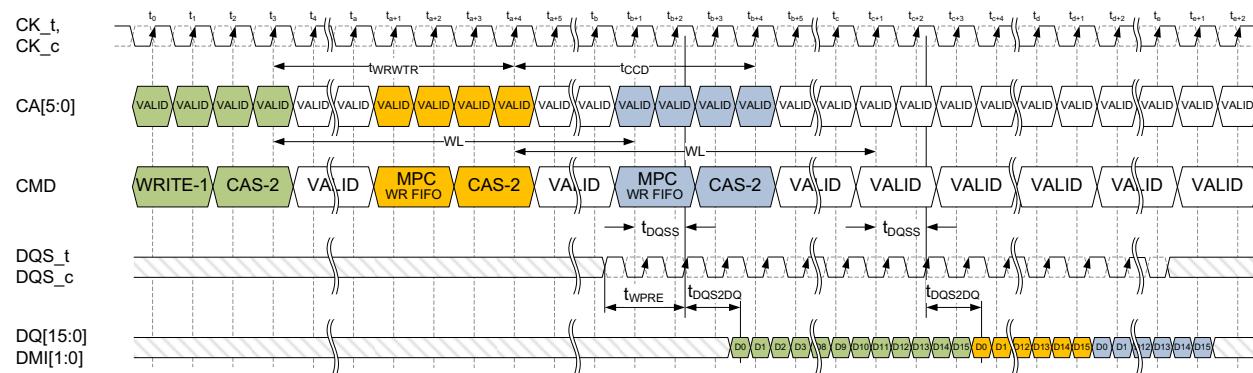
- Power-up initialization
- RESET_n asserted
- Power-down entry
- Self Refresh Power-Down entry

The MPC [Write DQ FIFO] command advances the WR-FIFO pointer, and the MPC [Read DQ FIFO] advances the RD-FIFO pointer. Also any normal (non-FIFO) Read Operation (RD, RDA) advances both WR-FIFO pointer and RD-FIFO pointer. Issuing (non-FIFO) Read Operation command is inhibited during Write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

$$\bullet b = a + (n \times c)$$

Where:

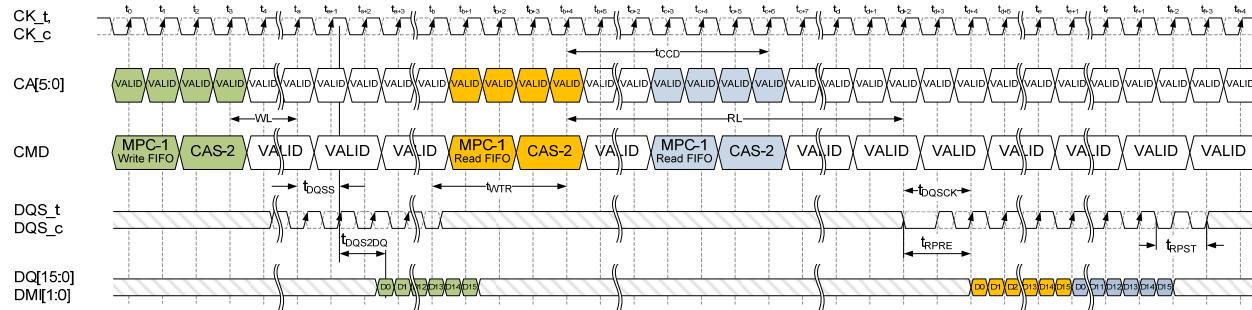
- 'a' is the number of MPC [Write DQ FIFO] commands
- 'b' is the number of MPC [Read DQ FIFO] commands
- 'c' is the FIFO depth (=5 for LPDDR4)
- 'n' is a positive integer, ≥ 0



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. Write-1 to MPC-1 is shown as an example of command-to-command timing for MPC.
Timing from Write-1 to MPC [WR-FIFO] is specified in the command-to-command timing table.
 3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
 4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
 5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data. The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
 6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW".
 7. To avoid corrupting the FIFO contents, MPC [RD-FIFO] must immediately follow MPC [WR-FIFO]/CAS-2 without any other commands disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR. See Write Training section for more information on FIFO pointer behavior.

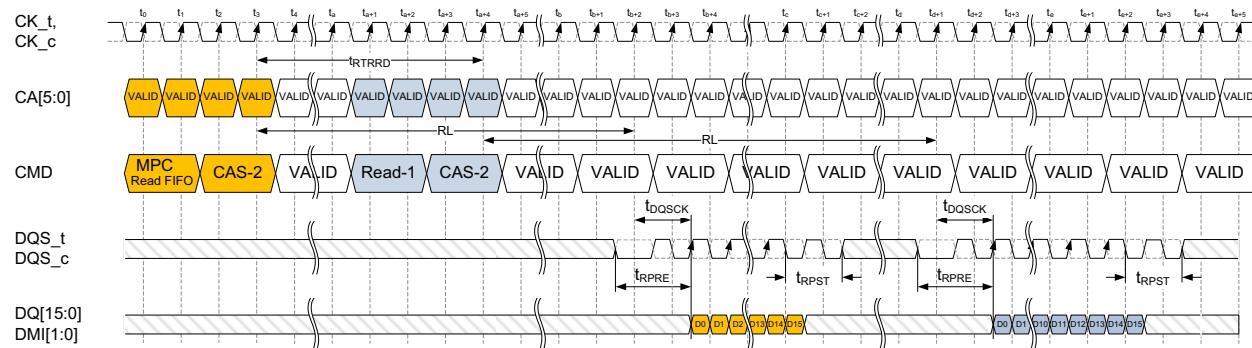
Figure 65 — MPC [Write FIFO] Operation (shown with tWPRE=2nCK, tWPST=0.5nCK)

4.25.1 FIFO Pointer Reset and Synchronism (cont'd)



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. MPC [WR-FIFO] to MPC [RD-FIFO] is shown as an example of command-to-command timing for MPC.
 3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
 4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR - FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following a MPC-1 command, the CAS-2 operands must be driven "LOW."
 7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 66 — MPC [Read FIFO] Operation
(shown with tWPRE=2nCK, tWPST=0.5nCK, tRPRE=toggling, tRPST=1.5nCK)**



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC.
 3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
 4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
 7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

Figure 67 — FIFO Read to Read Operation (shown with tRPRE=toggling, tRPST=1.5nCK)

4.26 DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The LPDDR4-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing a MPC [Start DQS Osc] command with OP[6:0] set as described in 4.28, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing a MPC [Stop DQS Osc] command with OP[6:0] set as described in 4.28, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (\text{DQS delay})}{\text{Run Time}}$$

Where:

Run Time = total time between start and stop commands

DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

DQS Oscillator Accuracy = 1 - Granularity Error - Matching Error

4.26 DQS Interval Oscillator (cont'd)

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (0.8\text{ns})}{100\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 12.8ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

Example: Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (0.8\text{ns})}{500\text{ns}} = 0.32\%$$

This equates to a granularity timing error of 2.56ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the "run time," determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0]. MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value ($=2^{16}$) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest Run Time Interval} = 2^{16} * \text{tDQS2DQ(min)} = 2^{16} * 0.2\text{ns} = 13.1\text{us}$$

4.26.1 Interval Oscillator matching error

The interval oscillator matching error is defined as the difference between the DQS training ckt(interval oscillator) and the actual DQS clock tree across voltage and temperature.

- Parameters:
 - tDQS2DQ: Actual DQS clock tree delay
 - tDQSOSC: Training ckt(interval oscillator) delay
 - OSCOffset: Average delay difference over voltage and temp(shown in Figure 68)
 - OSCMatch: DQS oscillator matching error

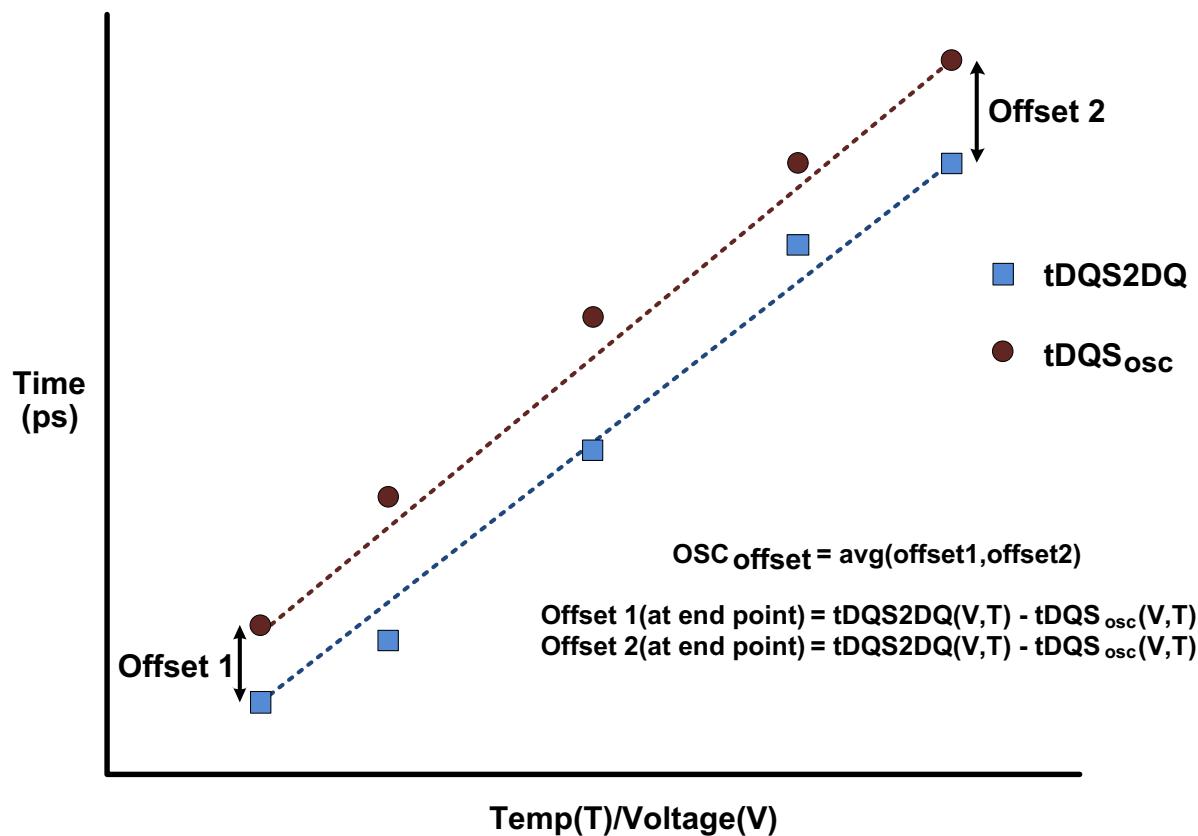


Figure 68 — Interval oscillator offset OSCoffset

- OSC_{Match} :

$$OSC_{Match} = [tDQS2DQ_{(V, T)} - tDQS_{osc(V, T)} - OSC_{offset}]$$

- $tDQS_{osc}$:

$$tDQS_{osc(V, T)} = \frac{\text{Runtime}}{2 * \text{Count}}$$

4.26.1 Interval Oscillator matching error (cont'd)

Table 44 — DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
DQS Oscillator Matching Error	$\text{OSC}_{\text{Match}}$	-20	20	ps	1,2,3,4,5,6,7
DQS Oscillator Offset	$\text{OSC}_{\text{offset}}$	-100	100	ps	2,4,7

NOTE 1 The $\text{OSC}_{\text{Match}}$ is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.

NOTE 2 This parameter will be characterized or guaranteed by design.

NOTE 3 The $\text{OSC}_{\text{Match}}$ is defined as the following:

$$\text{OSC}_{\text{Match}} = [tDQS2DQ_{(V,T)} - tDQS_{\text{OSC}(V,T)} - \text{OSC}_{\text{offset}}]$$

Where $tDQS2DQ_{(V,T)}$ and $tDQS_{\text{OSC}(V,T)}$ are determined over the same voltage and temp conditions.

NOTE 4 The runtime of the oscillator must be at least 200ns for determining $tDQS_{\text{OSC}(V,T)}$

$$tDQS_{\text{OSC}(V,T)} = \frac{\text{Runtime}}{2 * \text{Count}}$$

NOTE 5 The input stimulus for $tDQS2DQ$ will be consistent over voltage and temp conditions.

NOTE 6 The OSCoffset is the average difference of the endpoints across voltage and temp.

NOTE 7 These parameters are defined per channel.

4.26.2 DQS Interval Oscillator Readout Timing

OSC Stop to its counting value readout timing is shown in Figure 69 and Figure 70.

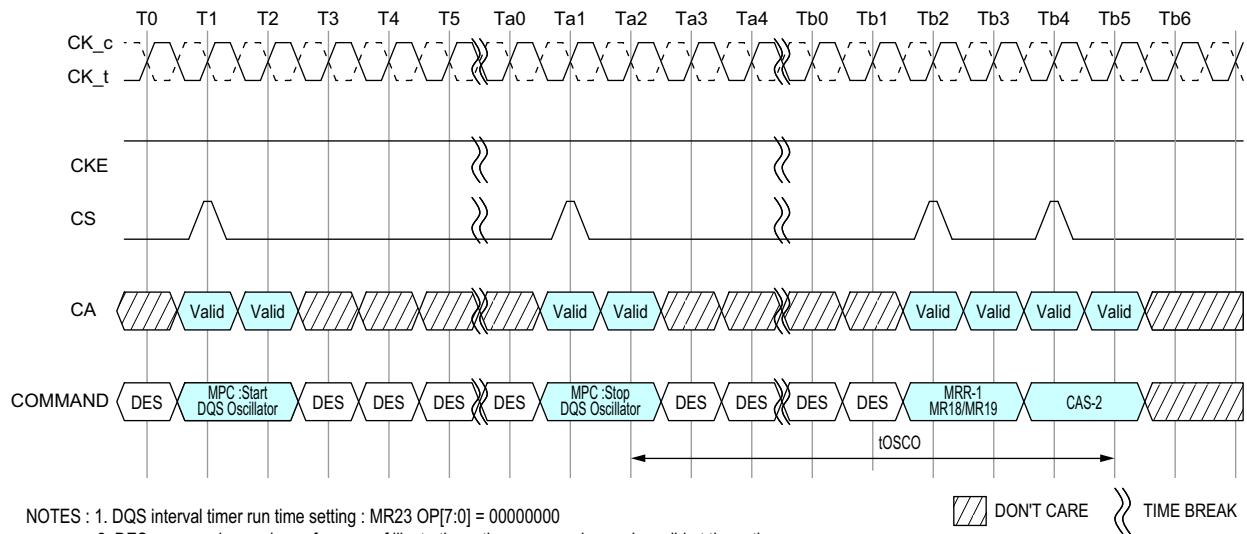


Figure 69 — In case of DQS Interval Oscillator is stopped by MPC Command

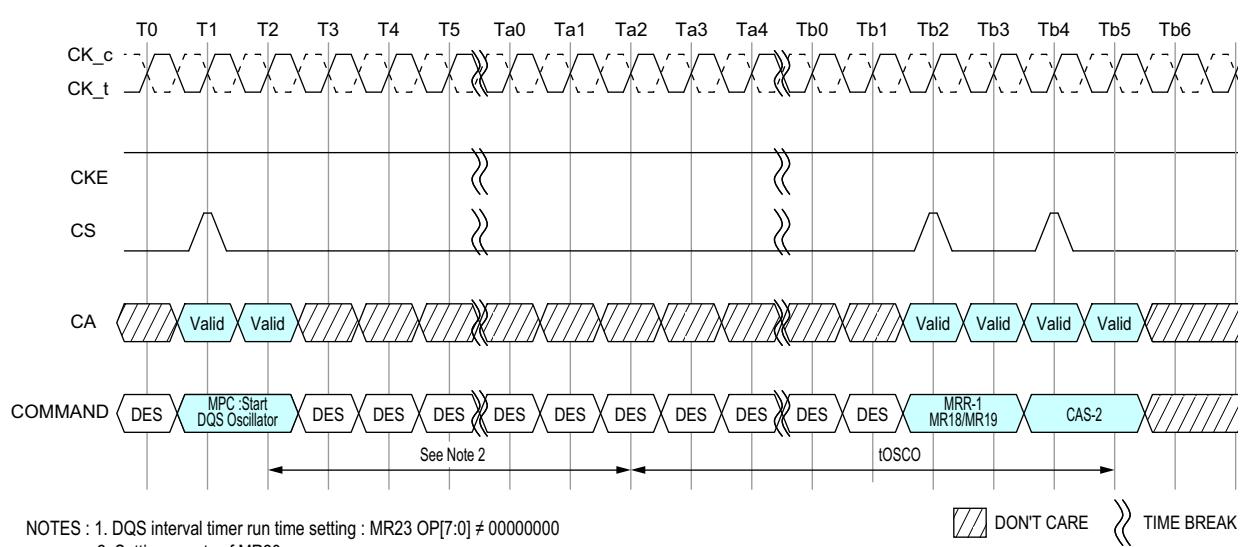


Figure 70 — In case of DQS Interval Oscillator is stopped by DQS interval timer

Table 45 —DQS Interval Oscillator AC Timing

Parameter	Symbol	Min/Max	Value	Units	Notes
Delay time from OSC stop to Mode Register Readout	tOSCO	Min	Max(40ns,8nCK)	ns	

4.27 READ Preamble Training

LPDDR4 READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13[OP1] = 1, the LPDDR4 DRAM will drive DQS_t LOW, DQS_c HIGH within tSDO and remain at these levels until an MPC DQ READ Training command is issued.

During READ Preamble Training the DQS preamble provided during normal operation will not be driven by the DRAM. Once the MPC DQ READ Training command is issued, the DRAM will drive DQS_t/DQD_c like a normal READ burst after RL. The DRAM may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Training commands may be issued.

READ Preamble Training is exited within tSDO after setting MR13[OP1] = 0.

The READ Preamble Training Feature is optional in the 8Gb device but required for other densities.

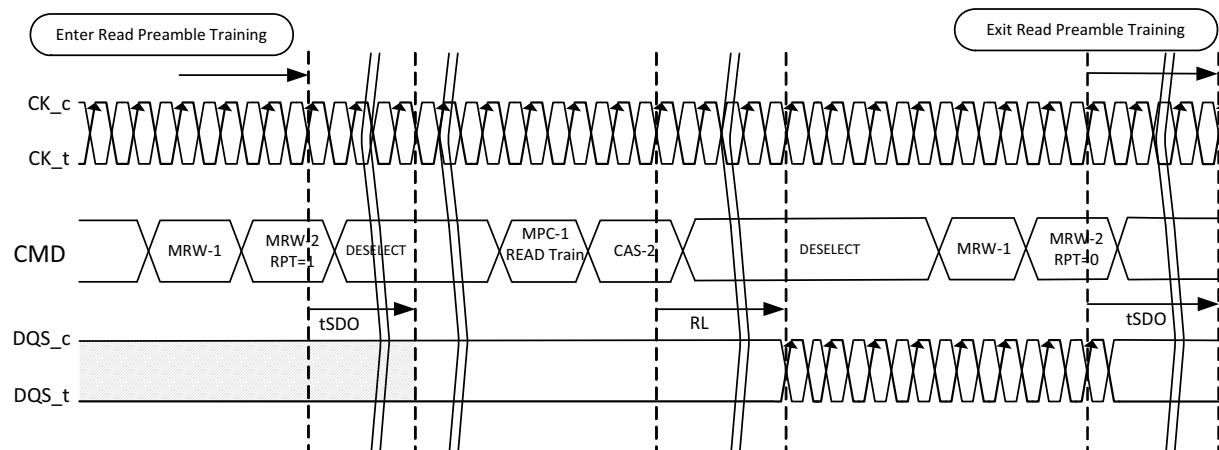


Figure 71 — Read Preamble Training

Table 46 — Timing Parameters

Parameter	Symbol	Min	Max
Delay from MRW command to DQS Driven Out	tSDO	-	min(24 nCK, 15ns)

4.28 Multi-Purpose Command (MPC)

LPDDR4-SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by Table 63 — Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW.

The following MPC commands must be followed by a CAS-2 command:

- Write FIFO
- Read FIFO
- Read DQ Calibration

All other MPC-1 commands do not require a CAS-2 command, including:

- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

Table 47 — MPC Command Definition

SDRAM Command	SDR Command Pins		SDR CA Pins							CK_t EDGE	Notes		
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5				
	CK_t(n-1)	CK_t(n)											
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	R1	1, 2		
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2			

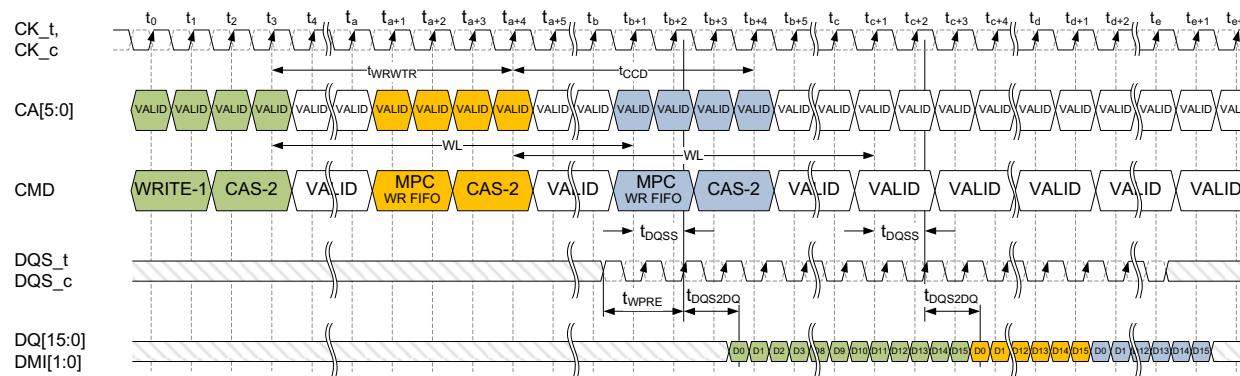
4.28 Multi-Purpose Command (MPC) (cont'd)

Table 48 — MPC Command Definition for OP[6:0]

Function	Operand	Data	Notes
Training Modes	OP[6:0]	0XXXXXX _B : NOP 1000001 _B : RD FIFO 1000011 _B : RD DQ Calibration (MR32/MR40) 1000101 _B : RFU 1000111 _B : WR FIFO 1001001 _B : RFU 1001011 _B : Start DQS Osc 1001101 _B : Stop DQS Osc 1001111 _B : ZQCal Start 1010001 _B : ZQCal Latch All Others: Reserved	1, 2

NOTE 1 See Table 63 — Command Truth Table for more information.

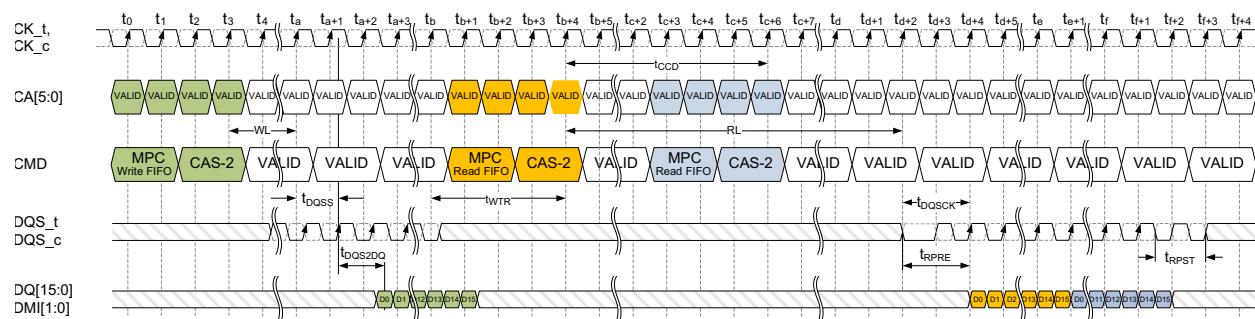
NOTE 2 MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is t_{WRWTR} .
 3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC [WR-FIFO] uses the same command-to-data timing relationship (t_{WL} , t_{DQSS} , t_{DQS2DO}) as a Write-1 command.
 5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data. The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
 6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
 7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR. See Write Training session for more information on FIFO pointer behavior.

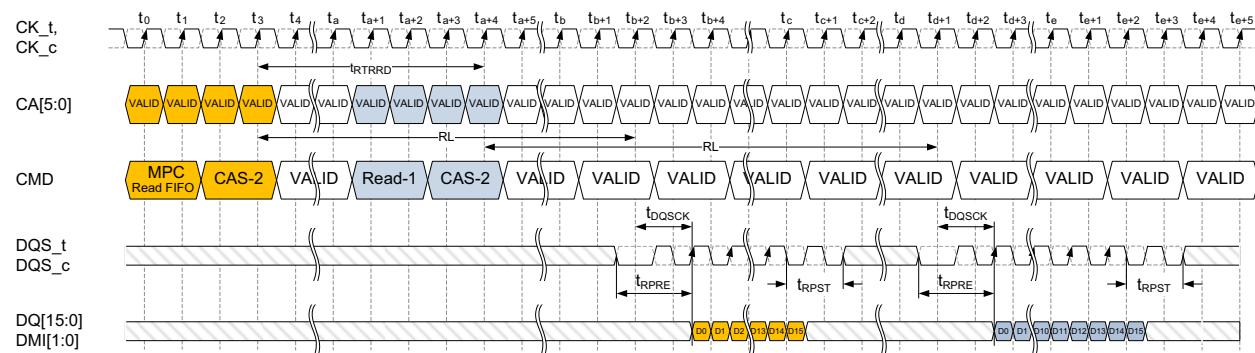
Figure 72 — MPC [WRITE FIFO] Operation: $t_{WPRE}=2nCK$, $t_{WPST}=0.5nCK$

4.28 Multi-Purpose Command (MPC) (cont'd)



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC-1 [WR-FIFO] is t_{WRWTR} .
 3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
 7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 73 — MPC [RD FIFO] Read Operation:
 $t_{WPRE}=2nCK$, $t_{WPST}=0.5nCK$, $t_{RPRE}=\text{toggling}$, $t_{RPST}=1.5nCK$**



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
 2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC-1 [RD-FIFO] command to Read is t_{IRRRD} .
 3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
 7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

Figure 74 — MPC [RD FIFO] Operation: $t_{RPRE}=\text{toggling}$, $t_{RPST}=1.5nCK$

4.28 Multi-Purpose Command (MPC) (cont'd)

Table 49 — Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Notes
WR/MWR	MPC [WR FIFO]	tWRWTR	nCK	1
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
RD/MRR	MPC [WR FIFO]	tRTW	nCK	4
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [WR FIFO]	WR/MWR	Not Allowed	-	2
	MPC [WR FIFO]	tCCD	nCK	
	RD/MRR	Not Allowed	-	2
	MPC [RD FIFO]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
	MPC [RD DQ Calibration]	Not Allowed	-	2
MPC [RD FIFO]	WR/MWR	tRTW	nCK	4
	MPC [WR FIFO]	tRTW	nCK	4
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	tCCD	nCK	
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [RD DQ Calibration]	WR/MWR	tRTW	nCK	4
	MPC [WR FIFO]	tRTW	nCK	4
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tCCD	nCK	

NOTE 1 tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + max(RU(7.5ns/tCK),8nCK)

NOTE 2 No commands are allowed between MPC [WR FIFO] and MPC-1 [RD FIFO] except MRW commands related to training parameters.

NOTE 3 tRTRRD = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) + max(RU(7.5ns/tCK),8nCK)

NOTE 4 tRTW :

In Case of DQ ODT Disable MR11 OP[2:0] = 000_B:

RL+RU(tDQSCK(max)/ tCK) +BL/2- WL+tWPRE+RD(tRPST)

In Case of DQ ODT Enable MR11 OP[2:0] ≠ 000_B:

RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon,min/tCK) + 1

4.29 Thermal Offset

Because of their tight thermal coupling with the LPDDR4 device, hot spots on an SOC can induce thermal gradients across the LPDDR4 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR4(6:5) to either or to both the channels. This temperature offset may modify refresh behavior for the channel to which the offset is provided. It will take a max of 200us to have the change reflected in MR4(2:0) for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR4 memory controller.

Support of thermal offset function is optional. Please refer to vendor datasheet to figure out if the function is supported or not.

4.30 Temperature Sensor

LPDDR4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR4 devices shall monitor device temperature and update MR4 according to tTSI. Upon assertion of CKE (Low to High transition), the device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in self refresh state with CKE HIGH.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 'b011. LPDDR4 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

4.30 Temperature Sensor (cont'd)

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (t_{TSI}) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + t_{TSI} + \text{SysRespDelay}) \leq 2 \text{ }^{\circ}\text{C}$$

Table 50 — Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	t_{TSI}	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$(10 \text{ }^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2 \text{ }^{\circ}\text{C}$$

In this case, ReadInterval shall be no greater than 167 ms.

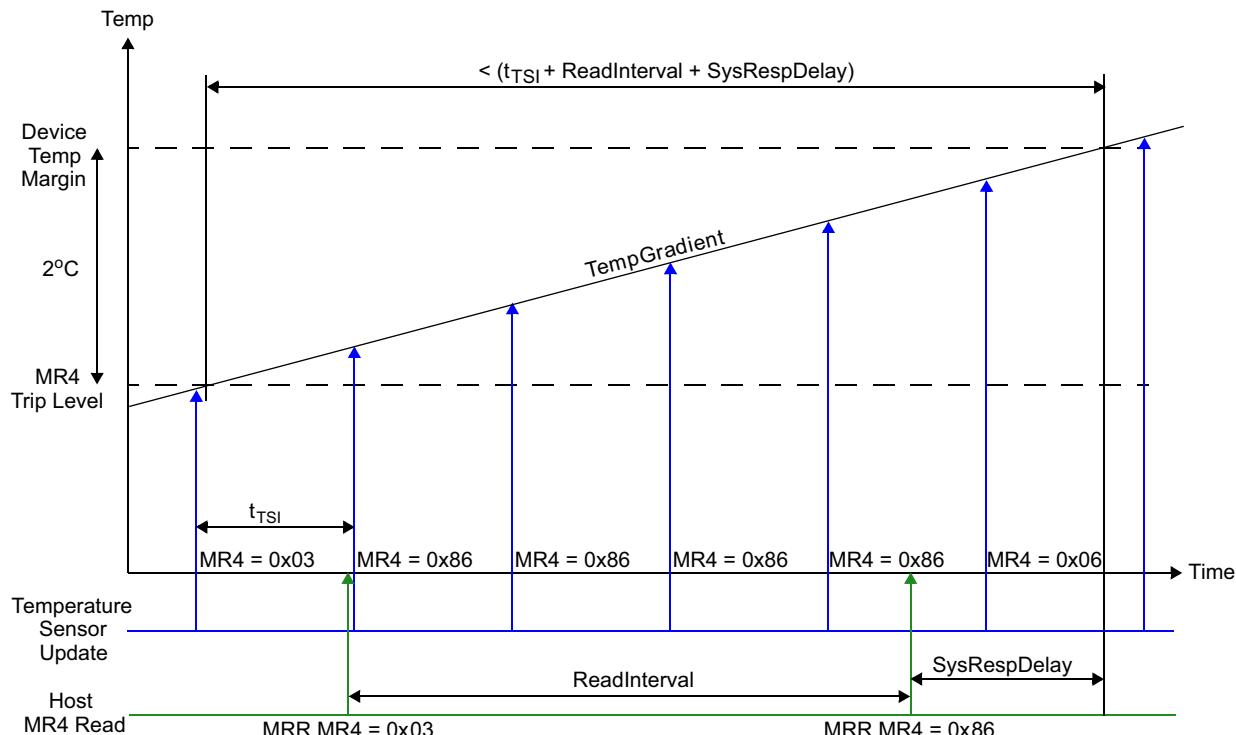


Figure 75 — Temp Sensor Timing

4.31 ZQ Calibration

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation, and is designed to eliminate any need for coordination between channels (i.e. it allows for channel independence).

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the LPDDR4-SDRAM is not in a power-down state. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated. The following mode register fields that modify I/O parameters cannot be changed following a ZQCal Start command and before tZQCAL has expired:

- PU-Cal (Pull-up Calibration VOH Point)
- PDDS (Pull Down Drive Strength and Rx Termination)
- DQ-ODT (DQ ODT Value)
- CA-ODT (CA ODT Value)

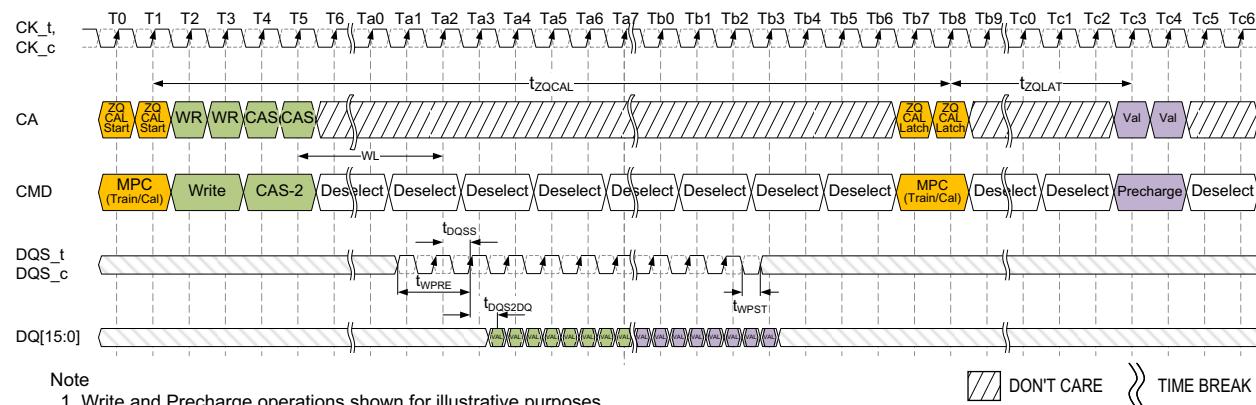
4.31.1 ZQCal Reset

The ZQCal Reset command resets the output impedance calibration to a default accuracy of +/- 30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/- 30% when ZQCal Start and ZQCal Latch commands are not used.

The ZQCal Reset command is executed by writing MR10 OP[0]=1B.

Table 51 — ZQCal Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ Calibration Time	tZQCAL	MIN	1	us
ZQ Calibration Latch Time	tZQLAT	MIN	max(30ns,8nCK)	ns
ZQ Calibration Reset Time	tZQRESET	MIN	max(50ns,3nCK)	ns



Note

1. Write and Precharge operations shown for illustrative purposes.
Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
2. Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed.
Write commands with DQ Termination must be given enough time to turn off the DQ-ODT before issuing the ZQ-Latch command.
See the ODT section for ODT timing.

Figure 76 — ZQCal Timing

4.31.2 Multi-Channel Considerations

The LPDDR4-SDRAM includes a single ZQ pin and associated ZQ Calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

1. ZQCal Start commands may be issued to either or both channels.
2. ZQCal Start commands may be issued when either or both channels are executing other commands and other commands may be issued during tZQCAL.
3. ZQCal Start commands may be issued to both channels simultaneously.
4. The ZQCal Start command will begin the calibration unless a previously requested ZQ calibration is in progress.
5. If a ZQCal Start command is received while a ZQ calibration is in progress on the SDRAM, the ZQCal Start command will be ignored and the in-progress calibration will not be interrupted.
6. ZQCal Latch commands are required for each channel.
7. ZQCal Latch commands may be issued to both channels simultaneously.
8. ZQCal Latch commands will latch results of the most recent ZQCal Start command provided tZQCAL has been met.
9. ZQCal Latch commands which do not meet tZQCAL will latch the results of the most recently completed ZQ calibration.
10. ZQ Reset MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCal Start and ZQCal Latch commands as needed without regard to the state of the other channel.

4.31.3 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel shall use a separate ZQCal resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF.

Example: If a system configuration shares a CA bus between 'n' channels to form a n * 16 wide bus, and no means are available to control the ZQCal separately for each channel (i.e. separate CS, CKE, or CK), then each x16 channel must have a separate ZQCal resistor.

Example: For a x32, two rank system, each x16 channel must have its own ZQCal resistor, but the ZQCal resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCal commands for Rank[0] and Rank[1] don't overlap.

4.32 Pull Up/Pull Down Driver Characteristics and Calibration

Table 52 — Pull-down Driver Characteristics, with ZQ Calibration

$R_{ONPD,nom}$	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 Ohm	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 Ohm	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 Ohm	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 Ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

NOTE 1 All value are after ZQ Calibration. Without ZQ Calibration R_{ONPD} values are $\pm 30\%$.

Table 53 — Pull-Up Characteristics, with ZQ Calibration

$VOH_{PU,nom}$	$VOH,nom(mV)$	Min	Nom	Max	Unit
$V_{DDQ}/2.5$	440	0.9	1	1.1	VOH,nom
$V_{DDQ}/3$	367	0.9	1	1.1	VOH,nom

NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration $VOH(nom)$ values are $\pm 30\%$.

NOTE 2 VOH,nom (mV) values are based on a nominal $VDDQ = 1.1V$.

Table 54 — Valid Calibration Points

$VOH_{PU,nom}$	ODT Value					
	240	120	80	60	48	40
$V_{DDQ}/2.5$	VALID	VALID	VALID	DNU	DNU	DNU
$V_{DDQ}/3$	VALID	VALID	VALID	VALID	VALID	VALID

NOTE 1 Once the output is calibrated for a given $VOH(nom)$ calibration point, the ODT value may be changed without recalibration.

NOTE 2 If the $VOH(nom)$ calibration point is changed, then re-calibration is required.

NOTE 3 DNU = Do Not Use

4.33 On Die Termination (ODT) for Command/Address Bus

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, CS and CA[5:0] signals without the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the DRAM ODT feature is shown in Figure 77.

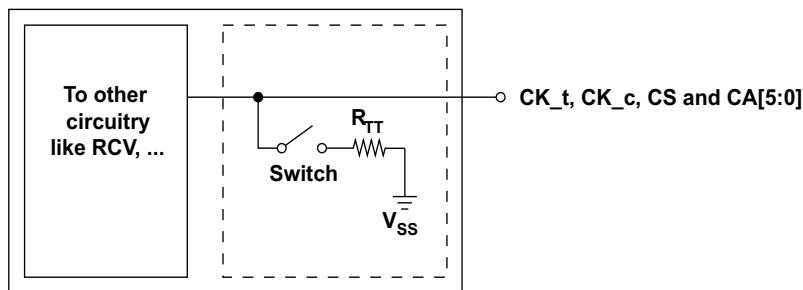


Figure 77 — Functional Representation of CA ODT

4.33.1 ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_C, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS and CA[5:0] signals. The CA ODT of the device is designed to enable one rank to terminate the entire command bus in a multirank system, so only one termination load will be present even if multiple devices are sharing the command signals. For this reason, CA ODT remains on even when the device is in the power-down or self-refresh power-down states.

The die has a bond-pad (ODT_CA) for multirank operations. When the ODT_CA pad is LOW, the die will not terminate the CA bus regardless of the state of the mode register CA ODT bits (MR11 OP[6:4]). If, however, the ODT_CA bond-pad is HIGH, and the mode register CA ODT bits are enabled, the die will terminate the CA bus with the ODT values found in MR11 OP[6:4]. In a multirank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

Table 55 — Command Bus ODT State

ODTE-CA MR11[6:4]	ODT_CA bond pad	ODTD-CA MR22[5]	ODTF-CK MR22[3]	ODTF-CS MR22[4]	ODT State for CA	ODT State for CK_t/CK_c	ODT State for CS
Disabled ¹	Valid ²	Valid ³	Valid ³	Valid ³	Off	Off	Off
Valid ³	0	Valid ³	0	0	Off	Off	Off
Valid ³	0	Valid ³	0	1	Off	Off	On
Valid ³	0	Valid ³	1	0	Off	On	Off
Valid ³	0	Valid ³	1	1	Off	On	On
Valid ³	1	0	Valid ³	Valid ³	On	On	On
Valid ³	1	1	Valid ³	Valid ³	Off	On	On

NOTE 1 Default Value

NOTE 2 “Valid” means “H or L (but a defined logic level)”

NOTE 3 “Valid” means “0 or 1”

NOTE 4 The state of ODT_CA is not changed when the DRAM enters power-down mode. This maintains termination for alternate ranks in multi-rank systems.

4.33.2 ODT Mode Register and ODT Characteristics

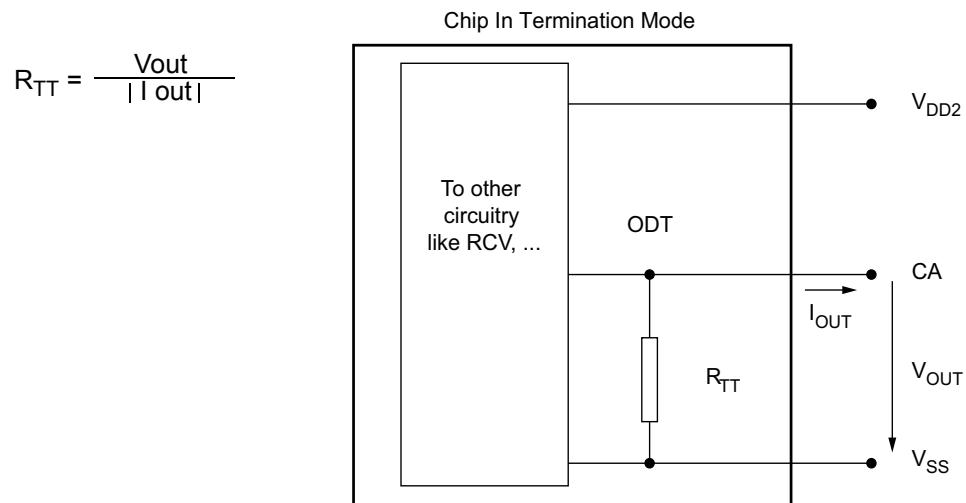


Figure 78 — On Die Termination for CA

4.33.2 ODT Mode Register and ODT Characteristics (cont'd)

Table 56 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω +/-1% over the entire operating temperature range after a proper ZQ calibration

MR11[6:4]	RTT	Vout	Min	Nom	Max	Unit	Note
001	240Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ	1,2,3
010	120Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ/2	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ/2	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ/2	1,2,3
011	80Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ/3	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ/3	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ/3	1,2,3
100	60Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ/4	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ/4	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ/4	1,2,3
101	48Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ/5	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ/5	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ/5	1,2,3
110	40Ω	VOLdc= 0.1 * V _{DD} 2	0.8	1.0	1.1	RZQ/6	1,2,3
		VOMdc= 0.33 * V _{DD} 2	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc= 0.5 * V _{DD} 2	0.9	1.0	1.2	RZQ/6	1,2,3
Mismatch CA-CA within clk group		0.33* V _{DD} 2	-		TBD	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see “voltage and temperature sensitivity”¹.

NOTE 2 Pull-dn ODT resistors are recommended to be calibrated at 0.33*V_{DD}2. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5*V_{DD}2 and 0.1*V_{DD}2.

NOTE 3 Measurement definition for RTT: TBD¹

NOTE 4 CA to CA mismatch within clock group (CA,CS) variation for a given component including CK_t and CK_c (characterized).

$$\text{CA - CA Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$

1. As of publication of this document, under discussion by the formulating committee.

4.33.3 ODT for Command/Address Update Time

ODT for Command/Address update time after Mode Register set are shown in Figure 79.

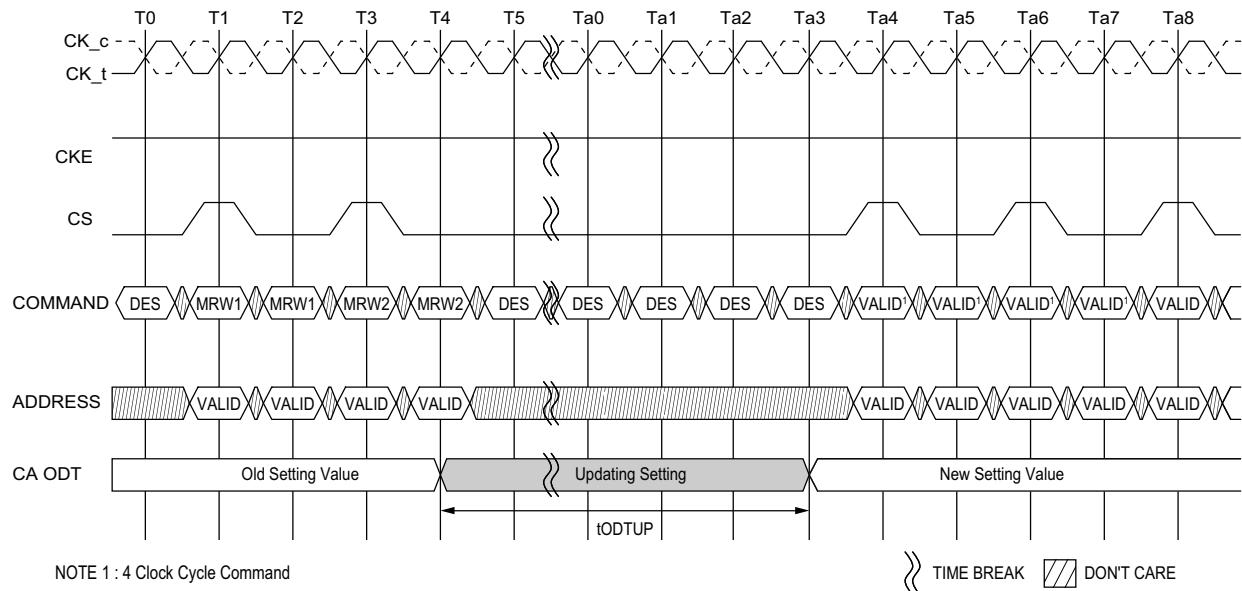


Figure 79 — ODT for Command/Address setting update timing in 4 Clock Cycle Command

Table 57 — ODT CA AC Timing

Speed		LPDDR4-1600/1866/2133/2400/3200/4266		Units	NOTE
Parameter	Symbol	MIN	MAX		
ODT CA Value Update Time	tODTUP	RU(TBdns/tCK(avg))	-		

4.34 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write or Mask Write operation.

The ODT feature is off and cannot be supported in Power Down and Self-Refresh modes.
A simple functional representation of the DRAM ODT feature is shown in Figure 80.

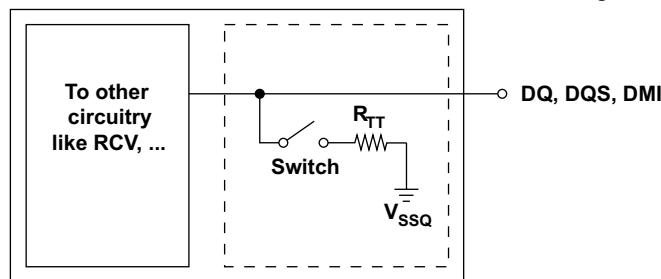


Figure 80 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the Write-1 or Mask Write-1 command and other mode register control information. The value of RTT is determined by the settings of Mode Register bits.

4.34.1 ODT Mode Register

The ODT Mode is enabled if MR11 OP[3:0] are non zero. In this case, the value of *RTT* is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP[3] = 0.

4.34.2 Asynchronous ODT

When ODT Mode is enabled in MR11 OP[3:0], DRAM ODT is always Hi-Z. DRAM ODT feature is automatically turned ON asynchronously based on the Write-1 or Mask Write-1 command that DRAM samples. After the write burst is complete, DRAM ODT featured is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled:

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max

ODTLon is a synchronous parameter and it is the latency from CAS-2 command to tODTon reference.

ODTLon latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLon latency.

Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum RTT turn on time (tODTon,max) is the point in time when the ODT resistance is fully on.

tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from CAS-2 command.

ODTloff is a synchronous parameter and it is the latency from CAS-2 command to tODToff reference.

ODTloff latency is a fixed latency value for each speed bin. Each speed bin has a different ODTloff latency.

Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance.

tODToff,min and tODToff,max are measured once ODTloff latency is satisfied from CAS-2 command.

4.34.2 Asynchronous ODT (cont'd)

Table 58 — ODTLon and ODTLoff Latency Values

ODTLon Latency ¹ tWPRE = 2 tCK		ODTloff Latency ²		Lower Clock Frequency Limit (>)	Upper Clock Frequency Limit (≤)
WL Set "A"	WL Set "B"	WL Set "A"	WL Set "B"		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133
nCK	nCK	nCK	nCK	MHz	MHz

NOTE 1 ODTLon is referenced from CAS-2 command. See Figure 81.

NOTE 2 ODTLoff as shown assumes BL=16. For BL32, 8 tCK should be added.

Table 59 — Asynchronous ODT Turn On and Turn Off Timing

Parameter	800 - 2133 MHz	Unit
tODTon, min	1.5	ns
tODTon, max	3.5	ns
tODToff, min	1.5	ns
tODToff, max	3.5	ns

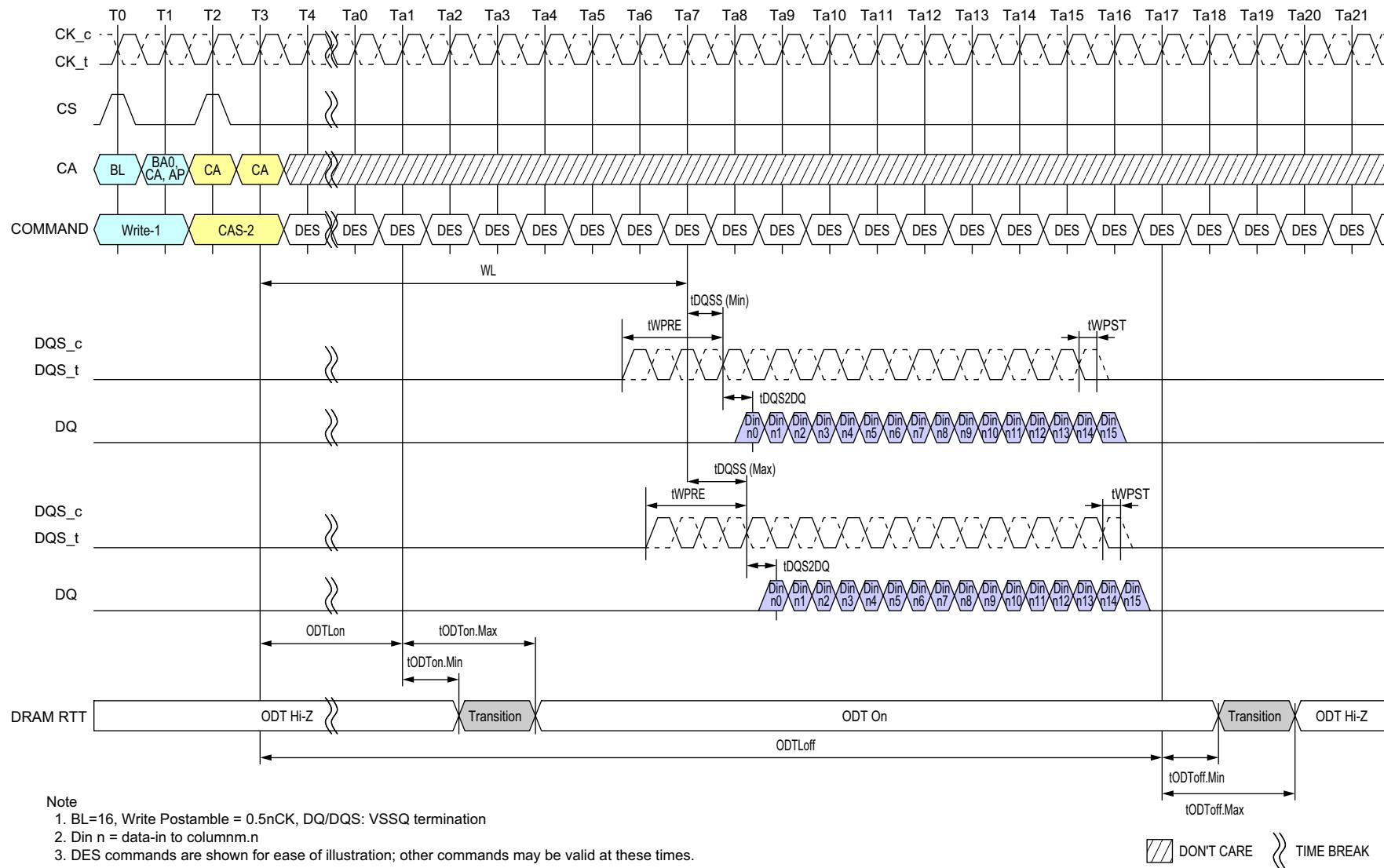


Figure 81 — Asynchronous ODTon/ODToff Timing

4.34.3 ODT during Write Leveling

If ODT is enabled in MR11 OP[3:0], in Write Leveling mode, DRAM always provides the termination on DQS_t/DQS_c signals. DQ termination is always off in Write Leveling mode regardless.

Table 60 — DRAM Termination Function in Write Leveling Mode

ODT Enabled in MR11	DQS_t/DQS_c termination	DQ termination
Disabled	OFF	OFF
Enabled	ON	OFF

4.35 On-Die Termination (ODT) for DQ, DQS, and DMI

On-Die Termination (ODT) effective resistance RTT is defined by MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS_t and DQS_c pins.

A functional representation of the on-die termination is shown in Figure 82.

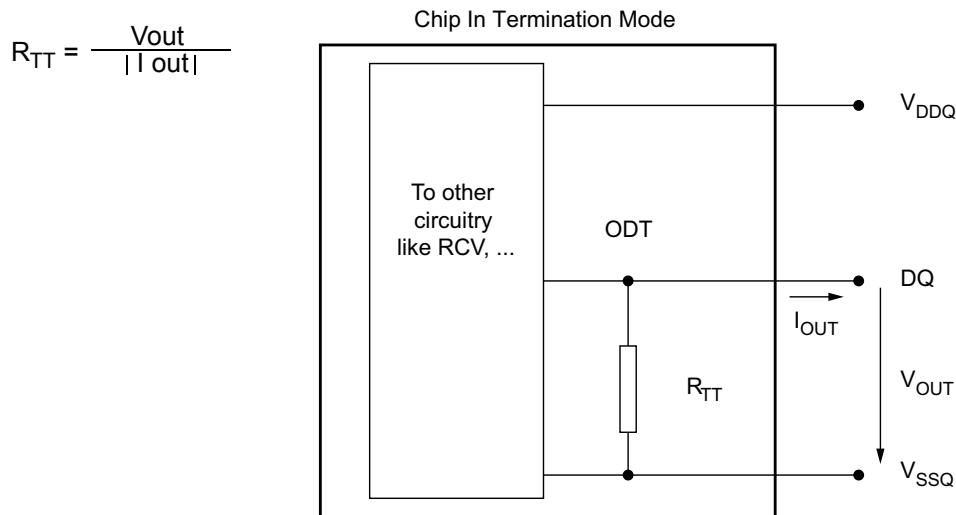


Figure 82 — On Die Termination

4.35 On-Die Termination (ODT) for DQ, DQS, and DMI (cont'd)

Table 61 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω +/-1% over the entire operating temperature range after a proper ZQ calibration.

MR11 OP[2:0]	RTT	Vout	Min	Nom	Max	Unit	Notes
001	240Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ	1,2,3
010	120Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ/2	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ/2	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ/2	1,2,3
011	80Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ/3	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ/3	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ/3	1,2,3
100	60Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ/4	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ/4	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ/4	1,2,3
101	48Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ/5	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ/5	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ/5	1,2,3
110	40Ω	VOLdc= 0.1* V _{DDQ}	0.8	1	1.1	RZQ/6	1,2,3
		VOMdc= 0.33* V _{DDQ}	0.9	1	1.1	RZQ/6	1,2,3
		VOHdc= 0.5* V _{DDQ}	0.9	1	1.2	RZQ/6	1,2,3
Mismatch DQ-DQ within byte		0.33* V _{DDQ}	-		2	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see "voltage and temperature sensitivity"¹.

NOTE 2 Pull-dn ODT resistors are recommended to be calibrated at 0.33*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5*V_{DDQ} and 0.1*V_{DDQ}.

NOTE 3 Measurement definition for RTT: TBD¹

NOTE 4 DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).

$$\text{DQ - DQ Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$

1. As of publication of this document, under discussion by the formulating committee.

4.36 Power-Down Mode

4.36.1 Power-Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOW while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- V_{REF}(CA) Range and Value setting via MRW
- V_{REF}(DQ) Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

And the LPDDR4 DRAM cannot be placed in power-down state during "Start DQS Interval Oscillator" operation.

CKE can go LOW while any other operations such as row activation, Precharge, Auto Precharge, or Refresh are in progress. The power-down I_{DD} specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 83.

Entering power-down deactivates the input and output buffers, excluding CKE and Reset_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable Low level and CA input level is don't care after CKE is driven LOW, this timing period is defined as tCKELCS. Clock input is required after CKE is driven LOW, this timing period is defined as tCKELCK. CKE LOW will result in deactivation of all input receivers except Reset_n after tCKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except Reset_n are "Don't Care". CKE LOW must be maintained until tCKE,min is satisfied.

V_{DDQ} can be turned off during power-down. Prior to exiting power-down, V_{DDQ} must be within its minimum/maximum operating range.

No refresh operations are performed in power-down mode except Self-Refresh power-down. The maximum duration in non-Self-Refresh power-down mode is only limited by the refresh requirements outlined in 4.12, Refresh command.

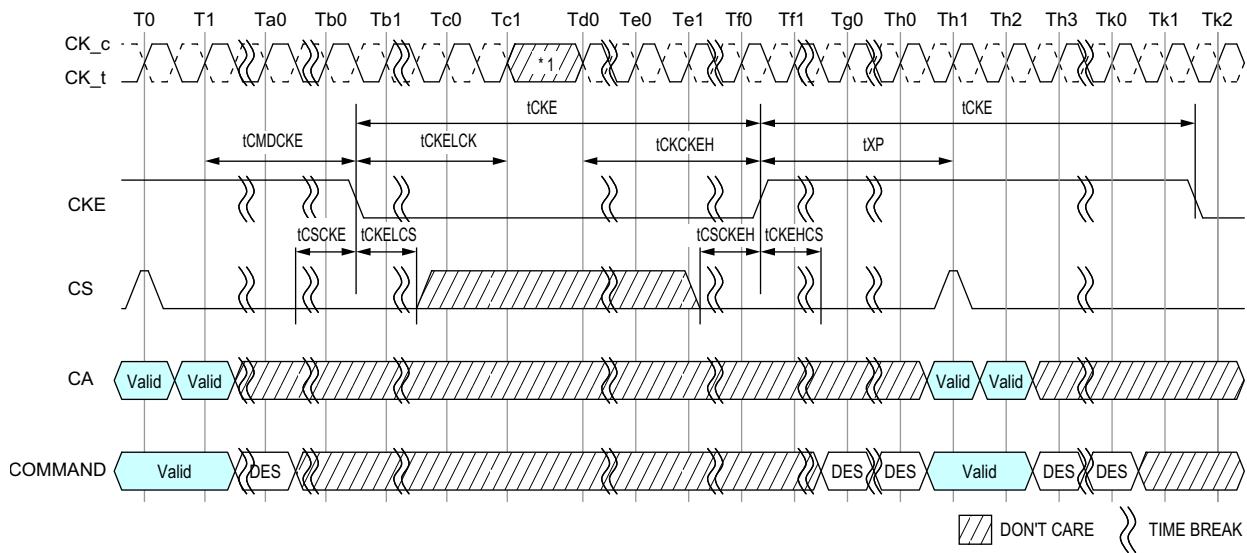
The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in Table 62.

Clock frequency change or Clock Stop is inhibited during tCMDCKE, tCKELCK, tCKCKEH, tXP, tMRWCKEL and tZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And If power-down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh power-down in which the internal refresh is continuing in the same way as Self Refresh mode.

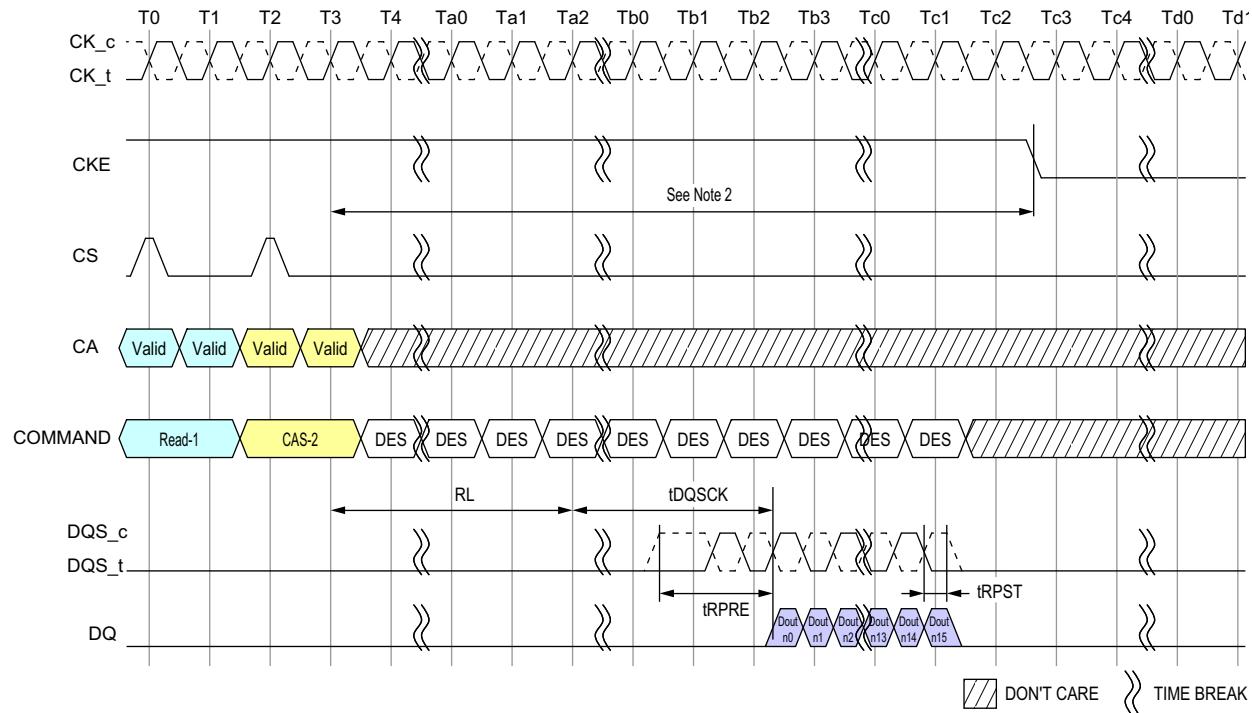
When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including power-down.

4.36.1 Power-Down Entry and Exit (cont'd)



NOTES : 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

Figure 83 — Basic Power-Down Entry and Exit Timing



NOTES : 1. CKE must be held HIGH until the end of the burst operation.

2. Minimum Delay time from Read Command or Read with Auto Precharge Command to falling edge of CKE signal is as follows.

Read Post-amble = 0.5nCK : MR1 OP[7]=0 : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 1tCK

Read Post-amble = 1.5nCK : MR1 OP[7]=1 : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 2tCK

Figure 84 — Read and Read with Auto Precharge to Power-Down Entry

4.36.1 Power-Down Entry and Exit (cont'd)

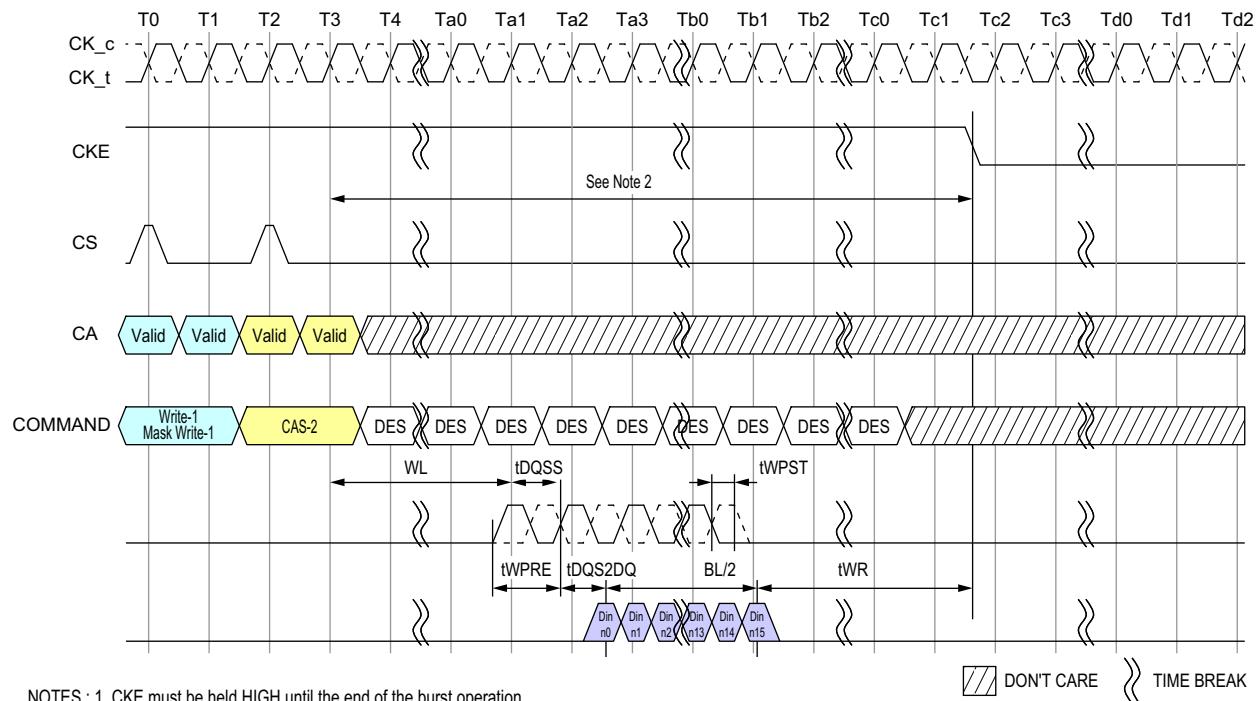


Figure 85 — Write and Mask Write to Power-Down Entry

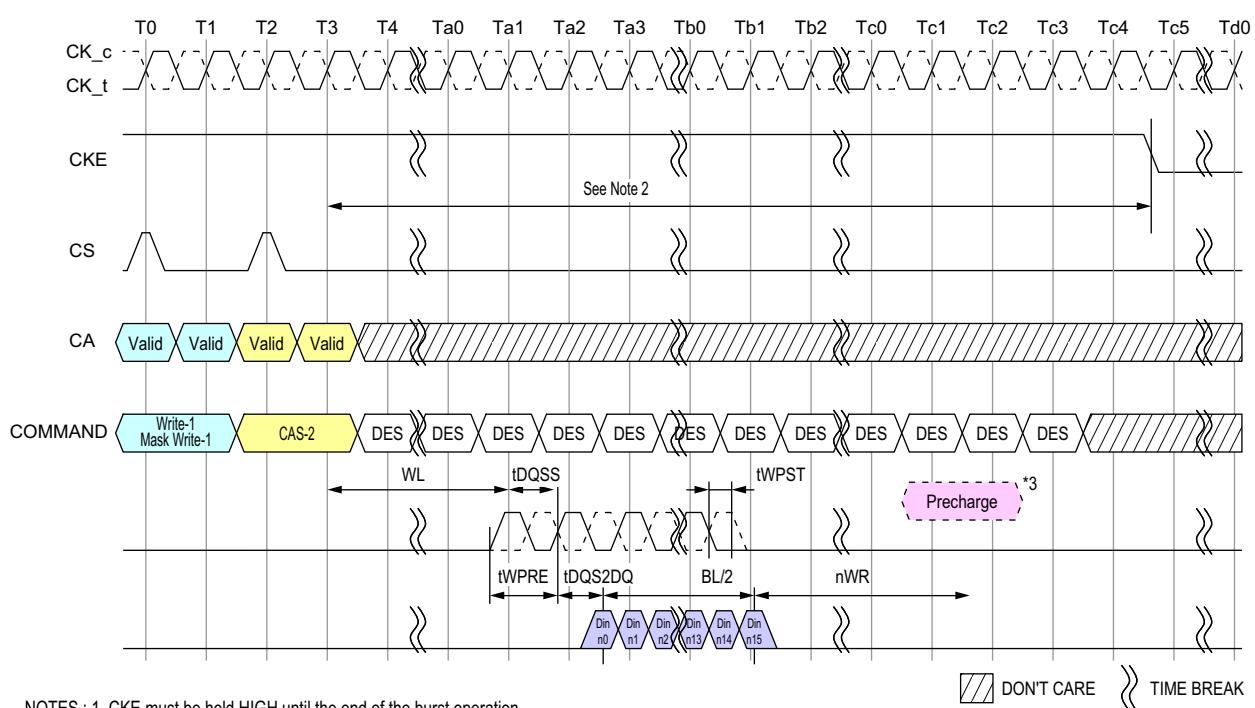


Figure 86 — Write with Auto Precharge and Mask Write with Auto Precharge to Power-Down Entry

4.36.1 Power-Down Entry and Exit (cont'd)

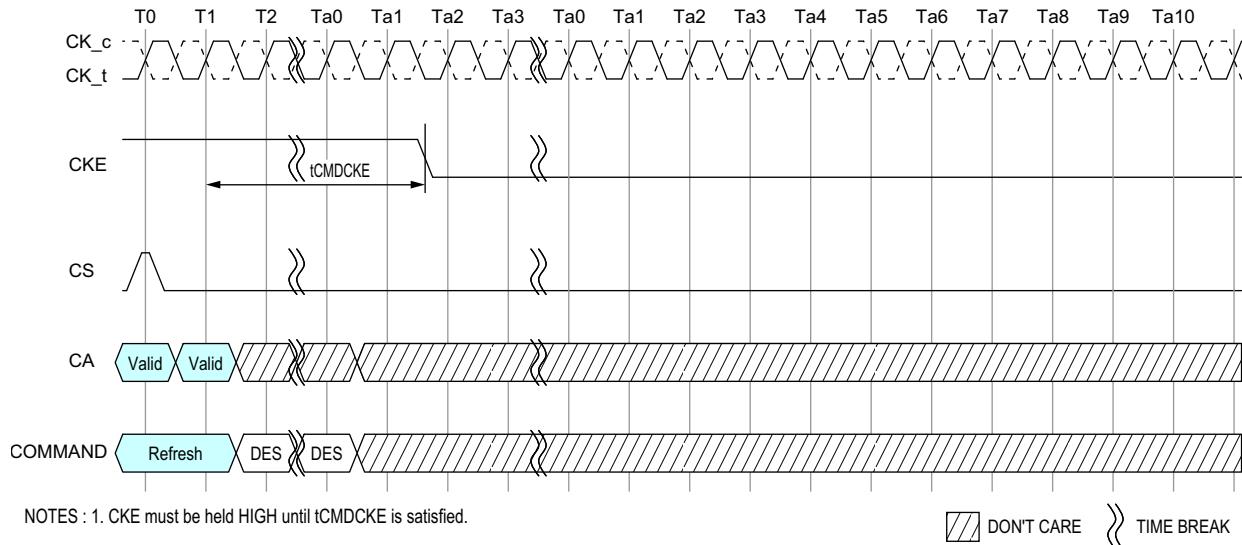


Figure 87 — Refresh entry to Power-Down Entry

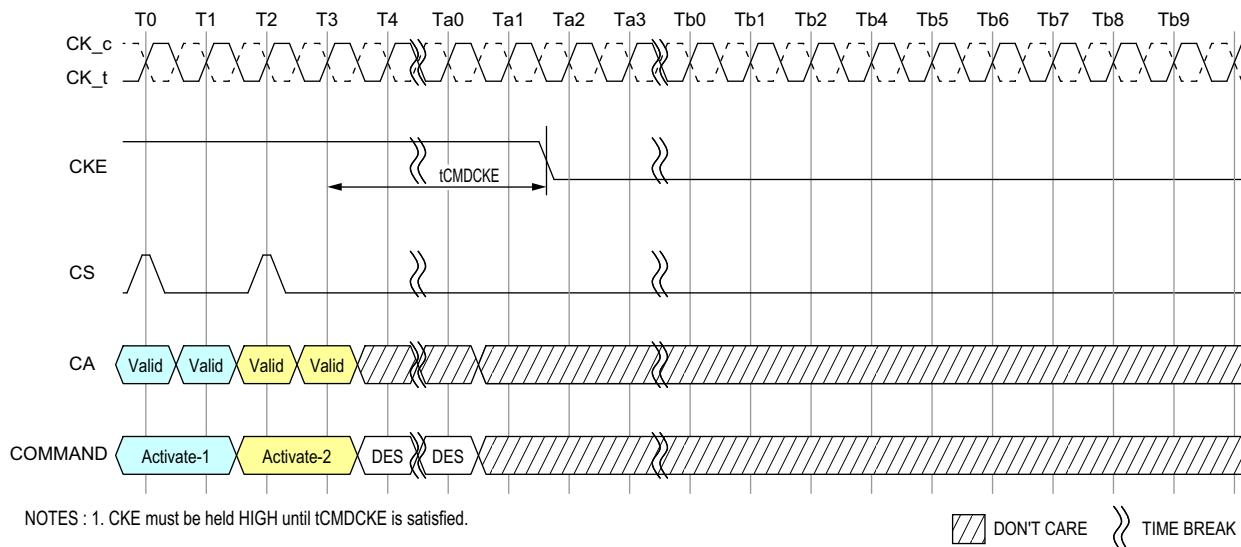


Figure 88 — Activate Command to Power-Down Entry

4.36.1 Power-Down Entry and Exit (cont'd)

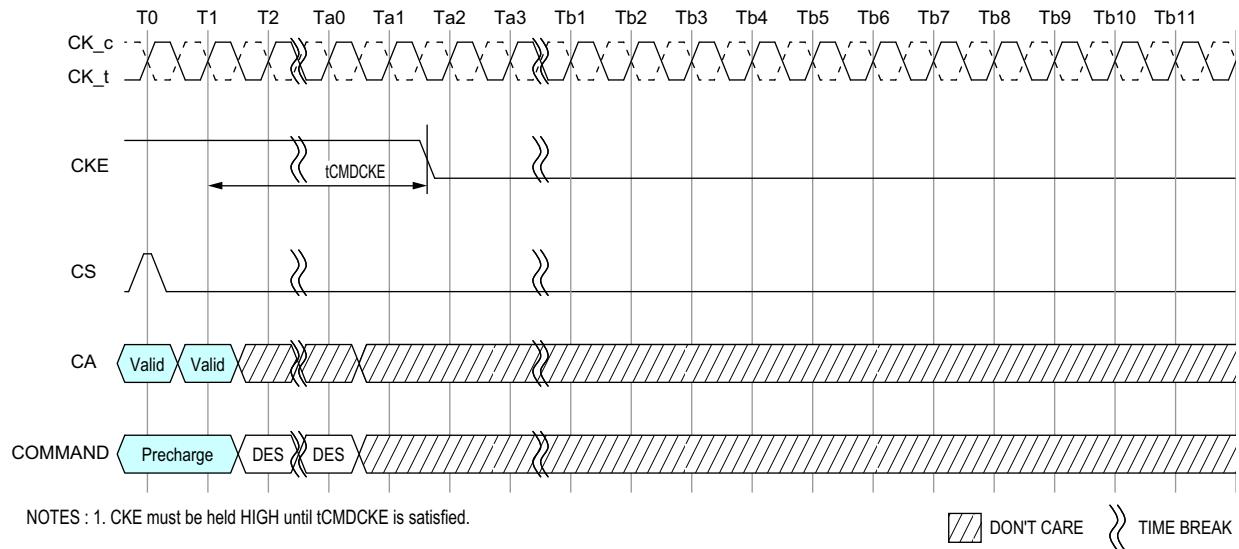


Figure 89 — Precharge Command to Power-Down Entry

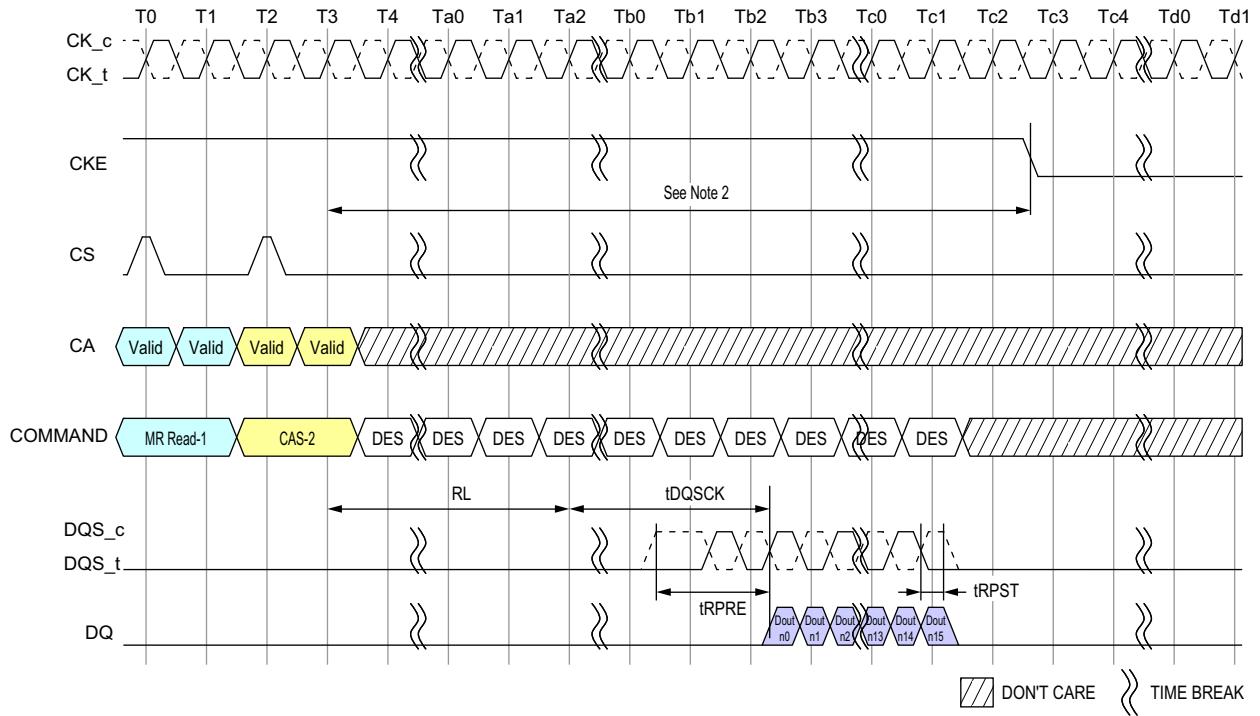


Figure 90 — Mode Register Read to Power-Down Entry

4.36.1 Power-Down Entry and Exit (cont'd)

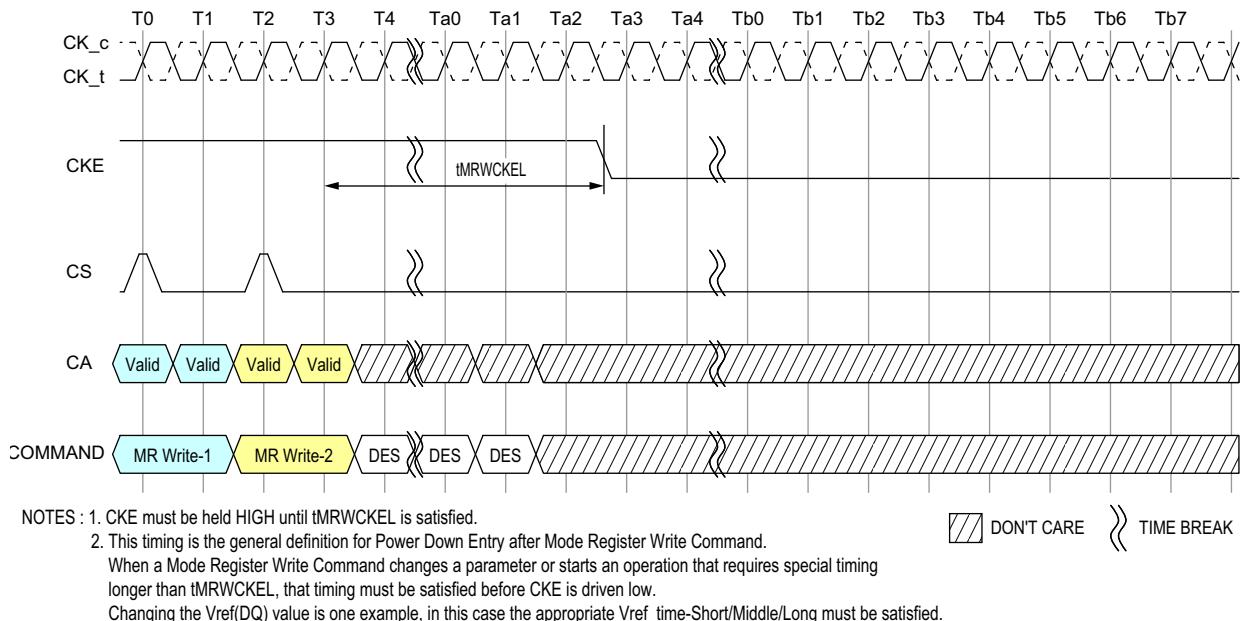


Figure 91 — Mode Register Write to Power-Down Entry

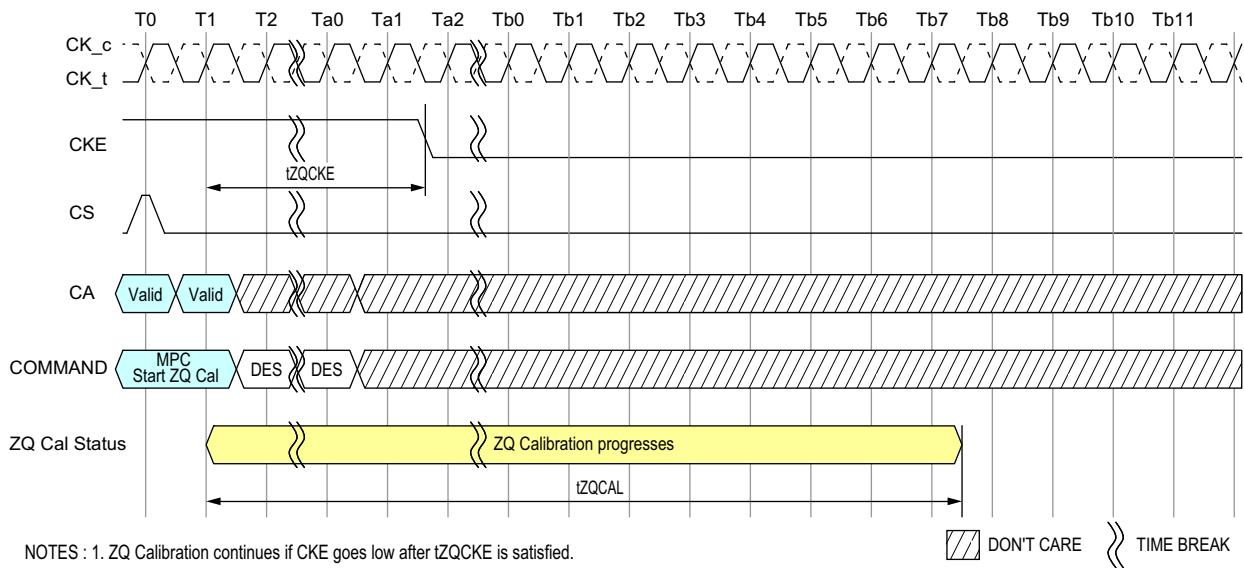


Figure 92 — Multi purpose Command for Start ZQ Calibration to Power-Down Entry

4.36.1 Power-Down Entry and Exit (cont'd)

Table 62 — Power-Down AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	Max(7.5ns, 4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns, 5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns, 5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns, 3nCK)	ns	1

NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK).

For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.

The case which 3nCK is applied to is shown in Figure 93.

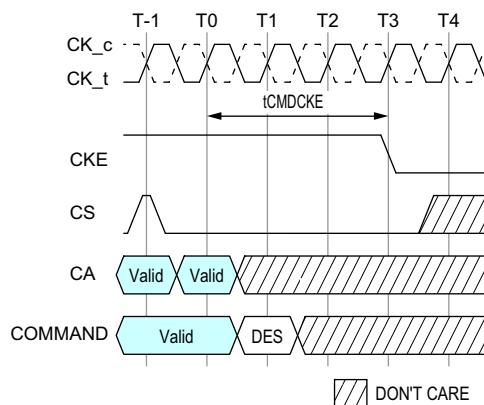


Figure 93 — tCMDCKE Timing

4.37 Input Clock Stop and Frequency Change

LPDDR4 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 4 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 4 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH

LPDDR4 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- CS shall be held LOW during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR4 SDRAM is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS shall be held LOW during clock clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
- The LPDDR4 SDRAM is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

4.38 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4 device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held High when the commands listed in Table 63 — Command Truth Table input.

4.38.1 Command Truth Table

Table 63 — Command Truth Table

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Deselect (DES)	L	X						R1	1,2
Multi Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,2,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,2,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,2,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

4.38.1 Command Truth Table (cont'd)

Table 63 — Command Truth Table (cont'd)

	SDR Command Pins	SDR CA Pins (6)								
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes	
RFU	H	L	H	H	H	H	V	R1	1,2	
	L	V						R2		
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10	
	L	BA0	BA1	BA2	V	R10	R11	R2		
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10	
	L	R0	R1	R2	R3	R4	R5	R2		

NOTE 1 All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.

NOTE 2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CS, CK_t, CK_c and CA[5:0] can be floated.

NOTE 3 Bank addresses BA[2:0] determine which bank is to be operated upon.

NOTE 4 AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.

NOTE 5 Mask Write-1 command supports only BL 16. For Mask Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).

NOTE 6 AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.

NOTE 7 If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".

NOTE 8 For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO and Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.

NOTE 9 Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO and Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.

NOTE 10 Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.

NOTE 11 MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.

NOTE 12 MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

4.39 TRR Mode - Target Row Refresh

A LPDDR4 SDRAM's row has a limited number of times a given row can be accessed within a refresh period ($tREFW * 2$) prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive actives is the Target Row (TRn), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TRn, either the LPDDR4 SDRAM receive all ($R * 2$) Refresh Commands before another row activate is issued, or the LPDDR4 SDRAM should be placed into Targeted Row Refresh (TRR) mode. The TRR Mode will re-fresh the rows adjacent to the TRn that encountered tMAC limit.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the actives from the two target rows on a victim row in a bank should not exceed MAC value as well.

MR24 fields required to support the new TRR settings. Setting MR24 [OP7=1] enables TRR Mode and setting MR24 [OP7=0] disables TRR Mode. MR24 [OP6:OP4] defines which bank (BAn) the target row is located in (See 3.4.24, MR24 table for details).

The TRR mode must be disabled during initialization as well as any other LPDDR4 SDRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR24 [OP7=0] to interrupt and reissue the TRR mode is allowed.

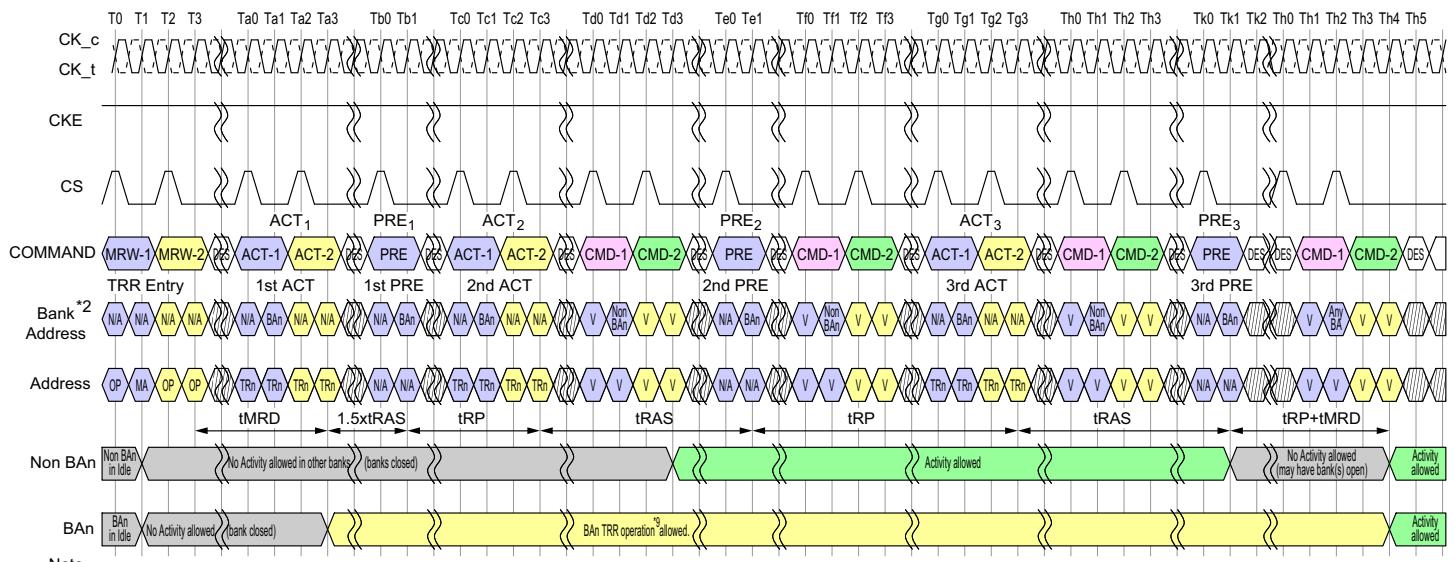
When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus tMRD. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR24 [OP7=0]; if the TRR is exited via another MRS command, the value written to MR24 [OP6:OP4] are don't cares.

4.39.1 TRR Mode Operation

1. The timing diagram in Figure 94 depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three corresponding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. A Precharge All (PREA) commands issued while LPDDR4 SDRAM is in TRR mode will also perform precharge to BAn and counts towards a PREn command.
2. Prior to issuing the MRW command to enter TRR mode, the SDRAM should be in the idle state. A MRW command must be issued with MR24 [OP7=1] and MR24 [OP6:4] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.
3. No activity is to occur in the DRAM until tMRD has been satisfied. Once tMRD has been satisfied, the only commands to BAn allowed are ACT and PRE until the TRR mode has been completed.
4. The first ACT to the BAn with the TRn address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until $[(1.5 * tRAS) + tRP]$ is satisfied.
5. After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued $(1.5 * tRAS)$ later; and then followed tRP later by the second ACT to the BAn with the TRn address. Once the 2nd activate to the BAn is issued, nonBAn banks are allowed to have activity.
6. After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the TRn address.

4.39.1 TRR Mode Operation (cont'd)

7. After the third ACT to the BA_n with the TR_n address is issued, a PRE to BA_n would be issued tRAS later; and once the third PRE has been issued, nonBA_n banks are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMRD is satisfied.
8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any-time the TRR mode is interrupted and not completed, the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR24 change is required with setting MR24 [OP7=0], MR24 [OP6:4] are don't care, followed by three PRE to BA_n, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.
9. Refresh command to the LPDDR4 SDRAM or entering Self-Refresh mode is not allowed while the DRAM is in TRR mode.



Note

1. TR_n is targeted row.
2. Bank BA_n represents the bank in which the targeted row is located.
3. TRR mode self-clears after tMRD + tRP measured from 3rd BA_n precharge PRE3 at clock edge Th4.
4. TRR mode or any other activity can be re-engaged after tRP + tMRD from 3rd BA_n precharge PRE3. PRE_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE3 to the BA_n bank.
5. Activate commands to BA_n during TRR mode do not provide refreshing support, i.e. the Refresh counter is unaffected.
6. The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row (TR_n) necessary to meet refresh requirements.
7. A new TRR mode must wait tMRD+tRP time after the third precharge.
8. BA_n may not be used with any other command.
9. ACT and PRE are the only allowed commands to BA_n during TRR Mode.
10. Refresh commands are not allowed during TRR mode.
11. All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1, ACT2 and ACT3 counts towards tFAW budget.

Figure 94 — TRR Mode

4.40 Post Package Repair (PPR)

LPDDR4 supports Fail Row address repair as optional feature and it is readable through MR25 OP[7:0]. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4 can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

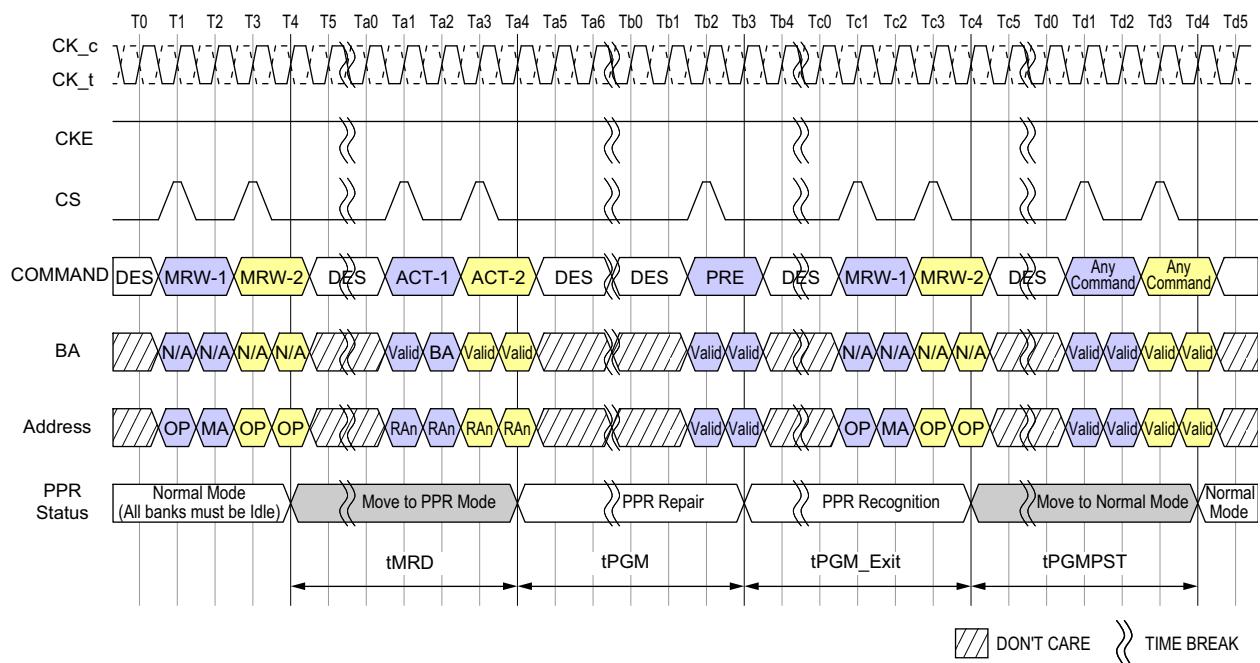
4.40.1 Fail Row Address Repair

The following is procedure of PPR.

1. Before entering 'PPR' mode, All banks must be Precharged
2. Enable PPR using MR4 bit "OP4=1" and wait tMRD
3. Issue ACT command with Fail Row address
4. Wait tPGM to allow DRAM repair target Row Address internally then issue PRE
5. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address RAn
6. Exit PPR with setting MR4 bit "OP4=0"
7. LPDDR4 will accept any valid command after tPGMPST
8. In More than one fail address repair case, Repeat Step 2 to 7

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [OP4=0] and tPGMPST.

The following Timing diagram shows PPR operation.



NOTE 1 During tPGM, any other commands (including refresh) are not allowed on each die.

NOTE 2 With one PPR command, only one row can be repaired at one time per die.

NOTE 3 When PPR procedure is done, reset command is required before normal operation.

NOTE 4 During PPR, memory contents is not refreshed and may be lost.

Figure 95 — PPR Timing

Table 64 — PPR Timing Parameters

Parameter	Symbol	min	max	Unit	Note
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting time	tPGMPST	50	-	us	

5 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this standard are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 65 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.5	V	1
Voltage on any ball except V_{DD1} relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

NOTE 1 See "Power-Ramp" in 3.3 for relationships between power supplies.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.

6 AC and DC Operating Conditions

6.1 Recommended DC Operating Conditions

Table 66 — Recommended DC Operating Conditions

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.5	V	1
Voltage on any ball except V_{DD1} relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.

NOTE 3 The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mv at the DRAM ball is not included in the TdIVW.

7 AC and DC Input/Output Measurement Levels

7.1 V High speed LVC MOS (HS_LLVC MOS)

This standard defines power supply voltage range, dc interface, switching parameter and overshoot/undershoot for high speed lower low-voltage CMOS family of non terminated digital circuits. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.

The purpose of this standard is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

7.1.1 Standard specifications

All voltages are referenced to ground except where noted.

7.1.2 Recommended DC Operating conditions

Table 67 — Recommended DC operating conditions

	Min.	Typ.	Max.	Unit	
V_{DD}	1.06	1.1	1.17	V	Input Buffer Power
V_{DDQ}	1.06	1.1	1.17	V	I/O Buffer Power

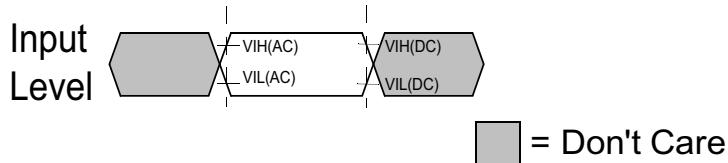
7.1.3 DC electrical characteristics

7.1.3.1 Class-1 LPDDR4 Input Level

Table 68 — Class-1 LPDDR4 Input Level

Parameter	Symbol	Min	Max	Unit	Note
Input high level (AC)	$VIH(AC)$	$0.75*V_{DD}(or V_{DDQ})$	$V_{DD}(or V_{DDQ})+0.2$	V	1
Input low level (AC)	$VIL(AC)$	-0.2	$0.25*V_{DD}(or V_{DDQ})$	V	1
Input high level (DC)	$VIH(DC)$	$0.65*V_{DD}(or V_{DDQ})$	$V_{DD}(or V_{DDQ})+0.2$	V	
Input low level (DC)	$VIL(DC)$	-0.2	$0.35*V_{DD}(or V_{DDQ})$	V	

NOTE 1 Refer 7.1.4, LPDDR4 AC Over/Undershoot.



Note
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

Figure 96 — Class-1 LPDDR4 Input AC timing definition

7.1.3.2 Class-1 LPDDR4 Output measurement Level

Table 69 — Class-1 LPDDR4 Output measurement Level

Parameter	Symbol	Min	Max	Unit
Output high voltage	VOH	$0.80 * V_{DDQ}$	-	V
Output low voltage	VOL	-	$0.20 * V_{DDQ}$	V

7.1.4 AC Over/Ubershoot

7.1.4.1 Class-1 LPDDR4 AC Over/Ubershoot

Table 70 — Class 1 LPDDR4 AC Over/Ubershoot

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35V
Maximum peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above V_{DD}/V_{DDQ}	0.8V·ns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.8V·ns

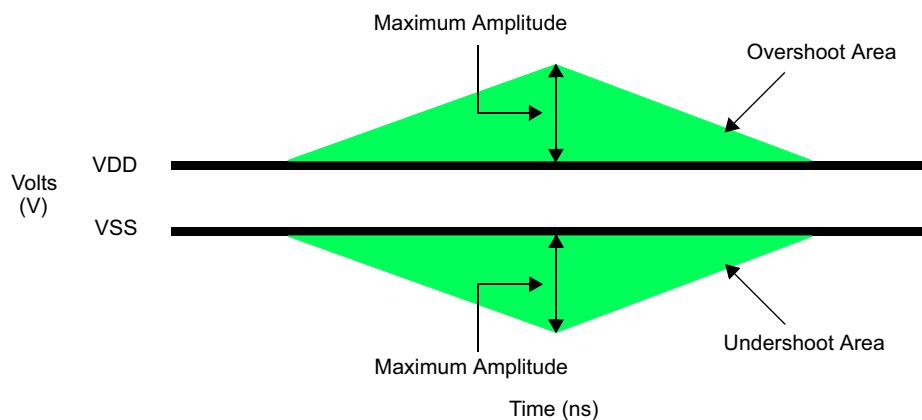


Figure 97 — AC Overshoot and Undershoot Definition for Address and Control Pins

7.2 Differential Input Cross Point Voltage

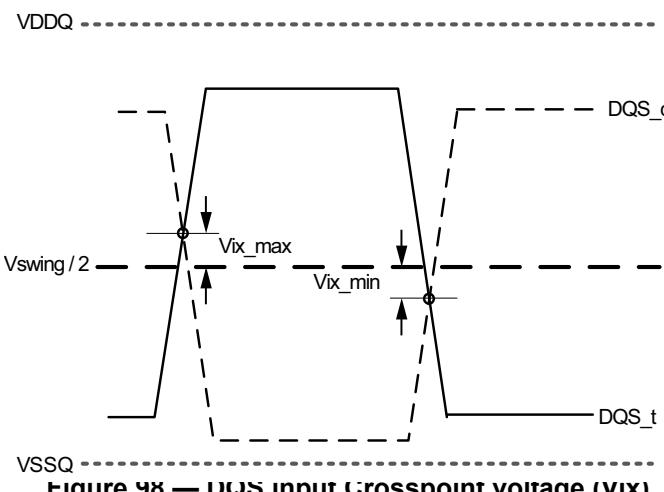


Figure 98 — DQS Input Crosspoint voltage (Vix)

Table 71 — QS input voltage crosspoint(Vix) ratio

Parameter	Symbol	LPDDR4-2133		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max		
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	20	-	20	-	20	%	1,2

NOTE 1 Vix voltage is referenced to $V_{swing}/2(\text{avg}) = 0.5(VDQS_t + VDQS_c)$ where the average is over (TBD¹) UI.

NOTE 2 Ratio of the Vix pk voltage divided by Vdiff_DQS : $\text{Vix_DQS_Ratio} = 100^* (\text{Vix_DQS}/\text{Vdiff DQS pkpk})$ where $\text{VdiffDQS pk-pk} = 2*|VDQS_t - VDQS_c|$

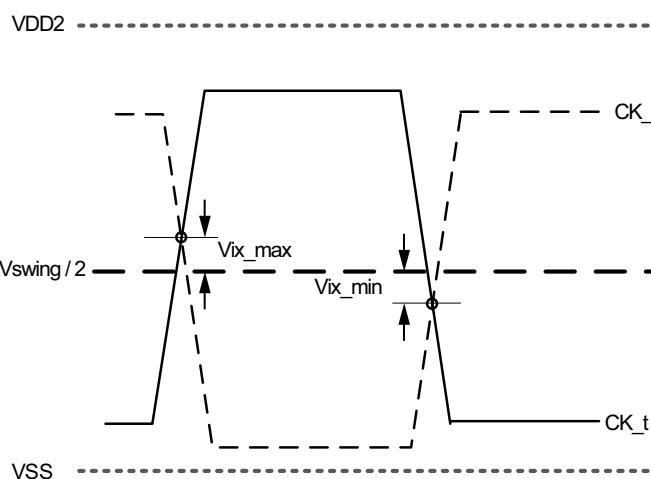


Figure 99 — CK input Crosspoint voltage (Vix)

Table 72 — CK input voltage crosspoint(Vix) ratio

Parameter	Symbol	LPDDR4-2133		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max		
CK Differential input crosspoint voltage ratio	Vix_CK_ratio	-	25	-	25	-	25	%	1,2

NOTE 1 Vix voltage is referenced to $V_{swing}/2(\text{avg}) = 0.5(VCK_t + VCK_c)$ where the average is over (TBD¹) UI.

NOTE 2 Ratio of the Vix pk voltage divided by Vdiff_CK : $\text{Vix_CK_Ratio} = 100^* (\text{Vix_CK}/\text{Vdiff CK pk-pk})$ where $\text{VdiffCK pk-pk} = 2*|VCK_t - VCK_c|$

1. As of publication of this document, under discussion by the formulating committee.

7.3 AC/DC Input level for ODT input

Table 73 — LPDDR4 Input Level for ODT

Symbol		Min	Max	Unit	Note
VIHODT(AC)	ODT Input High Level (AC)	0.75*V _{DD}	V _{DD} +0.2	V	1
VILODT(AC)	ODT Input Low Level (AC)	-0.2	0.25*V _{DD}	V	1
VIHODT(DC)	ODT Input High Level (DC)	0.65*V _{DD}	V _{DD} +0.2	V	
VILODT(DC)	ODT Input Low Level (DC)	-0.2	0.35*V _{DD}	V	

NOTE 1 See Table 76, Overshoot and Undershoot Specifications.

7.4 Single Ended Output Slew Rate

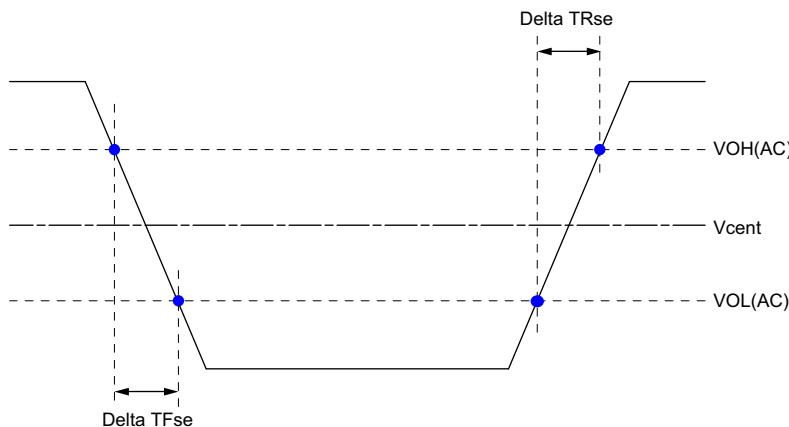


Figure 100 — Single Ended Output Slew Rate Definition

Table 74 — Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min ¹	Max ²	
Single-ended Output Slew Rate (VOH = V _{DD} Q/3)	SRQse*	3.5	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-

* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) se = Single-ended signals

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(AC) and VOH(AC)= 0.8*VOH(AC).

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.4 Single Ended Output Slew Rate (cont'd)

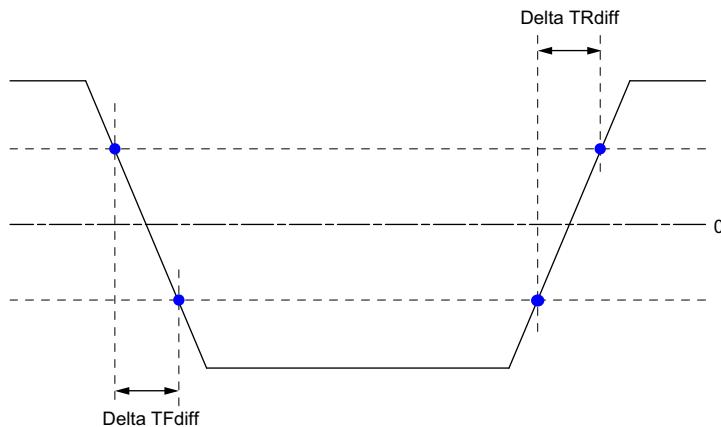


Figure 101 — Differential Output Slew Rate Definition

Table 75 — Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate ($V_{OH}=V_{DD}Q/3$)	SRQdiff*	7	18	V/ns

* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) diff = Differential signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between $VOL(AC)=0.2*V_{OH}(DC)$ and $V_{OH}(AC)= 0.8*V_{OH}(DC)$.

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.5 Overshoot and Undershoot for LVSTL

Table 76 — AC Overshoot/Undershoot Specification

Parameter		Data Rate				Units
		1600	1866	3200	4266	
Maximum peak amplitude allowed for overshoot area. (See Figure 102)	Max	0.3	0.3	0.3	TBD	V
Maximum peak amplitude allowed for undershoot area. (See Figure 102)	Max	0.3	0.3	0.3	TBD	V
Maximum area above V_{DD} . (See Figure 102)	Max	0.1	0.1	0.1	TBD	V-ns
Maximum area below V_{SS} . (See Figure 102)	Max	0.1	0.1	0.1	TBD	V-ns

NOTE 1 V_{DD2} stands for V_{DD} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for V_{DDQ} for DQ, DMI, DQS_t and DQS_c.

NOTE 2 V_{SS} stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t and DQS_c.

NOTE 3 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.

NOTE 4 Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

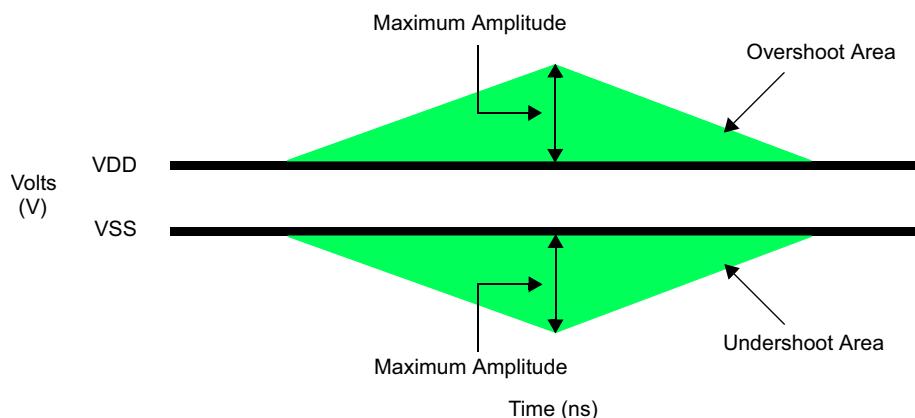
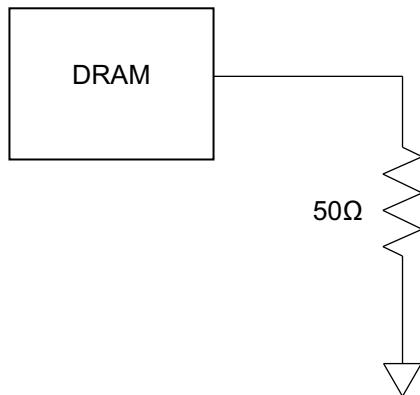


Figure 102 — Overshoot and Undershoot Definition

7.6 LPDDR4 Driver Output Timing Reference load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Note

1. All output timing parameter values are reported with respect to this reference load.
This reference load is also used to report slew rate.

Figure 103 — Driver Output Reference Load for Timing and Slew Rate

7.7 LVSTL(Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down dirver and a terminator. The basic cell is shown in Figure104.

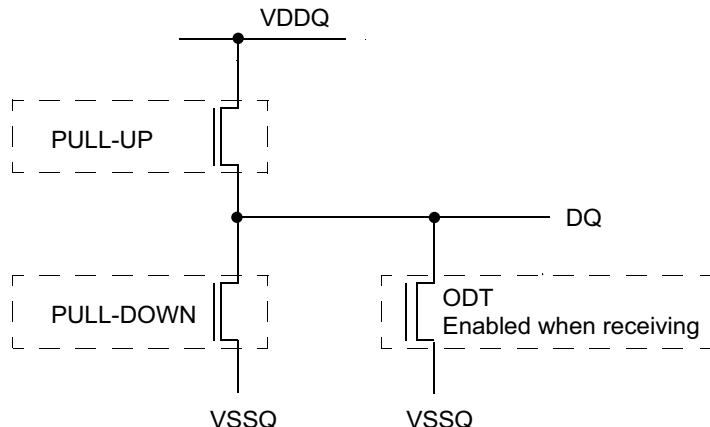


Figure 104 — LVSTL I/O Cell

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to be calibrated per the following procedure:

1. Calibrate the pull-down device against a 240 Ohm resister to V_{DDQ} via the ZQ pin.
 - Set Strength Control to minimum setting.
 - Increase drive strength until comparator detects data bit is less than $V_{DDQ}/2$.
 - NMOS pull-down device is calibrated to 240 Ohms.

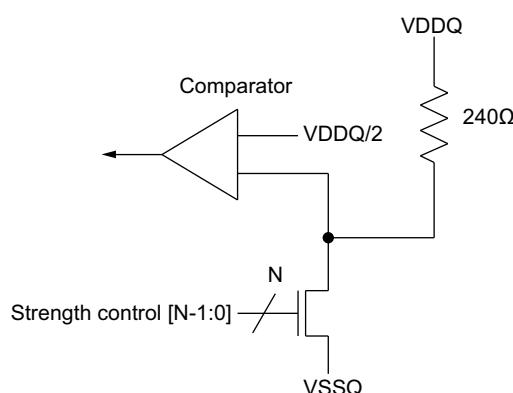


Figure 105 — Pull-down Calibration

7.7 LVSTL(Low Voltage Swing Terminated Logic) IO System (cont'd)

2. Calibrate the pull-up device against the calibrated pull-down device.

- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is grater than VOH target.
- NMOS pull-up device is now calibrated to VOH target.

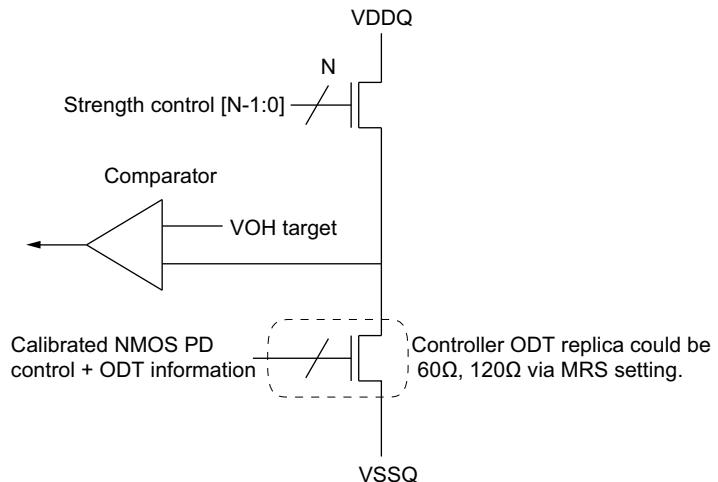


Figure 106 — Pull-up Calibration

8 Input/Output Capacitance

Table 77 — Input/output capacitance

Parameter	Symbol		LPDDR4 3200-533	LPDDR4 4266-3733	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	0.5	TBD	pF	1,2
		Max	0.9	TBD	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	TBD	pF	1,2,3
		Max	0.09	TBD	pF	1,2,3
Input capacitance, All other input-only pins	CI	Min	0.5	TBD	pF	1,2,4
		Max	0.9	TBD	pF	1,2,4
Input capacitance delta, All other input-only pins	CDI	Min	-0.1	TBD	pF	1,2,5
		Max	0.1	TBD	pF	1,2,5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	TBD	pF	1,2,6
		Max	1.3	TBD	pF	1,2,6
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0.0	TBD	pF	1,2,7
		Max	0.1	TBD	pF	1,2,7
Input/output capacitance delta, DQ, DMI	CDIO	Min	-0.1	TBD	pF	1,2,8
		Max	0.1	TBD	pF	1,2,8
Input/output capacitance, ZQ pin	CZQ	Min	0.0	TBD	pF	1,2
		Max	5.0	TBD	pF	1,2

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating.

NOTE 3 Absolute value of CCK_t . CCK_c.

NOTE 4 CI applied to CS_n, CKE, CA0~CA5.

NOTE 5 CDI = CI . 0.5 * (CCK_t + CCK_c)

NOTE 6 DMI loading matches DQ and DQS.

NOTE 7 Absolute value of CDQS_t and CDQS_c.

NOTE 8 CDIO = CIO . 0.5 * (CDQS_t + CDQS_c) in byte-lane.

9 I_{DD} Specification Parameters and Test Conditions

9.1 I_{DD} Measurement Conditions

The following definitions are used within the I_{DD} measurement tables unless stated otherwise:

LOW: VIN ≤ VIL(DC) MAX

HIGH: VIN ≥ VIH(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 78 and Table 79.

Table 78 — Definition of Switching for CA Input Signals

Switching for CA								
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH							
CS	LOW							
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 CS must always be driven LOW.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The above pattern is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 79 — CA pattern for I_{DD4R}

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 BA[2:0] = 010, CA[9:4] = 000000 or 111111, Burst Order CA[3:2] = 00 or 11 (Same as JESD209-3, Table 57)

NOTE 2 Difference from JESD209-3: CA pins are kept low with DES CMD to reduce ODT current.

9.1 I_{DD} Measurement Conditions (cont'd)

Table 80 — CA pattern for I_{DD4W}

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as JESD209-3, Table 58)

NOTE 2 Difference from JESD209-3: a) No burst ordering, and b) CA pins are kept low with DES CMD to reduce ODT current.

9.1 I_{DD} Measurement Conditions (cont'd)Table 81 - Data Pattern for $I_{DD}4W$ (DBI off)

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	0	2
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	0	0	0	6
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	0	0	0	6
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	0	2
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE 1 Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for $I_{DD}4W/R$ pattern programming.

9.1 I_{DD} Measurement Conditions (cont'd)

Table 82 — Data Pattern for $I_{DD}4R$ (DBI off)

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE 1 Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for $I_{DD}4W/R$ pattern programming.

9.1 I_{DD} Measurement Conditions (cont'd)Table 83 — Data Pattern for $I_{DD}4W$ (DBI on)

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	0	2
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	1	3
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	1	3
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	0	2
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	



DBI enabled burst

9.1 I_{DD} Measurement Conditions (cont'd)

Table 84 — Data Pattern for I_{DD4R} (DBI on)

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

 DBI enabled burst

9.2 I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of $I_{DD}6ET$ which is for the entire extended temperature range.

Table 85 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD0_1}	V_{DD1}	
	I_{DD0_2}	V_{DD2}	
	I_{DD0_Q}	V_{DDQ}	3
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2P_1}	V_{DD1}	
	I_{DD2P_2}	V_{DD2}	
	I_{DD2P_Q}	V_{DDQ}	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2PS_1}	V_{DD1}	
	I_{DD2PS_2}	V_{DD2}	
	I_{DD2PS_Q}	V_{DDQ}	3
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2N_1}	V_{DD1}	
	I_{DD2N_2}	V_{DD2}	
	I_{DD2N_Q}	V_{DDQ}	3
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2NS_1}	V_{DD1}	
	I_{DD2NS_2}	V_{DD2}	
	I_{DD2NS_Q}	V_{DDQ}	3

9.2 I_{DD} Specifications (cont'd)

Table 85 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions (cont'd)

Parameter/Condition	Symbol	Power Supply	Notes
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3P_1}	V_{DD1}	
	I_{DD3P_2}	V_{DD2}	
	I_{DD3P_Q}	V_{DDQ}	3
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3PS_1}	V_{DD1}	
	I_{DD3PS_2}	V_{DD2}	
	I_{DD3PS_Q}	V_{DDQ}	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3N_1}	V_{DD1}	
	I_{DD3N_2}	V_{DD2}	
	I_{DD3N_Q}	V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3NS_1}	V_{DD1}	
	I_{DD3NS_2}	V_{DD2}	
	I_{DD3NS_Q}	V_{DDQ}	4
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 8; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4R_1}	V_{DD1}	
	I_{DD4R_2}	V_{DD2}	
	I_{DD4R_Q}	V_{DDQ}	5

9.2 I_{DD} Specifications (cont'd)

Table 85 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions (cont'd)

Parameter/Condition	Symbol	Power Supply	Notes
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4W_1}	V_{DD1}	
	I_{DD4W_2}	V_{DD2}	
	I_{DD4W_Q}	V_{DDQ}	4
All-bank REFRESH Burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD5_1}	V_{DD1}	
	I_{DD5_2}	V_{DD2}	
	I_{DD5Q}	V_{DDQ}	4
All-bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD5AB_1}	V_{DD1}	
	I_{DD5AB_2}	V_{DD2}	
	I_{DD5AB_Q}	V_{DDQ}	4
Per-bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD5PB_1}	V_{DD1}	
	I_{DD5PB_2}	V_{DD2}	
	I_{DD5PB_Q}	V_{DDQ}	4
Self refresh current (-25°C to +85°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled	I_{DD6_1}	V_{DD1}	6,7,8,10
	I_{DD6_2}	V_{DD2}	6,7,8,10
	I_{DD6Q}	V_{DDQ}	4,6,7,8,10

NOTE 1 Published I_{DD} values are the maximum of the distribution of the arithmetic mean.

NOTE 2 ODT disabled: MR11[2:0] = 000B.

NOTE 3 I_{DD} current specifications are tested after the device is properly initialized.

NOTE 4 Measured currents are the summation of V_{DDQ} and V_{DD2} .

NOTE 5 Guaranteed by design with output load = 5pF and RON = 40 ohm.

NOTE 6 The 1x Self-Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.

NOTE 7 This is the general definition that applies to full array Self Refresh.

NOTE 8 Supplier datasheets may contain additional Self Refresh I_{DD} values for temperature subranges within the Standard or elevated Temperature Ranges.

NOTE 9 For all I_{DD} measurements, VIHCKE = 0.8 × V_{DD2} , VILCKE = 0.2 × V_{DD2} .

NOTE 10 I_{DD6} 85°C is guaranteed, I_{DD6} 45°C is typical of the distribution of the arithmetic mean.

10 Electrical Characteristics and AC Timing

10.1 Clock Timing

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

10.2 Core Timing

Table 89 — Core AC Timing

Parameter	Symbol	Min/Max	Data Rate								Unit
Core Parameters			533	1066	1600	2133	2667	3200	3733	4267	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns
Minimum Self-Refresh Time (Entry to Exit)	tSR	MIN	max(15ns, 3nCK)								ns
SELF REFRESH exit to next valid command delay	tXSR	MIN	max(tRFCab + 7.5ns, 2nCK)								ns
Exit Power-Down to next valid command delay	tXP	MIN	max(7.5ns, 3nCK)								ns
CAS-to-CAS delay	tCCD	MIN	8								tCK(avg)
Internal READ to PRECHARGE command delay	tRTP	MIN	max(7.5ns, 8nCK)								ns
RAS-to-CAS delay	tRCD	MIN	max(18ns, 4nCK)								ns
Row precharge time (single bank)	tRPpb	MIN	max(18ns, 3nCK)								ns
Row precharge time (all banks)	tRPab	MIN	max(21ns, 3nCK)								ns
Row active time	tRAS	MIN	max(42ns, 3nCK)								ns
		MAX	Min(9 * tREFI * Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])								-
WRITE recovery time	tWR	MIN	max(18ns, 4nCK)								ns
WRITE-to-READ delay	tWTR	MIN	max(10ns, 8nCK)								ns
Active bank-A to active bank-B	tRRD	MIN	max(10ns, 4nCK)								ns
Precharge to Precharge Delay ¹	tPPD	MIN	4								tCK
Four-bank ACTIVATE window	tFAW	MIN	40								ns

NOTE 1 Precharge to precharge timing restriction does not apply to Auto-Precharge commands.

10.3 Temperature Derating for AC timing

Table 90 — Temperature Derating AC Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Temperature Derating ¹												
DQS output access time from CK_tCK_c (derated)	tDQSCK	MAX									ps	
RAS-to-CAS delay (derated)	tRCD	MIN									ns	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	MIN									ns	
Row active time (derated)	tRAS	MIN									ns	
Row precharge time (derated)	tRP	MIN									ns	
Active bank A to active bank B (derated)	tRRD	MIN									ns	

NOTE 1 Timing derating applies for operation at 85 °C to 105 °C.

10.4 CA Rx voltage and timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 107. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

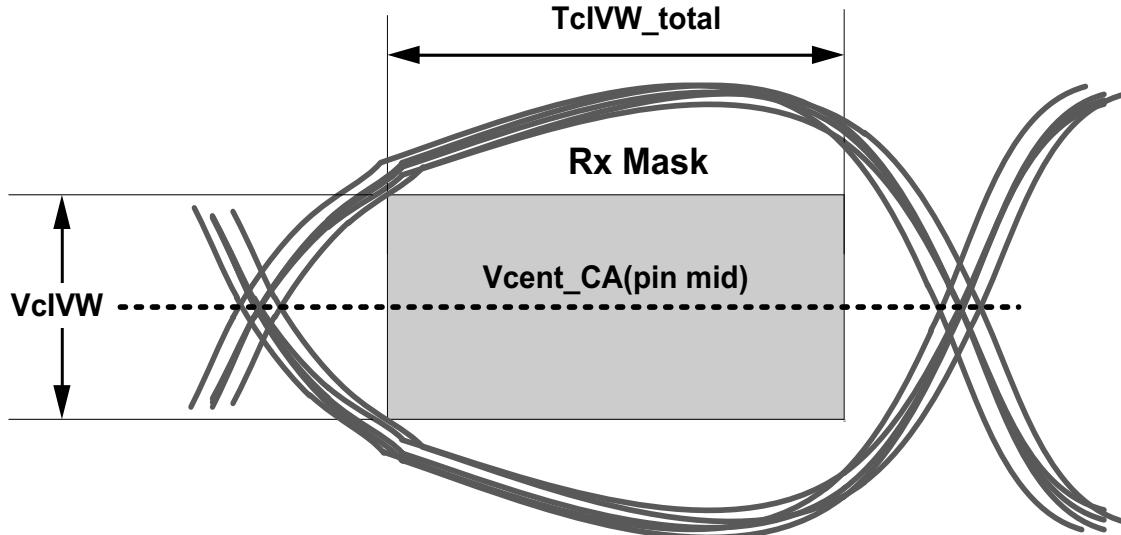


Figure 107 — CA Receiver(Rx) mask

$V_{cent_CA}(\text{pin mid})$ is defined as the midpoint between the largest V_{cent_CA} voltage level and the smallest V_{cent_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{cent} level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 108. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for R_{on} and ODT settings.

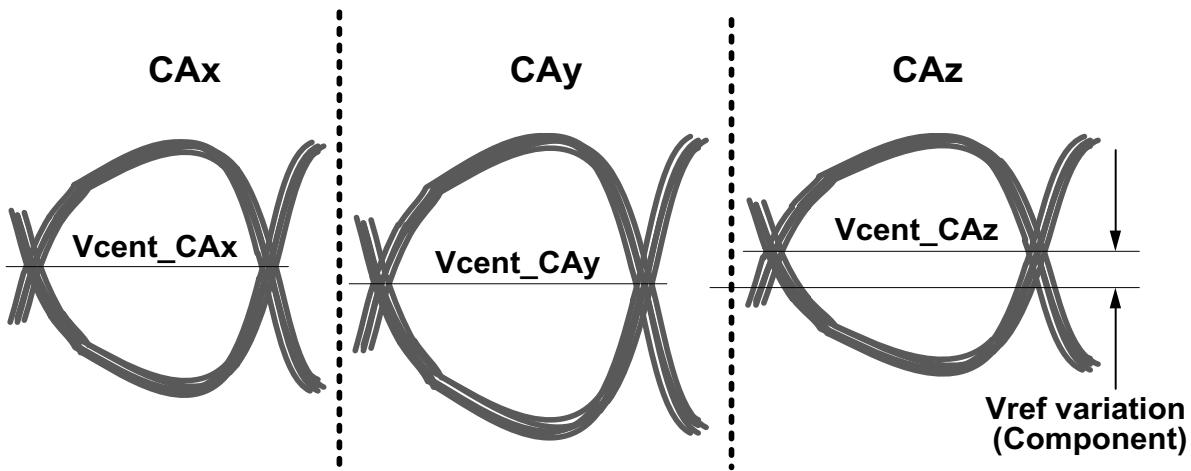


Figure 108 — Across pin V_{REF} CA voltage variation

10.4 CA Rx voltage and timing (cont'd)

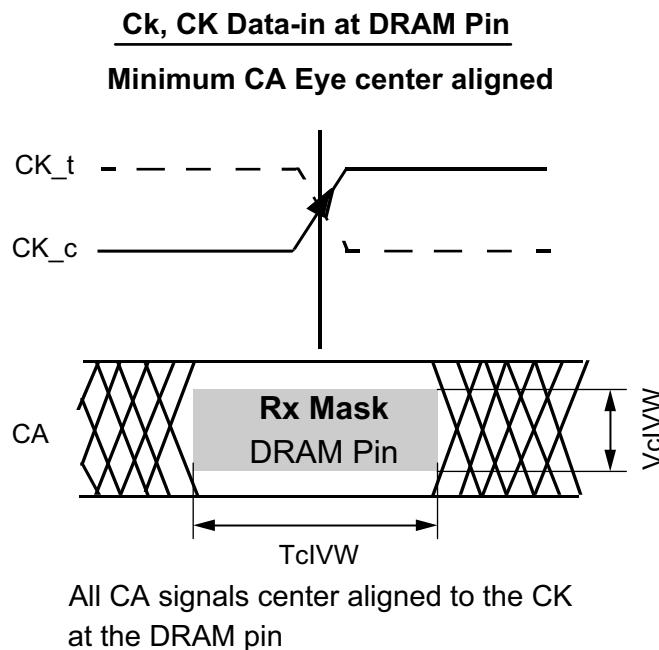


Figure 109 — CA Timings at the DRAM Pins

All of the timing terms in Figure 109 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VclVW_total voltage levels centered around Vcent_CA(pin mid).

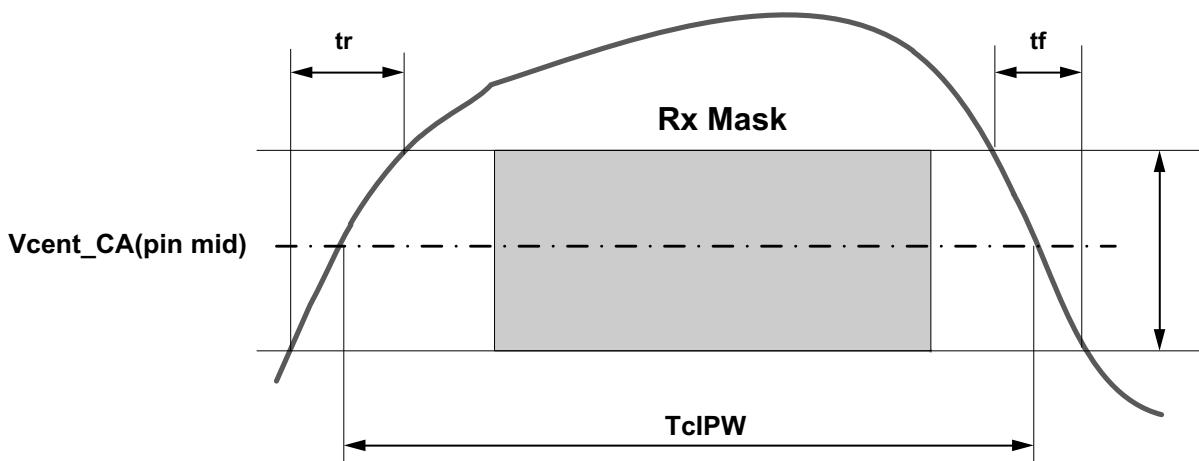


Figure 110 — CA TcIPW and SRIN_cIVW definition (for each input pulse)

10.4 CA Rx voltage and timing (cont'd)

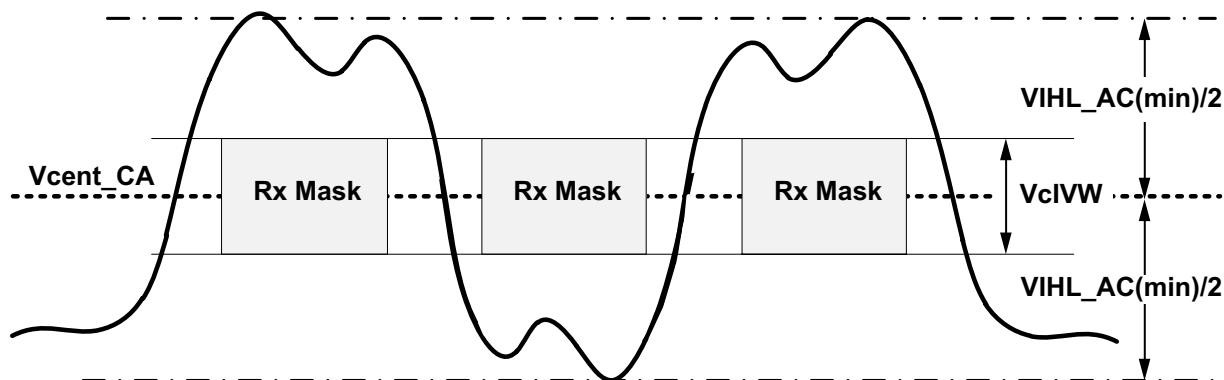


Figure 111 — CA VIHL_AC definition (for each input pulse)

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333 ^A		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VclVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TclVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TclPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VclVW	1	7	1	7	1	7	1	7	V/ns	7

* UI = tck(avg)min

^A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TclVW(ps) = 450ps at or below 1333 operating frequencies.

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

NOTE 2 Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).

NOTE 3 Rx differential CA to CK jitter total timing window at the VclVW voltage levels.

NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.

NOTE 5 CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.

NOTE 6 CA only minimum input pulse width defined at the Vcent_CA(pin mid).

NOTE 7 Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).

NOTE 8 VIHL_AC does not have to be met when no transitions are occurring.

10.5 DRAM Data Timing

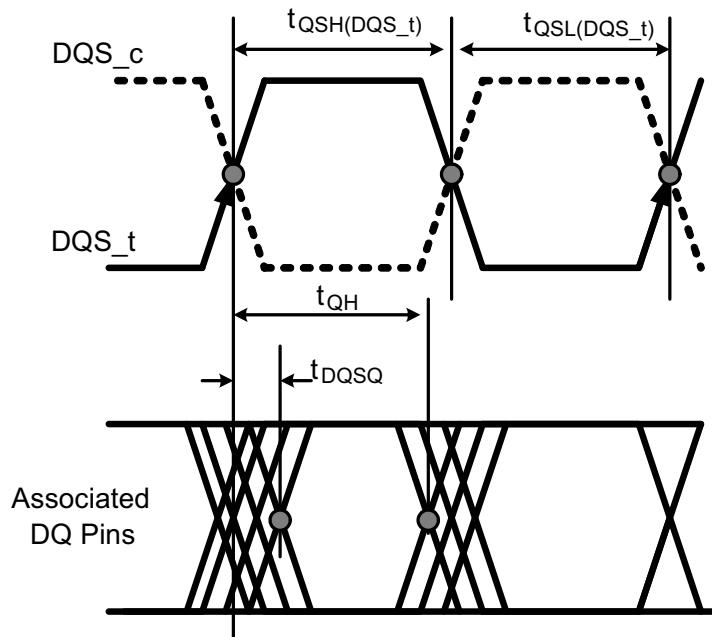


Figure 112 — Read data timing definitions t_{QH} and t_{DQSQ} across on DQ signals per DQS group

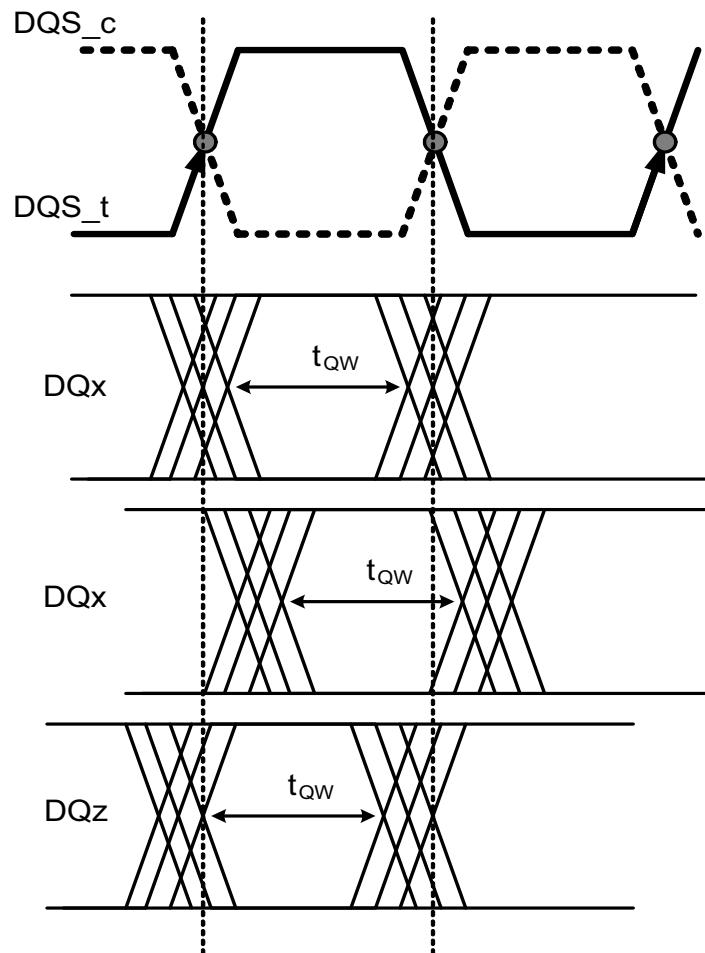


Figure 113 — Read data timing t_{QW} valid window defined per DQ signal

10.5 DRAM Data Timing (cont'd)

Table 92 — Read output timings

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled)	tDQSQ	-	0.18	-	0.18	-	0.18	-	0.18	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQL)	-	min(tQSH, tQL)	-	min(tQSH, tQL)	-	min(tQSH, tQL)	-	UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.75	-	0.73	-	0.7	-	0.7	-	UI	1,4
DQ output window time deterministic, per pin (DBIDisabled)	tQW_dj	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	TBD	-	TBD	-	TBD	-	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQL_DBI)	-	min(tQSH_DBI, tQL_DBI)	-	min(tQSH_DBI, tQL_DBI)	-	min(tQSH_DBI, tQL_DBI)	TBD	UI	1
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4

10.5 DRAM Data Timing (cont'd)

Table 92 — Read output timings (cont'd)

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe Timing											
DQS, DQS# differential output low time (DBI-Disabled)	tQSL	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	4,5
DQS, DQS# differential output high time (DBI-Disabled)	tQSH	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	4,6
DQS, DQS# differential output low time (DBI-Enabled)	tQSL_DBI	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	5,7
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	6,7
* Unit UI = tCK(avg)min/2											

NOTE 1 DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are TBD¹.

NOTE 2 The deterministic component of the total timing. Measurement method TBD¹.

NOTE 3 This parameter will be characterized and guaranteed by design.

NOTE 4 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

NOTE 5 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 6 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 7 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

1. As of publication of this document, under discussion by the formulating committee.

10.6 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown in Figure 114 is applied per pin. The "total" mask ($VdIVW_{total}$, $TdIVW_{total}$) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD¹. The mask is a receiver property and it is not the valid data-eye.

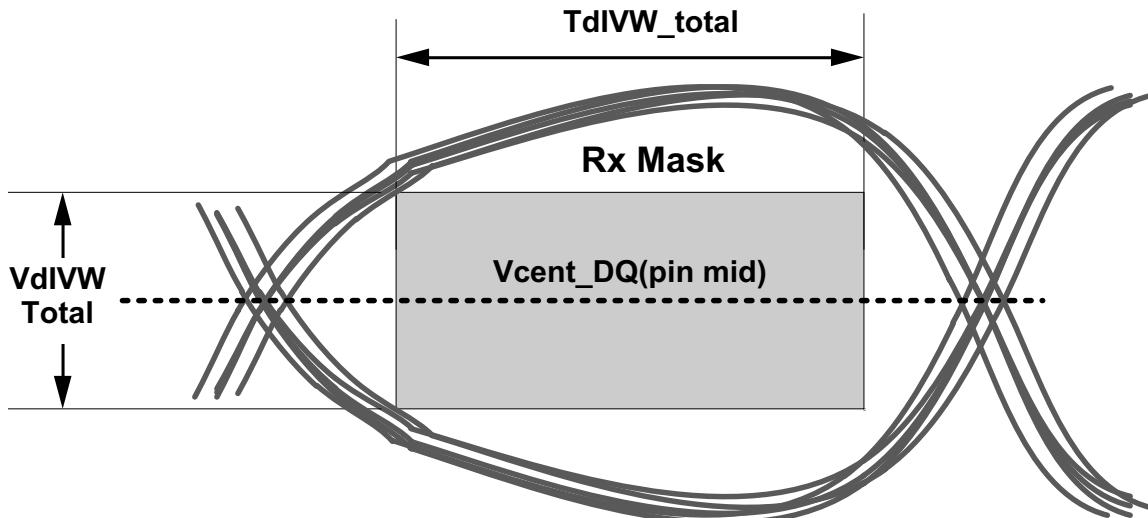


Figure 114 — DQ Receiver(Rx) mask

$V_{cent_DQ}(pin_mid)$ is defined as the midpoint between the largest V_{cent_DQ} voltage level and the smallest V_{cent_DQ} voltage level across all DQ pins for a given DRAM component. Each DQ V_{cent} is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 115. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level V_{REF} will be set by the system to account for R_{on} and ODT settings.

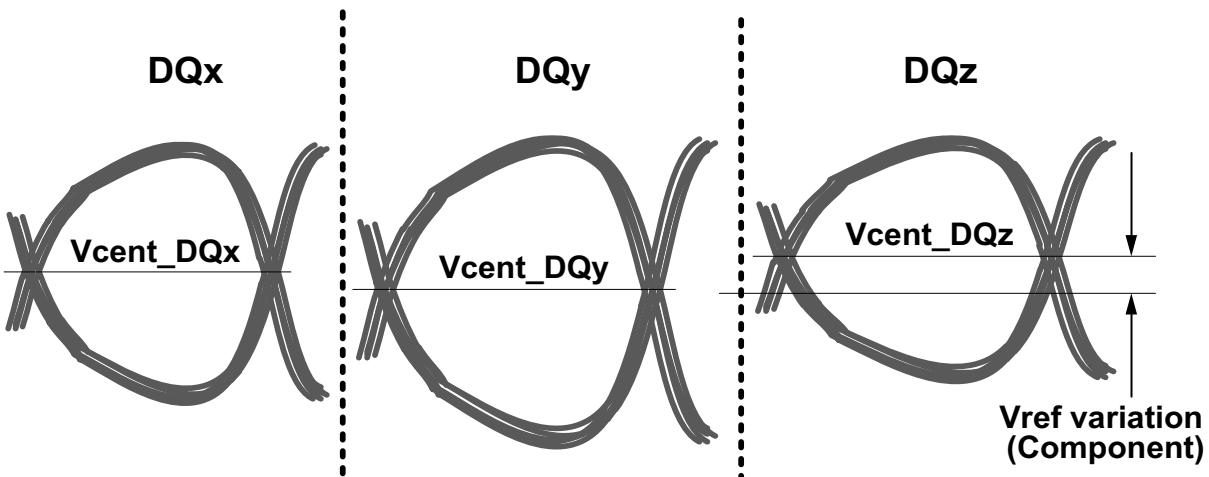
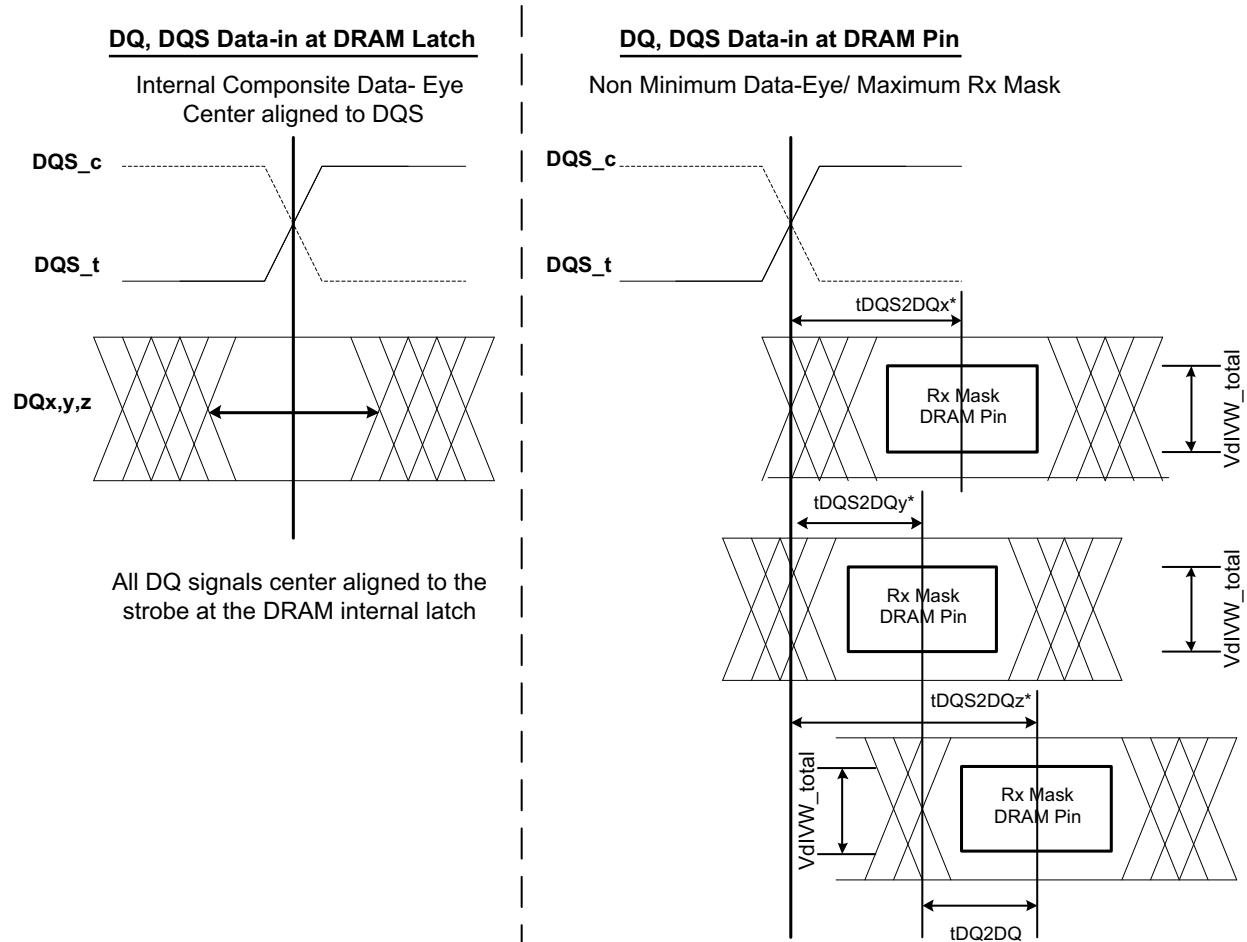


Figure 115 — Across pin V_{REF} DQ voltage variation

1. As of publication of this document, under discussion by the formulating committee.

10.6 DQ Rx Voltage and Timing (cont'd)



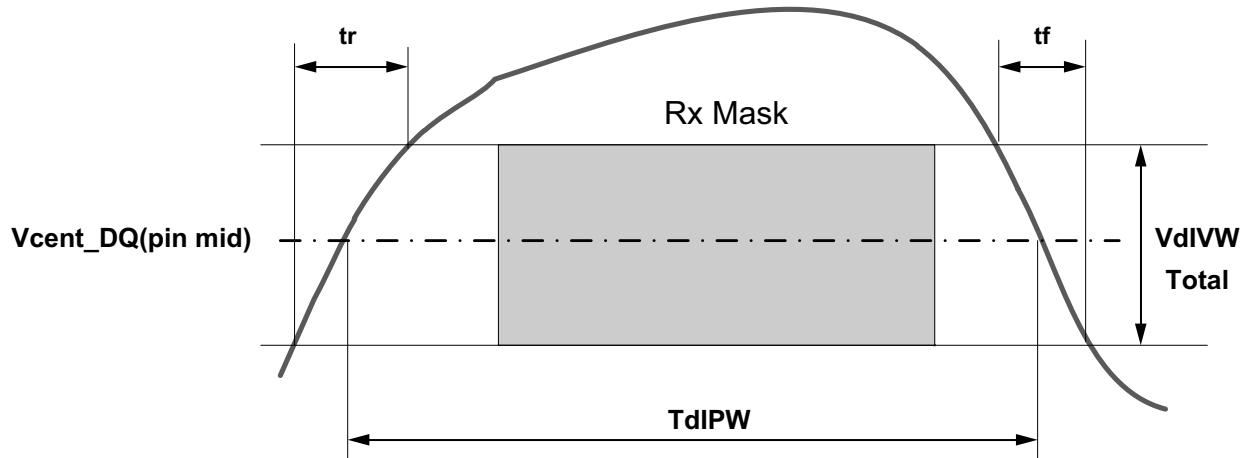
NOTE:

1. tDQS2DQ is measured at the center(midpoint) of the TdIVW window.
2. DQz represents the max tDQS2DQ in this example
3. DQy represents the min tDQS2DQ in this example

Figure 116 — DQ to DQS t_{DQS2DQ} and t_{DQDQ} Timings at the DRAM pins referenced from the internal latch

All of the timing terms in DQ to DQS t are measured from the DQS_t/DQS_c to the center(midpoint) of the TdIVW window taken at the VdIVW_total voltage levels centered around Vcent_DQ(pin_mid). In Figure 116 the timings at the pins are referenced with respect to all DQ signals center aligned to the DRAM internal latch. The data to data offset is defined as the difference between the min and max t_{DQS2DQ} for a given component.

10.6 DQ Rx Voltage and Timing (cont'd)



Note

1. $SRIN_{dIVW} = V_{dIVW\ Total}/(tr \text{ or } tf)$, signal must be monotonic within tr and tf range.

Figure 117 — DQ TdIPW and SRIN_dIVW definition (for each input pulse)

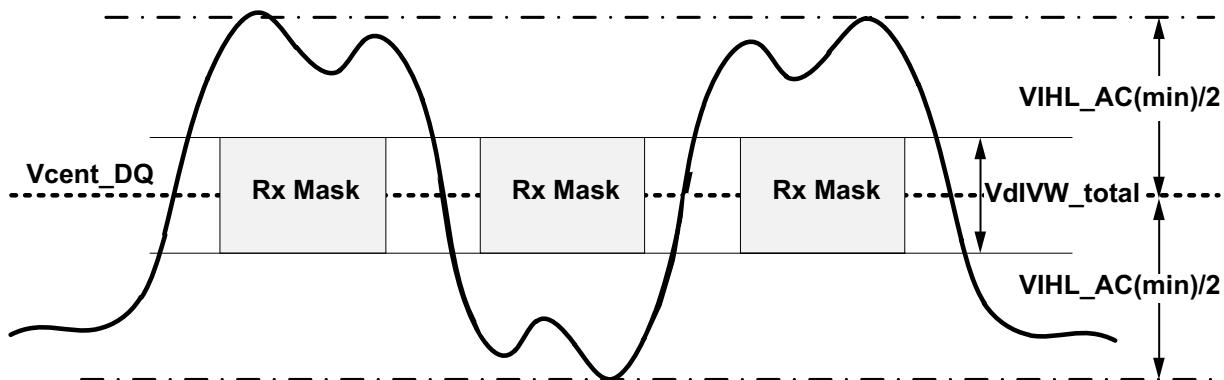


Figure 118 — DQ VIHL_AC definition (for each input pulse)

10.6 DQ Rx Voltage and Timing (cont'd)

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867 ^A		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW_DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

^A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TdIVW(ps) = 450ps at or below 1333 operating frequencies.

10.6 DQ Rx Voltage and Timing (cont'd)

Notes to Table 94.

NOTE 1 Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.

NOTE 2 The design specification is a BER (TBD¹). The BER will be characterized and extrapolated if necessary using a dual dirac method.

NOTE 3 Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).

NOTE 4 Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.

NOTE 5 Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} DQ range irrespective of the input signal common mode.

NOTE 6 Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method TBD¹.

NOTE 7 DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.

NOTE 8 DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).

NOTE 9 DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.

NOTE 10 DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.

NOTE 11 TDQS2DQ max delay variation as a function of temperature.

NOTE 12 TDQS2DQ max delay variation as a function of the DC voltage variation for V_{DD}Q and V_{DD}2. It includes the V_{DD}Q and V_{DD}2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement V_{DD}Q=V_{DD}2 is assumed.

NOTE 13 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).

NOTE 14 Rx mask defined for a one pin toggling with other DQ signals in a steady state.

NOTE 15 VIHL_AC does not have to be met when no transitions are occurring.

1. As of publication of this document, under discussion by the formulating committee.



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