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MARWADI UNIVERSITY

Faculty of Technology

Information and Communication Technology

B.Tech SEM: III WINTER:2018

Subject: - Computer Organization and Architecture (01CT0301)

Total Marks:-100

Date: - 20/10/2018

Time: - 03:00 hours

Instructions:

- 1. All Questions are Compulsory.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

Question:	1.	Do As	Directed

(a)	Multiple Choice Questions:	[10]

- 1. (24)₁₆ = (_____)₂
 - a. 11001111
 - b. 10101010
 - c. 00101000
 - d. 00100100

2.
$$(010110)_2 = (\underline{\hspace{1cm}})_8$$

- a. 32
- b. 47
- c. 26
- d. 27

_	TD1 .	CITE	D	1
.j.	The size	of Temporary	Register is	bits.

- a. 12
- b. 16
- c. 20
- d. 8

- a. Sets
- b. Clears
- c. Flips
- d. Resets

5. Which of the following is a branch instruction?

- a. ISZ
- b. CLE
- c. INC
- d. BSA

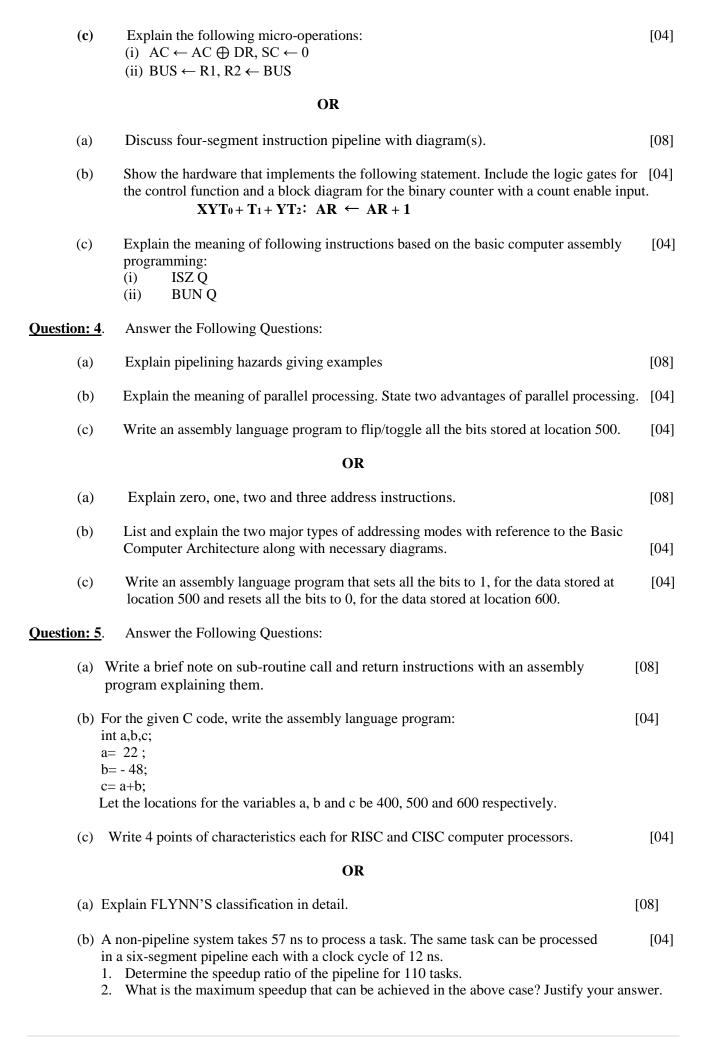
6. The size of Data Register is _____ bits.

- a. 12
- b. 16
- c. 20
- d. 8

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	7.	The size of Instruction Register is bits.	
		a. 12	
		b. 16	
		c. 20	
		d. 8	
		The carry if generated by addition of two numbers is stored in bit.	
		a. E b. F	
		c. G	
		d. A	
		u. A	
	9.	The size of Address Register is bits.	
		a. 12	
		b. 16	
		c. 20	
		d. 8	
		The size of Accumulator is bits.	
		a. 12 b. 16	
		b. 16 c. 20	
		d. 8	
		d. O	
(a)	Ans	wer the following questions in one sentence:	[10]
	1. What is meant by Computer Architecture?		
	2. Define Accumulator.		
	3.	Define Micro-Instruction	
		What is the use of E bit with reference to basic computer architecture?	
		What is meant by an Accumulator?	
		What is meant by compiler?	
		Write the functionality of Program Register for Basic Computer Architecture.	
		Define Assembler.	
		Write the functionality of Instruction Register for Basic Computer Architecture. Write the functionality of Input Register for Basic Computer Architecture.	
Question: 2. A	nswe	r the Following Questions:	
(a)	E	lain hardware Implementation of common bus system along with a neat sketch of	
(a)	•	bus architecture.	[08]
	ше	bus architecture.	լսօյ
(b)	Exp	lain different types of micro-operations in basic computer architecture. OR	[08]
(b)		at is meant by Stack? Explain push and pop operations on register stack giving able examples.	[08]
Question: 3.	Ans	wer the Following Questions:	
(a)	Wri	te a detailed note on instruction cycle with neat diagrams and flowchart.	[08]
(b)		lain whether the following microoperations can be executed or not? If no, Write the rect sequence of microoperations: IR ← M[PC] AC ← AC+TR	[04]

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(c) Give two points of advantages and disadvantages of pipelining system over conventional system. Give an example that shows "pipelining system is more beneficial than the conventional system."

Question: 6. Answer the Following Questions:

- (a) What is meant by the masking procedure over the data? Explain its importance. Write a program to unpack two characters from location WRD and store them in bits 0 through 7 of locations CH 1 and CH2. Bits 9 through 15 should contain zeros.
- (b) Write a program loop, using a pointer and a counter, that flips the values of the contents Stored at locations 500 through 5FF.
- (c) Write an assembly code to add 50 numbers and store it back to any memory location i.e. [04] Sum = $n_1 + n_2 + n_3 + \dots + n_{49} + n_{50}$.

OR

- (a) Write a program to evaluate the following arithmetic statement $X = \left[A * (B + C) D\right] / (E + F G)$
 - (i) using a general register computer with three-address instructions,
 - (ii) using an accumulator type computer with one-address instructions,
 - (iii) using a stack organized computer with zero
- (b) Write an assembly code to perform the XORing between two numbers and store into another variable i.e. $Z = X \oplus Y$.
- (c) Write a subroutine that accepts a number from the user and determine whether it is a positive, negative or zero number. [04]

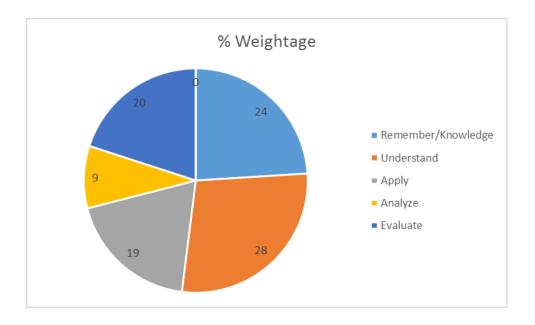
---Best of Luck---

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Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age		
		% of	Que. No.	
		weight -age		
1	Remember/Knowledge	24	Q.1 (a,b), Q.2 (a,b OR b)	
2	Understand	28	Q.3(a OR a), Q.4(a OR a), Q.5 (a OR a)	
3	Apply	19	Q.3 (b,c OR b,c), Q.4 (b OR b), Q.5 (c OR	
			b)	
4	Analyze	9	Q.4 (c OR c), Q.5 (c OR b)	
5	Evaluate	20	Q.6 (a,b,c OR a,b,c)	
6	Higher order Thinking			

GRAPH:



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