A Review of Borrow Select Subtractor for Low Power and Area Efficiency

1) Aryan Langhanoja
2) Jay Mangukiya
Department of Information and Communication Technology
Marwadi University
Rajkot , India

Abstract—

This paper presents two modified architectures of borrow select subtractor that consume lower power and have increased area efficiency. The modifications carried out in the logical flow of subtraction process by using blocks with lower number of logic gates lead to a smaller number of gates, thus resulting in less device count, lower area and lower power dissipation. The proposed architectures are validated using Cadence Virtuoso® simulations on UMC 90nm technology library and compared with existing architectures to demonstrate their comparative advantages.

Keywords— *Borrow Select Subtractor , Low power Subtractor , Area Efficient Subtractor , BSLS , Adder-Subtractor , Power consumption , Gate count , Area efficiency*

Introduction—

Adders, subtractors, and multipliers are the essential building blocks of processors. This paper focuses on the design aspect, architecture, and comparative operational advantages of modified borrow select subtractor using BLO and modified borrow select subtractor using RBHS operating at the same performance parameters, even while incurring lower power consumption even while maintaining the speed performance without incurring any adverse impact on the delay of the system. The primary focus is on reducing area and power consumption, which is achieved by using logic blocks with fewer gates occupying less area even while aiming for the same logic functionality.

Body—

The paper presents two modified architectures of the BSLS: BSLS-BLO and BSLS-RBHS. BSLS-BLO replaces the second n-bit RBS and BEC-1 with n+1-bit Binary-Less-One (BLO) logic. This modification reduces the number of gates and improves area efficiency. BSLS-RBHS replaces the second n-bit RBS and BEC-1 with n-bit ripple borrow half subtractor (RBHS). This modification also reduces the number of gates and improves power consumption.

[1] The paper provides gate count calculations for each architecture and compares them with the conventional BSLS. BSLS-BLO requires fewer gates compared to BSLS, resulting in improved area efficiency. BSLS-RBHS also requires fewer gates, further reducing power consumption. The gate count analysis demonstrates the advantages of the modified architectures in terms of gate reduction.

[2] To delve into further detail, let's explore the specifics of these two architectures:

[3] BSLS-BLO: BSLS-BLO is designed to optimize the subtraction process in terms of power consumption and area efficiency. It achieves this by replacing the second n-bit Ripple Borrow Subtractor (RBS) and Borrow Extension Circuit 1 (BEC-1) with n+1-bit Binary-Less-One (BLO) logic. This architectural modification is strategically aimed at reducing the number of gates and thereby improving area efficiency. The underlying principle here is to simplify the logic involved in subtraction to make it more energy-efficient and streamlined.

[4] The reduction in gate count achieved by BSLS-BLO is a key feature. With fewer gates, it consumes less power during operation. Additionally, the improvement in area

[5] efficiency is also noteworthy, as it optimizes the silicon real estate within the processor.

[6] BSLS-RBHS: In the case of BSLS-RBHS, the focus is on reducing power consumption while maintaining operational efficiency. This architecture replaces the second n-bit RBS and BEC-1 with n-bit ripple borrow half subtractor (RBHS). The result is a significant reduction in the number of gates used in the subtraction process. This reduction directly contributes to a decrease in power consumption.

[7] While BSLS-RBHS excels in terms of power efficiency, it is essential to acknowledge that there is a slight trade-off in terms of delay. The introduction of the RBHS component introduces a marginally higher delay in the subtraction process. However, this increased delay is often outweighed by the substantial benefits in power savings.

[8] Gate Count Analysis: The gate count calculations performed for both BSLS-BLO and BSLS-RBHS highlight the tangible advantages of these modified architectures over the conventional BSLS. In essence, they result in gate reduction, which is pivotal for improving both area efficiency and power consumption. The significance of gate count reduction cannot be overstated, as it directly translates to improved energy efficiency and reduced hardware complexity.

[9] Performance Analysis: The paper goes on to provide a comprehensive performance analysis, comparing these modified architectures with existing alternatives, including the conventional BSLS. This analysis encompasses critical parameters such as power consumption, delay, and the power delay product (PDP).

[10] BSLS-BLO demonstrates lower power consumption compared to the conventional BSLS while maintaining the same delay. This signifies a clear enhancement in power efficiency. In other words, it accomplishes the same computational tasks with less energy.

[11] BSLS-RBHS exhibits even lower power consumption than other architectures, although there is a slight increase in delay. The trade-off between power and delay is a common consideration in processor design, and BSLS-RBHS leans toward optimizing power efficiency.

Conclusion—

In conclusion, this paper introduces two innovative modified architectures of the borrow select subtractor (BSLS) with the primary goal of reducing power consumption and increasing area efficiency. These architectural modifications involve the strategic use of logic blocks with fewer gates, resulting in tangible benefits for modern processors.

The gate count analysis underscores the advantages of these architectures in terms of reducing gate count, thereby improving area efficiency and reducing power consumption. BSLS-BLO and BSLS-RBHS have distinct advantages, with the former excelling in area efficiency and the latter achieving remarkable power savings. The performance analysis demonstrates their prowess in power efficiency, delay, and the overall power delay product (PDP).

These modified architectures hold the potential to significantly enhance the performance of processors, making them more energy-efficient and optimized for modern computing demands. As technology continues to advance, further research can explore additional optimizations and delve into their impact on other crucial performance metrics, ensuring that processor design continues to evolve in step with the ever-changing landscape of computing needs.