Enroll. No._____

MARWADI UNIVERSITY
MU-FOT
CE-FOT1 (MU), IT-FOT1 (MU)
Semester 4 - Summer

Subject : COMPUTER ORGANIZATION AND ARCHITECTURE (01CE0402)
Date : 29-Apr-2022 **Time : 3 Hours** **Total Marks : 100**

Instructions :

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Que.1 (A) Answer the following objectives **[10]**

(1) Which of the following is an advantage of pipelining?

A. Instruction throughput increases.
B. Faster ALU can be designed when pipelining is used.
C. Pipelining increases the overall performance of the CPU.
D. All of the above

(2) A stack organized Computer uses instruction of _____

a) Zero Addressing
b) Indirect Addressing
c) Two Addressing
d) Index Addressing

(3) Equivalent Decimal value of packed BCD data 0010 1001 1001 0111?

a) 2997
b) 2995
c) 2883
d) 2080

(4) Pipeline register used to provide

a) Parellel Processing
b) Sequencial Processing
c) Partial Processing
d) None of this

(5) When arithmetic, logic and control unit of a computer are combined into a single unit, it is known as _____

a) CPU
b) Memory Unit
c) I/O Unit
d) Operating Unit

(6) Convert the hexadecimal number (1E2)16 to decimal.

a) 480 b) 483 c) 482 d) 484

(7) Relative mode of Addressing is most relevant to writing _____

a) Co-Routines
b) Position Indepemdent Code
c) Shareable Code
d) Interrupt Handerls

(8) Which one of the following is not a type of I/O Chnnel?
a) Selector
b) Multiplexer
c) Block Multiplexer
d) None of the above

(9) The spatial aspect of the locality of reference means _____
a) That the recently executed instruction is executed again next
b) That the recently executed won't be executed again
c) That the instruction executed will be executed at a later time
d) That the instruction in close proximity of the instruction executed will be executed in future

(10) Data Input command is just the opposite of a _____
a) Data Output
b) Control Command
c) Test Command
d) Data Channel

Que.1 (B) Answer the following questions. **[10]**

(1) Give full form of CAR.

(2) Define the term asynchronous data transfer.

(3) What do you mean by Magnetic disk?

(4) Define Microinstruction.

(5) Define Instruction Stream

(6) Convert the following binary number to decimal.
a. 101110
b. 1110101

(7) Explain processor status word.

(8) How overflow is detected in addtion operation.

(9) What is Program Counter

(10) Define Page Fault.

Que.2

(A) Differentiate machine instructions and microinstrucions. Explain micronstrunction Format With detail. [8]

(B) Write a short note on Content Associative Memory(CAM). [8]

OR

(B) Write a note on Vector processing. [8]

Que.3

(A) Draw and explain the organization of micro programmed control unit. [8]

(B) What is a Digital Computer System? Explain the role of binary number system in it. [4]

(C) Explain characteristics of RISC. [4]

OR

(A) Explain CPU Registers in details. [8]

(B) Which are the Logic Microopearions ? Create logic circuit with function table. [4]

(C) Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating numerical result [4]

1. (3*4) + (5*6)

Que.4

(A) Explain Common Bus System with details. [8]

(B) Define cache memory. Enlist various mapping technique to be used by cache memory. Discuss write through and write back cache write method. [8]

OR

(A) Explain Flynn's taxonomy for classifying parallel processors. Explain each class. [8]

(B) Explain with diagram circuit for BCD adder. [8]

Que.5

(A) Explain 4-bit adder-subtractor with diagram. [6]

(B) Explain design of control unit of basic computer with timing signal. [6]

(C) The 8 bit register AR, BR, CR and DR initially have the following values: [4]
AR = 11110010
BR = 11111111
CR = 10111001
DR = 11101010
Determine the 8 bit values in each register after the execution of the following sequence of microoperations
AR ← AR + BR
CR ← CR ^ DR, BR ← BR + 1
AR ← AR - CR

OR

(A) Describe flowchart of memory reference instructions. [6]

(B) With suitable example show application of Selective Set, Selective Complement and Clear [6]

(C) Differentiate Interrupt initiated I/O and DMA I/O. [4]

Que.6

(A) Enlist possible modes of data transfer to and from peripherals, and explain any one mode in detail. [8]

(B) Explain BSA instruction in detail. [4]

(C) Design a digital circuit for 4-bit binary adder. [4]

OR

(A) Write a note on Array processors. [8]

(B) Explain characteristics of CISC. [4]

(C) Explain daisy chaining priority interrupt. [4]

---Best of Luck---

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Difficulty Level	Weightage Recommended	Actual	No of Question	Total Marks	Question List
High	20	1.74	3	3	1(A)
Low	20	1.74	3	3	1(A), 1(B)
Medium	60	96.51	39	166	1(A), 1(B), 2(A), 2(B), 3(A), 3(B), 3(C), 4(A), 4(B), 5(A), 5(B), 5(C), 6(A), 6(B), 6(C)

Module Name	Weightage Recommended	Actual	No of Question	Total Marks	Question List
Computer Data Representation & Register Transfer and Micro-operations:	15	17.44	8	30	1(A), 1(B), 3(B), 5(A), 5(B), 5(C), 6(C)
Introduction to Computer Organization and Design:	20	19.19	6	33	1(B), 3(A), 4(A), 5(A), 5(B), 6(B)
undamental concepts of Micro programmed Control:	10	11.05	5	19	1(A), 1(B), 2(A), 3(A)
Concepts of Central Processing Unit:	15	9.30	7	16	1(A), 1(B), 3(C), 6(B)
Introduction to Pipeline:	10	15.12	5	26	1(A), 1(B), 2(B), 4(A), 6(A)
Basic of Computer Arithmetic:	10	5.81	3	10	1(A), 1(B), 4(B)
Input-Output Organization:	10	11.05	6	19	1(A), 1(B), 5(C), 6(A), 6(C)
Memory Classification and Organization:	10	11.05	5	19	1(A), 1(B), 2(B), 4(B)

Blooms Taxonomy	Weightage Recommended	Actual	No of Question	Total Marks	Question List
Remember / Knowledge	20	13.37	9	23	1(A), 1(B), 4(A)
Understand	30	63.95	24	110	1(A), 1(B), 2(A), 2(B), 3(A), 3(B), 3(C), 4(B), 5(A), 5(C), 6(A), 6(B), 6(C)
Apply	25	11.63	6	20	1(A), 3(B), 5(B), 6(B), 6(C)
Analyze	15	11.05	6	19	1(A), 5(A), 5(B), 5(C)
Evaluate	10	0.00	0	0	
Higher order Thinking	0	0.00	0	0