TCMP and CHIPPER Router design for Power Efficient Network on Chips

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Abstract— **Network on Chip (NoC) is an emerging design platform for on chip connections which overcomes issues faced by conventional bus build communication. The main aim in design of any NoC is to reduce average latency and deflection rate without reducing the operating speed. To overcome the surge in design area as well as Static and Dynamic power consumption issues in case on normal VC (Virtual Channel) based router, deflection routing concept has been suggested. The routing process used in case of BLESS (Buffer Less Router) depends upon deflection of packets to an unintended port. To curtail excess power consumption and design area, researchers have come up with buffer less and littlest buffer router. In this paper Tiled Chip Multiple Processor (TCMP) and CHIPPER router parameter details are discussed. Permutation deflection logic is used in this paper. Results shows that as compared to normal VC Buffer router, CHIPPER Router reduces Normalized Router area by 36.2% compared to BLESS Router, Normalized Critical Path is reduced by 29.1% while is almost same as compared to a normal VC Buffer Router**

Keywords- Network on Chip, Tiled Chip Multiple Processor, CHIPPER, latency, deflection

I. INTRODUCTION

Now a day's Network-on-chip has become essential modules in router design with far better results as compared with SoCs (System on chips). NoC is a better option to the bus based and ad hoc based seen in previous designs [2]. It provides low scalability, less latency and power among PEs (processing elements) connected on chip. The advanced bypass path technique is used in case of low traffic which reduces latency in the arrival of packets [3]. An NoC Router does the following functions VA: Virtual Channel Allocation, RC: Route Computation, BW: Buffer Write, ST: Switch Traversal and SA: Switch Allocation [9]. The order in which flits travel through the Virtual Channel is shown in figure 1 below. Area occupancy in the on chip design should also be reduces to improve the performance of the chip [13]. To discard cost of buffers an EB (Elastic Buffer) control technique is used in router design [4].The use of Virtual Channel VCs [7] lowers area, latency as well as static and dynamic power of the chip. The parameters involved in efficient router design involve Buffers, Arbiter, Virtual Channel Controller, Routing path Controller and Allocator [13]. Using power gating method [9] the static power can be reduced. TCMP creates thermal buffers which reduces temperature of adjacent tiles [18].

Figure 1. NoC Router Pipeline

II. NOC ROUTING

The typical bus concept implementation requires large Multiplexers and to solve problems of cache coherence. Hence the bus communications are not scalable for today's MPSoC structures [6].

Condition1: Suppose a cache misses request packet P1 with a destination address 13 injected into a router 7 in a 4x4 Mesh NoC that uses XY Routing. Following statements are true as derived from Figure 2.

12	13	14	15
8	9	10	11
4	5	6	7
0	1	2	3

Figure 2. 4x4 Mesh NoC packet flow structure

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a. P1 moves through router NoC 9

b. Reply packet of P1 moves through router 14.

c. Neither the request packet nor the reply packet passes through router 10.

On Chip router design aims to lower count of buffers [5] to increase SoC usable area. Control area overheads can be hided to reduce latency significantly. Impact related to less buffering also shrinks latency in router design by use of single cycle design.

Condition 2: A 25 core machine in which cores are organized as a regular Square Mesh Topology. A packet P1 is generated from core number 18 destined to core 6.The system follows minimal north last routing. The unique minimal paths from 18 to 6 are listed below.

18-17-16-11-6; 18-17-12-11-6; 18-17-12-7-6; 18-13-12-11-6; 18-13-12-7-6; 18-13-8-7-6

In all total we have 6 paths from 18 to 6 with minimal north last routing.

20	21	22	23	24
15	16	17	18	19
10	11	12	13	14
5	6	7	8	9
0	1	2	3	4

Figure 3. 5x5 Square Mesh Topology 25 core machine

III. NOC ROUTER SWITCH ARBITRATION

The age based switch allocation in XY Routing is given as <packet number, age, source, destination>

<P1,2,15,2> , <P2,1,10,0> , <P3,3,11,12> , <P4,2,9,3>

The condition to be satisfied is if R is Router 10 in a 4x4 Router NoC. Switch Arbitration is done based on age based priority. If there is only packet competing for a desired output it is granted (in case of south and east). But if there are more packets competing for the same output port we can choose only one out of them which is having higher age [18]. As P3 is having higher age as compared P1, P3 is granted West port while P2 is buffered.

56	57	58	59	60	61	62	63
48	49	50	51	52	53	54	55
40	41	42	43	44	45	46	47
32	33	34	35	36	37	38	39
24	25	26	27	28	29	30	31
16	17	18	19	20	21	22	23
8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7

Figure 4. 8x8 Mesh NoC Topology with XY Routing

Figure 4 shows 8x8 Mesh NoC Topology with XY Routing

TABLE1. XY Routing Switch Arbitration Summary

Packet No	Age	Source	Dest	IP	OP-Req	OP-Status
P1	2	15	2	N	S	S
P2	1	10	0	L	W	*(Buffer)
P3	3	11	12	E	W	W
P4	2	9	3	W	E	E

N: North, L: Local, E:East. W: West

IV. PATTERN AND LATENCY

Injection: A process by which a Local tile creates a new packet and injects into a local port is called as Injection

Ejection: A process by which a packet is removed from router to a tile is called as Ejection

We have considered 8x8 Mesh NoC, XY Routing, 3 cycle router and 1 cycle link. Packets P1, P2 and P3 are given Source from 6, 24 and 50 respectively. Injection and Ejection are considered for 2 cycles each. CHIPPER Router is working with golden packets [19]

Latency of packet = [hops x 4]+ 4 (1)

TABLE2. Transpose Pattern

Pkt. No.	Source	D_trans	Latency	D_ bitrev	Latency
P1	6	48	12x4+4 = 52	57	12x4+4 = 52
P2	24	3	6x4+4 = 28	39	8x4+4 = 36
P3	50	22	8x4+4 = 36	13	8x4+4 = 36

V. PERFORMANCE ANALYSIS OF CHIPPER ROUTER

As compared to Normal VC router design advanced version CHIPPER shows reduced deflection rate and latency.

a. Normalized Router Area

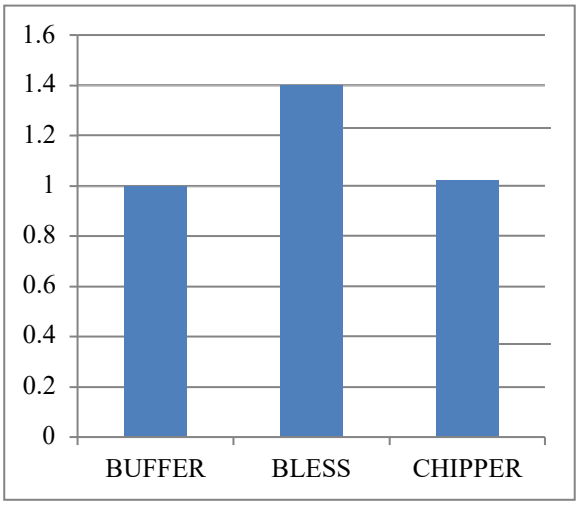

Figure 5. Normalized Router Area Analysis

As compared to normal VC Buffer router, CHIPPER Router reduces Normalized Router area by 36.2% .Rather than going for sequential port allocation we are switching towards parallel port allocation called as Permutation deflection logic [19]

b. Normalized Critical Path

As compared to BLESS Router, CHIPPER Router reduces Normalized Critical Path by 29.1% while is almost same as compared to a normal Buffer Router

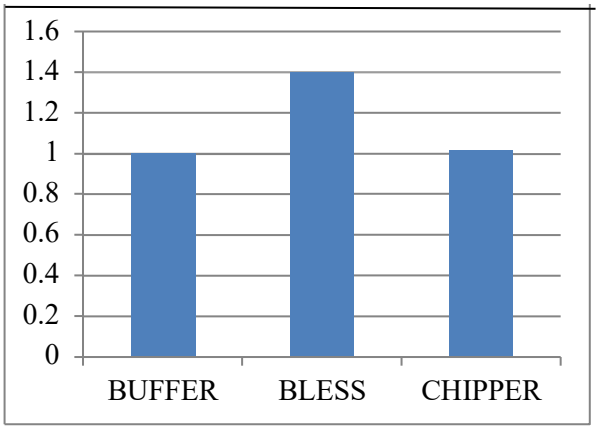

Figure 6. Normalized Critical Path Analysis

VI. CONCLUSION

A low cost technique to improve the performance of the NoC router is achieved by reduction of cycle time. The latency of the router is reduced significantly without hampering the efficiency of router. As compared with conventional buffer-less router average flit latency of CHIPPER is reduced by use of PDN (Permutation Deflection Network) which uses parallel output port allocation. Normalized Critical Path as well as Normalized Router area of CHIPPER router is reduced by 29.1% and 36.2% respectively.

VII. FUTURE SCOPE

The techniques discussed above can be applied for reducing normalized router area as well as Normalized critical path

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