A Review of Borrow Select Subtractor for Low Power and Area Efficiency

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Abstract—

The paper titled "Energy-Efficient Spin-Orbit Torque MRAM Operations for Neural Network Processor" explores the potential of using Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) as a replacement for Static Random Access Memory (SRAM) in developing large buffers for Artificial Intelligence (AI) processors. The paper focuses on developing the working memory of neural network processors with SOT-MRAM, including multiple-port memory, transpose memory, and data-streaming based buffer arrays.

Keywords— *Spin-Orbit Torque Magnetic Random Access Memory, Static Random Access Memory, Artificial Intelligence, Neural Network Processor, Energy Efficiency, Multiple-Port Memory, Transpose Memory, Data-Streaming Based Buffer Arrays.*

Introduction—

The paper proposes the use of SOT-MRAM as a replacement for SRAM in developing large buffers for AI processors. The research focuses on developing the working memory of neural network processors with SOT-MRAM, including multiple-port memory, transpose memory, and data-streaming based buffer arrays. The proposed SOT-MRAM outperforms the SRAM design in terms of area and power consumption.

Body—

The paper begins by highlighting the importance of energy efficiency in wearable devices and IoTs, where low-power AI processors are required to identify emergency/critical signals. The paper then discusses the use of deep neural networks (DNNs) to improve the accuracy of detection and classification. However, DNN applications are both compute- and memory-intensive algorithms, which are difficult to deploy on energy-efficient neural network processors.

The paper proposes the use of SOT-MRAM as a replacement for SRAM in developing large buffers for AI processors. The paper then discusses the development of the working memory of neural network processors with SOT-MRAM. The authors propose the use of multiple-port memory, transpose memory, and data-streaming based buffer arrays.

The transpose memory array can be used to build the online training neural network processor. The authors also develop an odd-even memory array structure to support the multi-port SOT-MRAM with parallel write and read operations. Based on simulation and evaluation, the proposed transpose- and multi-port based SOT-MRAM outperforms the SRAM design in terms of area and power consumption.

The paper concludes by discussing the potential of SOT-MRAM in developing energy-efficient neural network processors. The authors highlight the benefits of using SOT-MRAM in developing large buffers for AI processors, including improved area and power consumption. The authors also discuss the potential of SOT-MRAM in designing advanced computing architecture.

Conclusion—

The paper titled "Energy-Efficient Spin-Orbit Torque MRAM Operations for Neural Network Processor" proposes the use of SOT-MRAM as a replacement for SRAM in developing large buffers for AI processors. The paper focuses on developing the working memory of neural network processors with SOT-MRAM, including multiple-port memory, transpose memory, and data-streaming based buffer arrays. The proposed SOT-MRAM outperforms the SRAM design in terms of area and power consumption. The authors have made a significant contribution to the field of AI by proposing the use of SOT-MRAM as a solution to the memory-intensive algorithms used in DNN applications.