

MARWADI UNIVERSITY

Faculty of Technology

Computer Engineering / Information Technology Engineering

B.Tech SEM: 4th **SUMMER:2018**

Subject: - (Computer Organization) (01CE0402) Date: - 21/04/2018

Total Marks:-100 Time: - 03:00 hours

Instructions:

- 1. All Questions are Compulsory.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

Qυ

ıestic	on: 1.						
		rout	otion for following que tines, the return addres Stack	sses		d.	[10] Register
	The DMA transfers and Device interface		performed by a control DMA controller		cuit called as Data controller	d.	Over looker
	The DMA controller Processor BUS		connected to the System BUS	c.	External BUS	d.	None
4) a.	Which are the operar arithmetic		that a computer performance Logic		on data that put in reg Shift		r All
a.	Arithmetic	b.	Transfer	c.	Logical	d.	All
6) a.	Which memory devi RAM		s generally made of se Hard-disk		conductors Floppy disk	d.	CD Disk
	To reduce the memo Heap		ccess time, system ger RAM		lly make use of Cache	d.	SDRAM
8) a.	Size of PC is 12 bits	b.	16 bits	c.	8 bits	d.	20 bits
9) a.	In which addressing Implied		le operand is implicitl Register	-	pecified in definition Indirect	d.	Base Address
	Size of IR is 12 bits	b.	16 bits	c.	20 bits	d.	32 bits

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	(b)	Short Que. (answer in one sentence) 1. Obtain the 9's complement of following eight-digit decimal numbers 12349876, 00980100, 900009951.	[02]
		2. Obtain the 2's complement of following eight-digit Binary numbers 1010110, 10000001, 10000000	[02]
		 Define following term. Cache hit Interrupt Computer organization Micro-program Pseudo instruction Accumulator 	[06]
<u>Questio</u>	<u>n: 2</u> .		
	(a)	Explain 16-bit common bus architecture.	[80]
	(b)	Explain Arithmetic Logic Shift Unit	[08]
		OR	
	(b)	Explain DMA with block diagram and details.	[08]
Questio	on: 3.		
	(a)	Explain addressing modes with example.	[08]
	(b)	List out all characteristic of RISC	[04]
	(c)	Derive 4-bit adder subtractor circuit. [04]	
	(a)	OR Explain IR with instruction format for 3 types of Instruction.	[08]
	(b)	List out all characteristic of CISC	[04]
	(c)	Explain arithmetic and logical shift with example.	[04]
Questio	on: 4		
	(a)	Computer employs RAM chips of 128*8 and ROM chips of 256*8. The Computer system needs 512 bytes of RAM, 512 bytes of ROM 1. How many RAM and ROM chips are needed? 2. Draw a memory-address map for the system? 3. Give Address range in hexadecimal	[08]
	(b)	Draw Arithmetic pipeline.	[04]
	(c)	Solve the following arithmetic expressions from	[04]

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infix to reverse Polish notation A * B + C * D + E *F1. 2. (A + B) * [C * (D + E) + F]OR (a) Create table for addition and subtraction of signed-magnitude numbers [80] (b) Draw instruction pipeline. [04] Solve following expression into postfix and evaluate using stack. [04] (c) (3*4)+(5*6)/(3*2)Question: 5. (a) Compare RISC vs CISC [80] (b) Explain address sequencing with block diagram and details. [04] (c) Perform multiplication using Booth's Algorithm: (-7) * (+8) [04] OR Compare direct addressing vs indirect addressing [80] (a) (b) Explain techniques for handling Branch Difficulties [04] Perform multiplication using Booth's Algorithm: (+5) * (-20) (c) [04] Question: 6. Solve X = (A+B) * (C+D) using a general register computer with three address [80] (a) instruction and one address instruction. (b) Explain strobe asynchronous data transfer method. [04] (c) A non-pipeline system takes 50 ns to process a task. Same task can be processed [04] in a six-segment pipeline with a clock of 10 ns. Determine the speedup ration of the pipeline for 100 task.

OR

(a) Solve X= (A+B) * (C+D) using a general register computer with two address instruction and zero address instruction.

(b) Explain handshaking asynchronous data transfer method. [04]

(c) Draw Instruction cycle. [04]

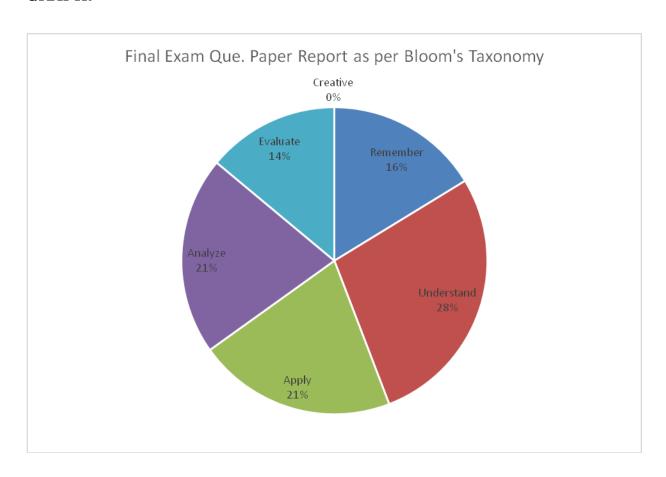
---Best of Luck---

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Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age			
		% of weight -age	Que. No.		
1	Remember/Knowledge	16.27	1(A), 1(B), 3(B), OR 3(B), OR 3(B)		
2	Understand	27.90	2(A),OR 2(B), 3(A), 5(B), OR 5(B), 6(B), 6(B)		
3	Apply	20.93	4(B), OR 4(B), OR 4(C), 6(A), OR 6(A), 6(C), OR6(C)		
4	Analyze	20.93	4(A), 4(C), 5(A),OR 5(A), 5(C), OR 5(C)		
5	Evaluate	13.95	2(B), 3(C), OR 3(C),OR 4(A)		
6	Higher order Thinking	0			

GRAPH:



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