Enroll. No._____

MARWADI UNIVERSITY

Faculty of Technology

Computer Engineering / Information Technology Engineering

B.Tech **SEM: 4th** **SUMMER:2018**

Subject: - (Computer Organization) (01CE0402) **Date:- 21/04/2018**

Total Marks:-100 **Time: - 03:00 hours**

Instructions:

1. **All Questions are Compulsory.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Question: 1.

(a) Select correct option for following questions. [10]

1) In case of nested subroutines, the return addresses are stored in
a. PC b. Stack c. Heap d. Register

2) The DMA transfers are performed by a control circuit called as
a. Device interface b. DMA controller c. Data controller d. Over looker

3) The DMA controller is connected to the
a. Processor BUS b. System BUS c. External BUS d. None

4) Which are the operation that a computer performs on data that put in register
a. arithmetic b. Logic c. Shift d. All

5) Which micro operations carry information from one register to another
a. Arithmetic b. Register Transfer c. Logical d. All

6) Which memory device is generally made of semi-conductors
a. RAM b. Hard-disk c. Floppy disk d. CD Disk

7) To reduce the memory access time, system generally make use of
a. Heap b. RAM c. Cache d. SDRAM

8) Size of PC is
a. 12 bits b. 16 bits c. 8 bits d. 20 bits

9) In which addressing mode operand is implicitly specified in definition
a. Implied b. Register c. Indirect d. Base Address

10) Size of IR is
a. 12 bits b. 16 bits c. 20 bits d. 32 bits

(b) Short Que. (answer in one sentence) [10]

1. Obtain the 9's complement of following eight-digit decimal numbers 12349876, 00980100, 900009951. [02]

2. Obtain the 2's complement of following eight-digit Binary numbers 1010110, 10000001, 10000000 [02]

3. Define following term. [06]
    1. Cache hit
    2. Interrupt
    3. Computer organization
    4. Micro-program
    5. Pseudo instruction
    6. Accumulator

Question: 2.

(a) Explain 16-bit common bus architecture. [08]

(b) Explain Arithmetic Logic Shift Unit [08]

OR

(b) Explain DMA with block diagram and details. [08]

Question: 3.

(a) Explain addressing modes with example. [08]

(b) List out all characteristic of RISC [04]

(c) Derive 4-bit adder subtractor circuit. [04]

OR

(a) Explain IR with instruction format for 3 types of Instruction. [08]

(b) List out all characteristic of CISC [04]

(c) Explain arithmetic and logical shift with example. [04]

Question: 4.

(a) Computer employs RAM chips of 128*8 and ROM chips of 256*8. [08]
The Computer system needs 512 bytes of RAM, 512 bytes of ROM
    1. How many RAM and ROM chips are needed?
    2. Draw a memory-address map for the system?
    3. Give Address range in hexadecimal

(b) Draw Arithmetic pipeline. [04]

(c) Solve the following arithmetic expressions from [04]

infix to reverse Polish notation

1. A * B + C * D + E *F
2. (A + B) * [C * (D + E) + F]

OR

(a)	Create table for addition and subtraction of signed-magnitude numbers	[08]
(b)	Draw instruction pipeline.	[04]
(c)	Solve following expression into postfix and evaluate using stack. (3 * 4) + (5 * 6) / (3 * 2)	[04]

Question: 5.

(a)	Compare RISC vs CISC	[08]
(b)	Explain address sequencing with block diagram and details.	[04]
(c)	Perform multiplication using Booth's Algorithm: (-7) * (+8)	[04]

OR

(a)	Compare direct addressing vs indirect addressing	[08]
(b)	Explain techniques for handling Branch Difficulties	[04]
(c)	Perform multiplication using Booth's Algorithm: (+5) * (-20)	[04]

Question: 6.

(a)	Solve X= (A+B) * (C+D) using a general register computer with three address instruction and one address instruction.	[08]
(b)	Explain strobe asynchronous data transfer method.	[04]
(c)	A non-pipeline system takes 50 ns to process a task. Same task can be processed in a six-segment pipeline with a clock of 10 ns. Determine the speedup ration of the pipeline for 100 task.	[04]

OR

(a)	Solve X= (A+B) * (C+D) using a general register computer with two address instruction and zero address instruction.	[08]
(b)	Explain handshaking asynchronous data transfer method.	[04]
(c)	Draw Instruction cycle.	[04]

---Best of Luck---

Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age	
		% of weight -age	Que. No.
1	Remember/Knowledge	16.27	1(A), 1(B), 3(B), OR 3(B), OR 3(B)
2	Understand	27.90	2(A),OR 2(B), 3(A), 5(B), OR 5(B), 6(B), 6(B)
3	Apply	20.93	4(B), OR 4(B), OR 4(C), 6(A),OR 6(A), 6(C), OR6(C)
4	Analyze	20.93	4(A), 4(C), 5(A),OR 5(A), 5(C), OR 5(C)
5	Evaluate	13.95	2(B), 3(C), OR 3(C),OR 4(A)
6	Higher order Thinking	0	

GRAPH: