A Review of Runtime-Reconfigurable Operand Masking Technique for Energy-Efficient Approximate Processor Architectures

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Abstract—

This paper proposes a runtime-reconfigurable operand masking technique for energy-efficient approximate processor architectures. The approach achieves lower energy consumption using approximate computing techniques in programmable high-performance processors. The technique enables programmable fine-grained accuracy control and switching energy reduction at runtime. The evaluation results show that the proposed approach achieves effective energy reduction for a horizontal SIMD vector processor architecture executing approximate SIFT image feature extraction for an error-resilient egomotion estimation algorithm.

Keywords— *approximate computing, operand masking, energy efficiency, high-performance processors, SIMD vector processor, SIFT image feature extraction, egomotion estimation.*

Introduction—

This paper presents a new approach to achieve lower energy consumption using approximate computing techniques in programmable high-performance processors. The proposed runtime-reconfigurable operand masking technique enables programmable fine-grained accuracy control and switching energy reduction at runtime. The technique is applied to high-performance horizontal and vertical SIMD vector processors to reduce power consumption. The effect is comparable to a reduced datapath width, but the hardware implementation is not application-dependent, and the accuracy-energy design space can be reconfigured deliberately by the programmer at runtime. The paper evaluates the effectiveness of the operand masking technique in terms of masking circuit implementation and area overhead, approximate egomotion estimation accuracy, and overall energy reduction due to masking.

Body—

The paper first introduces a reference application from related work, which is used to evaluate the proposed masking mechanism. The reference application is an error-resilient egomotion estimation algorithm that uses SIFT image feature extraction. The paper then describes the hardware implementation of the approximate vector processors, which employ either vertical or horizontal SIMD data-level parallelism and are designed as accelerating coprocessors for computational intensive image processing tasks. The architectures use conventional precise arithmetic circuits with runtime-reconfigurable approximated operands to achieve fine-grained accuracy selection at the bit-level. The required energy per arithmetic operation is lowered by decreasing the switching activity in the circuit. The paper identifies four computational intensive algorithmic parts in the SIFT implementation that may utilize approximation, i.e., scale-space pyramids construction (Gaussian and DoG), keypoint orientation assignment, descriptor histogram binning, and descriptor normalization. For each of these four parts, the masking control registers are set to defined parameters at runtime. Since there is independent masking of adder and MAC operands by using two control registers, the approximation behavior is described by a total of eight mask parameters.

The paper evaluates the effectiveness of the operand masking technique in terms of masking circuit implementation and area overhead, approximate egomotion estimation accuracy, and overall energy reduction due to masking. The evaluation results show that the proposed approach achieves effective energy reduction for a horizontal SIMD vector

processor architecture executing approximate SIFT image feature extraction for an error-resilient egomotion estimation algorithm. The total system energy savings of up to 4.5% for a 45 nm ASIC technology are achieved without a significant decrease in quality of the application result. The paper also discusses the limitations of the proposed approach, such as the need for additional mechanisms like clock gating to reduce clock-related switching activity in the dominating sequential parts of the circuit. This can lead to design complications during ASIC synthesis and may cause severe performance implications.

Conclusion—

In conclusion, this paper proposes a runtime-reconfigurable operand masking technique for energy-efficient approximate processor architectures. The approach enables programmable fine-grained accuracy control and switching energy reduction at runtime, which is evaluated using an error-resilient egomotion estimation application. The results show that the proposed approach achieves effective energy reduction for a horizontal SIMD vector processor architecture executing approximate SIFT image feature extraction. The paper identifies the limitations of the proposed approach and suggests combining the operand masking technique with other mechanisms like clock gating to reduce clock-related switching activity in the circuit. Overall, the proposed approach provides a promising direction for achieving energy-efficient approximate computing in programmable high-performance processors.