Enroll. No._____

MARWADI UNIVERSITY
MU-FOT
CE-FOT1 (MU)
Semester 4 - Winter

Subject : COMPUTER ORGANIZATION AND ARCHITECTURE (01CE0402)
Date : 18-Nov-2021 **Time : 3 Hours** **Total Marks : 100**

Instructions :

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Que.1 (A) Answer the following objectives **[10]**

(1) The concept of pipelining is most effective in improving performance if the tasks being performed in different stages :
A require different amount of time
B require about the same amount of time
C require different amount of time with time difference between any two tasks being same
D require different amount with time difference between any two tasks being different

(2) With same number of bits, which data type provides largest dynamic range?
a) Sign Magnitude
b) Sign 2's Complement
c) BCD
d) Floating point

(3) What is range of 8-bit Sign 2's complement data?
a) -127 to +128
b) - 128 to +127
c) -127 to +127
d) -64 to +64

(4) By default, memory will consider address from which register?
a) DR b) IR c) TR d) AR

(5) How many numbers of bits will be required to specify address of 4KB RAM?
a) 12 bits b) 13 bits c) 14 bits d) 15 bits

(6) In Arithmetic Pipeline, the floating point addition and subtraction is done in _____ parts.
A. 2 B. 3 C. 4 D. 5

(7) What is range of 6-bit Sign magnitude data?
a) -31 to +31
b) -32 to +32
c) -127 to +127
d) -64 to +64

(8) Arithmetic Pipeline is used for?
A. floating point operations B. interger operations C. character operations D. None of the above

(9) Which register is used to store address of next instruction to be executed?
a)IR b) TR c) DR d) PC

(10) Which addressing mode will give allow larger address space to be accessed?
a) Direct b) Indirect c) Implied d) None

Que.1 (B) Answer the following questions. **[10]**

(1) What does this mean: T0: R4 ← R0?

(2) What is an ALU?

(3) Diffrentiate arithmetic and logical shift with one example

(4) Explain effective address.

(5) What is Data Register

(6) What do you understand by Memory Address?

(7) What is Program Counter

(8) Define Memory Write

(9) Enlist major components of CPU.

(10) Explain Instruction Fetch.

Que.2

(A) What is virtual memory? Explain relation between address space and memory space in vitual memory system. [8]

(B) Show the step by step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers.
i) (+15) x (+13)
ii) (+15) x (-13) [8]

OR

(B) What is speedup? Derive the equation of speedup for k-segment pipeline processing for task. [8]

Que.3

(A)

What is the difference between microprocessor and micro program? Is it possible to design a microprocessor without a micro program? Are all micro-programmed computers also microprocessors? Define micro operation, micro-instruction and micro program in short. [8]

(B) Explain memory stack organization. [4]

(C) Explain Write-through and Write-back cache write method. [4]

OR

(A) How addressing mode is significant for referring memory? List and explain types of addressing modes by applying various addressing modes in memory. [8]

(B) Explain types of Asynchronous data transfer in brief. [4]

(C) Explain subtraction operation with signed 2's complement integer data. [4]

Que.4

(A) Explain data transfer and manipulation instructions. [8]

(B) Explain Stored Program Organization in detail. [8]

OR

(A) Explain shift micro operations and Draw neat and clean diagram for 4-bit combinational circuit shifter. [8]

(B) Draw and explain flowchart for interrupt cycle. [8]

Que.5

(A) In RISC pipeline, explain delayed load by taking suitable example. [6]

(B) Explain addition and subtraction operation using flowchart. [6]

(C) Draw the flowchart for Booth multiplication operation. [4]

OR

(A) Explain I/O interface with details. [6]

(B) Differentiate Machine instrucion and Microinstrucion.Explain mapping of instructions. [6]

(C) Differentiate Direct and Indirect Addressing modes. [4]

Que.6

(A) Explain Flynn's taxonomy for classifying parallel processors. Explain each class. [8]

(B) For the basic computer explain following instructions [4]
1. LDA
2. ADD
3. AND
4. CLA

(C) Define RTL. Explain how register transfer takes place in basic computer system. [4]

OR

(A) Differentiate SIMD, SISD, MISD and MIMD. [8]

(B) Draw the block diagram of common bus system of basic computer. [4]

(C) What is Interrupt? How it is useful for a system? [4]

---Best of Luck---

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Difficulty Level	Weightage Recommended	Actual	No of Question	Total Marks	Question List
High	20	18.60	4	32	2(A), 2(B), 3(A), 4(A)
Low	20	5.23	4	9	1(A), 5(B)
Medium	60	76.16	37	131	1(A), 1(B), 2(B), 3(A), 3(B), 3(C), 4(A), 4(B), 5(A), 5(B), 5(C), 6(A), 6(B), 6(C)

Module Name	Weightage Recommended	Actual	No of Question	Total Marks	Question List
undamental concepts of Micro programmed Control:	5	8.14	2	14	3(A), 5(B)
Input-Output Organization:	5	5.81	2	10	3(B), 5(A)
Memory Classification and Organization:	5	6.98	2	12	2(A), 3(C)
Computer Data Representation & Register Transfer and Micro-operations:	15	8.72	5	15	1(B), 4(A), 6(C)
Introduction to Pipeline:	15	19.19	7	33	1(A), 2(B), 5(A), 6(A)
Basic of Computer Arithmetic:	15	14.53	7	25	1(A), 2(B), 3(C), 5(B), 5(C)
Introduction to Computer Organization and Design:	20	25.00	17	43	1(A), 1(B), 4(B), 5(C), 6(B), 6(C)
Concepts of Central Processing Unit:	20	11.63	3	20	3(A), 3(B), 4(A)

Blooms Taxonomy	Weightage Recommended	Actual	No of Question	Total Marks	Question List
Remember / Knowledge	20	13.95	10	24	1(A), 1(B), 4(B), 6(A)
Understand	30	52.33	27	90	1(A), 1(B), 2(A), 3(B), 3(C), 4(B), 5(A), 5(B), 5(C), 6(A), 6(B), 6(C)
Apply	25	22.09	5	38	2(B), 3(A), 4(A), 5(A)
Analyze	15	11.63	3	20	2(B), 3(A), 5(C)
Evaluate	10	0.00	0	0	
Higher order Thinking	0	0.00	0	0