Enroll. No._____

MARWADI UNIVERSITY

Faculty of Technology

Information Technology / Computer Engineering

B.Tech **SEM:4** **SUMMER-2019**

Subject: - Computer Organization and Architecture (01CE0402) **Date:- 11/04/2019**

Total Marks:-100 **Time: - 03:00 hours**

Instructions:

1. **All Questions are Compulsory.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Question: 1.

(a) Objective MCQ [10]

1) Where the result of an arithmetic and logical operation are stored?
a. Accumulator b. Cache Memory c. ROM d. None

2) Whenever CPU detects an interrupt, what it do with current state?
a. Save b. Discard c. Depends on system d. First finish it

3) The performance of the cache memory is measured in terms of?
a. Hit Ratio b. Chat Ratio c. Miss Ratio d. None

4) Which instruction is used to store content of accumulator into memory
a. ADD b. BSA c. STA d. LDA

5) In case of nested subroutines, the return addresses are stored in
a. PC b. Stack c. Heap d. Register

6) Which are the operations that a computer performs on data that put in accumulator register
a. Arithmetic b. Logic c. Shift d. All

7) Which micro operations carry information from one register to another
a. Arithmetic b. Register Transfer c. Logical d. All

8) To reduce the memory access time, system generally make use of
a. Heap b. RAM c. Cache d. SDRAM

9) Size of PC is
a. 12 bits b. 16 bits c. 8 bits d. 20 bits

10) In which addressing mode operand is implicitly specified in definition
a. Implied b. Register c. Indirect d. Base Address

(b) Short Que. (answer in one sentence) [10]

Define following terms: [4]
Microprogram, Microinstruction, Binary Adder, Effective address

Find 2's complements of following decimal vales: [6]
56, 298, 325

Question: 2.

(a) List and explain pipeline conflicts with details. [08]

(b) Explain DMA with details. [08]

OR

(b) Draw neat and clean diagram of instruction cycle and explain it. [08]

Question: 3.

(a) Draw and explain microinstruction format with details of each fields. [08]

(b) Apply various shift micro-operation by taking proper example. [04]

(c) Draw block diagram of CPU-IOP communication. [04]

OR

(a) Explain common bus architecture with working of all registers. [08]

(b) Differentiate: Direct and Indirect Addressing modes. [04]

(c) Explain BSA and ISZ instruction with details. [04]

Question: 4.

(a) Draw neat and clean diagram of interrupt cycle and explain it. [08]

(b) Differentiate: Hardwired and Microprogrammed Control unit. [04]

(c) Explain various classes of computers according to flynn's classification. [04]

OR

(a) Convert following expression A*B+A*(B*D+C*E) into reverse polish notation and evaluate using stack using following values A=1, B=3, C=4, D=2, E=4. [08]

(b) Explain stack organization with push and pop operations. [04]

(c) A nonpipelined system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the for 100 tasks. What is the maximum speedup that can be achieved? [04]

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Question: 5.

(a) Perform multiplication using booth algorithm for (-13) * (+11). [08]

(b) Differentiate: Memory mapped I/O vs Isolated I/O. [04]

(c) Explain zero, one, two and three addresses instruction by taking suitable example. [04]

OR

(a) Create time-space diagram for 5 segment pipeline and 8 tasks, consider each segment takes 1 second for partial task completion. Find completion time. [08]

(b) Draw and explain 4-bit arithmetic circuit with all operations. [04]

(c) Explain format of basic computer instruction with details. [04]

Question: 6.

(a) Which are the various addressing modes? Explain with details and prepare small Memory map and apply various modes and show the effective address by applying various addressing modes. [08]

(b) Draw neat and clean diagram of control unit of basic computer and explain it. [04]

(c) Explain memory reference instructions by taking suitable value for example and apply instruction on values. [04]

OR

(a) Differentiate: RISC and CISC. [08]

(b) Explain interrupt types with details. [04]

(c) Draw flowchart for floating point arithmetic pipeline. [04]

---Best of Luck---

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Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age	
		% of weight - age	Que. No.
1	Remember/Knowledge	30%	1(b),2(b),3(c),4(a),4(b),4(c), 6(b),6(b)or,6(c)or
2	Understand	39%	1(a),2(a),2(b),3(a),3(a)or, 6(a)or,5(c),3(b)or,5(b),5(b)or
3	Apply	16%	3(b),3(c)or,4(b)or,4(c)or,5(c), 6(a)
4	Analyze	10%	5(a)or,6(c)
5	Evaluate	5%	4(a)or,5(a)
6	Higher order Thinking	0%	Nil

GRAPH: