A Review of Energy-efficient Deep Neural Network Training Processor with Bit-slicelevel Reconfigurability and Sparsity Exploitation

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Abstract—

The paper presents an energy-efficient deep neural network (DNN) training processor with four key features: Layer-wise Adaptive bit-Precision Scaling (LAPS), In-Out Slice Skipping (IOSS) core, double-buffered Reconfigurable Accumulation Network (RAN), and momentum-ADAM unified OPTimizer Core (OPTC). The proposed processor shows 5.9× higher energy efficiency compared to the state-of-the-art on-chip-learning processors.

Keywords—

DNN training processor , Energy efficiency , Bit-slice-level reconfigurability , Sparsity exploitation , Layer-wise adaptive bit-precision scaling , In-Out Slice Skipping , Reconfigurable Accumulation Network , Momentum-ADAM unified optimizer core , Bit-slice serial architect

Introduction—

Training DNN requires a significant amount of computation, which is possible only on cloud servers. However, cloud-based training is not suitable for real-time applications, and it also incurs high energy consumption and communication overhead. To address these issues, the paper proposes an energy-efficient DNN training processor that can perform training on the edge devices.

Body—

The proposed processor has four key features that contribute to its energy efficiency. First, LAPS performs layer-wise adaptive bit-precision scaling to minimize the throughput degradation caused by active precision searching. Second, IOSS core skips the unnecessary computation of zero slices to reduce energy consumption. Third, RAN is a double-buffered reconfigurable accumulation network that reduces the memory access overhead and improves energy efficiency. Fourth, OPTC is a momentum-ADAM unified optimizer core that optimizes the training process and improves energy efficiency.

The proposed processor uses a bit-slice serial architecture (BSSA) that enhances the training speed and efficiency further. It uses 4b × 4b MAC as a base unit and receives a 4b-slice at a time after dividing HBP data into a number of 4b-slices. The processor modifies existing task division methodologies and uses modified methods to support not only the FF stage but also EP and WG stage within limited on-chip and off-chip memory bandwidth.

Conclusion—

In conclusion, this paper presents a Low Power and High Speed 8-bit ALU Design using 17T Full Adder. The proposed design uses multiplexing logic and has a faster signal propagation delay compared to existing designs. The design is optimized to reduce power requirements and minimize delay, resulting in anefficient power-delay product. The proposed design is evaluated through simulations and results show that the proposed design has a 71.5% to 74.3% saving in power requirements compared to existing designs. Theproposed design is a significant contribution to the field of digital processors and can enhance the throughput of digital systems. Overall, the proposed design is a significant improvement over existing designs. The use of a 17T full adder and NMOS pass transistor logic style based multiplexers has resulted in a faster signal propagation delay and a significant reduction in power requirements. The proposed designcan be easily integrated into existing digital systems, and it can enhance the throughput of digital systems. The proposed design can be further optimized for specific applications, and it can be extended to higher bit-widths. The proposed design is a significant contribution to the field of digital processors, and it can pave the way for future research in this area.