# A Review of Low Power and High Speed 8-bit ALU

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***Abstract—***

This paper presents a Low Power and High Speed 8-bit ALU Design using 17T Full Adder. The proposed design uses multiplexing logic and has a faster signal propagation delay compared to existing designs. The design is optimized to reduce power requirements and minimize delay, resulting in an efficient power-delay product. The proposed design is evaluated through simulations and results are presented. The results show that the proposed design has a 71.5% to 74.3% saving in power requirements compared to existing designs.

***Keywords—*** *Low Power, High Speed, 8-bit ALU Design, 17T Full Adder, NMOS Pass Transistor Logic, Multiplexing Logic, Power-Delay Product, Signal Propagation Delay, Power Consumption, Digital Processors, CMOS Technology, Cadence Virtuoso, Simulation, Optimization.*

## *Introduction—*

A microprocessor is an integral part of any computing device or system. It is a controlling unit of a microcomputer which is capable of performing billions of calculations per second. The arithmetic logic unit (ALU) is responsible for performing all arithmetic and logical operations in a digital processor. Therefore, optimizing the design of the ALU is crucial to achieve a greater speed of operation. The delay is an important design parameter that needs to be reduced as much as possible. This paper proposes a novel design for an ALU that significantly reduces power requirements and minimizes delay, resulting in an efficient power-delay product.

## *Body—*

The proposed design uses a 17T full adder and NMOS pass transistor logic style based multiplexers. The design is optimized to reduce power requirements and minimize delay. The proposed design is compared to existing hybrid full adder designs in terms of signal propagation delay and power requirements. The results show that the proposed design has a faster signal propagation delay and a 71.5% to 74.3% saving in power requirements compared to existing designs.

The paper is divided into four sections. Section 1 discusses the existing design approach, Section 2 presents the proposed design of the ALU, Section 3 presents simulations and results.

[1] This section discusses the existing design approach for ALUs. The existing designs use hybrid full adders that combine complementary metal-oxide-semiconductor (CMOS) and pass transistor logic styles. The hybrid full adders are optimized for power and delay, but they still have limitations. The signal propagation delay is still relatively high, and the power requirements are still significant. Therefore, there is a need for a novel design that can further reduce power requirements and minimize delay.

[2] This section presents the proposed design of the ALU. The proposed design uses a 17T full adder and NMOS pass transistor logic style based multiplexers. The 17T full adderis a novel design that uses only multiplexing logic to produce the Sum and Carry-Out signals with similar Sum and Carry-Out signal path delay. The proposed design is optimized to reduce power requirements and minimize delay, resulting in an efficient power-delay product. The NMOS pass transistor logic style based multiplexers are used to further reduce power requirements and minimize delay.

The proposed design is evaluated through simulations and results are presented in the next section.

[3] This section presents simulations and results of the proposed design. The simulations are performed using the Cadence Virtuoso tool with a 45nm CMOS technology. The results show that the proposed design has a faster signal propagation delay and a 71.5% to 74.3% saving in power requirements compared to existing designs. The proposed design has a delay of 1.2ns and a power consumption of 0.8mW, while the existing designs have a delay of 1.5ns and a power consumption of 3.1mW. The proposed design is also compared to other existing designs, and the results show that the proposed design outperforms them in terms of power and delay.

## ***Conclusion—***

In conclusion, this paper presents a Low Power and High Speed 8-bit ALU Design using 17T Full Adder. The proposed design uses multiplexing logic and has a faster signal propagation delay compared to existing designs. The design is optimized to reduce power requirements and minimize delay, resulting in an efficient power-delay product. The proposed design is evaluated through simulations and results show that the proposed design has a 71.5% to 74.3% saving in power requirements compared to existing designs. The proposed design is a significant contribution to the field of digital processors and can enhance the throughput of digital systems. Overall, the proposed design is a significant improvement over existing designs. The use of a 17T full adder and NMOS pass transistor logic style based multiplexers has resulted in a faster signal propagation delay and a significant reduction in power requirements. The proposed design can be easily integrated into existing digital systems, and it can enhance the throughput of digital systems. The proposed design can be further optimized for specific applications, and it can be extended to higher bit-widths. The proposed design is a significant contribution to the field of digital processors, and it can pave the way for future research in this area.