A Low Power and High Speed 8-bit ALU Design using 17T Full Adder

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***Abstract*— In this paper, a novel 17T full adder and its application in implementing an efficient Arithmetic Logic Unit (ALU) design have been proposed. The proposed design will be able to significantly reduce the power requirements of a digital processor. Further, it also minimizes the delay and the design is efficient in terms of power-delay product. The ALU is one of the important entities of a digital processor. In a digital processor, an ALU as the name suggest performs logical and arithmetic operations. Thus, increasing the speed of operation while reducing the power requirements can cause a cumulative increase in the throughput of the digital system. Further, the proposed 17T full adder uses only multiplexing logic to produce the Sum and the Carry-Out signals with similar Sum and Carry-Out signal path delay. Moreover, the signal propagation delay from input to output of the proposed adder has been found to be 83.8% to 89.9% less as compared to existing hybrid full adder design like HFA-22T, HFA-20T and HFA-19T as well as full adders like 10T and 11T. Further, 71.5% to 74.3% saving in power requirements has been observed. Thus, the proposed 8-bit ALU has also been able to perform almost 52% better than the existing design in terms of the overall power-delay product. We have simulated the designs as well as evaluated the results using the Cadence Virtuoso EDA tool v15.0 in 45 nm process technology. Performance analyses were done with respect to power, delay, and power-delay product.**

Keywords—ALU, XOR, Multiplexer, Adder, Design, Power, Delay, Processor

I. INTRODUCTION

In today's world we are moving towards developing technologies that consume as much less power as possible, this comes with an increasing demand for battery-operated portable devices such as cell phones, wearables and laptops. Therefore, low power VLSI is a trending area of research, where an engineer works on a transistor level to find a trade-off between power dissipation and propagation delay. Complementary metal-oxide-semiconductor (CMOS) has been a key element in the design of a low power digital logic circuits including a microprocessor and an ALU within it. The static power consumption of a CMOS device is almost negligible, which is due to leakage current only. However, the dynamic power dissipation is significant and is the addition of the transient power consumption (PT), and capacitive-load power consumption (PL). This power is mostly dissipated in translating charges in the parasitic capacitors in the CMOS gates. There are various methods to control the power consumption at the device level which includes scaling, varying frequency of operation or supply voltage, changing the load capacitances, etc.

Further, apart from controlling power at the device level, we can also control power consumption either at the architecture or module level. Here, in this paper, we are concerned about optimizing power requirements at the module level.

A microprocessor is an integral part of any computing device or system. It is a controlling unit of a microcomputer which is capable of performing billions of calculations per second. Further, all such arithmetic and logical operations are performed with the help of the arithmetic logic unit inside a digital processor. Thus, for the effective operation of a digital processor, we need to optimize the design of the ALU in order to meet a greater speed of operation. Hence, the delay also becomes one of the important design parameters which needs to be reduced as less as possible.

In this paper, we mainly focus on reducing the power, delay and thus deducing the optimum power-delay product (PDP) of an ALU, using 17T full adder and NMOS pass transistor logic style based multiplexers. The rest of the paper has been distributed in 4 sections namely II. Existing Design Approach III. Proposed Design of ALU IV. Simulations and Results V. Conclusion.

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II. EXISTING DESIGN APPROACH

A full-adder and a multiplexer are the building blocks of an ALU and can be re-designed in several ways to get an optimum design. There have been several works done in the field of low power and fast full-adder design such as hybrid full adders (HFA) [1], low power 11-transistor full adder (FA) [10], Transmission Gate (TG) full adder [4][5]. Further, ALU has also been designed using FinFET technology which also has two gates that are electrically independent, makes the circuit more simpler in design, while the leakage current has been further reduced to lower down the power consumption [8]. Though, FinFETs are complex to fabricate thus are on the costlier side as compared to planar transistors. Further, attempt of designing an ALU using the reconfigurable logic of multi-input floating gate metal oxide semiconductor (MIFG-MOS) transistor has been done. It helps in increasing the functional capacity of the circuit. MIFG-MOS transistor too helps in making the circuit simpler, which further leads to improved performance of the circuit [9].

Furthermore, the Gate diffusion input technique (GDI) based multiplexer has been used earlier, which is an area-efficient technique at the same time is allowing less power consumption [11]. Gate diffusion input technique is reliable for low voltage operations [13].

In this paper, we propose an efficient ALU design by utilizing 17T full adder and NMOS multiplexers based on pass transistor logic style [12] which are highly optimized in terms of power consumption and delay. The high speed of operation achieved by the proposed 17T full adder compensates the extra transistors used, as compared to the existing 10T full adder [6]. Further, the use of low power XOR gates [1] significantly improves the performance of our ALU.

III. PROPOSED DESIGN OF ALU

The design which has been proposed by Sharma et. al [2] provides good results in terms of power dissipation and delay. However, the output arithmetic results are not reliable in case of the input combinations “000”, “010” and “110”. This made the requirements for an additional NMOS gate at the output of the full adder used. Thus, this causes an increase in an extra RC delay at the output node of the adder circuit, which causes output loading and is undesirable. However, our proposed 8-bit ALU has no such requirement. In an ALU layout design, the area occupied by a full adder and a multiplexer is much greater as compared to another element. Thus, our main focus is to optimize the performance of these two modules. Further, in the existing ALU design, the full adder and the multiplexers utilizes a large number of intra-module connections which is more problematic as compared to inter-module interconnects. Thus, the more the number of local interconnections, the more the number of overlapping interconnects. Additionally, the overlapping interconnects act as a parallel plate capacitor which adds to RC delay along the path. As given by the below equation (1).

$$\text{Clumped total} = C_{\text{parallel-plate}} + C_{\text{fringe}} + C_{\text{path}} \quad (1)$$

Moreover, the increase in the path capacitance will cause more dynamic power dissipation during switching events. The power dissipation becomes significant at the higher operating frequency, which elevates the power requirements of the circuit. Thus, reducing the number of logic gates from the circuit using simplified logic is the goal of our design.

We have designed a 8-bit ALU by utilizing a proposed 17T full adder because it offers a very less carry propagation delay. Further, a similar time to generate the Sum and Carry signals has also been observed. This renders an increase in the speed of operation of the ALU. Furthermore, the 17T full adder has been designed with a low power multiplexers and a XOR gate.

As an ALU is a digital circuit and considered as one of the integral elements of a processor for various operations, like addition, subtraction, compliment, XOR, AND, OR etc. The truth table for all these operations is given in Table 1. The three bits S2S1S0 represents the selection lines for selecting out the operation to be performed by the ALU. Further, there can be one or more than one ALUs in a processor depending on the application.

TABLE I. TRUTH TABLE FOR ALU

S0	S1	S2	OPERATION
0	0	0	ADDITION
0	0	1	XOR
0	1	0	XNOR
0	1	1	NOT
1	0	0	SUBTRACTION
1	0	1	AND
1	1	0	OR
1	1	1	NOR

The ALU that we are proposing, consists of two basic components adders and multiplexers. Further, the adders are itself designed by using XOR gates and multiplexers. The same XOR and similar logic style can be used to generate other logic signals like AND, OR. The following sub-sections disclose all the elements that we have used for our design, and finally the proposed 8-bit ALU.

A. Low power XOR gate

We are using a low power XOR gate [1] for our 17T full adder design. The given XOR consists of 5 transistors. Further, the critical path of the circuit is devoid of NOT gates. The effect of this is that this optimum gate allows low delay and better driving capabilities as compared to conventional ones. Furthermore,There is presence of asymmetric capacitances at the inputs A and B of the XOR circuit, as shown in Fig. 1. Moreover, during the optimum condition the capacitances of the input A and B of transistors N2 and N3 are unequal. Therefore, the input A, which is also connected to the CMOS inverter, is being connected to the transistor with smaller input capacitance. The power requirements of the circuit is hence greatly reduced. Additionally, this circuit also offers less delay, full-swing output, better driving capability. The given XOR circuit is saving almost 16.2% in PDP, and it is 10% faster in the best possible way than the other conventional circuits.

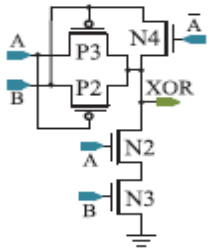


Fig. 1 Low power XOR gate

B. NMOS-Multiplexer

Multiplexers play a key role in switching between various operations in an ALU. In our design, we are using the NMOS pass transistor logic style based multiplexer design. It uses a total of four transistors in which two of the NMOS transistors are responsible for selecting the signals at the inputs. Both the NMOS transistors are having the same threshold voltage. Further, all the physical parameters of both the NMOS transistors are the same be its length, width, etc. Depending upon the number of inputs requirements and the number of usable select lines, we are using as 2-to-1 and 4-to-1 multiplexers. The reason for selecting the NMOS based logic style for the multiplexer is that it offers a simpler design with less number of total transistors which is only 4. Thus, this leads to the reduction of parasitic capacitances and less interconnect delay. Moreover, the earlang delay calculation yields minimum delay from input to output node for this multiplexer as compared to other available multiplexers.

Thus, because of the overlying characteristics, it offers less power consumption and delay. Also, it is better to be used in our design as compared to the several logic styles such as CMOS Transmission gate (TG), Double pass-transistor logic (DPL), LEAN Integrated pass gate logic (LEAP), etc.

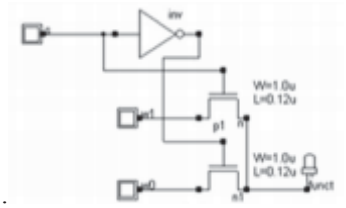
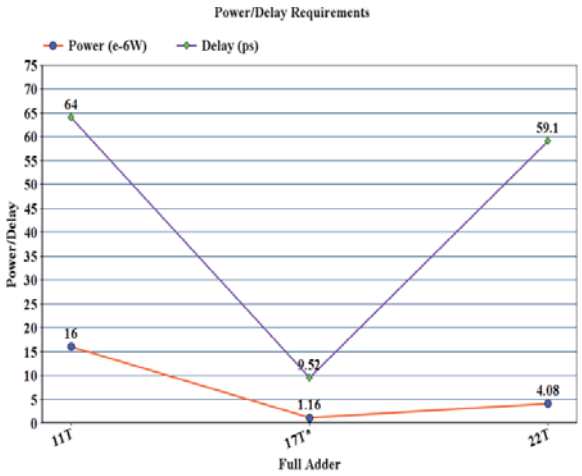


Fig. 2 PTL based 2-to-1 NMOS multiplexer

C. Novel 17T Full Adder

We are using FA-17T i.e. 17 transistors full adder in our ALU design. Fig. 4 depicts the full adder used for our ALU design. Further, the function of this full adder in our ALU is to perform all the arithmetic operations as indicated in the Table 1. Furthermore, the adder is made with the use of low power XOR gates as discussed previously. Moreover, we have used NMOS pass transistor logic style based 2-to-1 multiplexer as discussed, for our full adder design. The advantage of this adder structure is that it provides lower power dissipation, high speed of operation to generate the Sum and the Carry signals and invariance towards device scaling. Further, as compared to existing hybrid full-adder structures like 17T, 19T, 20T, 22T etc. the power, delay and the power-delay product (PDP) have been found out to be minimum. For comparison, we have considered the most optimum hybrid full adder out of the aforementioned ones i.e HFA 22T. We have observed a 71.5% reduction in power requirements of the proposed 17T full adder from 4.08 e-6 W to 1.16 e-6 W. Similarly, there has been 83.8% increase in the speed of operation i.e the average delay has been reduced from 59.10 ps to 9.52 ps, with 29.55 ps as the critical propagation delay. Further, it also offers a simpler design topology. Fig. 3 shows the performance comparison as discussed. Further, if we compare 11T or 10T full adders to our 17T full adder, although both the full adders seems to offer a somewhat less number of transistors but the 17T FA

provides 85% faster response to propagate the Carry signal. Moreover, 17T full adders offer 92% improvement in power consumption. In the case of 11T full adder, the average delay comes out to be 64 ns while the average power consumption as 16 e-6W.



*Means proposed design

Fig. 3 Power/Delay comparison of the proposed 17T full adder with 11T full adder and 22T hybrid full adder

The full adder uses the logic that whenever the A XOR B = 0, the Carry-Out (C_{out}) signal is equal to the input signal A or B else it is equal to Carry-In (C_{in}) signal. Further, whenever the A XOR B = 0, the Sum signal (Sum) is equal to the Carry-In (C_{in}) signal else it is equal to complement of Carry-In ($\tilde{C}_{in}$) signal. One thing to note here is that we could have used a low power XNOR gate (similar to XOR gate) to fed the select line of the multiplexer. But, we are deliberately using a CMOS inverter to complement the intermediate A XOR B signal instead of A XNOR B. Because, it dramatically reduces the total number of transistors required from 25 to 17. Further, we wanted to use only XOR logic as the select lines to generate the Sum as well as the Carry signals.

Additionally, the choice of NMOS multiplexer among a variety of multiplexers available has an added advantage that we have already discussed in section B. Further, instead of using an extra XOR gate to produce the Sum signal we are using an additional NMOS multiplexer. Thus, using an additional multiplexer instead of a XOR gate does help in reducing average power consumption i.e. 112.9e-9 W for the NMOS multiplexer as compared to 359.0e-9 W for the XOR gate. Thus, our adder consists of two similar multiplexers to generate two different signals one is Sum and the other is Cout. Moreover, the propagation delay of the Sum and the Carry-Out signal from the input to the output are almost equal.

D. Proposed 8-bit ALU Design

Firstly, the proposed 1-bit ALU cell is designed with the help of three different modules namely NMOS multiplexer, XOR gate and 17T Full Adder. Further, to increase the operations, we suggest an 8-bit ALU that could perform additional logic funtions like NOR, AND and arithmetic like Subtraction. Fig. 9 and Fig. 12 depicts the schematics of the proposed 1-bit ALU cell and the 8-bit ALU design respectively. The given 8-bit ALU consists of two 8-bit inputs, one 8-bit output, three selection lines, and one carry input/ output each cell. The proposed ALU is designed in 45 nm technology.

The logical operations are performed with the use of low power XOR [1] and NMOS gates accompanied by the cascaded multiplexers. The full adder used here itself consists of similar XOR gates and multiplexers, thus overall ALU unit looks like a chain of XOR gates, cascaded with the help of the multiplexers. For an 8-bit ALU, we require a total number of sixteen 4-to-1 NMOS multiplexers, eight 2-to-1 NMOS multiplexers and eight 17T Full Adders.

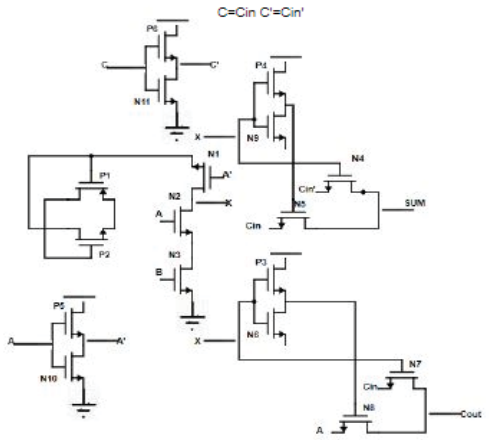


Fig. 4 Proposed 17T full adder

IV. SIMULATIONS AND RESULTS

The design and simulation have been done with the help of Cadence Virtuoso EDA tool v15.0 in 45 nm process technology. Fig. 5 shows the schematic of the novel 17T full adder used in our proposed ALU design. We have used 3-terminal MOS while the power supply given to the circuit is 1.2 V at an operating frequency of 1 GHz. The input signals A, B and Cin have been given as pulsating inputs with a time period of 4 ns, 8ns, 16 ns respectively having rise/fall time of 2 ps each. Further, Fig. 6-8 shows the simulation results of the novel 17T full adder.

Moreover, the Sum and Carry-Out signal for all the possible input combinations has been shown in the simulation waveform.

Fig. 10-11 shows the simulation results of the proposed 1-bit ALU cell. The proposed ALU design consumes less power and incurs less propagation delay, thus performs better as compared to the conventional one. Table 2 indicates the value for each of the power consumption, delay and the corresponding power-delay product for various optimum designs. The power indicates the average of the total transient power taken over a run time of 100 ns. Similarly, the delay indicates the average input to output signal propagation delay at each instant time for 100 ns. Thus, comparing the results it can be seen that the proposed full adder and the proposed 8-bit ALU and 17T full adder offers a better performance.

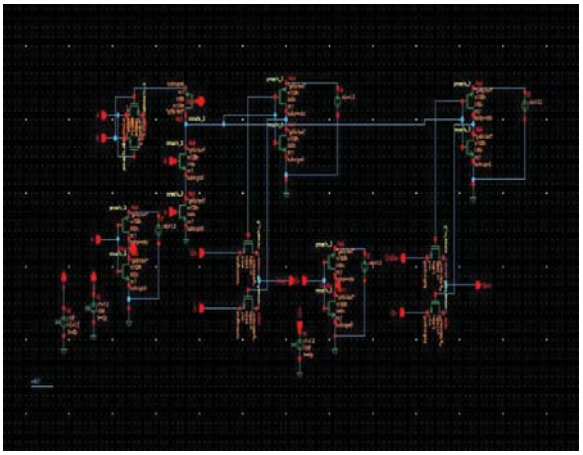


Fig. 5 Schematic of proposed 17T full adder

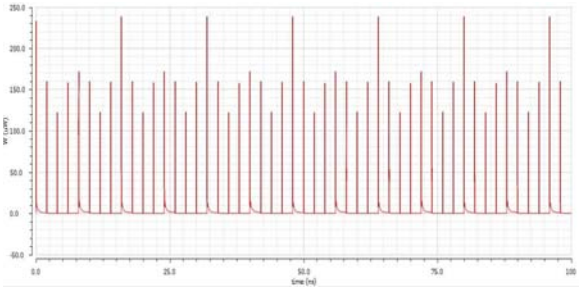


Fig. 6 Transient Power requirements of 17T full adder

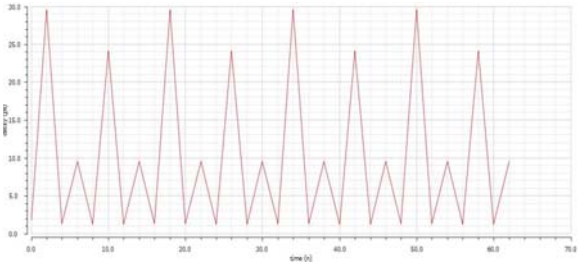


Fig. 7 Transient propogation Delay of 17T full adder

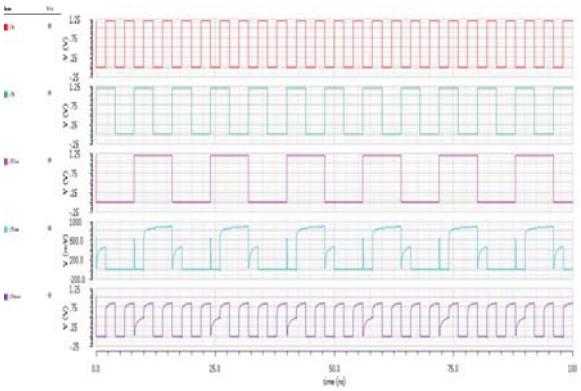


Fig. 8 Simulation output waveform for 17T full adder

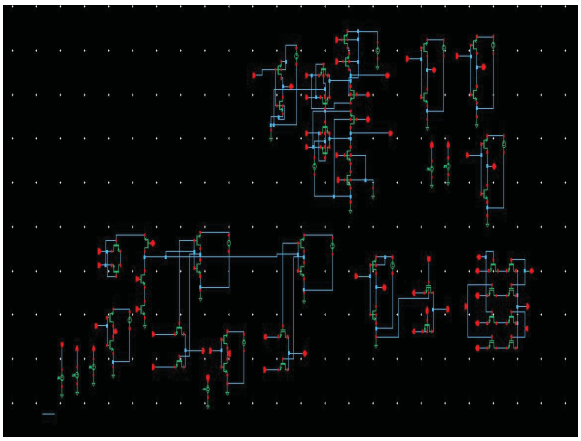


Fig. 9 Schematic of proposed 1-bit ALU cell

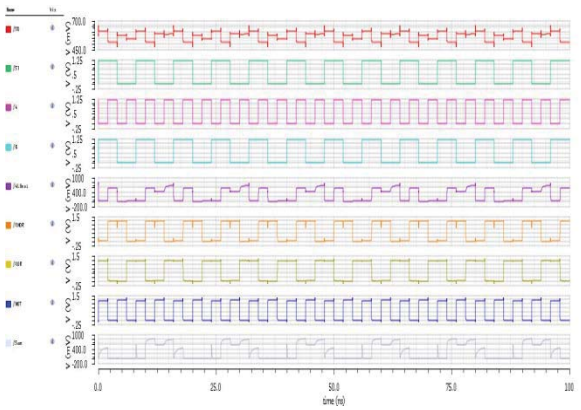


Fig. 10 Simulation output waveform for 1-bit ALU cell

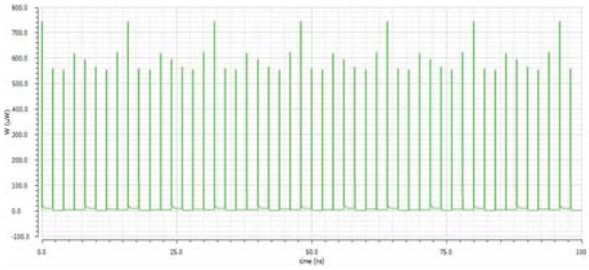


Fig. 11 Transient Power requirements of 1-bit ALU

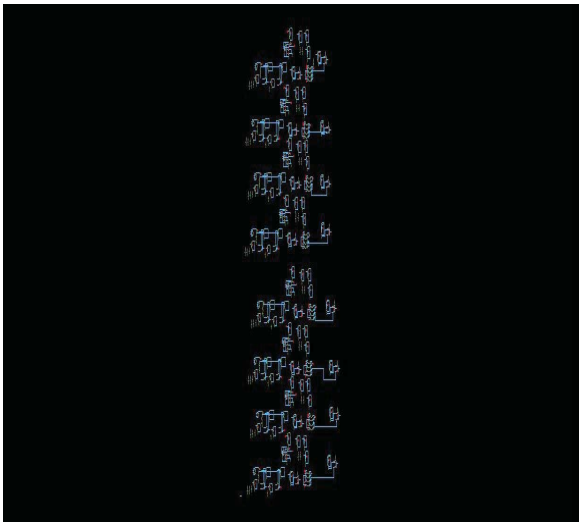


Fig. 12 Schematic of proposed 8-bit ALU

TABLE II. SIMULATION RESULTS (POWER IN e-6W, DELAY (units), AND PDP IN aJ) FOR DIFFERENT DESIGNS

Design	Power	Delay	PDP
FA-11T	16	64 ps	1024
HFA-22T	4.08	59.1 ps	241.1
*FA-17T	**1.16**	**9.52** ps	**11.04**
1-bit ALU [2]	4.47	20.33 ns	90.87
*1-bit ALU	**3.82**	**15.58** ns	**59.51**
8-bit ALU [2]	32.9	6.95 ns	228.65
*8-bit ALU	**26.30**	**4.18** ns	**109.93**

*Means proposed design

V. CONCLUSION

In this paper, we have worked on evaluating the performance of various existing full adders and hybrid full adder. Further, all these adder circuits use a number interconnect/wire of varying lengths to propagate the signal. Thus, because of the varying RC delay along the path, the Sum and Carry signals take different times to propagate. When we are dealing with one-bit input this will not pose a problem but in case of multi-bit inputs, these kinds of circuits will have major drawbacks of a greater carry propagation delay, which affects the overall speed of operation of the digital system wherever it is being used. Also, the use of one or more logic gates in the circuit to implement the sum operation imposes two other drawbacks. First, it involves most of the series MOS connection which causes an increase in power consumption. Second, this involves greater area required for the layout design. All of these drawbacks have been resolved in our proposed 17T full adder design. Further, we have evaluated various multiplexer design and XOR gates to find the most optimum one. Finally, by using the proposed 17T full adder, NMOS pass transistor logic style based multiplexer and a low per XOR gate we have designed a 1-bit ALU cell. Which is then extended to 8-bit ALU intending to optimize the performance of a digital processor. The simulation results/outcomes show that the proposed 17T full adder saves 95.4% to 98% in the PDP while the proposed 8-bit ALU gives almost 52% reduction in the PDP.

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