Enroll.	No.	



MARWADI UNIVERSITY

Faculty of Technology

Information and Communication Technology

B.Tech SEM: III **WINTER:2018**

Subject: - Computer Organization and Architecture (01CT0301) Date: - 20/10/2018 **Total Marks:-100** Time: - 03:00 hours

Instructions:

1. All Questions are Compulsory.

c. 20 d. 8

- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

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ion: 1.	Do As Directed:	
(a)	Multiple Choice Questions:	[10]
	1. (42) ₁₆ = () ₂ a. 11001111 b. 10101010 c. 10001000 d. 01000010	
	2. (101101) ₂ = () ₈ a. 32 b. 47 c. 55 d. 27	
	 3. The size of Data Register is bits. a. 12 b. 16 c. 20 d. 8 	
	 4. The instruction CLA the Accumulator. a. Sets b. Clears c. Flips d. Resets 	
	 5. Which of the following is a logical micro-operation? a. CLA b. ADD c. BSA d. BUN 	
	6. The size of Temporary Register is bits. a. 12 b. 16	

1 | MARWADI UNIVERSITY

	7. The size of Address Register is bits. a. 12 b. 16 c. 20 d. 8		
	 8. The carry if generated by addition of two numbers is stored in bit. a. E b. F c. G d. A 		
	9. The size of Instruction Register is bits. a. 12 b. 16 c. 20 d. 8		
	10. The size of Accumulator is bits. a. 12 b. 16 c. 20 d. 8		
(b)	Answer the following questions in one sentence:	[10]	
	 What is meant by Computer Architecture? Define Accumulator. Define Micro-Operation Define Effective Address What is meant by an assembler? What is Register Transfer Language? Write the functionality of Instruction Register for Basic Computer Architecture. Write the functionality of ISZ instruction with reference to assembly Language prog Write the functionality of Data Register for Basic Computer Architecture. Write the functionality of Address Register for Basic Computer Architecture. 	gram.	
Question: 2. A	Answer the Following Questions:		
(a)	Explain hardware Implementation of common bus system along with neat sketch of the bus architecture. Also explain the selection of any register w.r.t. the selection lines.	[08]	
(b)	Explain different types of micro-operations in basic computer architecture.	[08]	
(b)	OR Draw a flowchart for first pass of an assembler and explain the same in brief	[08]	
Question: 3.	Answer the Following Questions:		
(a)	Discuss four-segment instruction pipeline with diagram(s).	[08]	
(b)	What is assembly language? How it differs from Middle Level Languages like 'C Programming Language'? [04]		
(c)	What is meant by stack? Explain Push and Pop Operations with reference to the stack.	[04]	
	OR		

MARWADI UNIVERSITY 2 |

(ł	 (b) Draw a timing diagram with waveform assuming that SC is cleared to 0 at time T₃ if control signal c₅ is active. C₅T₃: SC →0 C₅ is activated with the positive clock transition associated with T₃. 		[04]
(0	c)	Explain whether the following microoperations can be executed or not? If no, Write the correct sequence of microoperations: (i) IR ← M[PC] (ii) AC ← AC+TR	[04]
Question	: 4.	Answer the Following Questions:	
(8	a)	Explain pipelining hazards giving examples	[08]
(t	b)	(i) Explain the meaning of following microoperation:	[04]
		yT3: $R2 \leftarrow R1$, $R1 \leftarrow R2$ (ii) Show the block diagram of hardware that implements the above register transfer	r statement.
(0	c)	Write an assembly language program to flip/toggle all the bits stored at location 500.	[04]
		OR	
(8	a)	Explain zero, one, two and three address instructions.	[08]
(t	b)	List and explain the two major types of addressing modes with reference to the Basic Computer Architecture along with necessary diagrams.	[04]
(0	c)	Explain the meaning of parallel processing. State two advantages of parallel processing.	[04]
Question: 5. Answer the Following Questions:			
(8		Write a brief note on sub-routine call and return instructions with an assembly program explaining them.	08]
J)	int a= b=	or the given C code, write the assembly language program: t a,b,c; 41; -21; a+b;	04]
(0	c) V	Write 4 points of characteristics each for RISC and CISC computer processors.	[04]
		OR	
(8	a) Ex	aplain FLYNN'S classification in detail.	08]
(1		explain the statement, "pipelining technique is more preferable than the inventional instruction execution", giving suitable example.	[04]
(6	in 1.	non-pipeline system takes 48 ns to process a task. The same task can be processed a six-segment pipeline each with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved in the above case? Justify your answer.	[04] wer.

Write a detailed note on instruction cycle with neat diagrams and flowchart.

(a)

[08]

MARWADI UNIVERSITY 3 |

Question: 6. Answer the Following Questions:

- (a) Draw a flowchart for multiplication of two numbers. Write an Assembly Program for multiplying 2 numbers stored at locations 600 and 700.
- (b) Write an assembly language program to add 10 numbers from memory stored at location starting from 600. [04]
- (c) Write an assembly program to perform logically OR of two numbers without using "OR" instruction [04]
- (a) Write an assembly code to perform the XORing between two numbers and store into another variable i.e. $Z = X \oplus Y$. [NOTE: Take inputs X and Y from the user at run time].
- (b) List the assembly language program (of the equivalent binary instructions) generated by [04] a compiler for the following IF statement. Let the location for variable X be 500.

$$if((A-B) == 0) \\ X=10;$$
 else
$$X=20;$$

(c) Write a program loop, using a pointer and a counter, that sets the value to 1, the contents of hexadecimal locations 500 through 54F. [04]

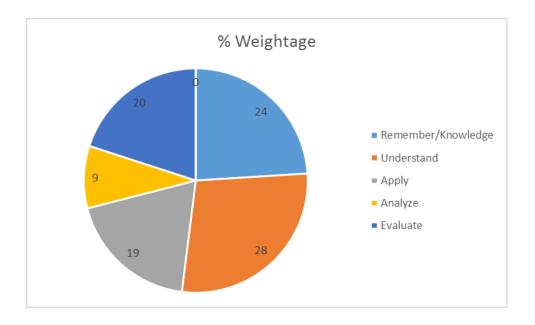
---Best of Luck---

MARWADI UNIVERSITY 4 |

Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age	
		% of	Que. No.
		weight -age	
1	Remember/Knowledge	24	Q.1 (a,b), Q.2 (a,b OR b)
2	Understand	28	Q.3(a OR a), Q.4(a OR a), Q.5 (a OR a)
3	Apply	19	Q.3 (b,c OR b,c), Q.4 (b OR b), Q.5 (c OR
			b)
4	Analyze	9	Q.4 (c OR c), Q.5 (c OR b)
5	Evaluate	20	Q.6 (a,b,c OR a,b,c)
6	Higher order Thinking		

GRAPH:



MARWADI UNIVERSITY 5 |