A Review of TCMP and CHIPPER Router design for Power Efficient Network on Chips

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Abstract—

The paper titled "TCMP and CHIPPER Router design for Power Efficient Network on Chips" discusses the design and implementation of Network on Chip (NoC) routers to overcome the limitations of conventional bus-based communication. The authors highlight the importance of NoC in improving scalability, latency, and power efficiency in on-chip connections. They also introduce the concept of deflection routing to reduce power consumption and design area. The paper aims to present the details of TCMP and CHIPPER router designs and their performance analysis.

Keywords— Network on Chip, Tiled Chip Multiple Processor, CHIPPER, latency, deflection

Introduction—

The abstract provides a concise overview of the paper's content. It mentions the significance of NoC as a design platform for on-chip connections and the need to reduce latency and deflection rate without compromising operating speed. The authors introduce the TCMP and CHIPPER router designs, which utilize permutation deflection logic. The results show that CHIPPER router reduces the normalized router area by 36.2% compared to BLESS router and the normalized critical path by 29.1% compared to a normal VC buffer router.

Body—

The body of the paper is divided into several sections that provide a comprehensive analysis of the TCMP and CHIPPER router designs and their performance. The authors discuss the NoC routing techniques, including XY routing and minimal north last routing, and provide examples to illustrate their effectiveness. They also explain the switch arbitration process based on age-based priority.

The paper presents the pattern and latency analysis of the CHIPPER router, comparing it with a normal VC buffer router. The results show that the CHIPPER router significantly reduces the latency of packets and improves performance. The authors also analyze the normalized router area and the normalized critical path, demonstrating the superiority of the CHIPPER router in terms of reduced area and critical path length.

Conclusion—

The conclusion summarizes the key findings of the paper. The authors emphasize that the TCMP and CHIPPER router designs offer improved performance and power efficiency compared to conventional buffer-based routers. The use of permutation deflection logic and parallel port allocation in the CHIPPER router reduces deflection rate and latency. The normalized router area and normalized critical path are also significantly reduced. The paper concludes by suggesting future research directions in reducing the normalized router area and critical path further.

Overall, the paper provides a detailed analysis of the TCMP and CHIPPER router designs and their performance in terms of latency, area, and critical path. The findings highlight the potential of these designs in improving the efficiency of Network on Chip systems.