

MARWADI UNIVERSITY

Faculty of Technology

Computer Engineering / Information Technology Engineering

B.Tech SEM: 4th **SUMMER:2018**

Subject: - (Computer Organization) (01CE0402) Date: 21/04/2018

Total Marks:-100 Time: - 03:00 hours

Instructions:

1. All Questions are Compulsory.

2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

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Ouestion:	

es ti	on: 1.						
	(a) Select correct o	ptio	n for following questi	ons.			[10]
1) a.	Where the result of an a Accumulator		netic and logical oper Cache Memory		n are stored? ROM	d.	None
a.	Whenever CPU detects Save		nterrupt, what it do w Discard		urrent state ? Depends system to system	d.	First finish it
3) a.	RISC stands for ? Risk Instruction Source Computer	b.	Reduced Instruction Set Computer	c.	Risk Instruction Set Computer	d.	Risk Instruction Set Computing
4) a.	The performance of the Hit Ratio		he memory is measure Chat Ratio		terms of ? Miss Ratio	d.	None
5) a.	Which registers can inte		with the secondary s		ge TR	d.	None
6) a.	During the execution of MDR	_	ogram which gets init		zed first PC	d.	MAR
7) a.	What converts the progr Machine compiler		written in assembly Interpreter		uage into machine ins Assembler		tions. Converter
8) a.	What indicate the starting ORG	ıg po b.	~		the program block is HEX		e stored? None
9) a.	Which directive specifie LDA		e end of execution of STA		ogram. END	d.	XCHNG

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(b)	Short Que. (answer in one sentence) 1. Convert the following binary number to decimal numbers 01011, 011101, 1010101.	[10] [02]
	2. Obtain the 2's complement of following eight-digit Binary numbers 1010110, 10000001, 10000000	[02]
	 Define following term. Compiler Parallel processing Accumulator Micro-operation Effective address sequencer 	[06]
Question: 2.		
(a)	Explain instruction cycle.	[08]
(b)	List out all addressing mode and explain all addressing mode.	[08]
	OR	rumber to decimal numbers [02] [7 following eight-digit Binary numbers of the properties of the prop
(b)	Explain SIMD, SISD, MISD, MIMD	[08]
Question: 3.		
(a)	Compare direct addressing vs indirect addressing	[08]
(b)	List out basic computer register with size and write a function of each.	[04]
(c)	Explain Tri-state buffer with block diagram and details.	[04]
(a)		
(b)	(b) List out input-output instruction with proper meaning	
(c)	Explain Data Transfer Instruction with description.	[04]
Question: 4.		
(a)	Explain interrupt cycle.	[08]
(b)	Draw and explain Adder Subtractor circuit	[04]
(c)	A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction code has 4 parts. Indirect bit, opcode, register code part to specify one of 64 registers and address part. 4. How many bits are there in opcode, register code part and the address part 5. Draw Instruction word format and Indicate the number of bits in each part	?

c. Software

d. All

10) Interrupts which are initiated by an I/O drive are known as a. Internal b. External c. Softw

a. Internal

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		UK	
	(a)	Explain arithmetic pipe line	[08]
	(b)	Draw and explain Timing and control circuit block diagram.	[04]
	(c)	Starting from an initial value of $R=11011101$, Determine the sequence of binary values in R after a logical shift – left, followed by a circular shift-right, followed by a logical shift – right and a circular shift-left	[04]
Questic	on: 5.		
	(a)	Explain instruction pipeline with flowchart	[08]
	(b)	Differentiate Hardwired Control vs Micro Programmed Control.	[04]
	(c)	Apply selective set, selective complement and selective clear operation With suitable example.	[04]
		OR	
	(a)	Explain CPU-IOP Communication with diagram	[08]
	(b)	List out register reference instruction with name	[04]
	(c)	Solve following infix expression into post fix and evaluate using stack. (3+4) [10(2+6) 8]	[04]
Questic	on: 6		
	(a)	Solve multiplication using Booth algorithm for (+15) * (-13)	[08]
	(b)	Draw 4-bit arithmetic circuit.	[04]
	(c)	Explain cache mapping techniques with details.	[04]
		OR	
	(a)	Solve multiplication using Booth algorithm for (-8) * (+7).	[08]
	(b)	Draw common bus system using general purpose registers	[04]
	(c)	Explain pipeline conflicts with details	[04]

6. How many bits are there in the data and address inputs of memory?

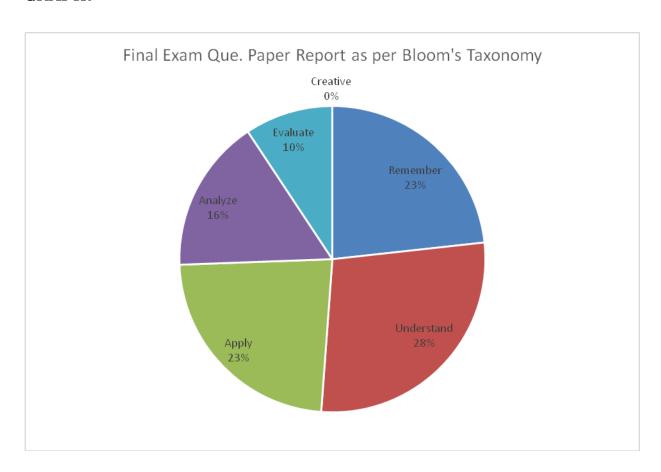
---Best of Luck---

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Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age		
		% of weight -age	Que. No.	
1	Remember/Knowledge	23.25	1(B), 1(B), 2(B), 3(B), OR 3(B), OR 5(B)	
2	Understand	27.90	2(A), OR 2(B), 2(C), OR 2(C), 4(B), OR 4(B), 5(B),	
3	Apply	23.25	4(B), OR 4(B), 5(C), OR 5(C), 6(A), OR 6(A), 6(B), OR 6(B)	
4	Analyze	16.27	3(A), OR 3(A), 4(C), OR4 (C), 5(B)	
5	Evaluate	9.30	OR 5(A), 6(C), OR 6(C)	
6	Higher order Thinking	0		

GRAPH:



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