Enroll. No._____

MARWADI UNIVERSITY

Faculty of TECHNOLOGY

COMPUTER ENGINEERING/ INFORMATION TECHNOLOGY

B.TECH. **SEM: 4** **SUMMER: 2019**

Subject: - computer organization & architecture (01CE0402) **Date:- 11/4/2019**

Total Marks:-100 **Time: - 03:00 hours**

Instructions:

1. **All Questions are Compulsory.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Question: 1. (a) Answer below the given MCQs [10]

1. Below is not type of Micro-operation.

   A: Register transfer B : Arithmetic C: Logic D: Floating point

2. Full for of RISC architecture is:

   A: Reduced instruction set computer(RISC) C: Reduced instruction size computer(RISC)

   B: Resized instruction set computer(RISC) D: none of above

3. Each stage of pipelining should be completed within _____ cycle.

   A: 0 B : 1 C: 2 D: Undefined

4. In reverse polish notation, expression A*B+C*D is written as

   A: AB*CD*+ C: AB*CD+*

   B: A*BCD*+ D: A*B*CD+

5. SIMD represent an organization that

   A: refers to a computer system capable of processing several programs at the same time

   C: includes many processing unit under the supervision of a common control unit.

   B: represents organization of single computer containing a control unit, processor unit and a memory unit.

   D: none of the above.

6. Floating point representation is used to store

   A: Boolean values B : whole numbers C: real integers D: integers

7. In computers, subtraction is generally carried out by

   A: 9's complement B : 10's complement C: 1's complement D: 2's complement

8. What characteristic of RAM memory makes it not suitable for permanent storage?

   A: too slow B : unreliable C: it is volatile D: too bulky

9. Computers use addressing mode technique for _____.

A: Giving programming versatility to the user by providing facilities as pointers to

C: specifying rules for modifying or interpreting address field of the instruction

B: To reduce no. of bits in the field of instruction

D: All the above

10. Cache memory act between

A: CPU and RAM B : RAM and ROM C: CPU and Hard disk D: None of these

(b) Define the following terms in brief. [10]
1. Arithmetic shift
2. Asynchronous data transfer
3. Parallel processing
4. Working of interface
5. Cache memory

Question: 2.

(a) What is pipelining? Explain instruction pipeline with example. [08]

(b) List and explain steps of communication flow between CPU – IOP. [08]

OR

(b) Define Associative memory? Explain its hardware organization in detail. [08]

Question: 3.

(a) What is an interrupt? Draw and explain interrupt cycle. [08]

(b) Convert the following expression into reverse polish notation by assuming A=6, B=2, C=3, D=3, E=6 (also mention stack operation) [04]

AB/C-DE*AC*-+

(c) Differentiate RISC and CISC. [04]

OR

(a) What is DMA? Draw block diagram of DMA controller and explain in detail. [08]

(b) Draw hardware organization for addition and subtraction of sign 2's complement number. [04]

(c) Differentiate isolated I/O and memory mapped I/O. [04]

Question: 4.

(a) Write a short note on various method of implementing priority interrupt. [08]

(b) Demonstrate advantages of virtual memory over cache memory. [04]

(c) Demonstrate various steps to perform address sequencing process in micro-program. [04]

OR

(a) What do you mean by mode of transfer? Explain any two technique in detail. [08]

(b) Enlist detail of below instruction: [04]
CLA, INC, LDA, CME.

(c) Sketch circuit of multiplication to perform 2 bit by 2 bit array multiplier. [04]

Question: 5.

(a) Draw and explain Tri/Three state bus buffer. [08]

(b) Experiment timing and control signal for particular example. [04]

(c) Explain three and two address instruction with an example. [04]

OR

(a) Draw and explain general register organization in detail. [08]

(b) Test space time diagram for four segment pipeline showing the time taken by six task. [04]

(c) Define locality of reference. Calculate effective access time (EAT) for below given data.
TC: 45ns
TM: 55ns
H: 72%
EAT: ? [04]

Question: 6.

a) Solve multiplication of (15) with (13) using Booth's algorithm. Give each step. [08]

b) Differentiate SIMD and MIMD. [04]

c) Justify which organization is better among hardwire and micro programmed control unit. [04]

OR

a) Show content of register E, A, Q and SC during the process of division of two number 01110 (dividend) and 10001 (divisor). [08]

b) Enlist various types of addressing mode. Explain any two in brief. [04]

c) Draw circuit of Binary adder. [04]

---Best of luck---

Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age	
		% of weight -age	Que. No.
1	Remember/Knowledge	26	1(b), 5(a), 6(b), 2(b)
2	Understand	38	1(a), 2(a), 3(a), 4(a), 6(c)
3	Apply	20	3(b), 4(b), 4(C), 6(a)
4	Analyze	12	3(c),5(b), 4(c)
5	Evaluate	4	5(c)
6	Higher order Thinking	----	-----