Enroll. No._____

MARWADI UNIVERSITY

Faculty of Technology

Information and Communication Technology

B.Tech **SEM: III** **WINTER:2018**

Subject: - Computer Organization and Architecture (01CT0301) **Date: - 20/10/2018**
Total Marks:-100 **Time: - 03:00 hours**

Instructions:

1. **All Questions are Compulsory.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Question: 1. Do As Directed:

(a) Multiple Choice Questions: [10]

1. $(24)_{16} = (\_\_\_\_\_)_2$
   a. 11001111
   b. 10101010
   c. 00101000
   d. 00100100

2. $(010110)_2 = (\_\_\_\_\_)_8$
   a. 32
   b. 47
   c. 26
   d. 27

3. The size of Temporary Register is _____ bits.
   a. 12
   b. 16
   c. 20
   d. 8

4. The instruction CLE _____ the E bit.
   a. Sets
   b. Clears
   c. Flips
   d. Resets

5. Which of the following is a branch instruction?
   a. ISZ
   b. CLE
   c. INC
   d. BSA

6. The size of Data Register is _____ bits.
   a. 12
   b. 16
   c. 20
   d. 8

7. The size of Instruction Register is _____ bits.
   a. 12
   b. 16
   c. 20
   d. 8

8. The carry if generated by addition of two numbers is stored in ___ bit.
   a. E
   b. F
   c. G
   d. A

9. The size of Address Register is _____ bits.
   a. 12
   b. 16
   c. 20
   d. 8

10. The size of Accumulator is _____ bits.
    a. 12
    b. 16
    c. 20
    d. 8

(a) Answer the following questions in one sentence: [10]

1. What is meant by Computer Architecture?
2. Define Accumulator.
3. Define Micro-Instruction
4. What is the use of E bit with reference to basic computer architecture?
5. What is meant by an Accumulator?
6. What is meant by compiler?
7. Write the functionality of Program Register for Basic Computer Architecture.
8. Define Assembler.
9. Write the functionality of Instruction Register for Basic Computer Architecture.
10. Write the functionality of Input Register for Basic Computer Architecture.

Question: 2. Answer the Following Questions:

(a) Explain hardware Implementation of common bus system along with a neat sketch of the bus architecture. [08]

(b) Explain different types of micro-operations in basic computer architecture. [08]

OR

(b) What is meant by Stack? Explain push and pop operations on register stack giving suitable examples. [08]

Question: 3. Answer the Following Questions:

(a) Write a detailed note on instruction cycle with neat diagrams and flowchart. [08]

(b) Explain whether the following microoperations can be executed or not? If no, Write the correct sequence of microoperations: [04]

(i) IR ← M[PC]

(ii) AC ← AC+TR

(c) Explain the following micro-operations: [04]
(i) AC ← AC ⊕ DR, SC ← 0
(ii) BUS ← R1, R2 ← BUS

OR

(a) Discuss four-segment instruction pipeline with diagram(s). [08]

(b) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input. [04]

$$XYT_0 + T_1 + YT_2 : AR \leftarrow AR + 1$$

(c) Explain the meaning of following instructions based on the basic computer assembly programming: [04]
(i) ISZ Q
(ii) BUN Q

Question: 4. Answer the Following Questions:

(a) Explain pipelining hazards giving examples [08]

(b) Explain the meaning of parallel processing. State two advantages of parallel processing. [04]

(c) Write an assembly language program to flip/toggle all the bits stored at location 500. [04]

OR

(a) Explain zero, one, two and three address instructions. [08]

(b) List and explain the two major types of addressing modes with reference to the Basic Computer Architecture along with necessary diagrams. [04]

(c) Write an assembly language program that sets all the bits to 1, for the data stored at location 500 and resets all the bits to 0, for the data stored at location 600. [04]

Question: 5. Answer the Following Questions:

(a) Write a brief note on sub-routine call and return instructions with an assembly program explaining them. [08]

(b) For the given C code, write the assembly language program: [04]

```
int a,b,c;
a=  22 ;
b= - 48;
c= a+b;
```

Let the locations for the variables a, b and c be 400, 500 and 600 respectively.

(c) Write 4 points of characteristics each for RISC and CISC computer processors. [04]

OR

(a) Explain FLYNN'S classification in detail. [08]

(b) A non-pipeline system takes 57 ns to process a task. The same task can be processed in a six-segment pipeline each with a clock cycle of 12 ns. [04]
1. Determine the speedup ratio of the pipeline for 110 tasks.
2. What is the maximum speedup that can be achieved in the above case? Justify your answer.

(c) Give two points of advantages and disadvantages of pipelining system over conventional system. Give an example that shows "pipelining system is more beneficial than the conventional system." [04]

Question: 6. Answer the Following Questions:

(a) What is meant by the masking procedure over the data? Explain its importance. Write a program to unpack two characters from location WRD and store them in bits 0 through 7 of locations CH 1 and CH2. Bits 9 through 15 should contain zeros. [08]

(b) Write a program loop, using a pointer and a counter, that flips the values of the contents Stored at locations 500 through 5FF. [04]

(c) Write an assembly code to add 50 numbers and store it back to any memory location i.e. Sum = $n_1 + n_2 + n_3 + \ldots\ldots\ldots\ldots + n_{49} + n_{50}$. [04]

OR

(a) Write a program to evaluate the following arithmetic statement [08]

$$X= [A * (B + C) –D] / (E + F -G)$$

(i) using a general register computer with three-address instructions,
(ii) using an accumulator type computer with one-address instructions,
(iii) using a stack organized computer with zero

(b) Write an assembly code to perform the XORing between two numbers and store into another variable i.e. $Z = X \oplus Y$. [04]

(c) Write a subroutine that accepts a number from the user and determine whether it is a positive, negative or zero number. [04]

---Best of Luck---

Que. Paper weight-age as per Bloom's Taxonomy

No.	Que. Level	% of weight-age	
		% of weight -age	Que. No.
1	Remember/Knowledge	24	Q.1 (a,b), Q.2 (a,b OR b)
2	Understand	28	Q.3(a OR a), Q.4(a OR a), Q.5 (a OR a)
3	Apply	19	Q.3 (b,c OR b,c), Q.4 (b OR b), Q.5 (c OR b)
4	Analyze	9	Q.4 (c OR c), Q.5 (c OR b)
5	Evaluate	20	Q.6 (a,b,c OR a,b,c)
6	Higher order Thinking	--	--

GRAPH: