Marwadi University	Marwadi University Faculty of Technology Department of Information and Communication Technology	
Subject: Analog and Digital Communication (01CT0404)	Aim:Transmit and receive digital signal using Quadrature Phase Shift Keying.	
Experiment No: 10	Date:	Enrolment No: 92200133030

Aim:

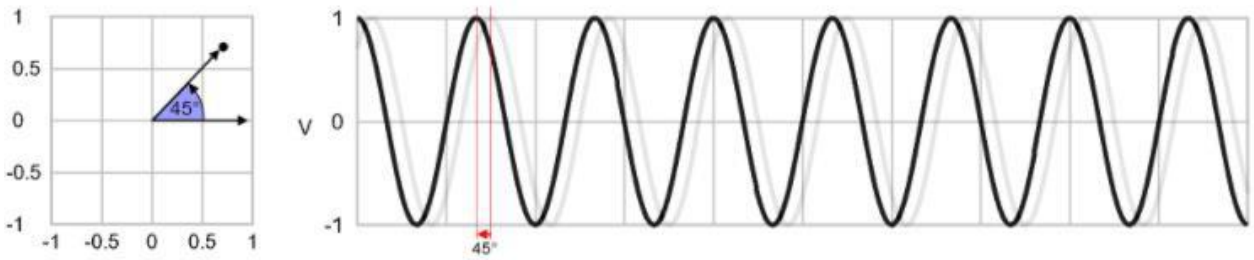
Transmit and receive digital signal using Quadrature Phase Shift Keying.

Apparatus: Scientech ST2153,2154,2156 and 2157, Connecting Wires, DSO, Probes

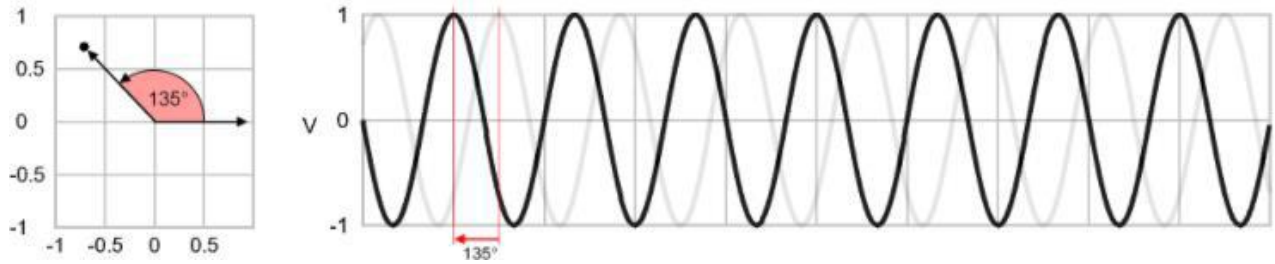
Theory:

Phase Shift Keying is a modulation technique where we change the phase of the carrier signal to show the relativeness with modulating signal. Basically, PSK is of BPSK that is Binary Phase Shift Keying. Here, generally 2 phases is used for the variance. QPSK that is Quadrature Phase Shift Keying is a modulation technique where multiple phases are used to show relative change. To transmit information QPSK modulator varies the signal's phase. Some Equations and Plots.

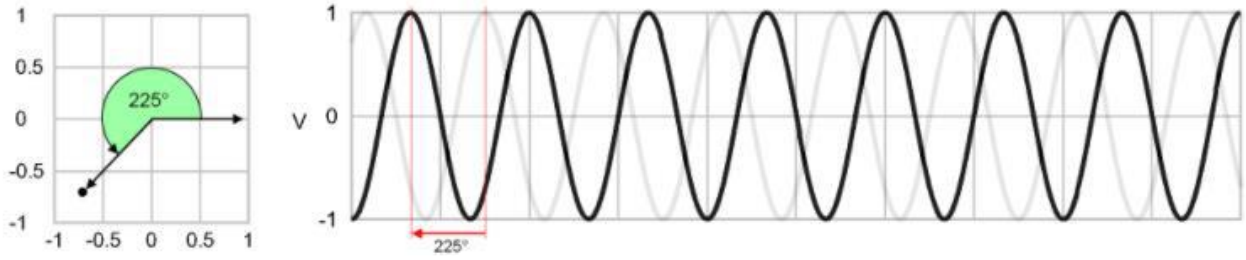
1. 00 bit: Equation: Ecmax Cos(wct+45˚) 2. →01 bit: Equation: Ecmax Cos(wct+135˚)



2. 01 bit: Equation: Ecmax Cos(wct+135˚)

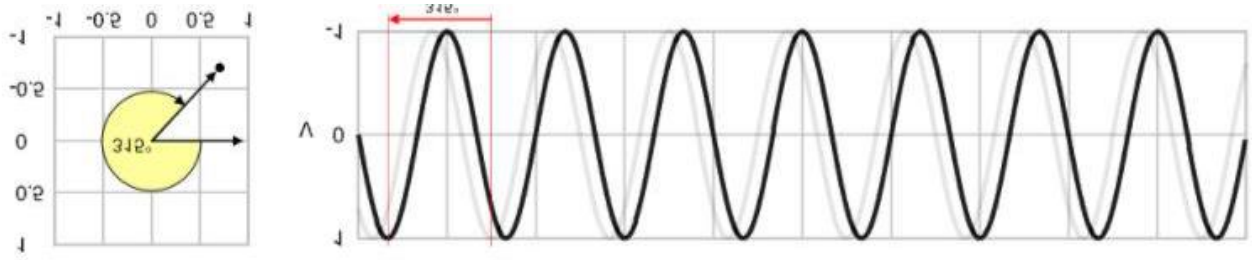


3. 10 bit: Equation: Ecmax Cos(wct+225˚) 4. →11 bit: Equation: Ecmax Cos(wct+315˚)

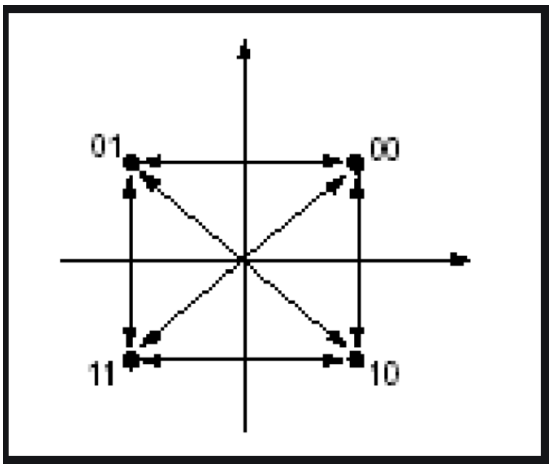


4. 11 bit: Equation: Ecmax Cos(wct+315˚)

Marwadi University	**Marwadi University** **Faculty of Technology** **Department of Information and Communication Technology**	
Subject: Analog and Digital Communication (01CT0404)	**Aim:Transmit and receive digital signal using Quadrature Phase Shift Keying.**	
Experiment No: 10	**Date:**	**Enrolment No: 92200133030**



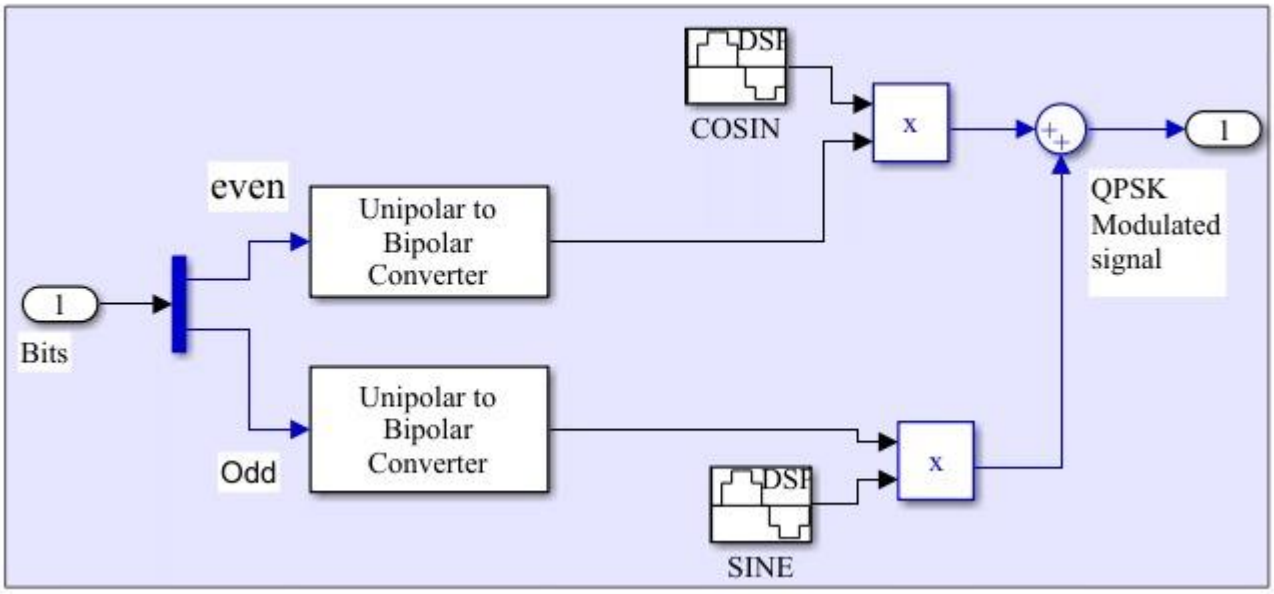
PHASOR DIAGRAM FOR QPSK:



Block Diagram:

Marwadi University	Marwadi University Faculty of Technology Department of Information and Communication Technology	
Subject: Analog and Digital Communication (01CT0404)	Aim:Transmit and receive digital signal using Quadrature Phase Shift Keying.	
Experiment No: 10	Date:	Enrolment No: 92200133030

Simulink Diagram:



Procedure:

Steps (1) to (13) : Follow the set up procedure for steps 1 to 13 as given in experiment 10, Also Set pulse generator delay adjust fully clock wise in step 6.

1. Make the additional connections as shown in figure 44 as shown in following steps.
   a. On ST2156 trainer :
      i) Differentially encoded dibit MSB (TP10) to unipolar bipolar converter 1 input (TP20)
      ii) Unipolar-Bipolar converter 1 output (TP21) to modulator 1 input (TP27).
      iii) Differentially encoded dibit LSB (TP11) to unipolar -bipolar 2 input (TP23).
      iv) Unipolar-Bipolar converter 2 output (TP24 to modulator 2 input (TP30).
      v) 960KHz (1) output (TP17) to modulator 1 carrier input (TP26).
      vi) 960KHz (Q) output (TP18) to modulator 2 carrier input (TP29)
      vii) Modulator 1 output (TP28) to summing amplifier's input A (TP34).
      viii) Modulator 2 output (TP31) to summing amplifier's input B (TP35).
   b. Between ST2156 & ST2157 :
      i) Summing amplifier's output (TP36) to QPSK demodulator input (TP1).
   c. On ST2157 trainer :
      i) QPSK demodulator output 1 (TP8) to low pass filter 1 input (TP23).
      ii) QPSK demodulator's Q output (TP9) to low pass filter 2 input (TP23).
      iii) Low pass filter 1 output (TP24) to comparator 1 input (TP46).

iv) Low pass filter 2 output (TP28) to comparator 2 input (TP49).

v) Data squaring circuit comparator 1 output (TP47) to differential decoder MSB input (TP42).

vi) Data squaring circuit comparator 2 output (TP50) to differential decoder LSB input (TP43).

d. Between ST2157 & ST2154 Trainers :

i) Comparator 1 output (TP47) to clock regeneration circuit input (TP3).

ii) Dibit decoder output (TP47) to PCM data input (TP3)

iii) Dibit decoder clock input (TP41) to clock regeneration circuit output (TP8).

e. On ST2154 trainer :

i) Clock regeneration circuit output (TP8) to RX clock input (TP46).

2. Monitor the output of modulator 1 (TP28) in ST2156 trainer. Adjust the scope's trigger level manually to obtain a stable display Use the controls provided in the modulator as shown in followings steps.

a. Gain : This controls the overall amplitude of the modulated waveform. Adjust it till you obtain a 2VPP signal.

b. Modulation off set : This controls the peak to peak amplitude of the 0 & 180 phases, relative to each other. Adjust this pot such that the amplitudes of the two phases are equal.

3. Make the same adjustments for modulator 2's output (TP31) by monitoring its outputs on the oscilloscope.

4. Monitor the output of the summing amplifier (TP36). The output is a QPSK Signal with 0, 90, 180 & 270 phase shifts clearly visible.

5. To observe the QPSK demodulation process, monitor each output (TP8 & 9) of the QPSK demodulator with reference to input signal (TP1) on ST2157. Also monitor the test points provided at various block outputs, to understand the process of demodulation clearly.

6. Observe the two low pass filter's outputs (TP24 & 28). Adjust the phase adjust control provided on QPSK demodulator block until you obtain two levels only at low pass filter's outputs. The incorrect placement of phase adjust control produces multilevel output at filter output.

1. Monitor both the comparator's output (TP47 & 50). Adjust the bias level control of both comparators till their output doesn't have the correct pulse width.
    a. Now that the filter's output is balanced around 0Volts. Adjustment of bias level to produce 0V terminal of the comparator help achieving 'Squared up' version of the filter's output signal. This can be compared by simultaneously displaying the filter's output & the comparator's output on the oscilloscope.
2. Temporarily disconnect & then reconnect the QPSK input to the QPSK demodulator. Observe that after some trial you will obtain four different combinations at comparator's outputs (TP47 & 50). This explains the phase ambiguity in QPSK system.

Marwadi University	**Marwadi University** **Faculty of Technology** **Department of Information and Communication Technology**	
Subject: Analog and Digital Communication (01CT0404)	**Aim:Transmit and receive digital signal using Quadrature Phase Shift Keying.**	
Experiment No: 10	**Date:**	**Enrolment No: 92200133030**

3. To resolve the phase ambiguity problem the outputs from the comparators (TP47 & 50) are fed to the two inputs (TP42 & 43) of the differential dibit decoder which is driven by the regenerated clock from the ST2154 trainer. It is synchronized to the rising edge of the signal at output of ST2157 trainer's comparator 1.
   a. On observing the differential dibit decoder's output (TP44) along with the NRZ (L) waveform (TP5) on the other channel you will notice that the output is nothing but the delayed NRZ (L) waveform.
   b. Try disconnecting & reconnecting the QPSK modulation output for a short period. Notice that this time the decoders output is unchanged. This is become the Differential decoder looks for the change in tap bit code rather than the absolute value. Thus, the phase ambiguity problem is solved.
4. Turn 'On' the ST2153 pseudo-random sync code generator. The transmitter & receiver one locked in 'frame synchronization'. This can be checked by verifying that A/D converter LEDs on ST2154 & trainer now carry the same data. Try varying the DC input to the ST2153 trainer. The ST2154 trainer should follow the changes.
5. Turn 'Off' the trainers. Discount the CH0 & CH1 inputs of ST2153 trainer. Connect CH0 input to ~2 KHz signal.

6. Turn 'On' the trainers. Observe the CH0 & CH1 outputs (TP33 & 36) at ST2154 trainers. The output should be identical to the input signal fed to each channel. The notice that the two signals are independent of each other & verification of one do not affect the other. If some interference is present it can be removed by varying the phase generator delay adjust control on ST2154 trainer.

Step-5

Design Simulink model for QPSK and observe signals and constellation diagram.

Conclusion:

Marwadi University	**Marwadi University** **Faculty of Technology** **Department of Information and Communication Technology**	
Subject: Analog and Digital Communication (01CT0404)	**Aim:Transmit and receive digital signal using Quadrature Phase Shift Keying.**	
Experiment No: 10	**Date:**	**Enrolment No: 92200133030**

Post Lab Exercise:

1. List applications of QPSK.
2. Write equation for BER and sketch BER performance curve for QPSK.
3. Draw QPSK modulator and demodulator block diagram.