

Name:- Abhinav Kaulhik
Roll No:- 2100290110003
Batch:- A-1

Flip-Flop

It is a device which stores a single bit of data.

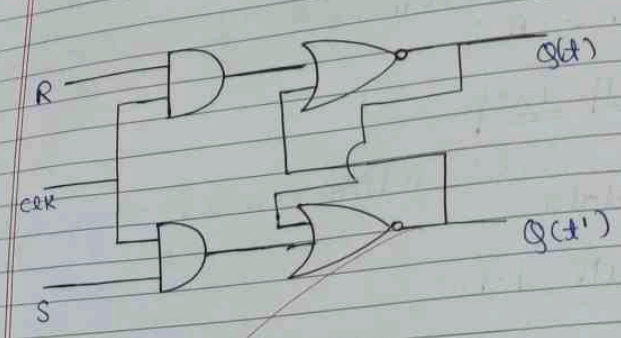
Truth Table

S	R	Q _{in}	Q _{out}
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

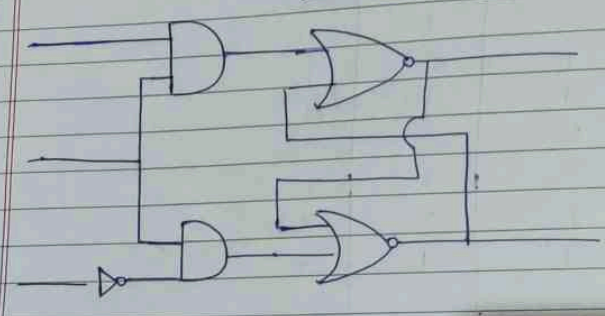
Circuit Diagram



of evaluation of



D-Type



Name:- Abhinav Kaushik

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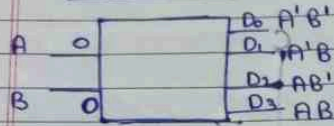
Abhinav Kaushik

2100290110003

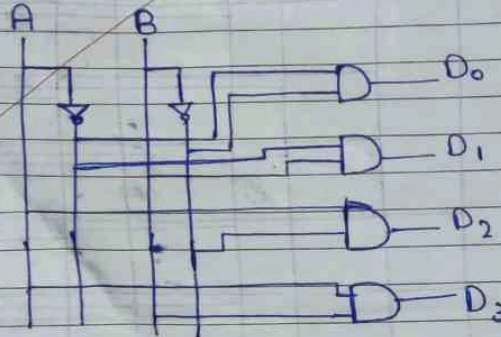
Batch A1

2X4 and 3X8 Decoder

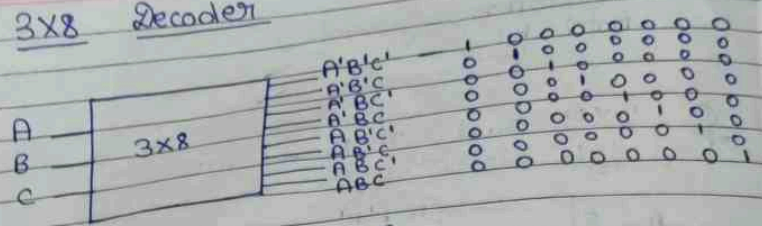
2X4 Decoder



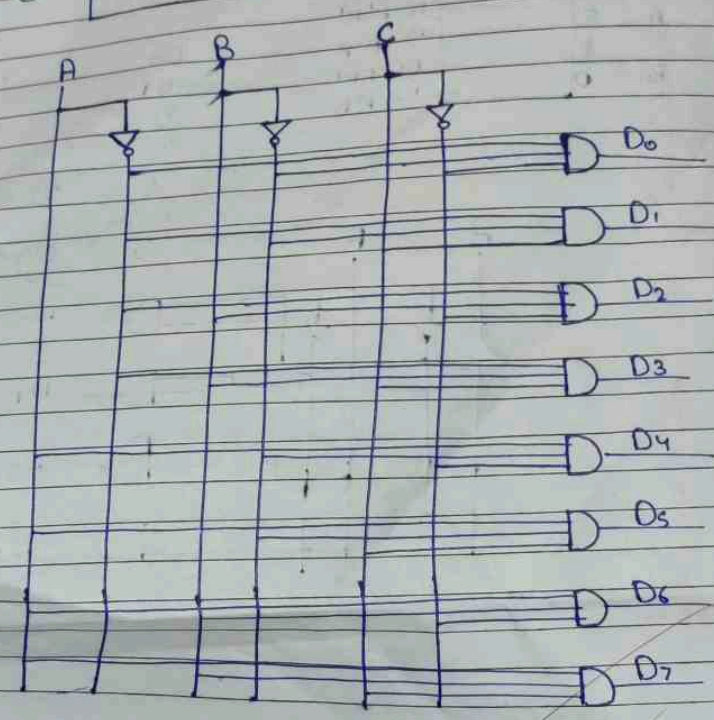
	00	01	10	11
0	0	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1



3x8 Decoder



000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000
000	000	000	000	000	000	000	000

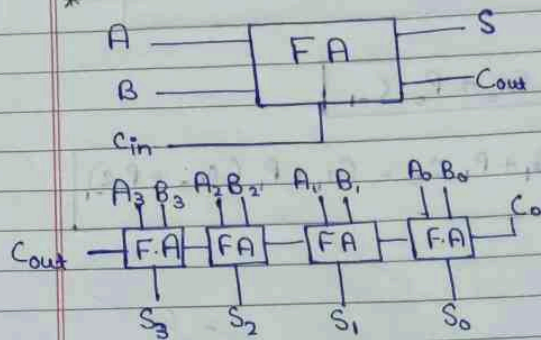


→ Abhinav Kaushik
 → 2100290110003
 → A

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Adder

CARRY LOOK-AHEAD - ADDER *



$A = A_3 \ A_2 \ A_1 \ A_0$
 $B = B_3 \ B_2 \ B_1 \ B_0$
 $C_{out} \ S_3 \ S_2 \ S_1 \ S_0$

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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Page No.

$$C_i = A_i B_i + (A_i \oplus B_i) C_{i-1}$$

$$C_0 = G_0 + P_0 \cdot C_{-1}$$

$$C_1 = G_1 + P_1 \cdot C_0 = G_1 + P_1 (G_0 + P_0 C_{-1})$$

3. NOT gate

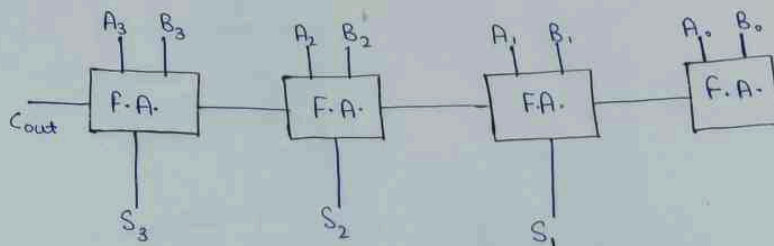
Name:- Abhinav Kaushik

Roll. No:- 2100290110003

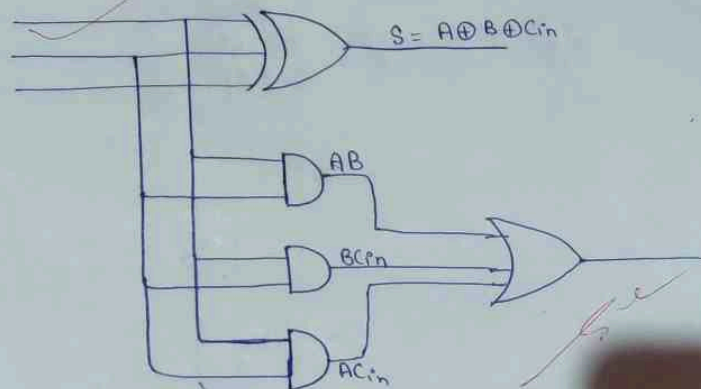
Batch:- A-1

Experiment:- 4-bit binary Adder/subtractor.

$$\begin{array}{r} A = A_3 \ A_2 \ A_1 \ A_0 \\ B = B_3 \ B_2 \ B_1 \ B_0 \\ \hline \text{Cout} \ S_2 \ S_1 \ S_0 \end{array}$$



4-bit binary Adder



Full Adder

3. NOT gate

The logic gate that inverts the input.

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Roll No :- 2100230110003

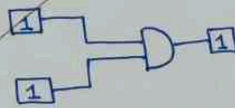
Group :- A1

1. AND Gate

The logic And gate is a type of logic gate whose output goes high to a logic level 1 only when all of its inputs are high.

Truth Table

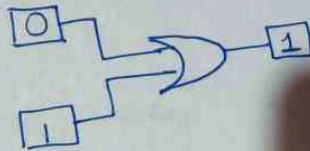
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



2. OR Gate

It is a logic gate in which if both inputs are high then output is high, if either inputs are high output is high if both inputs are low output is low.

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1



3.) NOT gate

The logic gate that inverts the input on

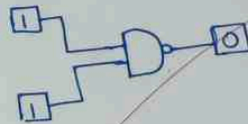
A	\bar{A}
0	1
1	0



4.) NAND Gate

A logic gate which produces an output which is false only if all its input are true.

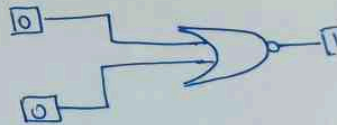
A	B	$(A \cdot B)'$
0	0	1
0	1	1
1	0	1
1	1	0



5.) NOR Gate

A logic gate that provides high output if both inputs are low or either inputs are low and high if both inputs are then it gives low output.

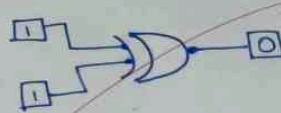
A	B	$(A+B)'$
0	0	1
0	1	0
1	0	0
1	1	0



⑥ XOR Gate

A logic gate that gives a true output when the number of true input is odd.

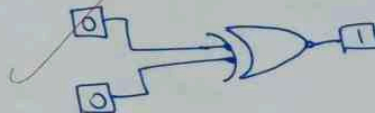
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



⑦ XNOR Gate

A logic gate that gives true output when the no. of inputs are even.

A	B	$(A \oplus B)'$
0	0	1
0	1	0
1	0	0
1	1	1



ASSIGNMENT-2

* Abhinav

Page No:
 Date:

Name:- Abhinav Kauthik

Roll No:- 2100290110003

Group:- A-1

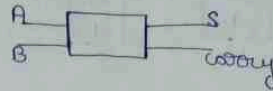
Experiment:- Study and verify the half adder and full adder.

Half adder: An electronic device that performs addition of numbers; It is able to add two single digit binary numbers.

Truth Table:-

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Symbol:-



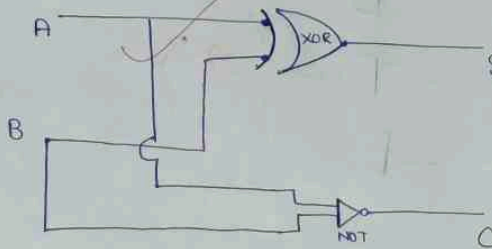
A	B	C
A'	B'	0
A	B	1

$$C = AB$$

Circuit diagram

A	B	S
A'	B'	0
A	B	1

$$S = A'B + AB' \\ = A \oplus B$$



Full adder

It consists two XOR gates, two AND gates and one OR gate. It adds three inputs and produce two outputs.

ASSIGNMENT-2
UNIT-2

* Abhinav Kaur
* 2100000000000000

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Truth Table

A	B	C _{in}	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A \ B C _{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

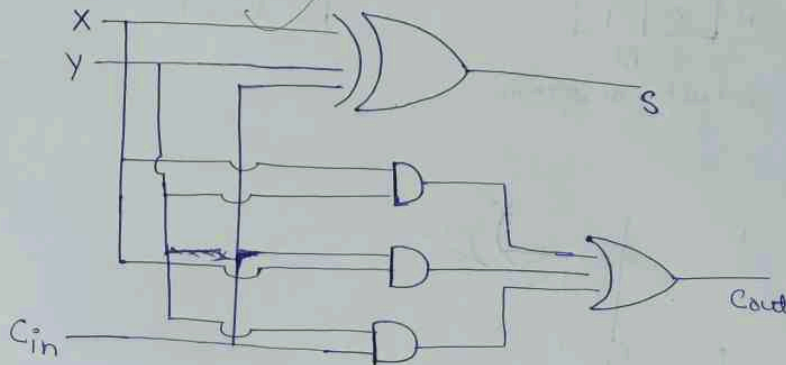
$$C_{out} = BC_{in} + AC_{in} + AB$$

A \ B C _{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$S = A'BC_{in} + A'BC'_{in} + AB'C_{in} + ABC_{in}$$

$$S = A \oplus B \oplus C$$

Circuit Diagram



Abhinav Kaur
210029000003
Batch AI

2*2 Binary multiplier

$$\begin{array}{r} A = A_1 A_0 \\ B = B_1 B_0 \\ \hline A_1 B_1 \quad A_1 B_0 \\ P_2 \quad P_1 \quad P_0 \end{array}$$

