TEAM MAVERICKS

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COMMNET PROBLEM STATEMENT 1

Problem Statement :

We are required to design a two stage miller-compensated op-amp with a capacitive load.A typical two stage op-amp looks like:

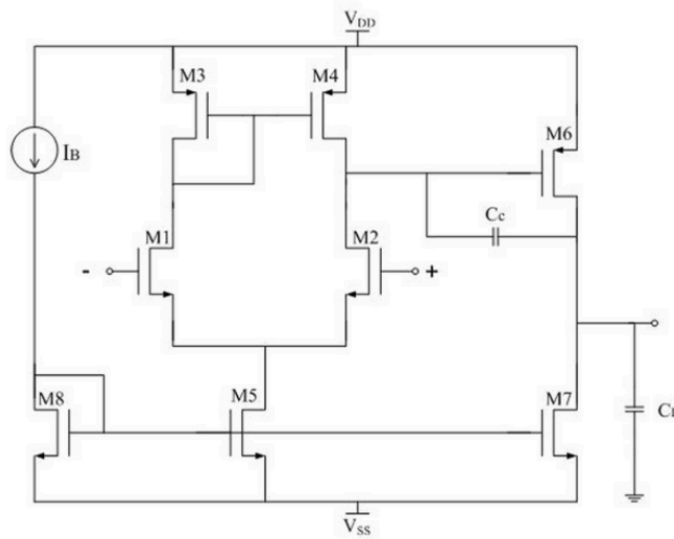


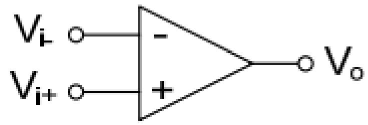
Figure 1: NMOS Two Stage op amp

Specifications	Value
DC Gain	2000
Input Common Mode Range	0.7 V to 1.6 V
Phase margin	> 60 degrees
Capacitive load (C_L)	5 pF
Gain-bandwidth (GBW) product	50 MHz

V_{th}(for nmos) = 0.7 ± 0.15V, λ = 0.04 and U_nC_{ox} = 100 uA/V^2 ± 10%
V_{th}(for pmos) = -0.7 ± 0.15, λ = 0.05, U_pC_{ox} = 50 uA/V^2 ± 10 %

Introduction to Two Stage OpAmp :

Operational amplifiers (opamp) are essential components of analog system design. Integrated circuit design, as well as board level design, often uses operational amplifiers. This component is basically a high gain voltage amplifier used in many analog systems such as filters, regulators and function generators. This rudimentary device is also used to create buffers, logarithmic amplifiers and instrumentation amplifiers. Op Amps can also function as simple comparators. Knowledge of operational amplifier functionality and design is important in analog design.



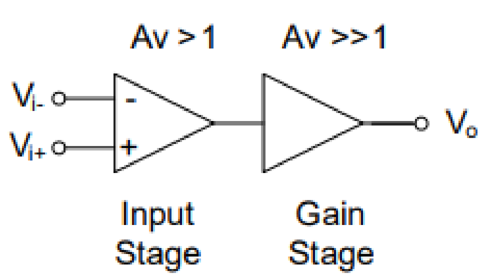
The operational amplifier functions as a voltage amplifier. The relationship between the input and output voltage is given by:

$$V_o^+ = A_{vo}\,(V_i^+ - V_i^-)$$

The simplest operational amplifier is the simple differential amplifier studied earlier. This amplifier can be improved by adding a second stage as an inverting amplifier with a current source load. The two stage amplifier shown in Figure 1(on pg no. 1) is referred to as a Miller compensated Opamp.

There was a need for two-stage operational amplifiers because they can provide high gain and high output swing in comparison to single Op Amp.

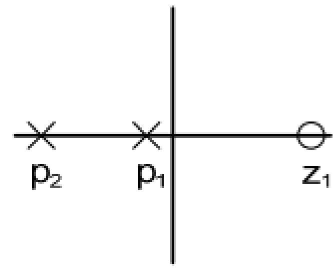
The two-stage amplifier can be modeled as a cascade of two amplifiers, as illustrated in Figure 8-4. The first stage is a differential amplifier, which produces an amplified version of the difference in input signals. This stage determines the CMRR, slew rate and other performance specifications determined by the differential amplifier. The second stage is an inverting amplifier. The purpose of this stage is to provide a large voltage gain. The gain stage and the input stage create two poles, which affect the stability of the feedback system. Usually some form of compensation is required to assure the amplifier is stable at unity gain. The technique used here is called Miller Compensation. Additional gain stages can be employed to increase the gain, but this degrades stability and requires complex compensation techniques.



What is Miller Compensation :

Miller compensation is a technique for stabilizing op-amps by means of a capacitance *Cf* connected in *negative-feedback fashion* across one of the *internal gain stages*, typically the second stage.

The addition of the compensation capacitor C_C caused the poles to split. One pole moved closer to the origin, while the other pole moved away from the origin .This compensation technique is called "pole splitting". The pole-zero plot of this transfer function is illustrated in Figure 8-8.



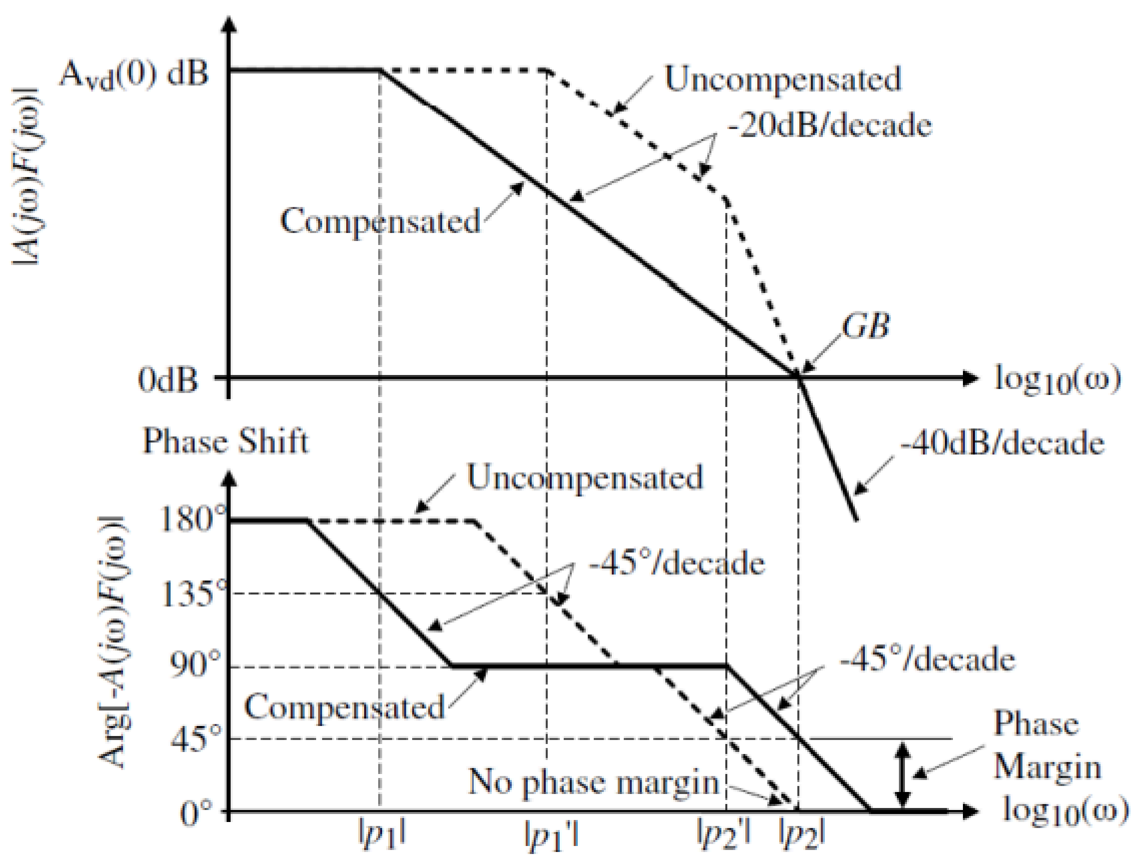
Important formulas :

GBW = gm_1 / C_C

p_1 = 1 / (gm_2 ✖ R_1 ✖ R_2 ✖ C_C)

p_2 = gm_2 / C_L

Zero = gm_2 / C_C



Design Procedure (Using Miller Compensation) :

Step 1 :

- Evaluation of C_c from C_L To obtain a phase margin of 60° , it is required that the compensating capacitor C_c satisfy this following condition, i.e

$$C_c \geq 0.22 \times C_L$$

Step 2 :

- Evaluation of Io from slew rate The slew rate of 2-stage Miller compensated OTA is given by,

$$I_{D5} = SR \times C_c$$

Step 3 :

- Evaluation of $(w/l)_{3,4}$

$$(w/l)_{3,4} = I_{D5} / (U_p C_{ox} \times (V_{dd} - |V_{th3(max)}| - V_{in(max)} + V_{th1(min)})^2)$$

Step 4 :

- Evaluation of gm_1 We have,

$$gm_1 = GBW \times 2\pi \times C_c$$

- Now Evaluation of $(w/l)_{1,2}$

$$(w/l)_{1,2} = (gm_1)^2 /(U_n C_{ox} \times I_{D5})$$

Step 5 :

- Calculation of $V_{D5(sat)}$

$$V_{D5(sat)} = V_{in(min)} - V_{ss} - V_{th1(max)} - \sqrt{}(I_{D5} / (U_n C_{ox} \times (w/l)_{1,2}))$$

- Evaluation of $(w/l)_5$

$$(w/l)_5 = (2 \times I_{D5}) / (U_n C_{ox} \times V_{D5(sat)}{}^2)$$

$(w/l)_5 = (w/l)_8$; Since they form a current mirror circuit

Step 6 :

- Evaluation of gm_6

$$gm_6 \geq 10 \times gm_1$$

Select gm_6 from here then,

- Evaluation of gm_4

$$gm_4 = \sqrt{}(I_{D5} \times U_p C_{ox} \times (w/l)_{3,4})$$

- Evaluation of $(w/l)_6$

$$(w/l)_6 = (w/l)_{3,4} \times (gm_6 / gm_4)$$

Step 7 :

- Evaluation of I_{D6}

$$I_{D6} = (gm_6)^2 /(2 \times U_p C_{ox} \times (w/l)_6)$$

$$I_{D7} = I_{D6}$$

Step 8 :

- Evaluation of $(w/l)_7$

$$(w/l)_7 = (w/l)_5 \times (I_{D7} / I_{D5})$$

Code for parameter calculations :

```cpp
commnet.cpp > main()
#include<bits/stdc++.h>
using namespace std;
int main(){
    float icmrpos,icmrneg,vdd,vss;
    // cout<<"enter vdd"<<endl;
    cin>>vdd;
    // cout<<"enter vss"<<endl;
    cin>>vss;
    float sr;
    // cout<<"enter sr"<<endl;
    cin>>sr;
    float cc;
    // cout<<"enter cc"<<endl;
    cin>>cc;
```

>>As it was tedious to calculate manually again and again so We have written, C++ code for calculating parameters by taking user input V_{dd}, V_{ss} , Slew Rate, and Cc.

```cpp
commnet.cpp > main()
int main(){
    if(cc>1.1){
        float id5=sr*cc;
        cout<<"id5 ="<<id5<<"micro"<<endl;
        float r3=(id5/(50*((vdd-1.9)*(vdd-1.9))));
        // int r4=r3;
        cout<<"r3 = "<<r3<<endl;
        // cout<<"r4 = "<<r4<<endl;
        float gm1=314.159*cc;
        cout<<"gm1 = "<<gm1<<" micro"<<endl;
        int r1=ceil((gm1*gm1)/(100*id5));
        cout<<"r1 = "<<r1<<endl;
        int r2=r1;
        float vd5sat=(-0.15-vss-sqrt(id5/(100*r1)));
        cout<<"vd5sat = "<<vd5sat<<endl;
        int r5=ceil((2*id5)/(100*vd5sat*vd5sat));
        cout<<"r5 = "<<r5<<endl;
        int gm6=ceil(10*gm1);
        cout<<"gm6 = "<<gm6<<"micro"<<endl;
        float gm4=sqrt(id5*50*r3);
        cout<<"gm4 = "<<gm4<<"micro"<<endl;
        int r6=ceil((r3*gm6)/(gm4));
        cout<<"r6 = "<<r6<<endl;
        float id6=(gm6*gm6)/(100*r6);
        cout<<"id6 = "<<id6<<"micro"<<endl;
        int r7=ceil((id6*r5)/id5);
        cout<<"r7 = "<<r7<<endl;
        float gain=(2*gm1*gm6)/(id5*id6*0.09*0.09);
```

>>Defining all parameters with given formulas and printing the calculated values .

```cpp
        cout<<"gain = "<<gain<<endl;
    }
    return 0;

}
```

>>Gain as Output

For input V_{dd} = 2.5v

V_{ss} = -1.5v

Slew Rate = 32 v/us

C_c = 1.4pf (i.e greater than 1.1pf as from step 1 as C_L is 5 pf)

Output from given code is:

```
Received Output:                Copy
id5 =44.8micro
r3 = 2.48889
gm1 = 439.823 micro
r1 = 44
vd5sat = 1.24909
r5 = 1
gm6 = 4399micro
gm4 = 74.6667micro
r6 = 147
id6 = 1316micro
r7 = 30
gain = 8102.94
```

I_{D5} = Drain current of M_5

$r_3 = (w/l)_{3,4}$

gm_1 = Transconductance of M_1

$r_1 = (w/l)_{1,2}$

$V_{D5(sat)}$ = Voltage required for M_5 to remain in saturation

$r_5 = (w/l)_{5,8}$

gm_6 = Transconductance of M_6

gm_4 = Transconductance of M_4

$r_6 = (w/l)_6$

I_{D6} = Drain current of M_6

$r_7 = (w/l)_7$

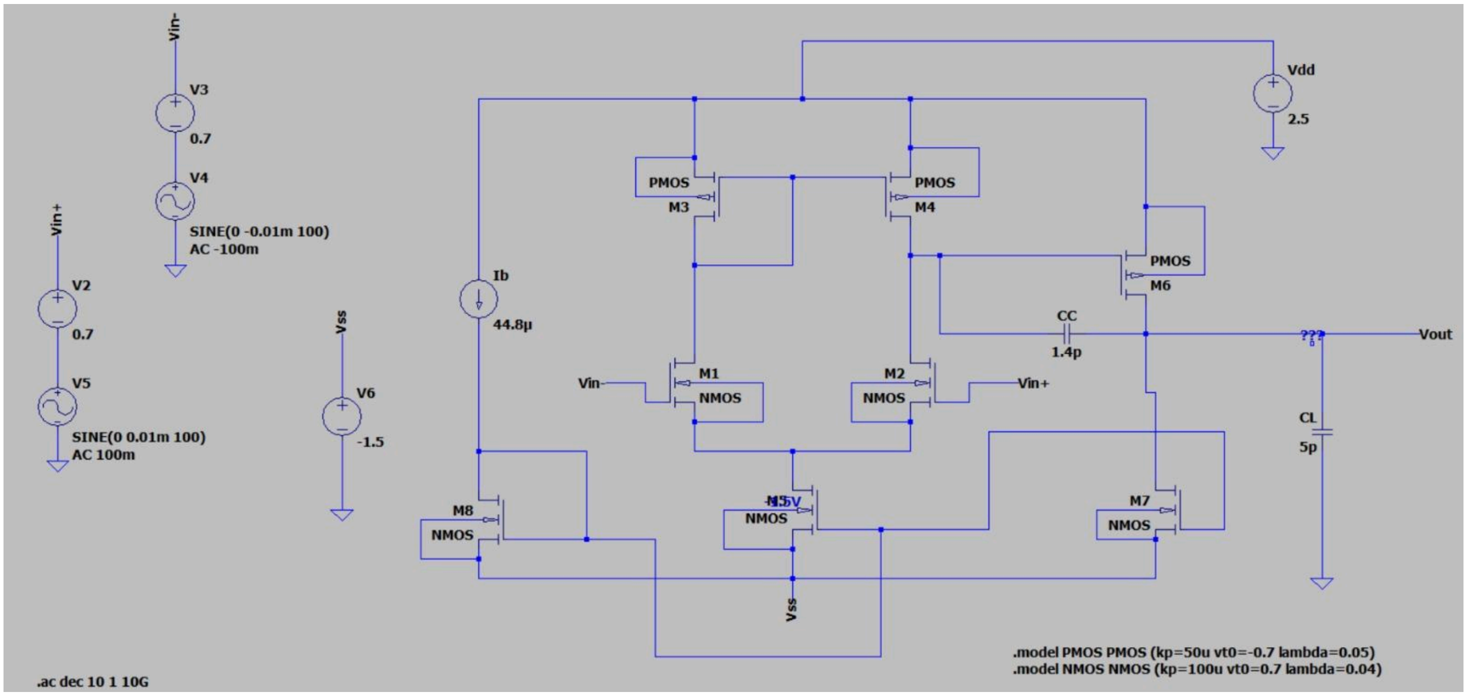
Gain = Calculated gain at particular frequency

Calculated Parameters:-

Specifications	Value	Width
$(w/l)_{1,2}$	44	22u
$(w/l)_{3,4}$	2.5	1245n
$(w/l)_{5,8}$	1	500n
$(w/l)_6$	147	73.5u
$(w/l)_7$	30	15u
I_{D5}	44.8 micro	
C_C	1.4 pf	

Value of L for all mosfets are taken as 500 nm and value of width is calculated accordingly.

Circuit Diagram (for output results) :



Result :

DC operating point :

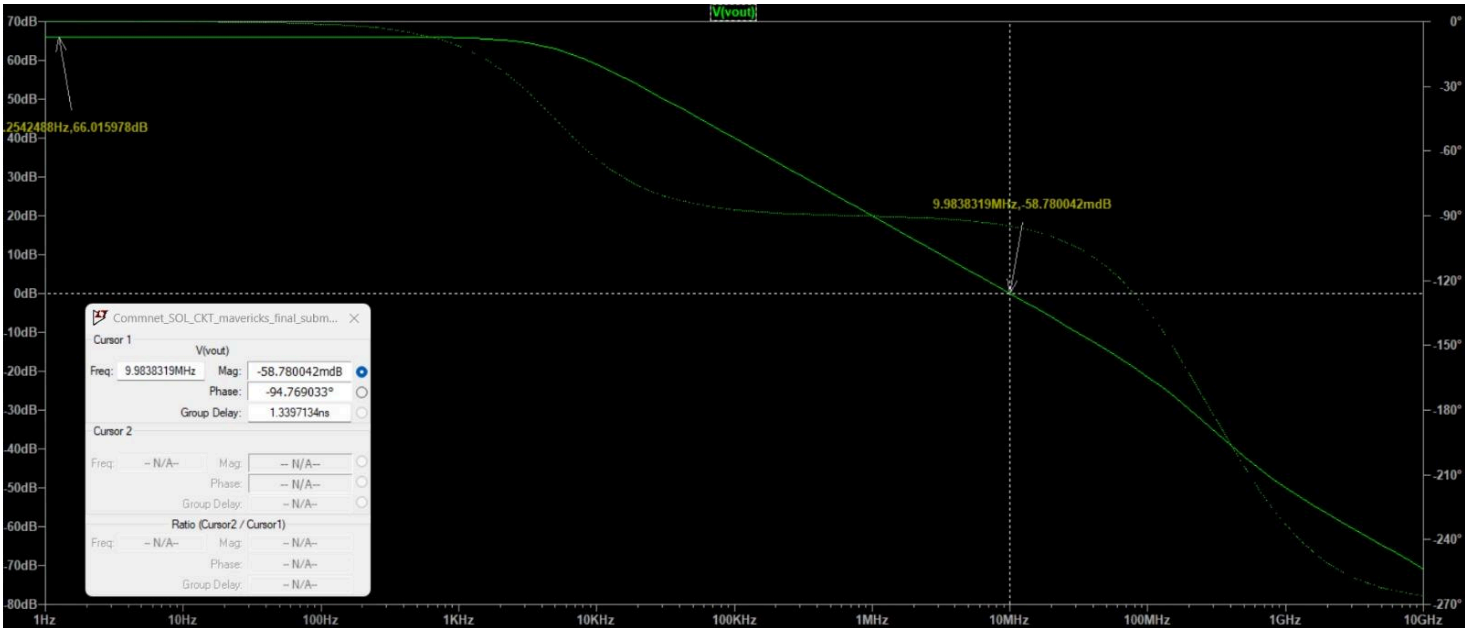
--- Operating Point ---

V(n001):	2.5	voltage
V(n007):	0.117364	voltage
V(vout):	0.436008	voltage
V(n004):	1.2208	voltage
V(vin+):	0.7	voltage
V(n005):	0	voltage
V(vin-):	0.7	voltage
V(n002):	0	voltage
V(n003):	1.2208	voltage
V(n006):	-0.0979459	voltage
V(vss):	-1.5	voltage
Id(M1):	2.22188e-05	device_current
Ig(M1):	0	device_current
Ib(M1):	-1.32875e-12	device_current
Is(M1):	-2.22188e-05	device_current
Id(M2):	2.22188e-05	device_current
Ig(M2):	0	device_current
Ib(M2):	-1.32875e-12	device_current
Is(M2):	-2.22188e-05	device_current
Id(M5):	4.44376e-05	device_current
Ig(M5):	0	device_current
Ib(M5):	-1.41205e-12	device_current
Is(M5):	-4.44376e-05	device_current
Id(M8):	4.48e-05	device_current
Ig(M8):	0	device_current

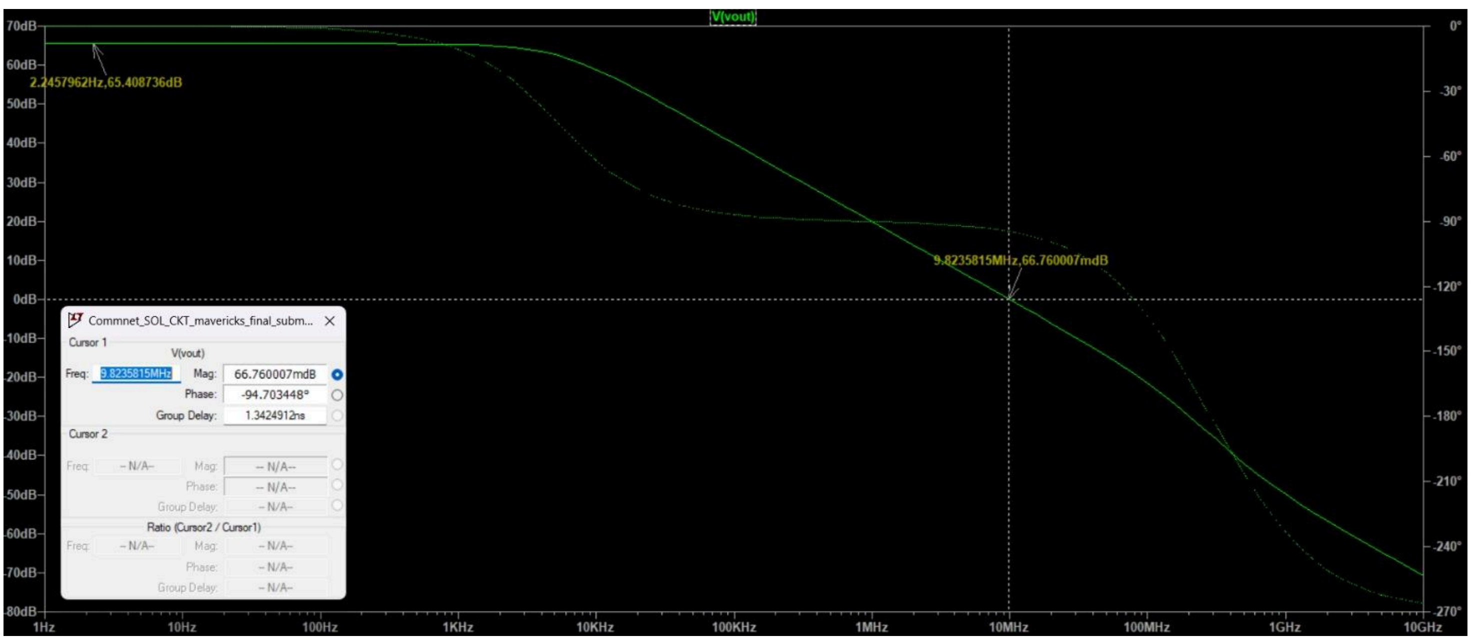
Ib(M5):	-1.41205e-12	device_current
Is(M5):	-4.44376e-05	device_current
Id(M8):	4.48e-05	device_current
Ig(M8):	0	device_current
Ib(M8):	-1.62736e-12	device_current
Is(M8):	-4.48e-05	device_current
Id(M7):	0.00136009	device_current
Ig(M7):	0	device_current
Ib(M7):	-1.94601e-12	device_current
Is(M7):	-0.00136009	device_current
Id(M4):	-2.22188e-05	device_current
Ig(M4):	-0	device_current
Ib(M4):	1.2892e-12	device_current
Is(M4):	2.22188e-05	device_current
Id(M6):	-0.00136009	device_current
Ig(M6):	-0	device_current
Ib(M6):	2.07399e-12	device_current
Is(M6):	0.00136009	device_current
Id(M3):	-2.22188e-05	device_current
Ig(M3):	-0	device_current
Ib(M3):	1.2892e-12	device_current
Is(M3):	2.22188e-05	device_current
I(Cc):	-1.09871e-24	device_current
I(Cl):	-2.18004e-24	device_current
I(Ib):	4.48e-05	device_current
I(Vdd):	-0.00144933	device_current
I(V2):	0	device_current
I(V3):	0	device_current
I(V4):	0	device_current
I(V5):	0	device_current
I(V6):	0.00144933	device_current

Bode plot :

At Input common dc voltage 0.7 Volts



At Input common dc voltage 1.6 Volts



Error :

Calculated Gain (at particular frequency) :- 78.17 dB

DC Gain (simulation):- 66.01 dB(for 0.7 volts) and 65.408 dB(for 1.6 volts)

Absolute Error = 12.16 dB (for 0.7 volts) and 12.762 dB(for 1.6 volts)

Specifications(LTSpice)	Value(At 0.7v)	Value(At 1.6v)
DC Gain	1997.56	1862.08
Phase Margin	85.23	85.297
Gain Bandwidth Product	9.98 MHz	9.82 MHz

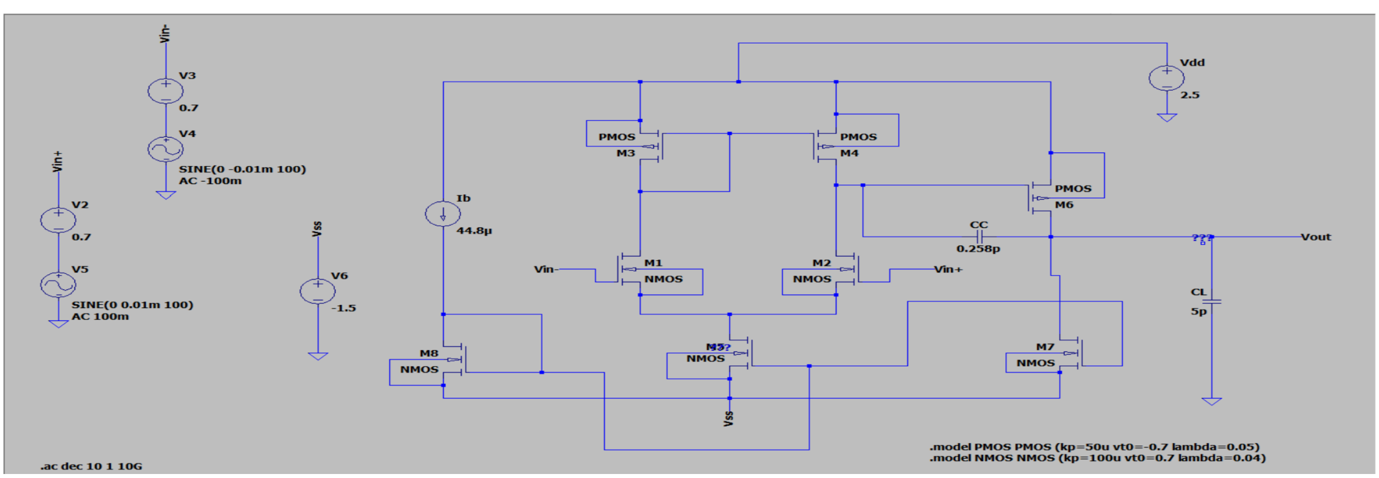
As we can clearly see that our gain bandwidth product is very far away from expected (50 Mhz). Hence we try to decrease C_C as our GBW product is inversely proportional to C_C (as seen from table below). But after repeated simulations and calculations we see that our gain bandwidth remains nearly 10 Mhz for decreasing C_C value to 1.2pf.
So now we further decrease it below 1.1pf to see the output results.
And after the simulation at somewhat lower values of C_C also we see that our phase margin is (>60°).
We have not increased the value of current I_5 because it will change our DC gain.
We have to compromise any value between Gain and Gain Bandwidth product as there is tradeoff between Gain and Gain Bandwidth product.The below circuit is realized only on the simulation basis.

Dependencies of device performance on various parameters

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap..
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase DC Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\downarrow$

Image source - Allen and Holberg - CMOS Analog Circuit Design

So now we decrease the value of C_c to 0.258pf



Result :

DC operating point :

```
       --- Operating Point ---

V(n001):        2.5             voltage
V(n007):        0.117364        voltage
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V(n004):        1.2208          voltage
V(vin+):        0.7             voltage
V(n005):        0               voltage
V(vin-):        0.7             voltage
V(n002):        0               voltage
V(n003):        1.2208          voltage
V(n006):        -0.0979459      voltage
V(vss):         -1.5            voltage
Id(M1):         2.22188e-05     device_current
Ig(M1):         0               device_current
Ib(M1):         -1.32875e-12    device_current
Is(M1):         -2.22188e-05    device_current
Id(M2):         2.22188e-05     device_current
Ig(M2):         0               device_current
Ib(M2):         -1.32875e-12    device_current
Is(M2):         -2.22188e-05    device_current
Id(M5):         4.44376e-05     device_current
Ig(M5):         0               device_current
Ib(M5):         -1.41205e-12    device_current
Is(M5):         -4.44376e-05    device_current
Id(M8):         4.48e-05        device_current
Ig(M8):         0               device_current
Ib(M8):         -1.62736e-12    device_current
Is(M8):         -4.48e-05       device_current
Id(M7):         0.00136009      device_current
Ig(M7):         0               device_current
Ib(M7):         -1.94601e-12    device_current
Is(M7):         -0.00136009     device_current
Id(M4):         -2.22188e-05    device_current
Ig(M4):         -0              device_current
Ib(M4):         1.2892e-12      device_current
Is(M4):         2.22188e-05     device_current
Id(M6):         -0.00136009     device_current
Ig(M6):         -0              device_current
Ib(M6):         2.07399e-12     device_current
Is(M6):         0.00136009      device_current
Id(M3):         -2.22188e-05    device_current
Ig(M3):         -0              device_current
Ib(M3):         1.2892e-12      device_current
Is(M3):         2.22188e-05     device_current
I(Cc):          -2.02476e-25    device_current
I(Cl):          -2.18004e-24    device_current
I(Ib):          4.48e-05        device_current
I(Vdd):         -0.00144933     device_current
I(V2):          0               device_current
I(V3):          0               device_current
I(V4):          0               device_current
I(V5):          0               device_current
I(V6):          0.00144933      device_current
```
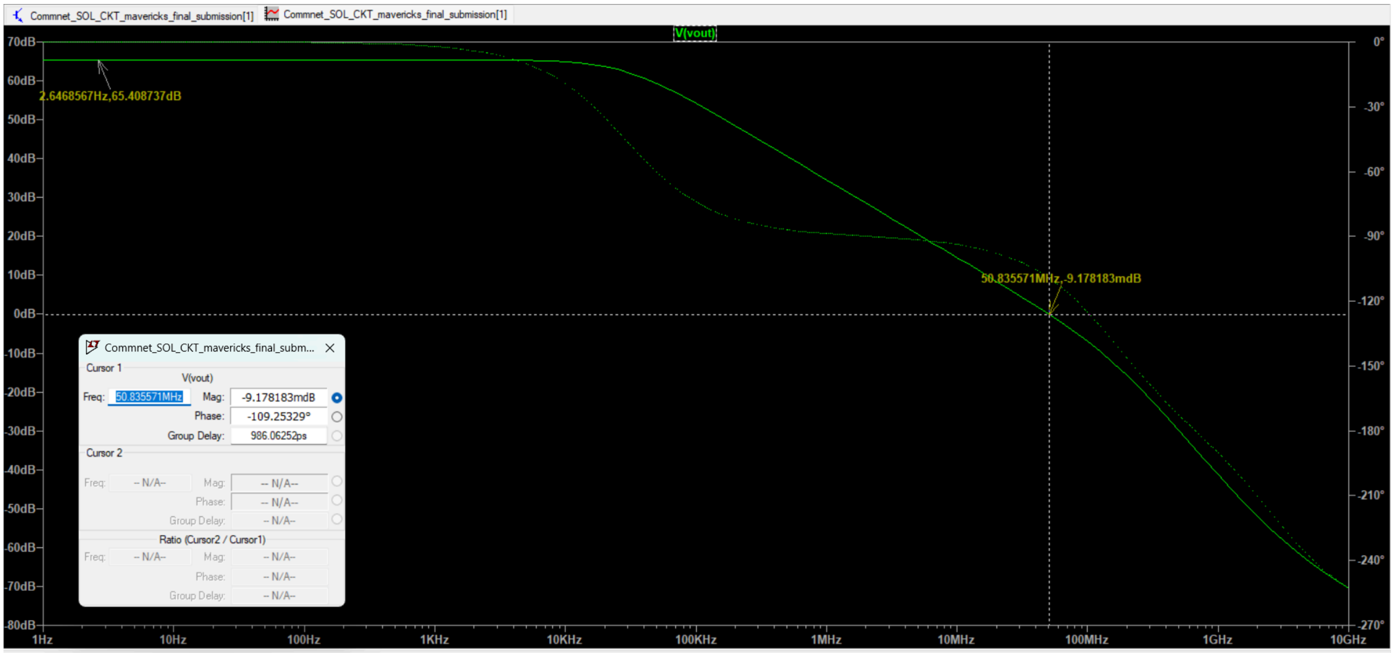

Bode plot :

At Input common dc voltage 0.7 Volts

At Input common dc voltage 1.6 Volts



DC Gain (simulation):- 66.01 dB(for 0.7 volts) and 65.408 dB(for 1.6 volts)

Specifications(LTSpice)	Value(At 0.7v)	Value(At 1.6v)
DC Gain	1997.56	1862.08
Phase Margin	70.05	70.74
Gain Bandwidth Product	50.35 MHz	50.83 MHz

LT Spice (Output log) :

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:        m1          m2          m5          m8          m7           m4          m6          m3
Model:      nmos        nmos        nmos        nmos        nmos         pmos        pmos        pmos
Id:        2.30e-05    2.30e-05    4.59e-05    4.48e-05    1.38e-03    -2.30e-05   -1.38e-03   -2.30e-05
Vgs:       8.01e-01    8.01e-01    1.62e+00    1.62e+00    1.62e+00    -1.29e+00   -1.29e+00   -1.29e+00
Vds:       4.13e-01    4.13e-01    2.30e+00    1.62e+00    2.33e+00    -1.29e+00   -1.67e+00   -1.29e+00
Vbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Vth:       7.00e-01    7.00e-01    7.00e-01    7.00e-01    7.00e-01    -7.00e-01   -7.00e-01   -7.00e-01
Vdsat:     1.01e-01    1.01e-01    9.17e-01    9.17e-01    9.17e-01    -5.89e-01   -5.89e-01   -5.89e-01
Gm:        4.53e-04    4.53e-04    1.00e-04    9.77e-05    3.01e-03     7.80e-05    4.69e-03    7.80e-05
Gds:       9.04e-07    9.04e-07    1.68e-06    1.68e-06    5.05e-05     1.08e-06    6.37e-05    1.08e-06
Gmb:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cbd:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgsov:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgdov:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgbov:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgd:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
Cgb:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00     0.00e+00    0.00e+00    0.00e+00
```

END OF REPORT !!!