UDYAM'24

ANNUAL TECHNICAL FEST OF ELECTRONICS ENGINEERING SOCIETY

COMMNET ' 24

PS - 1

The Two Stage op-amp

You are required to design a two stage miller-compensated op-amp with a capacitive load. Set Vss in the below figure to 0 (ground). A typical two stage op-amp looks like:

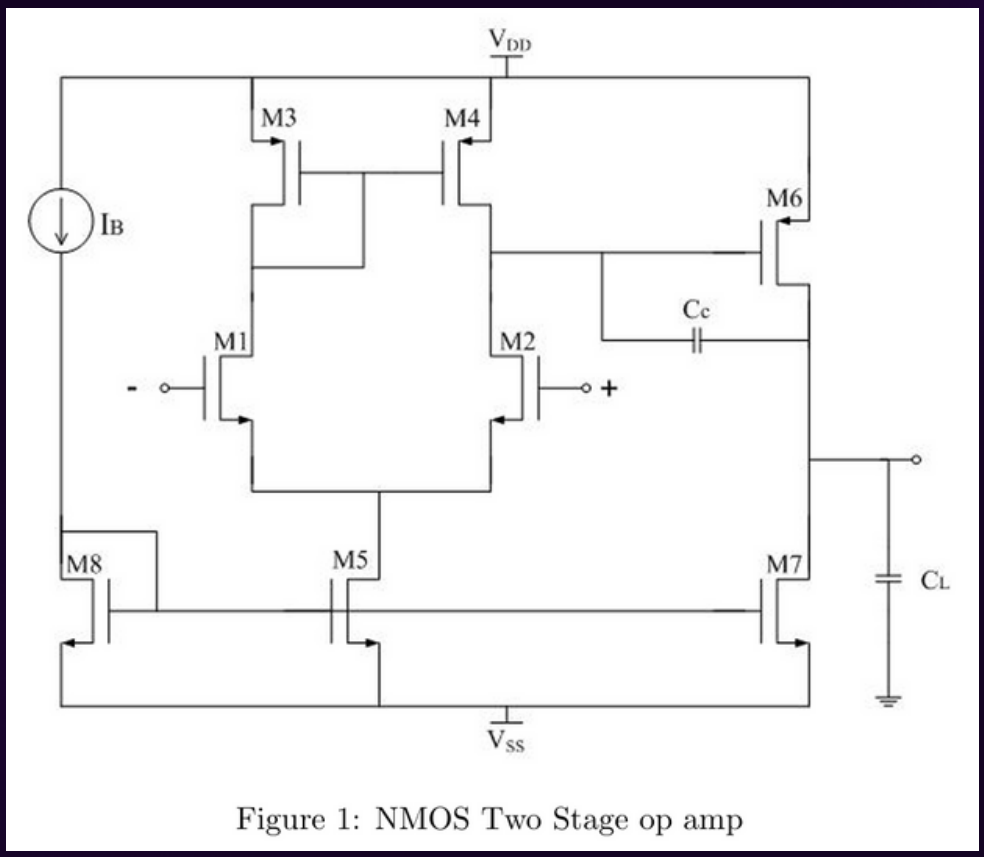

Figure 1: NMOS Two Stage op amp

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Design Specifications

Your op-amp model would be evaluated based on the closeness to achieving the below specifications -

- Reasonable Lengths and Widths of NMOS transistors have to be used.
  Report W and L of each transistor [5 points]
- DC gain = 2000 [5 points]
- Input Common Mode Range 0.7 V to 1.6 V [5 points]
- Phase margin > 60 degrees for a capacitive load of 5 pF [5 points]
- Gain-bandwidth (GBW) product of 50 MHz [5 points]

Design and simulate this circuit in any one of the simulation software including ADS or LTSpice. Attach the relevant circuit diagrams and make a detailed report regarding your approach in this PS.