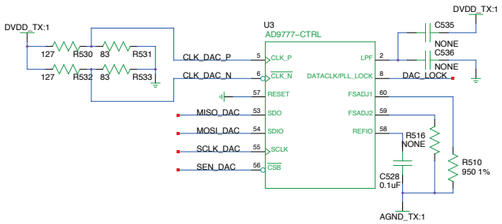
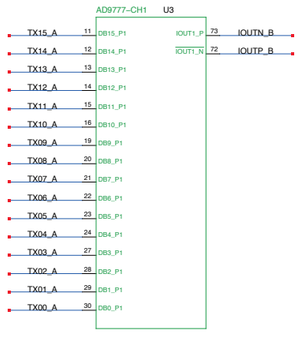
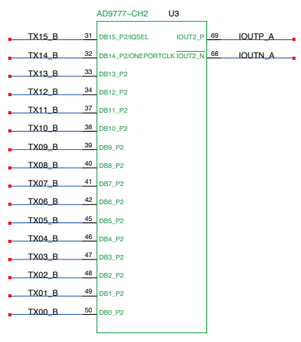
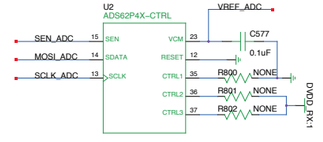
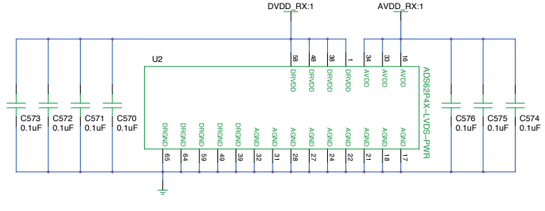






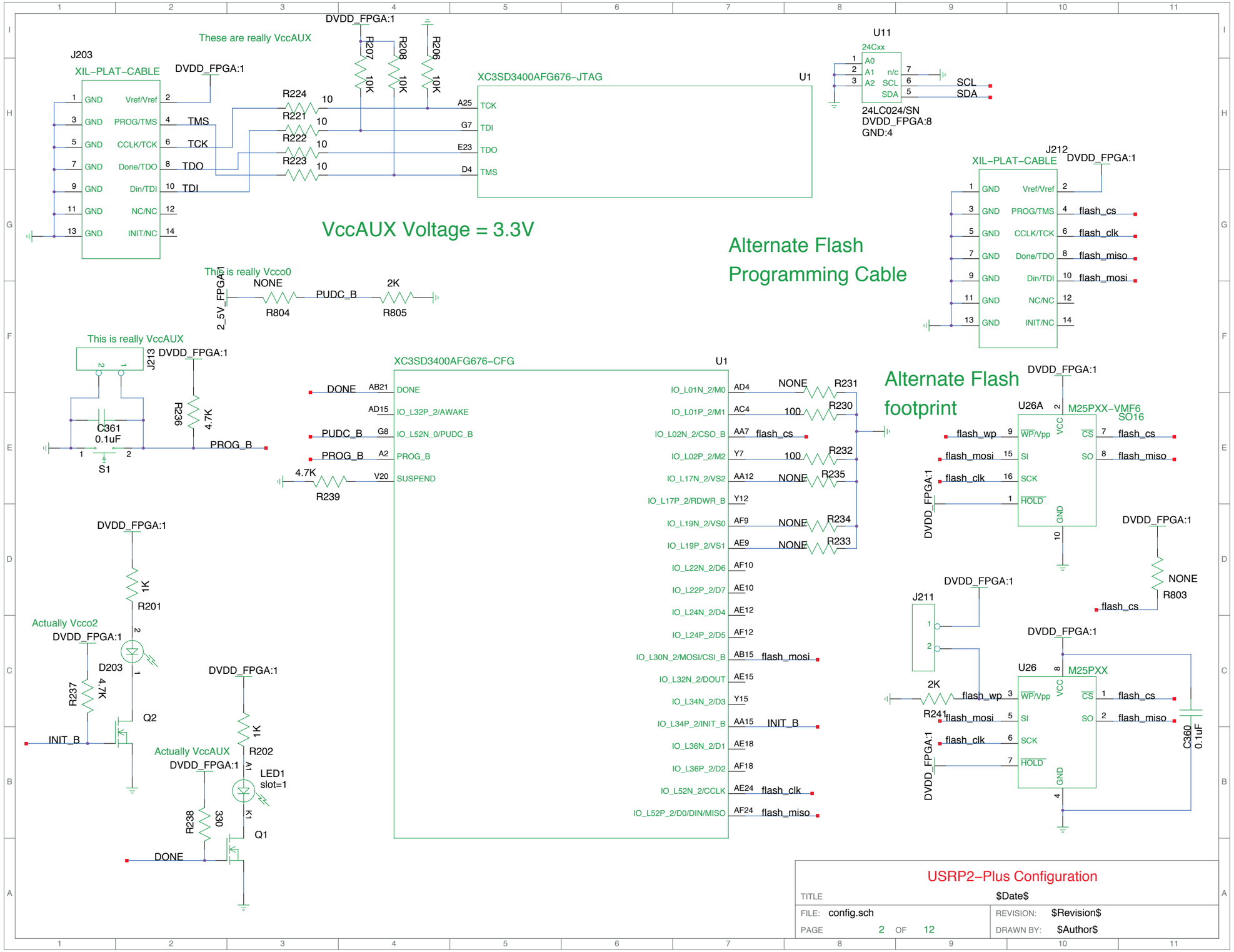
Inverted Input A to make routing easier
fix in FPGA

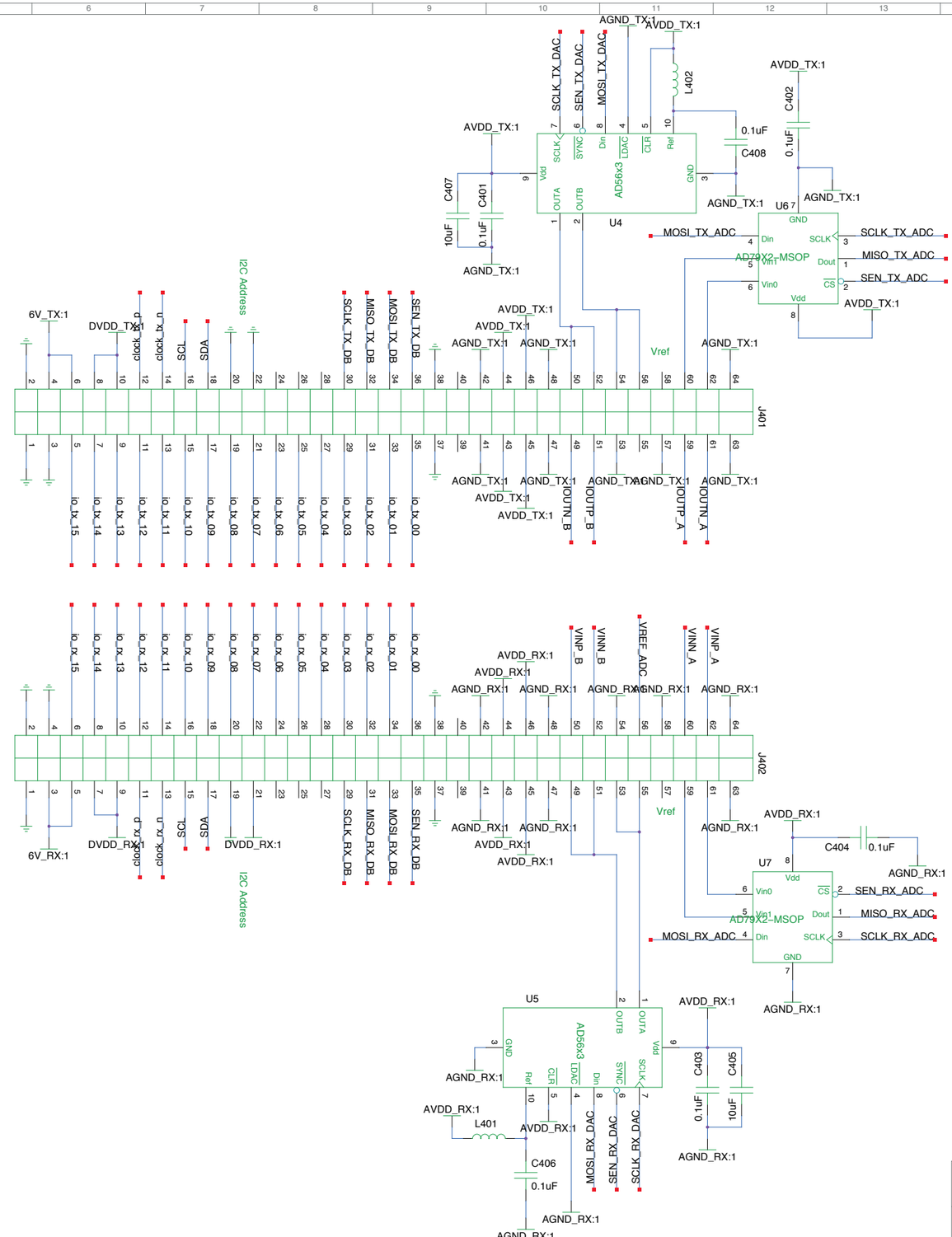




USRP2-Plus CODECs

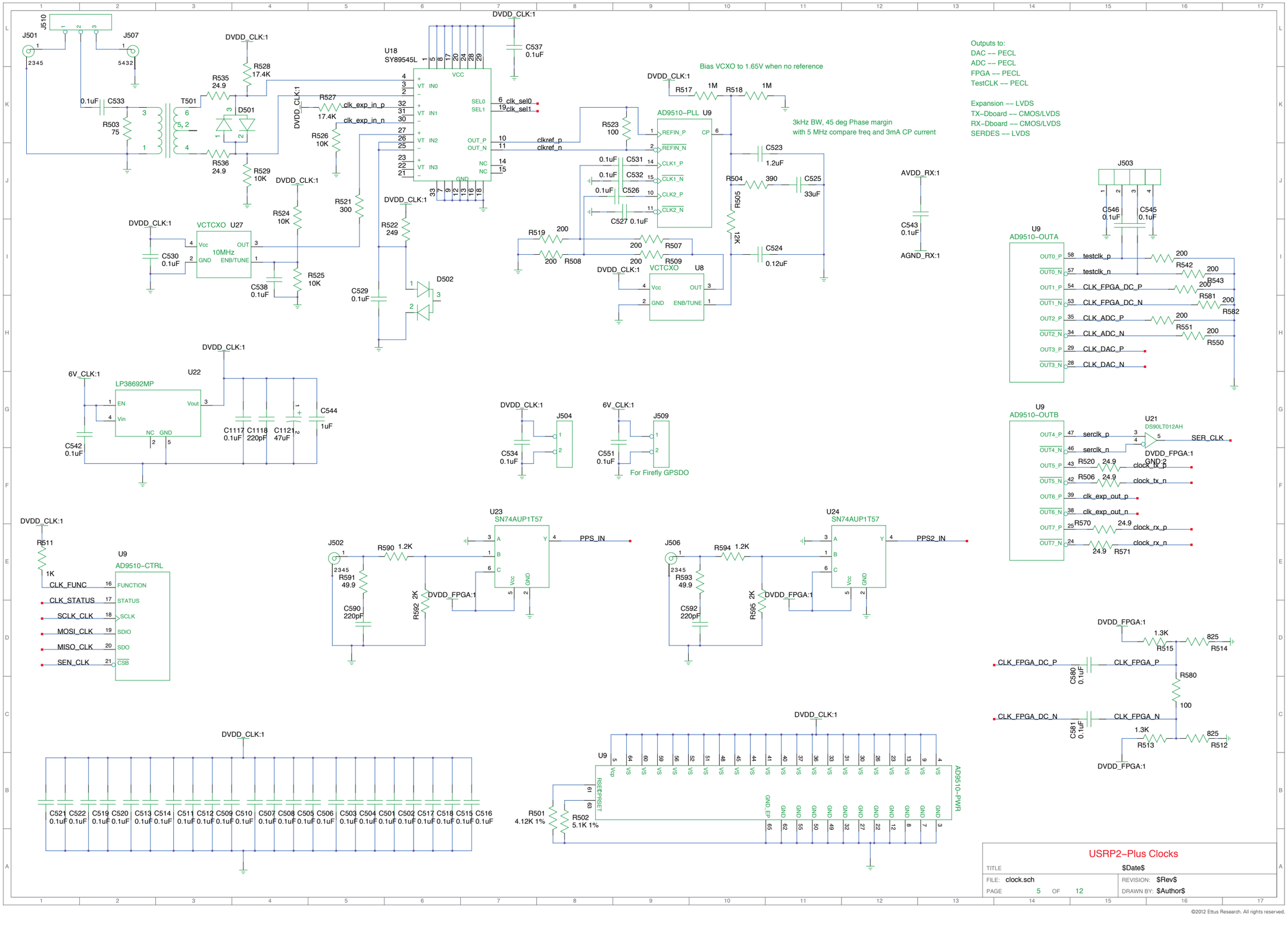
TITLE	$Date$		
FILE: codecs.sch		REVISION:	Rev
PAGE 3 OF 12		DRAWN BY:	$Author$

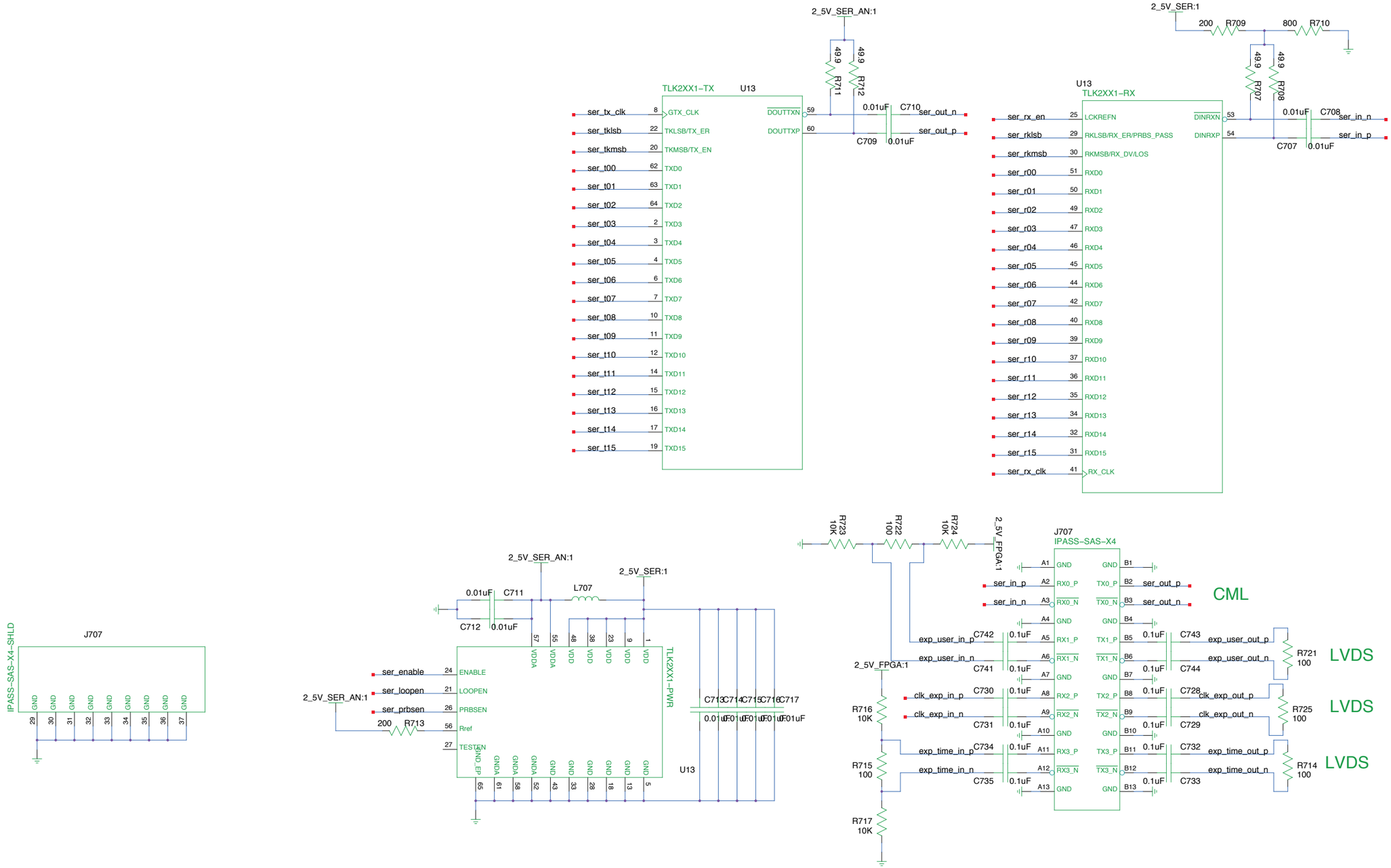




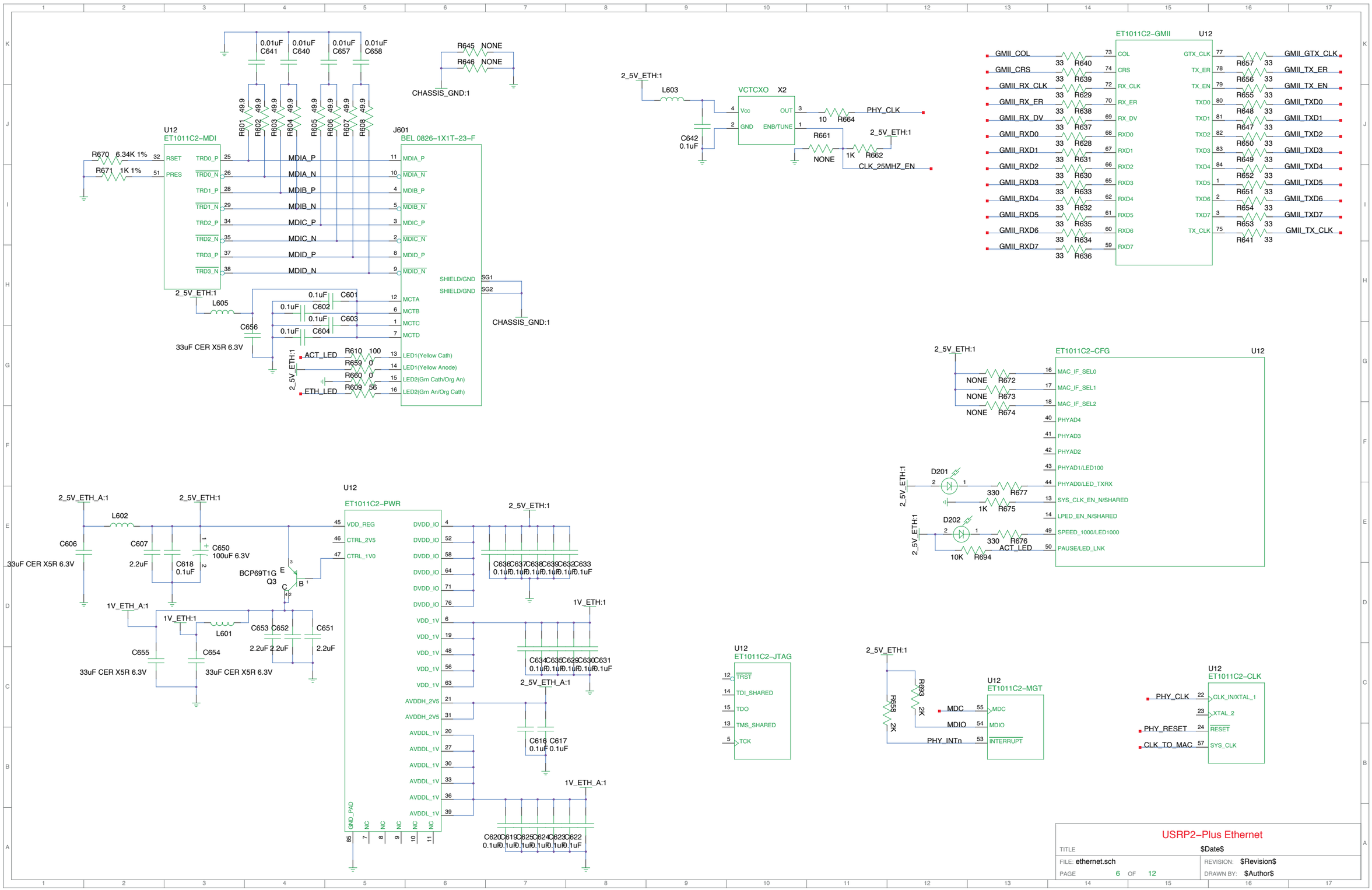
USRP2-Plus Daughterboad Interface

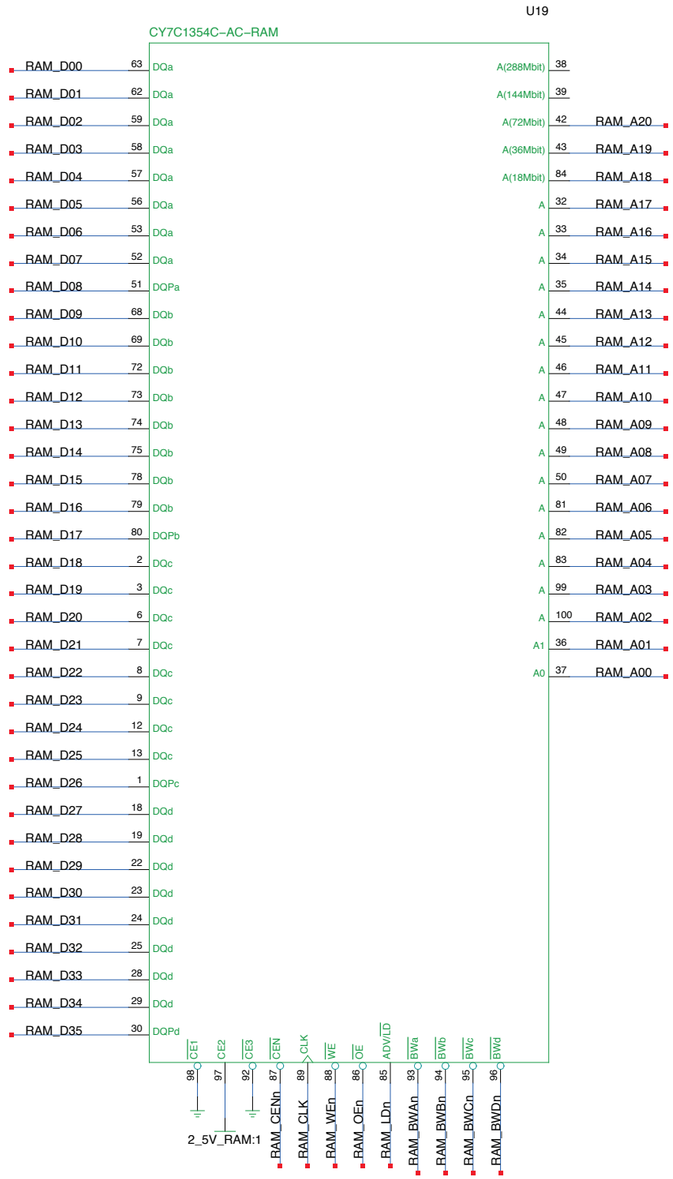
TITLE	$Date$
FILE: dboard.sch	REVISION: $Revision$
PAGE 4 OF 12	DRAWN BY: $Author$



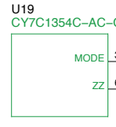


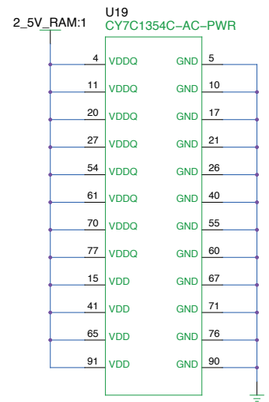
TITLE	USRP2-Plus Expansion
	$Date$
FILE: expansion.sch	REVISION: $Revision$
PAGE 7 OF 12	DRAWN BY: $Author$

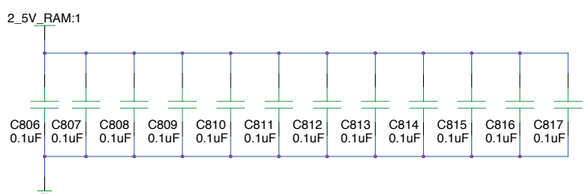




FIXME -- Extra Power Supply Pins for IDT Version?



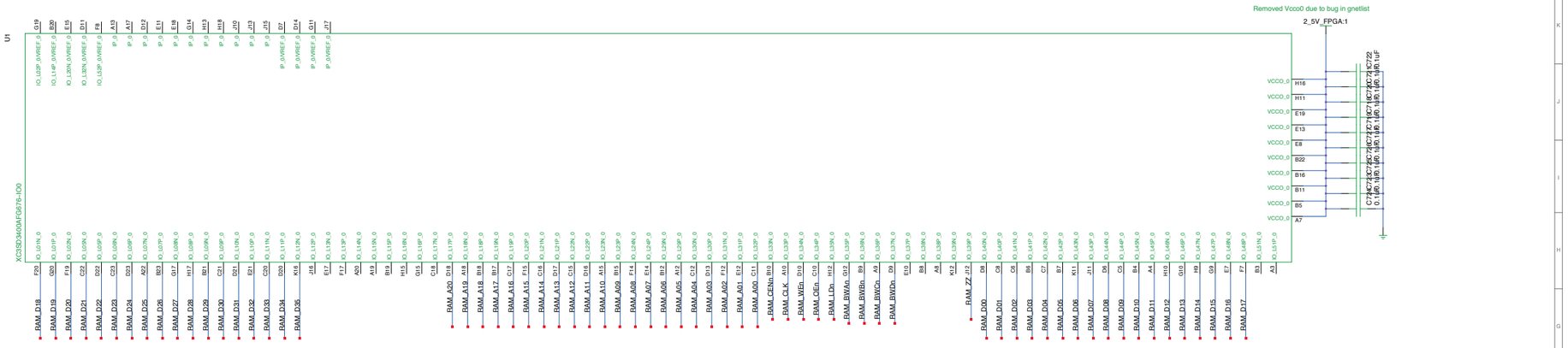


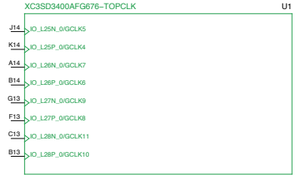


USRP2-Plus RAM

TITLE	$Date$
FILE: ram.sch	REVISION: Rev
PAGE 8 OF 12	DRAWN BY: $Author$

Bank 0, 2.5V
RAM





USRP2-Plus FPGA Bank 0

TITLE:	$Date$
FILE: fpga-bank0.sch	REVISION: Rev
PAGE: 9 OF 12	DRAWN BY: $Author$

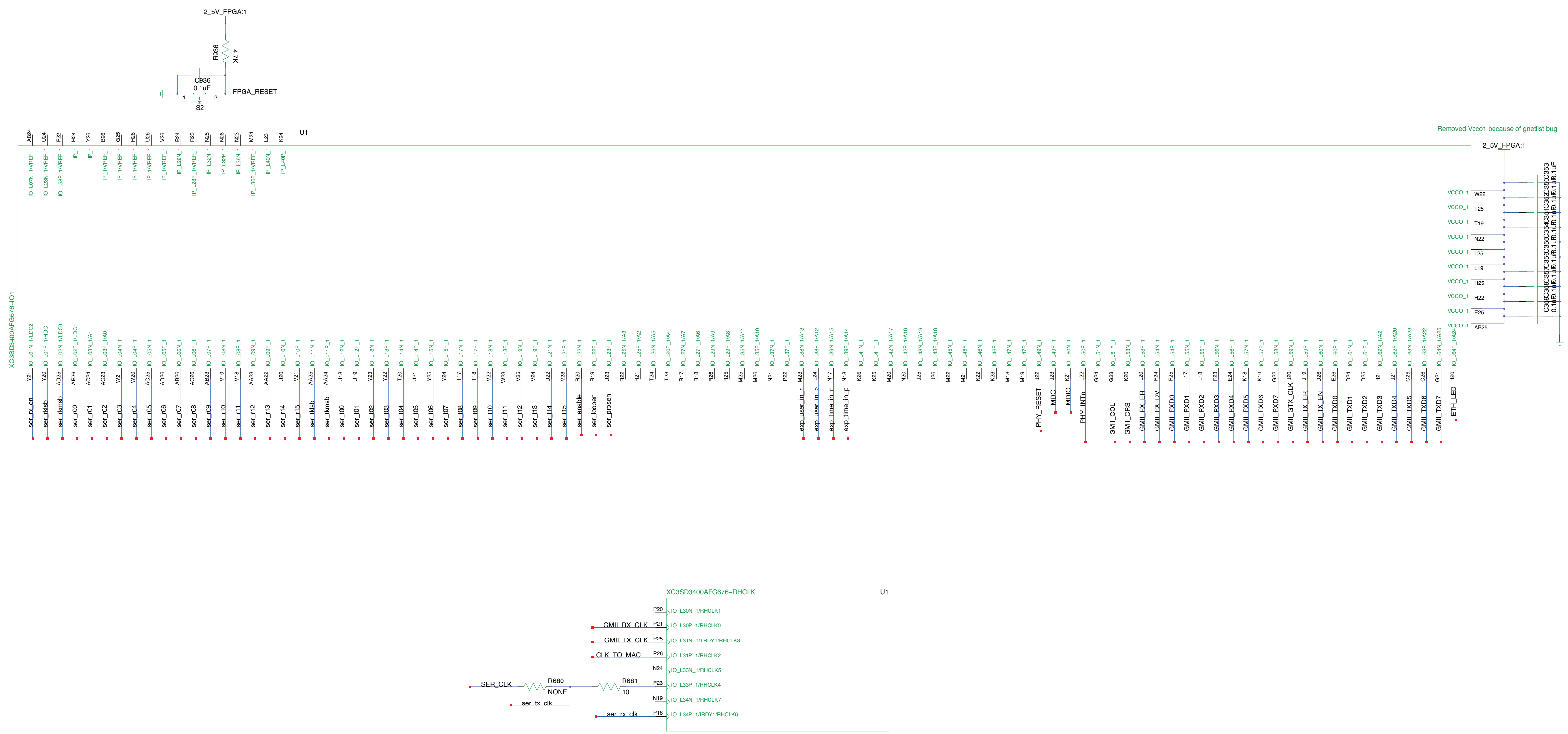
Bank 1, 2.5V

No LVDS Out

Ethernet

SERDES

Expansion LVDS in



USRP2-Plus FPGA Bank 1

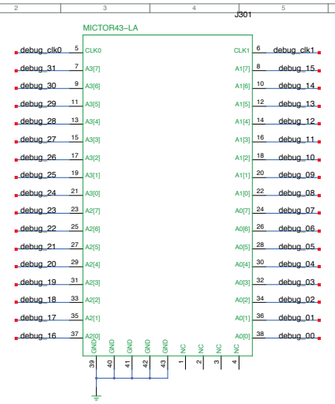
TITLE $Date$

FILE: fpga-bank1.sch

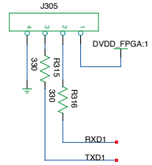
REVISION: Rev

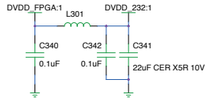
PAGE 10 OF 12

DRAWN BY: $Author$

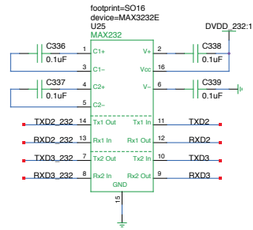


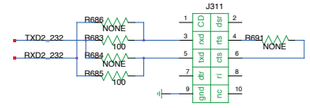
Bank 2, 3.3V
SPI Config
Clock Interface
Debug
I2C
BOTCLK
LEDs
RS232

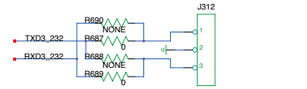


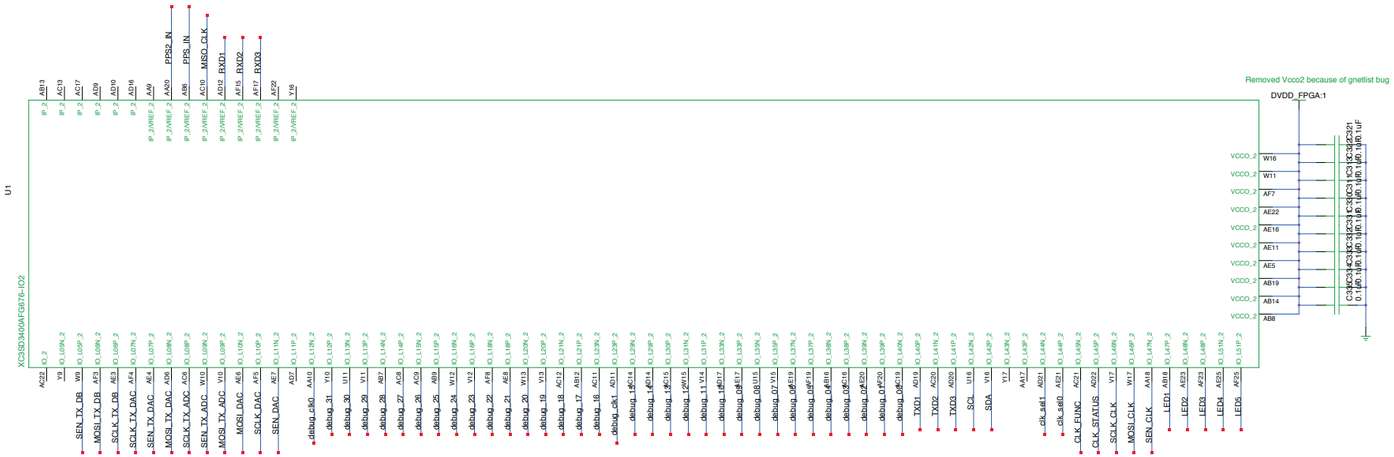


FIXME ~~~ Do we need RTS, CTS, DTR, DSR, CD, RI?

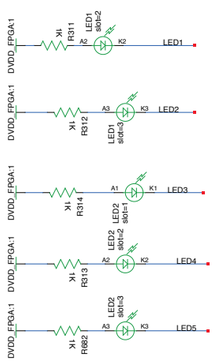


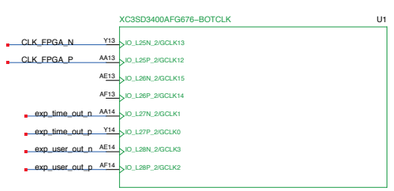






{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved from bank 3 (12 total lines)

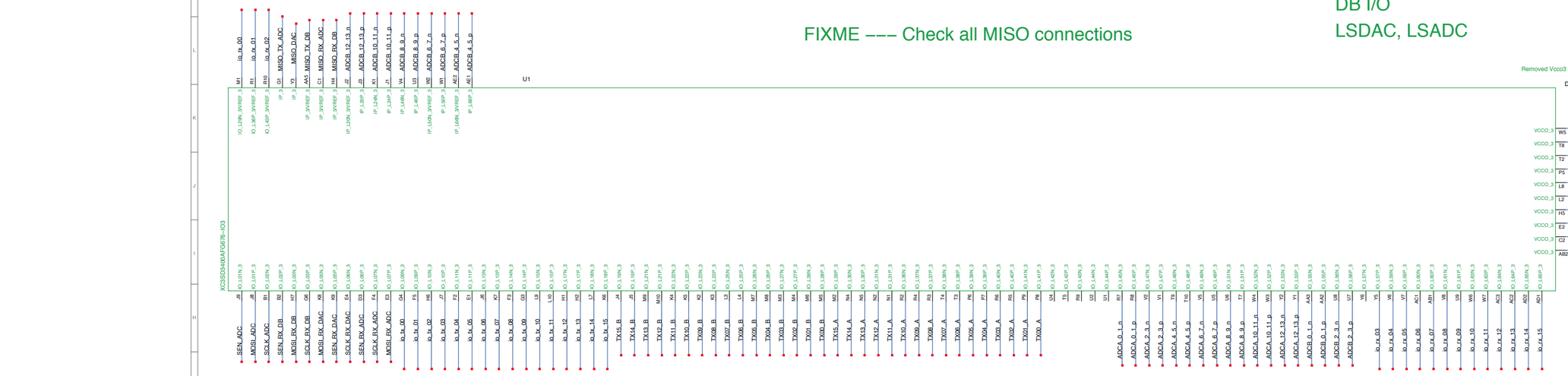




TITLE	USRP2-Plus FPGA Bank 2
	$Date$
FILE:	fpga-bank2.sch
REVISION:	Rev
PAGE	11 OF 12
DRAWN BY:	$Author$

Bank 3, 3.3V
DAC
ADC
DB I/O
LSDAC, LSADC

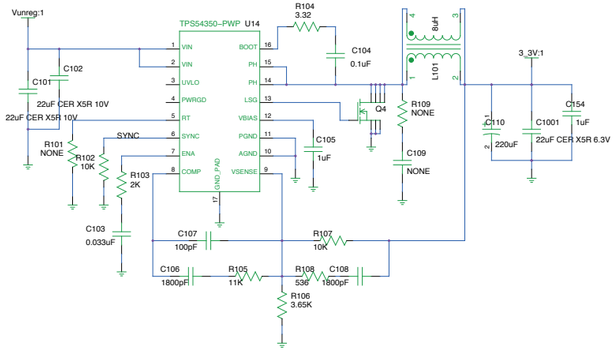
FIXME ––– Check all MISO connections

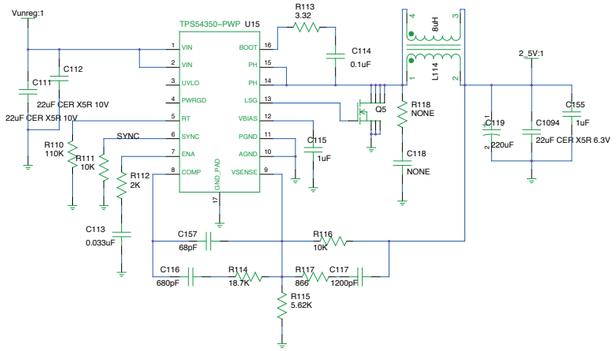


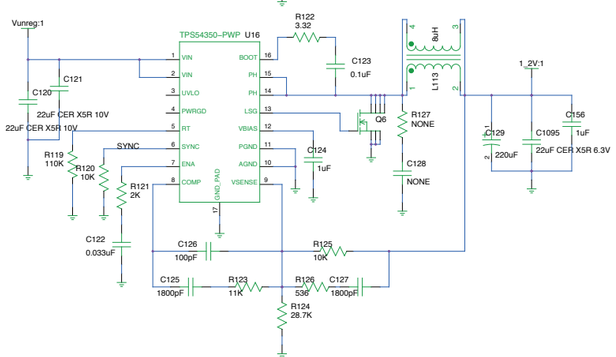
Removed Vcco3 because of gnetlist bug

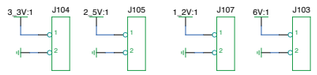
{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved to bank 2 (12 total lines)

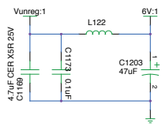
USRP2–Plus FPGA Bank 3	
TITLE: $Date$	
FILE: fpga–bank3.sch	REVISION: Rev
PAGE 12 OF 12	DRAWN BY: $Author$

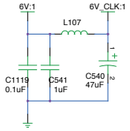


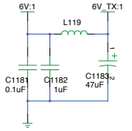


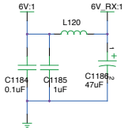




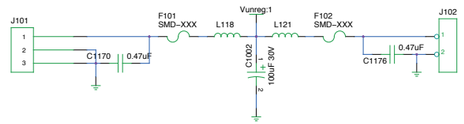








Front Panel Power

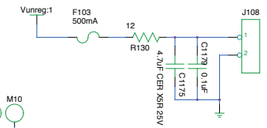


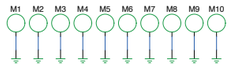
ALT Power

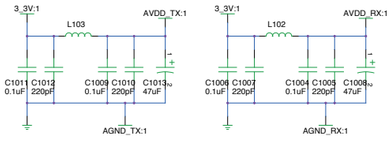
Power Supplies

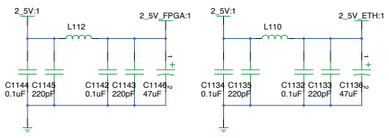
6V Daughterboard Power (<1A), 5V for clock reg
3.3VCLK AD9510 (<500mA), Clock (88mA)
3.3VAN ADC (200mA), DAC (<500mA)
3.3VDIG All IO (<2A), FPGA AUX
2.5V 1A –– Ethernet Core (600mA), SERDES (<150mA), RAM (<300mA)
1.2V FPGA Core (<2A)
1.0V Ethernet Core

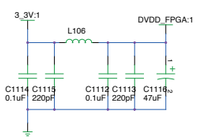
FAN Power



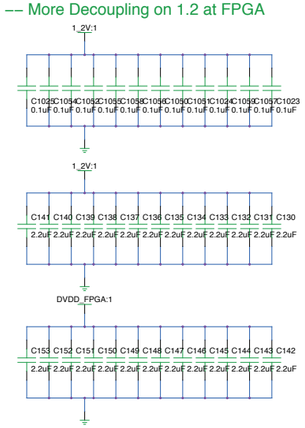


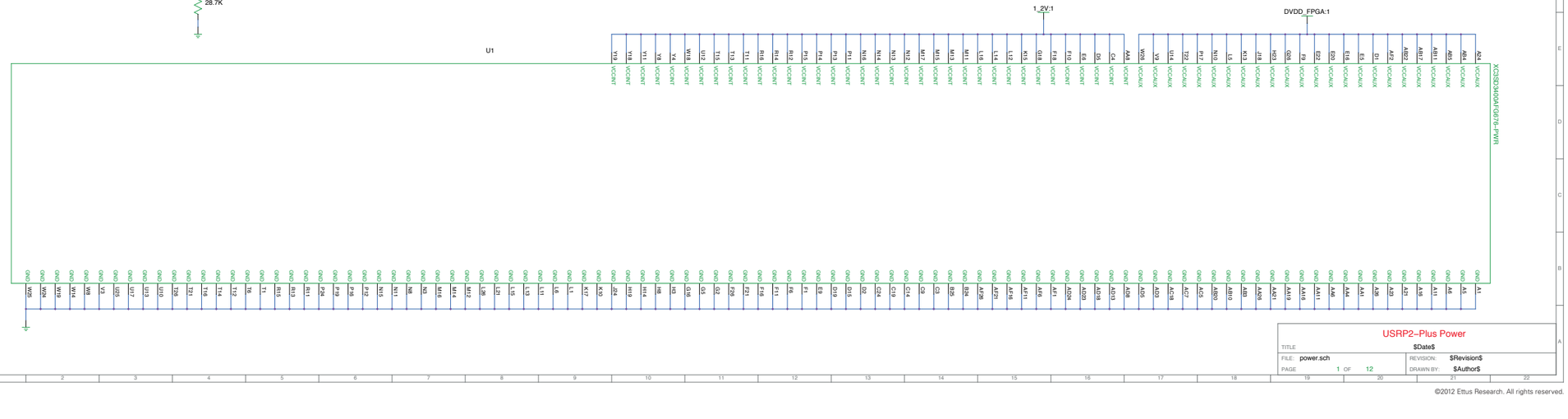






FIXME –– More Decoupling on 1.2 at FPGA





TITLE: USRP2–Plus Power	
	$Date$
FILE: power.sch	REVISION: $Revision$
PAGE 1 OF 12	DRAWN BY: $Author$