SVKM'S NMIMS

MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT& ENGINEERING/

SCHOOL OF TECHNOLOGY MANAGEMENT

Academic Year: 2023-2024

Program/s: B TECH / MBA TECH / B. Tech Integrated — Year: II/IV Semester: IV /VIII

Stream/s : IT/Comp Engg/CSE CS

Subject: Computer Organization and Architecture — Time: 03 hrs (10:00am to 1:00pm)

Date: 3 / 7 / 2024 — No. of Pages: 2

Marks: 100

**Re-examination(2022-23)**

**Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.**

1) Question No. _1___ is compulsory.
2) Out of remaining questions, attempt any __4___ questions.
3) **In all ___5_ questions to be attempted.**
4) All questions carry equal marks.
5) **Answer to each new question to be started on a fresh page.**
6) **Figures in brackets on the right hand side indicate full marks.**
7) **Assume Suitable data if necessary.**

| **Q1** | | Answer briefly: | |
|---|---|---|---|
| CO1, SO1,2 BL3 | a. | Compare computer organization and computer architecture | [5] |
| CO2 SO1,2 BL-2 | b. | Describe any five memory characteristics. | [5] |
| CO2 SO1,2 BL-2 | c. | Explain memory hierarchy in brief. | [5] |
| CO3 SO1,2 BL-2,3 | d. | Sketch and explain sequential circuit based ALU. | [5] |
| **Q2** CO1 SO1,2 BL-1,3 | a. | What is a bus? What are its functions? Draw and explain the bus-architecture and its interconnections. | [10] |
| CO2 SO1,2 BL3 | b. | Demonstrate the difference between SRAM and DRAM. Draw the DRAM structure and explain in brief. | [10] |

| | | | |
|---|---|---|---|
| **Q3**<br>CO3,4<br>SO1,2<br>BL-2 | a. | Describe the concept of Interrupt Driven I/O and its role in improving system performance. | **[10]** |
| CO3<br>SO1,2<br>BL-3,5 | b. | Sketch the flowchart of Booth's algorithm. Evaluate (-7) * (+3) using Booth's algorithm. | **[10]** |
| **Q4**<br>CO2<br>SO1,2<br>BL-1,2 | a. | Define cache memory. Explain direct mapping techniques for cache memory addressing. | **[10]** |
| CO4<br>SO1<br>BL1,2 | b. | What is Flynn's Classification? Describe the types of Flynn's classification in detail. | **[10]** |
| **Q5**<br>CO3<br>SO1,2<br>BL-1,5 | a. | How do we represent the floating-point number in IEEE 754 format? Represent the number "85.125" in single precision format and double precision format. | **[10]** |
| CO3<br>SO1,2<br>BL-2 | b. | Discuss the different type of addressing modes of 8086 processor with suitable example. | **[10]** |
| **Q6**<br>CO3<br>SO1,2<br>BL-1,3 | a. | How does the micro operation contribute to instruction execution within the CPU? In the context of the control unit, what are the key distinctions between hardwired control and microprogrammed control? | **[10]** |
| CO1<br>SO1,2<br>BL-1,2 | b. | What is Bus arbitration technique ? Explain any one arbitration method in detail. | **[10]** |
| **Q7**<br>CO3,4<br>SO1,2<br>BL-2,3 | a. | Outline the steps involved in DMA's basic operation for transferring data between peripherals and memory. Draw the required diagram to show the DMA transfer | **[10]** |
| CO3<br>SO1,2<br>BL-2 | b. | Discuss RISC and CISC computers. | **[10]** |