EE 460: Digital Design II
Design Assignment #03

Design of Fibonacci Number Generator

Due October 2, 2021

Requirements

Design a Fibonacci number generator that accepts as input a number n on the port **numberIn** and output the n^{th} Fibonacci number on the output port **numberOut**.

The n^{th} Fibonacci number is the sum of the $(n-1)$ and $(n-2)$ Fibonacci numbers, and the first two numbers in the sequence are 0 and 1. So the Fibonacci sequence is:

$$0, 1, 1, 2, 3, 5, 8, 13, 21, \ldots$$

Your design should accept the input value of n on the port **numberIn** when a start signal called **go** is high. The **reset** signal is active low and should be asynchronous. The output consists of the n^{th} Fibonacci number on the port **numberOut** and a **done** signal of 1 for one clock cycle indicating that the output is valid.

The maximum number of n is 24 and hence the 24^{th} Fibonacci number is $46,368$. The Fibonacci numbers generator algorithm can be described in the following C-code:

```
unsigned int fibonacci (int n){
    unsigned int previous = 0;
    unsigned int current  = 1;

    unsigned int tmp;

    unsigned int count = 1;

    while(count < n) {
```

```
        tmp      = current;
        current  = current + previous;
        previous = tmp;

        count = count + 1;
      }
      return current;
}
```

Your Design

You should follow all design steps.

- Start with the top-level block diagram and identify all external (primary) input and output signals for the whole design.
- Divide your design into two units: Data Path unit and Control Unit. Identify all the signals to the data path and control unit.
- Show the design of the Data Path Unit: Identify the required blocks (i.e., storage elements, functional units, and interconnects) and design them.
- Show the design of the Control Unit: Identify the required control signals, design the Control Unit, and connect it to the data path.
- Write Verilog modules for both data path and control unit.
- Write Verilog module for the whole design.
- Write a test unit (test bench) to test and simulate your design.

Your Report

The quality of your report is as important as the quality of your design. One must sell the design by justifying all design decisions. Be sure to provide all relevant information.

Your report must include the following:

- **Cover Page**: Design Title, Your Name and student ID
- **Introduction**: The objective of your design and the problem you want to solve

- **Top Level Design**: The block diagram of your design showing inputs and outputs and the interaction between control unit and data path.
- Your design of the data path.
- Your design of controller.
- Your simulation and timing diagram (Wave forms).

Submission

You need to submit your complete report and your Quartus project. Zip all files into one zip file.