EE 460: Digital Design II
Design Assignment #01

Tristate Adder

Due January 29, 2022

In this design assignment, you are required to modify the Tristate Bus (Figure 1-56 on page 48 of the textbook) to add an Adder. The adder will add the contents of registers A and C and store the result into register A, B, or C. **Your design must be clear and neat**.

Write a Quartus project that **implements** your design. Use the Verilog codes in class website (also attached to this assignment). Simulate your project to show the correctness of your design.

Implement the following operations in your simulation (test bench):

- The operation B = A + C.
- The operation C = C + B.
- The operation B = A + A.

You need to submit:

- Your design; the tristate buffer with Adder. Show all the connections and control signals.
- The Quartus project of your implementation include your test bench.
- An image of the waveform that shows all three operations.

zip all your submission into one file.