Department of Electrical Engineering Due 30 September 2024

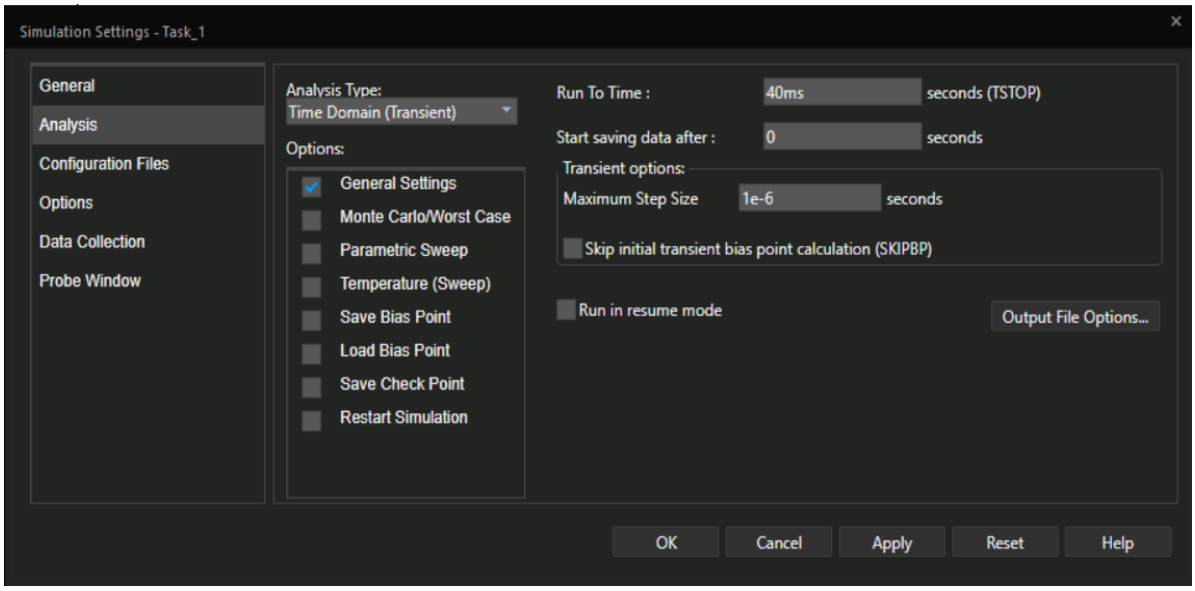
ELEC 4170 Midterm
Electric Drives Laboratory

Submitted By:

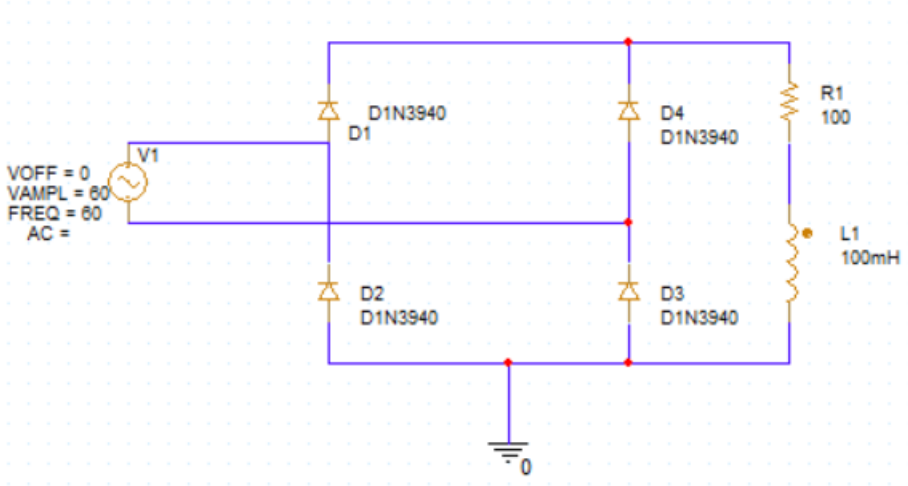
University of Colorado
Denver

Task 1: Singe-phase full-wave diode rectifier with RL load

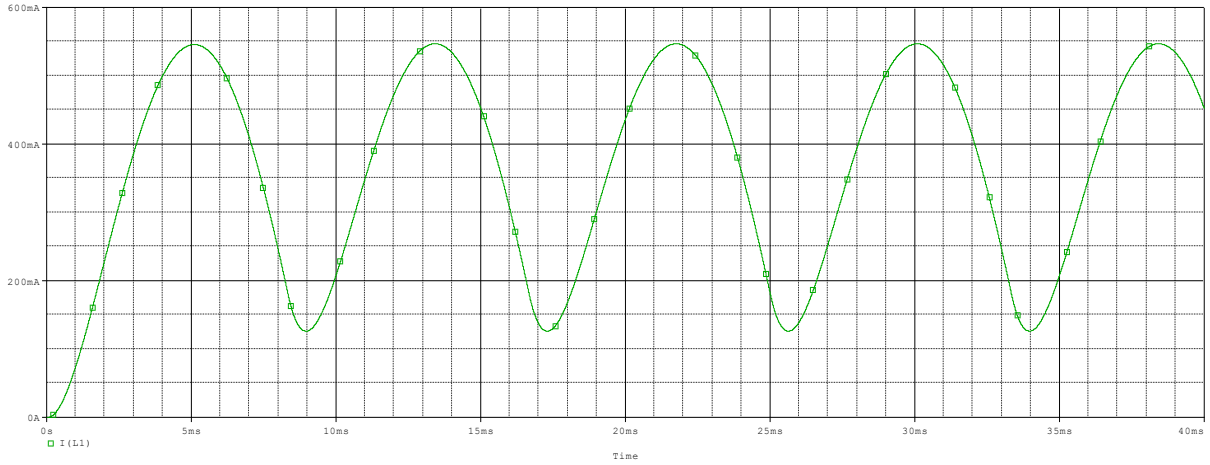
a. Show your analysis tab of simulation settings.



b. Show your schematic with all essential parameters.

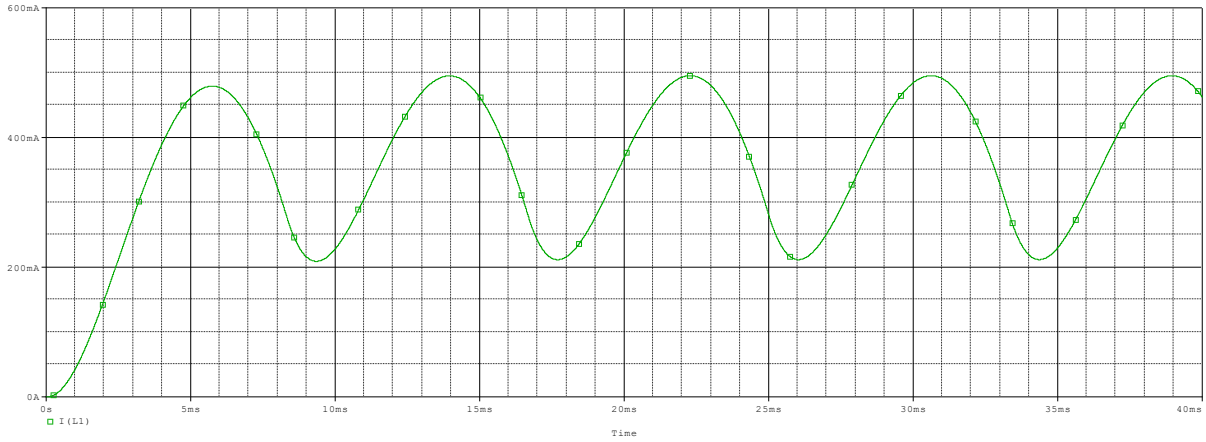


c. Plot the inductor current



d. Replace the inductor to ***<u>200mH</u>***

1) Plot the new inductor current



2) Compare your answer from c. and answer from d.1). Use equations to explainthe difference between.

- For a full-wave rectifier, the current through an inductor can be determined using the relationship :

$$V_L = L\frac{di_L}{dt}$$

For higher inductance (such as L=200mH), the inductor opposes changes in current more strongly, causing the current to rise and fall more slowly. This results in smoother, less rippled current over time.

Task 2: Three-phase half-wave phase-controlled rectifier with RC load

a.If we have voltage pulse (a phase gate signal) appears at *5ms*,

1) Calculate the firing angle.

Ans: Since the frequency f is 20 Hz, the period T of the sinusoidal wave is given by:

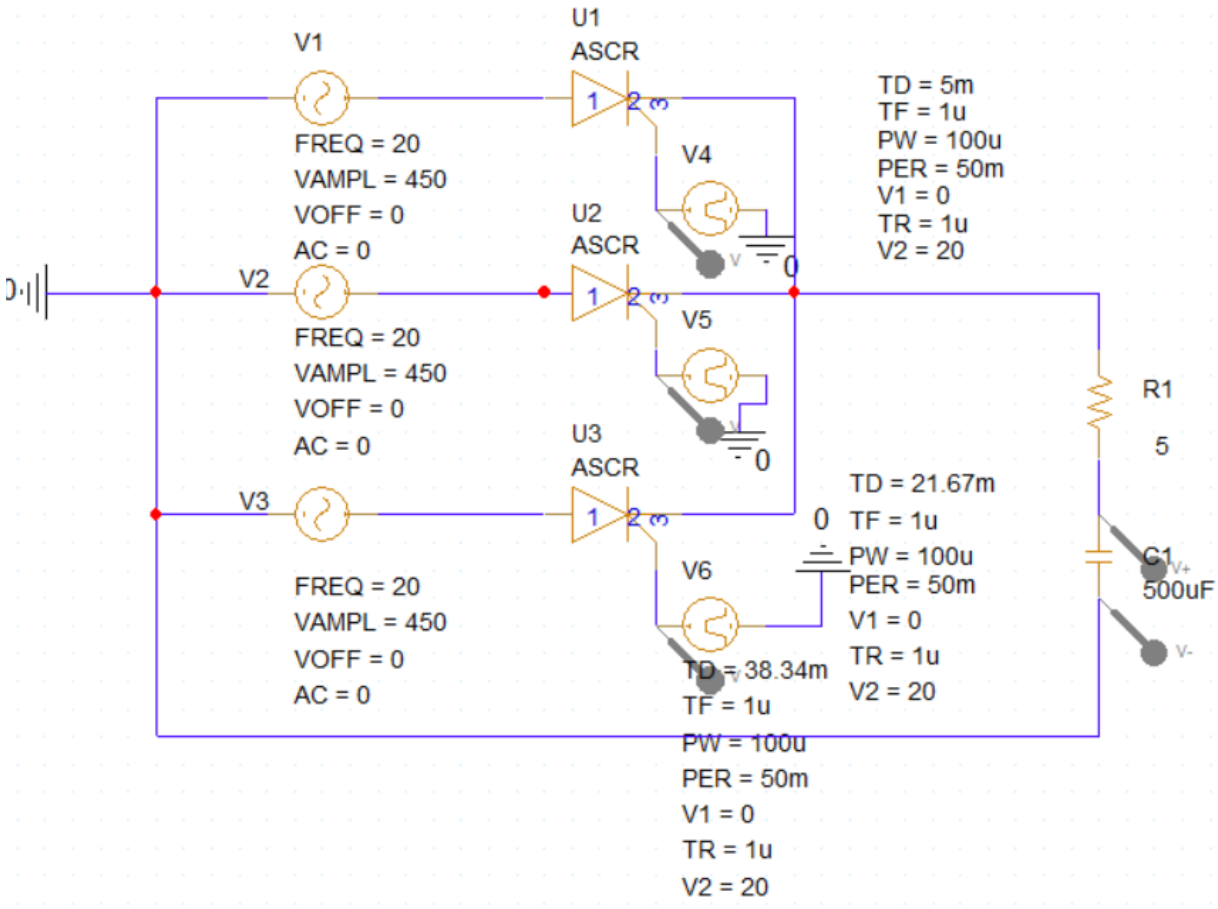
$$T = f/20 = 0.05 \text{ seconds} = 50 \text{ ms}$$

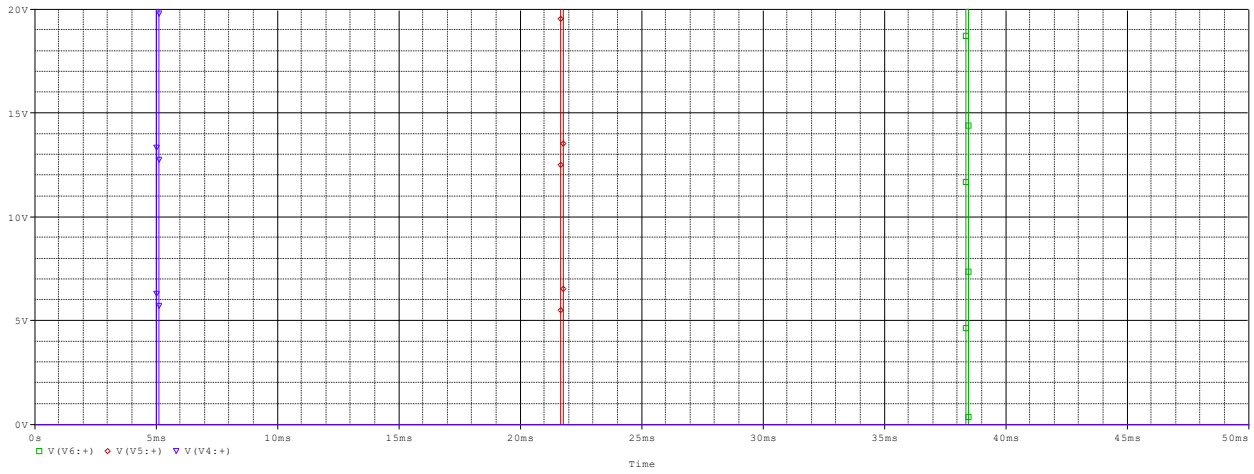
Find the Phase Angle Corresponding to 5 ms:

Since 1 complete cycle (360°) lasts for 50 ms, the phase angle 0 corresponding to 5 ms can be found by:

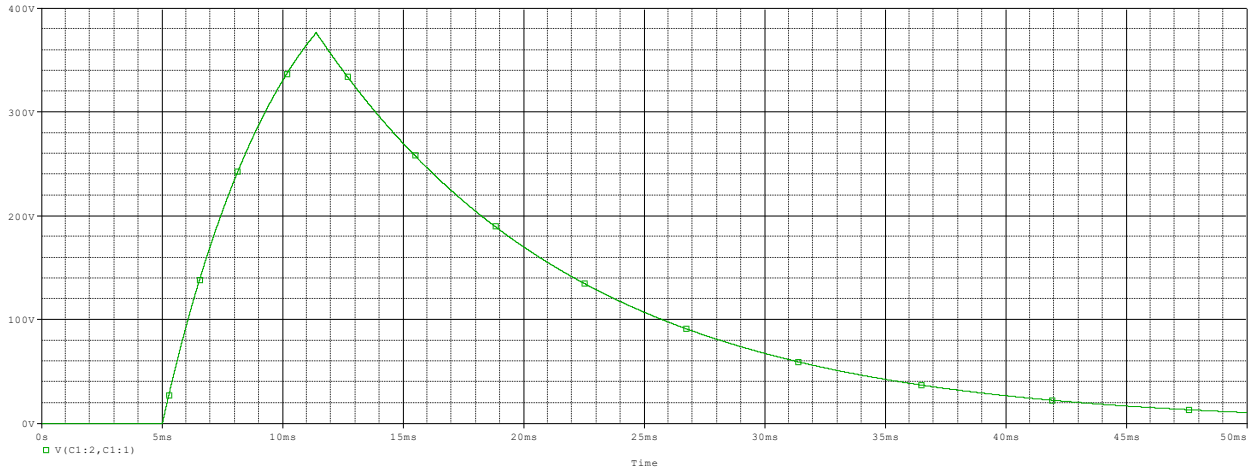
(5 ms/50ms)*360=36 Degree

2) Show the schematic of all gate signals.



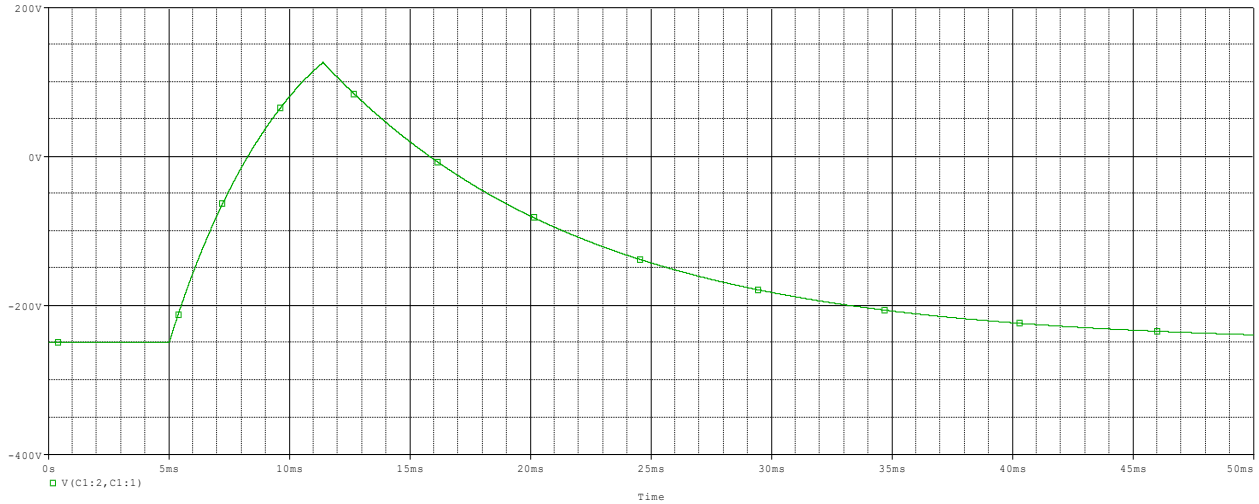


3) Plot the voltage across the capacitor.



b. If we add another *250V* constant voltage load in series with the resistance, otherconditions remain the same as in part a.

1) Plot the new voltage across the capacitor.



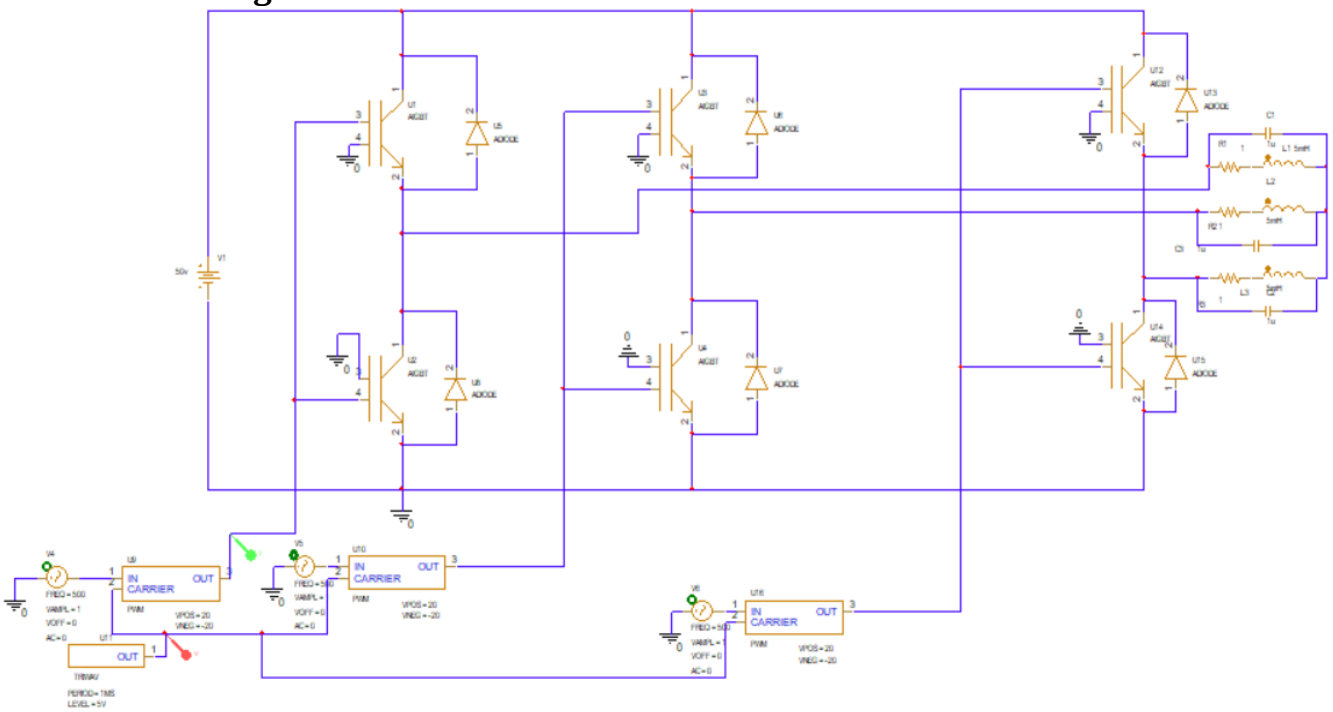
2) Compare your answers from a.3) with b.1). Briefly explain about what causesthe difference.

Ans: The main reason for the difference is the **constant voltage source** (250V) added in series with the resistance. This load alters the voltage distribution in the circuit:

- The additional voltage source reduces the maximum possible voltage across the capacitor since the total voltage now has to account for the 250V drop.
- The capacitor's discharge is impacted, causing the voltage to decrease more rapidly and eventually go negative as the load provides a consistent opposing voltage during the discharge phase.

Task 3: Three-phase bridge converter with RLC load.

a. Show your bridge converter schematic with load, no source and referencevoltage needed.



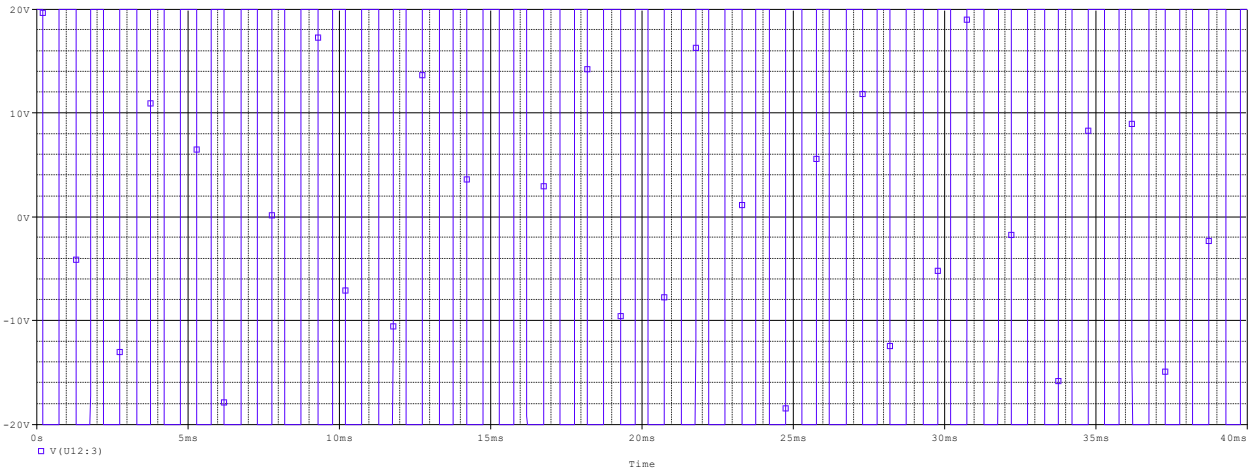
b. Assume positive sequence balanced output and the desired output voltage wavegiven as,$v_a(t) = 20\sin(10\pi * t)$

1) Write down the expression for other two phases.

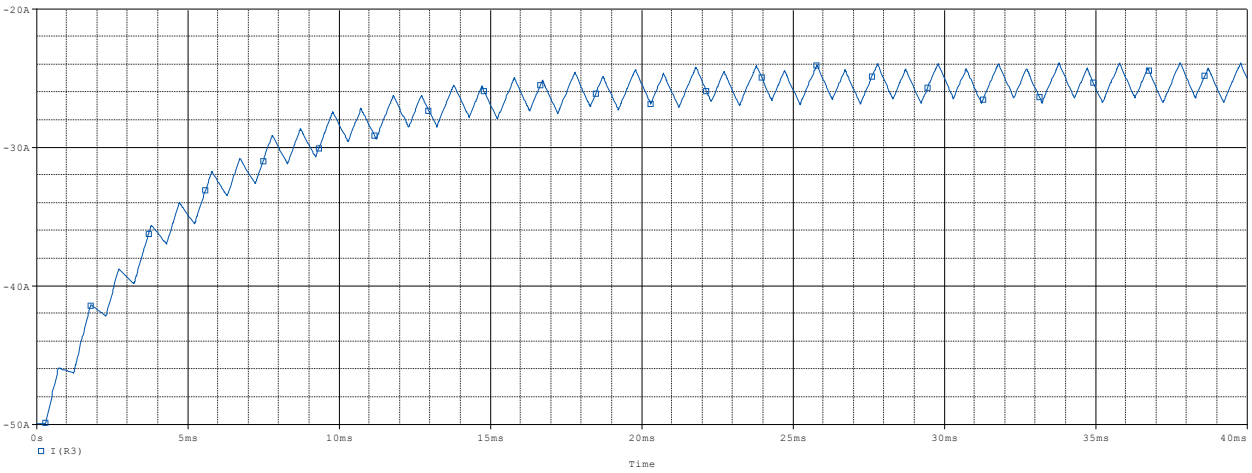
$$vb(t)=20\sin(10\pi t-32\pi)=20\sin(10\pi t-120\circ)$$

$$vc(t)=20\sin(10\pi t+32\pi)=20\sin(10\pi t+120\circ)$$

2) Plot the PWM for phase c, and briefly explain about PWM.



3) Plot the inductor current ripple.



4) Now the desired output voltage wave changes to $v_a(t) = 20\sin(1000\pi * t)$,other conditions remain the same.Can you use the same PWM generator? If not, then design your own and brieflyexplain about it.

Ans: The desired output voltage wave has changed to $va(t)$ = 20 sin(1000π $*$ t), which means:

1. The amplitude has increased to 20V (peak)

2. The frequency has increased to 500 Hz (1000π rad/s)

No, we cannot use the exact same PWM generator as shown in the circuit. Here's why:

1. Amplitude: The circuit needs to be adjusted to handle the higher voltage (20V peak instead of the previous value).

2. Frequency: The significant increase in frequency (from 60 Hz to 500 Hz) requires a much higher carrier frequency for effective PWM generation.

Design modifications needed:

1. DC Bus Voltage: Increase the DC bus voltage (V1 in your circuit) to at least 30V to accommodate the new 20V peak output.

2. Carrier Frequency: The carrier generators in your circuit (U1, U2, U3) need to be set to a much higher frequency. For a 500 Hz fundamental, a carrier frequency of at least 10 kHz is recommended. Adjust these to about 15 kHz for better performance.

3. Reference Signal: The sine wave generator (not shown in your circuit) needs to be adjusted to produce a 500 Hz sine wave.

4. Power Devices: The MOSFETs (M1-M6) and their respective gate drivers may need to be replaced with ones capable of handling higher switching frequencies and voltages.

5. Output Filter: The LC filter components (L1, L2, L3, C1, C2, C3) need to be redesigned for the new fundamental frequency of 500 Hz. The cutoff frequency should be between 500 Hz and the new carrier frequency.

6. Control Logic: The control logic generating the PWM signals needs to be updated to handle the higher frequencies.

Brief explanation of the modified design:

1. Generate the 500 Hz sine wave reference and the 15 kHz carrier signals.

2. Implement the comparison logic in software or with faster comparators.

3. Use gate drivers capable of operating at 15 kHz.

4. Select MOSFETs rated for at least 60V and capable of switching at 15 kHz.

5. Design the output LC filter with a cutoff frequency around 5 kHz.
