All codes in Main module and test bench are fully working…….Only 1 is executed and all others are commented

Code is for Single port RAM……..This is not fpga block ram……..it is just to design our own ram on fpga area……It is asynchronous ,,,,,,,,,,For synchronous we have to use clock.

In test bench first of all for loop will be executed completely and then repeat loop….commands inside of both loops will run sequentially……..if $display is not showing on console increase simulation time or run simulation for further nanoseconds……..

It can be seen from waveform that when data assigning ends then random addresses are generated and we see data on these random addresses that already stored