#Design a 2-input AND gate and simulate its question.

```
module and_gate(
input a,b,output c
);
assign c=a&b;
endmodule
module tb;
reg a,b;
wire c;
and_gate aa(.a(a),.b(b),.c(c));
initial begin
$monitor("time:%0t | a=%b b=%b => c=%b",$time,a,b,c);
a=0;b=0;#50;
a=0;b=1;#50;
a=1;b=0;#50;
a=1;b=1;#50;
end
endmodule
```

4-bit Binary Adder Design and simulation

```
input [3:0] A, B,
input Cin,
output [3:0] Sum,
output Cout
);
```

```
assign {Cout, Sum} = A + B + Cin;
endmodule

module test_four_bit_adder_test;
reg [3:0] A, B;
reg Cin;
wire [3:0] Sum;
wire Cout;

four_bit_adder adder1(A, B, Cin, Sum, Cout);

initial begin
$monitor("time=%0t | A=%b | B=%b | Cin=%b | Sum=%b | Cout=%b",$time,A,B,Cin,Sum,Cout);

A=4'b0000; B=4'b0000; Cin=0; #50;
A=4'b0101; B=4'b0011; Cin=0; #50;
A=4'b1111; B=4'b0001; Cin=0; #50;
A=4'b1010; B=4'b0101; Cin=1; #50;
A=4'b1111; B=4'b1111; Cin=1; #50;
end
endmodule
# design a 2-to1 multiplexer and simulate it
module mul(
input a,b,sel,
output y
);
```

```
assign y=(sel)?b:a;
endmodule
module tb;
reg a,b,sel;
wire y;
mul m(.a(a),.b(b),.sel(sel),.y(y));
initial begin
$monitor("time=%0t a=%b b=%b sel=%b y=%b",$t,a,b,sel,y);
a=0;b=0;sel=0;#100;
a=0;b=1;sel=0;#100;
a=1;b=1;sel=1;#100;
a=0;b=1;sel=1;#100;
end
endmodule
#design an 8 bit 2-to-1 multiplexer in Verilog
module m821(
input [7:0] a,b,
input sel,
output [7:0]y
);
assign y=(sel)?a:b;
endmodule
module tb;
reg [7:0]a,b;
reg sel;
wire [7:0]y;
```

```
m821 m(.a(a),.b(b),.sel(sel),.y(y));
initial begin
$monitor("time:%0t a=%b b=%b sel=%b y=%b",$time,a,b,sel,y);
a=8'b0000;b=8'b0001;sel=1;#100;
a=8'b1111;b=8'b0101;sel=0;#100;
end
endmodule
```