Cache Simulator Report

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First of all, I did the extra credit, please give me point for that. Thank you.

For this assignment, I built a software to simulate the hardware: cache. The main data structure I create is called line which contain three elements: Tag, Valid and Time. Tag is the tag index used to find in which block the address is in. Valid is an int variable that have two possible value: 1 and 0; If is is 0 it means the block is empty. The other variable time is used for the FIFO and LRU.

And then I allocate space for a 2-D array holds the structure line based on different number of set and assoc. Because the set index is numbers like 0,1,2 I can use the set index to find the right position in the array.

For FIFO, every time I write something into the cache I increase the number of count and update the time variable in line to count so when I want to kick something out I will find the minimum number of time and kick that from cache. For LRU, I increase the count whenever there is a hit too. So the least number of time means it is less recently used. Because for variable count, I use the unsigned long int so it will be safe.

My observation of prefetch: Memory write is the same, but it increase the chance of cache hit and decrease the time for cache miss so the running time will be short based on the locality.

Thank you. Last but not least, please give me extra credit for LRU because it gives me full mark when I run autograder in ilab machine! Thank you and wish you a Merry Christmas~~~~~