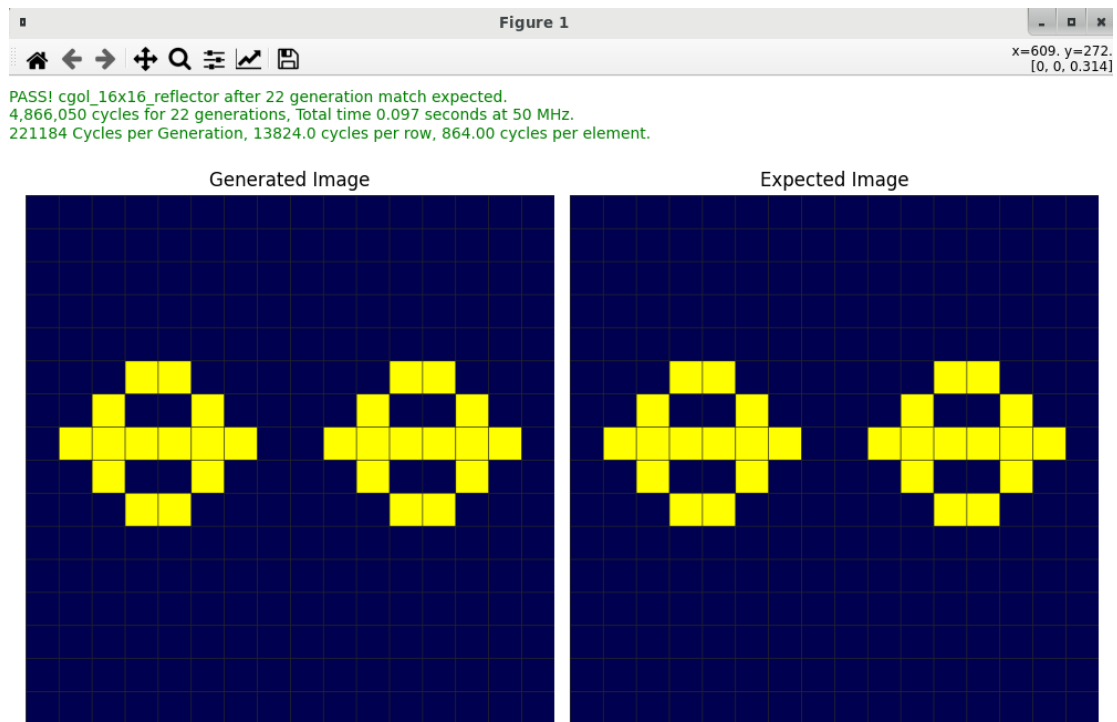


## CGOL XLR DDP25 – סיכום דוח

ראשית, התחלנו בהרצה של התוכנה:

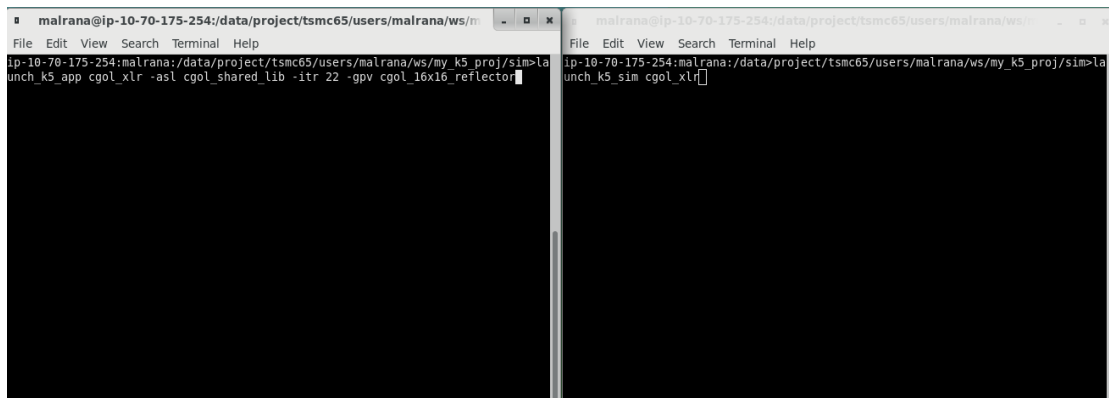
```
malrana@ip-10-70-175-254:/data/project/tsmc65/users/malrana/ws/...  
File Edit View Search Terminal Help  
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/sim>la  
unch_k5_app cgol -asl cgol_shared_lib -itr 22 -gpv cgol_16x16_reflector[]  
  
malrana@ip-10-70-175-254:/data/project/tsmc65/users/malrana/ws/m...  
File Edit View Search Terminal Help  
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/sim>la  
unch_k5_sim
```

וקיבלנו:

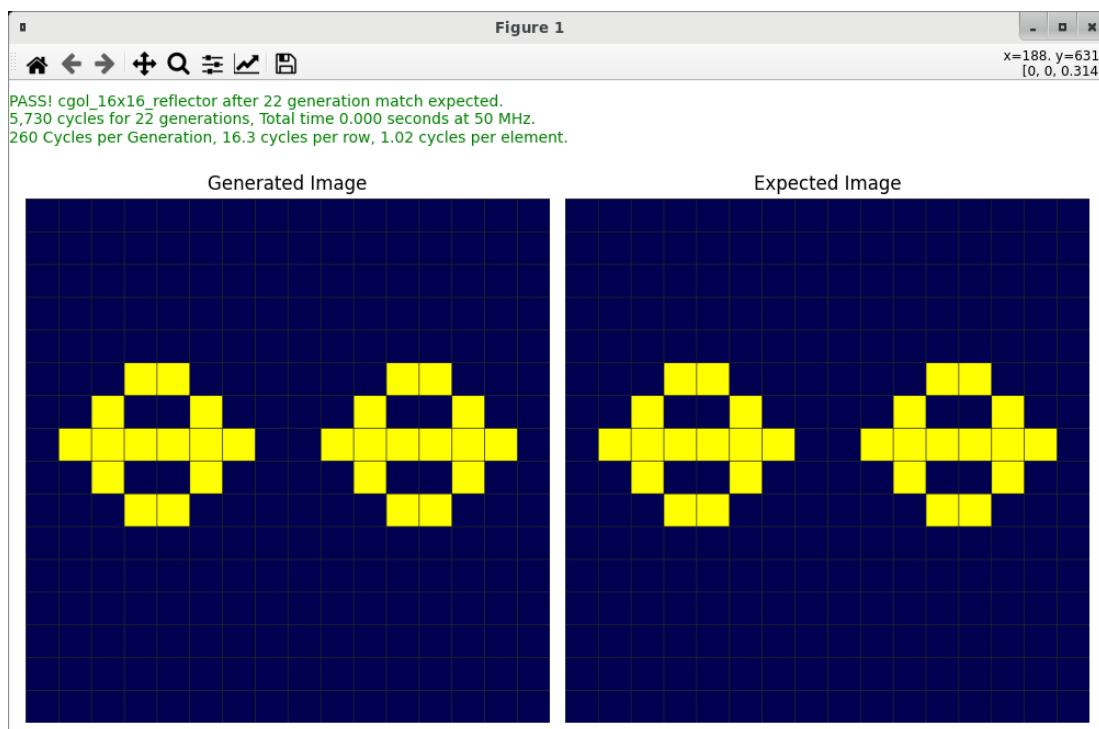


ניתן לראות שבריצת התוכנה חישוב כל ביט בודד לוקח 864 מחזורי שעון.

לאחר מכן הרצנו את החומרה עם הקוד שכתבנו למאיץ ה cgol:



וקיבלנו:



כעת, ניתן לראות שכאשר אנו מריצים את מאיץ החומרה, הוא מחשב כל ביט בתוך 1.02 מחזורי שעות, כלומר שיפרנו את זמן החישוב פי 847!

כעת, לאחר שהקוד רץ כמו שצריך, ביצענו בדיקת סינטזה כדי לוודא שהקוד סינטזבלי, וקיבלנו הערות שלא מזיקות:

```
malrana@ip-10-70-175-254:/data/project/tsmc65/users/malrana/ws/my_k5_proj/hw/xlrs/cgol_xlr
File Edit View Search Terminal Help
Thread 0 DONE quit app detected
No active thread
Server is Quitting
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/sim-cd SMY K5 XLR5
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/hw/xlrs-cd cgol_xlr/
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/hw/xlrs/cgol_xlr-qsyn_xlr cgol_xlr -all
Checking Synthesis ...
Done Synthesis ...

Total FPGA Logic Elements: 7,360
Total FPGA memory registers: 1,448
Total FPGA memory bits: 0
Info: Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 non-justified warnings
Please Check Report for following non-justified Warning IDs
[13024, 13410]

NOTICE! Your design include some possible justified warnings as:
"No output dependent on input pin"
"input pin(s) that do not drive logic"
Please Carefully review the report and make sure the specific reported unused inputs are justified

For more details see qsyn_output_files/cgol_xlr.map.rpt

Checking Fit ...

Info: Quartus Prime Fitter was successful. 0 errors, 0 non-justified warnings
For more details see qsyn_output_files/cgol_xlr.fit.rpt

Checking Timing (STA) ...

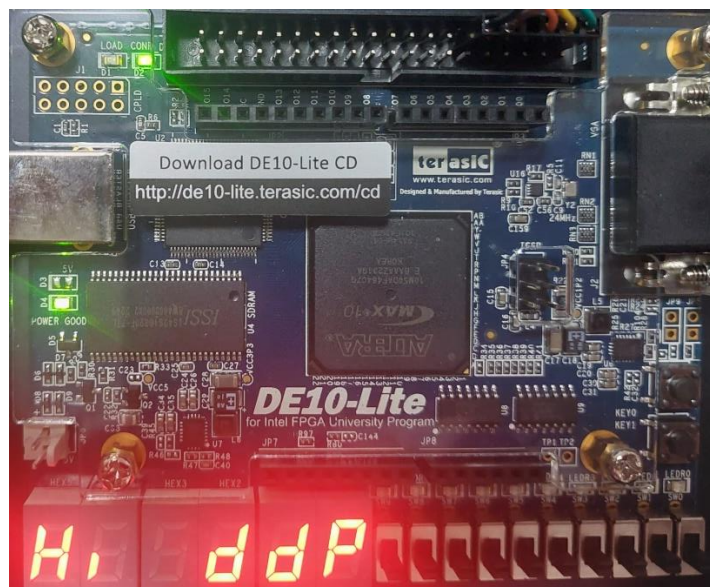
Info: Quartus Prime Timing Analyzer was successful. 0 errors, 0 non-justified warnings
Max FPGA Frequency 85.89 MHz

For more details see qsyn_output_files/cgol_xlr.sta.rpt
ip-10-70-175-254:malrana:/data/project/tsmc65/users/malrana/ws/my_k5_proj/hw/xlrs/cgol_xlr/
```

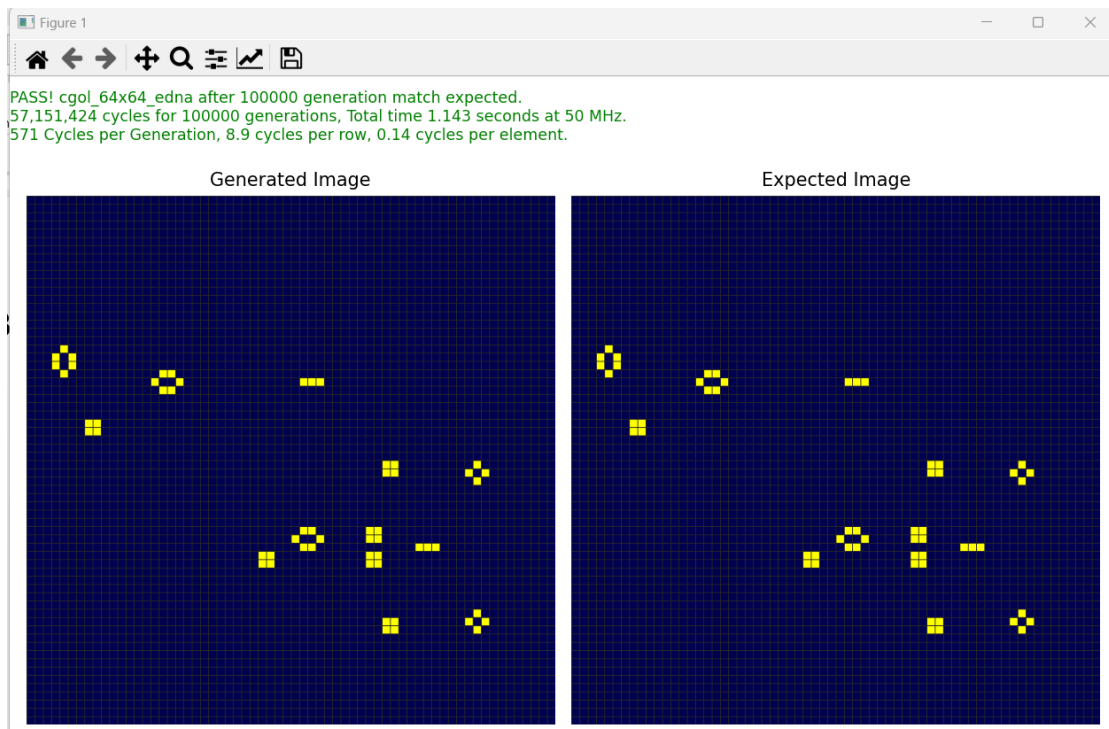
לבסוף הרצנו את הקוד על ה FPGA:

```
MINGW64/C:/USER/K5_xbox_env/K5_xbox_fpga_win/threads_runspace
$ prog_fpga cgol_xlr
Info: Warning Quartus Prime Programmer
Info: Version 24.1std.0 Build 1077 03/04/2025 SC Standard Edition
Info: Copyright (C) 2025 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and any partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus Prime License Agreement,
Info: the Altera IP License Agreement, or other applicable license
Info: agreement, including, without limitation, that your use is for
Info: the sole purpose of programming logic devices manufactured by
Info: Altera and sold by Altera or its authorized distributors. Please
Info: refer to the Altera Software License Subscription Agreements
Info: on the Quartus Prime software download page.
Info: Processing started: Sun Jun 29 23:28:53 2025
Info: Command: quartus_pgm -m jtag -q p:/C:/USER/K5_xbox_env/K5_xbox_fpga_win/fpga_prog_files/K5_xbox_cgol_xlr.sof
Info (213045): Using programming cable "USB-Blaster [USB-1]"
Info (213011): Using programming file c:/USER/K5_xbox_env/K5_xbox_fpga_win/fpga_prog_files/K5_xbox_cgol_xlr.sof with checksum 0x019291D6 for device 10M500AF48401
Info (209060): Started Programmer operation at Sun Jun 29 23:28:55 2025
Info (209018): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x03105000
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209062): Ended Programmer operation at Sun Jun 29 23:28:57 2025
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 4439 megabytes
Info: Processing ended: Sun Jun 29 23:28:57 2025
Info: Elapsed time: 00:00:04
Info: Total CPU time (on all processors): 00:00:00

MINGW64/C:/USER/K5_xbox_env/K5_xbox_fpga_win/threads_runspace (main)
$ launch_k5_app cgol_xlr -asl cpl_shared.lib -itr 100000 -gpv cgol_64x64.edna -ccd1 01SP/5
```



וקיבלנו:



כעת, זמן החישוב של ביט אחד הוא 0.14 מחזורי שעון, כלומר שיפרנו את זמן החישוב פי 7.3 מזמן החישוב של הרצת החומרה ללא FPGA, ופי 6183 מזמן החישוב של הרצת התוכנה!

