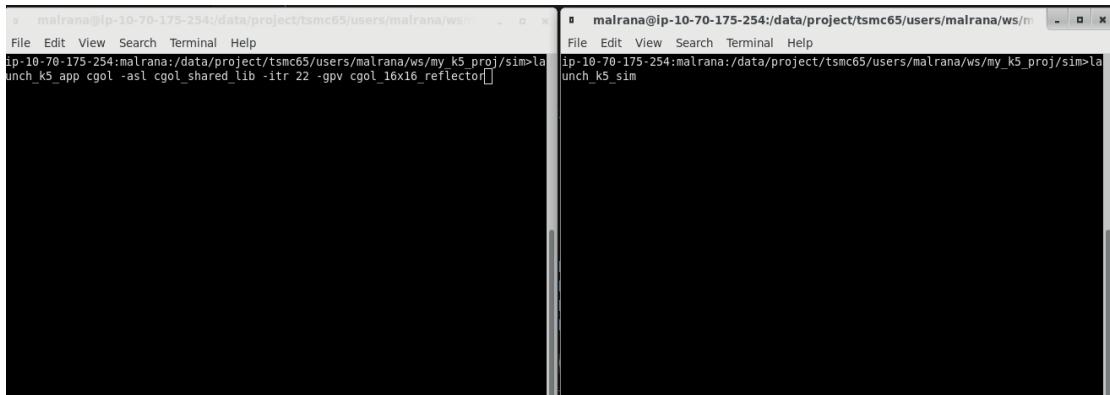


דוח סיכום – CGOL XLR DDP25

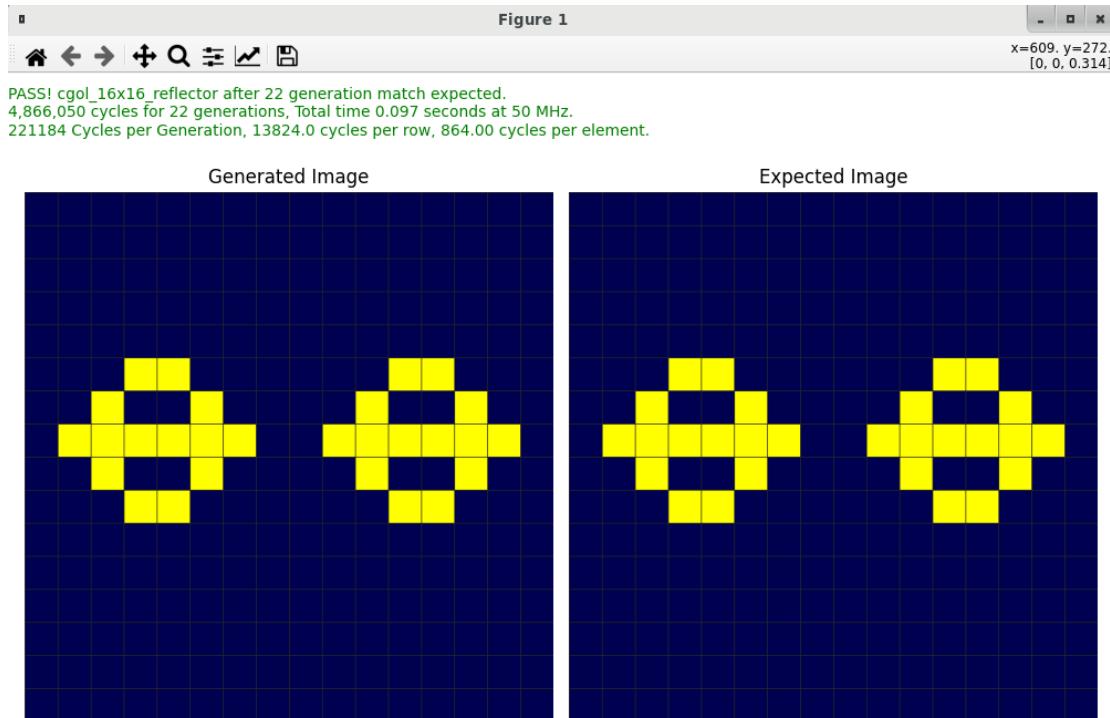
ראשית, התחלו בהריצה של התוכנה:



```
mairana@ip-10-70-175-254:/data/project/tsmc65/users/mairana/ws/my_k5_proj>sim>launch k5_app cgol -asl cgol shared_lib -itr 22 -gpv cgol_16x16_reflector[ ]
```

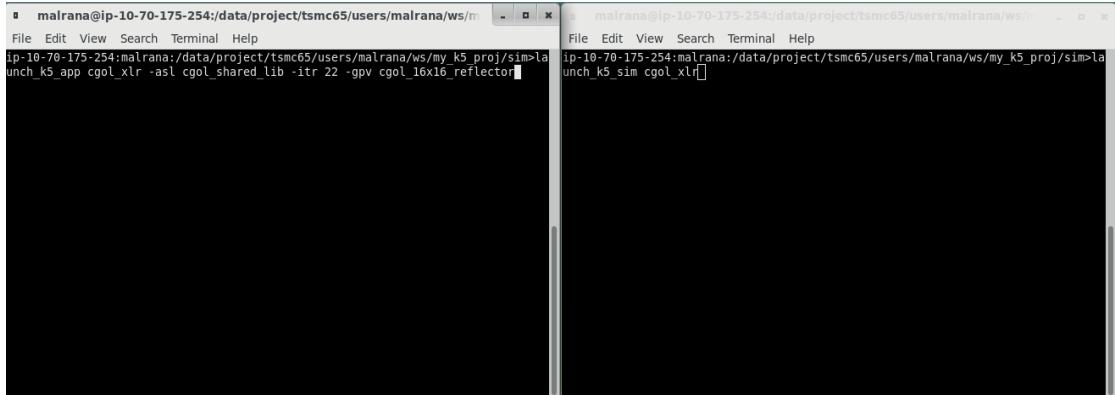
```
mairana@ip-10-70-175-254:/data/project/tsmc65/users/mairana/ws/my_k5_proj>sim>launch k5_sim
```

וליבלנו:

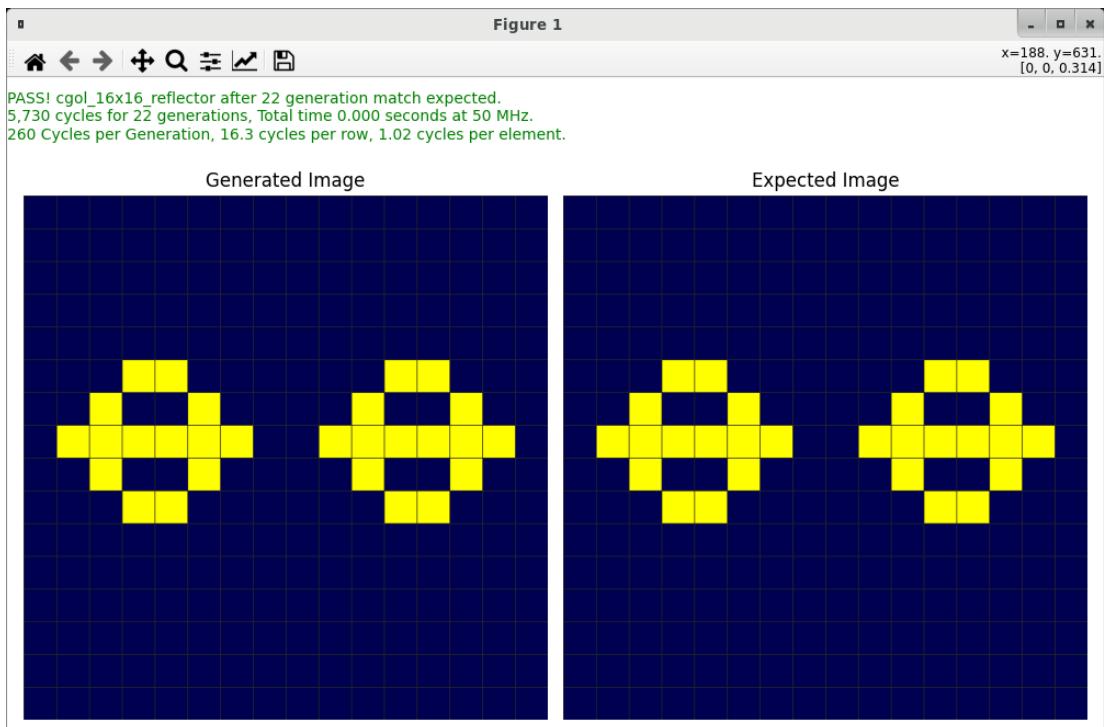


ניתן לראות שבריצת התוכנה חישב כל בית בודד לוקח 864 מחזורי שעון.

לאחר מכן הרצמו את החומרה עם הקוד שכתבנו למאיצ' ה `cgol`:



וקיבלנו:



כעת, ניתן לראות שכאשר אנו מרכיבים את מאיצ' החומרה, הוא מחשב כל בית בתוך 1.02 מillisecond!
שעון, כלומר שיפרנו את זמן החישוב פי 847!

כעת, לאחר שהקוד רץ כמו שצריך, ביצענו בדיקת סינטזה כדי לוודא שהקוד סינטטי, וקיבולם הערות שלא מזיקות:

```
#                                     mailrana@ip-10-70-175-254:/data/project/tsmc65/users/mailrana/ws/my_k5_proj/hw/xlsr/cgol_xlr
File Edit View Search Terminal Help
Thread 0 DONE quit_app detected
No active thread
Generating report...
ip-10-70-175-254:mailrana:/data/project/tsmc65/users/mailrana/ws/my_k5_proj$simcd SWV K5_XLRS
ip-10-70-175-254:mailrana:/data/project/tsmc65/users/mailrana/ws/my_k5_proj$hw/xlsr>cd cgol_xlr/
ip-10-70-175-254:mailrana:/data/project/tsmc65/users/mailrana/ws/my_k5_proj$hw/xlsr/cgol_xlr>qsyn_xlr_cgol_xlr -all
Checking Synthesis ...
done Synthesis ...

Total FPGA Logic Elements:    7,360
Total FPGA Memory registers:   1,448
Total FPGA Memory bits:       0
Info: Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 non-justified warnings
Please Check Report for following non-justified Warning IDs
13024, 13410

NOTICE! Your design include some possible justified warnings as:
  "No output depended on input"
  "Unused inputs can't drive logic"
Please Carefully review the report and make sure the specific reported unused inputs are justified

For more details see qsym_output_files/cgol_xlr.map.rpt

Checking Fit ...
Info: Quartus Prime Fitter was successful. 0 errors, 0 non-justified warnings
For more details see qsym_output_files/cgol_xlr.fit.rpt

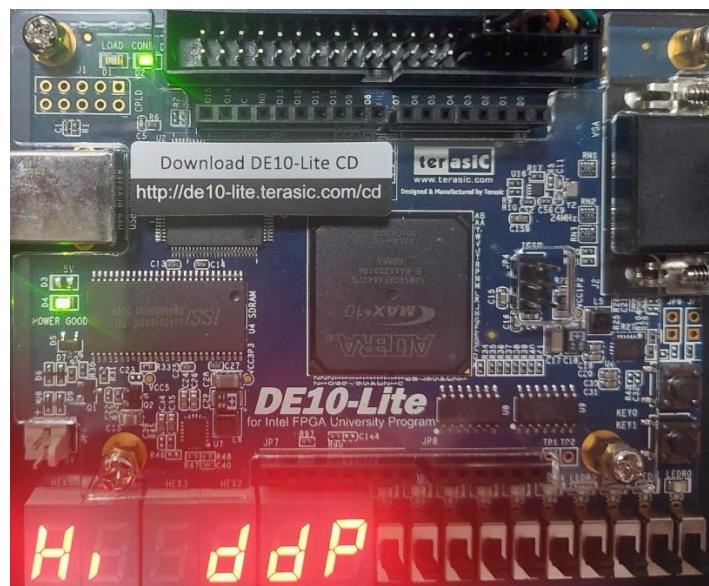
Checking Timing (STA) ...
Info: Quartus Prime Timing Analyzer was successful. 0 errors, 0 non-justified warnings
Max FPGA Frequency 85.89 MHz

For more details see qsym_output_files/cgol_xlr.sta.rpt
ip-10-70-175-254:mailrana:/data/project/tsmc65/users/mailrana/ws/my_k5_proj$hw/xlsr/cgol_xlr$
```

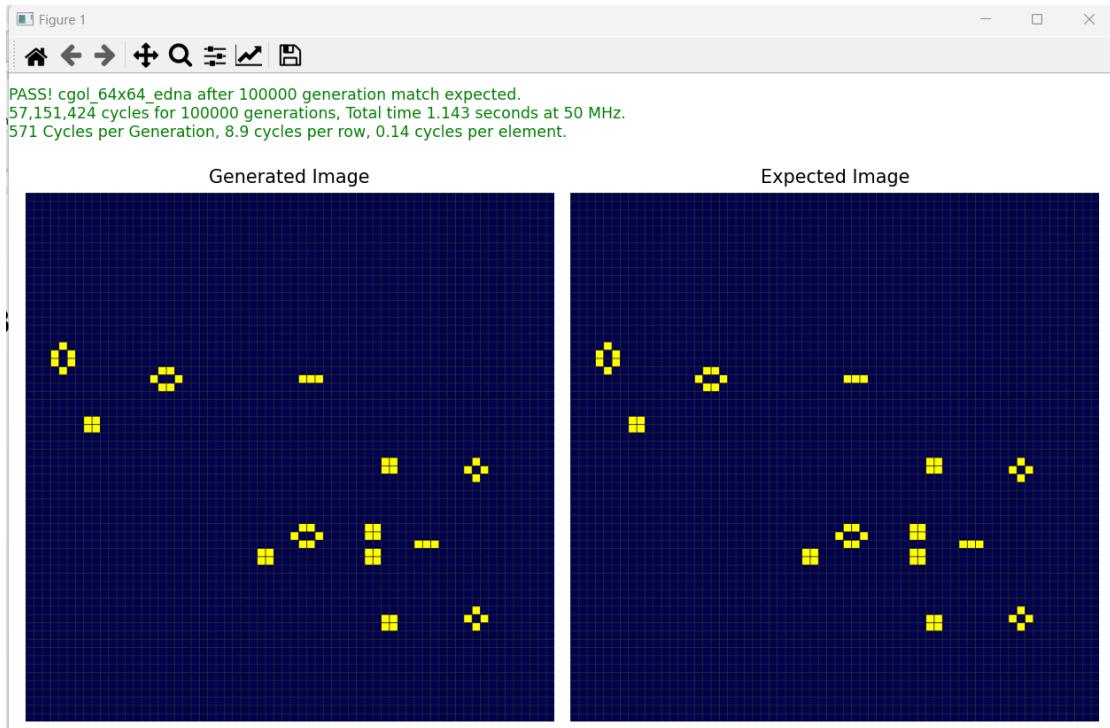
מגניב! הרכבתו את הקוד על ה-FPGA.

בסוף הרצינו את הקוד על ה-FPGA.

```
# MINGW64/c/USER/k5_xbox_env/k5_xbox_fpga_win/thread/runspace
$ prog_fpga_cgol_xlr
prog_fpga_cgol_xlr: ./prog_fpga_cgol_xlr -m main
Info: ****
Info: Running Quartus Prime Programmer
Info: Version 24.1std.0 Build 107 03/04/2025 SE Standard Edition
Info: Copyright (C) 2025 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and any partner logic
Info: functions, and any output files from any of the foregoing
Info: (the "Program"), except as expressly licensed to you in any
Info: associated documentation or information, are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus Prime License Agreement,
Info: the Altera® License Agreement or other applicable license
Info: for the Program, including its EULA and Terms of Use for the
Info: sole purpose of programming logic devices manufactured by
Info: Altera and sold by Altera or its authorized distributors. Please
Info: refer to the Altera Software License Subscription Agreements
Info: for more details.
Info: Quartus Prime Programmer version 24.1std.0
Info: Processing started: Sun Jun 29 23:28:53 2025
Info: Command: quartus_pgm -n jtag -o pyc:/USER/k5_xbox_env/k5_xbox_fpga_win/fpga_prog_files/k5_xbox_cgol_xlr.sof
Info: (211001) Using programming cable: USB-Blaster (USB)
Info: (211001) Using device: ALTERA DE10-Lite Evaluation Board(k5_xbox_fpga_win/fpga_prog_files/k5_xbox_cgol_xlr.sof) with checksum 0x019291D6 for device 10M50DAF4B401
Info: (209060): Started Programmer operation at Sun Jun 29 23:28:55 2025
Info: (209016): Configuring device index 1
Info: (209017): device 1 contains JTAG ID code 0x03105000
Info: (209011): Configuration of device index 1 completed
Info: (209011): Successfully performed operations()
Info: (209011): Ended Programmer operation at Sun Jun 29 23:28:57 2025
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
Info: Peak Virtual memory: 4459 pages
Info: Total CPU time (on all processors): 00:00:00
Info: Elapsed time: 00:00:04
Info: Total CPU time (on all processors): 00:00:00
$ launch_k5_app cgol_xlr -as1 cgol_shared_lib -itr 100000 -gpv cgol_64x64_edna -ccdi D1SP7s
```



אנו יכולים:



כעת, זמן החישוב של בית אחד הוא 0.14 ממחזורי שעון, כלומר שיפרנו את זמן החישוב פי 7.3 מזמן החישוב של הריצת החומרה ללא FPGA, ופי 6183 מזמן החישוב של הריצת התוכנה!

