Embedded System Design Assignment

Jahnvi Dua

IEC2019106

Objective: Progress report of 32-bit processor design.

IF stage code:

```
Module mux(input[31:0]in,
            input[15:0]branch,
            input pcsrc,
            output reg[31:0]out);
always @(pcsrc)
  begin
  if(pcsrc == 0)
     out<=in
   else
    out<= branch;
   end
endmodule
//////////////////////////////////////////////
module add4(input [31:0]in,
             input reset,
             output reg[31:0]out);
always @(*)
begin
if(reset)
```