Exam Date & Time: 17-May-2022 (10:00 AM - 01:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, MAY 2022

PARALLEL COMPUTER ARCHITECTURE AND PROGRAMMING [CSE 3252]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates:
Answer ALL questions.
Missing data may be suitably assumed

1) A) Write an efficient MPI program to read matrix *A* of size 4*x*4. It produces a resultant matrix *RES* of size 4*x*4 by adding every row element of *A* with a key value. The key value for the first row is the product of elements in the last row and the key value for remaining row is the product of the elements from the previous row of matrix *A*. Use 4 processes (including root) to solve this problem. **Use only collective communication routines except MPI_Bcast.** (4)

Sample I/O:

A

1 1 1 1
2 2 2 2
3 3 3 3
1 2 1 2

Res

5 5 5 5
3 3 3 3
19 19 19 19
82 83 82 83

B) With a neat diagram explain the architecture of a modern GPU. (3)

C) With the diagrams, explain the computer architectures that deal with Multiple Data streams. (3)

2) A) Explain the following parallel computer structures:
i. Pipeline computer
ii. Array computer
iii. Multiprocessor systems (4)

B) Illustrate the concept of rank and communicator in MPI. (3)

C) What type of memory model that has been adopted in MPI? What are the advantages of it? (3)

3) Explain the following with respect to OpenCL.

A) i. Platform and platform model
ii. Context
iii. global_work_size
iv. local_work_size (4)

B) Show how the threads collaboratively load M and N elements into the shared memory before they individually use these elements in their dot product calculation. Show the activities performed in execution phases of a tiled matrix multiplication kernel by dividing the input matrices M and N into 2x2 tiles. Here M and N are 4*4 Matrices. (3)

Note: Do not write kernel function.

C) Write an OpenCL kernel to implement parallel selection sort to sort an Integer input array of size N in ascending order. (3)

4) Write a kernel program in CUDA for tiled convolution using the following mask. Use constant memory wherever applicable.

A) 3 2 1

2 4 6

3 2 1 (4)

B) Assume a kernel function ***findSoln*** which is launched as follows.

dim3 a(140,120,1); dim3 b(15,8,3); FindSoln< < < a,b>>>(...);

Determine how many blocks are preceding a thread with global id 10000. Also, determine how many threads are succeeding a thread with global id 10000. Show clearly the steps. (3)

C) What is CGMA? Explain the importance of CGMA. Calculate CGMA for the vector-vector addition kernel. (3)

5) How sparse matrix multiplication can be improved using CSR technique? Write and explain parallel sparse matrix multiplication kernel code using CSR technique. (4)

A)

B) The following function prototype is used for 1D parallel convolution kernel. Mention the method which changes this prototype to improve the performance by utilizing the cache memory? Explain it with the required code snippet including the kernel. (3)

__global__ void convolution_1D_basic_kernel(float *N, float *M, float *P, int Mask_Width, int Width);

C) Consider an integer matrix of size MxN. The integers can be positive, negative or zero. Write a CUDA kernel function to count the number of positive, negative and zero elements in the matrix. Show the kernel launch configuration. (3)

-----End-----