Design of Low Power NXN Magnitude Comparator Using GDI Technique

Students:

Donia Yasin #1201831

Klarein Wassaya #1210279

Aseel Assi #1211974

Instructor:

Dr. Khader Mohammad

Affiliation:

Birzeit University- Faculty of Engineering and Technology- Department of Electrical and Computer Engineering- Digital integrated circuits - ENCS3330.

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Abstract

Design for Low power, high speed and reliable design is a very important role in emerging technologies in Integrated circuit. To reduce power consumption and propagation delay involved in the circuit, the paper presents GDI technique for implementation of digital logic circuit. In this paper, 1, 2, 4, 8 bits magnitude comparator is designed using conventional CMOS logic style and GDI technique. The proposed GDI magnitude Comparator requires 14 transistors for 1 bit and implementation using CMOS logic requires 226 transistors. The power consumed by the NXN-bit magnitude comparator using the conventional CMOS technique is 114.3 μW, whereas the power consumed by the NXN-bit magnitude comparator using the GDI technique is 77.0162 μW, which is significantly lower compared to the conventional CMOS style. The delay present in the conventional CMOS magnitude comparator is 29.75 ns, whereas the delay produced by the GDI technique for the magnitude comparator is 1.27205 ns. The delay is also substantially reduced in the proposed GDI technique. Thus, the proposed GDI technique shows approximately 32.62% efficiency in power measurement. All this circuit simulation is done by using ELECTRIC TOOL EDA version 9.07 at 300nm process technology.

1. Introduction

Gate Diffusion Input (GDI) is a novel technique for designing low-power digital combinatorial circuits. This approach significantly reduces power consumption, propagation delay, and the area of digital circuits while maintaining a low complexity of logic design. The GDI technique leverages the inherent advantages of transistors, such as small mechanical sensitivity, no power consumption by the cathode heater, fast switching, long life, low cost, and compact size, making them suitable for small signal applications.

Transistors have revolutionized communication and design devices, making them more practical and efficient. In our project, we utilized transistors in both schematic and layout designs to implement a magnitude comparator. Our design aimed to build a comparator in four stages using the GDI technique: 1-bit comparator, 2-bit comparator, 4-bit comparator, and 8-bit comparator.

The construction process was hierarchical: the 8-bit comparator was built from two 4-bit comparators, the 4-bit comparator from two 2-bit comparators, and the 2-bit comparator from two 1-bit comparators. Additionally, we designed 3-input AND gates and 2-input OR gates using the same GDI technique. While there are multiple methods to build a comparator, we focused on optimizing for low power consumption and minimal area.

This project demonstrates the effectiveness of the GDI technique in designing digital circuits with enhanced performance metrics.

2. Specifications

GDI Technique:

In Basic GOI cell, there is three input G (Common gate input of nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source/drain of pMOS). The Substrate of both nMOS and pMOS are connected to N or P (respectively).

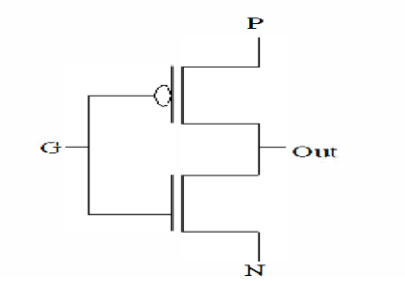

Figure 1:Basic GDI cell

Design Specifications:

1. 1-Bit Comparator:

   The truth table is:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

   The logical expressions for each output can be expressed as follows:

   A > B: AB'

   A < B: A'B

   A = B: A'B' + AB

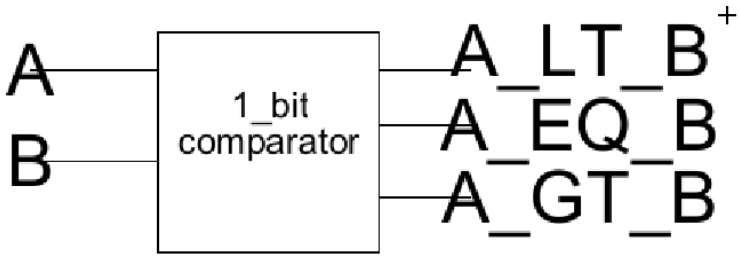

Figure 2: 1-Bit Comparator Block Diagram

2. 2- Bit Comparator:

The truth table is:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

The logical expressions for each output can be expressed as follows:

A > B: A1B1’ + A0B1’B0’ + A1A0B0’

A = B: A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’

: A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)

: (A0B0 + A0’B0’) (A1B1 + A1’B1’)

: (A0 Ex-Nor B0) (A1 Ex-Nor B1)

A < B: A1’B1 + A0’B1B0 + A1’A0’B0

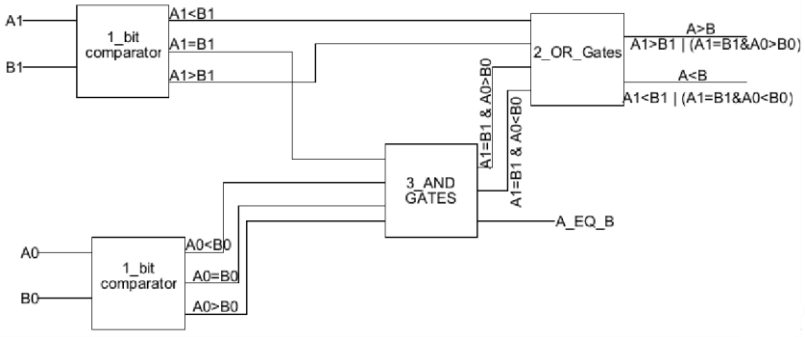

Figure 3: 2-Bit Comparator Block Diagram

3. 4-Bit Comparator:

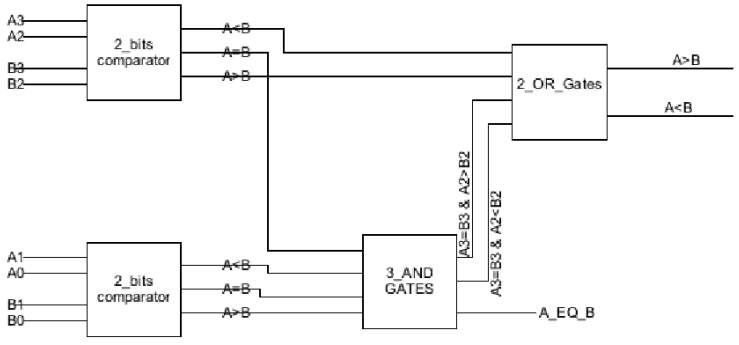

Figure 4: 4-Bit Comparator Block Diagram

4. 8-Bit Comparator:

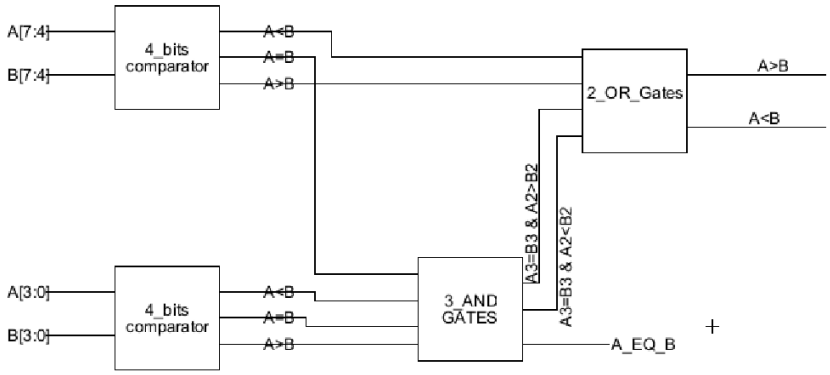

Figure 5: 8-Bit Comparator Block Diagram

5. we constructed the 2-input OR using GDI technique:
   Schematic:

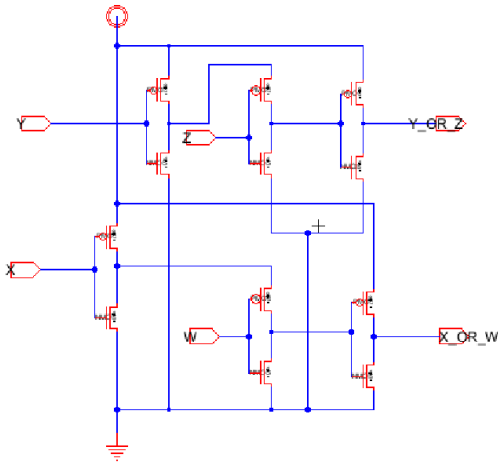

Figure 6: 2-input OR Schematic

Layout:

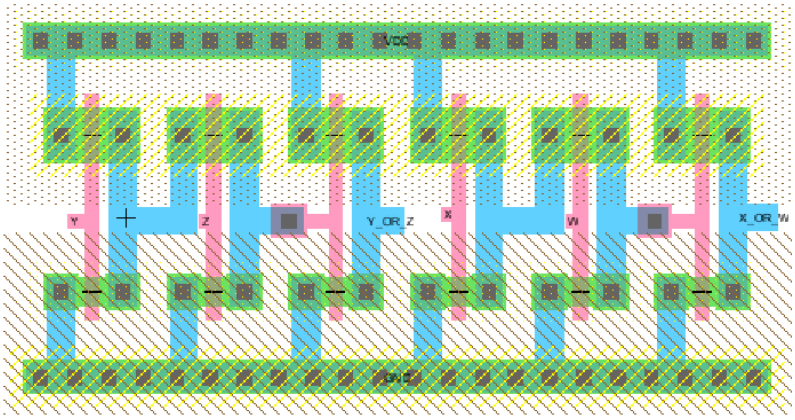

Figure 7: 2-input OR Layout

6. we constructed the 3-input AND using GDI technique:
   Schematic:

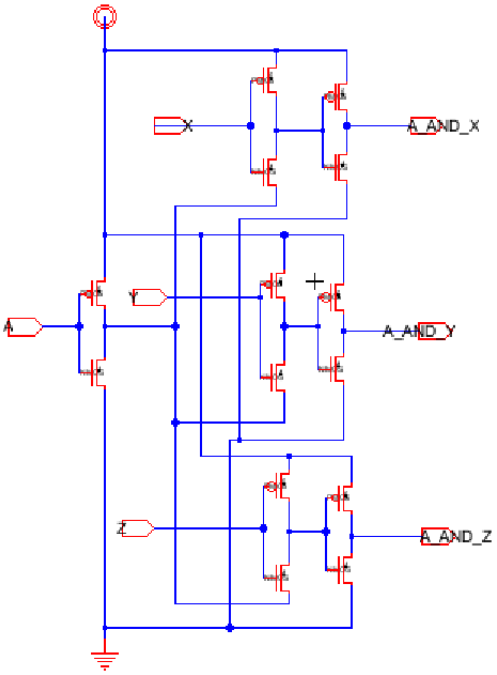

Figure 8: 3-input AND Schematic

Layout:

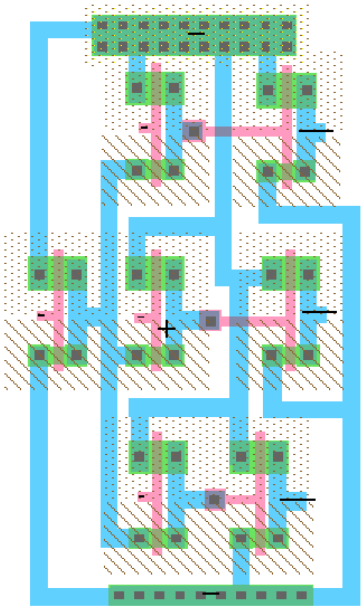

Figure 9: 3-input AND Layout

4. Proposed Design

We used 300 nm technology in our whole project, so the width for NMOS will be 4µm, the width for PMOS will be 8µm and the length for both will be 2µm.

The schematic diagram of the 1-, 2-, 4- and 8-bits comparator shows the utilization of transistors to achieve the required logic operations for comparing two input bits, A and B. The GDI technique simplifies the design by reducing the number of transistors needed, which in turn minimizes power consumption and propagation delay. The outputs A>B, A=B, and A<B are clearly delineated in the schematic, indicating the successful implementation of the comparator logic.

The layout diagram illustrates the physical implementation of the 1-, 2-, 4- and 8-bit comparator on a silicon chip. The use of GDI technique is evident in the compact and efficient arrangement of transistors. The design ensures minimal area usage, which is crucial for scaling the comparator to higher bit widths. The reduced area not only conserves silicon real estate but also contributes to lower parasitic capacitances, further enhancing the performance of the comparator.

1. 1-Bit Comparator:
   Schematic:

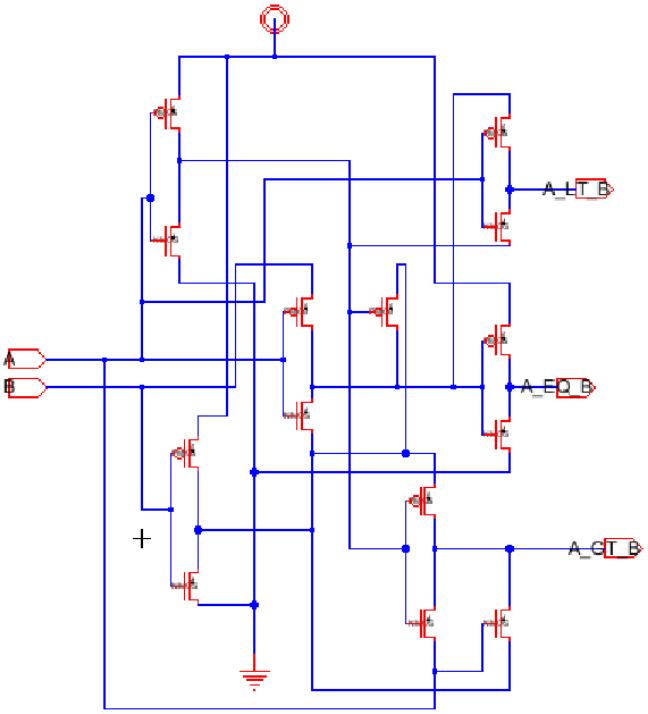

Figure 10: 1-Bit Comparator Schematic

   Layout:

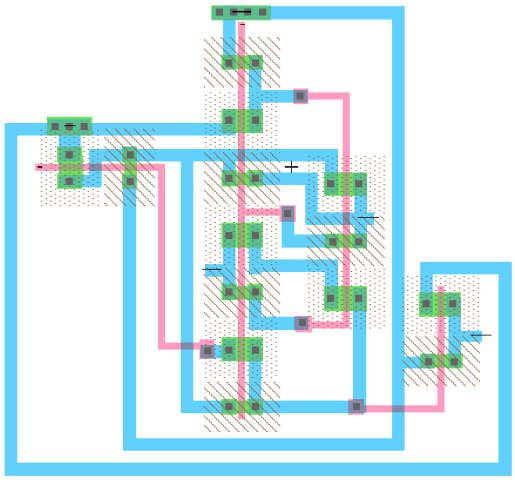

Figure 11: 1-Bit Comparator Layout

2. 2-Bit Comparator:
   Schematic:

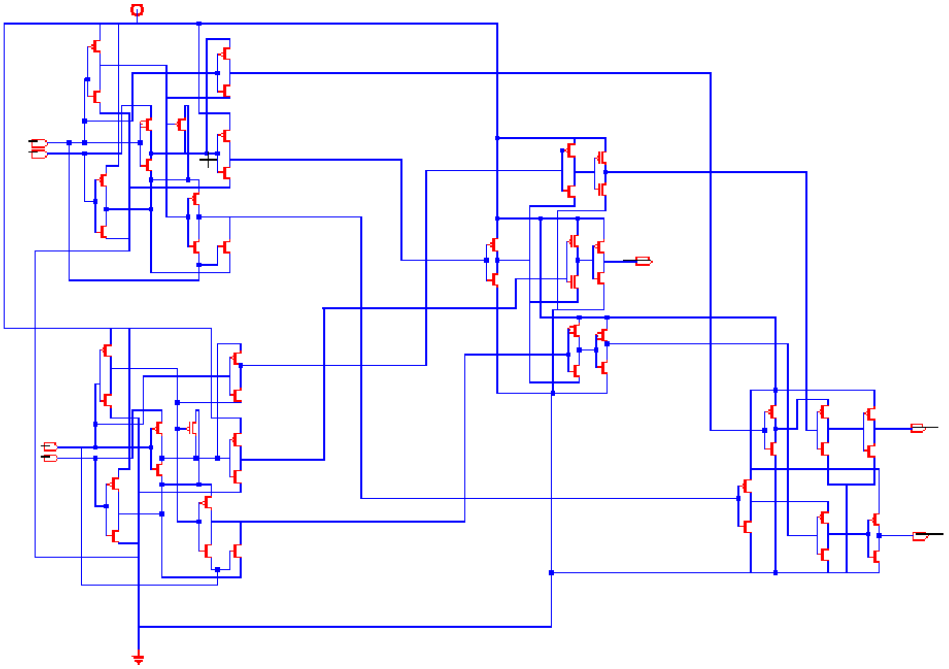

Figure 12: 2-Bit Comparator Schematic

   Layout:

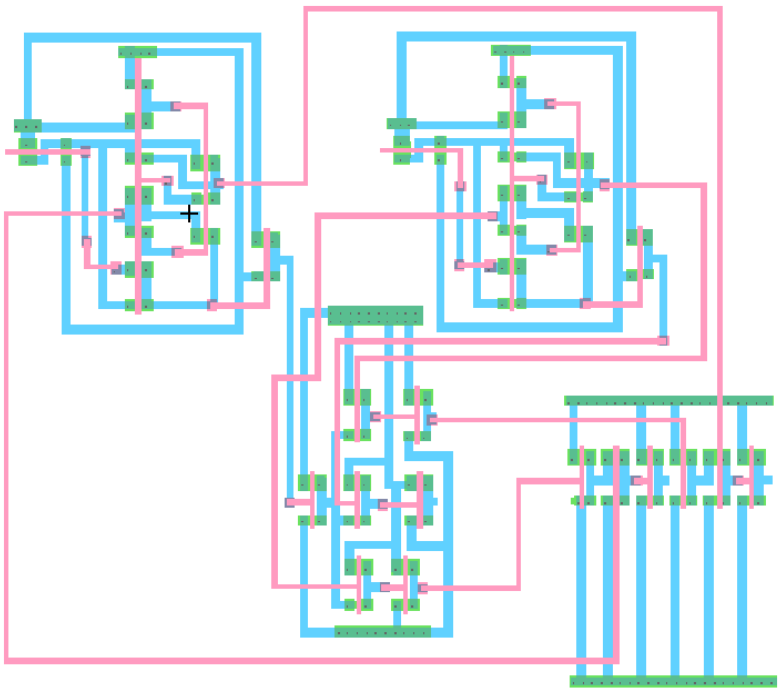

Figure 13: 2-Bit Comparator Layout

3. 4-Bit Comparator:
   Schematic:

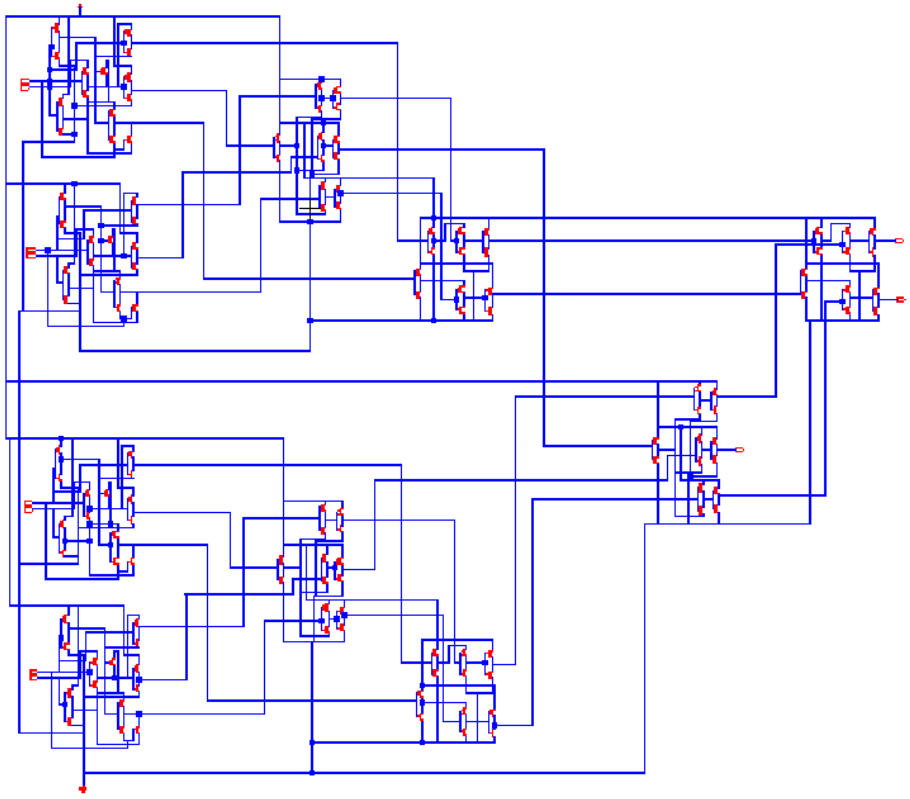

Figure 14: 4-Bit Comparator Schematic

Layout:

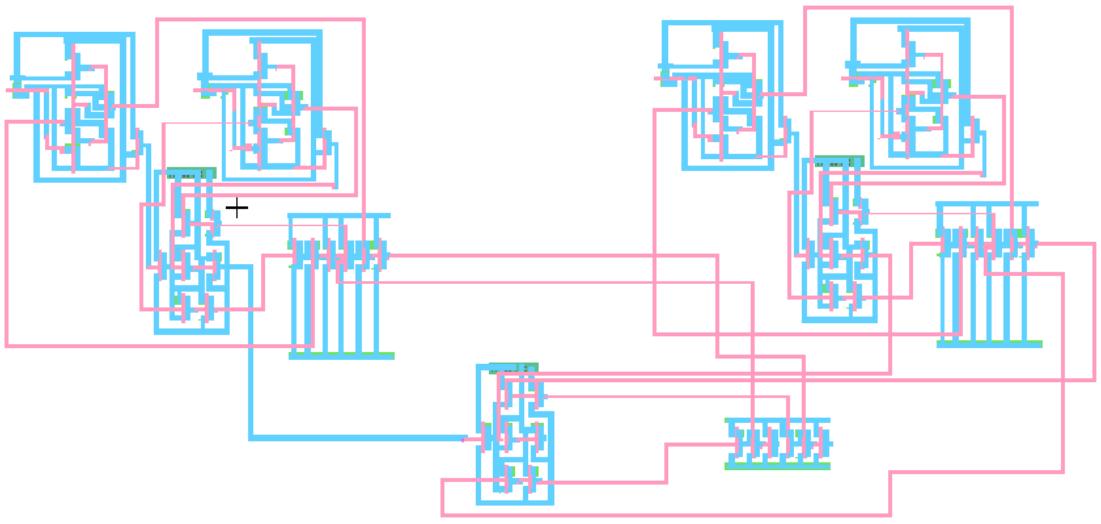

Figure 15: 4-Bit Comparator Layout

4. 8-Bit Comparator:
   Schematic:

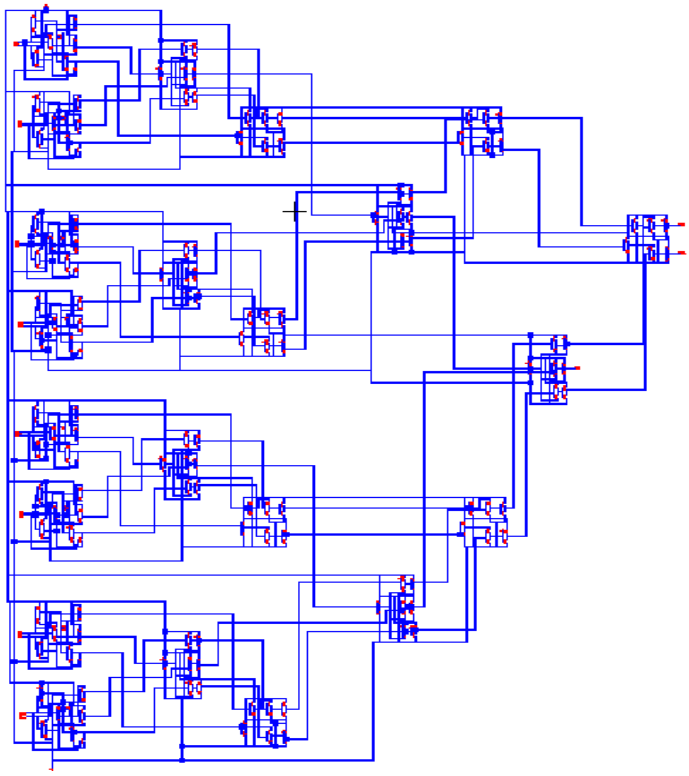

Figure 16: 8-Bit Comparator Schematic

Layout:

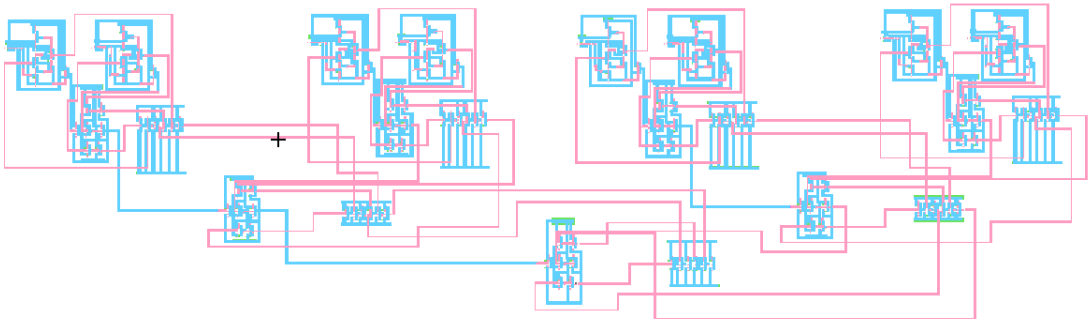

Figure 17: 8-Bit Comparator Layout

5. Results

Simulation Results:

1. 1-Bit Comparator:

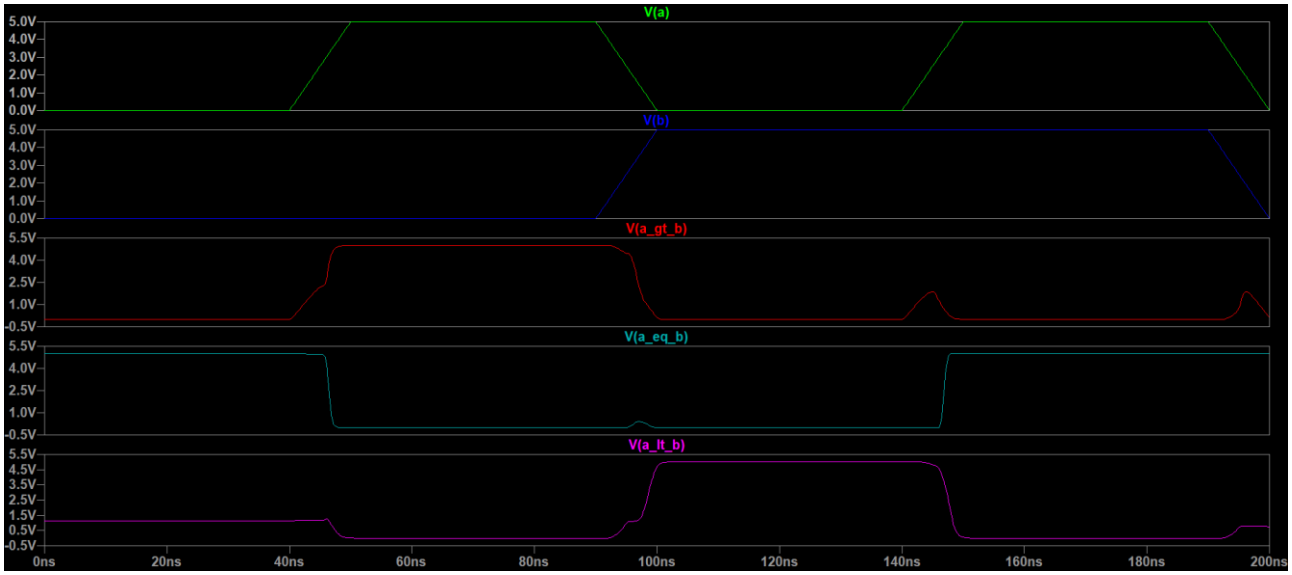

Figure 18: 1-Bit Comparator simulation

2. 2-Bit Comparator:

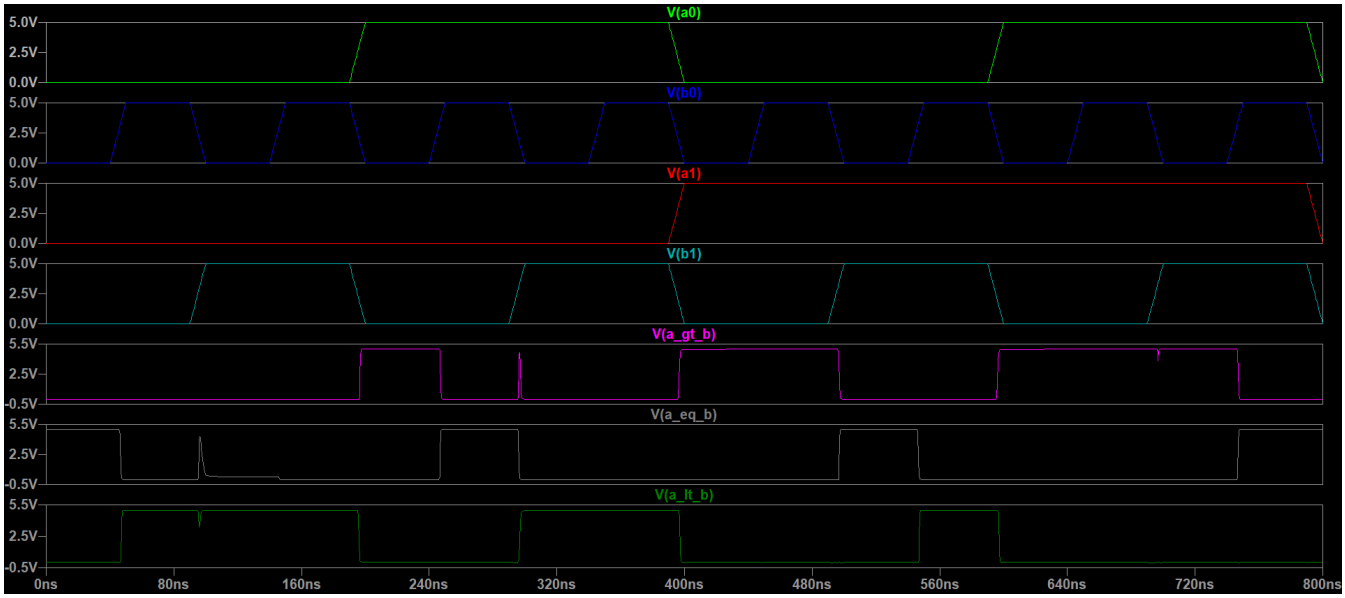

Figure 19: 2-Bit Comparator simulation

2. 4-Bit Comparator:

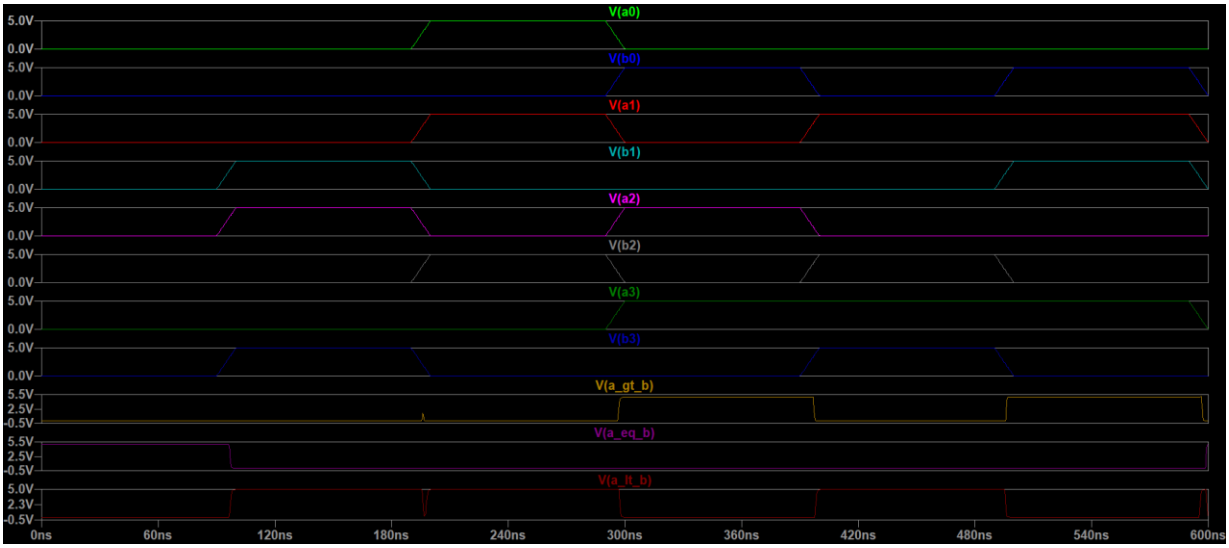

Figure 20: 4-Bit Comparator simulation

3. 8-Bit Comparator:

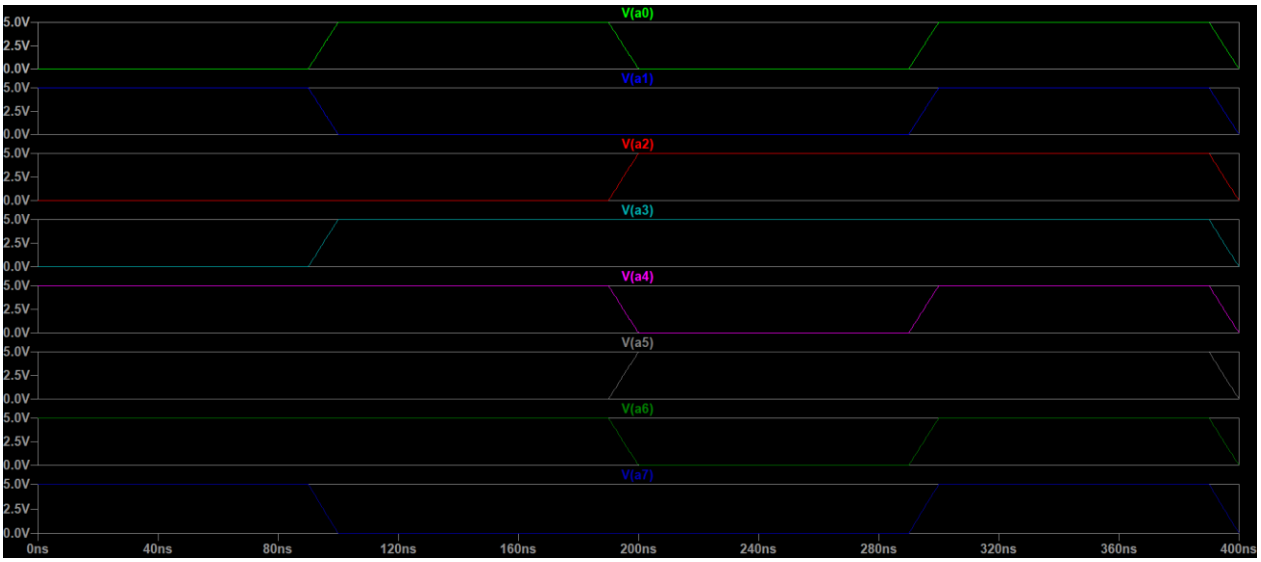

Figure 21: 8-Bit Comparator simulation-input A

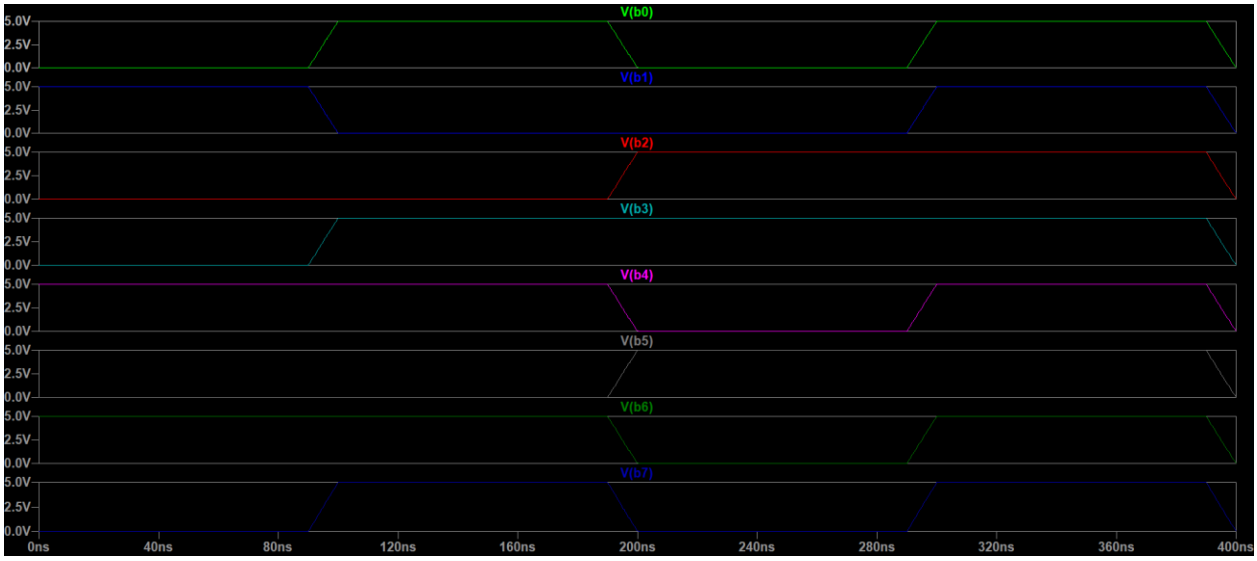

Figure 22: 8-Bit Comparator simulation-input B

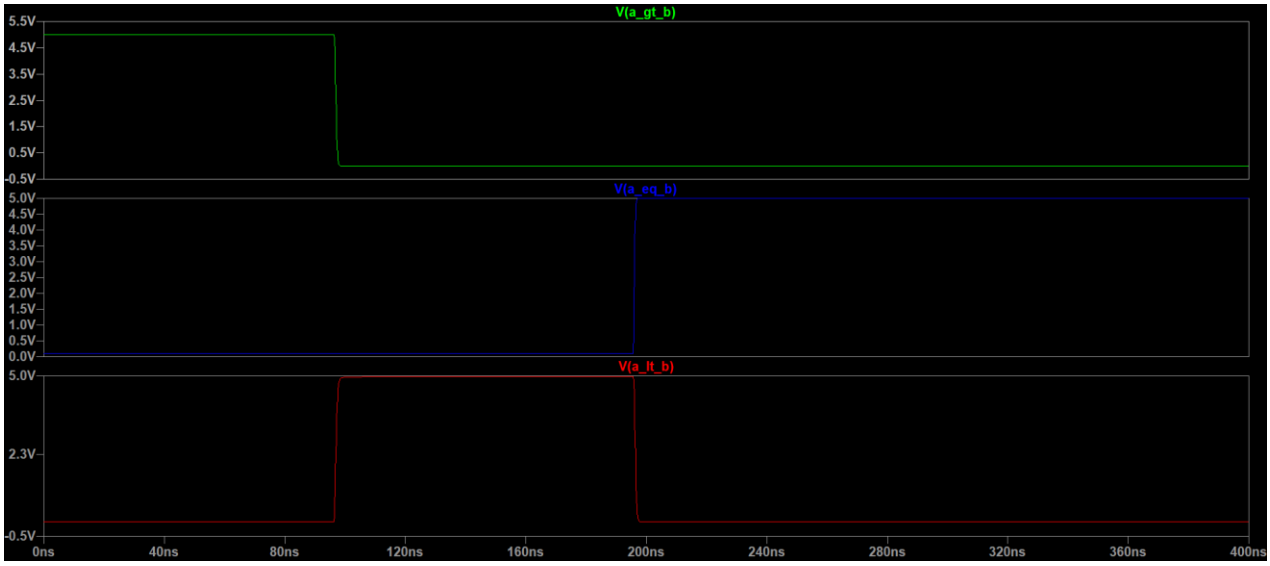

Figure 23: 8-Bit Comparator simulation

The 8-bit comparator simulation results (Figures 21, 22, and 23) underscore the scalability and efficiency of the GDI technique. The performance metrics are particularly noteworthy. The average power consumption for the 8-bit comparator using the GDI technique is 77.0162 microwatts, significantly lower than the 114.3 microwatts consumed by the CMOS-based design. Furthermore, the GDI-based 8-bit comparator exhibits an average delay of 1.27205 nanoseconds, which is substantially lower than the 29.75 nanoseconds delay of the CMOS design. The hierarchical design of the GDI comparator ensures minimal area usage, maintaining compactness even at higher bit-widths. When comparing the GDI technique to traditional CMOS logic, the advantages are clear: GDI-based designs consume significantly less power, making them ideal for energy-sensitive

applications; they have reduced propagation delay, enhancing the speed of the comparators, which is critical for high-performance computing tasks; and their compact layout ensures efficient use of silicon real estate, allowing for more functionality within a limited space.

7. Conclusion

In this project, we have successfully designed and implemented NXN magnitude comparators using the Gate Diffusion Input (GDI) technique. The key findings of our research demonstrate the significant advantages of the GDI technique in terms of power consumption, propagation delay, and area efficiency. The 1-bit, 2-bit, 4-bit, and 8-bit comparators were designed and simulated, showing consistent improvements over traditional CMOS designs. Specifically, the GDI-based 8-bit comparator exhibited an average power consumption of 77.0162 microwatts and an average delay of 1.27205 nanoseconds, compared to 114.3 microwatts and 29.75 nanoseconds for the CMOS-based design. These results highlight the potential of the GDI technique for low-power and high-speed digital circuit applications.

Future research can focus on further enhancing the comparator design by utilizing smaller technology nodes. As semiconductor technology advances, scaling down to smaller geometries can provide even greater reductions in power consumption and delay while maintaining or improving area efficiency. Additionally, exploring the integration of the GDI technique with other low-power design methodologies and advanced materials could lead to further performance gains. Investigating the robustness of GDI-based comparators in various operating conditions and their applicability in diverse digital systems can also be valuable areas for future work.

8.References

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