-- Company:

-- Engineer:

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-- Create Date: 02/28/2024 07:08:56 PM

-- Design Name:

-- Module Name: PBdebounce - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity ASM is

Port ( x : in STD\_LOGIC\_VECTOR (7 downto 0);

sqrt : out STD\_LOGIC\_VECTOR (7 downto 0);

clk : in STD\_LOGIC;

reset : in STD\_LOGIC;

S : in STD\_LOGIC);

end ASM;

architecture Behavioral of ASM is

type state\_type is (T0, T1, T2,T3,T4,T5);

signal current\_state, next\_state :state\_type ;

signal q, a, d : std\_logic\_vector(7 downto 0) := (others => '0');

signal temp : std\_logic\_vector (7 downto 0);

begin

state\_register : process( CLK, Reset)

begin

if(Reset = '1') then

current\_state <= T0;

elsif (CLK'event and CLK = '1') then

current\_State <= next\_state;

end if;

end process ;

next\_state\_process : process( S, current\_State)

begin

case current\_state is

when T0 => next\_state<=T1;

when T1 =>

if(s='0') then

next\_State<=T1;

else

next\_state<=T2;

end if;

when T2 =>

next\_State<=T3;

when T3 =>

if(q>a) then

next\_state<=T4;

else

next\_state<=T2;

end if;

when T4 => next\_State<=T5;

when T5 =>next\_State<=T1;

end case;

end process;

output\_process : process( CLK)

begin

if(CLK'event and CLK = '1') then

case current\_state is

when T0 => sqrt<="00000000";

when T1 =>

if(s='1') then

a<=x;

q<="00000001";

d<="00000011";

end if;

when T2 => q<=q+d;

when T3 => d<=d+2;

--when T4 => temp <= d srl 1;

when T5 => sqrt<=d-1;

when others => sqrt<="00000";

end case;

end if;

end process ;

end Behavioral;

TESTBENCH:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity testbench is

-- Port ( );

end testbench;

architecture Behavioral of testbench is

component design is

Port ( x : in STD\_LOGIC\_VECTOR (7 downto 0);

sqrt : out STD\_LOGIC\_VECTOR (7 downto 0);

clk : in STD\_LOGIC;

reset : in STD\_LOGIC;

S : in STD\_LOGIC);

end component;

signal x : STD\_LOGIC\_VECTOR (7 downto 0);

signal sqrt : STD\_LOGIC\_VECTOR (7 downto 0);

signal clk : STD\_LOGIC;

signal reset : STD\_LOGIC;

signal S : STD\_LOGIC;

begin

uut :design

Port map ( x ,

sqrt ,

clk ,

reset ,

S );

clk\_gen:process

begin

clk<='0';

wait for 2ns;

clk<='1';

wait for 2ns;

end process;

p1: process

begin

reset <= '0';

S<='0';

x<="00000000";

innerloop:for j in 0 to 255 loop

wait for 5ns;

x<=x+1;

S<='1';

wait for 124ns;

s<='0';

wait for 124ns;

end loop ;

Reset<='1';

x<="00010000";

wait for 124 ns;

x<="00000001";

wait for 124 ns;

end process p1;

end Behavioral;

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--library UNISIM;

--use UNISIM.VComponents.all;

entity PBdebounce is

Port ( PB\_out : out STD\_LOGIC;

PB\_in : in STD\_LOGIC;

clk : in STD\_LOGIC);

end PBdebounce;

architecture Behavioral of PBdebounce is

signal max: integer :=1000000;

signal count: integer :=0;

signal old:std\_logic:='0';

signal ton:std\_logic:='0';

signal pb\_debounce:std\_logic:='0';

begin

pro1 : process(clk)

begin

if(CLK'event and CLK = '1') then

if(ton='0') then

if (PB\_in /= old)then

ton<='1';

count<=0;

old<=PB\_in;

PB\_debounce<= not PB\_debounce;

end if;

end if;

else

count<=count+1;

if(count=max)then

ton<='0';

end if;

end if;

pb\_out<=PB\_debounce;

end process;

end Behavioral;