Tutorial 2

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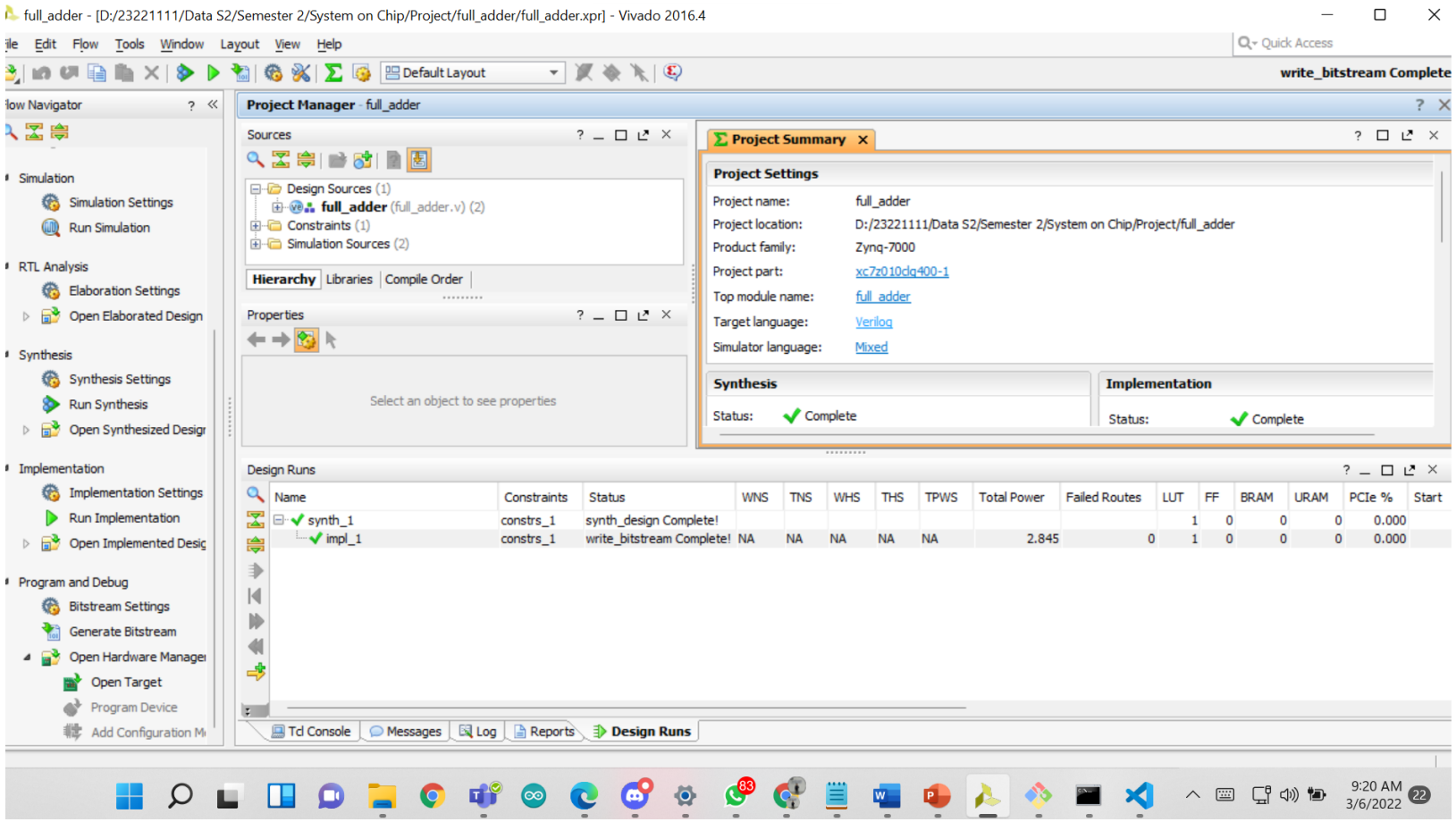
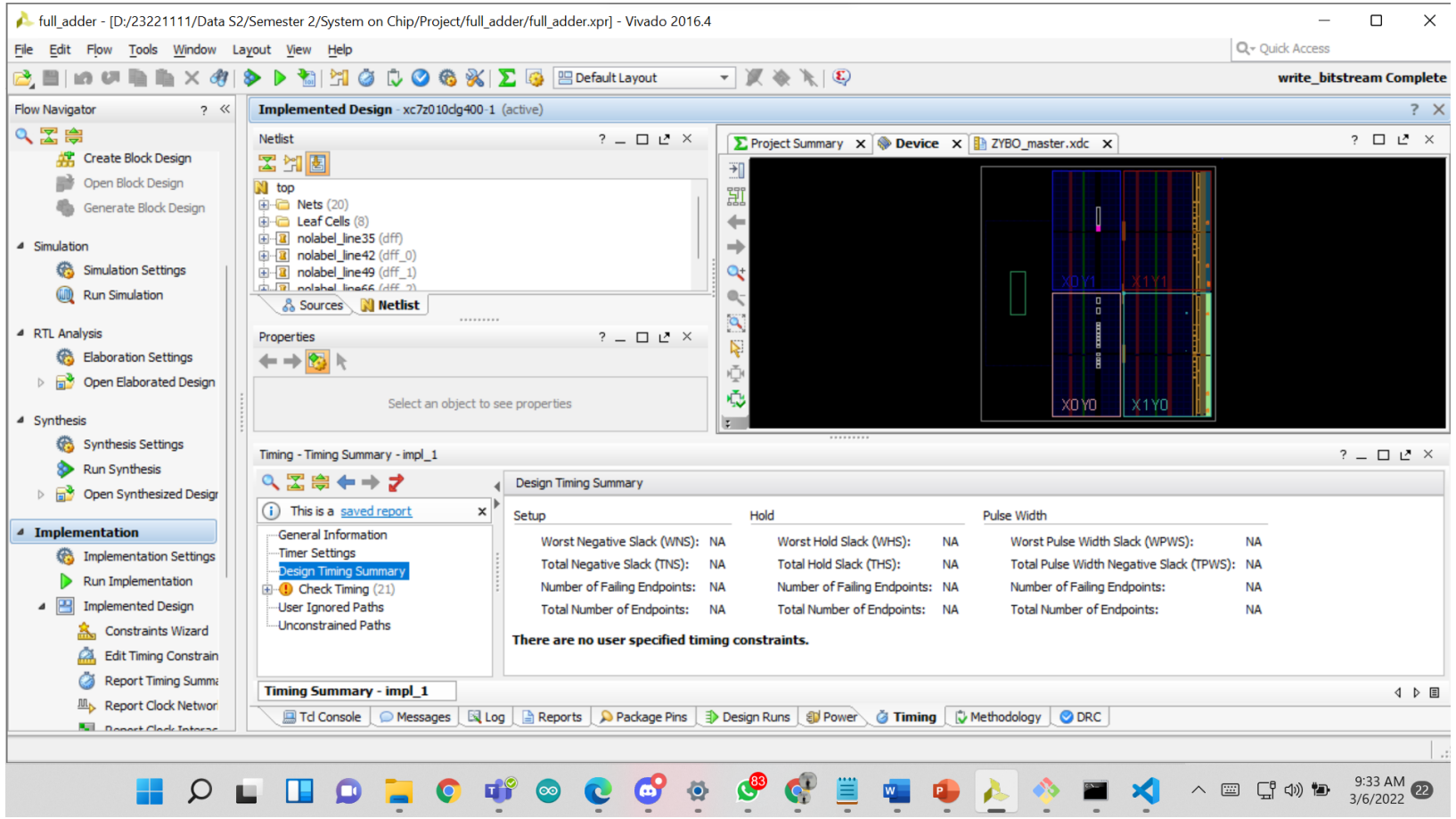
23221111

Lanjutan Tutorial Modul 1



Open Implementated Design



full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4

File Edit Flow Tools Window Layout View Help

Quick Access

Default Layout

Synthesis Complete

Flow Navigator

- Elaboration Settings
- Open Elaborated Design
- **Synthesis**
  - Synthesis Settings
  - Run Synthesis
  - Synthesized Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Set Up Debug
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design

Synthesized Design - xc7z010clg400-1 (active)

Net...

top
- Nets (20)
- Leaf Cells (8)
- nolabel_line35 (dff)
- nolabel_line42 (dff_
- nolabel_line49 (dff_
- nolabel_line66 (dff_
- nolabel_line73 (dff_

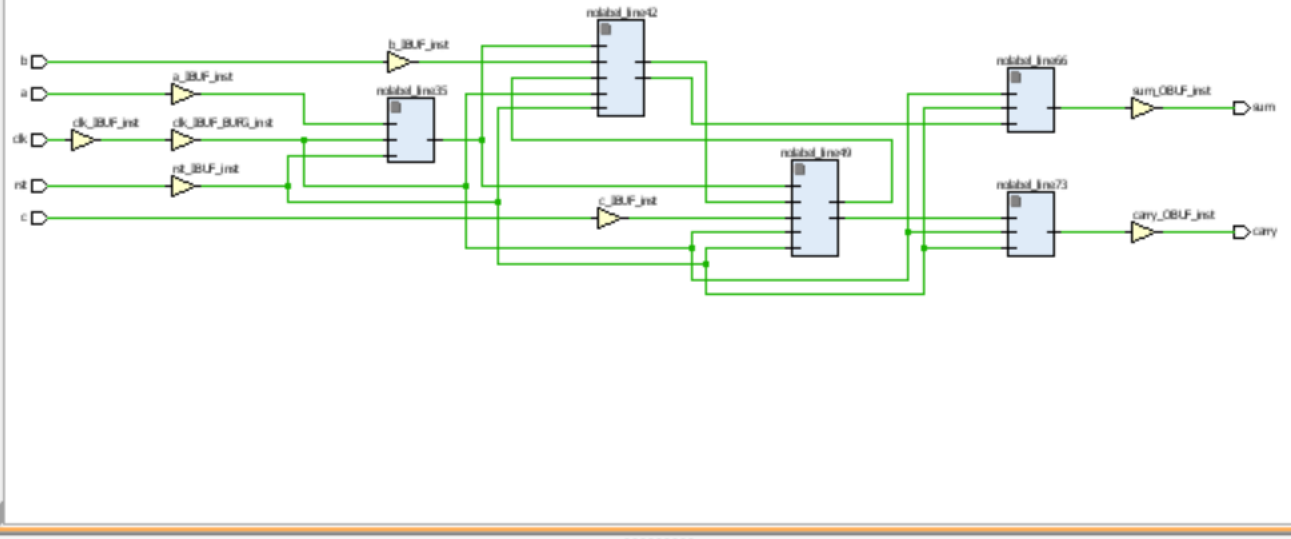
Sour.. Netl..

Pro...

Select an object to see properties

Project Summary | Device | Schematic

13 Cells | 7 I/O Ports | 20 Nets



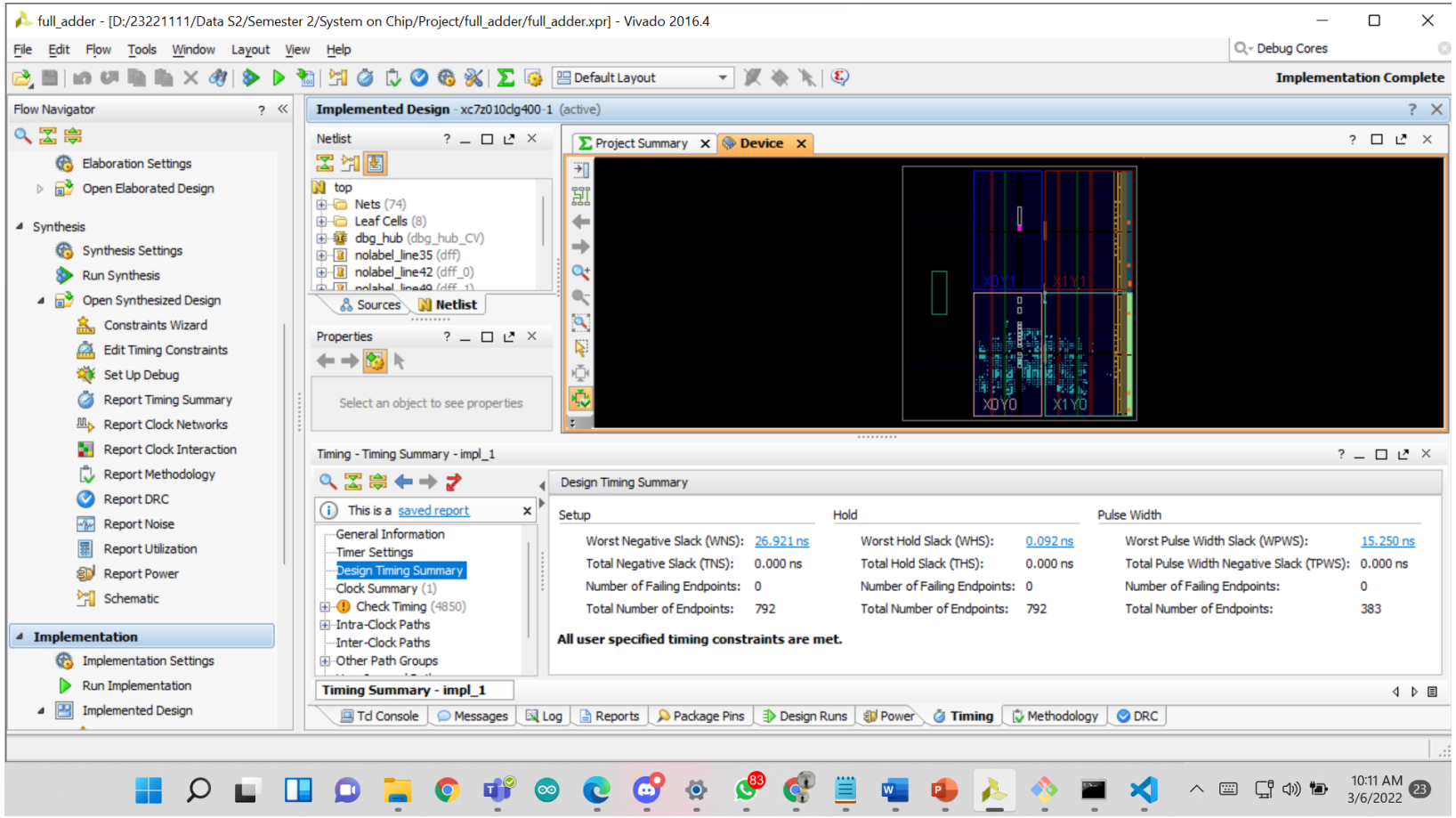
Tcl Console

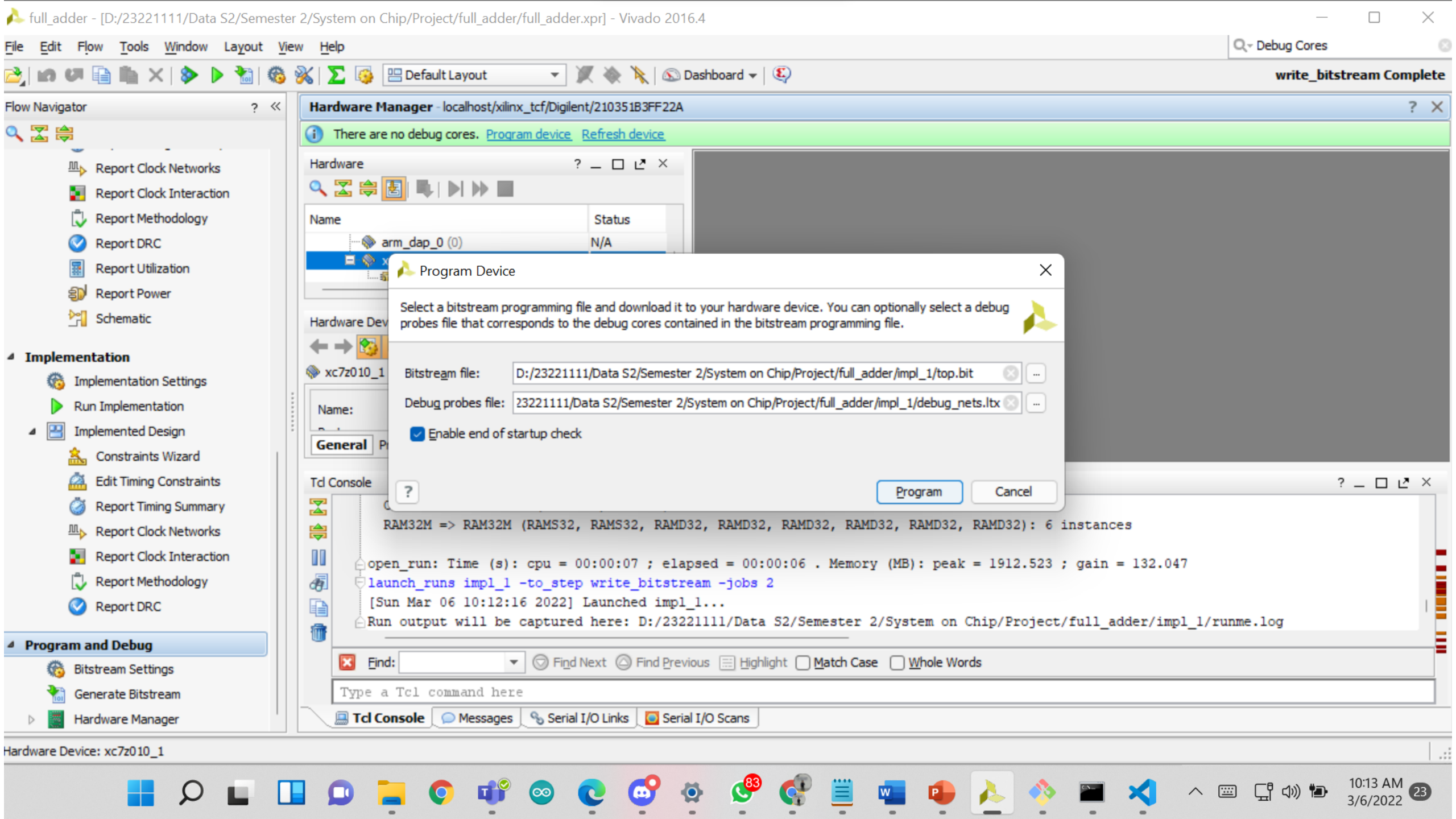
```
INFO: [Project 1-479] Netlist was created with Vivado 2016.4
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.srcs/constrs_1/new/ZYBO_master.xdc]
invalid command name "clk"
Finished Parsing XDC File [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.srcs/constrs_1/new/ZYBO_maste
```

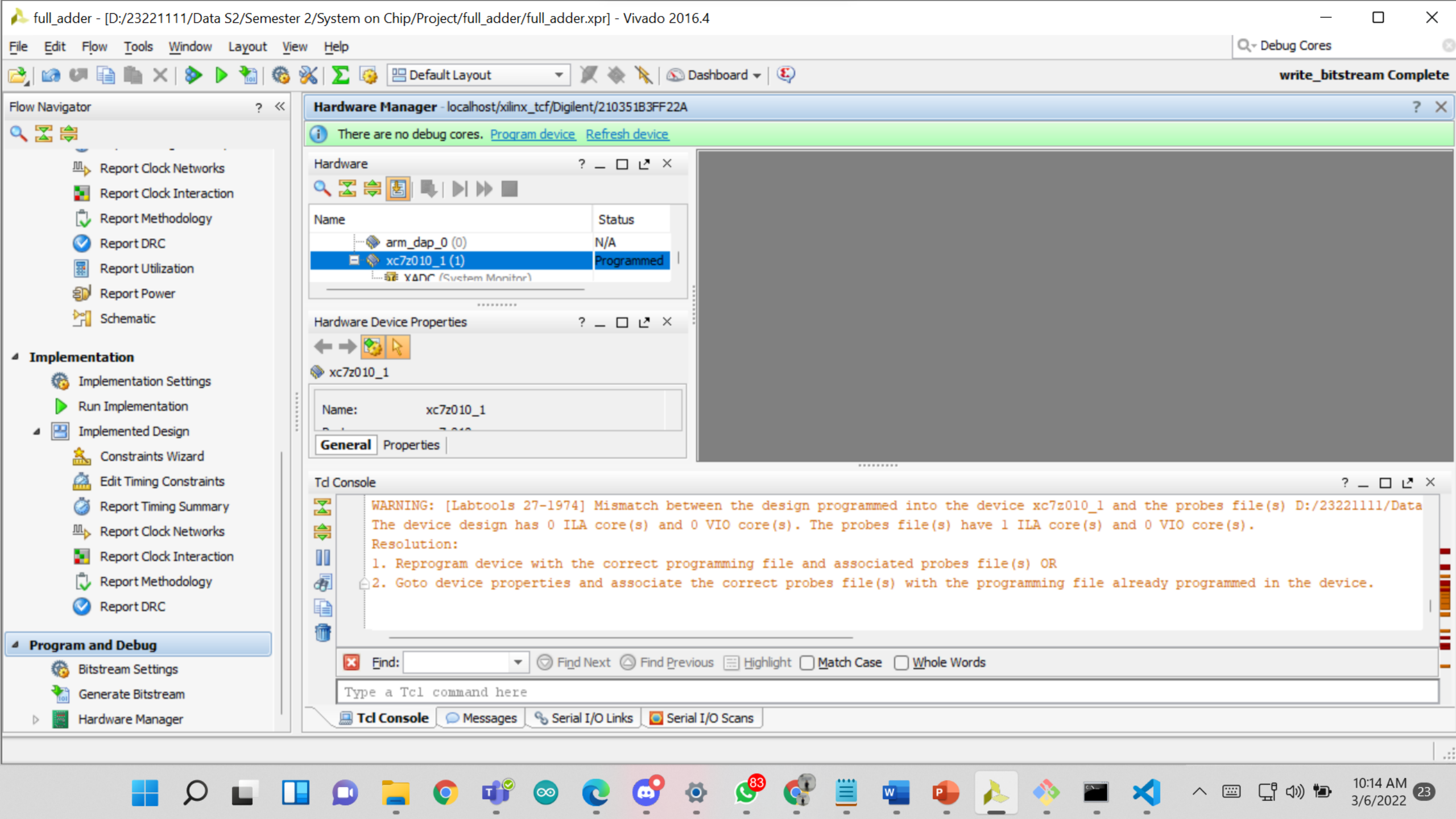
Type a Tcl command here

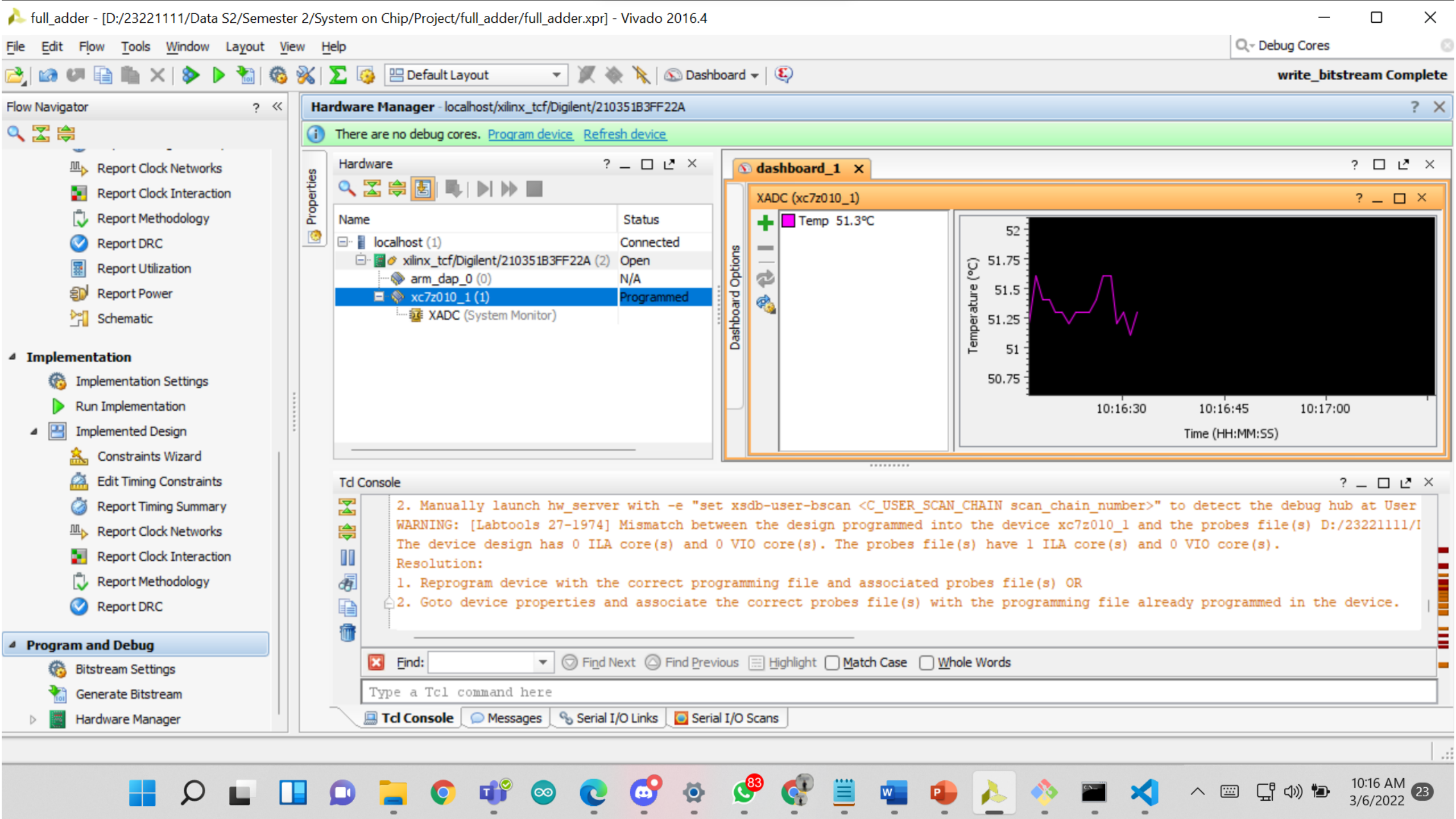
Tcl Console | Messages | Log | Reports | Design Runs

9:52 AM
3/6/2022


full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Debug Cores
Default Layout
Implementation Complete
Flow Navigator
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Implemented Design
Implemented Design - xc7z010clg400-1 (active)
Netlist
top
Nets (74)
Leaf Cells (8)
dbg_hub (dbg_hub_CV)
nolabel_line35 (dff)
nolabel_line42 (dff_0)
Sources
Netlist
Properties
Select an object to see properties
Project Summary
Device
X0Y1
X1Y1
X0Y0
X1Y0
Timing - Timing Summary - impl_1
This is a saved report
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (4850)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Design Timing Summary
Setup
Worst Negative Slack (WNS): 26.921 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 792
Hold
Worst Hold Slack (WHS): 0.092 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 792
Pulse Width
Worst Pulse Width Slack (WPWS): 15.250 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 383
All user specified timing constraints are met.
Timing Summary - impl_1
Tcl Console
Messages
Log
Reports
Package Pins
Design Runs
Power
Timing
Methodology
DRC
10:11 AM
3/6/2022


full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Debug Cores
Default Layout
Dashboard
write_bitstream Complete
Flow Navigator
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Hardware Manager - localhost/xilinx_tcf/Digilent/210351B3FF22A
There are no debug cores. Program device Refresh device
Hardware
Name
Status
arm_dap_0 (0)
N/A
Hardware Dev
xc7z010_1
Name:
General
Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/impl_1/top.bit
Debug probes file:
23221111/Data S2/Semester 2/System on Chip/Project/full_adder/impl_1/debug_nets.ltx
Enable end of startup check
Program
Cancel
Tcl Console
RAM32M => RAM32M (RAMS32, RAMS32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32): 6 instances
open_run: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 1912.523 ; gain = 132.047
launch_runs impl_1 -to_step write_bitstream -jobs 2
[Sun Mar 06 10:12:16 2022] Launched impl_1...
Run output will be captured here: D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/impl_1/runme.log
Find:
Find Next
Find Previous
Highlight
Match Case
Whole Words
Type a Tcl command here
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
Hardware Device: xc7z010_1
10:13 AM
3/6/2022


full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Debug Cores
Default Layout
Dashboard
write_bitstream Complete
Flow Navigator
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Hardware Manager - localhost/xilinx_tcf/Digilent/210351B3FF22A
There are no debug cores. Program device Refresh device
Hardware
Name
Status
arm_dap_0 (0)
N/A
xc7z010_1 (1)
Programmed
Hardware Device Properties
xc7z010_1
Name: xc7z010_1
General
Properties
Tcl Console
WARNING: [Labtools 27-1974] Mismatch between the design programmed into the device xc7z010_1 and the probes file(s) D:/23221111/Data
The device design has 0 ILA core(s) and 0 VIO core(s). The probes file(s) have 1 ILA core(s) and 0 VIO core(s).
Resolution:
1. Reprogram device with the correct programming file and associated probes file(s) OR
2. Goto device properties and associate the correct probes file(s) with the programming file already programmed in the device.
Find:
Find Next
Find Previous
Highlight
Match Case
Whole Words
Type a Tcl command here
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
10:14 AM
3/6/2022


full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Debug Cores
Default Layout
Dashboard
write_bitstream Complete
Flow Navigator
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Hardware Manager - localhost/xilinx_tcf/Digilent/210351B3FF22A
There are no debug cores. Program device Refresh device
Properties
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210351B3FF22A (2)
Open
arm_dap_0 (0)
N/A
xc7z010_1 (1)
Programmed
XADC (System Monitor)
dashboard_1
Dashboard Options
XADC (xc7z010_1)
Temp 51.3°C
52
51.75
51.5
51.25
51
50.75
Temperature (°C)
10:16:30
10:16:45
10:17:00
Time (HH:MM:SS)
Tcl Console
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User
WARNING: [Labtools 27-1974] Mismatch between the design programmed into the device xc7z010_1 and the probes file(s) D:/23221111/I
The device design has 0 ILA core(s) and 0 VIO core(s). The probes file(s) have 1 ILA core(s) and 0 VIO core(s).
Resolution:
1. Reprogram device with the correct programming file and associated probes file(s) OR
2. Goto device properties and associate the correct probes file(s) with the programming file already programmed in the device.
Find:
Find Next
Find Previous
Highlight
Match Case
Whole Words
Type a Tcl command here
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
10:16 AM
3/6/2022