Tutorial 1

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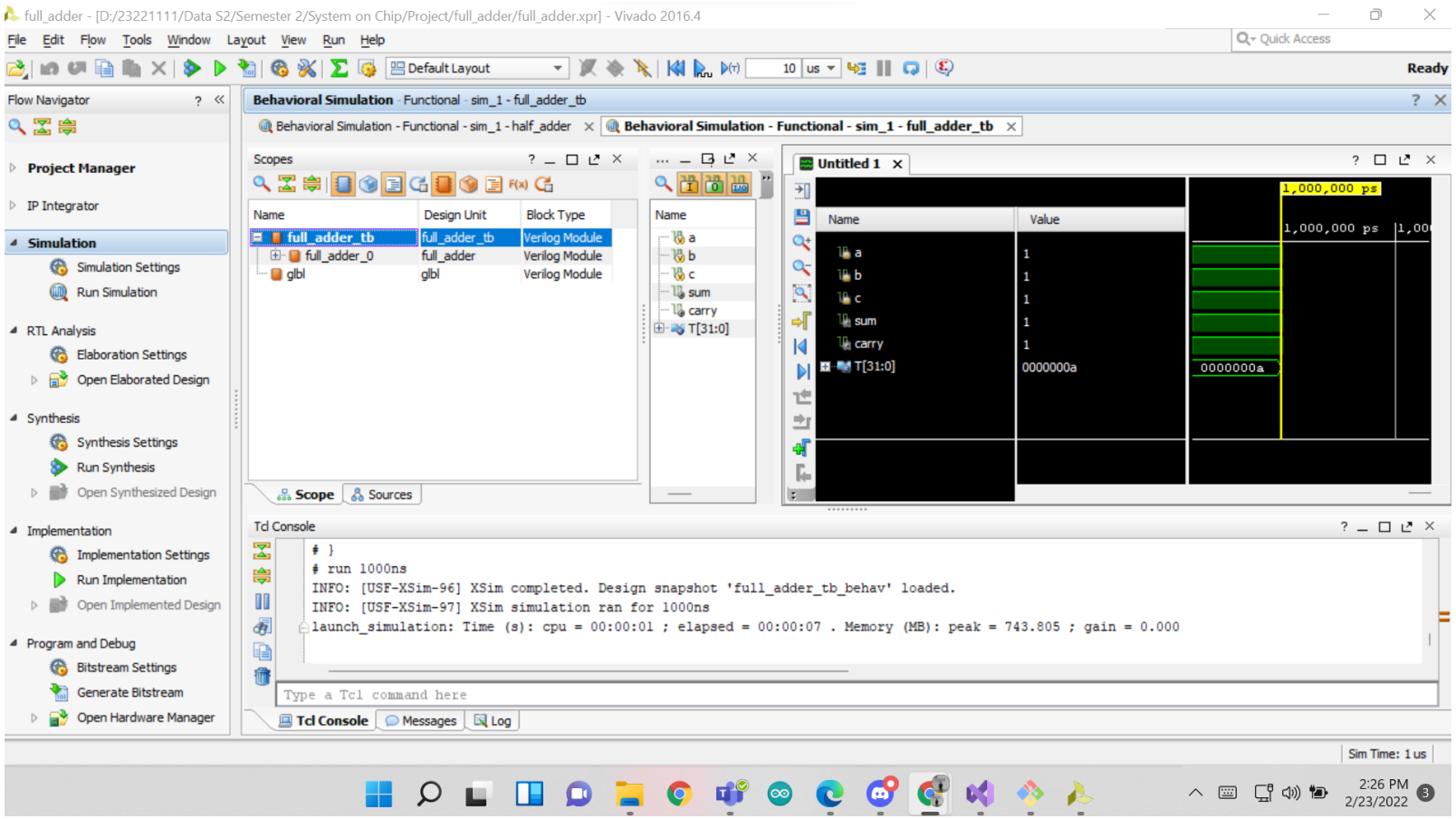
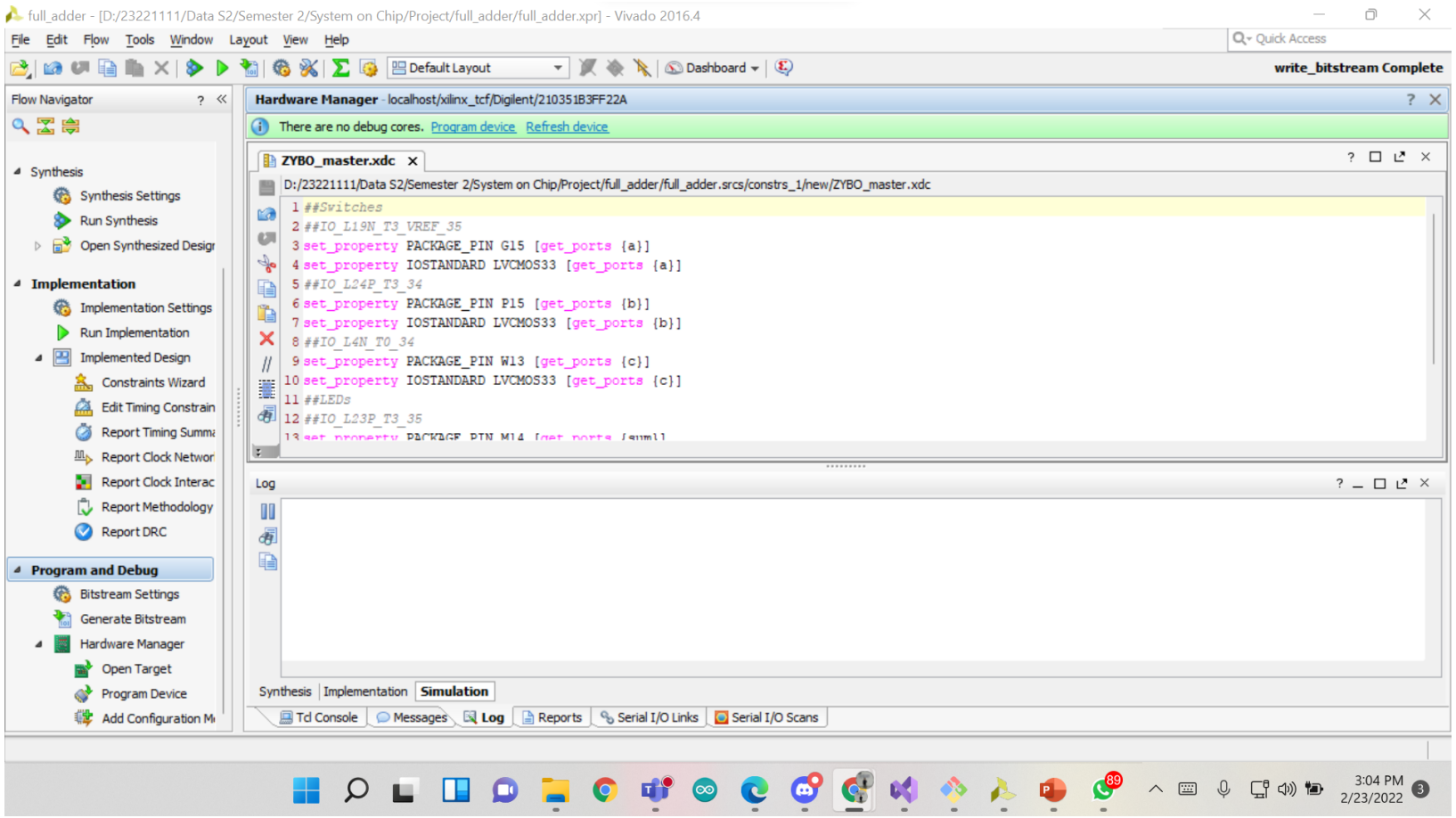

full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
IP Integrator
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Program and Debug
Bitstream Settings
Generate Bitstream
Open Hardware Manager
Behavioral Simulation - Functional - sim_1 - full_adder_tb
Behavioral Simulation - Functional - sim_1 - half_adder
Behavioral Simulation - Functional - sim_1 - full_adder_tb
Scopes
Name
Design Unit
Block Type
full_adder_tb
full_adder_tb
Verilog Module
full_adder_0
full_adder
Verilog Module
glbl
glbl
Verilog Module
Scope
Sources
Untitled 1
Name
Value
a
b
c
sum
carry
T[31:0]
1
1
1
1
1
0000000a
1,000,000 ps
0000000a
Tcl Console
}
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'full_adder_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:01 ; elapsed = 00:00:07 . Memory (MB): peak = 743.805 ; gain = 0.000
Type a Tcl command here
Tcl Console
Messages
Log
Sim Time: 1 us
2:26 PM
2/23/2022


full_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Quick Access
Default Layout
Dashboard
write_bitstream Complete
Flow Navigator
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constrain
Report Timing Summa
Report Clock Networ
Report Clock Interac
Report Methodology
Report DRC
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Open Target
Program Device
Add Configuration M
Hardware Manager - localhost/xilinx_tcf/Digilent/210351B3FF22A
There are no debug cores. Program device Refresh device
ZYBO_master.xdc
D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.srcs/constrs_1/new/ZYBO_master.xdc
1 ##Switches
2 ##IO_L19N_T3_VREF_35
3 set_property PACKAGE_PIN G15 [get_ports {a}]
4 set_property IOSTANDARD LVCMOS33 [get_ports {a}]
5 ##IO_L24P_T3_34
6 set_property PACKAGE_PIN P15 [get_ports {b}]
7 set_property IOSTANDARD LVCMOS33 [get_ports {b}]
8 ##IO_L4N_T0_34
9 set_property PACKAGE_PIN W13 [get_ports {c}]
10 set_property IOSTANDARD LVCMOS33 [get_ports {c}]
11 ##LEDs
12 ##IO_L23P_T3_35
Log
Synthesis Implementation Simulation
Tcl Console Messages Log Reports Serial I/O Links Serial I/O Scans
3:04 PM
2/23/2022