



# Tutorial 2

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# Lanjutan Tutorial Modul 1

full\_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full\_adder/full\_adder.xpr] - Vivado 2016.4

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Open Hardware Manager
  - Open Target
  - Program Device
  - Add Configuration Memory

Project Manager - full\_adder

Sources

- Design Sources (1)
  - full\_adder (full\_adder.v) (2)
- Constraints (1)
- Simulation Sources (2)

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Project Summary

Project Settings

Project name: full\_adder

Project location: D:/23221111/Data S2/Semester 2/System on Chip/Project/full\_adder

Product family: Zynq-7000

Project part: xc7z010clg400-1

Top module name: full\_adder

Target language: Verilog

Simulator language: Mixed

Synthesis

Status: Complete

Implementation

Status: Complete

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCIE %	Start
synth_1	constrs_1	synth_design Complete!								1	0	0	0	0.000	
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	2.845	0	1	0	0	0	0.000	

Td Console Messages Log Reports Design Runs

9:20 AM 3/6/2022

# Open Implemented Design

The screenshot shows the Vivado 2016.4 IDE with the following components:

- Flow Navigator (Left):** A tree view showing the project workflow. The 'Implementation' section is selected, with 'Open Implemented Design' highlighted.
- Implemented Design - xc7z010dgc400-1 (active):** The main design view. It shows a netlist with components like 'top', 'Nets (20)', 'Leaf Cells (8)', and several 'nolabel\_line' components. Below the netlist is a 'Properties' panel.
- Physical Implementation:** A window showing the physical layout of the design on the device, with components like 'X0 Y0', 'X0 Y1', 'X1 Y0', and 'X1 Y1' visible.
- Design Timing Summary - impl\_1:** A report window showing timing analysis results. It includes a table with columns for Setup, Hold, and Pulse Width, and rows for various timing metrics.

**Design Timing Summary - impl\_1**

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

There are no user specified timing constraints.



Default Layout

Synthesis Complete

## Flow Navigator



? &lt;&lt;

- Elaboration Settings
- Open Elaborated Design

## Synthesis

- Synthesis Settings
- Run Synthesis
- Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

## Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

## Synthesized Design - xc7z010dg400-1 (active)

Net... ? - □ &lt; &gt; ×



- top
  - Nets (20)
  - Leaf Cells (8)
  - nolabel\_line35 (dff)
  - nolabel\_line42 (dff)
  - nolabel\_line49 (dff)
  - nolabel\_line66 (dff)
  - nolabel\_line73 (dff)

Sour... Netl...

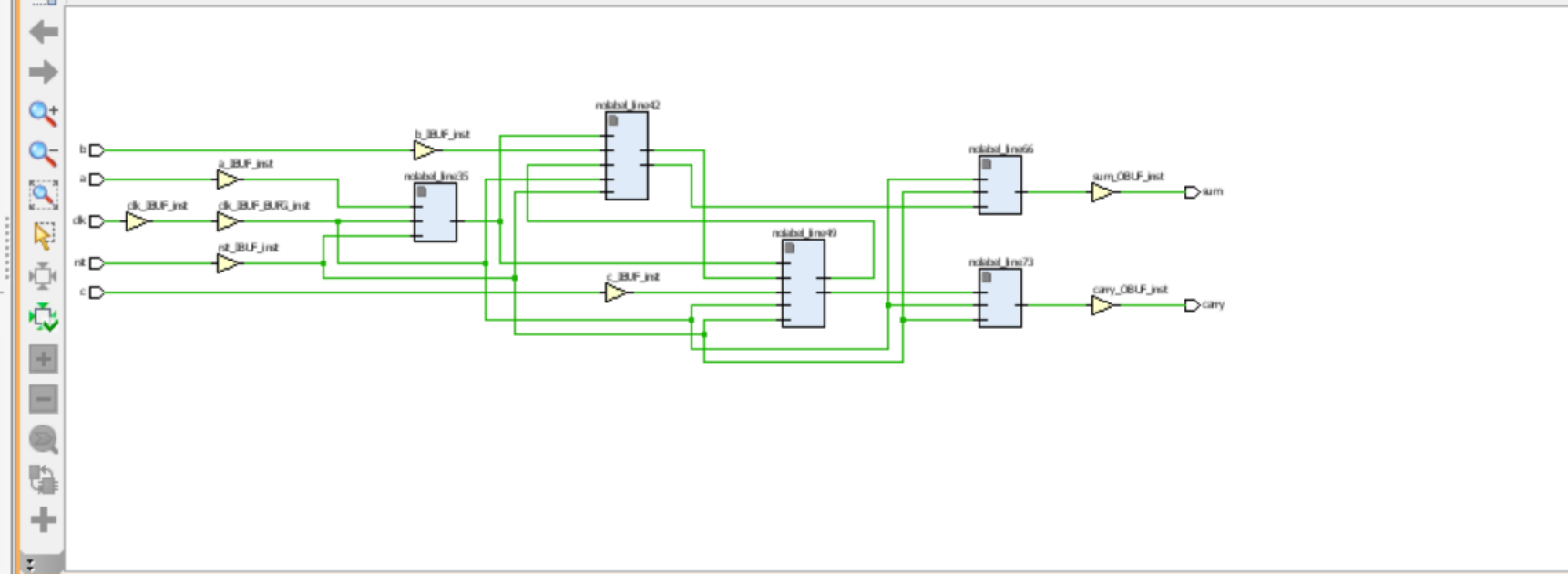
Pro... ? - □ &lt; &gt; ×



Select an object to see properties

Project Summary x Device x Schematic x

13 Cells 7 I/O Ports 20 Nets



## Tcl Console

```
INFO: [Project 1-479] Netlist was created with Vivado 2016.4
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.srscs/constrs_1/new/ZYBO_master.xdc]
invalid command name "clk"
Finished Parsing XDC File [D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/full_adder.srscs/constrs_1/new/ZYBO_master.xdc]
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

full\_adder - [D:/23221111/Data S2/Semester 2/System on Chip/Project/full\_adder/full\_adder.xpr] - Vivado 2016.4

File Edit Flow Tools Window Layout View Help

Default Layout

Implementation Complete

Flow Navigator

- Elaboration Settings
- Open Elaborated Design
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  - Synthesis Settings
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    - Constraints Wizard
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    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- Implementation
  - Implementation Settings
  - Run Implementation
  - Implemented Design

Implemented Design - xc7z010dgg400-1 (active)

Netlist

- top
  - Nets (74)
  - Leaf Cells (8)
  - dbg\_hub (dbg\_hub\_CV)
  - nolabel\_line35 (dff)
  - nolabel\_line42 (dff\_0)
  - nolabel\_line40 (dff\_1)

Sources Netlist

Properties

Select an object to see properties

Project Summary Device

Timing - Timing Summary - impl\_1

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <a href="#">26.921 ns</a>	Worst Hold Slack (WHS): <a href="#">0.092 ns</a>	Worst Pulse Width Slack (WPWS): <a href="#">15.250 ns</a>
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 792	Total Number of Endpoints: 792	Total Number of Endpoints: 383

All user specified timing constraints are met.

Timing Summary - impl\_1

Td Console Messages Log Reports Package Pins Design Runs Power Timing Methodology DRC

10:11 AM 3/6/2022

## Flow Navigator

- Report Clock Networks
- Report Clock Interaction
- Report Methodology
- Report DRC
- Report Utilization
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- Schematic

## Implementation

- Implementation Settings
- Run Implementation
- Implemented Design
  - Constraints Wizard
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## Program and Debug

- Bitstream Settings
- Generate Bitstream
- Hardware Manager

## Hardware Manager - localhost/xilinx\_tcf/Digilent/210351B3FF22A

There are no debug cores. [Program device](#) [Refresh device](#)

## Hardware

Name	Status
arm_dap_0 (0)	N/A

## Hardware Dev

xc7z010\_1

Name:

General

## Tcl Console

```
RAM32M => RAM32M (RAMS32, RAMS32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32): 6 instances  
open_run: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 1912.523 ; gain = 132.047  
launch_runs impl_1 -to_step write_bitstream -jobs 2  
[Sun Mar 06 10:12:16 2022] Launched impl_1...  
Run output will be captured here: D:/23221111/Data S2/Semester 2/System on Chip/Project/full_adder/impl_1/runme.log
```

Find: Find Next Find Previous Highlight Match Case Whole Words

Type a Tcl command here

Tcl Console Messages Serial I/O Links Serial I/O Scans

Hardware Device: xc7z010\_1



## Flow Navigator

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- Implementation Settings
- Run Implementation
- Implemented Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC

## Program and Debug

- Bitstream Settings
- Generate Bitstream
- Hardware Manager

## Hardware Manager - localhost/xilinx\_tcf/Digilent/210351B3FF22A

There are no debug cores. [Program device](#) [Refresh device](#)

## Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z010_1 (1)	Programmed
YADC (System Monitor)	

## Hardware Device Properties

xc7z010\_1

Name: xc7z010\_1

General Properties

## Tcl Console

WARNING: [Labtools 27-1974] Mismatch between the design programmed into the device xc7z010\_1 and the probes file(s) D:/23221111/Data. The device design has 0 ILA core(s) and 0 VIO core(s). The probes file(s) have 1 ILA core(s) and 0 VIO core(s).  
Resolution:  
1. Reprogram device with the correct programming file and associated probes file(s) OR  
2. Goto device properties and associate the correct probes file(s) with the programming file already programmed in the device.

Find: Find Next Find Previous Highlight Match Case Whole Words

Type a Tcl command here

Tcl Console Messages Serial I/O Links Serial I/O Scans

## Flow Navigator

- Report Clock Networks
- Report Clock Interaction
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## Implementation

- Implementation Settings
- Run Implementation
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  - Constraints Wizard
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  - Report Methodology
  - Report DRC

## Program and Debug

- Bitstream Settings
- Generate Bitstream
- Hardware Manager

## Hardware Manager - localhost/xilinx\_tcf/Digilent/210351B3FF22A

There are no debug cores. [Program device](#) [Refresh device](#)

## Properties

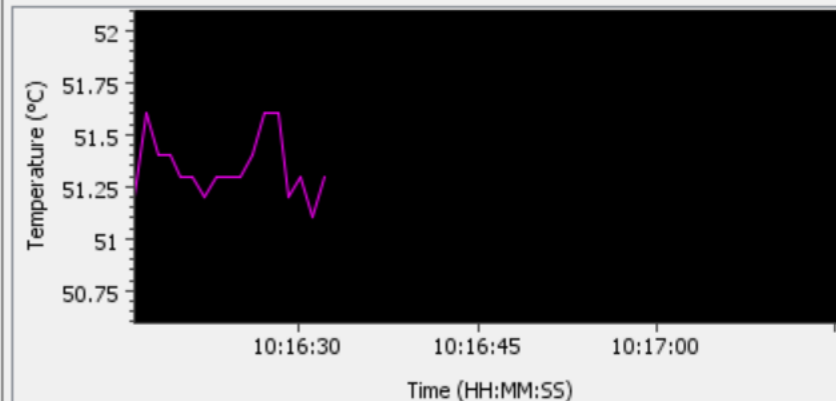
## Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210351B3FF22A (2)	Open
arm_dap_0 (0)	N/A
xc7z010_1 (1)	Programmed
XADC (System Monitor)	

## dashboard\_1

## XADC (xc7z010\_1)

Temp 51.3°C



## Tcl Console

```
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User
WARNING: [Labtools 27-1974] Mismatch between the design programmed into the device xc7z010_1 and the probes file(s) D:/23221111/1
The device design has 0 ILA core(s) and 0 VIO core(s). The probes file(s) have 1 ILA core(s) and 0 VIO core(s).
Resolution:
1. Reprogram device with the correct programming file and associated probes file(s) OR
2. Goto device properties and associate the correct probes file(s) with the programming file already programmed in the device.
```

Find:  Find Next Find Previous Highlight Match Case Whole Words

Type a Tcl command here

Tcl Console Messages Serial I/O Links Serial I/O Scans